A31G213, A31G212

32-bit Cortex-M0+ based General Purpose Microcontroller With Touch & LED Driver

Datasheet Version 1.08

Feature

Core

- ARM Cortex-M0+ Core
- Maximum operating frequency: up to 48MHz

Memories

- 64/32KB code flash memory
- 6KB SRAM

Clock, reset and power management

- Two main operating clocks: HCLK, PCLK
  - Real time clock and calendar
- Two system reset: cold reset, warm reset
- Power management mode: Run mode, Sleep mode, Power Down mode

Interrupt management

- Nested vector interrupt controller (NVIC) with 32 interrupt sources

Timers

- Watchdog Timer
- 16-bit 4ch general purpose timers
  - Periodic, one-shot, PWM, capture mode
- 32-bit 2ch general purpose timers
  - Periodic, one-shot, PWM, capture mode
- 16-bit 6ch PWM timers

Communication interfaces

- External communication ports
  - 2 USART (UART + SPI), 2 UARTs,
  - 2 SPIs, 2 I2Cs

12-bit ADC

- 14-channels inputs

Capacitive Touch Switch

- 48-Pin: 24-ch

LED driver

- 10 segments and 16 commons

CRC generator

- CRC-CCITT, CRC-16

Development support

- SWD debug interface

Package

- 48-pin LQFP (7 x 7, 0.5mm pitch)
- 44-pin MQFP (10 x 10, 0.8mm pitch)
- 32-pin LQFP (7 x 7, 0.8mm pitch)
- 32-pin QFN (5 x 5, 0.5mm pitch)
- 28-pin TSSOP (9.7x 4.4, 0.65mm pitch)

Operating Voltage

- 1.8V to 5.5V

Operating temperature

- Commercial grade (-40℃ to +85℃)
- Industrial grade (-40℃ to +105)

Product selection table

Part Number	Flash	SRAM	UART	USART	SPI	I2C	TIMER	PWM	ADC	I/O Ports	Package
A31G213CL	64KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	14	44	LQFP-48
A31G213SQ*	64KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	12	40	MQFP-44
A31G213KU*	64KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	QFN-32
A31G213KN*	64KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	LQFP-32
A31G213GR*	64KB	6KB	2	1	1	2	4(16bit)/2(32bit)	6	6	24	TSSOP-28
A31G212CL*	32KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	14	44	LQFP-48
A31G212SQ*	32KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	12	40	MQFP-44
A31G212KN*	32KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	LQFP-32
A31G212KU*	32KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	QFN-32
A31G212GR*	32KB	6KB	2	1	1	2	4(16bit)/2(32bit)	6	6	24	TSSOP-28

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.

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1 Description

A31G21x lines are 32-bit general purpose microcontrollers with up to 64 Kbytes of flash memory.

In this section, features of A31G21x and peripheral counts are introduced.

Table 1. A31G213 and A31G212 Device Features and Peripheral Counts

Classification	Module/ Peripherals	Description
Core	CPU	• ARM Cortex-M0+ Core Maximum operating frequency: up to 48MHz
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 32 peripheral interrupts supported
Memory	Code Flash	• A31G213 64KB Code Flash Memory • A31G212 32KB Code Flash Memory
	SRAM	• 6KB SRAM
System Control Units (SCU)	Operating frequency	• Up to 48 MHz
	Clock	• High Speed Internal oscillator (HSI) : 32MHz, • Low Speed Internal oscillator (LSI) : 500KHz • External oscillator(HSE) : 2MHz ~16MHz • External sub-oscillator (LSE) : 32.768 KHz • Phase-locked loop (PLL) frequency generator Generates a high-speed clock (up to 48 MHz)
	Clock Monitoring	• System Fail-Safe function by Clock Monitoring External oscillator(HSE) External sub-oscillator (LSE) Main system clock (MCLK)
	Operating Mode	• RUN mode • SLEEP mode • Power-Down mode
	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power-On Reset) • LVR (Low Voltage-Reset) • Reset due to clock oscillating error

Table 1. A31G213 and A31G212 Device Features and Peripheral Counts (continued)

Classification	Module/ Peripherals	Description
Timer	TIMER1x	• 16-bit : 4-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
	Timer2x	• 32-bit : 2-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
PWM	Timer3x	• 16-bit : 6-ch Periodic timer mode, Back-to-Back mode, Capture mode
Communication function	USART	• 48-pin, 44-Pin, 32-pin : 2-ch 28-pin : 1-ch
	UART	• 2 channels
	SPI	• 48-pin, 44-pin : 2 channels 32-pin, 28-pin : 1 channel
	I2C	• 2 channels
A/D converter		•12-bit ADC : 150ksps 48-pin : 14-ch 44-pin : 12-ch 32-pin : 8-ch 28-pin : 6-ch
D/A converter		• 1 channel • 5-bit resolution
Capacitive Touch Switch		• Capacitive Touch Switch 48-Pin : 24-ch 44-Pin : 21-ch 32-Pin : 13-ch 28-Pin : 11-ch
LED Driver		• 10 SEG x 16 COM LED Driver
CRC calculator		• CRC-CCITT, CRC-16
Operating Voltage		• 1.8V ~ 5.5V
Operating temperature		• Commercial grade (-40℃ ~ +85℃) • Industrial grade (-40℃ ~ +105℃)
Package		• Four types of package options 48-pin LQFP (7 x 7, 0.5mm pitch) 44-pin MQFP (10 x 10, 0.8mm pitch) 32-pin LQFP (7 x 7, 0.8mm pitch) 32-pin QFN (5 x 5, 0.5mm pitch) 28-pin TSSOP (9.7x 4.4, 0.65mm pitch)

1.1 Block diagram

In Figure 1, A31G21x series with peripherals is described in block diagram.

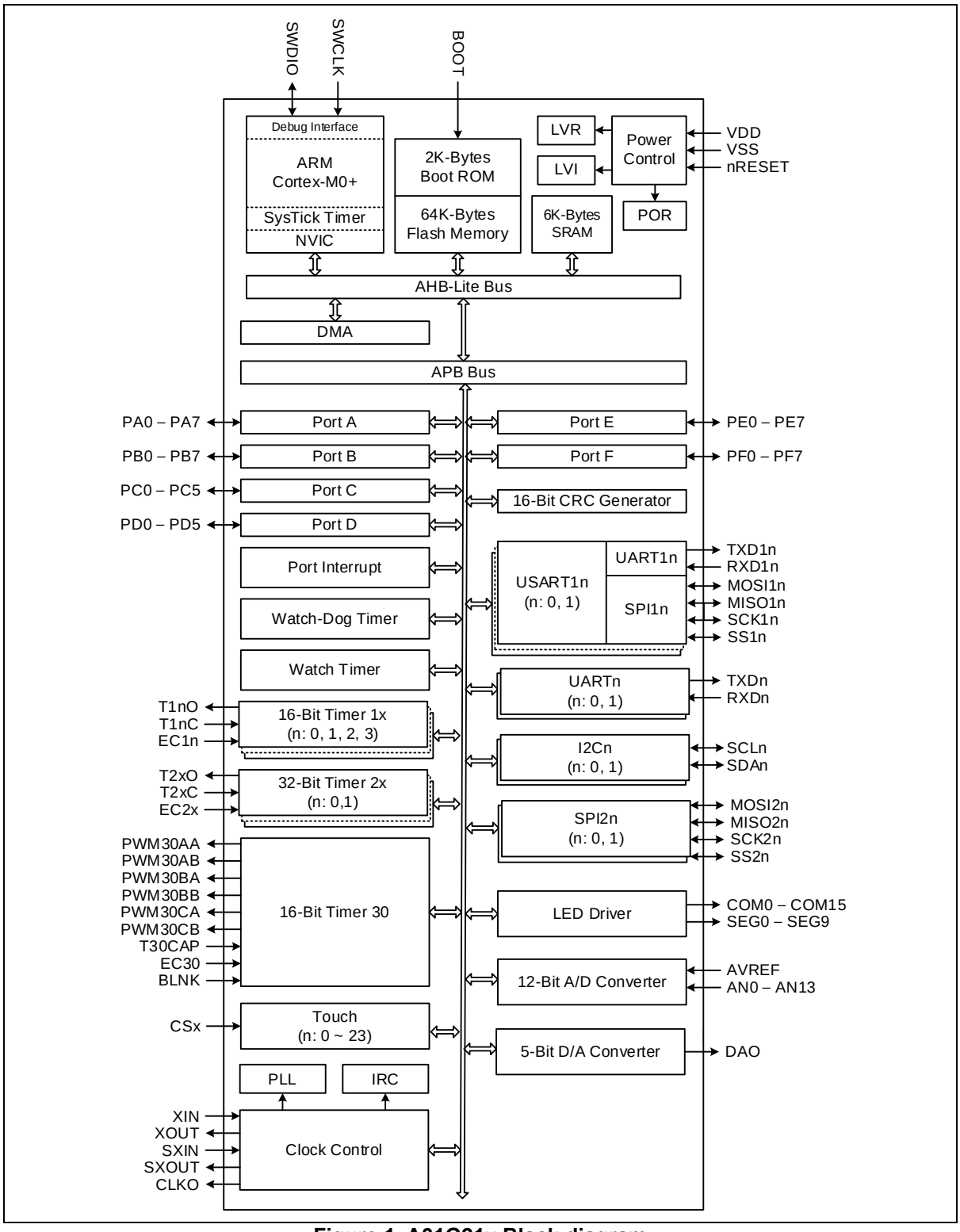


Figure 1. A31G21x Black diagram

2 Pinouts and pin descriptions

In this chapter, A31G21x devices pinouts and pin descriptions are introduced.

2.1 Pinouts

2.1.1 A31G212CLN, A31G213CLN, A31G212CL2N, A31G213CL2N (48-LQFP)

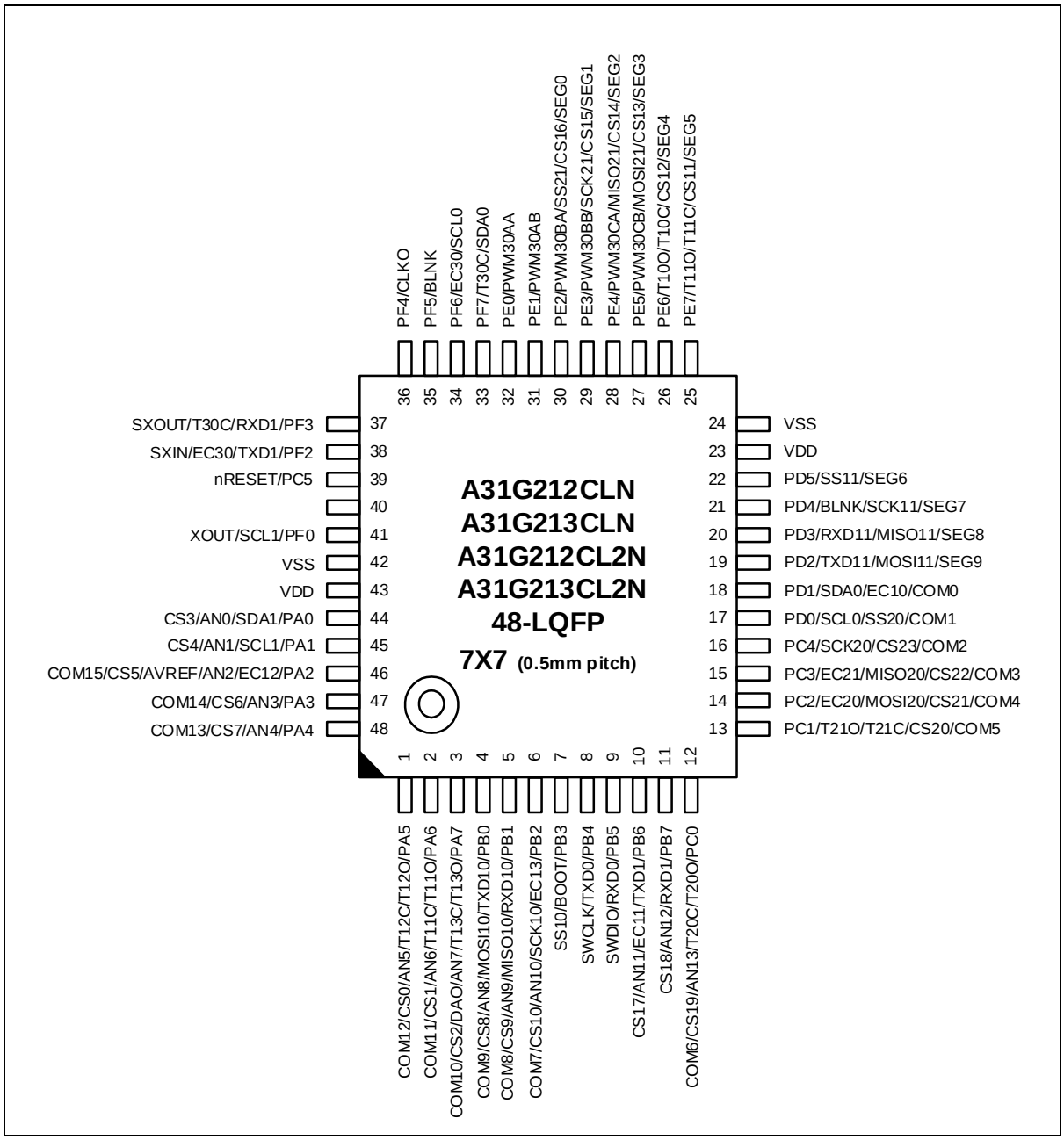


Figure 2. LQFP 48 Pinouts

2.1.2 A31G212SQN, A31G213SQN, A31G212SQ2N, A31G213SQ2N (44-MQFP)

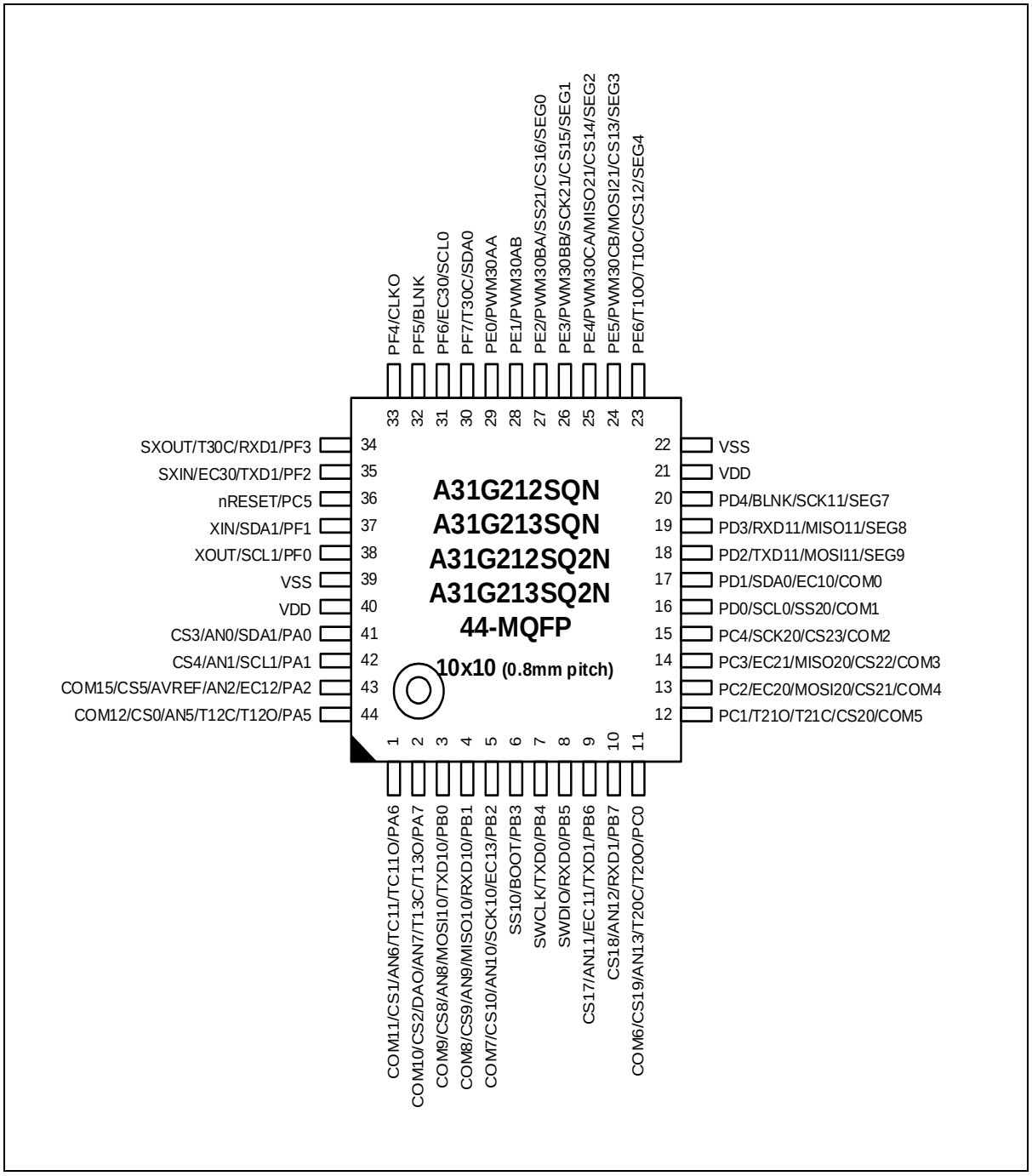


Figure 3. MQFP 44 Pinouts

2.1.3 A31G212KNN, A31G213KNN, A31G212KN2N, A31G213KN2N (32-LQFP)

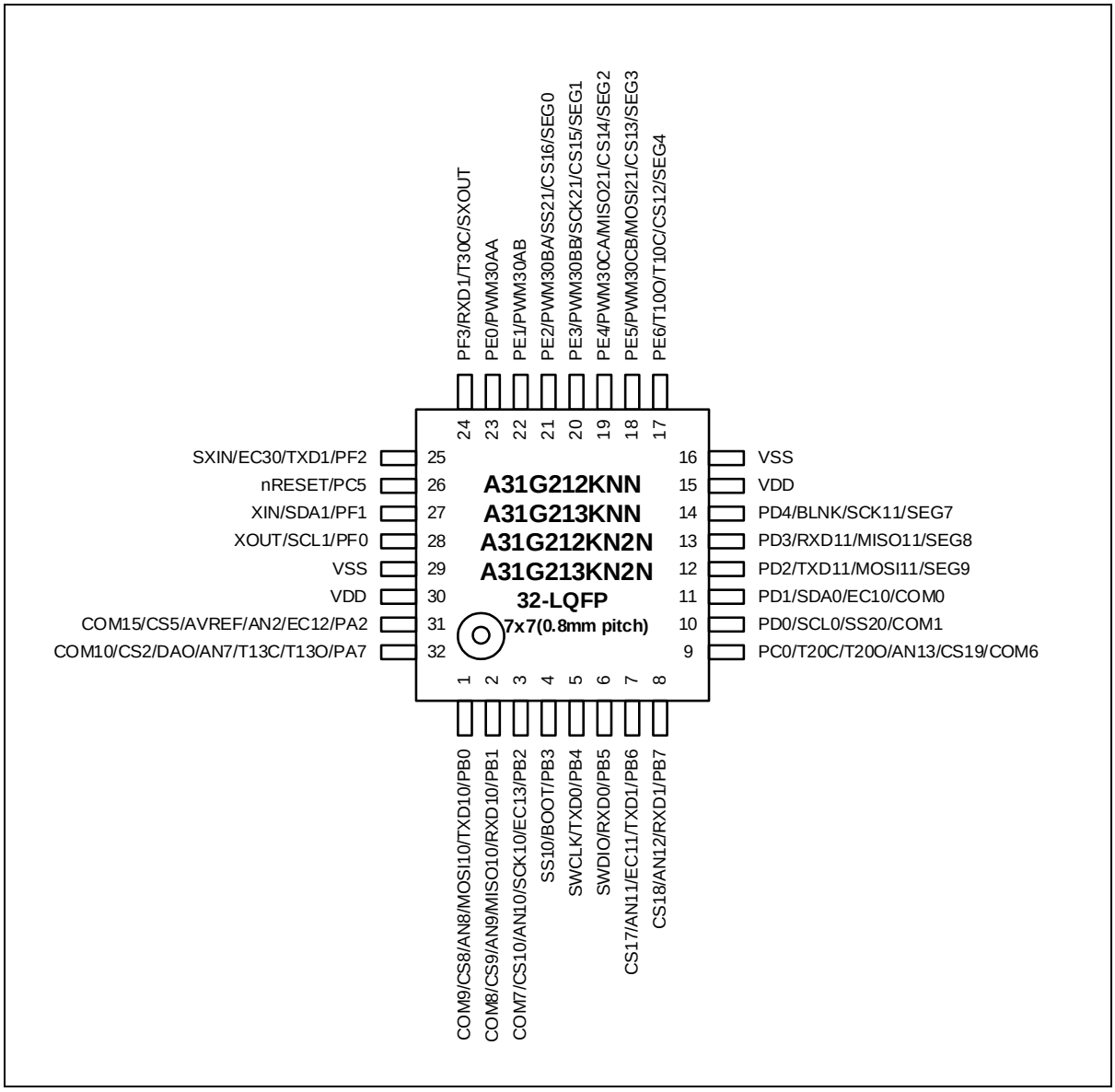


Figure 4. LQFP 32 Pinouts

2.1.4 A31G212KUN, A31G213KUN, A31G212KU2N, A31G213KU2N (32-QFN)

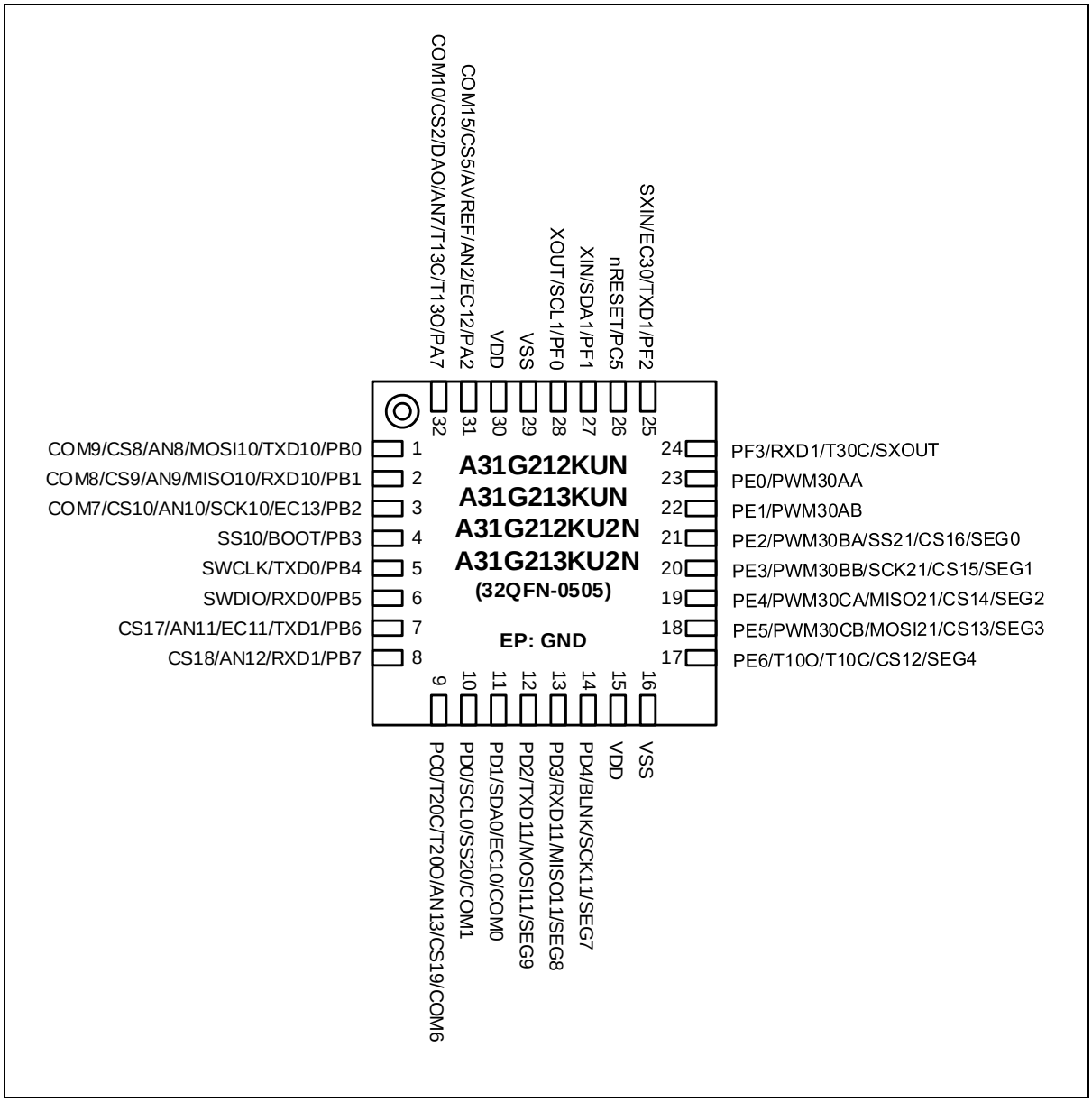


Figure 5. QFN 32 Pinouts

2.1.5 A31G212GRN, A31G213GRN, A31G212GR2N, A31G213GR2N (28-TSSOP)

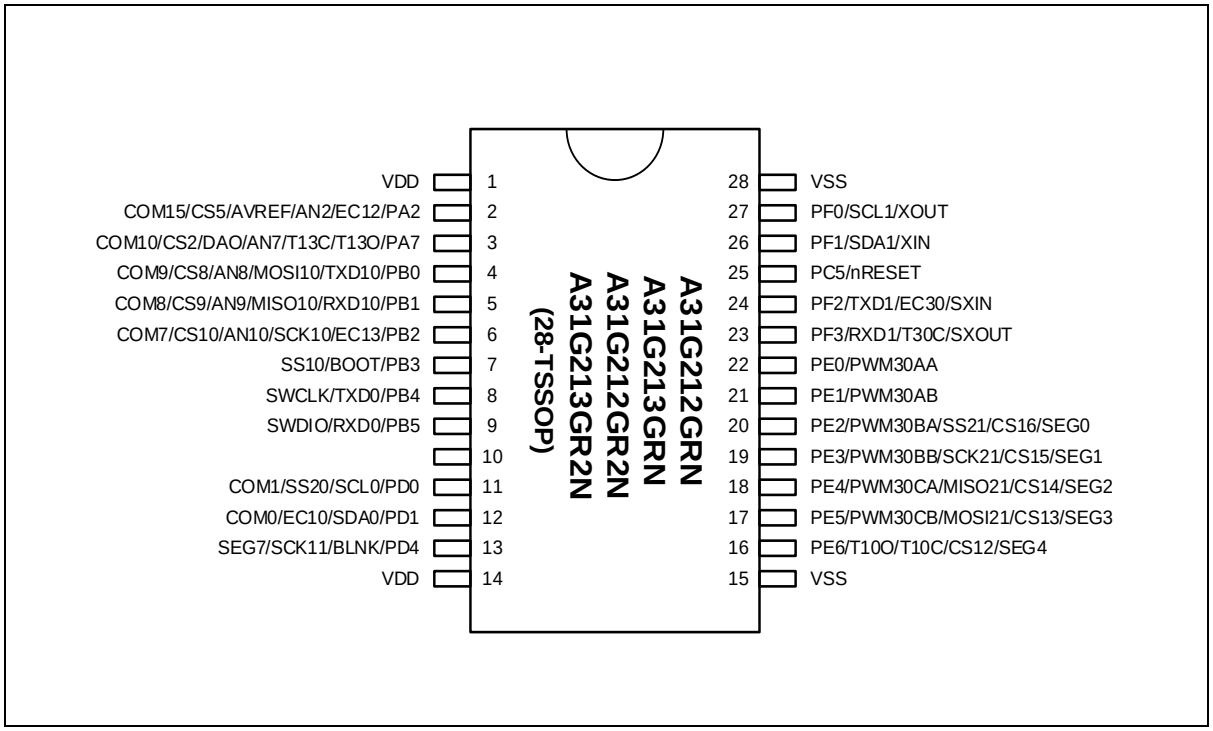


Figure 6. TSSOP 28 Pinouts

2.2 Pin description

Pin configuration information in Table 2 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to ten selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 2. Pin Description

Pin No				Pin Name	Type	Description	Remark
48	44	32	28				
1	44	-	-	PA5*	IOUDS	PORT A Bit 5 Input/Output	
				T12O	O	Timer 12 Output	
				T12C	I	Timer 12 Clock/Capture Input	
				AN5	IA	Analog Input 5	
				CS0	IA	Capacitive Touch switch input 0	
				COM12	O	LED Common Signal 12 Output	
2	1	-	-	PA6*	IOUDS	PORT A Bit 6 Input/Output	
				T11O	O	Timer 11 Output	
				T11C	I	Timer 11 Clock/Capture Input	
				AN6	IA	Analog Input 6	
				CS1	IA	Capacitive Touch switch input 1	
				COM11	O	LED Common Signal 11 Output	
3	2	32	3	PA7*	IOUDS	PORT A Bit 7 Input/Output	
				T13O	O	Timer 13 Output	
				T13C	I	Timer 13 Clock/Capture Input	
				AN7	IA	Analog Input 7	
				DAO	OA	Digital to analog output	
				CS2	IA	Capacitive Touch switch input 2	
				COM10	O	LED Common Signal 10 Output	
4	3	1	4	PB0	IOUDS	PORT B Bit 0 Input/Output	
				TXD10*	O	UART Channel 10 TxD Input	
				MOSI10	I/O	SPI Channel 10 Master Out / Slave In	
				AN8	IA	Analog Input 8	
				CS8	IA	Capacitive Touch switch input 8	
				COM9	O	LED Common Signal 9 Output	
5	4	2	5	PB1	IOUDS	PORT B Bit 1 Input/Output	
				RXD10*	I	UART Channel 10 RxD Input	
				MISO10	I/O	SPI10 Master-Input/Slave-Output Data signal	
				AN9	IA	Analog Input 9	
				CS9	IA	Capacitive Touch switch input 9	
				COM8	O	LED Common Signal 8 Output	
6	5	3	6	PB2*	IOUDS	PORT B Bit 2 Input/Output	
				EC13	I	Timer 13 Event Count Input	
				SCK10	I/O	SPI10 Data Clock Input/Output	
				AN10	IA	Analog Input 10	
				CS10	IA	Capacitive Touch switch input 10	
				COM7	O	LED Common Signal 7 Output	
7	6	4	7	PB3	IOUDS	PORT B Bit 3 Input/Output	
				BOOT*	I	Boot mode Selection Input	Pull-up
				SS10	I/O	SPI Channel 10 Slave Select signal	

Table 2. Pin Description (continued)

Pin No				Pin Name	Type	Description	Remark
48	44	32	28				
8	7	5	8	PB4	IOUDS	PORT B Bit 4 Input/Output	
				TXD0	O	UART Channel 0 TxD Input	
				SWCLK*	I	SWD Clock Input	Pull-up
9	8	6	9	PB5	IOUDS	PORT B Bit 5 Input/Output	
				RXD0	I	UART Channel 0 RxD Input	
				SWDIO*	I/O	SWD Data Input/Output	Pull-up
10	9	7	-	PB6*	IOUDS	PORT B Bit 6 Input/Output	
				TXD1	O	UART Channel 1 TxD Input	
				EC11	I	Timer 11 Event Count Input	
				AN11	IA	Analog Input 11	
				CS17	IA	Capacitive Touch switch input 17	
11	10	8	-	PB7*	IOUDS	PORT B Bit 7 Input/Output	
				RXD1	I	UART Channel 1 RxD Input	
				AN12	IA	Analog Input 12	
				CS18	IA	Capacitive Touch switch input 18	
12	11	9	10	PC0*	IOUDS	PORT C Bit 0 Input/Output	
				T20O	O	Timer 20 Output	
				T20C	I	Timer 20 Clock/Capture Input	
				AN13	IA	Analog Input 13	
				CS19	IA	Capacitive Touch switch input 19	
				COM6	O	LED Common Signal 6 Output	
13	12	-	-	PC1*	IOUDS	PORT C Bit 1 Input/Output	
				T21O	O	Timer 21 Output	
				T21C	I	Timer 21 Clock/Capture Input	
				CS20	IA	Capacitive Touch switch input 20	
				COM5	O	LED Common Signal 5 Output	
14	13	-	-	PC2*	IOUDS	PORT C Bit 2 Input/Output	
				EC20	I	Timer 20 Event Count Input	
				MOSI20	I/O	SPI Channel 20 Master Out / Slave In	
				CS21	IA	Capacitive Touch switch input 21	
				COM4	O	LED Common Signal 4 Output	
15	14	-	-	PC3*	IOUDS	PORT C Bit 3 Input/Output	
				EC21	I	Timer 21 Event Count Input	
				MISO20	I/O	SPI20 Master-Input/Slave-Output Data signal	
				CS22	IA	Capacitive Touch switch input 22	
				COM3	O	LED Common Signal 3 Output	
16	15	-	-	PC4*	IOUDS	PORT C Bit 4 Input/Output	
				SCK20	I/O	SPI20 Data Clock Input/Output	
				CS23	IA	Capacitive Touch switch input 23	
				COM2	O	LED Common Signal 2 Output	

Table 2. Pin Description (continued)

Pin No				Pin Name	Type	Description	Remark
48	44	32	28				
17	16	10	11	PD0*	IOUDS	PORT D Bit 0 Input/Output	
				SCL0	O	I²C Channel 0 SCL In/Out	
				SS20	I/O	SPI Channel 20 Slave Select signal	
				COM1	O	LED Common Signal 1 Output	
18	17	11	12	PD1*	IOUDS	PORT D Bit 1 Input/Output	
				SDA0	O	I²C Channel 0 SDA In/Out	
				EC10	I	Timer 10 Event Count Input	
				COM0	O	LED Common Signal 0 Output	
19	18	12	-	PD2*	IOUDS	PORT D Bit 2 Input/Output	
				TXD11	O	UART Channel 11 TxD Input	
				MOSI11	I/O	SPI Channel 11 Master Out / Slave In	
				SEG9	O	LED Segment Signal 9 Output	
20	19	13	-	PD3*	IOUDS	PORT D Bit 3 Input/Output	
				RXD11	I	UART Channel 11 RxD Input	
				MISO11	I/O	SPI11 Master-Input/Slave-Output Data signal	
				SEG8	O	LED Segment Signal 8 Output	
21	20	14	13	PD4*	IOUDS	PORT D Bit 4 Input/Output	
				BLNK	I	External Sync Signal Input for T30 PWM	
				SCK11	I/O	SPI11 Data Clock Input/Output	
				SEG7	O	LED Segment Signal 7 Output	
22	-	-	-	PD5*	IOUDS	PORT D Bit 5 Input/Output	
				SS11	I/O	SPI Channel 11 Slave Select signal	
				SEG6	O	LED Segment Signal 6 Output	
23	21	15	14	VDD	P	VDD	
24	22	16	15	VSS	P	VSS	
25			-	PE7*	IOUDS	PORT E Bit 7 Input/Output	
				T11O	O	Timer 11 Output	
				T11C	I	Timer 11 Clock/Capture Input	
				CS11	IA	Capacitive Touch switch input 11	
				SEG5	O	LED Segment Signal 5 Output	
26	23	17	16	PE6*	IOUDS	PORT E Bit 6 Input/Output	
				T10O	O	Timer 10 Output	
				T10C	I	Timer 10 Clock/Capture Input	
				CS12	IA	Capacitive Touch switch input 12	
				SEG4	O	LED Segment Signal 4 Output	
27	24	18	17	PE5*	IOUDS	PORT E Bit 5 Input/Output	
				PWM30CB	O	Timer 30 PWM Output	
				MOSI21	I/O	SPI Channel 21 Master Out / Slave In	
				CS13	IA	Capacitive Touch switch input 13	
				SEG3	O	LED Segment Signal 3 Output	

Table 2. Pin Description (continued)

Pin No				Pin Name	Type	Description	Remark
48	44	32	28				
28	25	19	18	PE4*	IOUDS	PORT E Bit 4 Input/Output	
				PWM30CA	O	Timer 30 PWM Output	
				MISO21	I/O	SPI21 Master-Input/Slave-Output Data signal	
				CS14	IA	Capacitive Touch switch input 14	
				SEG2	O	LED Segment Signal 2 Output	
29	26	20	19	PE3*	IOUDS	PORT E Bit 3 Input/Output	
				PWM30BB	O	Timer 30 PWM Output	
				SCK21	I/O	SPI21 Data Clock Input/Output	
				CS15	IA	Capacitive Touch switch input 15	
				SEG1	O	LED Segment Signal 1 Output	
30	27	21	20	PE2*	IOUDS	PORT E Bit 2 Input/Output	
				PWM30BA	O	Timer 30 PWM Output	
				SS21	I/O	SPI Channel 21 Slave Select signal	
				CS16	IA	Capacitive Touch switch input 16	
				SEG0	O	LED Segment Signal 0 Output	
31	28	22	21	PE1*	IOUDS	PORT E Bit 1 Input/Output	
				PWM30AB	O	Timer 30 PWM Output	
32	29	23	22	PE0*	IOUDS	PORT E Bit 0 Input/Output	
				PWM30AA	O	Timer 30 PWM Output	
33	30	-	-	PF7*	IODS	PORT F Bit 7 Input/Output	Open-drain
				T30C	I	Timer 30 Clock/Capture Input	
				SDA0	O	I^2C Channel 0 SDA In/Out	
34	31	-	-	PF6*	IODS	PORT F Bit 6 Input/Output	Open-drain
				EC30	I	Timer 30 Event Count Input	
				SCL0	O	I^2C Channel 0 SCL In/Out	
35	32	-	-	PF5*	IODS	PORT F Bit 5 Input/Output	Open-drain
				BLNK	I	External Sync Signal Input for T30 PWM	
36	33	-	-	PF4*	IOUDS	PORT F Bit 4 Input/Output	
				CLKO	O	System Clock Output	
37	34	24	23	PF3*	IOUDS	PORT F Bit 3 Input/Output	
				RXD1	I	UART Channel 1 RxD Input	
				T30C	I	Timer 30 Clock/Capture Input	
				SXOUT	O	Sub Oscillator Output	
38	35	25	24	PF2*	IOUDS	PORT F Bit 2 Input/Output	
				TXD1	O	UART Channel 1 TxD Input	
				EC30	I	Timer 30 Event Count Input	
				SXIN	I	Sub Oscillator Input	
39	36	26	25	PC5	IOUDS	PORT C Bit 5 Input/Output	
				nRESET*	IU	External Reset Input	Pull-up

Table 2. Pin Description (continued)

Pin No				Pin Name	Type	Description	Remark
48	44	32	28				
40	37	27	26	PF1*	IOUDS	PORT F Bit 1 Input/Output	
				SDA1	O	I^2C Channel 1 SDA In/Out	
				XIN	I	Main Oscillator Input	
41	38	28	27	PF0*	IOUDS	PORT F Bit 0 Input/Output	
				SCL1	O	I^2C Channel 1 SCL In/Out	
				XOUT	O	Main Oscillator Output	
42	39	29	28	VSS	P	GND	
43	40	30	1	VDD	P	VDD	
44	41	-	-	PA0*	IOUDS	PORT A Bit 0 Input/Output	
				SDA1	O	I^2C Channel 1 SDA In/Out	
				AN0	IA	Analog Input 0	
				CS3	IA	Capacitive Touch switch input 3	
45	42	-	-	PA1*	IOUDS	PORT A Bit 1 Input/Output	
				SCL1	O	I^2C Channel 1 SCL In/Out	
				AN1	IA	Analog Input 1	
				CS4	IA	Capacitive Touch switch input 4	
46	43	31	2	PA2*	IOUDS	PORT A Bit 2 Input/Output	
				EC12	I	Timer 12 Event Count Input	
				AN2	IA	Analog Input 2	
				AVREF	IA	A/D Converter Reference Input	
				CS5	IA	Capacitive Touch switch input 5	
				COM15	O	LED Common Signal 15 Output	
47	-	-	-	PA3*	IOUDS	PORT A Bit 3 Input/Output	
				AN3	IA	Analog Input 3	
				CS6	IA	Capacitive Touch switch input 6	
				COM14	O	LED Common Signal 14 Output	
48	-	-	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
				AN4	IA	Analog Input 4	
				CS7	IA	Capacitive Touch switch input 7	
				COM13	O	LED Common Signal 13 Output	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. The * means ‘selected pin function after reset condition’.
3. Pin order may be changed with revision notice.

3 System and memory overview

3.1 System architecture

Main system of A31G21x series consists of the followings:

- ARM® Cortex® -M0+ core
- General purpose DMA
- Internal SRAM
- Internal Flash memory
- Two AHB buses

3.1.1 Cortex-M0+ Core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

3.1.2 Interrupt controller

Table 3. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA,B
4	0x0000_0050	GPIOC,D
5	0x0000_0054	GPIOE
6	0x0000_0058	GPIOF
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20

Table 3. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
16	0x0000_0080	TIMER21
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	UART0
20	0x0000_0090	UART1
21	0x0000_0094	TIMER13
22	0x0000_0098	Reserved
23	0x0000_009C	Reserved
24	0x0000_00A0	Reserved
25	0x0000_00A4	SPI20
26	0x0000_00A8	SPI21
27	0x0000_00AC	Reserved
28	0x0000_00B0	LED
29	0x0000_00B4	TOUCH
30	0x0000_00B8	Reserved
31	0x0000_00BC	CRC

NOTES:

1. Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits).NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

   ** __NVIC_PRIO_BITS = 2

2. Figure 7 is a caution when using Peripheral Interrupts. Interrupt don’t work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.

   * __enable_irq > NVCI_EnableIRQ(Peripheral) > Each Peripheral Interrupt

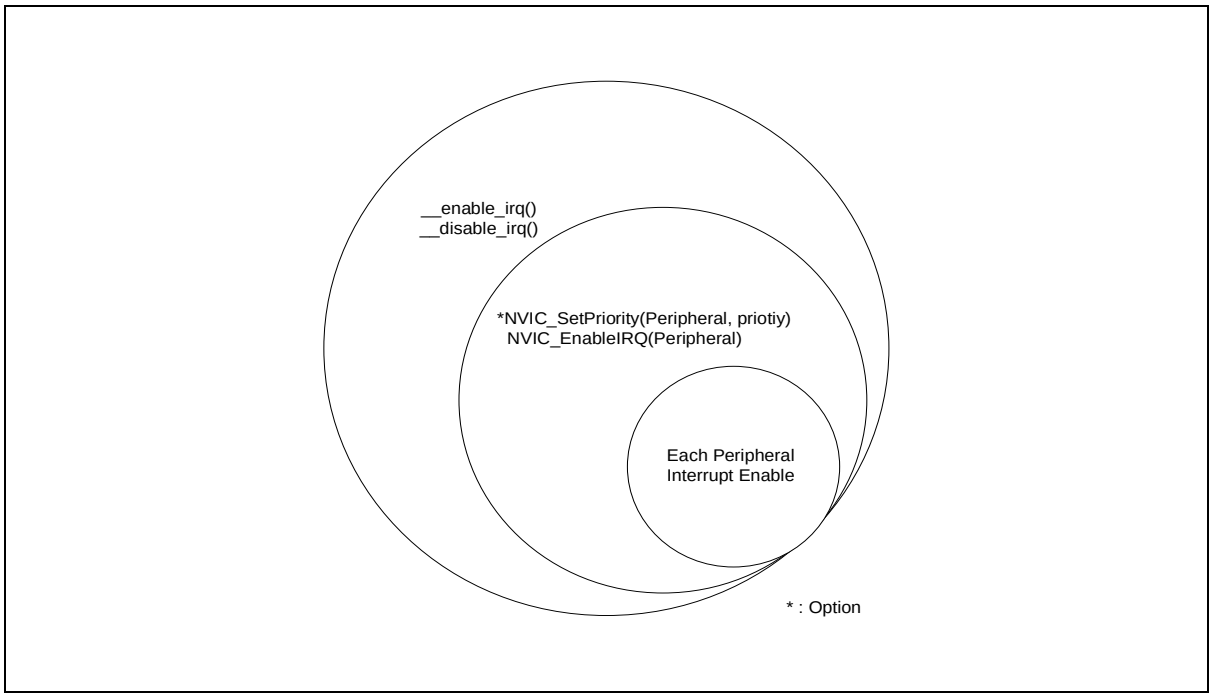


Figure 7. Interrupt Block Diagram

3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Register boundary address

Table 4 gives the boundary addresses of peripherals in A31G21x series.

Table 4. A31G21x Memory Boundary Addresses

Boundary address	Memory area
0x4000_0000	SCU
0x4000_5100	LVI/LVR
0x4000_1000/1100/1200/1300/1400/1500	PCU A/B/C/D/F
0x4000_0100	Flash controller
0x2000_0000	Internal SRAM
0x4000_0400/0410/0420/0430	DMACH0/1/2/3
0x4000_1A00	WDT
0x4000_2000	WT
0x4000_2100/2200/2300/2700	Timer 10/11/12/13
0x4000_2500	Timer 20
0x4000_2600	Timer 21
0x4000_2400	Timer 30
0x4000_3800/3900	USART 10/11
0x4000_4000/4100	UART0/1
0x4000_4800/4900	I2C 0/1
0x4000_4C00/4D00	SPI 20/21
0x4000_3000	12-bit ADC
0x4000_3500	5-bit DAC
0x4000_3600	TOUCH
0x4000_6000	LED
0x4000_0300	CRC

3.2.2 Memory map

Figure 8 shows addressable memory space in memory map.

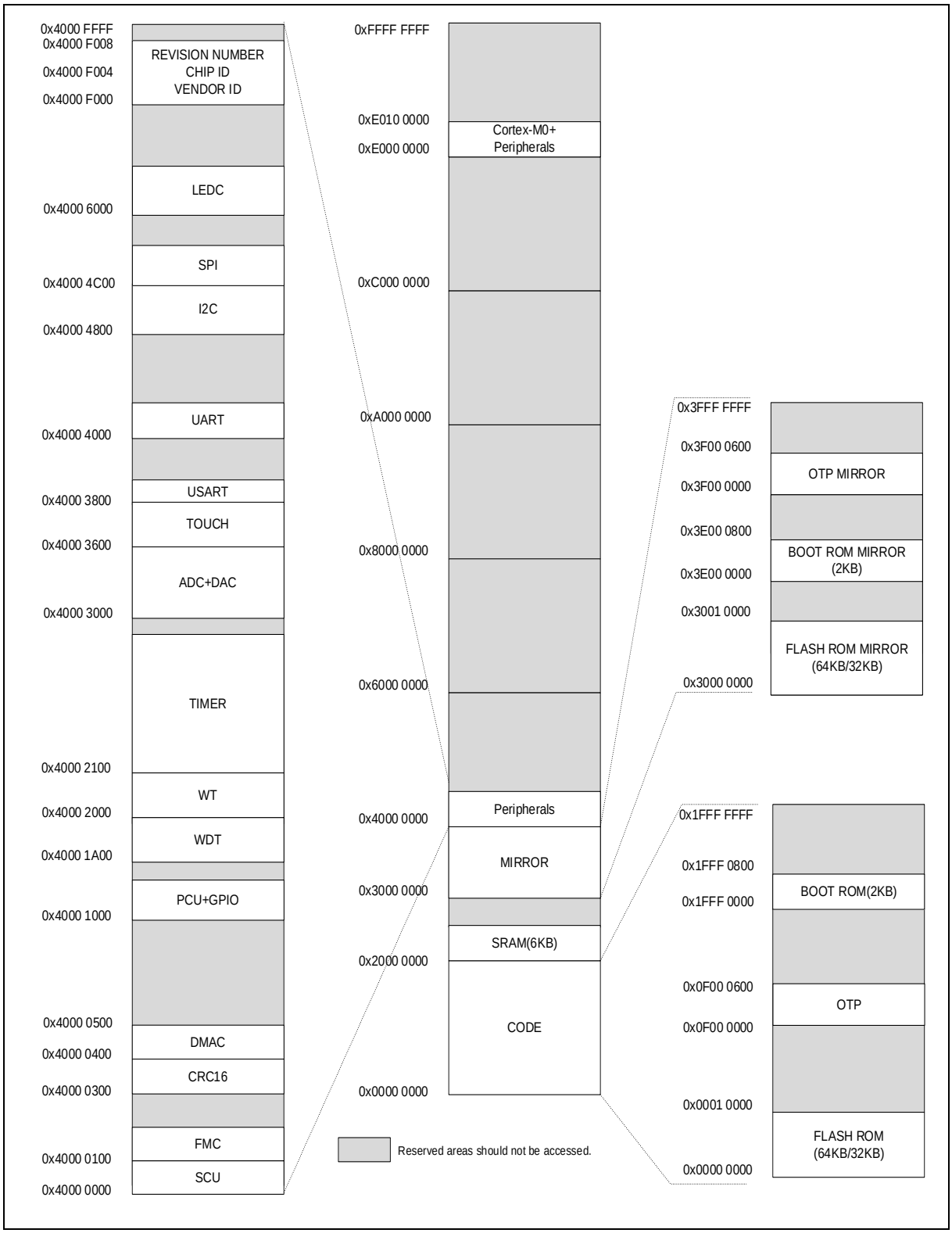


Figure 8. Memory Map

3.2.3 Embedded SRAM

A31G21x series have a block of 0-wait on-chip SRAM. The size of SRAM is 6KB and its base address is 0x2000_0000.

SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So jump and return are required to perform the code in SRAM memory area.

3.2.4 Flash memory overview

A31G21x series provides internal 64KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 48MHz bus frequency.

3.3 Boot mode

Boot mode pins

A31G21x series has Boot mode option to program internal flash memory. The Boot mode can be entered by setting BOOT pin to ‘L’ at reset timing. (Normal state is ‘H’)

The Boot mode supports UART boot and SPI boot. UART boot uses TXD10/RXD10 port, and SPI boot uses MOSI10/MISO10/SCK10/SS10 port.

The pins for Boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Dir	Description
SYSTEM	nRESET/PC5	I	Reset Input signal
	BOOT/PB3	I	‘L’ to enter Boot mode
UART mode of USART10	RXD10/PB1	I	UART Boot Receive Data
	TXD10/PB0	O	UART Boot Transmit Data
SPI mode of USART10	SS10/PB3	I	SPI Boot Slave Selectable after Boot ROM
	SCK10/PB2	I	SPI Boot Clock Input
	MISO10/PB1	I	SPI Boot Data Input with function exchange
	MOSI10/PB0	O	SPI Boot Data Output with function exchange

Boot mode connections

User can design a target board using any of boot mode ports such as SPI or UART mode of USART10. Sample connection diagrams of boot mode are introduced in the following figures:

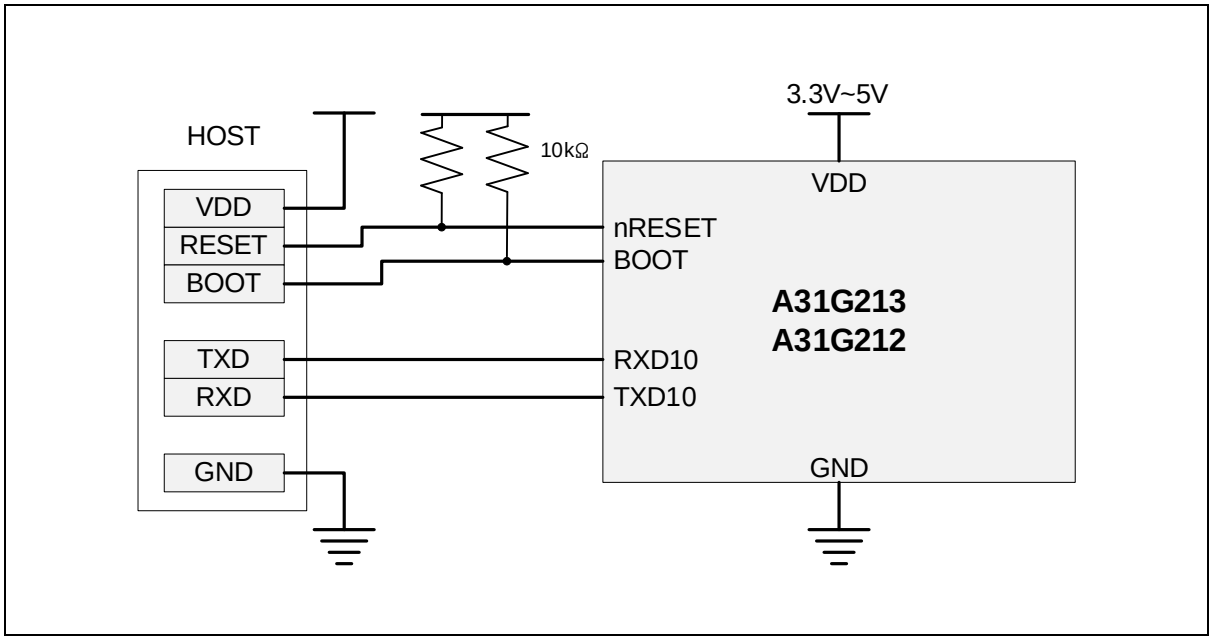


Figure 9. Connection Diagram of UART Boot

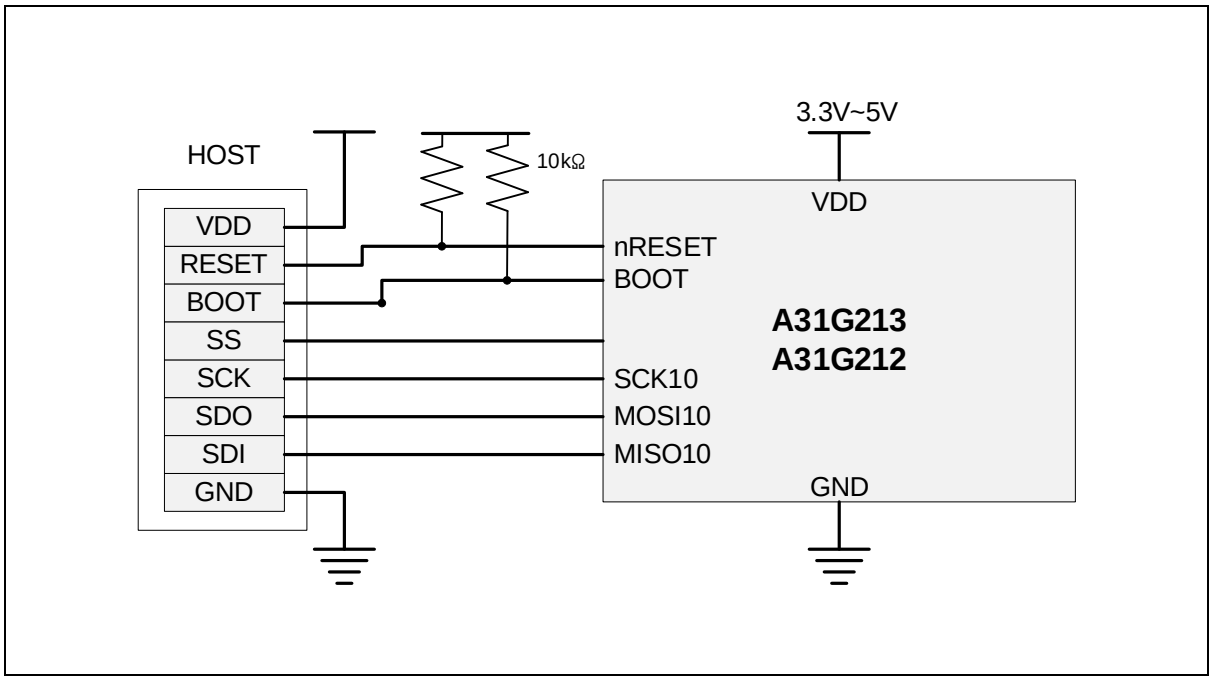
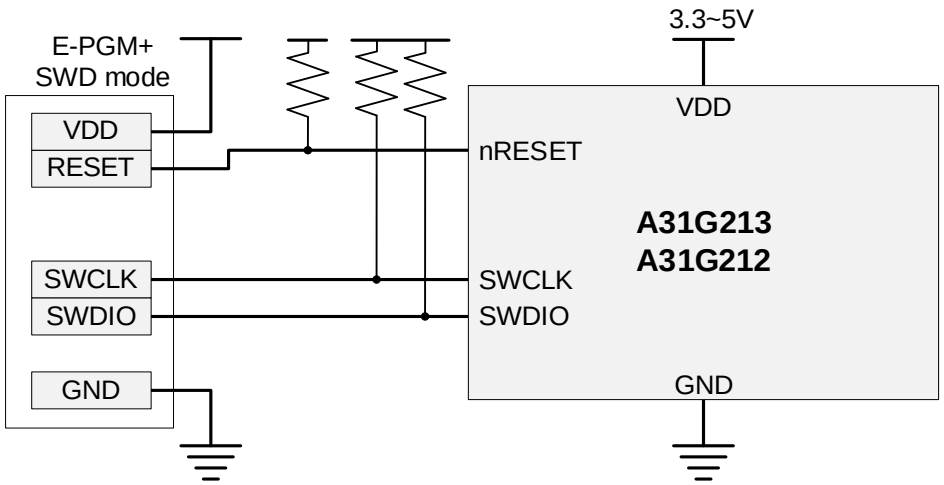


Figure 10. Connection Diagram of SPI Boot

SWD mode connections

A user can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.



NOTE: A31G21x series must not be connected to SWD mode in Boot Mode.

Figure 11. Connection Diagram of E-PGM+ and SWD Port

4 System control unit

A31G21x series have a built-in intelligent power control block which manages system analog blocks and operating modes. System control unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 6 are assigned for SCU block.

Table 6. SCU Pins

Pin name	Type	Description
nRESET/PC5	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

In this subsection, SCU block diagram is introduced in Figure 12.

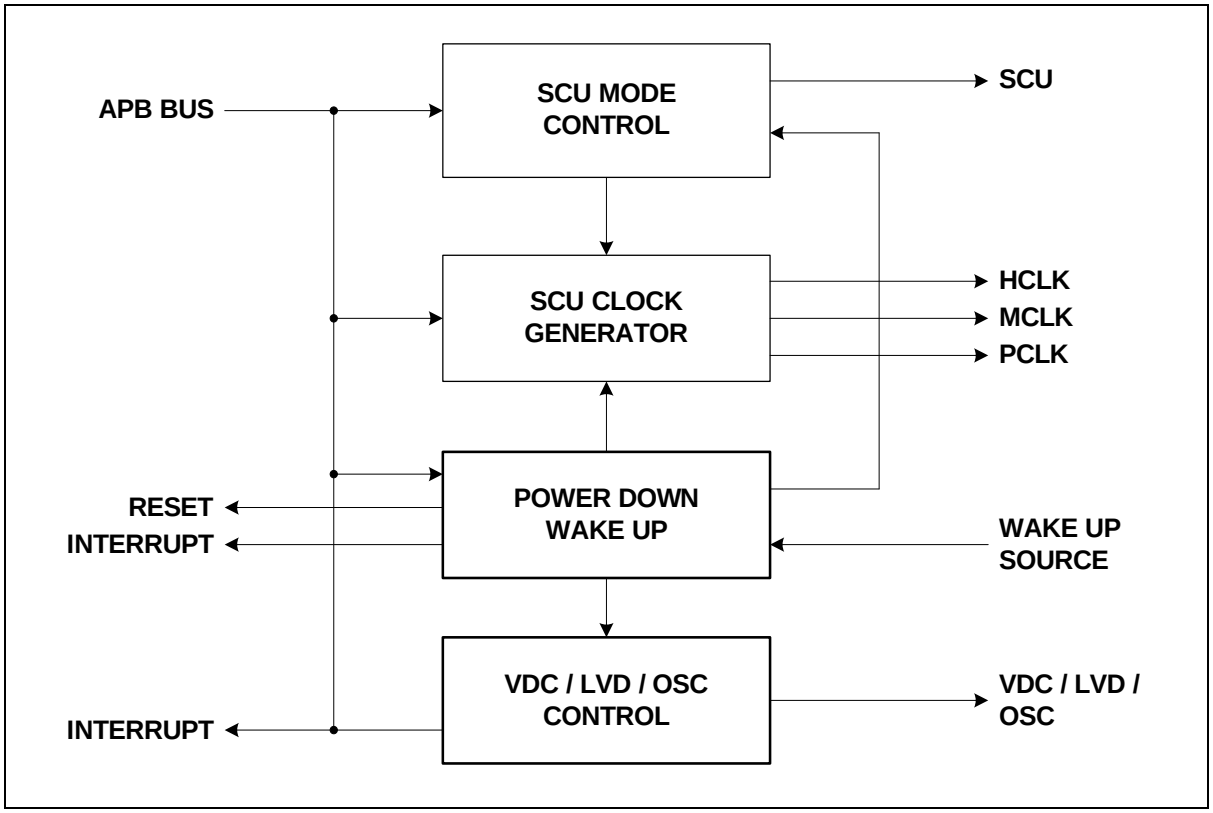


Figure 12. SCU Block diagram

4.2 Clock system

A31G21x series have two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 13 and Table 7, users learn about the clock system of A31G21x devices and clock sources.

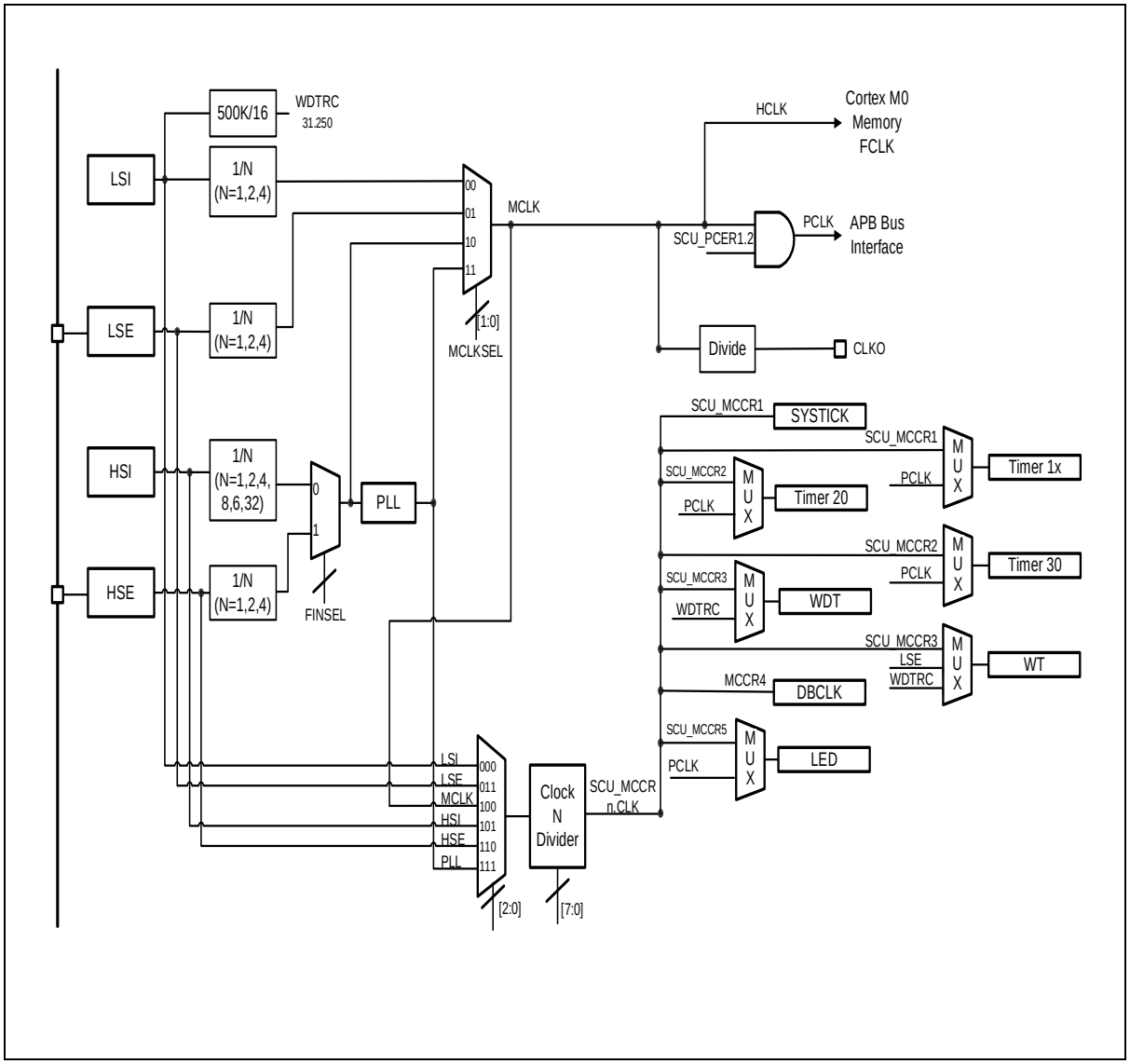


Figure 13. Clock Tree Configuration

All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 7. Clock Sources

Clock name	Frequency	Description
HSE	2-16 MHz	High Speed External Oscillator
LSE	32.768 KHz	Low Speed External Oscillator
HSI	32 MHz	High Speed Internal OSC
LSI	500 KHz	Low Speed Internal OSC

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and the AHB bus. Cortex-M0+ CPU requires 2 clocks related with FCLK and HCLK. FCLK is free running clock and it is always running except in power down mode. HCLK can be stopped in SLEEP mode and power down mode. BUS system and memory systems are operated by MCLK clock. Maximum bus operating clock speed is 48MHz.

4.2.2 PCLK clock domain

PCLK is the master clock of all peripherals. Each peripheral clock is enabled by SCU_PCER1, and SCU_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can't be accessible even reading its registers. It can be stopped in power down mode.

4.2.3 Clock configuration procedure

After power up, the default system clock is fed by LSI (500KHz) clock. LSI is default enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

HSI (32MHz) clock can be enabled by SCU_CSCR register.

HSE (2-16MHz) clock can be enabled by SCU_CSCR register. Before enable HSE block, the pin mux configuration should be set for XIN, XOUT function. PF1 and PF0 pins are shared with HSE's XIN and XOUT function – PF_MOD and PF_AFSR1 registers should be configured properly. After enabling the HSE block, you must wait for more than 5msec time to ensure stable operation of crystal oscillation.

LSE (32.768KHz) clock can be enabled by SCU_CSCR register. Before enable LSE block, the pin mux configuration should be set for SXIN, SXOUT function. PF2 and PF3 pins are shared with LSE's SXIN and SXOUT function – PF_MOD and PF_AFSR1 registers should be configured properly. After enabling the LSE block, you must wait for more than 10msec time to ensure stable operation of crystal oscillation.

You can change the MCLK by SCU_SCCR Register.

You can find an example flow chart to configure the system clock in below Figure. You can find an example flow chart configuring the system clock in Figure 14.

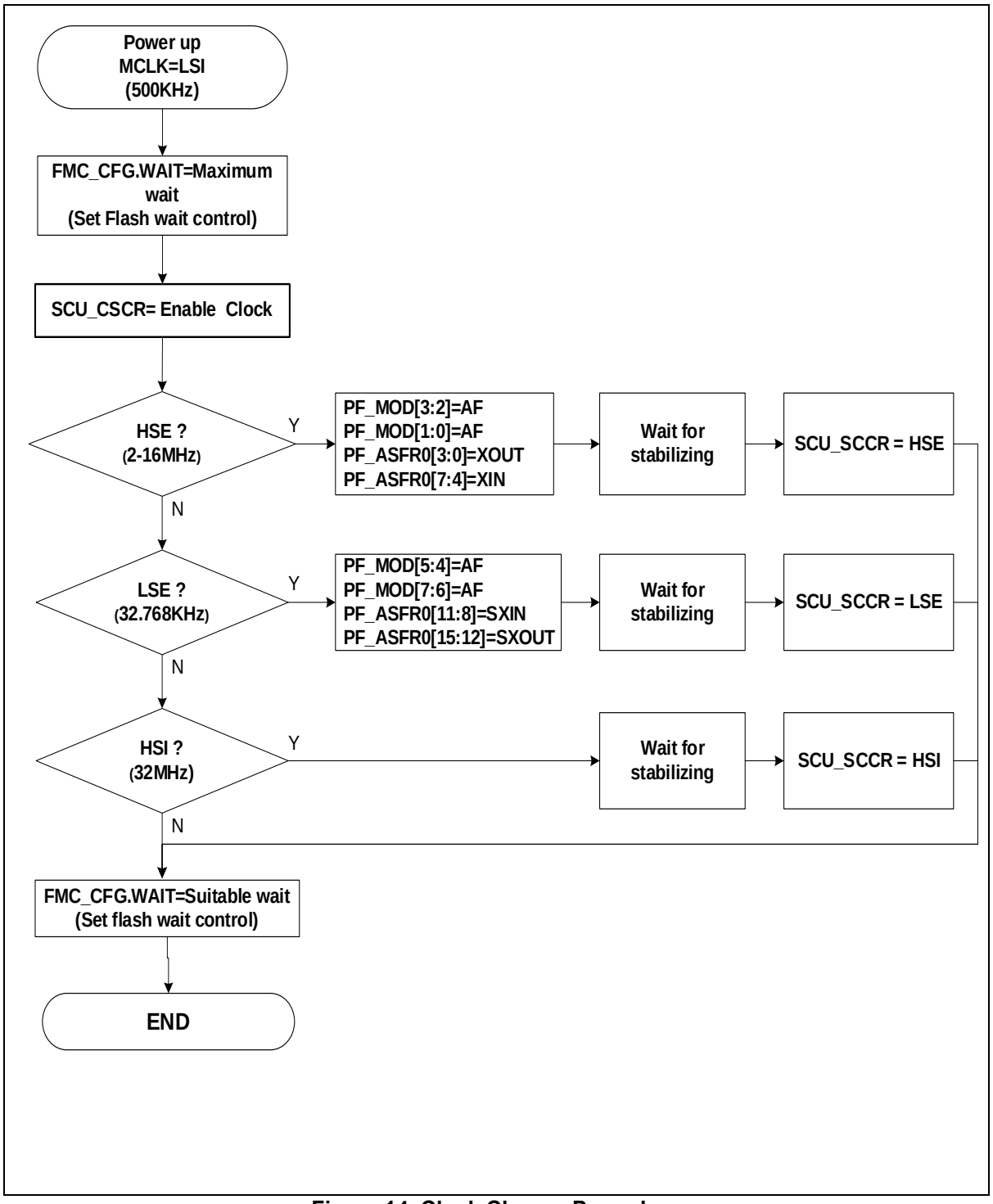


Figure 14. Clock Change Procedure

When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 8.

Table 8. Flash Wait Control Recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
000	0 clock wait	Up to 20MHz
001	1 clock wait	Up to 0MHz
010	2 clock wait	Up to 48MHz
011	3 clock wait	Up to 48MHz
100	4 clock wait	Up to 48MHz
11x	5 clock wait	Up to 48MHz

4.3 Reset

A31G21x series have two system reset options. One is to cold reset that is effective during power up or down sequence. The other is warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 9.

Table 9. Reset Sources of Cold Reset and Warm Reset

	Reset
Reset sources	• nRESET Pin • WDT reset • LVD reset • MCLK Fail reset • HSE Fail reset • S/W reset • CPU request reset

4.3.1 Cold reset

Cold reset is important feature of the chip when power is up. This characteristic will globally affect the system boot. Internal VDC is enabled when VDDEXT power is turn on. Internal POR trigger level is 1.4V of VDDEXT voltage out level. At this time, boot operation is started. The LSI clock is enabled and counts 4.25msec time for internal VDC level stabilizing. In this time, VDDEXT voltage level should be over than initial LVD level (1.65V). After 4.25msec counting, the cold reset is released and counts 0.4msec time for warm reset synchronizing. After released cold and warm reset, BOOTROM and CPU are running.

Figure 15 shows power up sequence and internal reset waveforms.

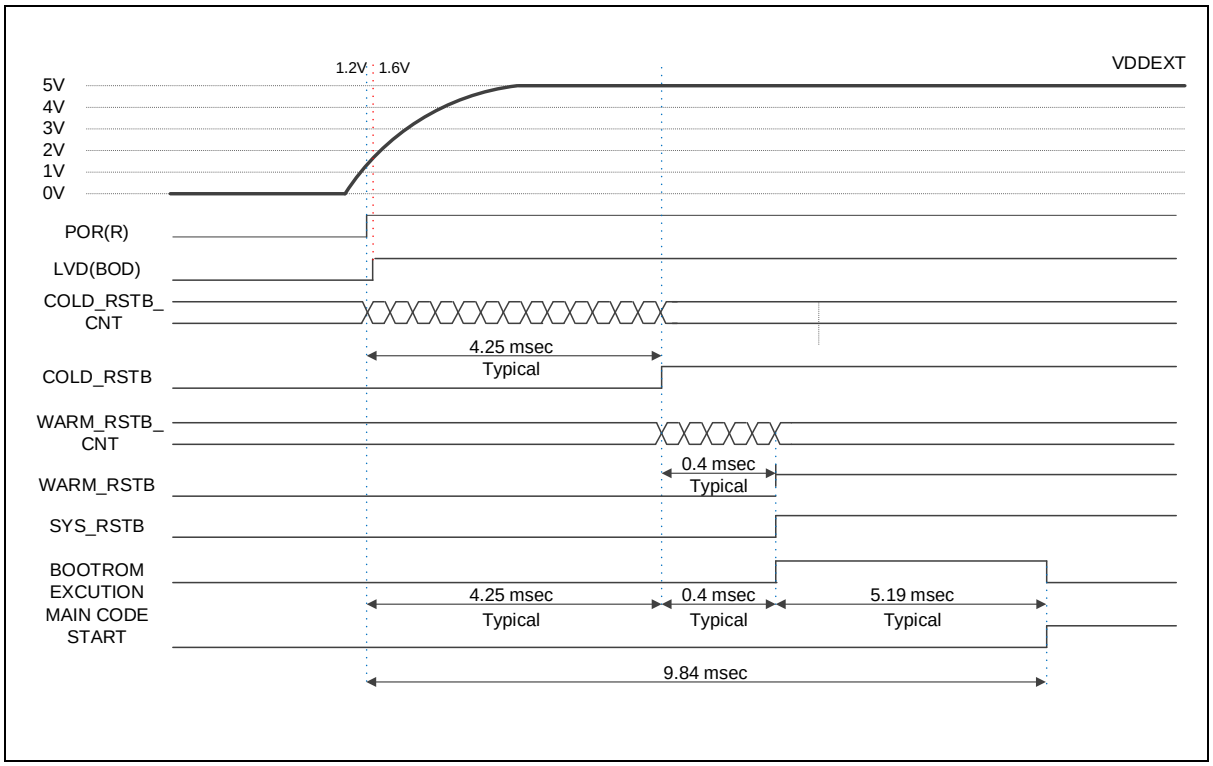


Figure 15. Power up Procedure

4.3.2 Warm reset

Warm reset event has several reset sources and some parts of chip returns to an initial state when the warm reset condition is occurred.

The warm reset source is controlled by SCU_RSER register and the status is appeared in SCU_RSSR register. The reset for each peripheral blocks is controlled by SCU_PRER register. The reset can be masked independently.

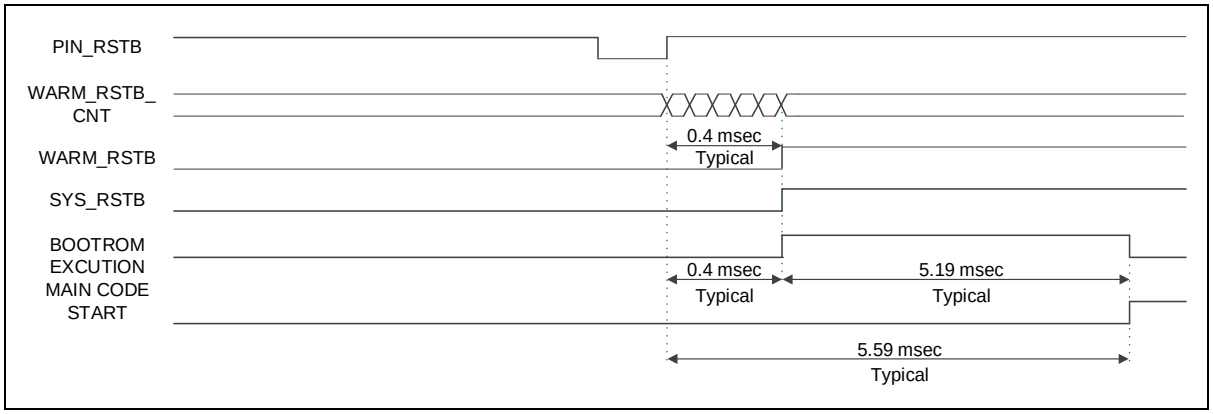


Figure 16. Warm Reset Diagram

4.3.3 LVR reset

Voltage level of LVR is set by the low voltage reset configuration register (SCULV_LVRCNFG).

The LVR reset status is appeared in RSTSSR register. The reset for LVR is controlled by SCULV_LVRCR register. The register is cleared to “0x00” on POR reset.

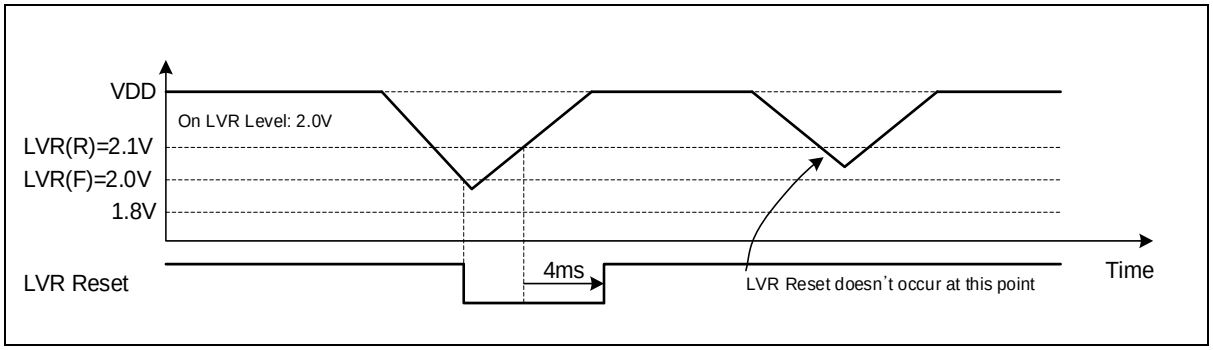


Figure 17. LVR Reset Timing Diagram

4.3.4 Reset tree

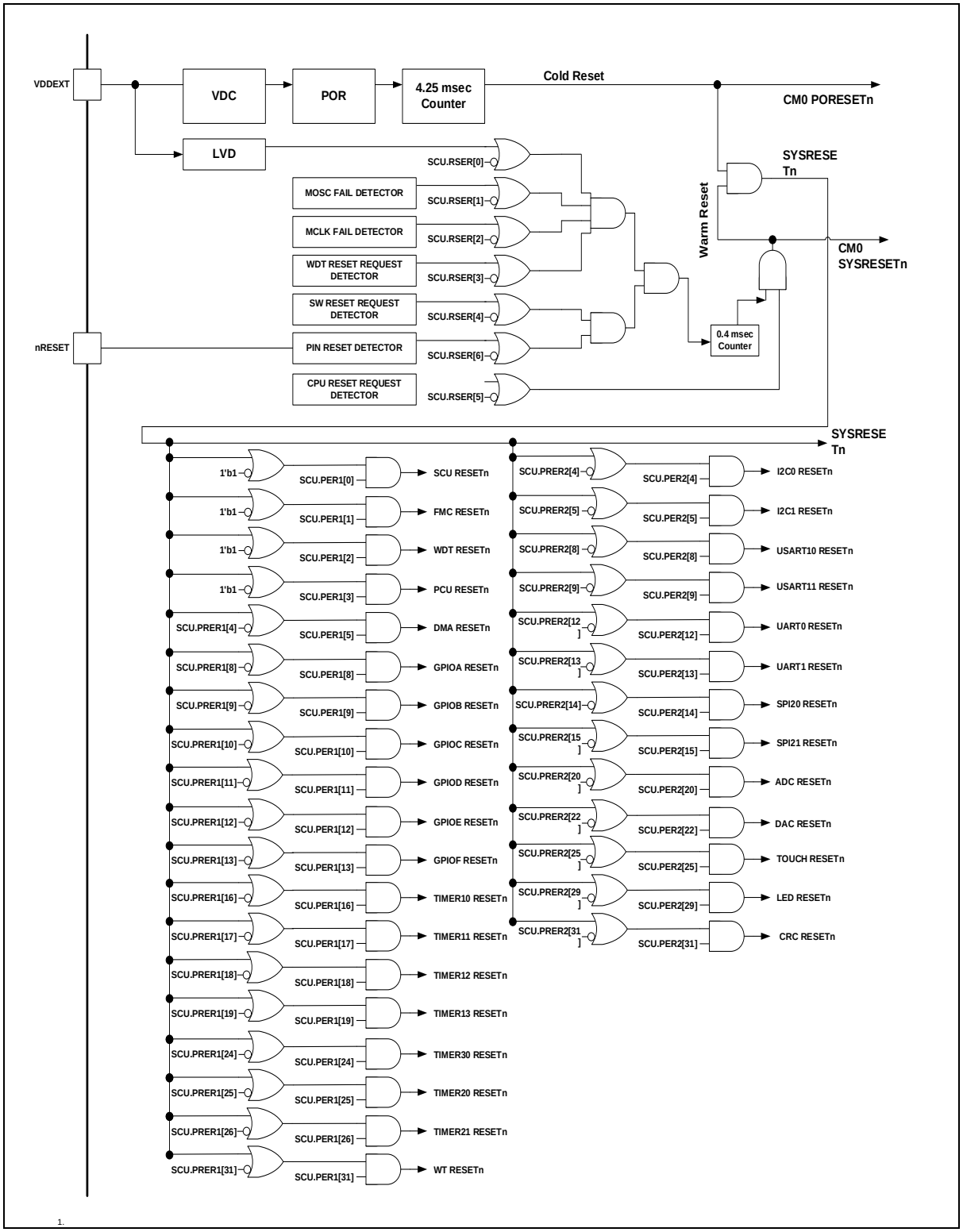
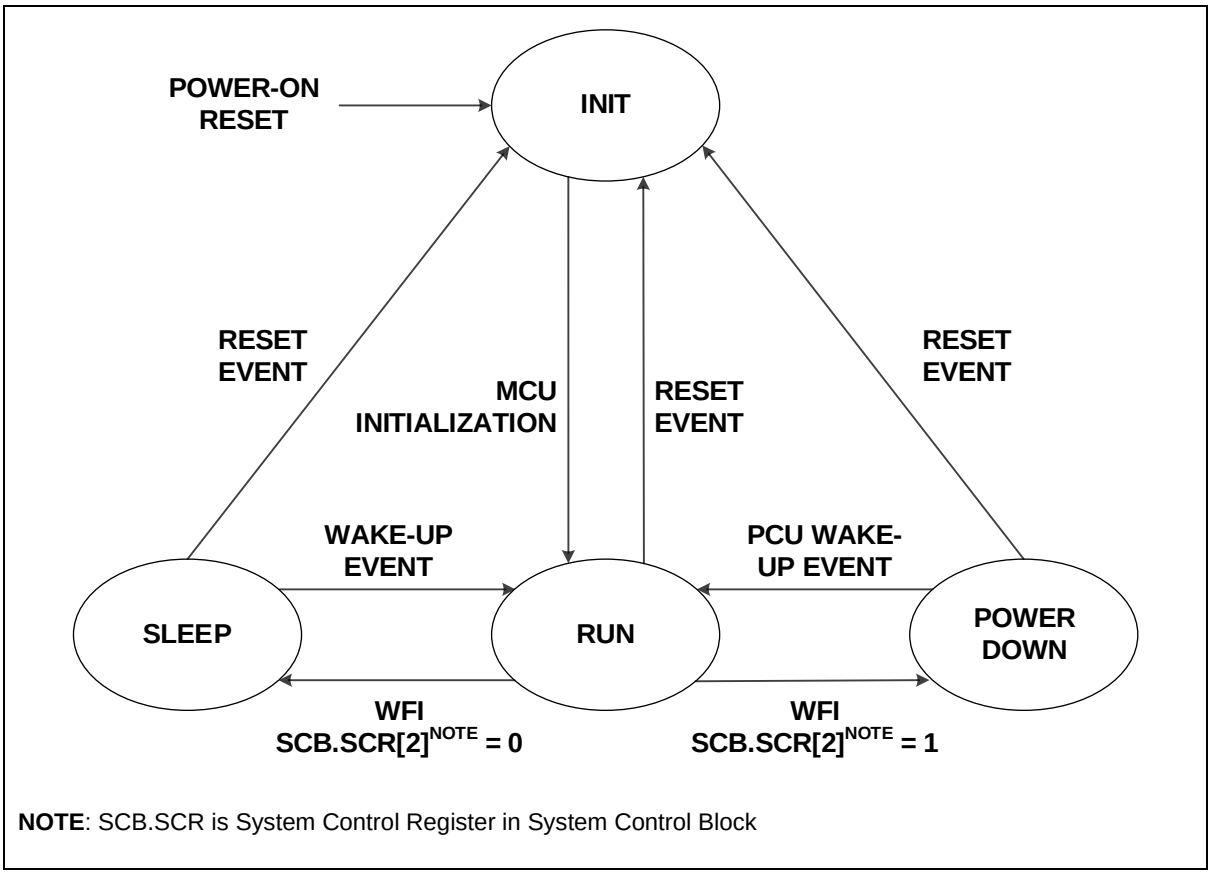


Figure 18. Reset Tree Configuration

4.4 Operation mode

INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP and the Power Down mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals. Figure 19 describes transition between the operation modes.



NOTE: SCB.SCR is System Control Register in System Control Block

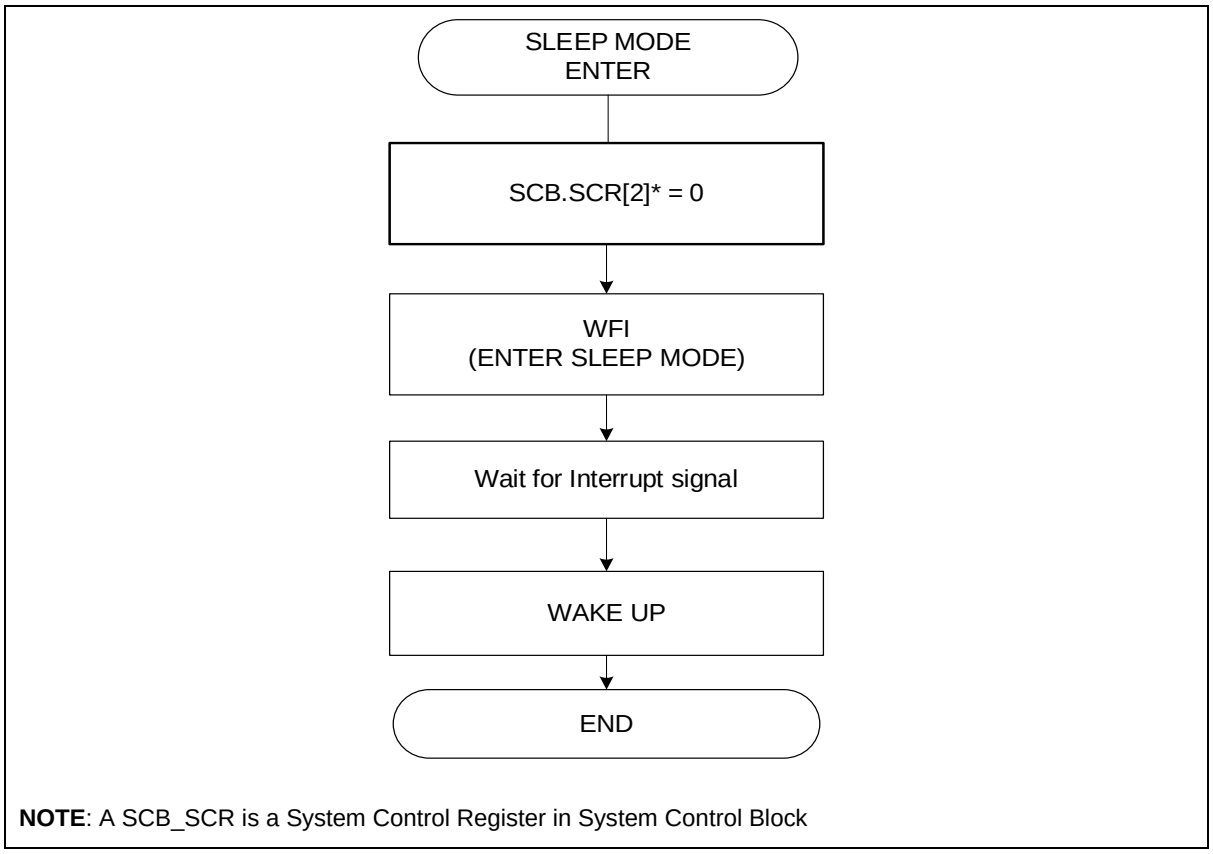
Figure 19. Transition between Operation Modes

4.4.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in the RUN mode.

4.4.2 SLEEP mode

Only CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the SCU_PER and SCU_PCER register.

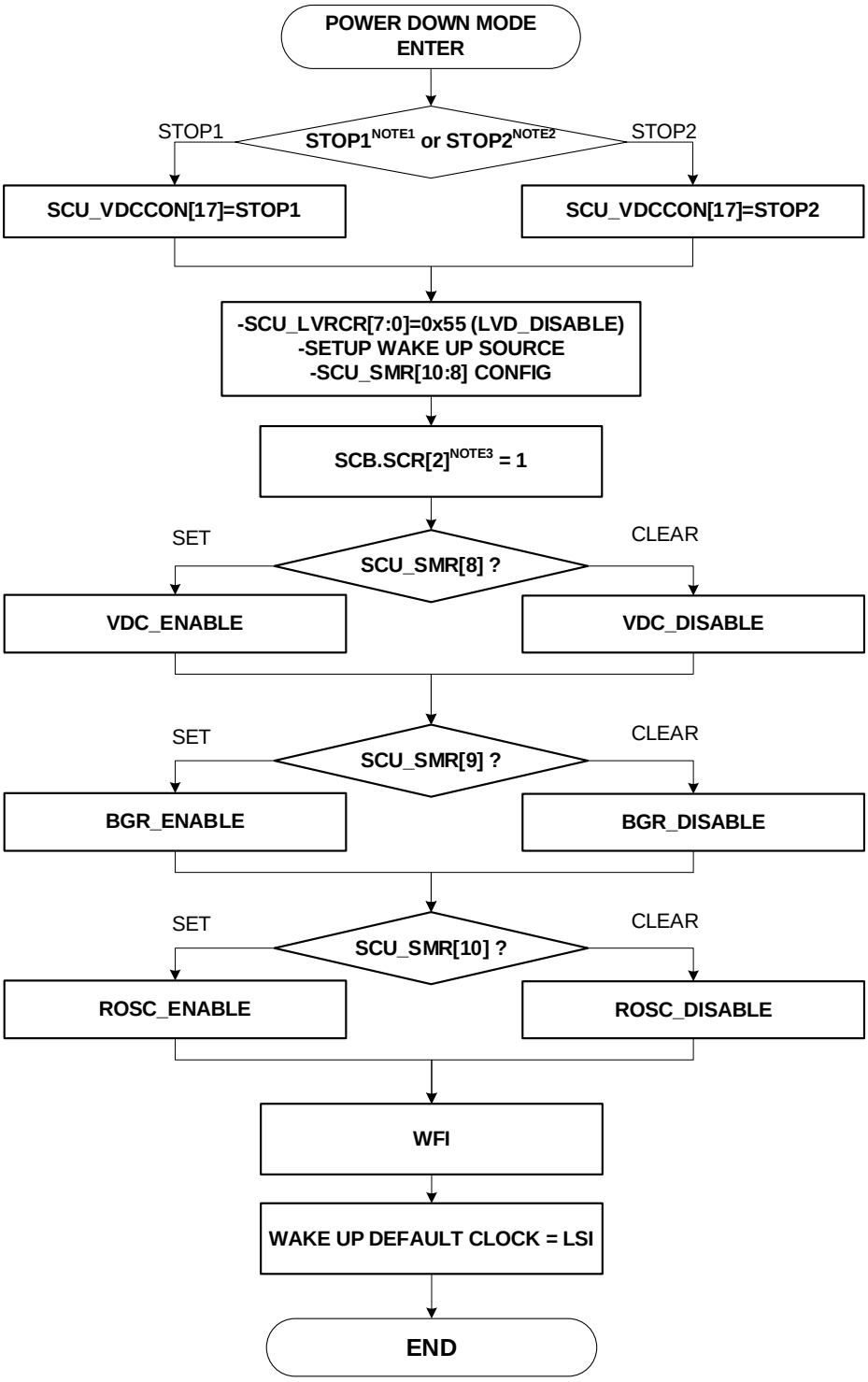


NOTE: A SCB_SCR is a System Control Register in System Control Block

Figure 20. SLEEP Mode Operation Sequence

4.4.3 Power-down mode

The A31G21x series has three power down modes:



NOTES:

1. When STOP1, VDC current is limited to 500uA.
2. When STOP2, VDC current is limited to 10uA.
3. The SCB.SCR is a System Control Register in System Control Block.

Figure 21. Power down Mode Block Diagram

5 PCU and GPIO

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- External signal directions of each pins
- Interrupt trigger mode for each pins
- Internal pull-up/down register control and open drain control

General Purpose Input/Output (GPIO) is corresponding to the most pins except dedicated-function pins. GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) select
- External interrupt interface
- Pull up/down enable or disable

Four pins in Table 10 are assigned for PCU and GPIO blocks.

Table 10. PCU and GPIO pins

Pin name	Type	Description
PA	IO	PA0 to PA7
PB	IO	PB0 to PB7
PC	IO	PC0 to PC5
PD	IO	PD0 to PD5
PF	IO	PF0 to PF7

5.1 PCU and GPIO Block diagram

Figure 22 describes PCU in block diagram.

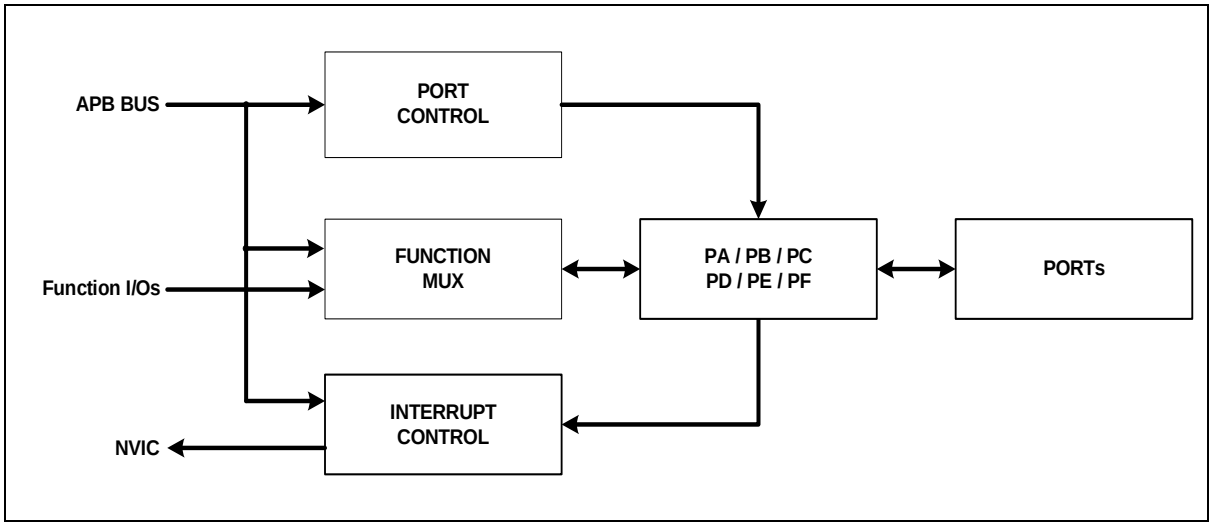


Figure 22. PCU Block Diagram

Figure 23 describes GPIO in block diagram, and Figure 24 introduces external interrupt I/O pins.

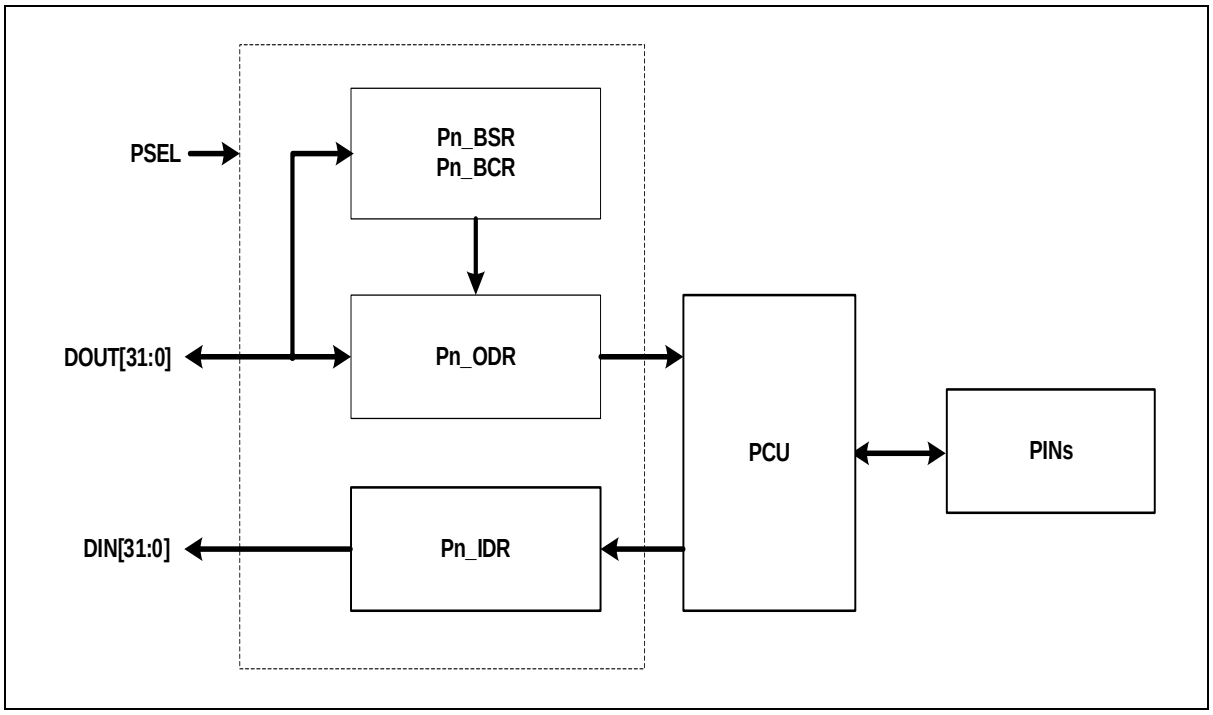


Figure 23. GPIO Block Diagram

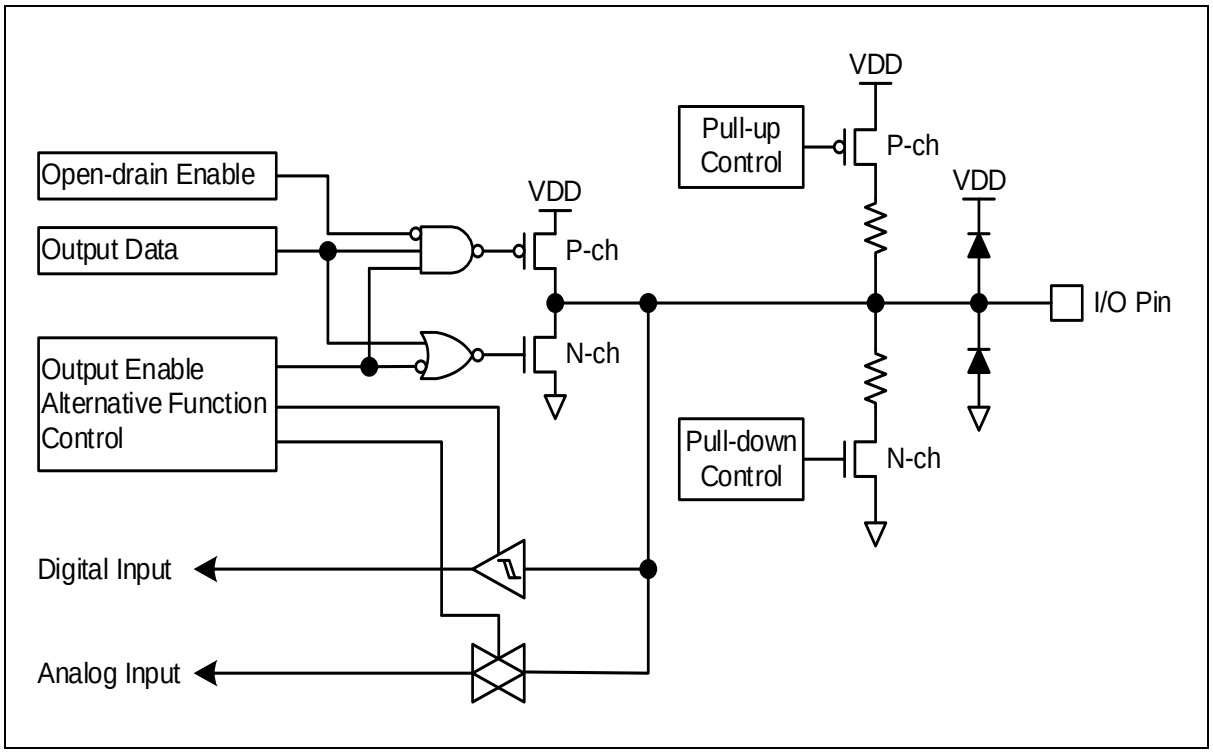


Figure 24. I/O Port Block Diagram (General I/O Pins)

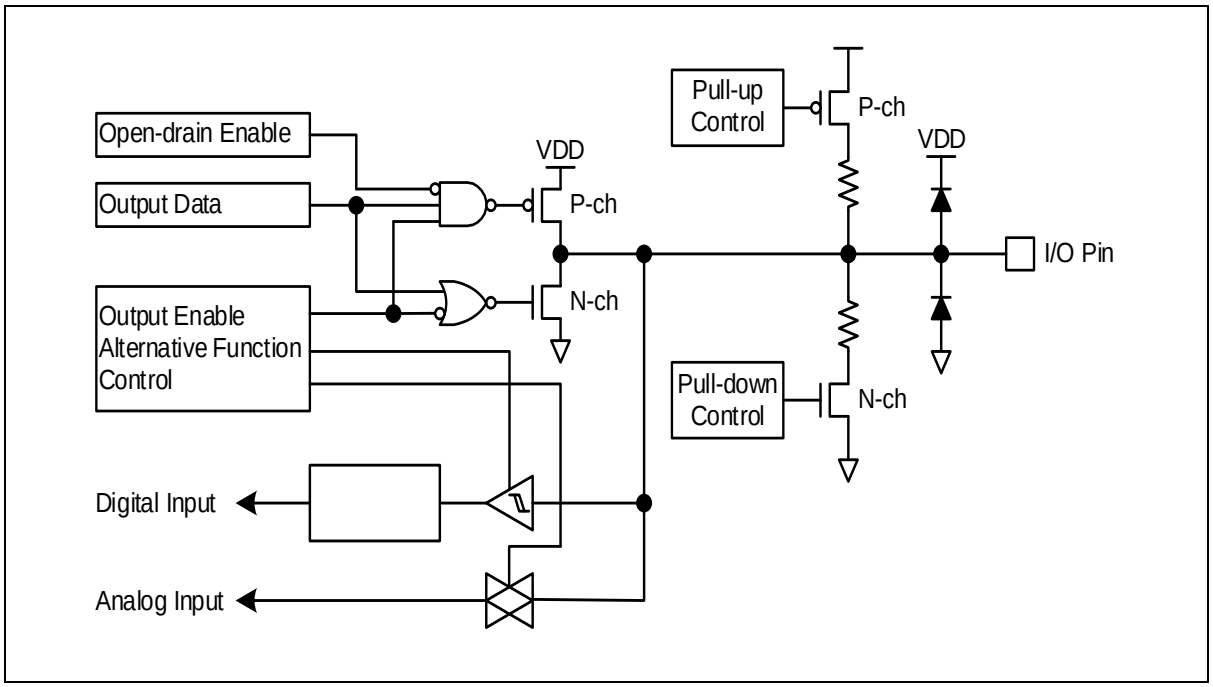


Figure 25. I/O Port Block Diagram (External Interrupt I/O Pins)

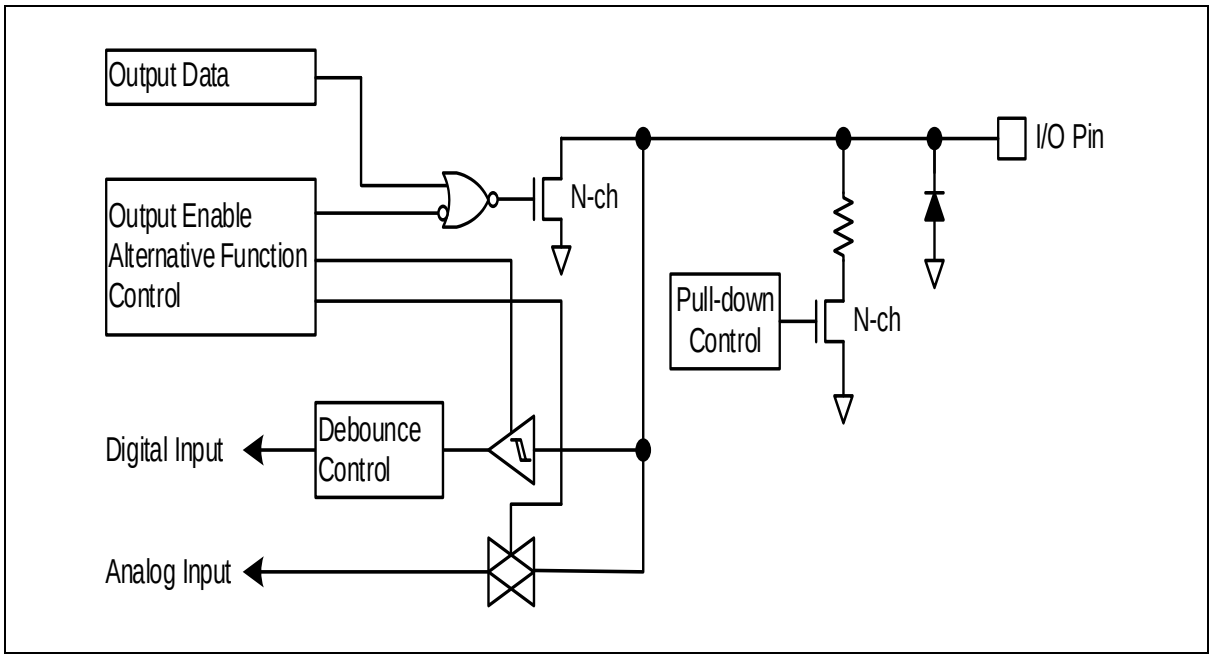


Figure 26. I/O Port Block Diagram (PF5, PF6, PF7 I/O pins)

5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 11 shows pin multiplexing information.

Table 11. GPIO Alternative Function

PORT	PIN	Functions				
		AF0	AF1	AF2	AF3	AF4
PA	0		SDA1		AN0	CS3
	1		SCL1		AN1	CS4
	2		EC12		AN2/AVREF	CS5/COM15
	3				AN3	CS6/COM14
	4				AN4	CS7/COM13
	5		T12O	T12C	AN5	CS0/COM12
	6		T11O	T11C	AN6	CS1/COM11
	7		T13O	T13C	AN7/ DAO	CS2/COM10
PB	0		TXD10	MOSI10	AN8	CS8/COM9
	1		RXD10	MISO10	AN9	CS9/COM8
	2		EC13	SCK10	AN10	CS10/COM7
	3		BOOT	SS10		
	4		TXD0	SWCLK		
	5		RXD0	SWDIO		
	6		TXD1	EC11	AN11	CS17
	7		RXD1		AN12	CS18
PC	0		T20O	T20C	AN13	CS19/COM6
	1		T21O	T21C		CS20/COM5
	2		EC20	MOSI20		CS21/COM4
	3		EC21	MISO20		CS22/COM3
	4			SCK20		CS23/COM2
	5	nRESET				

Table 11. GPIO Alternative Function (continued)

PORT	PIN	Functions				
		AF0	AF1	AF2	AF3	AF4
PD	0		SCL0	SS20		COM1
	1		SDA0	EC10		COM0
	2		TXD11	MOSI11		SEG9
	3		RXD11	MISO11		SEG8
	4		BLNK	SCK11		SEG7
	5			SS11		SEG6
PE	0		PWM30AA			
	1		PWM30AB			
	2		PWM30BA	SS21		CS16/SEG0
	3		PWM30BB	SCK21		CS15/SEG1
	4		PWM30CA	MISO21		CS14/SEG2
	5		PWM30CB	MOSI21		CS13/SEG3
	6		T10O	T10C		CS12/SEG4
	7		T11O	T11C		CS11/SEG5
PF	0		SCL1		XOUT	
	1		SDA1		XIN	
	2		TXD1	EC30	SXIN	
	3		RXD1	T30C	SXOUT	
	4		CLKO			
	5		BLNK			
	6		EC30	SCL0		
	7		T30C	SDA0		

NOTE: On connection with debugger host, The SWCLK and SWDIO pins are always for SW-DP pins. So, the corresponding bits of PB_MOD/PB_TYP/PB_AFSR/PB_PUPD registers may not be written by software.

6 Flash memory controller

Flash Memory Controller is an internal flash memory interface controller, and includes following features as shown below:

- 64 or 32KB Flash code memory
- Programmable wait control (0 to 4)
- Read protection support
- Self-Program support
- User option area
- 3-page (each 512 Bytes)
- Erase, Program in user mode

Table 12. Flash Memory Controller Features

Item	Description	
Size	64KB	32KB
Start Address	0x0000_0000	0x0000_0000
End Address	0x0001_0000	0x0000_7FFF
Page Size	512-byte	512-byte
Total Page Count	64 / 128 pages	64 / 128 pages
PGM Unit	512-byte	512-byte
Erase Unit	512-byte / 1KB / 4KB / bulk	512-byte/ 1KB/ 4KB/ bulk

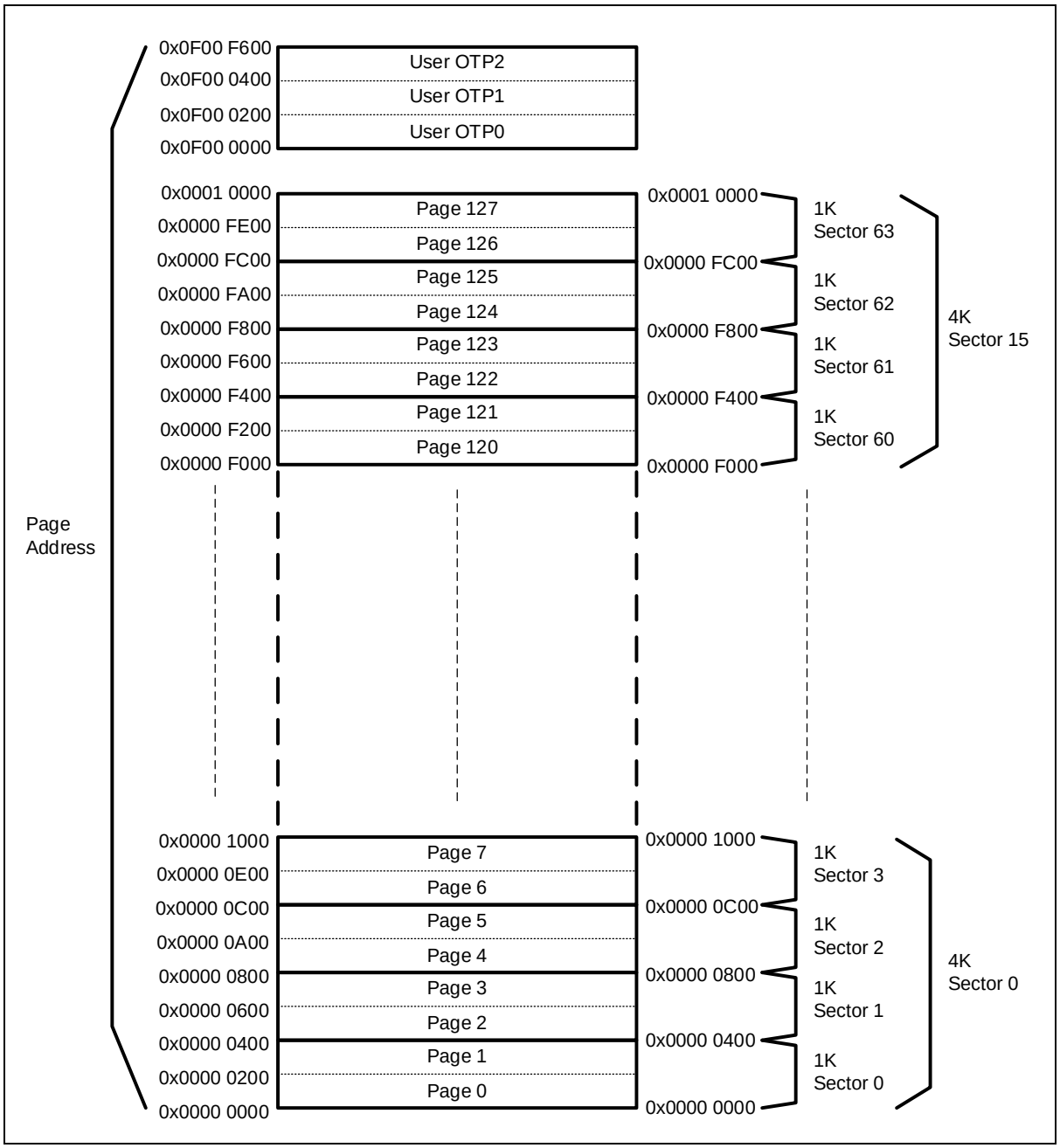


Figure 27. Flash Memory Map (64 KB Code Flash)

7 Direct Memory Access Controller (DMAC)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 4 channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size

Interrupt condition is transferred through a peripheral interrupt

7.1 Block diagram

In this section, DMAC block diagram is introduced in Figure 28.

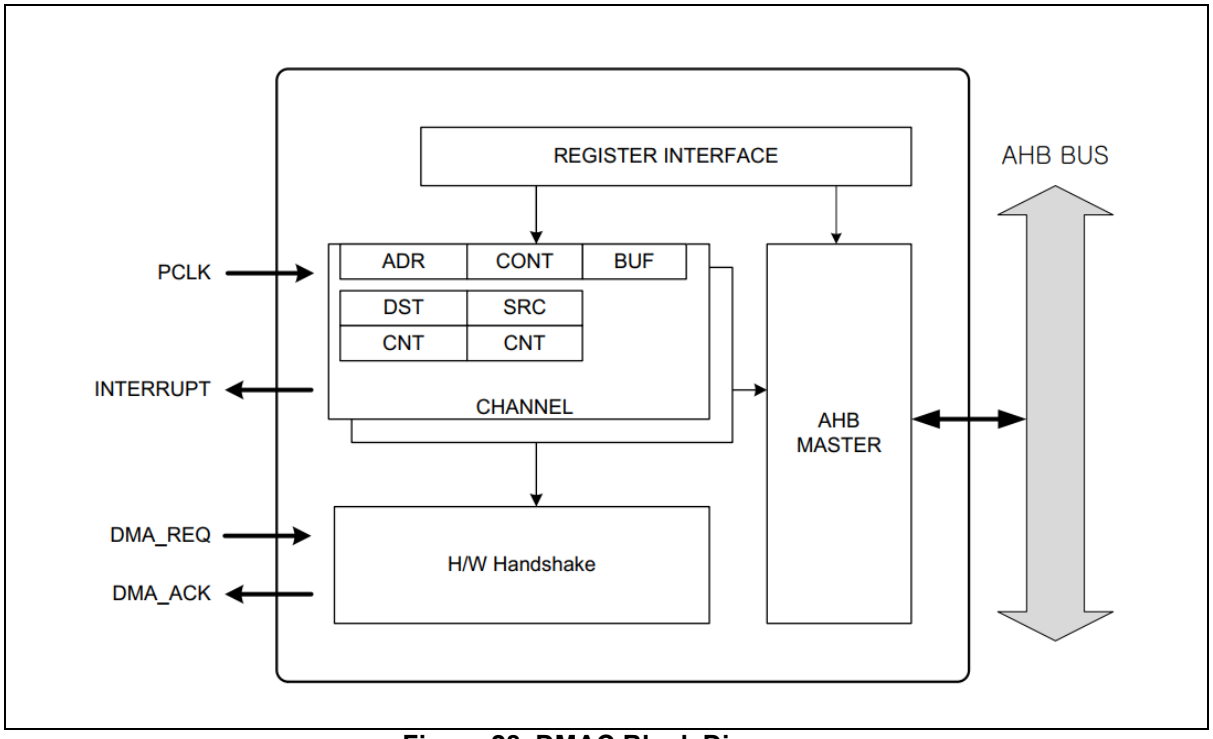


Figure 28. DMAC Block Diagram

8 Watchdog Timer (WDT)

Watchdog timer (WDT) rapidly detects CPU's malfunction such as endless looping caused by noise, and resumes the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request. When WDT is not being used for malfunction detection, it can be used as a timer generating an interrupt at fixed intervals.

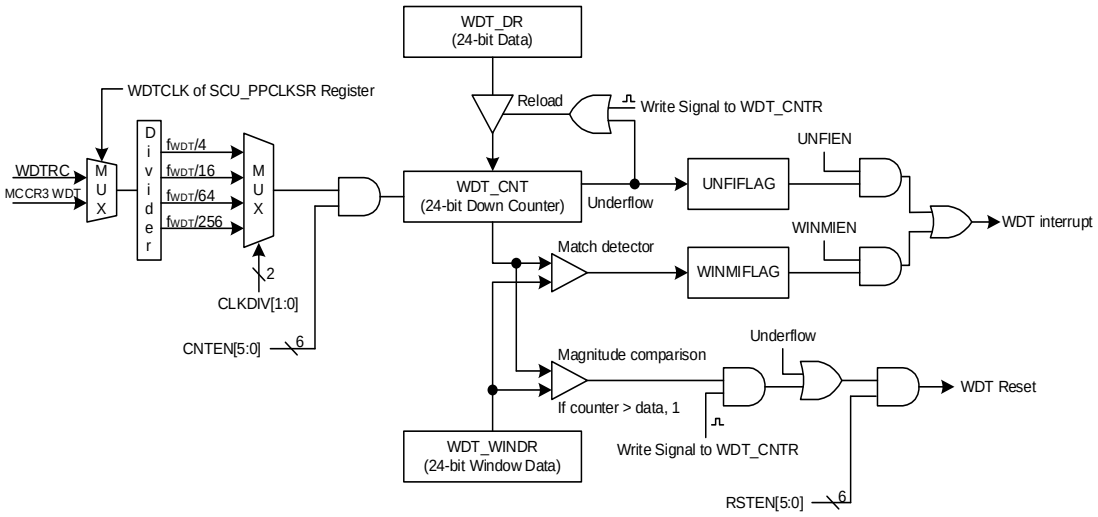
When WDT_CNT value is reached to WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of WDT can be set by WDT_DR. If the underflow occurs, an internal reset is generated. WDT operates on the WDTRC embedded RC oscillator clock.

WDT of A31G21x series features followings:

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Counter window function

8.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 29.



NOTE: If a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register after 1 clock delay with the clock which is selected by the CLKDIV bits.

Figure 29. WDT Block Diagram

9 Watch Timer

Watch timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN as '1' in watch timer control register (WT_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT_CR register.

Watch timer counter circuit corporates a 26-bit counter. Low 14 bits of the counter form a binary counter and high 12 bits form an auto reload counter in order to raise resolution. In WTR, it can control WT clear and set interval value at write time, and it can read 12-bit WT counter value at read time.

9.1 WT block diagram

As shown in Figure 30, WT of A31G21x series have the following blocks:

- 14-bit divider
- 12-bit up-counter
- RTC function

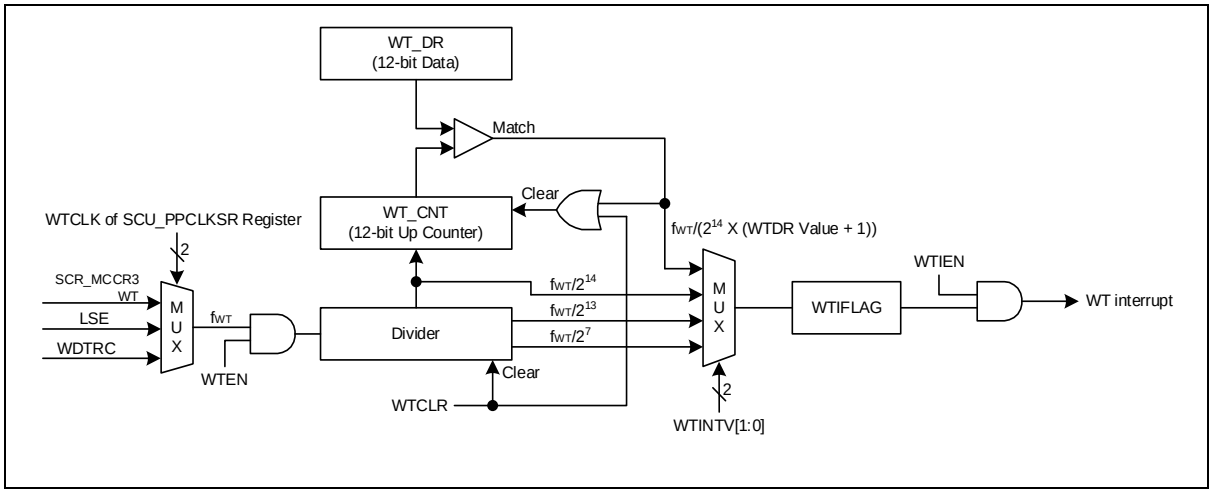


Figure 30. Watch Timer Block Diagram

10 16-bit TIMER10/11/12/13

16-bit timer block comprises 4 channels of 16-bit general purpose timers. Each channel has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. 16-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 16-bit timer is a periodical tick timer.

16-bit timer of A31G21x series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 13 introduces pins assigned for 16-bit timer.

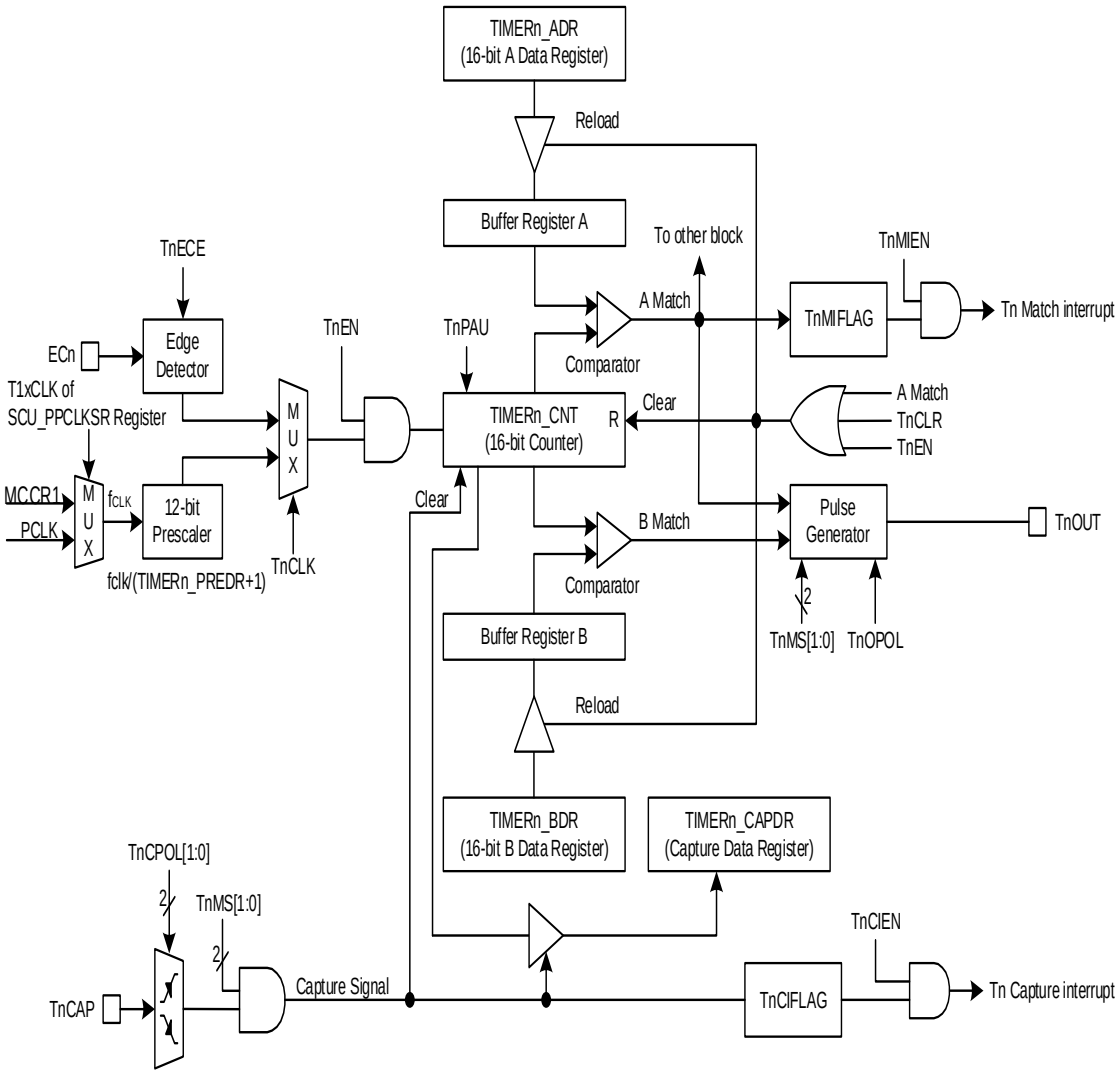
Table 13. Pin Assignment of 16-bit Timer: External Pins

Pin name	Type	Description
ECn	I	Timer 1n External Clock input
TnC	I	Timer 1n Capture input
TnO	O	Timer 1n Output

NOTE: n = 10, 11, 12, and 13

10.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 31.



NOTES:

1. The TnEN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the TnEN bit is set, the counting of TIMERn_CNT may be delayed 2 clocks or more.

Figure 31. 16-bit Timer Block Diagram

11 32-bit TIMER20

32-bit timer block comprises 1 channels of 32-bit general purpose timers. Each channel has an independent 32-bit counter and a dedicated prescaler that feeds a counting clock. 32-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 32-bit timer is a periodical tick timer.

32-bit timer of A31G21x series features the followings:

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

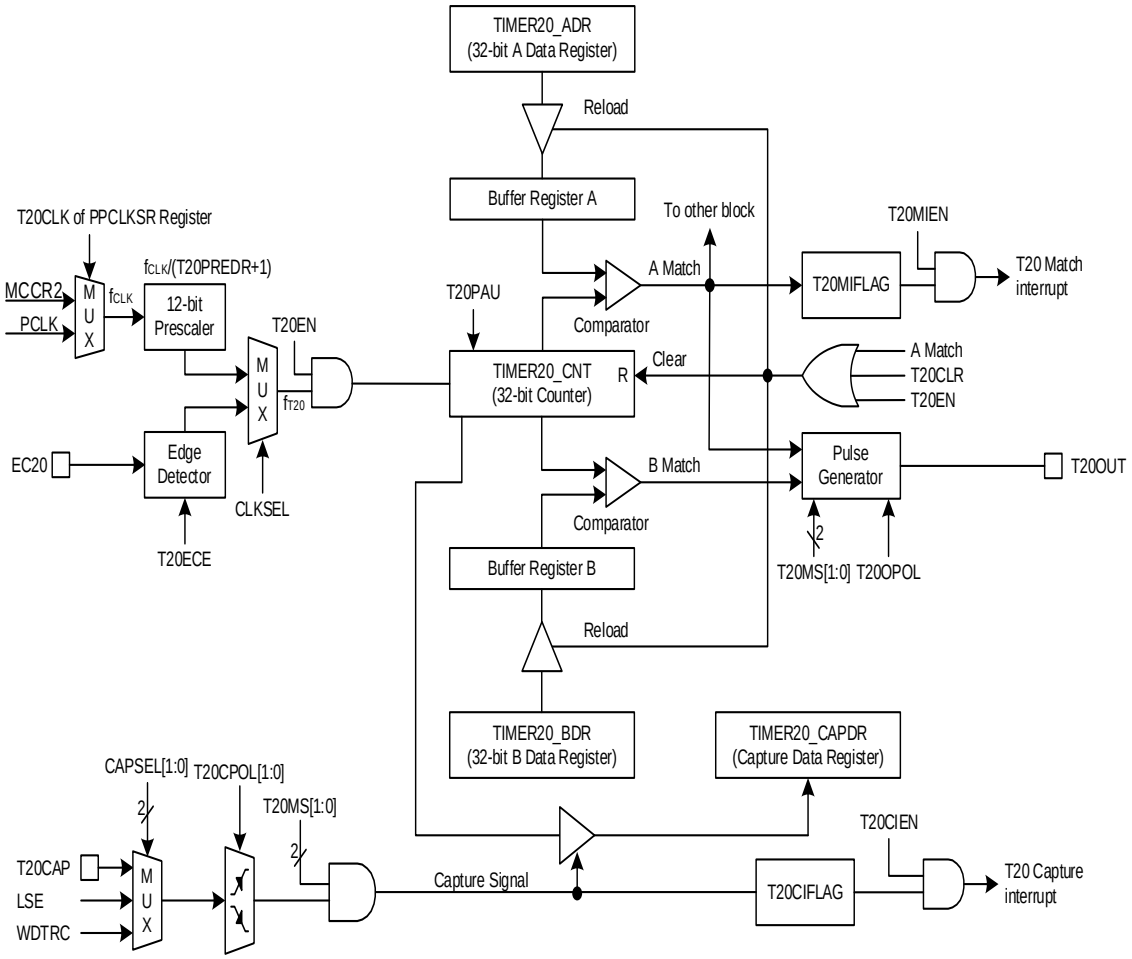
Table 14 introduces pins assigned for 32-bit timer.

Table 14. Pin Assignment of 32-bit Timer: External Pins

Pin name	Type	Description
EC20	I	Timer 20 external clock input
T20C	I	Timer 20 capture input
T20O	O	Timer/PWM/one-shot output

11.1 32-bit timer block diagram

In this section, 32-bit timer is described in a block diagram in Figure 32.



NOTES:

1. The T20EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T20EN bit is set, the counting of TIMER20_CNT may be delayed 2 clocks or more.

Figure 32. 32-bit Timer20 Block Diagram

12 32-bit TIMER21

32-bit timer block comprises 1 channels of 32-bit general purpose timers. Each channel has an independent 32-bit counter and a dedicated prescaler that feeds a counting clock. 32-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 32-bit timer is a periodical tick timer.

32-bit timer of A31G21x series features the followings:

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

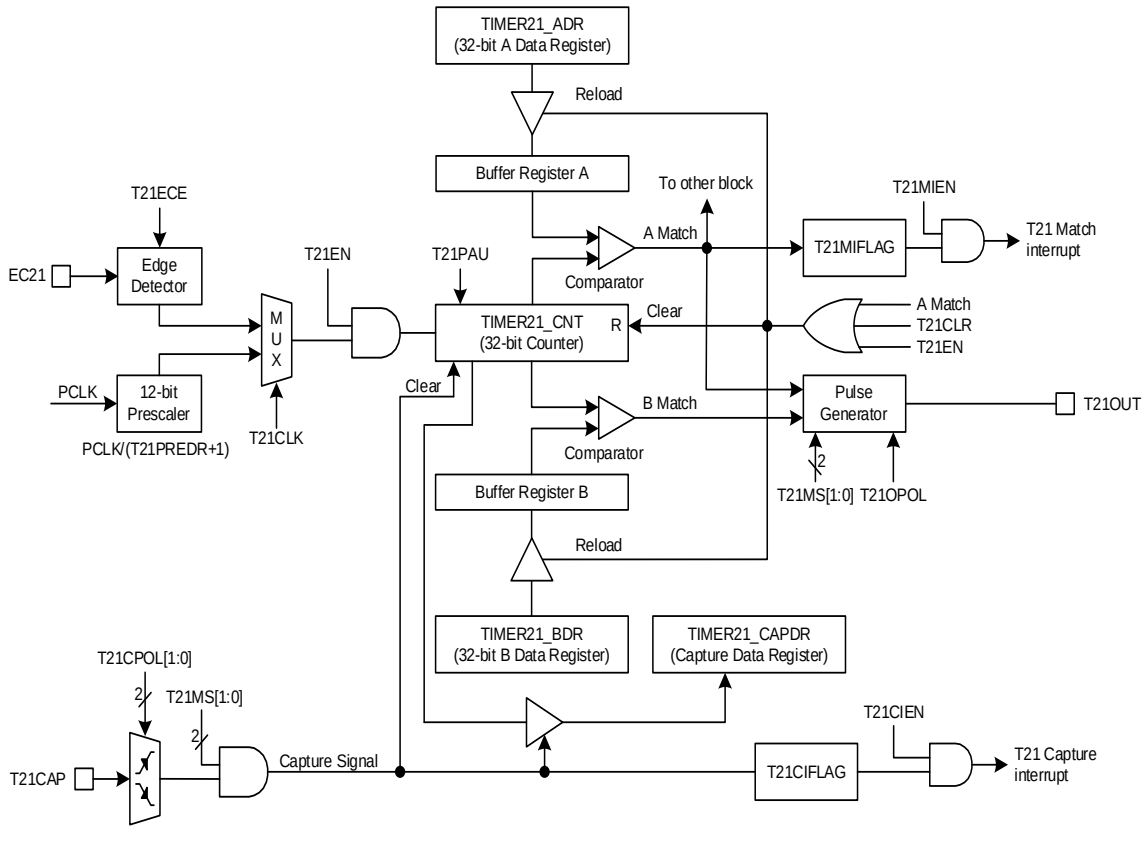
Table 15 introduces pins assigned for 32-bit timer.

Table 15. Pin Assignment of 32-bit Timer: External Pins

Pin name	Type	Description
EC21	I	Timer 21 external clock input
T21C	I	Timer 21 capture input
T21O	O	Timer/PWM/one-shot output

12.1 32-bit timer block diagram

In this section, 32-bit timer is described in a block diagram in Figure 33.



NOTES:

1. The T21EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T21EN bit is set, the counting of TIMER21_CNT may be delayed 2 clocks or more.

Figure 33. 32-bit Timer21 Block Diagram

13 16-bit timer count 30

Timer counter 30 of A31G21x series consist of a multiplexer, a comparator, 16-bit sized timer data registers A/B/C, and many other registers used for its operation. Main features are listed in the followings:

- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

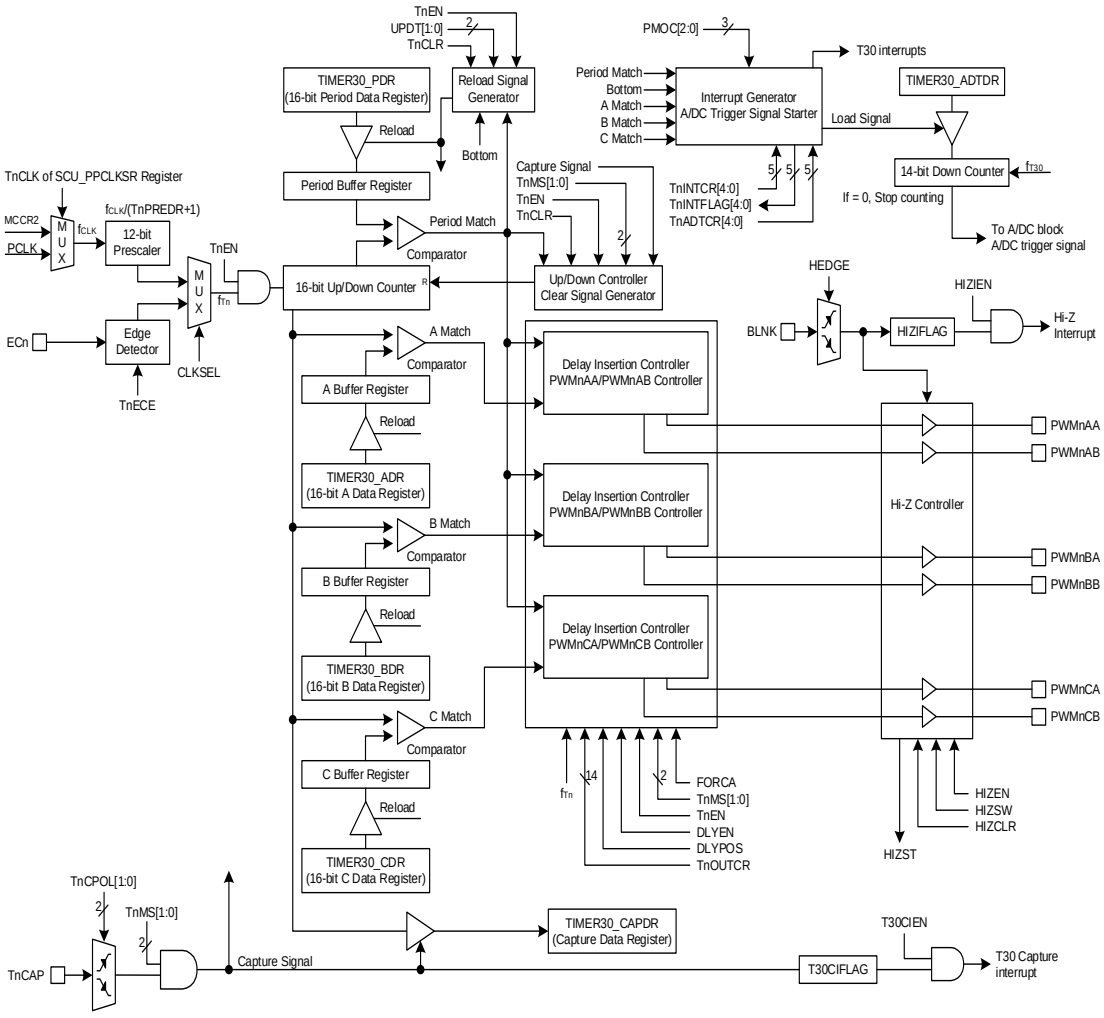
Table 16 introduces pins assigned for the timer counter 30.

Table 16. Pin Assignment of Timer Counter 30: External Pins

Pin name	Type	Description
EC30	I	External clock input
T30CAP	I	Capture input
BLNK	I	External sync signal input
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

13.1 Timer counter 30 block diagram

In this section, timer counter 30 is introduced in a block diagram.



NOTES:

1. The Period/A/B/C match interrupts except for Bottom can occur in the interval mode.
2. The Period match interrupt only can occur in the capture mode.
3. The 16-bit up/down counter in the capture mode is cleared to “0x0000” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
4. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, All T30PWM outputs can be high-impedance state with setting the HIZSW bit to ‘1’ by the UI of debugger.
5. After the T30EN bit is set, the counting of TIMER30_CNT may be delayed 2 clocks or more.

Figure 34. Timer Counter 30 Block Diagram

14 Universal Synchronous/Asynchronous Receiver/ Transmitter (USART)

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data OverRun Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Table 17 introduces pins assigned for the USART.

Table 17. Pin Assignment of USART: External Pins

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 10, 11

14.1 USART block diagram

In this section, USART and SPIN are introduced in block diagrams.

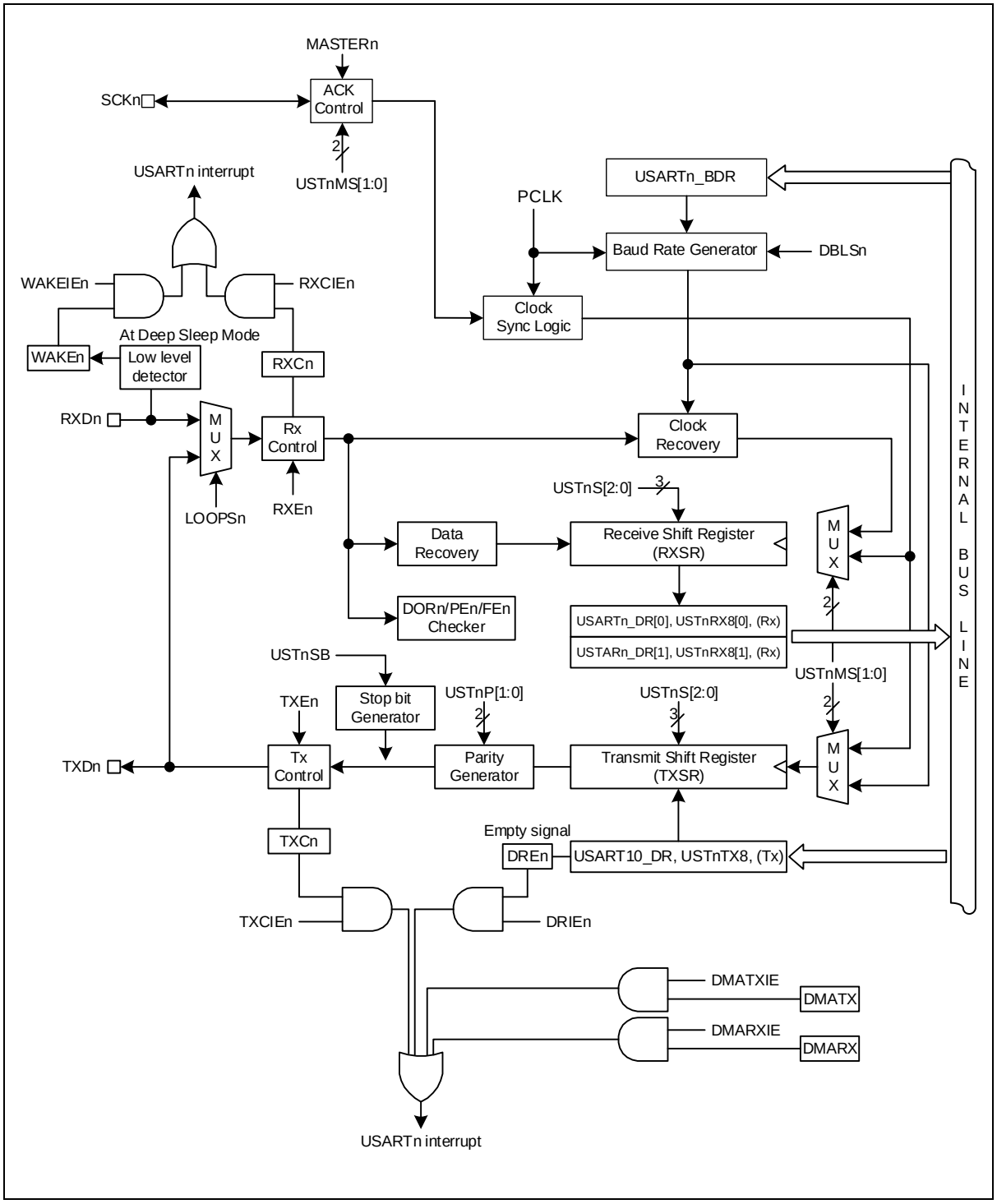


Figure 35. UART Block Diagram (n = 10, 11)

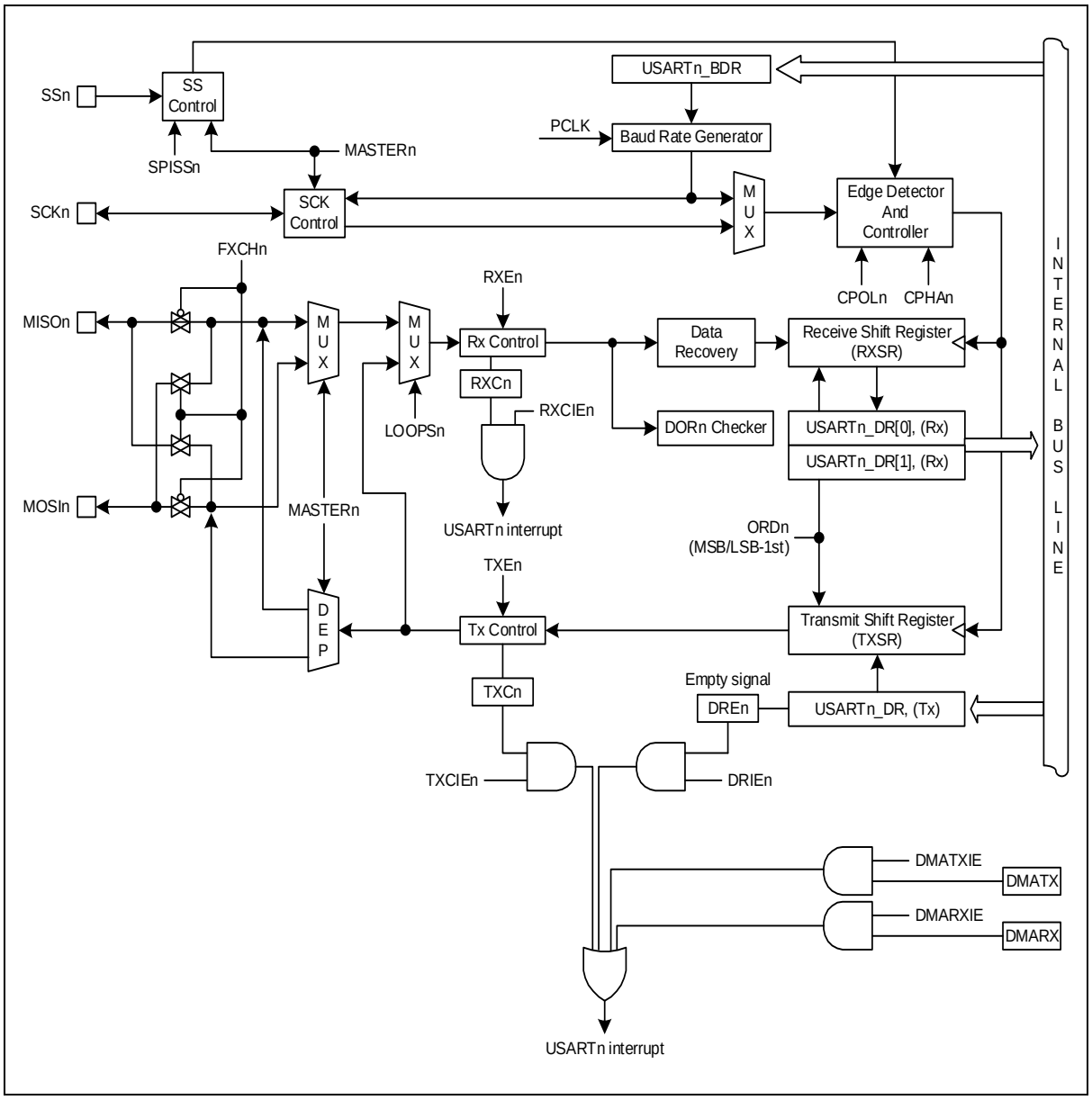


Figure 36. SPIN Block Diagram (n = 10, 11)

15 Universal Synchronous Receiver/ Transmitter (UART)

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

Table 18 introduces pins assigned for the USART.

Table 18. Pin Assignment of USART: External Pins

Pin name	Type	Description
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

15.1 USART block diagram

In this section, USART and SPIN are introduced in block diagrams.

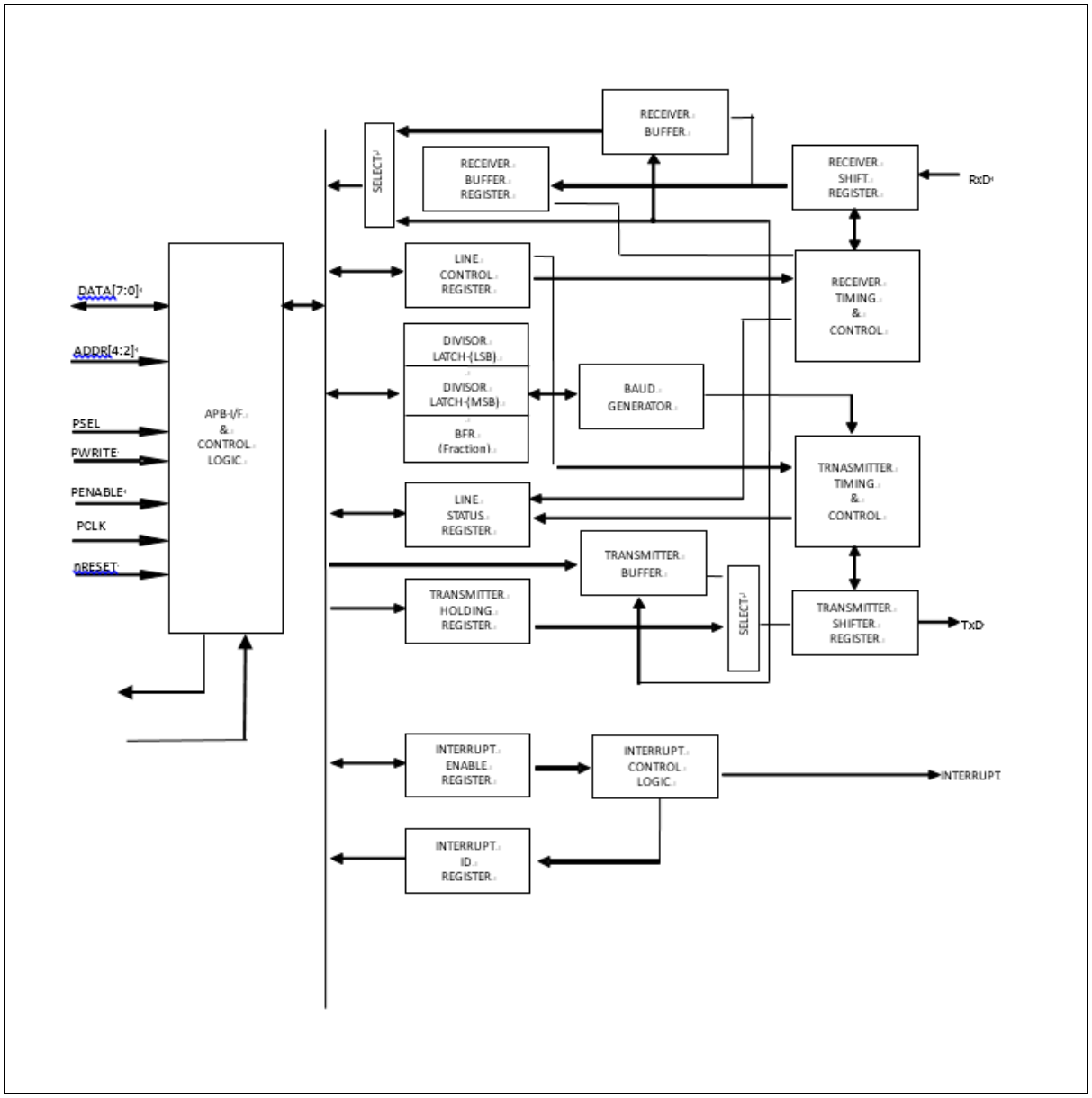


Figure 37. UART Block Diagram

16 I2C interface

I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines such as Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor respectively.

I2C features the followings (n = 0 and 1):

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 400KHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Table 19 introduces pins assigned for I2C interface.

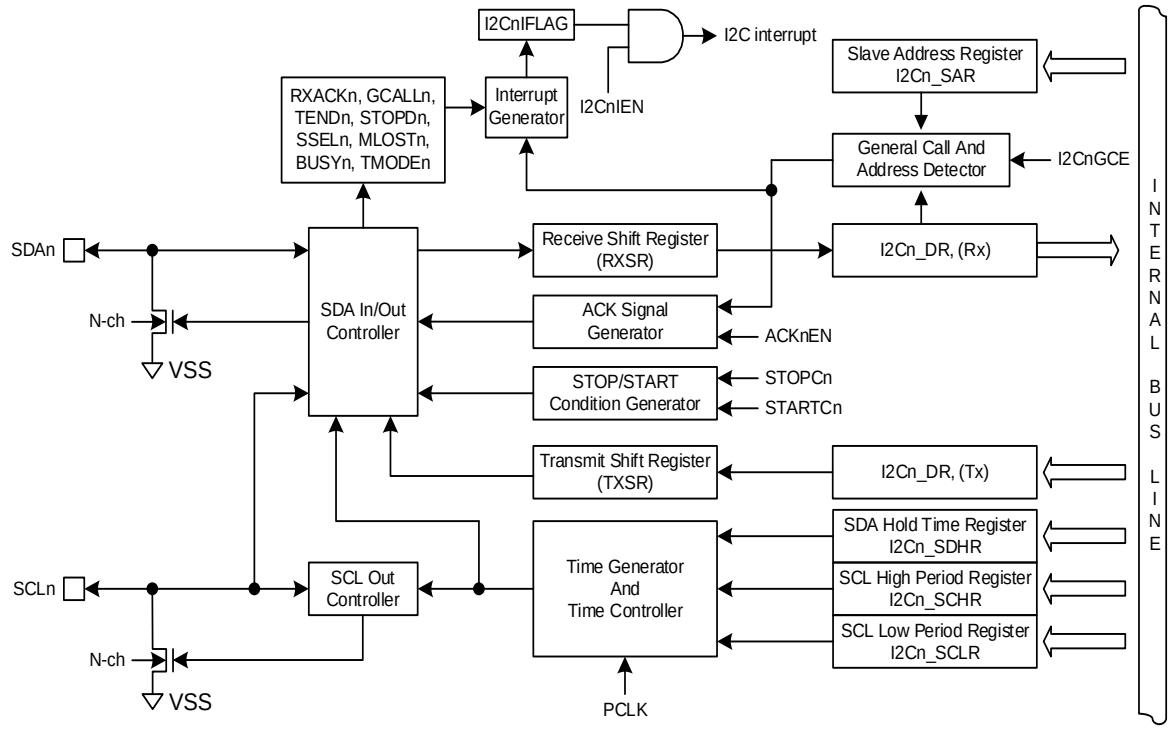
Table 19. Pin Assignment of I2C: External Pins

Pin name	Type	Description
SCL0	I/O	I2C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I2C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I2C channel 1 Serial clock bus line
SDA1	I/O	I2C channel 1 Serial data bus line

NOTE: n = 0 and 1

16.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.



NOTE: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 38. I2C Block Diagram

17 Serial Peripheral Interface (SPI)

A channel serial interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. Four signals will be used for SPI communication such as SS, SCK, MOSI, and MISO.

SPI of A31G21x series features the followings:

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

Table 20 introduces pins assigned for SPI.

Table 20. Pin Assignment of SPI: External Pins

Pin name	Type	Description
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 20 and 21

17.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 39.

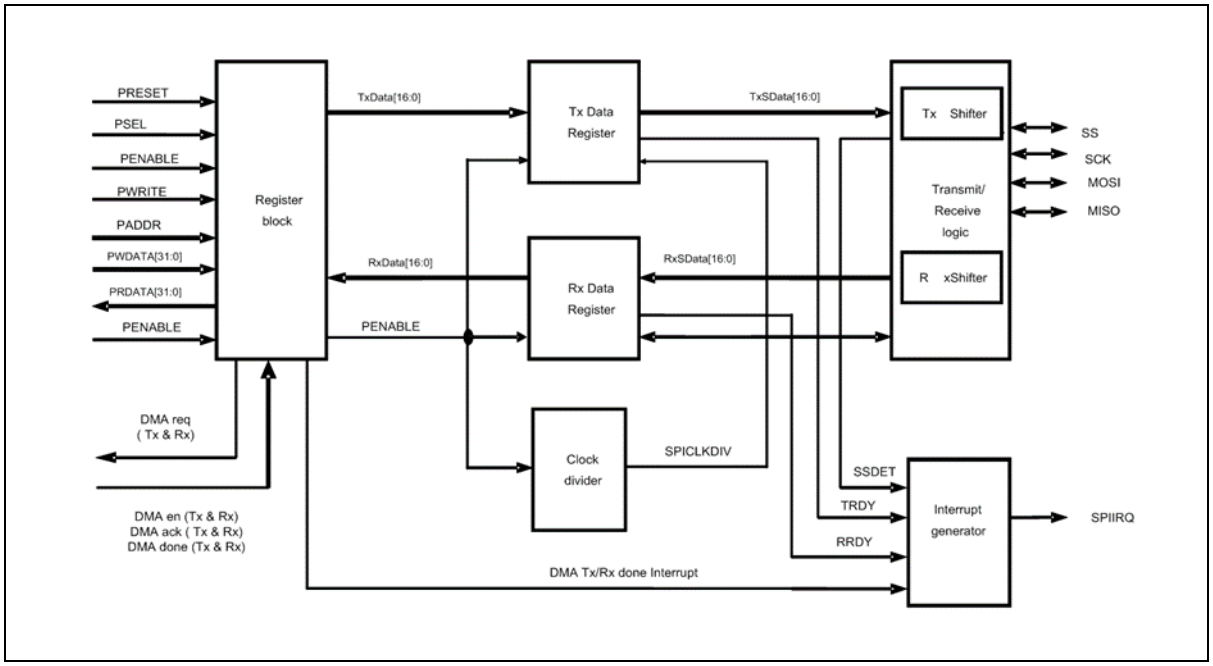


Figure 39. SPI Block Diagram

18 12-bit ADC

Analog-to-digital converter (A/D) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has 14 analog inputs. The output of the multiplexer is the input into the converter which generates the result through successive approximation.

The A/D module has three registers which are the A/D converter control register (ADC_CR), A/D converter data register (ADC_DR) and A/D converter prescaler data register (ADC_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC_DRH and ADC_DRL contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC_DR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

ADC block of A31G21x series consists of an independent ADC unit featuring the followings:

- 14 channels of analog inputs
- S/W (ADST) and timer trigger: support "TIMER10/11/12 A match and ADC trigger signal from TIMER30"
- Maximum 4.5MHz conversion rate (Max. 150Ksps)
- Conversion time : 30 clock
- 6-bit prescaler

Table 21 introduces pins assigned for ADC.

Table 21. Pin Assignment of ADC: External Signal

Pin name	Type	Description
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13

18.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 40.

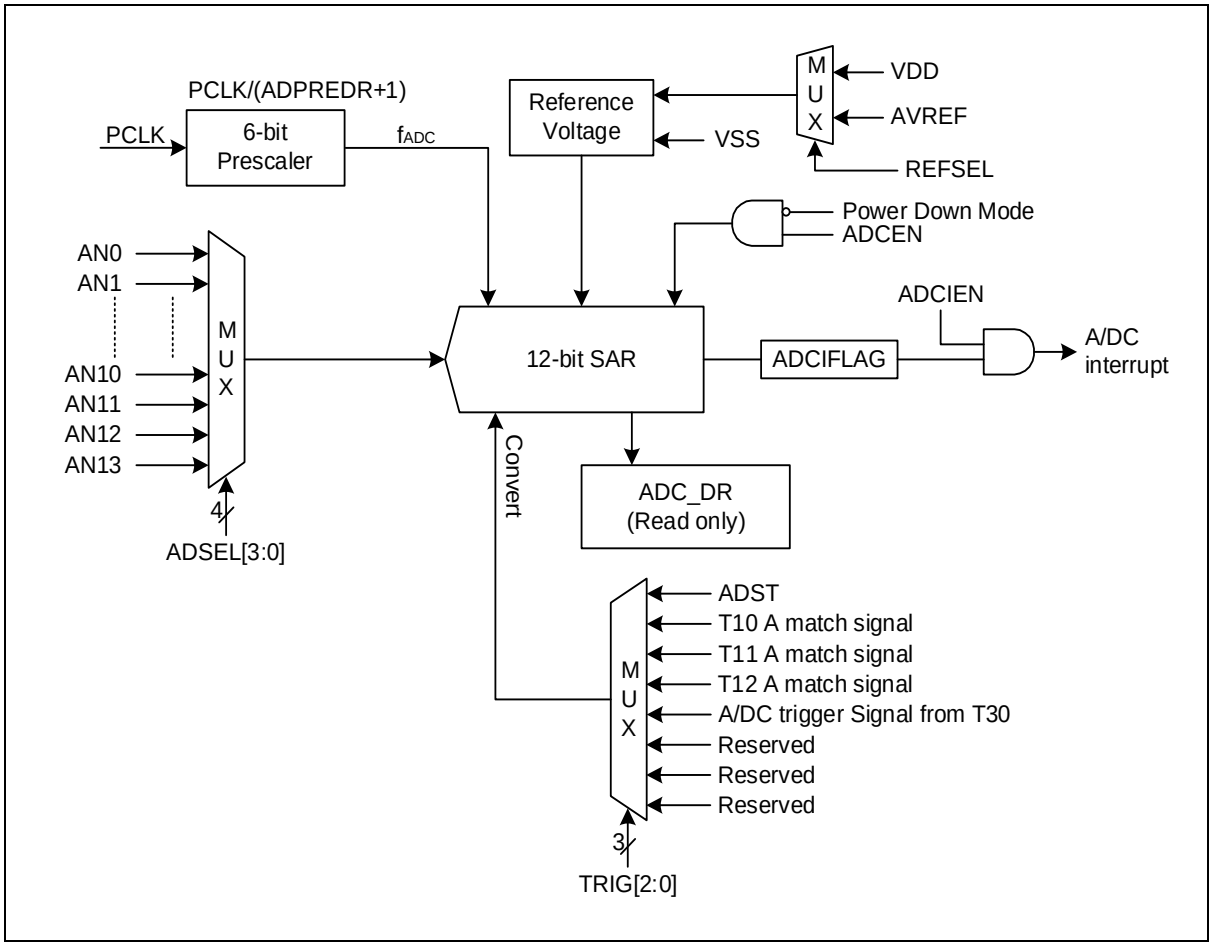


Figure 40. 12-bit ADC Block Diagram

19 5-bit DAC

Digital-to-analog (D/A) converter uses successive approximation logic to convert 5-bit digital value to an analog output level.

Table 22 introduces pins assigned for ADC.

Table 22. Pin Assignment of ADC: External Signal

Pin name	Type	Description
DAO	A	D/A converter Output

19.1 5-bit DAC block diagram

In this section, 5-bit DAC is described in a block diagram in Figure 41.

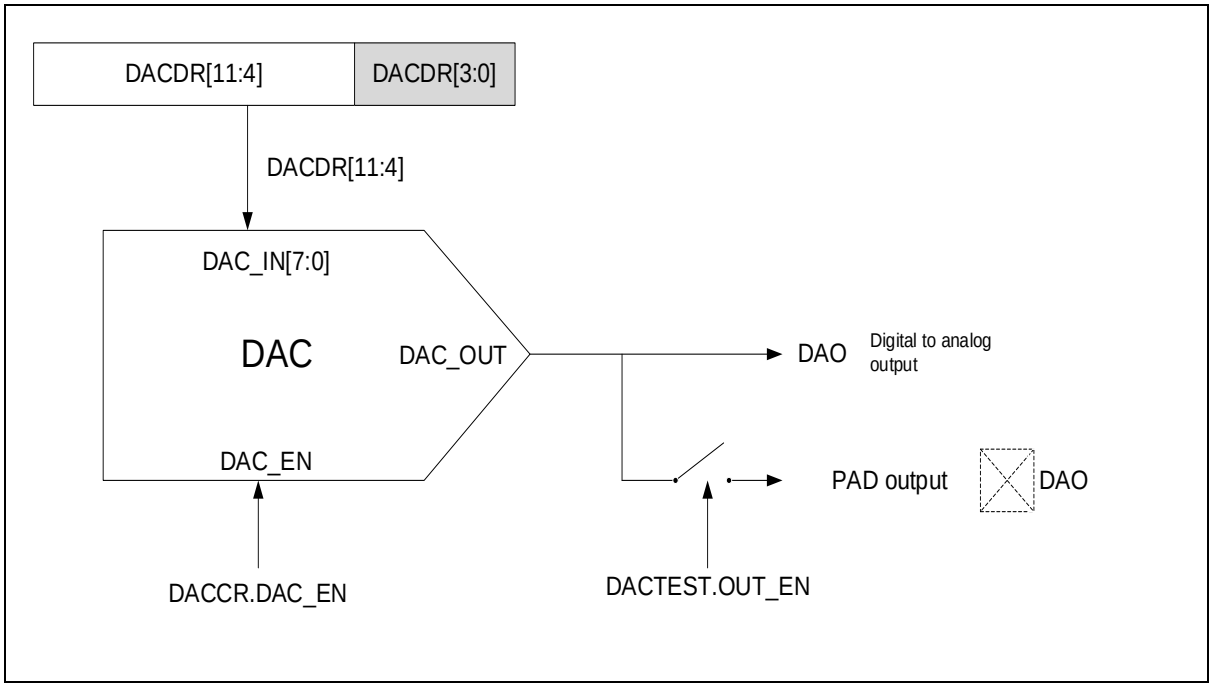


Figure 41. 5-bit DAC Block Diagram

20 Touch sensor system

Capacitive touch sensor systems are typical human machine interfaces (HMI) which operate by detecting changes in electrostatic capacitance produced by the touch of a finger or other conductor.

The use of capacitive touch technology can easily improve reliability in product design, and enhance the end-user experience. It also enables manufacturing costs to be lowered in a wide range of fields such as household appliances (white goods), healthcare devices, and other electric and electronic equipment.

The comparator features the followings:

- Self-Capacitive Touch Key Sensor.
- Total 24-channel Touch Key Support.
- 16-bits Sensing Resolutions.
- Fast Initial Self Calibration.
- Key Detection mode: Single/Multi mode.
- The Improvement of the SNR by Bias-Calibration in Analog Sensing Block

Table 23 introduces pins assigned for TOUCH

Table 23. Pin Assignment of Touch: External Pins

Pin name	Type	Description
CS0 to CS23	IA	Capacitive Touch switch input

20.1 Touch block diagram

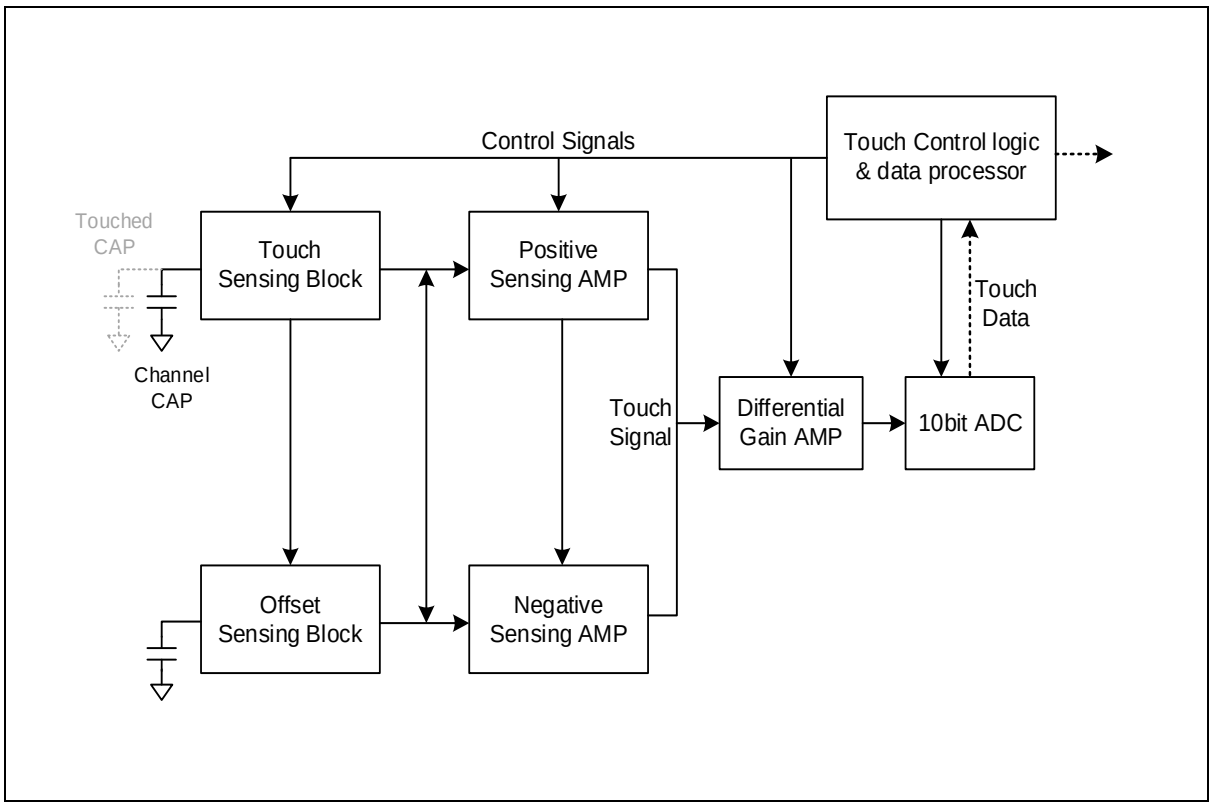


Figure 42. Touch Block Diagram

21 LED driver

LED drive contains 16 COM X 10 SEG output pin.

The controller consists of display data RAM memory, COM and SEG generator.

COM0-COM15 and SEG0-SEG9 pin can also be used as I / O pins. COMOE1, COMOE2 and SEGOE1, SEGOE2 registers are used to select SEG0-9, COM0 – COM15. During reset procedures from power-on, reset-input, low voltage or watchdog timer, LEDs are turned off.

The comparator features the followings:

- 16 COM X 10 SEG
- COM0-COM15 and SEG0-SEG9 pin

Table 24 introduces pins assigned for ADC.

Table 24. Pin Assignment of LED: External Signal

Pin name	Type	Description
COM0 to COM15	O	LED common signal outputs
SEG0 to SEG9	O	LED segment signal outputs

21.1 LED block diagram

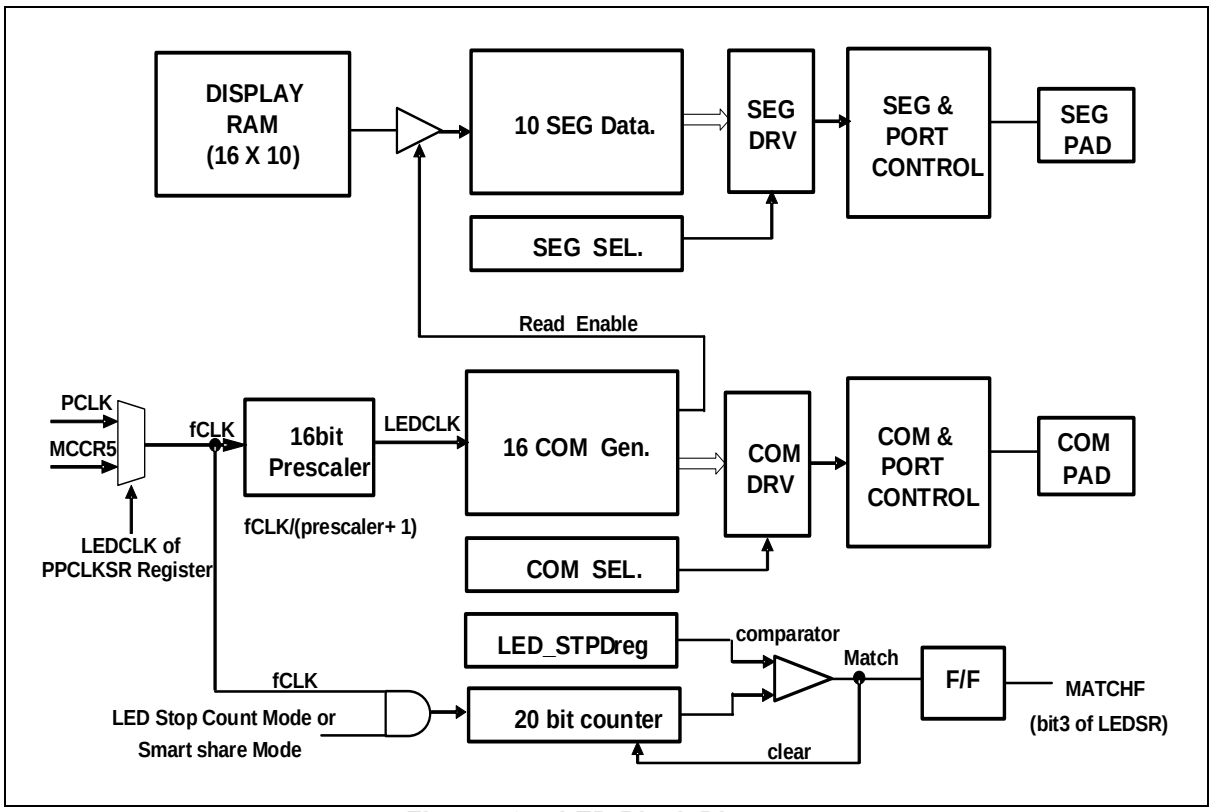


Figure 43. LED Block Diagram

22 Cyclic Redundancy Check and checksum (CRC checksum)

Cyclic redundancy check (CRC) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

CRC generator of A31G21x series features the followings:

- Auto CRC (DMA) and User CRC Mode.
- Polynomial:
  - CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
  - CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC Mode and Checksum Mode.

22.1 CRC and checksum block diagram

Figure 44 describes the CRC and checksum in a block diagram.

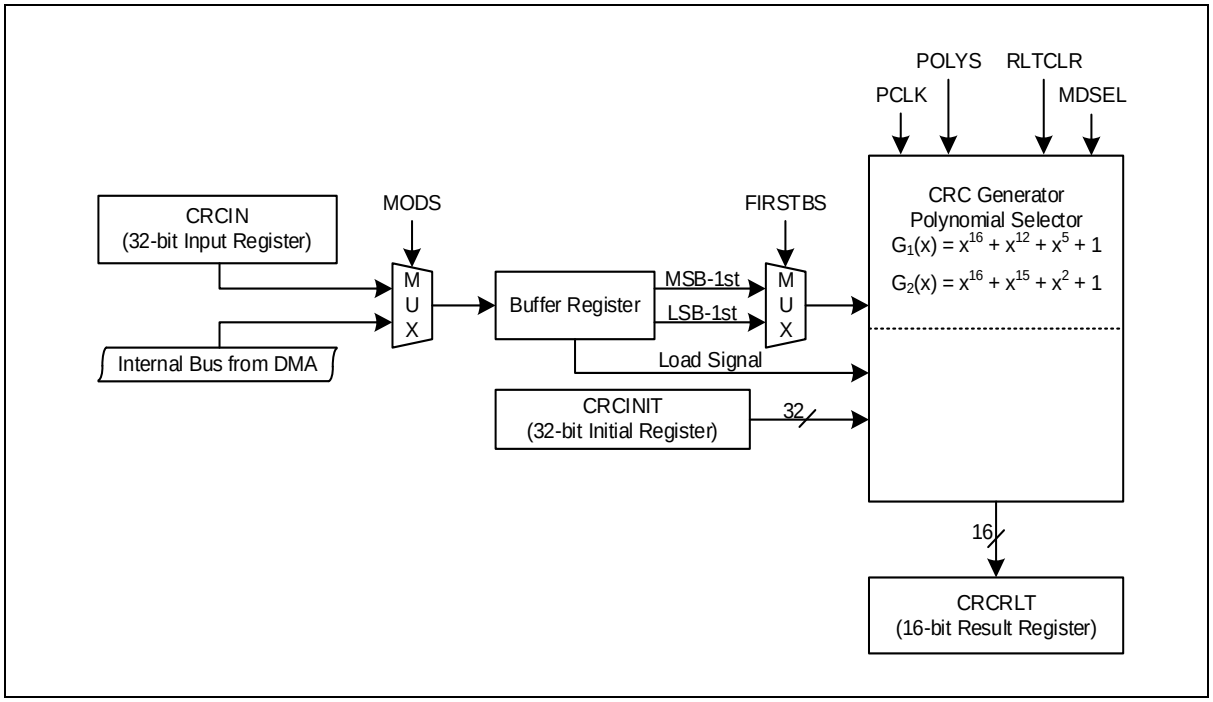


Figure 44. CRC and Checksum Block Diagram

23 Electrical characteristics

23.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 25. Absolute maximum rating

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage	VDD	-0.3 to +6.5	V	—
Normal pin	V_I	-0.3 to VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD+0.3	V	
	I_{OH}	-20	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-100	mA	Maximum current (ΣI_{OH})
	I_{OL}	25	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	210	mA	Maximum current (ΣI_{OL})
Total power dissipation	T_P	300	mW	—
Storage temperature	T_{STG}	-45 to +125	℃	—

23.2 Recommended operating conditions

Table 26. Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply voltage	VDD	Logic block	1.8	—	5.5	V
		Touch	2.7	—	5.5	V
		LED	3.3		5.5	
Operating frequency	FREQ	HSE	2	—	16	MHz
		LSE	—	32.768	—	KHz
		HSI	31.52	32	32.48	MHz
		LSI500KHz	400	500	600	KHz
		LSI40KHz	22.8	40	62.6	KHz
Operating temperature	Top	VDD = 1.8 to 5.5V (Commercial grade)	-40	—	+85	℃
		VDD = 1.8 to 5.5V (Industrial grade)	-40		+105	℃

23.3 ADC characteristics

Table 27. ADC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Operating voltage	AVDD		2.4	5	5.5	V
Resolution				12		Bit
Operating current	IDDA	AVDD = 5.0VA		1	2	mA
Analog input range	V_{AN}		VSS		AVREF	V
Conversion rate	F_{CONV}			—	150	Ksps
Operating frequency	ACLK				4.5	MHz
Integral Non-Linearity Differential Non-Linearity	INL	AVDD=2.4V < AVDD < 5.5V,T_A = 25 °C		±4	±10	LSB
	DNL			±1	±4	LSB
Top Offset Error(FSE)	TOE			±6	±12	LSB
Zero Offset Error	ZOE			±4	±8	LSB

23.4 Power on reset characteristics

Table 28. POR Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	IDD	—	-	60	-	uA
POR set level	V_{set}	—	1.05	1.2	1.35	V
POR reset level	V_{reset}	—	1.0	1.1	1.2	V

23.5 Low voltage reset/indicator characteristics

Table 29. Low Voltage Reset/Indicator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection level	V_{LVR}	Falling Voltage (Error rate 5%)		1.60		V
				1.69		
				1.78		
				1.90		
				1.99		
				2.12		
				2.30		
				2.47		
				2.67		
				3.04		
				3.18		
				3.59		
				3.72		
				4.03		
				4.20		
				4.48		
Hysteresis	-		-	100	200	mV
Noise cancelling time	-		-	2	-	us
Operation current	I_{DD}		-	3.5	5	uA
Operation current(stop)	$I_{DD, STOP}$		-	2.5	3	nA

23.6 High frequency internal RC oscillator characteristics

Table 30. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HSI}	VDD = 1.8V to 5.5V	31.52	32	32.48	MHz
Tolerance		T_A = – 40 °C to + 85 °C (Commercial grade)	–	–	±1.0	%
		T_A = – 40 °C to + 105 °C (Industrial grade)	–	–	±1.5	
Clock duty ratio	T_{OD}	–	–	50	–	%
Stabilization time	t_{HFS}	–	–	–	–	us
Irc current	I_{HSI}	Enable	–	190	–	uA
		Disable	–	1	--	uA

23.7 Low frequency internal RC oscillator characteristics

Table 31. Low Frequency (500KHz) Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		1.8	5	5.5	V
Operating current	I_{LIRC}	Enable	—	1.5	2	uA
		Disable	—	1	20	nA
Frequency	f_{LIRC}	VDD = 1.8V to 5.5V	400	500	600	KHz
Stabilization time	t_{LFS}	—	—	100		us

23.8 Touch Switch characteristics

Table 32. Touch Switch Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{DD}	–	2.7	-	5.5	V
	V_{DDA}	–	2.7	-	5.5	V
VDC Voltage	V_{CCL}	From MCU	–	1.9	–	V
SNR(Signal-toNoise Ratio)	SNR	–	–	20	–	dB
Self-Calibration Time	T_{CAL}	–	–	10	–	ms
Scan Speed	T_{SCAN}	–	–	10	–	ms
Supply Current	I_{DD}	–	–	1	–	mA
Operation Temperature	T_{OPER}	VDD = 2.7 – 5.5V (Commercial grade)	-40	–	+85	℃
		VDD = 2.7 – 5.5 V(Industrial grade)	-40	–	+105	℃

23.9 LED Driver characteristics

Table 33. LED Driver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{Ddext}		3.3	–	5.5	V
Operating Temperature	T_A	Commercial grade	-40	–	85	℃
		Industrial grade	-40	–	105	℃
COM output leakage	I_{CLKG}		-1		1	uA
SEG output leakage	I_{SLKG}		-1		1	uA
SEG Current	I_{SEG}	V_{Ddext} = 3.3V ,V_{OL_LED} = 0.3V	23	–	–	mA

23.10 DC electrical characteristics

Table 34. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins, nRESET	0.8VDD	-	VDD	V
	V_{IH2}	PF5,PF6,PF7 are input 1.8V level	0.9	-	VDD	
Input low voltage	V_{IL1}	All input pins, nRESET	0	-	0.2VDD	V
	V_{IL2}	PF5,PF6,PF7 are input 1.8V level	0	-	0.6	
Output high voltage	V_{OH1}	VDD=5V, I_{OH1} = – 2.36mA	0.8VDD	-	VDD	V
Output low voltage	V_{OL1}	VDD=5V, I_{OL1} = 4.86mA	0	-	0.2VDD	V
Input high leakage Current	I_{IH}	All Input ports	-4	-	-	uA
Input low leakage current	I_{IL}	All Input ports	-	-	+4	uA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, All Input ports	40	-	70	KΩ
		V_I=0V, T_A=25°C, nRESET PIN		250		
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, All Input ports	40	-	70	KΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=5V		1		MΩ

23.11 Supply current characteristics

Table 35. Supply Current Characteristics

Parameter	Symbol	Conditions		Typ	Max	Units
Supply current	I_{DD1} (Run)	f_{XIN} = 8MHz	VDD=5V±10%	4.0	12.0	mA
		f_{HSI} = 32MHz		10.0	30.0	
		f_{HSI} = 8MHz		3.5	10.0	
		f_{LSI} = 500KHz		200	600	uA
		F_{LSE} = 32.768KHz		140	300	
	I_{DD2} (Sleep)	f_{XIN} = 8MHz		5	15	mA
		f_{HSI} = 32MHz		6	18	
		f_{HSI} = 8MHz		2	6	
		f_{LSI} = 500KHz		180	500	uA
		F_{LSE} = 32.768KHz		130	400	
	I_{DD3} (Deep Sleep)	WDT block(WDTRC) ON, LVD ON T_A = 25 °C		8		uA
	I_{DD4} (Deep Sleep)	WDT block(WDTRC) ON, LVD OFF T_A = 25 °C		6		
	I_{DD5} (Deep Sleep)	WDT block(WDTRC) OFF, LVD ON T_A = 25 °C		4		uA
	I_{DD6} (Deep Sleep)	WDT block(WDTRC) OFF, LVD OFF T_A = 25 °C		2		
		WDT block(WDTRC) OFF, LVD OFF T_A = 85 °C		10		
		WDT block(WDTRC) OFF, LVD OFF T_A = 105 °C		30		

NOTES:

1. All supply current items don't include the current of a low frequency internal RC oscillator and a peripheral block.
2. All supply current items include the current of the power-on reset (POR) block.

23.12 AC characteristics

Table 36. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 5V	10	—	—	us
Interrupt input high low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 5V	100	—	—	ns
External counter input high low pulse width	t_{ECWH}, t_{ECWL}	VDD = 5V All external counter input	100	—	—	
External counter transition time	t_{REC}, t_{FEC}	Ecn, VDD = 5V All external counter input	—	—	20	

NOTE: Data based on characterization results, not tested in production.

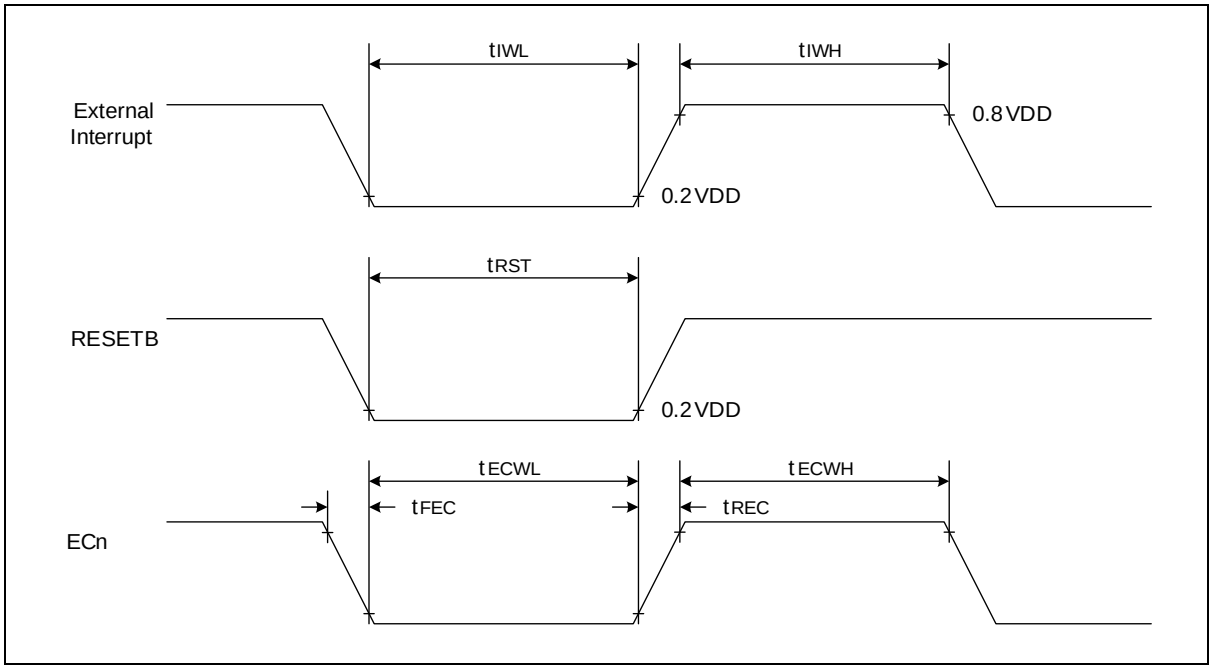


Figure 45. AC Timing

23.13 SPI characteristics

Table 37. SPI Characteristics (2.7 -5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Clock Pulse Period	t_{SCK}	Internal SCK source	400	–	–	ns
Input Clock Pulse Period		External SCK source	400	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	180	–	–	
Input Clock High, Low Pulse Width		External SCK source	180	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	200	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	100	
Input Setup Time	t_{DIS}	–	180	–	–	
Input Hold Time	t_{DIH}	–	180	–	–	

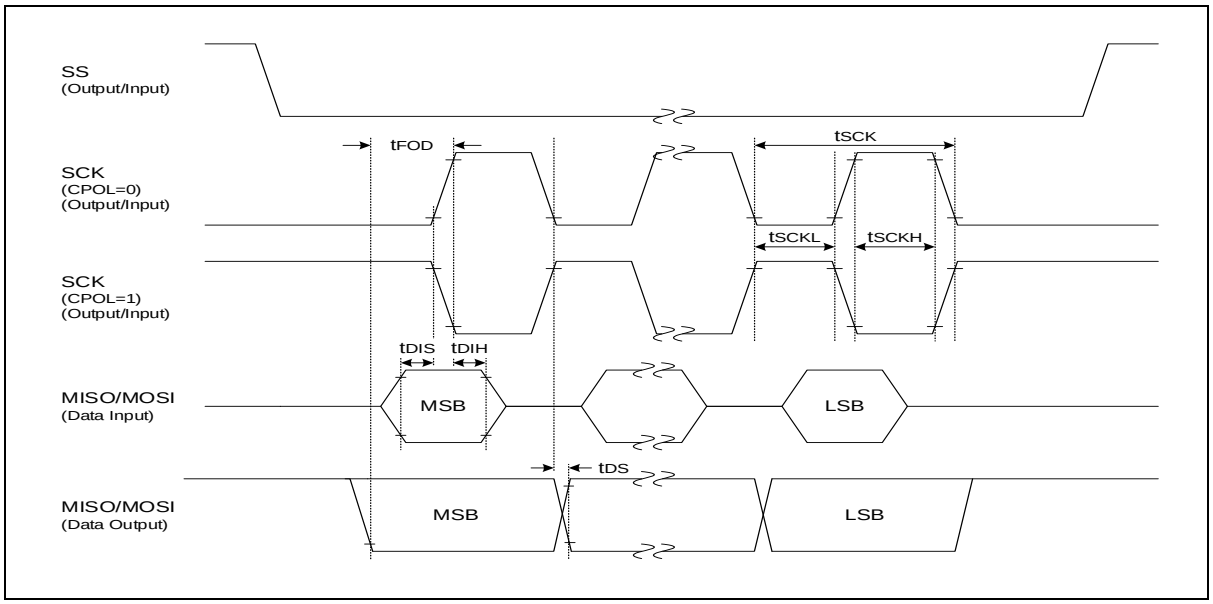


Figure 46. SPI Timing

23.14 I2C characteristics

Table 38. I2C Characteristics

(VDD = 1.8 to 5.5V)

Parameter	Symbol	Min	Max	Units
Clock frequency	t_{SCL}	0	400	KHz
Clock high pulse width	t_{SCLH}	0.6	—	us
clock low pulse width	t_{SCLL}	1.3	—	
Bus free time	t_{BF}	1.3	—	
Start condition setup time	t_{STSU}	0.6	—	
Start condition hold time	t_{STHD}	0.6	—	
Stop condition setup time	t_{SPSU}	0.6	—	
Stop condition hold time	t_{SPHD}	0.6	—	
Output valid from clock	t_{VD}	0	—	
Data input hold time	t_{DIH}	0	1.0	
Data input setup time	t_{DIS}	100	—	ns

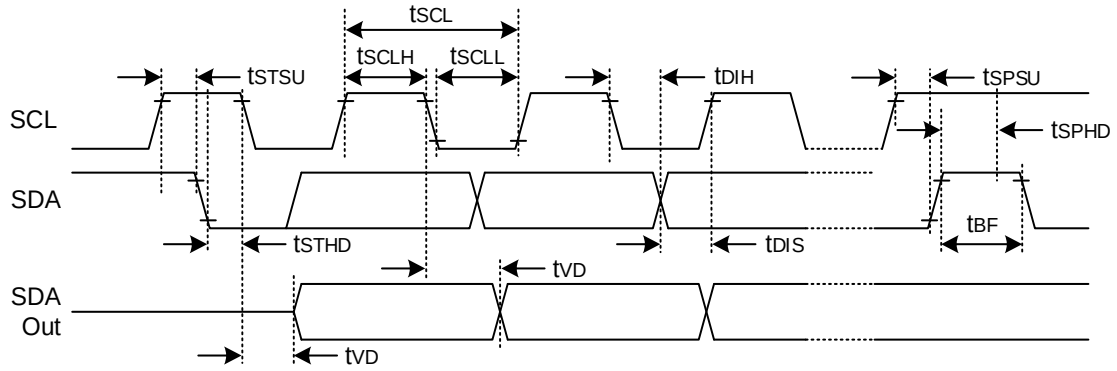


Figure 47. I2C Timing

23.15 USART UART timing characteristics

Table 39. UART Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	—	
Clock rising edge to input data valid	t_{S2}	—	—	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	—	
Input data hold after clock rising edge	t_{H2}	0	—	—	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

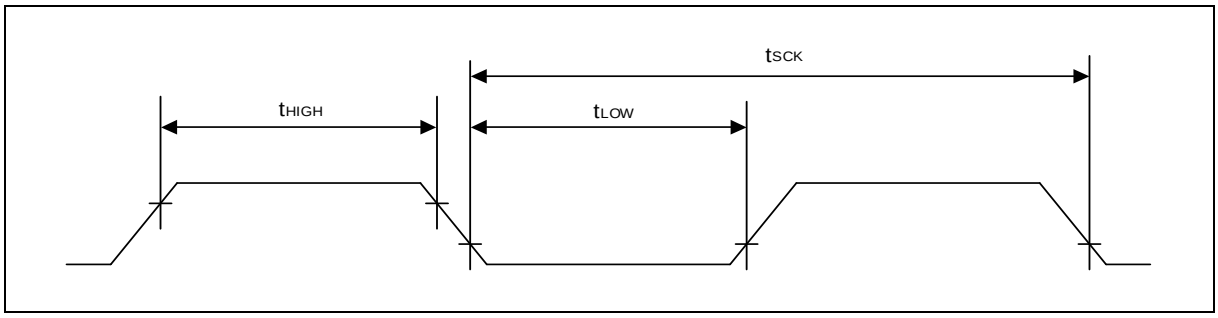


Figure 48. Waveform of UART Timing Characteristics

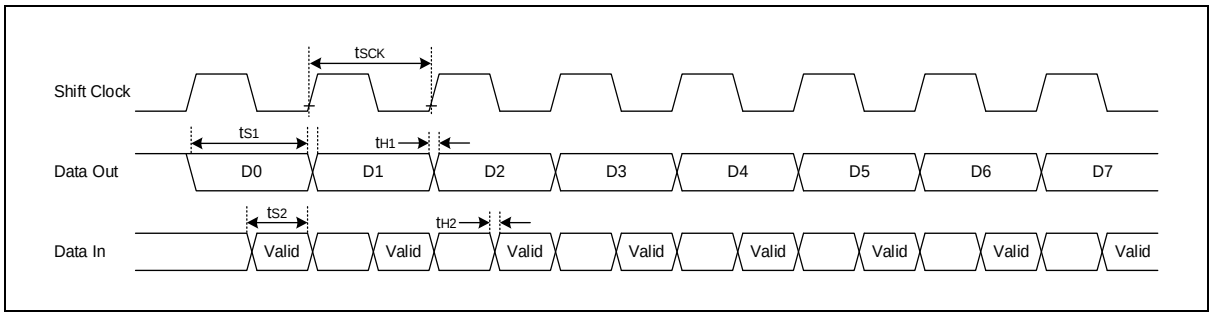


Figure 49. UART Module Timing

23.16 Data retention voltage in stop mode

Table 40. Data Retention Voltage in Stop mode

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	—	1.8	—	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8V, (T_A = 25°C), Deep sleep mode	—	—	1	uA

23.17 Internal Flash ROM characteristics

Table 41. Internal Flash ROM Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Cycle Time	fRSTBUSY	–	5.6	8	10.4	us
Fuse Program Cycle Time	fFRDBUSY		4.2	6	7.8	
Normal Program Cycle Time	tPGMBUSY		21	30	42	
Normal Page Erase Cycle Time	tPERSBUSY		2.8	4	5.2	ms
Sector Erase Cycle Time	tSERSBUSY		2.8	4	5.2	
Chip Erase Cycle Time	tMERSBUSY	–	5.6	8	10.4	
Flash Program Voltage	V_{PGM}	On erase/write	1.8	–	5.5	V
Endurance of Write/Erase	N_{FWE}	T_A=25 °C, Page unit	10,000	–	–	Times
Retention Time	t_{FRT}		10	–	–	Years

23.18 Input/Output Capacitance

Table 42. Input/ Output Capacitance

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f=500KHz Unmeasured pins are connected VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

23.19 Main oscillator characteristics

Table 43. Main Oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	1.8 V – 5.5 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	1.8 V – 5.5 V	2.0	–	16.0	

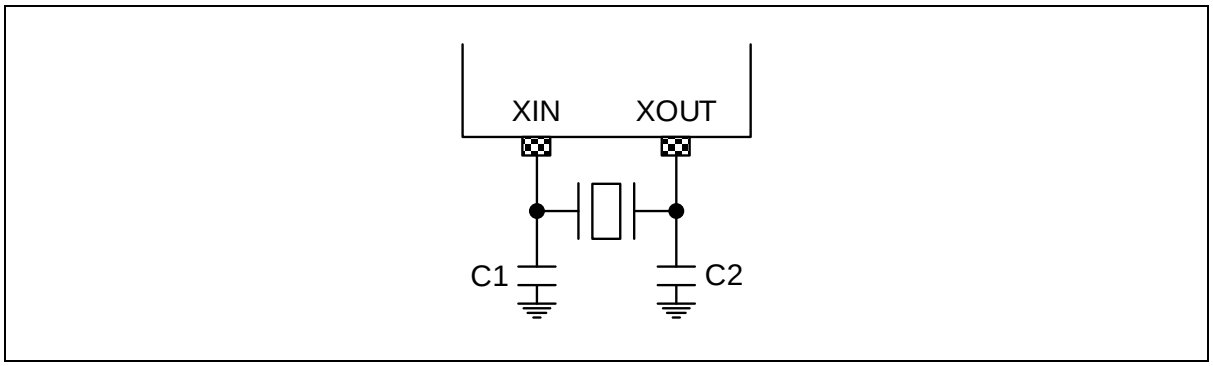


Figure 50. Crystal/Ceramic Oscillator

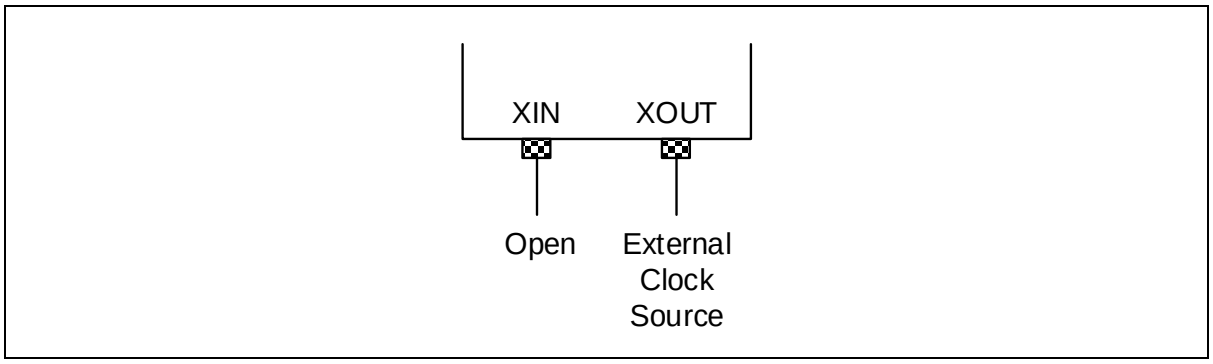


Figure 51. External Clock

23.20 Sub oscillator characteristics

Table 44. Sub Oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 5.5 V	32	32.768	38	KHz

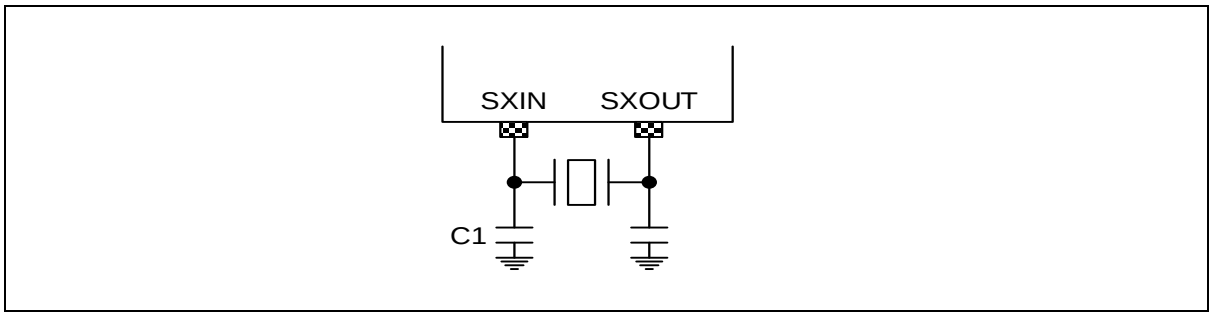


Figure 52. Crystal Oscillator

23.21 Main oscillator stabilization time

Table 45. Main Oscillation Stabilization Time

Oscillator	Conditions	Min	Typ	Max	Units
Crystal	f_{XIN} ≥ 2 MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	
External Clock	f_{XIN} = 2.0 to 40 MHz XIN input high and low width (t_{XL}, t_{XH})	12.5	–	250	ns

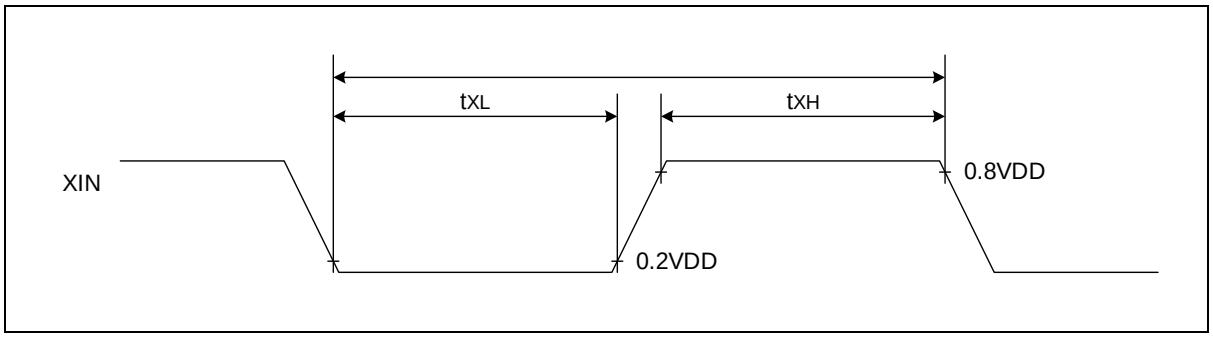


Figure 53. Clock Timing Measurement at XIN

23.22 Sub oscillator Stabilization time

Table 46. Sub Oscillation Stabilization Time

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD=3V, T_A=25°C	–	0.7	1.5	

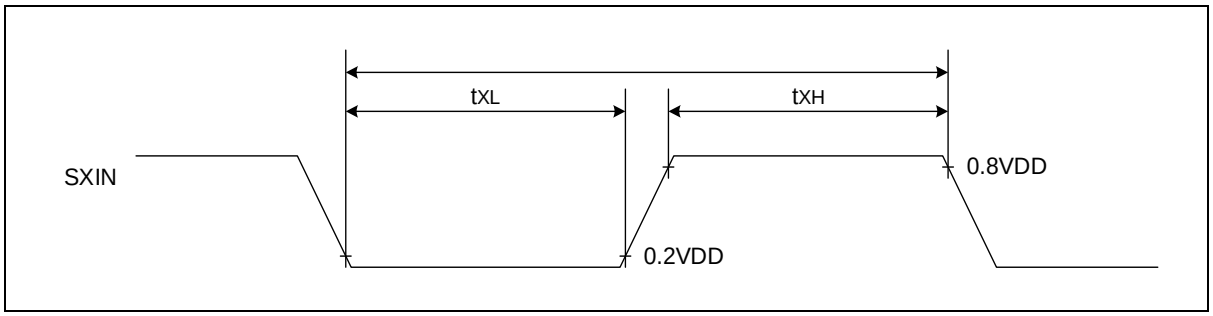


Figure 54. Clock Timing Measurement at SXIN

23.23 Operating voltage range

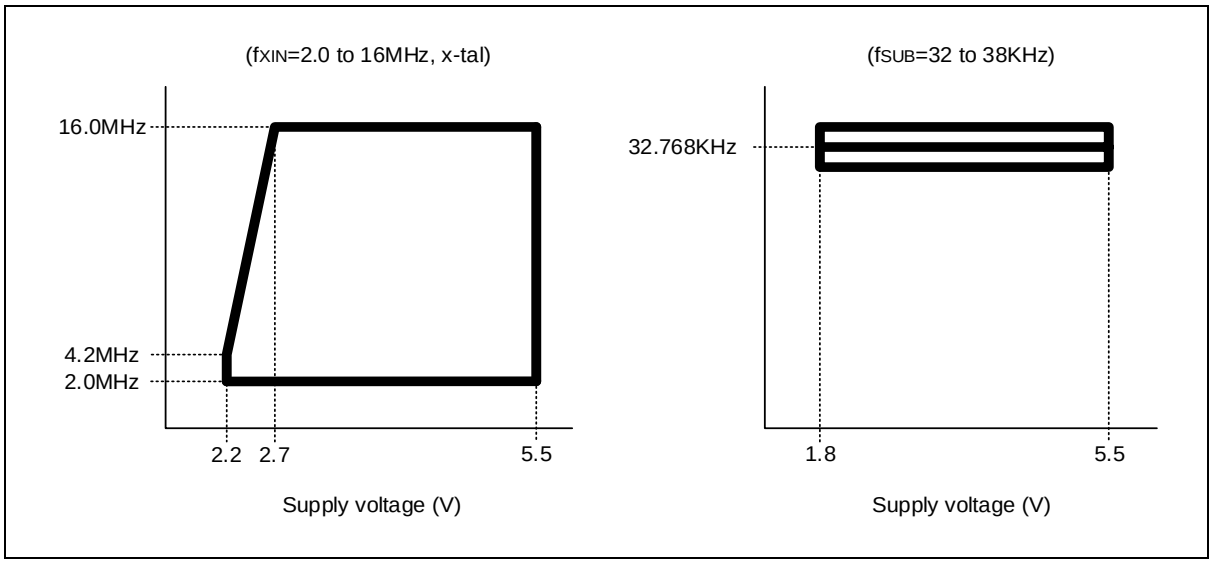


Figure 55. Operating Voltage Range

23.24 PLL electrical characteristics

Table 47. PLL Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency	f_{OUT}	–	-	-	48	MHz
Operating Current	I_{DD}		–	-	1	mA
Duty	f_{DUTY}		40	–	60	%
VCO	f_{VCO}		0.8	–	192	MHz
Input Frequency	f_{IN}		2	8	16	MHz
Locking Time	t_{LOCK}				190	us

23.25 D/A Converter characteristics

Table 48. D/A Converter Characteristics (V_{DD}=1.8-5.5V, V_{DD}=DAVREF, V_{ss}=0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution	-	-	-	-	5	Bit
Analog Output Voltage	D_{AOUT}		GND+0.02	-	AV_{DD}-0.02	V
Reference Input Voltage	EXTREF		2.7	-	AV_{DD}	V
Integral Nonlinearity	INL	@AVDD=5V or EXTREF_A=5V	-	-±1	±4	LSB
Differential Nonlinearity	DNL		-	±1	±2	LSB
D/AC Current	I_{DAC}		-	0.6	1.0	mA
Conversion Time	-		-	1	2	Us

24 Development tools

This chapter introduces wide range of development tools for A31G21x. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

24.1 Compiler

ABOV semiconductor does not provide any compiler for A31G21x. However, since A31G21x have ARM's high-speed 32-bit Cortex-M0+ Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

24.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A31G21x MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 56. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

Figure 56. A-Link and Pin Descriptions

24.3 Programmer

24.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

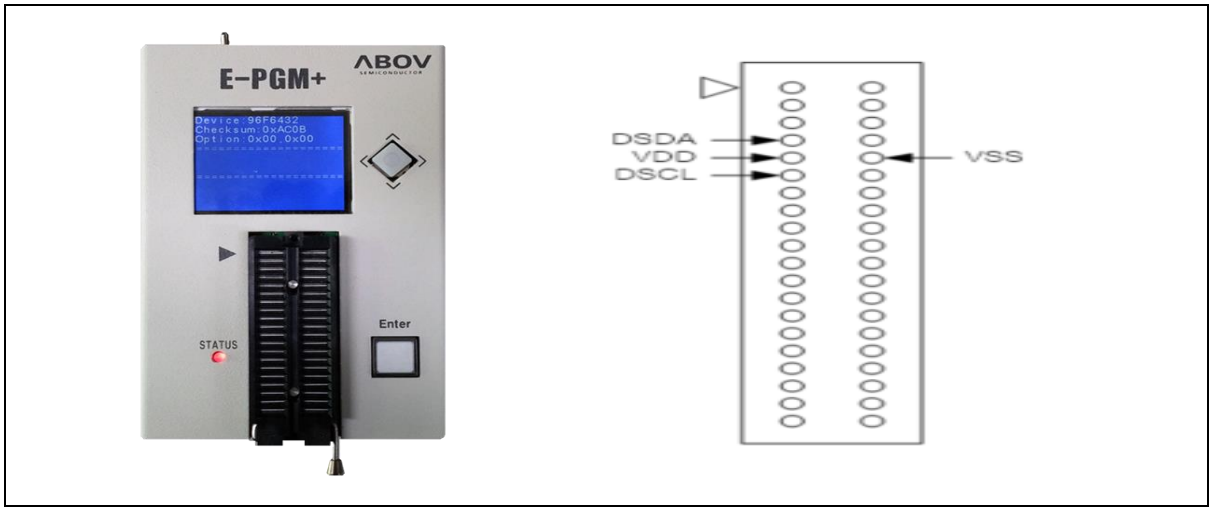


Figure 57. E-PGM+ (Single Writer) and Pin Descriptions

24.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 58. E-Gang4 and E-Gang6 (for Mass Production)

25 Circuit design guide

Refer to the Recommended Circuit and Layout Design as shown below.

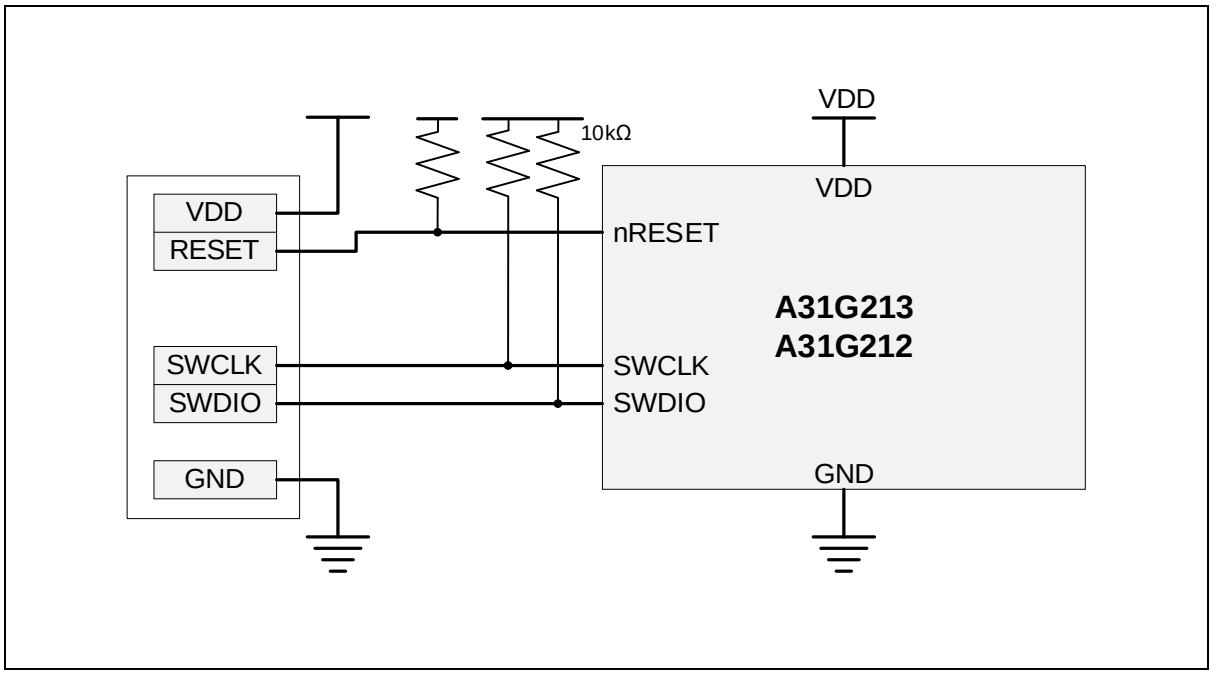


Figure 59. PCB Design Guide for On-Board Programming

26 Package information

This chapter provides A31G21x series package information.

26.1 48 LQFP package information

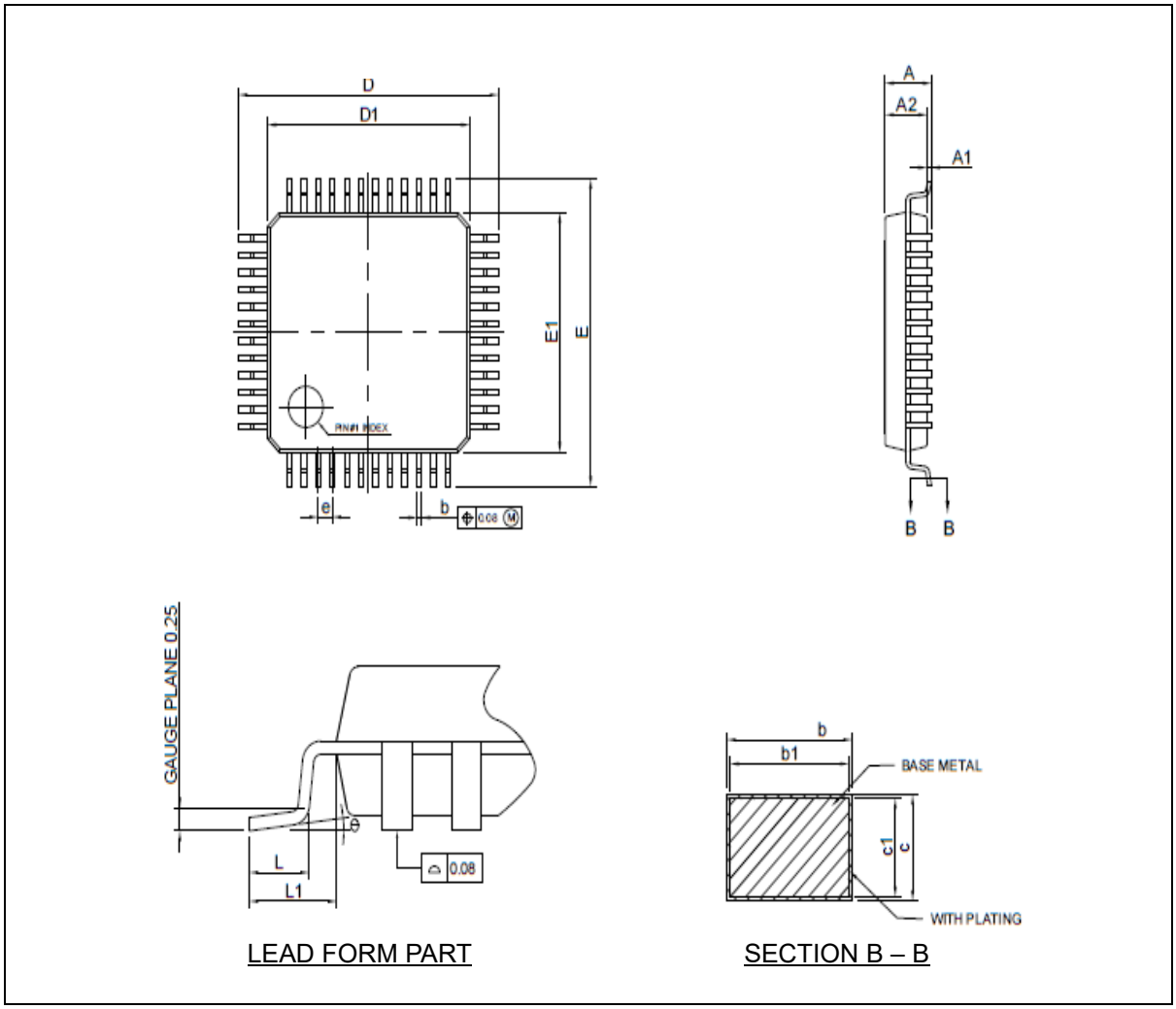


Figure 60. 48 LQFP Package Outline

Table 49. 48LQFP 7 x 7 Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimensions refer to JEDEC standard MS-026-BBC.
2. Dimensions ‘D1’ and ‘E1’ do not include mold protrusions. Allowable protrusion is 0.25mm per side. ‘D1 and ‘E1’ are maximum plastic body dimensions including mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

26.2 44 MQFP package information

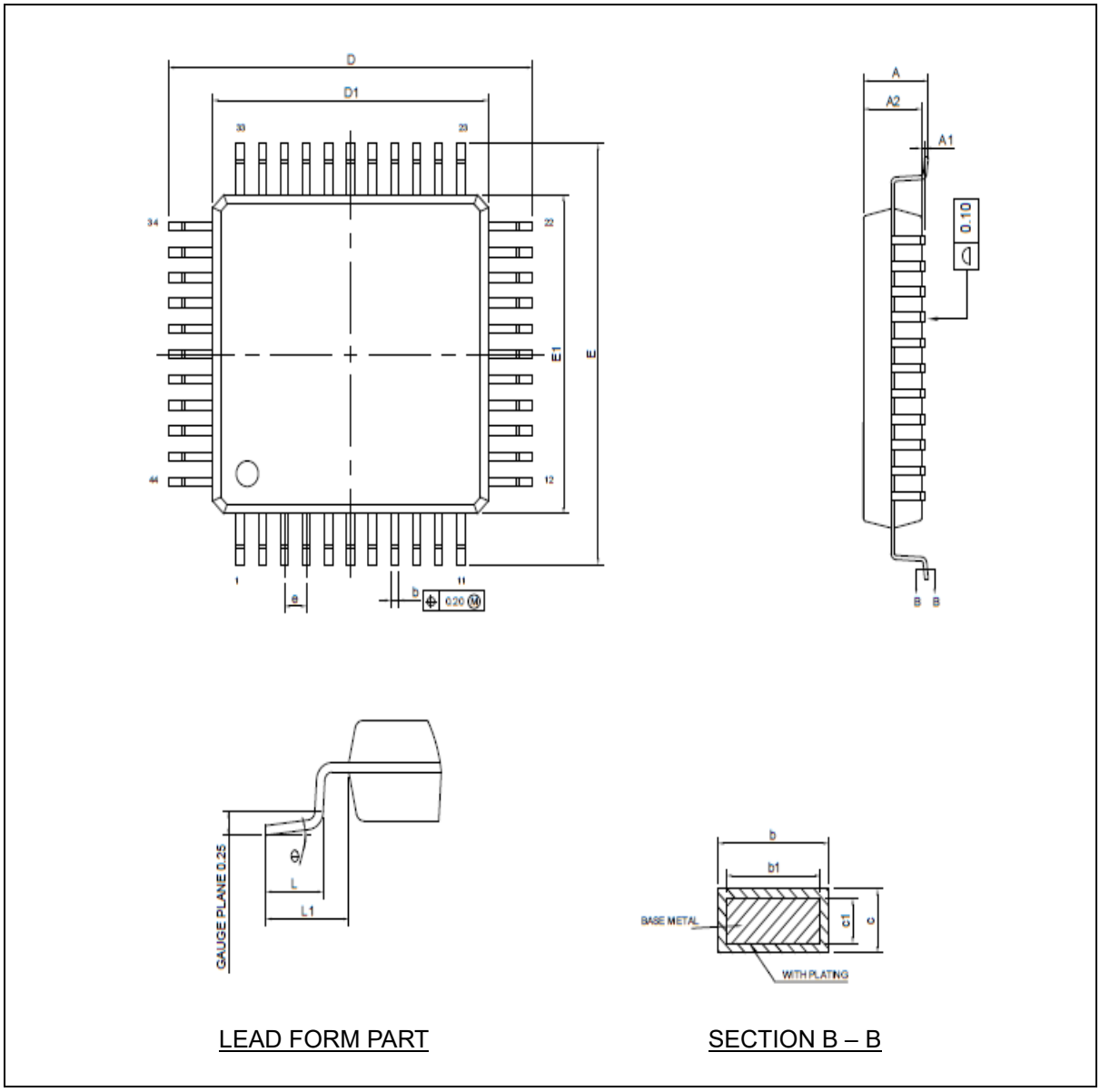


Figure 61. 44 MQFP Package Outline

Table 50. 44MQFP 10 x 10 Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	2.45
A1	0.00	—	0.25
A2	1.80	2.10	2.20
b	0.28	—	0.45
b1	0.28	0.35	0.41
c	0.11	—	0.23
c1	0.11	0.15	0.19
D	12.90	13.20	13.50
D1	9.80	10.00	10.20
E	12.90	13.20	13.50
E1	9.80	10.00	10.20
e	0.80 BSC		
L	0.60	—	1.03
L1	1.60 REF		
Θ	0°	—	8°

NOTES:

1. All dimension refer to JEDEC standard MS-022-AB.
2. Dimensions ‘D1’ and ‘E1’ do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions ‘D1 and ‘E1’ do not include mold mismatch.
3. Dimension ‘b’ does not include dambar protrusion. The dambar protrusion shall not cause the lead width to exceed the maximum ‘b’ dimension by more than 0.08mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

26.3 32 LQFP package information

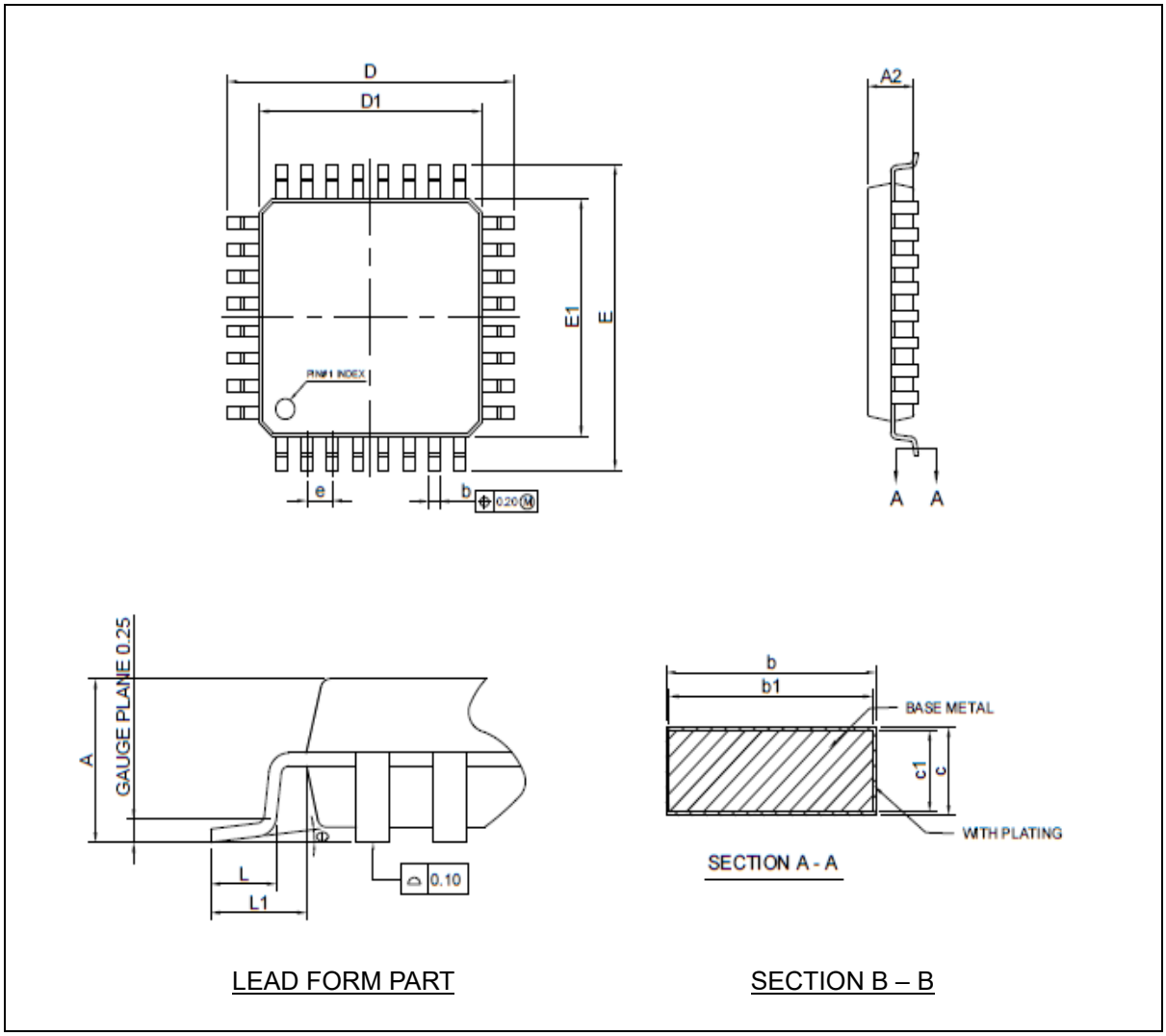


Figure 62. 32 LQFP Package Outline

26.4 32 QFN package information

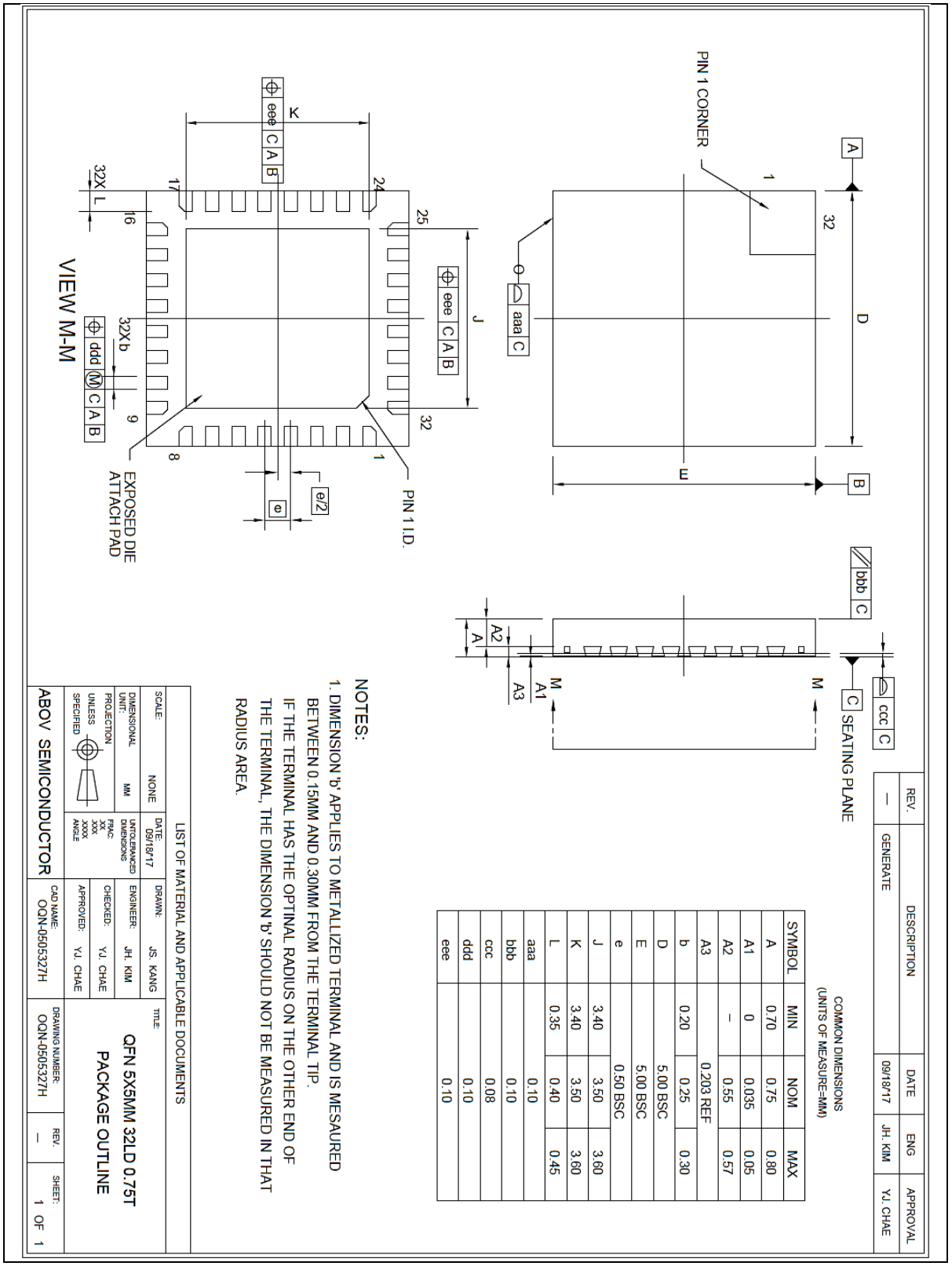


Figure 63. 32 QFP Package Outline

26.5 28 TSSOP package information

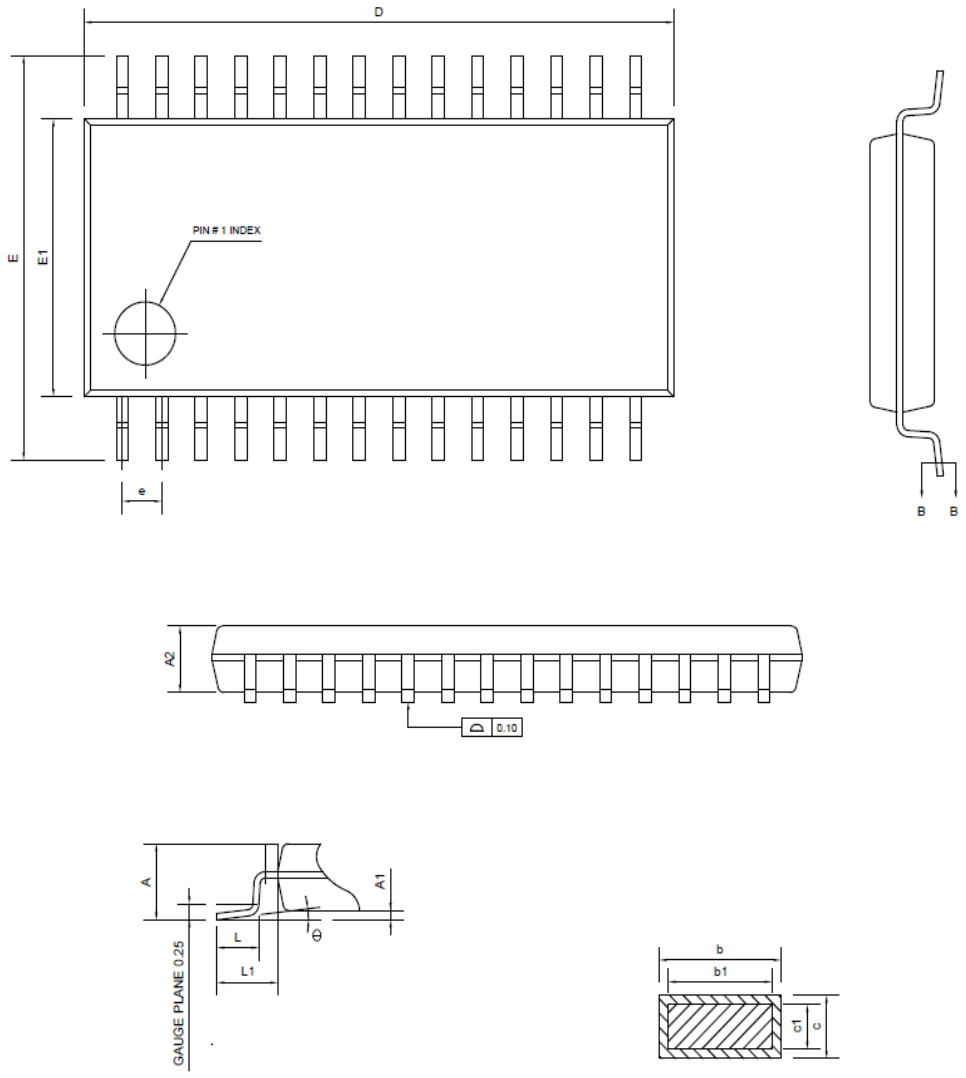


Figure 64. 28 TSSOP Package Outline

Table 51. 28 TSSOP 4.4MM Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	—	8°

NOTES:

1. All dimensions refer to JEDEC standard MO-153-AE.
2. Dimension 'D' does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burr shall not exceed 0.15mm per side.
3. Dimension 'E1' does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the 'b' dimension at maximum material condition.
5. 'A1' is defined as the vertical distance from the seating plane to the lowest point on the package body.

27 Ordering information

Table 52. A31G21x Device Ordering Information

Device name	Flash	SRAM	UART	USART	SPI	I2C	TIMER	PWM	ADC	I/O Ports	Package
A31G213CL	64KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	14	44	LQFP-48
A31G213SQ*	64KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	12	40	MQFP-44
A31G213KN*	64KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	LQFP-32
A31G213KU*	64KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	QFN-32
A31G213GR*	64KB	6KB	2	1	1	2	4(16bit)/2(32bit)	6	6	24	TSSOP-28
A31G212CL*	32KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	14	44	LQFP-48
A31G212SQ*	32KB	6KB	2	2	2	2	4(16bit)/2(32bit)	6	12	40	MQFP-44
A31G212KN*	32KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	LQFP-32
A31G213KU*	32KB	6KB	2	2	1	2	4(16bit)/2(32bit)	6	8	28	QFN-32
A31G212GR*	32KB	6KB	2	1	1	2	4(16bit)/2(32bit)	6	6	24	TSSOP-28

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.

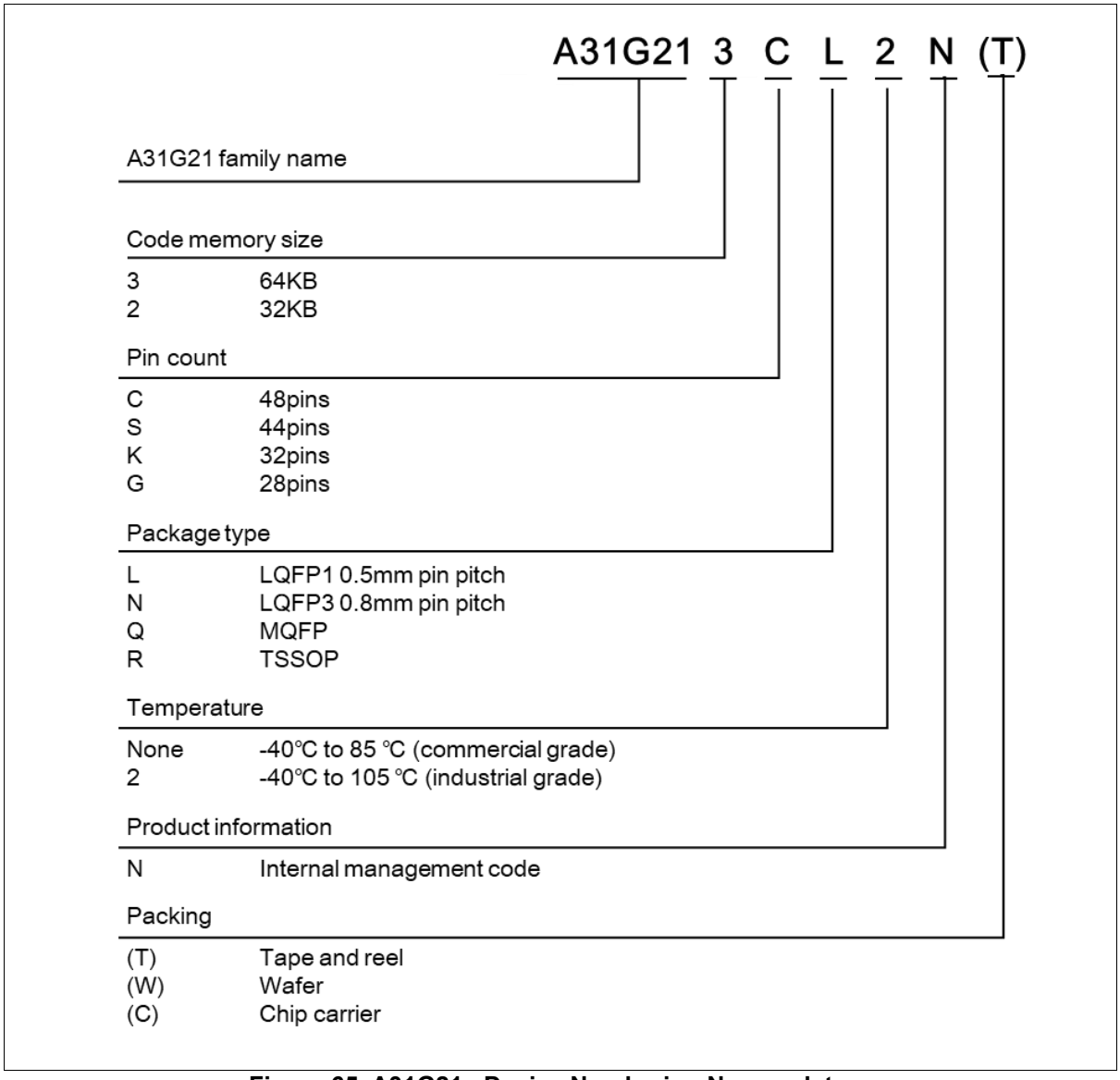


Figure 65. A31G21x Device Numbering Nomenclature

Revision history

Date	Revision	Description
Aug.22, 2019	1.00	1st creation
Dec.30, 2019	1.01	Change to new format
Jul. 10. 2020	1.02	Feature : Maximum operating frequency and Operating Voltage added. Table 1 : ARM Cortex-M0+ Core modified.
Aug.10. 2020	1.03	Figure 66 modified.
Sep.09. 2020	1.04	Figure 67, Figure 68,Table 88. Absolute maximum rating modified.
Feb.02. 2021	1.05	12-bit ADC conversion time, Table 47 and Table 41 modified.
Nov.09. 2022	1.06	Add a package type, “A31G213KU*, A31G212KU (32 QFN)”. Product selection table modified. Add a figure, “Figure 63. 32 QFP Package Outline.” Add a table, “Table 52. A31G21x Device Ordering Information.” Modify a table “Table 52. A31G21x Device Ordering Information.”
Dec.08. 2022	1.07	Revised the font of this document
Jan. 12. 2023	1.08	Change pull-up min/max value in Table 91 DC Electrical Characteristics

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