32-bit Cortex-M0+ based General Purpose Microcontroller

FlashROM 64·128·256 KB / SRAM 16KB

A31G31x

DATA SHEET

Version 1.07

2023.01.27.

Revision History:

Date	By	Version	Description
2018/5/3	Donghyo Shin	1.0.0	Published the standard version of this document
2018/5/29	Donghyo Shin	1.0.1	- A31G314 → A31G31x - Added description for each flash memory options. - Update user manual format - Typo about number of ADC channel In ADC block is modified.
2018/7/19	Donghyo Shin	1.0.2	-Nomenclature is modified
2019/9/24	Hyogeun Song	1.0.3	- Delete USB Function
2020/2/4	Hyogeun Song	1.0.4	- To change VDD33 pin to VDD pin. - To change document disclaimer and distributor
2020/8/5	Hyogeun Song	1.0.5	- Added description for external oscillator load capacitor value. - Correction of typos in relation to LSI characteristics.
2021/11/17	ABOV	1.0.6	- 1.3 Main Features Endurance modified - Table 25.13 Supply Current Characteristics modified
2023/01/27	ABOV	1.07	- 25.1.12 pull-up resistor spec modified - Revised the font of this document

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CHAPTER 1. OVERVIEW

1.1 Overview

A31G31x is designed for the main controller of various appliances.

In particular, accordance with the tendency that the microcontroller is becoming more complicated and high performance in consumer electronics, ARM's high-speed 32-bit Cortex-M0+ Core is used. And for handling more features, this microcontroller has a variety of peripheral devices and large amounts of flash memory. Powerful and various external serial interfaces help to communicate with on-board sensors and devices.

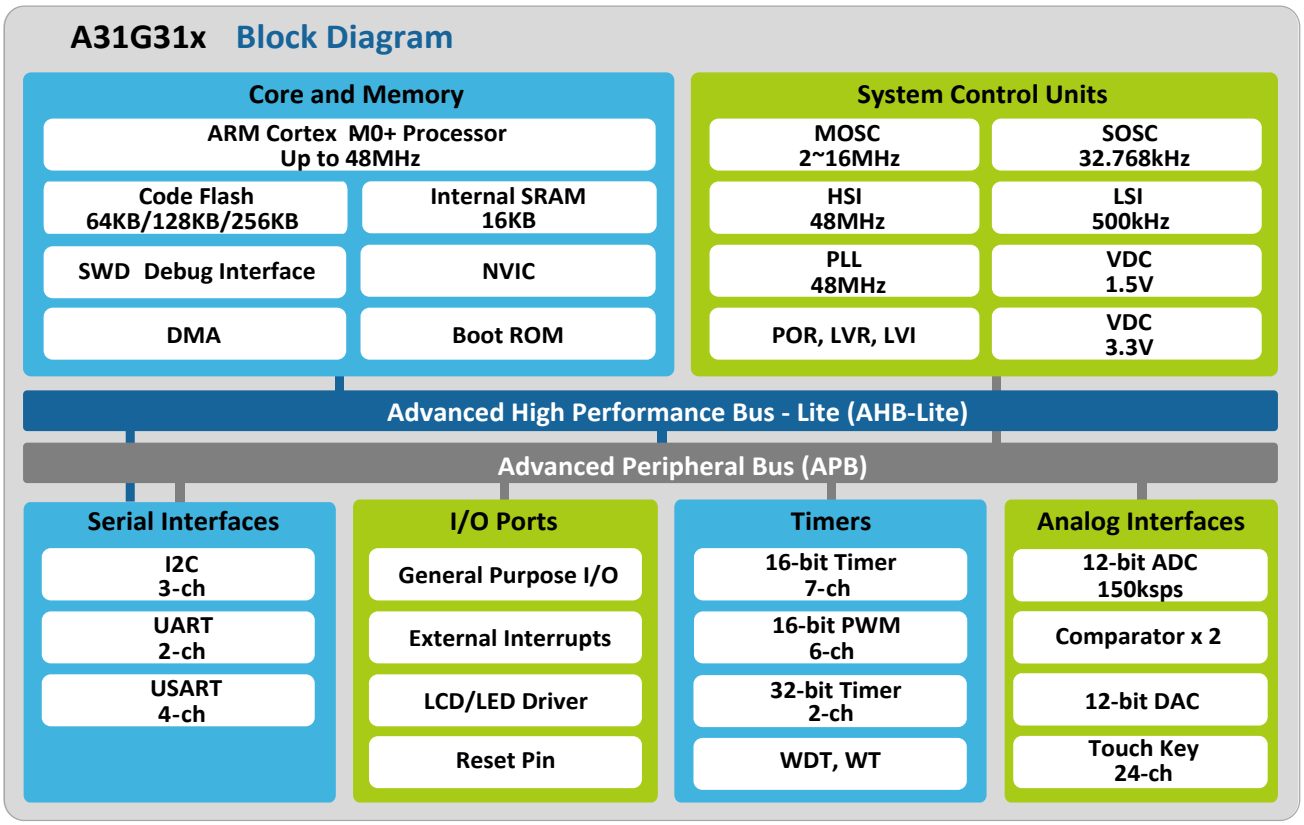


Figure 1.1 Block diagram

1.2 Ordering Information

Table 1.1. Ordering Information

Product Name	CODE Flash [KB]	SRAM [KB]	UART [ch]	USART [ch]	I2C [ch]	TIMER [ch]	PWM [ch]	12-bit ADC [ch]	I/O Ports [ch]	Package
A31G316MMN	256KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP 14
A31G316MLN	256KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP 12
A31G316RMN	256KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP 12
A31G316RLN	256KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP 10
A31G314MMN	128KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP 14
A31G314MLN	128KB	16KB	2	4	3	7(16bit)/ 2(32bit)	6	14	74	80LQFP 12
A31G314RMN	128KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP 12
A31G314RLN	128KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP 10
A31G314CLN	128KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48LQFP
A31G314CUN	128KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48QFN
A31G314SNN	128KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	9	39	44LQFP
A31G313RMN	64KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP 12
A31G313RLN	64KB	16KB	2	3	3	7(16bit)/ 2(32bit)	6	14	58	64LQFP 10
A31G313CLN	64KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48LQFP
A31G313CUN	64KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	11	43	48QFN
A31G313SNN	64KB	16KB	2	2	2	7(16bit)/ 2(32bit)	6	9	39	44LQFP

Device Nomenclature

A31G31 x M L 2 N (T)

A31G31 Family Name

Code Memory Size

6	256Kbytes
4	128Kbytes
3	64Kbytes

Pin Count

M	80 pin
R	64 pin
C	48 pin
S	44 pin

Package type

L	LQFP1	0.5mm pin pitch
M	LQFP2	0.65mm pin pitch
N	LQFP3	0.8mm pin pitch
U	QFN	

Temperature

none	-40°C ~ 85°C
2	-40°C ~ 105°C

Bonding Wire

none	Au wire
N	Pd-Cu wire

Packing

(T)	Tape & Reel
(W)	Wafer
(C)	Chip Carrier

1.3 Main Features

Product features of A31G31x is below

- High Performance Low-power Cortex-M0+ Core
- 64KB/128KB/256KB Code Flash Memory
  - Endurance : 10,000 times
  - Retention : 10 years
- 16KB SRAM
- General Purpose I/O (GPIO)
  - 74 Ports (PA[11:9,7:0], PB[15:0], PC[12:0], PD[5:0], PE[15:0], PF[11:0]) : 80-Pin
  - 58 Ports (PA[11:9,7:0], PB[11:0], PC[12:11,6:0], PD[5:0], PE[11:0], PF[7:0]) : 64-Pin
  - 43 Ports (PA[7:0], PB[7:0], PC[4:0], PD[5:0], PE[11:0], PF[7:0]) : 48-Pin
  - 39 Ports (PA[7:5,2:0], PB[7:0], PC[4:0], PD[4:0], PE[6:0], PF[7:0]) : 44-Pin
- LCD Driver
  - 42 SEG x 8 COM LCD Driver
  - “1/3, 1/4, 1/5, 1/6, 1/8” duty selectable, “1/2, 1/3, 1/4” resistor bias, 16-step contrast control, and automatic bias control
- LED Driver
  - 11 ISEG x 27 ICOM LED Driver
  - ICOM 26.4mA, ISEG 2.4mA @3.3V
- Timer
  - 16 Bit 7-ch, Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
  - 32 Bit 2-ch, Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
- PWM
  - 16 Bit 6-ch, Periodic timer mode, Back-to-Back mode, Capture mode
- Watchdog Timer
  - 24 Bit 1-ch, WDTRC 31.250kHz
- Watch Timer
  - 14 Bit divider with extended 12 Bit counter 1-ch
- External communication ports:
  - 2-ch UART, 4-ch USART, 3-ch I^2C : 80-Pin
  - 2-ch UART, 3-ch USART, 3-ch I^2C : 64-Pin
  - 2-ch UART, 2-ch USART, 2-ch I^2C : 48-Pin, 44-Pin
- Direct Memory Access Controller
  - 4-ch
- 150kSPS 12-bit ADC
  - 14-ch : 80-Pin, 64-Pin
  - 11-ch : 48-Pin
  - 9-ch : 44-Pin
- Comparator
  - 1 reference 1 input comparator 1-ch
  - 1 reference 3 input comparator 1-ch
- 12-bit DAC
- Capactive Touch Switch
  - 24-ch : 80-Pin
  - 20-ch : 64-Pin
  - 13-ch : 48-Pin
  - 11-ch : 44-Pin
- On-Chip RC-Oscillator

- HSI : 48MHz(±3.5% @-40 ~ +85℃)
- LSI : 500kHz(±20% @-40 ~ +85℃)

◆ External main crystal oscillator
- 2MHz ~16MHz

◆ System Fail-Safe function by Clock Monitoring
◆ XTAL OSC Fail monitoring
◆ CRC
- CRC-CCITT, CRC-16

◆ Power On Reset
◆ Programmable Low Voltage Reset, Low Voltage Indicator
◆ Debug and Emergency stop function
◆ SWD Debugger
◆ Power Down Mode
- IDLE, STOP Mode

◆ Sub-Active mode
- System used external 32.768kHz crystal or system used internal 500kHz LSI

◆ Operating Frequency
- 500kHz ~ 48MHz
- External 32.768kHz crystal
- PLL 48MHz

◆ Operating Voltage
- 1.8V ~ 5.5V

◆ Operating Temperature
- -40 ~ +85℃

◆ package options
- A31G316(FLASH 256KB) : 80LQFP14/80LQFP12/64LQFP12/64LQFP10
- A31G314(FLASH 128KB) : 80LQFP14/80LQFP12/64LQFP12/64LQFP10/ 48LQFP / 48QNF / 44LQFP
- A31G313(FLASH 64KB) : 64LQFP12/64LQFP10/48LQFP/48QFN/44LQFP

1.3.1 Functional Description

The following section provides an overview of the features of A31G31x microcontroller.

ARM Cortex-M0+

ARM powered Cortex-M0+ Core based on ARMv6M architecture which is optimized for small size and low power system.

On core system timer (SYSTICK) provides a simple 24-bit timer easy to manage the system operation

Thumb-compatible Thumb-2 only instruction set processor core makes code high-density.

Hardware division and single-cycle multiplication is present

Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.

SWD debugging features are provided.

Max 48MHz operating frequency with one wait execution

Nested Vector-Interrupt Controller (NVIC)

The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M0+ core is included which handles all the internal and external exceptions. When interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of interrupt service routine.

The vector is fetched in parallel to the state saving, which enables efficient interrupt entry.

The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoring.

128KB Internal Code Flash Memory

The A31G31x provides internal 128KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. The CPU can access flash memory with one wait state up to 48 MHz bus frequency.

16KB 0-wait Internal SRAM

On chip 16KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

DMA Controller

The DMA controller performs direct memory transfer by sharing the system bus with CPU core.

Boot Logic

The smart boot logic supports the flash programming. The A31G31x can be entered by external boot pin and UART and SPI programming are available in boot mode. USART10 is used in boot mode communication.

System Control Unit (SCU)

The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (Oscillator Block, VDC, LVR and LVI)

32-bit Watchdog Timer (WDT)

The watchdog timer performs system monitoring function. It will generate internal reset or interrupt to notice abnormal status of the system.

Multi-purpose 16/32-bit Timer

Seven-channel 16-bit and Two-channel 32-bit general purpose timers supports below functions.

- Periodic timer mode
- PWM mode
- Counter mode
- Capture mode

16-bit Timer with 6 Channel PWMs

The 16-bit timer has 6 channel PWMs for 3-phase motor application. 16-bit up/down counter with prescaler supports both of triangular and saw tooth waveform.

The PWM has ability to generate internal ADC trigger signal to measure the signal on time.

Dead time insertion and emergency stop functionality help that the chip and system are under safety conditions.

Universal Asynchronous Receiver/Transmitter (UART)

The A31G31x has 2 channels UART block. For accurate baud rate control, the fractional baud rate generator is provided.

Universal Asynchronous Receiver/Transmitter and Serial Peripheral Interface (USART: UART and SPI)

The USART supports UART and SPI mode. The A31G31x series has 4 channel USART modules.

Boot mode will use this USART block to download flash program.

Inter-Integrated Circuit Interface (I^2C)

The A31G31x has 3 channel I^2C block and it supports up to 400 kHz I^2C communication. The master and the slave mode are supported.

General PORT I/Os

11-bit PA, 16-bit PB, 13-bit PC, 6-bit PD, 16-bit PE and 12-bit PF ports are available and provide multiple functionality.

- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Programmable pull-up and open-drain selection
- On-chip input debounce filter

LCD Driver

LED Driver

12-bit Analog-to-Digital Converter (ADC)

One built-in ADC can convert analog signal up to 150kSPS(sample per second) conversion rate. 14-channel analog MUX provides various combinations from external analog signals.

12-bit Digital-to-Analog Converter (DAC)

Touch

16-bit Cyclic Redundancy Check (CRC) Generator

The A31G31x series has two polynominals for CRC generator. They are CRC-CCITT and CRC-16.

1.4 Block Diagram

A31G31x is shown as below consists of a variety of peripheral devices.

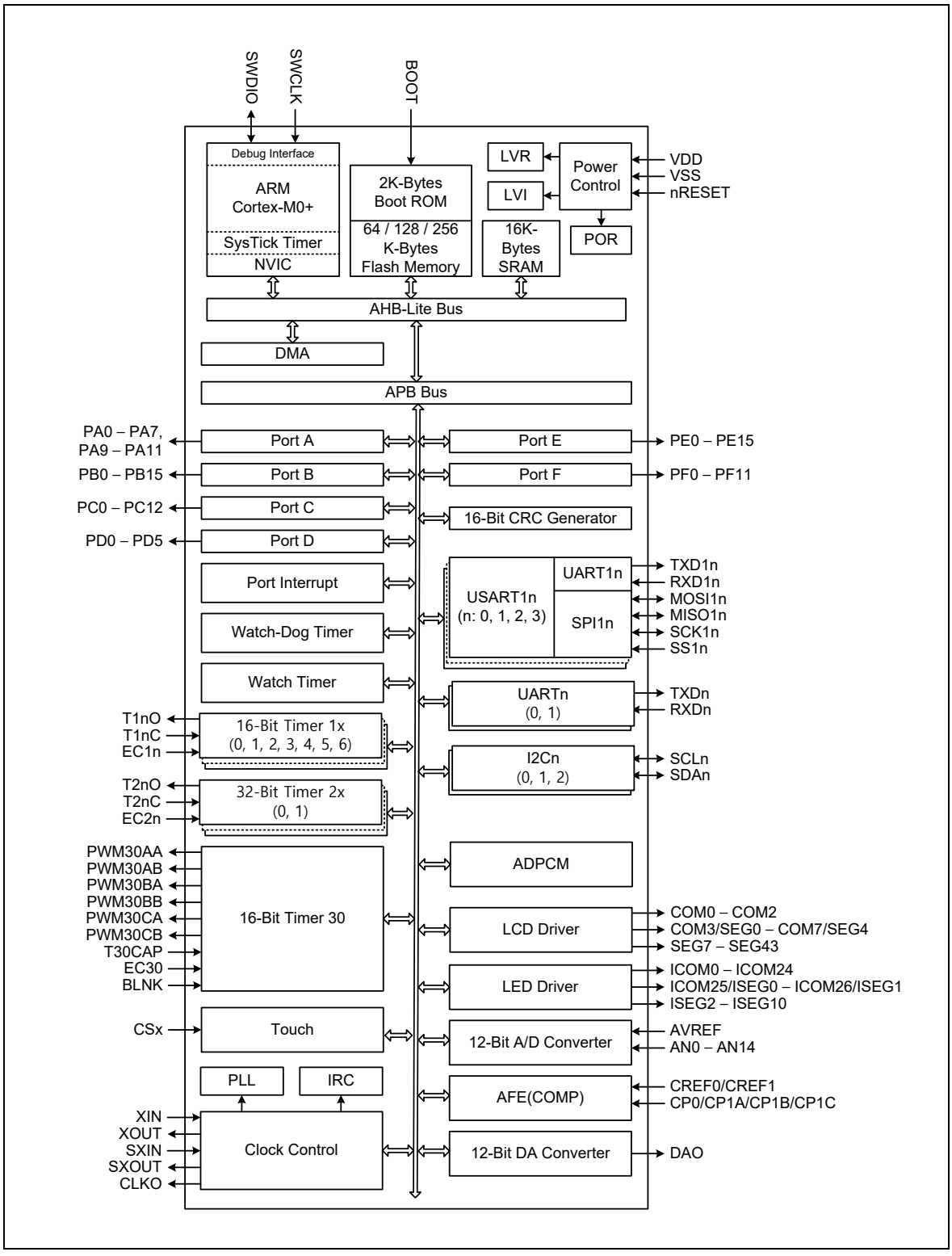


Figure 1.2 Internal block diagram of A31G31x MCUs

1.5 Pin Layout of Packages

1.5.1 A31G31xMMN (80LQFP14)

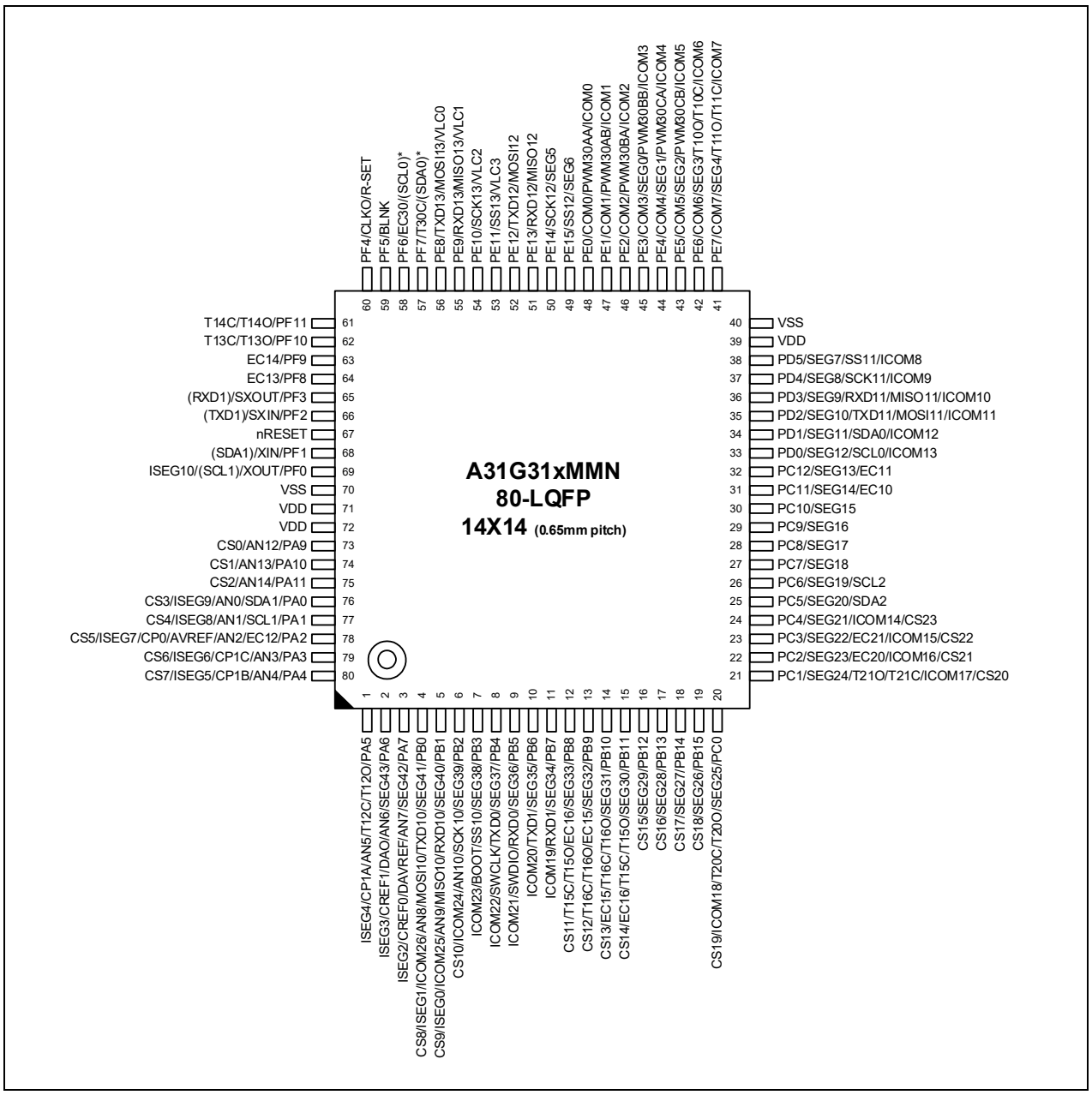


Figure 1.3 PIN LAYOUT (80LQFP14)

1.5.2 A31G31xMLN (80LQFP12)

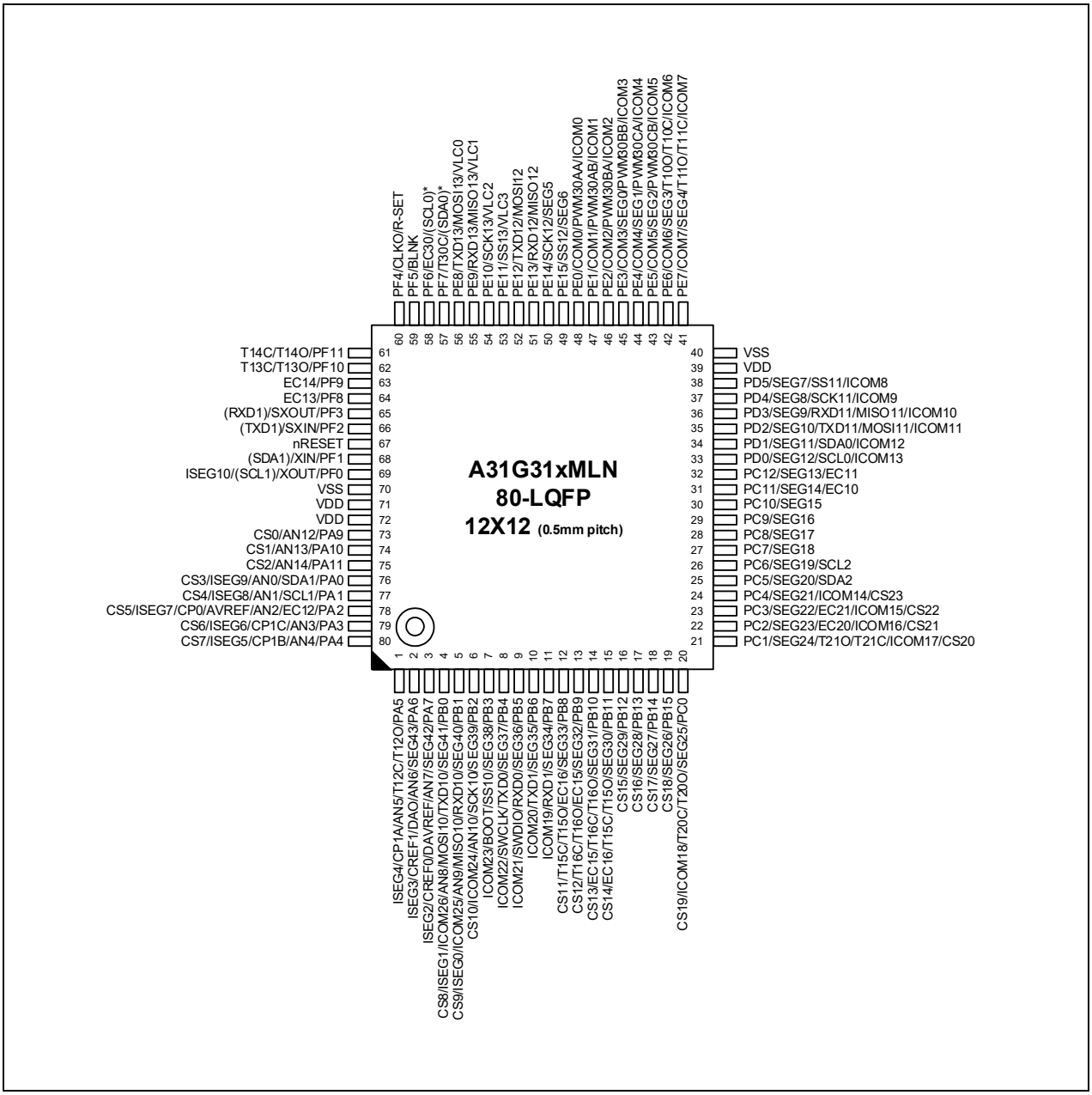


Figure 1.4 PIN LAYOUT (80LQFP12)

1.5.3 A31G31xRMN (64LQFP12)

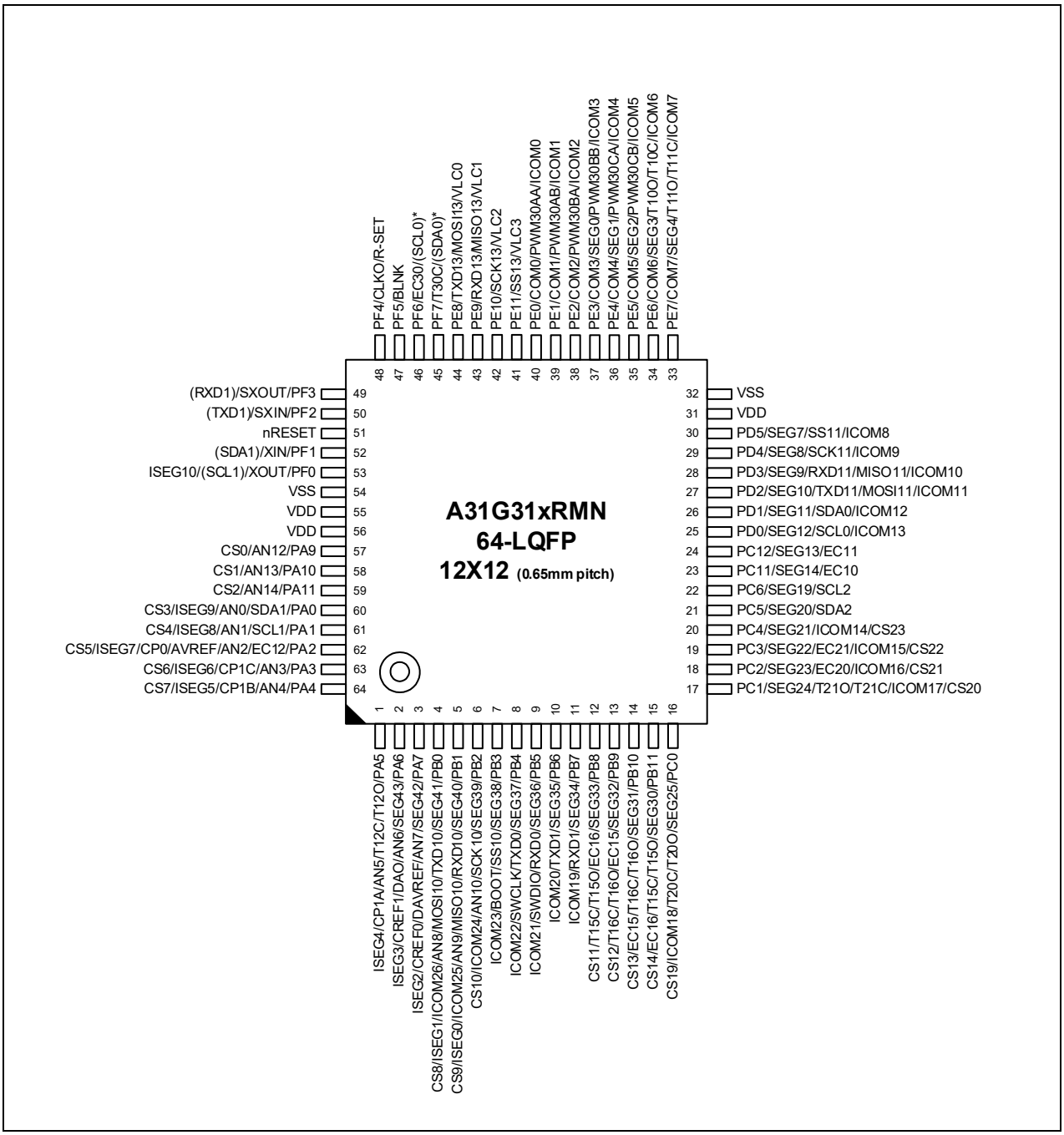


Figure 1.5 PIN LAYOUT (64LQFP12)

1.5.4 A31G31xRLN (64LQFP10)

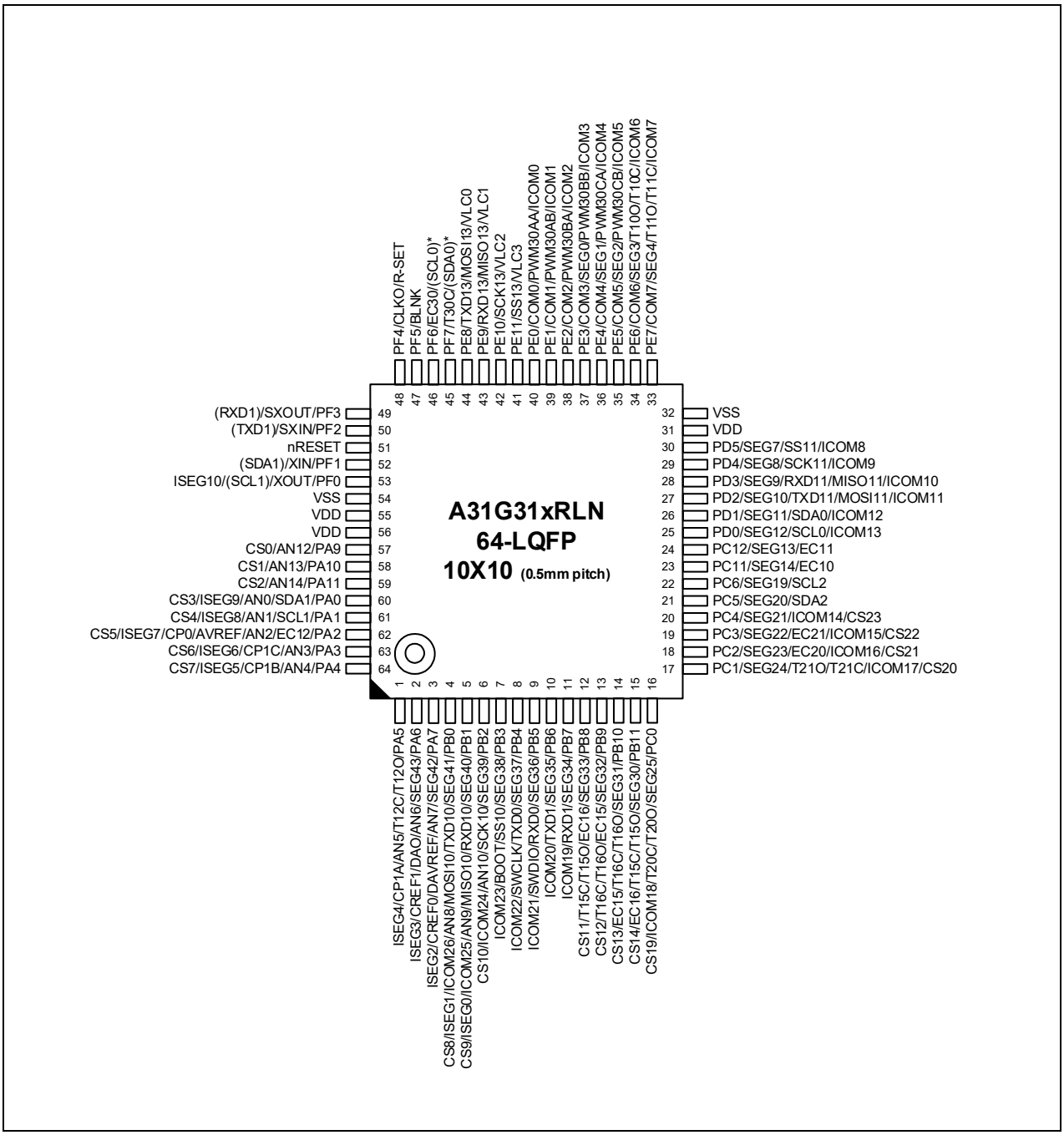


Figure 1.6 PIN LAYOUT (64LQFP10)

1.5.5 A31G31xCLN (48LQFP)

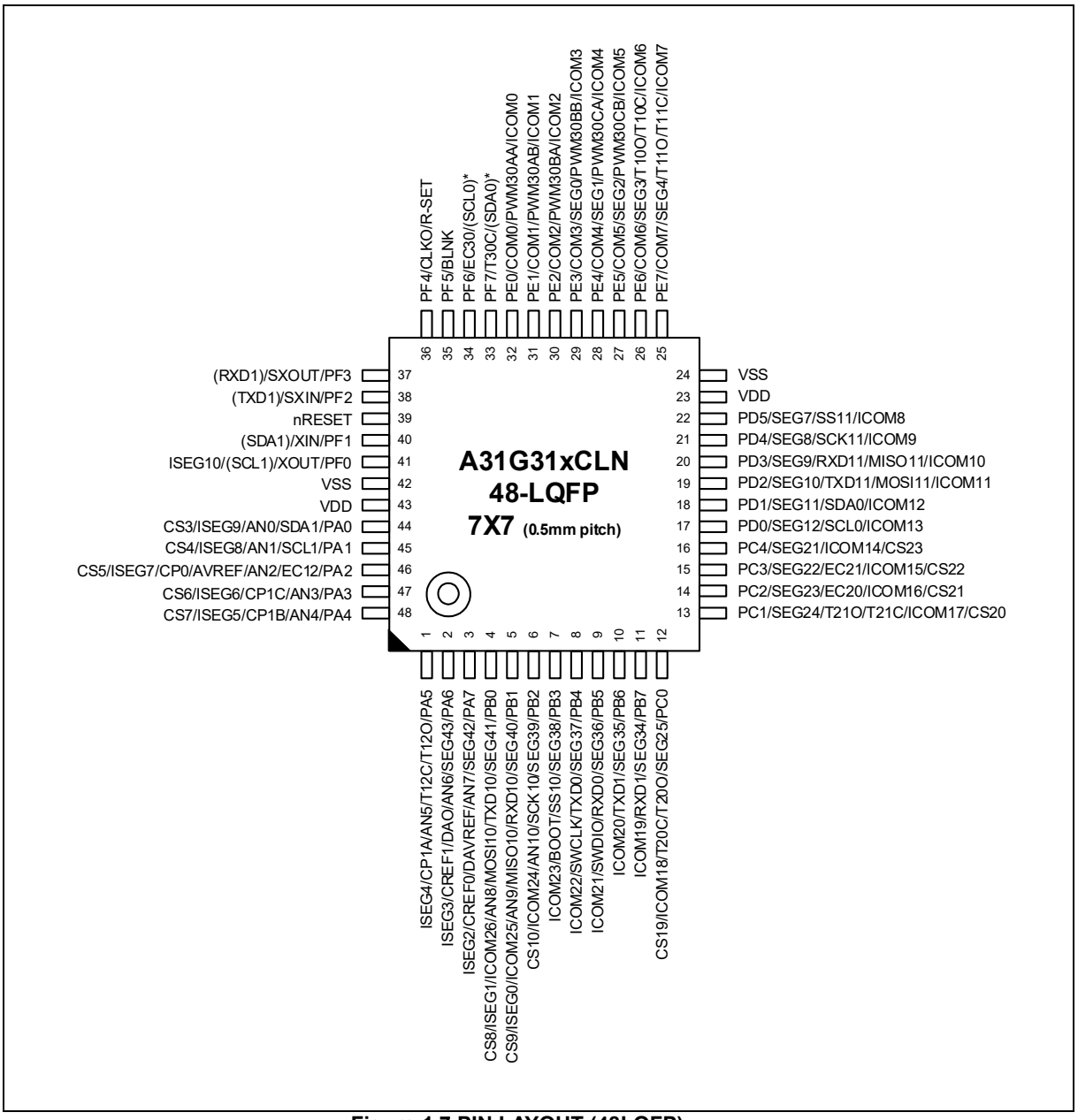


Figure 1.7 PIN LAYOUT (48LQFP)

1.5.6 A31G31xCUN (48QFN)

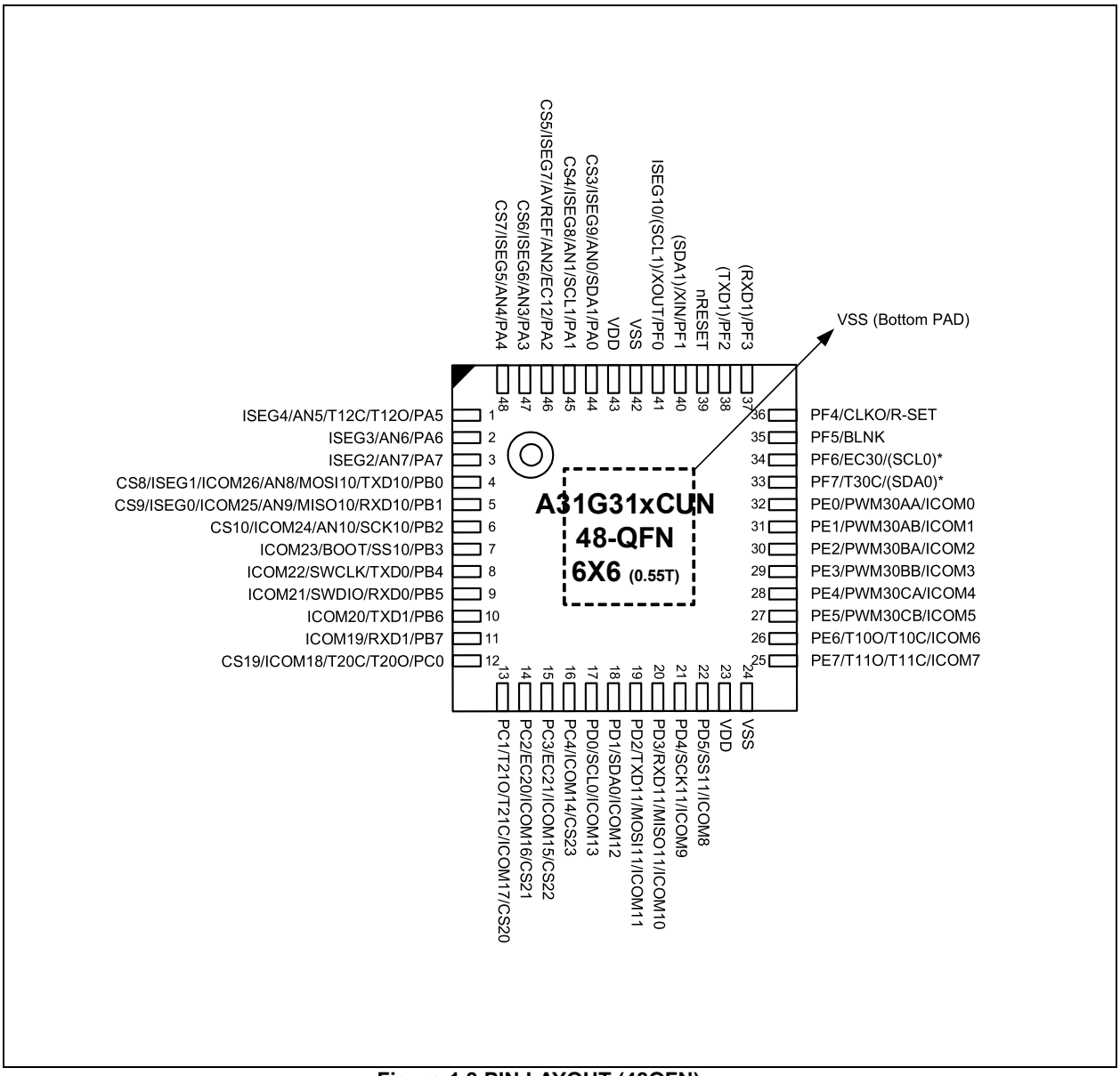


Figure 1.8 PIN LAYOUT (48QFN)

1.5.7 A31G31xSNN (44LQFP)

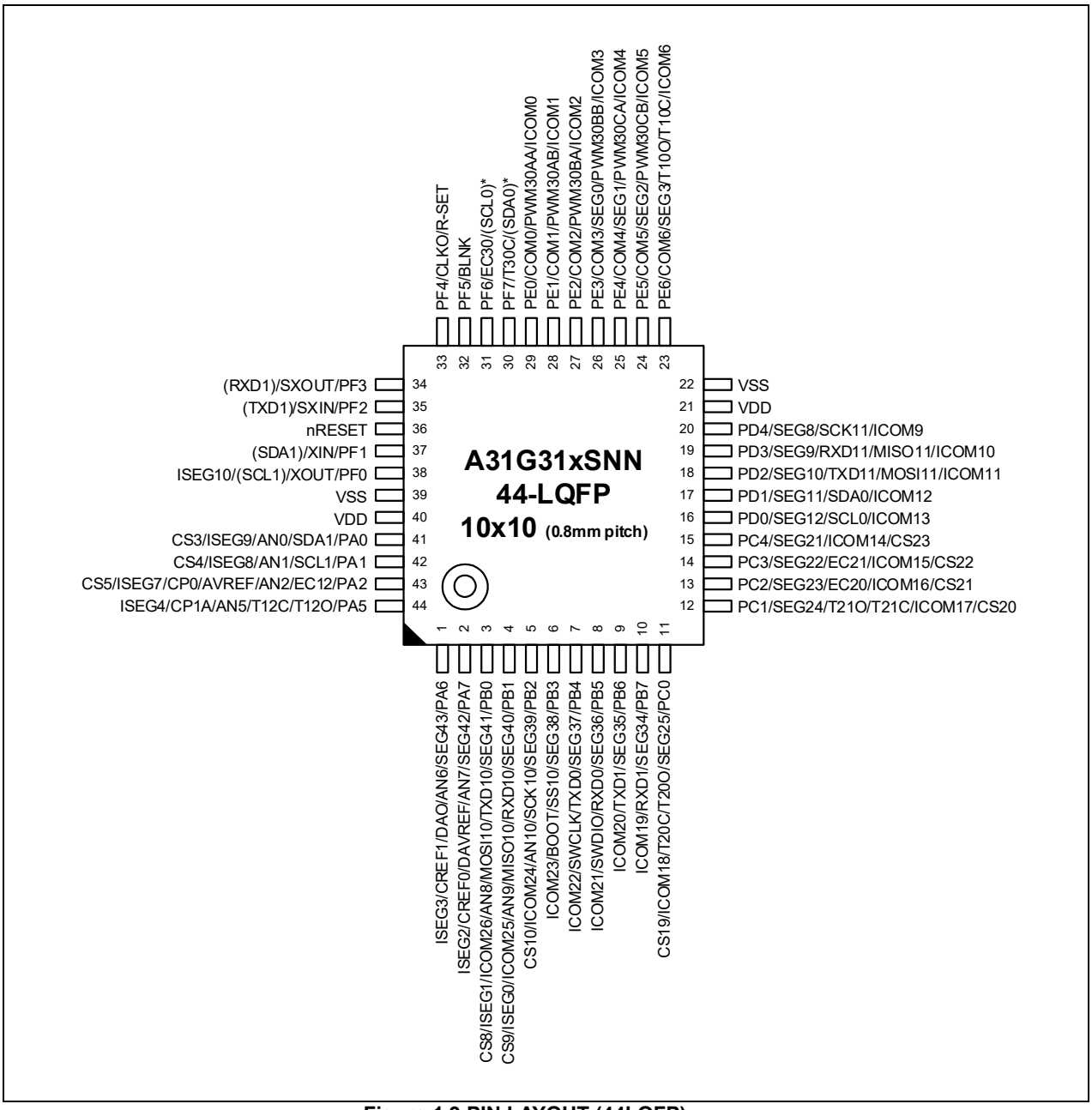


Figure 1.9 PIN LAYOUT (44LQFP)

1.6 Pin Configuration

Depending on the package type of each A31G31x microcontroller, there are some differences in the number of pins and configurations.
The pin configuration of A31G31x MCUs is as follows.

Table 1.2 Pin Configuration

Pin No				Pin Name	Type	Description	Remark
80LQFP14 80LQFP12	64LQFP12 64LQFP10	48LQFP 48QFN	44LQFP				
1	1	1	44	PA5*	IOUDS	PORT A Bit 5 Input/Output	
				T12O	O	Timer 12 Output	
				T12C	I	Timer 12 Capture Input	
				AN5	IA	Analog Input 5	
				CP1A	IA	Comparator input 1A	
				ISEG4	O	LED Segment Signal 4 Output	
2	2	2	1	PA6*	IOUDS	PORT A Bit 6 Input/Output	
				SEG43	O	LCD Segment Signal 43 Output	
				AN6	IA	Analog Input 6	
				DAO	OA	Digital to analog output	
				CREF1	IA	Comparator 1 Reference Input	
				ISEG3	O	LED Segment Signal 3 Output	
3	3	3	2	PA7*	IOUDS	PORT A Bit 7 Input/Output	
				SEG42	O	LCD Segment Signal 42 Output	
				AN7	IA	Analog Input 7	
				DAVREF	IA	D/A converter reference input	
				CREF0	IA	Comparator 0 Reference Input	
				ISEG2	O	LED Segment Signal 2 Output	
4	4	4	3	PB0	IOUDS	PORT B Bit 0 Input/Output	
				SEG41	O	LCD Segment Signal 41 Output	
				TXD10*	O	UART Channel 10 TxD Input	
				MOSI10	I/O	SPI Channel 10 Master Out / Slave In	
				AN8	IA	Analog Input 8	
				ICOM26	O	LED Common Signal 26 Output	
				ISEG1	O	LED Segment Signal 1 Output	
				CS8	IA	Capacitive Touch switch input 8	
5	5	5	4	PB1	IOUDS	PORT B Bit 1 Input/Output	
				SEG40	O	LCD Segment Signal 40 Output	
				RXD10*	I	UART Channel 10 RxD Input	
				MISO10	I/O	SPI10 Master-Input/Slave-Output Data signal	
				AN9	IA	Analog Input 9	
				ICOM25	O	LED Common Signal 25 Output	

				ISEG0	O	LED Segment Signal 0 Output	
				CS9	IA	Capacitive Touch switch input 9	
6	6	6	5	PB2*	IOUDS	PORT B Bit 2 Input/Output	
				SEG39	O	LCD Segment Signal 39 Output	
				SCK10	I/O	SPI10 Data Clock Input/Output	
				AN10	IA	Analog Input 10	
				ICOM24	O	LED Common Signal 24 Output	
				CS10	IA	Capacitive Touch switch input 10	
7	7	7	6	PB3	IOUDS	PORT B Bit 3 Input/Output	
				SEG38	O	LCD Segment Signal 38 Output	
				SS10	I/O	SPI Channel 10 Slave Select signa	
				BOOT*	I	Boot mode Selection Input	Pull-up
				ICOM23	O	LED Common Signal 23 Output	
8	8	8	7	PB4	IOUDS	PORT B Bit 4 Input/Output	
				SEG37	O	LCD Segment Signal 37 Output	
				TXD0	O	UART Channel 0 TxD Input	
				SWCLK*	I	SWD Clock Input	Pull-up
				ICOM22	O	LED Common Signal 22 Output	
9	9	9	8	PB5	IOUDS	PORT B Bit 5 Input/Output	
				SEG36	O	LCD Segment Signal 36 Output	
				RXD0	I	UART Channel 0 RxD Input	
				SWDIO*	I/O	SWD Data Input/Output	Pull-up
				ICOM21	O	LED Common Signal 21 Output	
10	10	10	9	PB6*	IOUDS	PORT B Bit 6 Input/Output	
				SEG35	O	LCD Segment Signal 35 Output	
				TXD1	O	UART Channel 1 TxD Input	
				ICOM20	O	LED Common Signal 20 Output	
11	11	11	10	PB7*	IOUDS	PORT B Bit 7 Input/Output	
				SEG34	O	LCD Segment Signal 34 Output	
				RXD1	I	UART Channel 1 RxD Input	
				ICOM19	O	LED Common Signal 19 Output	
12	12	-	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
				SEG33	O	LCD Segment Signal 33 Output	
				EC16	I	Timer 16 Event Count Input	
				T15O	O	Timer 15 Output	
				T15C	I	Timer 15 Capture Input	
				CS11	IA	Capacitive Touch switch input 11	
13	13	-	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	

				SEG32	O	LCD Segment Signal 32 Output	
				EC15	I	Timer 15 Event Count Input	
				T16O	O	Timer 16 Output	
				T16C	I	Timer 16 Capture Input	
				CS12	IA	Capacitive Touch switch input 12	
14	14	-	-	PB10*	IOUDS	PORT B Bit 10 Input/Output	
				SEG31	O	LCD Segment Signal 31 Output	
				T16O	O	Timer 16 Output	
				T16C	I	Timer 16 Capture Input	
				EC15	I	Timer 15 Event Count Input	
				CS13	IA	Capacitive Touch switch input 13	
15	15	-	-	PB11*	IOUDS	PORT B Bit 11 Input/Output	
				SEG30	O	LCD Segment Signal 30 Output	
				T15O	O	Timer 15 Output	
				T15C	I	Timer 15 Capture Input	
				EC16	I	Timer 16 Event Count Input	
				CS14	IA	Capacitive Touch switch input 14	
16	-	-	-	PB12*	IOUDS	PORT B Bit 12 Input/Output	
				SEG29	O	LCD Segment Signal 29 Output	
				CS15	IA	Capacitive Touch switch input 15	
17	-	-	-	PB13*	IOUDS	PORT B Bit 13 Input/Output	
				SEG28	O	LCD Segment Signal 28 Output	
				CS16	IA	Capacitive Touch switch input 16	
18	-	-	-	PB14*	IOUDS	PORT B Bit 14 Input/Output	
				SEG27	O	LCD Segment Signal 27 Output	
				CS17	IA	Capacitive Touch switch input 17	
19	-	-	-	PB15*	IOUDS	PORT B Bit 15 Input/Output	
				SEG26	O	LCD Segment Signal 26 Output	
				CS18	IA	Capacitive Touch switch input 18	
20	16	12	11	PC0*	IOUDS	PORT C Bit 0 Input/Output	
				SEG25	O	LCD Segment Signal 25 Output	
				T20O	O	Timer 20 Output	
				T20C	I	Timer 20 Capture Input	
				ICOM18	O	LED Common Signal 18 Output	
				CS19	IA	Capacitive Touch switch input 19	
21	17	13	12	PC1*	IOUDS	PORT C Bit 1 Input/Output	
				SEG24	O	LCD Segment Signal 24 Output	
				T21O	O	Timer 21 Output	
				T21C	I	Timer 21 Capture Input	
				ICOM17	O	LED Common Signal 17 Output	
				CS20	IA	Capacitive Touch switch input 20	
22	18	14	13	PC2*	IOUDS	PORT C Bit 2 Input/Output	

				SEG23	O	LCD Segment Signal 23 Output	
				EC20	I	Timer 20 Event Count Input	
				ICOM16	O	LED Common Signal 16 Output	
				CS21	IA	Capacitive Touch switch input 21	
23	19	15	14	PC3*	IOUDS	PORT C Bit 3 Input/Output	
				SEG22	O	LCD Segment Signal 22 Output	
				EC21	I	Timer 21 Event Count Input	
				ICOM15	O	LED Common Signal 15 Output	
				CS22	IA	Capacitive Touch switch input 22	
24	20	16	15	PC4*	IOUDS	PORT C Bit 4 Input/Output	
				SEG21	O	LCD Segment Signal 21 Output	
				ICOM14	O	LED Common Signal 14 Output	
				CS23	IA	Capacitive Touch switch input 23	
25	21	-	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
				SEG20	O	LCD Segment Signal 20 Output	
				SDA2	O	I²C Channel 2 SDA In/Out	
26	22	-	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
				SEG19	O	LCD Segment Signal 19 Output	
				SCL2	O	I²C Channel 2 SCL In/Out	
27	-	-	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
				SEG18	O	LCD Segment Signal 18 Output	
28	-	-	-	PC8*	IOUDS	PORT C Bit 8 Input/Output	
				SEG17	O	LCD Segment Signal 17 Output	
29	-	-	-	PC9*	IOUDS	PORT C Bit 9 Input/Output	
				SEG16	O	LCD Segment Signal 16 Output	
30	-	-	-	PC10*	IOUDS	PORT C Bit 10 Input/Output	
				SEG15	O	LCD Segment Signal 15 Output	
31	23	-	-	PC11*	IOUDS	PORT C Bit 11 Input/Output	
				SEG14	O	LCD Segment Signal 14 Output	
				EC10	I	Timer 10 Event Count Input	
32	24	-	-	PC12*	IOUDS	PORT C Bit 12 Input/Output	
				SEG13	O	LCD Segment Signal 13 Output	
				EC11	I	Timer 11 Event Count Input	
33	25	17	16	PD0*	IOUDS	PORT D Bit 0 Input/Output	
				SEG12	O	LCD Segment Signal 12 Output	
				SCL0	O	I²C Channel 0 SCL In/Out	
				ICOM13	O	LED Common Signal 13 Output	
34	26	18	17	PD1*	IOUDS	PORT D Bit 1 Input/Output	
				SEG11	O	LCD Segment Signal 11 Output	

				SDA0	O	I²C Channel 0 SDA In/Out	
				ICOM12	O	LED Common Signal 12 Output	
35	27	19	18	PD2*	IOUDS	PORT D Bit 2 Input/Output	
				SEG10	O	LCD Segment Signal 10 Output	
				TXD11	O	UART Channel 11 TxD Input	
				MOSI11	I/O	SPI Channel 11 Master Out / Slave In	
				ICOM11	O	LED Common Signal 11 Output	
36	28	20	19	PD3*	IOUDS	PORT D Bit 3 Input/Output	
				SEG9	O	LCD Segment Signal 9 Output	
				RXD11	I	UART Channel 11 RxD Input	
				MISO11	I/O	SPI11 Master-Input/Slave-Output Data signal	
				ICOM10	O	LED Common Signal 10 Output	
37	29	21	20	PD4*	IOUDS	PORT D Bit 4 Input/Output	
				SEG8	O	LCD Segment Signal 8 Output	
				SCK11	I/O	SPI11 Data Clock Input/Output	
				ICOM9	O	LED Common Signal 9 Output	
38	30	22	-	PD5*	IOUDS	PORT D Bit 5 Input/Output	
				SEG7	O	LCD Segment Signal 7 Output	
				SS11	I/O	SPI Channel 11 Slave Select signa	
				ICOM8	O	LED Common Signal 8 Output	
39	31	23	21	VDD	P	VDD	
40	32	24	22	VSS	P	VSS	
41	33	25	-	PE7*	IOUDS	PORT E Bit 7 Input/Output	
				COM7	O	LCD Common Signal 7 Outputs	
				SEG4	O	LCD Segment Signal 4 Output	
				T11O	O	Timer 11 Output	
				T11C	I	Timer 11 Capture Input	
				ICOM7	O	LED Common Signal 7 Output	
42	34	26	23	PE6*	IOUDS	PORT E Bit 6 Input/Output	
				COM6	O	LCD Common Signal 6 Output	
				SEG3	O	LCD Segment Signal 3 Output	
				T10O	O	Timer 10 Output	
				T10C	I	Timer 10 Capture Input	
				ICOM6	O	LED Common Signal 6 Output	
43	35	27	24	PE5*	IOUDS	PORT E Bit 5 Input/Output	
				COM5	O	LCD Common Signal 5 Output	
				SEG2	O	LCD Segment Signal 2 Output	
				PWM30CB	O	Timer 30 PWM Output	
				ICOM5	O	LED Common Signal 5 Output	
44	36	28	25	PE4*	IOUDS	PORT E Bit 4 Input/Output	
				COM4	O	LCD Common Signal 4 Output	

				SEG1	O	LCD Segment Signal 1 Output	
				PWM30CA	O	Timer 30 PWM Output	
				ICOM4	O	LED Common Signal 4 Output	
45	37	29	26	PE3*	IOUDS	PORT E Bit 3 Input/Output	
				COM3	O	LCD Common Signal 3 Output	
				SEG0	O	LCD Segment Signal 0 Output	
				PWM30BB	O	Timer 30 PWM Output	
				ICOM3	O	LED Common Signal 3 Output	
46	38	30	27	PE2*	IOUDS	PORT E Bit 2 Input/Output	
				COM2	O	LCD Common Signal 2 Output	
				PWM30BA	O	Timer 30 PWM Output	
				ICOM2	O	LED Common Signal 2 Output	
47	39	31	28	PE1*	IOUDS	PORT E Bit 1 Input/Output	
				COM1	O	LCD Common Signal 1 Output	
				PWM30AB	O	Timer 30 PWM Output	
				ICOM1	O	LED Common Signal 1 Output	
48	40	32	29	PE0*	IOUDS	PORT E Bit 0 Input/Output	
				COM0	O	LCD Common Signal 0 Output	
				PWM30AA	O	Timer 30 PWM Output	
				ICOM0	O	LED Common Signal 0 Output	
49	-	-	-	PE15*	IOUDS	PORT E Bit 15 Input/Output	
				SS12	I/O	SPI Channel 12 Slave Select signal	
				SEG6	O	LCD Segment Signal 6 Output	
50	-	-	-	PE14*	IOUDS	PORT E Bit 14 Input/Output	
				SCK12	I/O	SPI12 Data Clock Input/Output	
				SEG5	O	LCD Segment Signal 5 Output	
51	-	-	-	PE13*	IOUDS	PORT E Bit 13 Input/Output	
				RXD12	I	UART Channel 12 RxD Input	
				MISO12	I/O	SPI12 Master-Input/Slave-Output Data signal	
52	-	-	-	PE12*	IOUDS	PORT E Bit 12 Input/Output	
				TXD12	O	UART Channel 12 TxD Input	
				MOSI12	I/O	SPI Channel 12 Master Out / Slave In	
53	41	-	-	PE11*	IOUDS	PORT E Bit 11 Input/Output	
				SS13	I/O	SPI Channel 13 Slave Select signal	
				VLC3	IA	External LCD Voltage bias 3	
54	42	-	-	PE10*	IOUDS	PORT E Bit 10 Input/Output	
				SCK13	I/O	SPI13 Data Clock Input/Output	

				VLC2	IA	External LCD Voltage bias 2	
55	43	-	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
				RXD13	I	UART Channel 13 RxD Input	
				MISO13	I/O	SPI13 Master-Input/Slave-Output Data signal	
				VLC1	IA	External LCD Voltage bias 1	
56	44	-	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
				TXD13	O	UART Channel 13 TxD Input	
				MOSI13	I/O	SPI Channel 13 Master Out / Slave In	
				VLC0	IA	External LCD Voltage bias 0	
57	45	33	30	PF7*	IODS	PORT F Bit 7 Input/Output	Open-drain
				T30C	I	Timer 30 Capture Input	
				(SDA0)	O	I²C Channel 0 SDA In/Out	
58	46	34	31	PF6*	IODS	PORT F Bit 6 Input/Output	Open-drain
				EC30	I	Timer 30 Event Count Input	
				(SCL0)	O	I²C Channel 0 SCL In/Out	
59	47	35	32	PF5*	IODS	PORT F Bit 5 Input/Output	Open-drain
				BLINK	I	External Sync Signal Input for T30 PWM	
60	48	36	33	PF4*	IOUDS	PORT F Bit 4 Input/Output	
				CLKO	O	System Clock Output	
				R-SET	IA	LED Segment current setting	
61	-	-	-	PF11*	IOUDS	PORT F Bit 11 Input/Output	
				T14O	O	Timer 14 Output	
				T14C	I	Timer 14 Capture Input	
62	-	-	-	PF10*	IOUDS	PORT F Bit 10 Input/Output	
				T13O	O	Timer 13 Output	
				T13C	I	Timer 13 Capture Input	
63	-	-	-	PF9*	IOUDS	PORT F Bit 9 Input/Output	
				EC14	I	Timer 14 Event Count Input	
64	-	-	-	PF8*	IOUDS	PORT F Bit 8 Input/Output	
				EC13	I	Timer 13 Event Count Input	
65	49	37	34	PF3*	IOUDS	PORT F Bit 3 Input/Output	
				SXOUT	O	Sub Oscillator Output	
				(RXD1)	I	UART Channel 1 RxD Input	
66	50	38	35	PF2*	IOUDS	PORT F Bit 2 Input/Output	
				SXIN	I	Sub Oscillator Input	
				(TXD1)	O	UART Channel 1 TxD Input	
67	51	39	36	nRESET	IU	External Reset Input	Pull-up
68	52	40	37	PF1*	IOUDS	PORT F Bit 1 Input/Output	
				XIN	I	Main Oscillator Input	
				(SDA1)	O	I²C Channel 2 SDA In/Out	
69	53	41	38	PF0*	IOUD	PORT F Bit 0 Input/Output	

					S		
				XOUT	O	Main Oscillator Output	
				(SCL1)	O	I²C Channel 2 SCL In/Out	
				ISEG10	O	LED Segment Signal 26 Output	
70	54	42	39	VSS	P	VSS	
71	55	43	40	VDD	P	VDD	
72	56	-	-	VDD	P	VDD	
73	57	-	-	PA9*	IOUDS	PORT A Bit 9 Input/Output	
				AN12	IA	Analog Input 12	
				CS0	IA	Capacitive Touch switch input 0	
74	58	-	-	PA10*	IOUDS	PORT A Bit 10 Input/Output	
				AN13	IA	Analog Input 13	
				CS1	IA	Capacitive Touch switch input 1	
75	59	-	-	PA11*	IOUDS	PORT A Bit 11 Input/Output	
				AN14	IA	Analog Input 14	
				CS2	IA	Capacitive Touch switch input 2	
76	60	44	41	PA0*	IOUDS	PORT A Bit 0 Input/Output	
				SDA1	O	I²C Channel 1 SDA In/Out	
				AN0	IA	Analog Input 0	
				ISEG9	O	LED Segment Signal 9 Output	
				CS3	IA	Capacitive Touch switch input 3	
				-	-	-	
77	61	45	42	PA1*	IOUDS	PORT A Bit 1 Input/Output	
				SCL1	O	I²C Channel 1 SCL In/Out	
				AN1	IA	Analog Input 1	
				ISEG8	O	LED Segment Signal 8 Output	
				CS4	IA	Capacitive Touch switch input 4	
				-	-	-	
78	62	46	43	PA2*	IOUDS	PORT A Bit 2 Input/Output	
				EC12	I	Timer 12 Event Count Input	
				AN2	IA	Analog Input 2	
				AVREF	IA	A/D Converter Reference Input	
				CP0	IA	Comparator plus input 0	
				ISEG7	O	LED Segment Signal 7 Output	
				CS5	IA	Capacitive Touch switch input 5	
79	63	47	-	PA3*	IOUDS	PORT A Bit 3 Input/Output	
				AN3	IA	Analog Input 3	
				CP1C	IA	Comparator plus input 1C	
				ISEG6	O	LED Segment Signal 22 Output	
				CS6	IA	Capacitive Touch switch input 6	
80	64	48	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
				AN4	IA	Analog Input 4	
				CP1B	IA	Comparator plus input 1B	
				ISEG5	O	LED Segment Signal 21 Output	

				CS7	IA	Capacitive Touch switch input 7	

Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

1.7 Memory Map

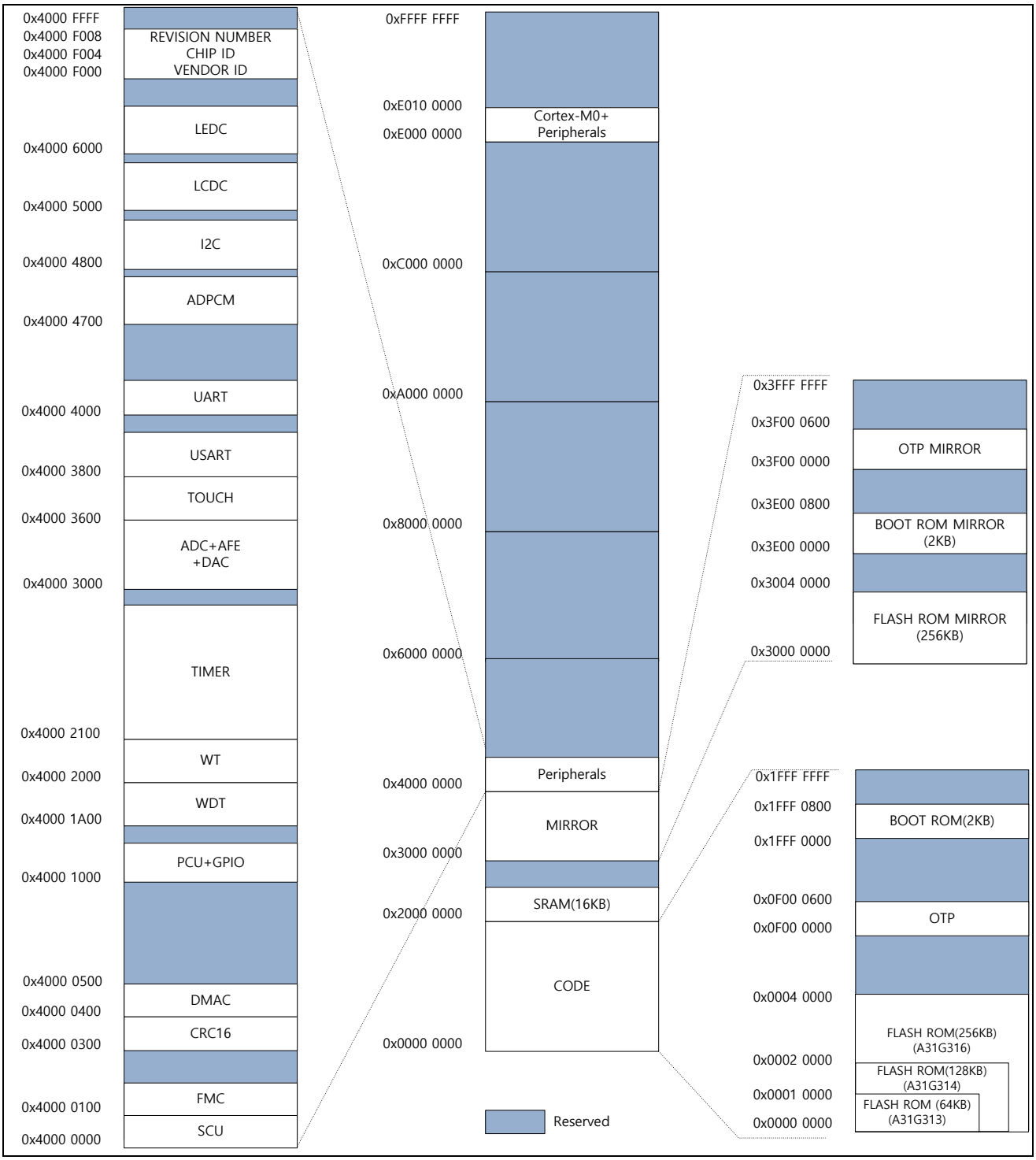


Figure 1.10 Memory Map

CHAPTER 2. CPU

2.1 Cortex-M0+ Core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

2.2 Interrupt Controller

Table 2.1 Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA,B
4	0x0000_0050	GPIOC,D
5	0x0000_0054	GPIOE
6	0x0000_0058	GPIOF
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20
16	0x0000_0080	TIMER21
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	UART0
20	0x0000_0090	UART1
21	0x0000_0094	TIMER13
22	0x0000_0098	TIMER14
23	0x0000_009C	TIMER15
24	0x0000_00A0	TIMER16

25	0x0000_00A4	I2C2
26	0x0000_00A8	USART12/USART13
27	0x0000_00AC	ADPCM/DAC
28	0x0000_00B0	LED
29	0x0000_00B4	TOUCH
30	0x0000_00B8	Reserved
31	0x0000_00BC	COMP/CRC

(Note)

Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits). NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

** __NVIC_PRIO_BITS = 2

CHAPTER 3. Boot Mode

3.1 Boot Mode Pins

A31G31x has boot mode option to program internal flash memory.
Boot mode can be entered by setting BOOT pin to 'L' at reset timing. (Normal state is 'H')
The boot mode supports UART boot and SPI boot.
UART boot uses TXD10/RXD10 port, and SPI boot uses MOSI10/MISO10/SCK10/SS10 port.
The pins for boot mode are listed as following:

Table 3.1 Boot mode pin list

Block	Pin Name	Dir	Description
SYSTEM	**nRESET**	I	Reset Input signal
	BOOT/PB3	I	'0' to enter Boot mode
UART mode of USART10	**RXD10/PB1**	I	UART Boot Receive Data
	TXD10/PB0	O	UART Boot Transmit Data
SPI mode of USART10	**SS10/PB3**	I	SPI Boot Slave Selectable after Boot ROM
	SCK10/PB2	I	SPI Boot Clock Input
	MISO10/PB1	I	SPI Boot Data Input with function exchange
	MOSI10/PB0	O	SPI Boot Data Output with function exchange

3.2 Boot Mode Connections

User can design target board using any of boot mode ports – UART or SPI mode of USART10.
Followings are sample connection diagrams of boot mode.

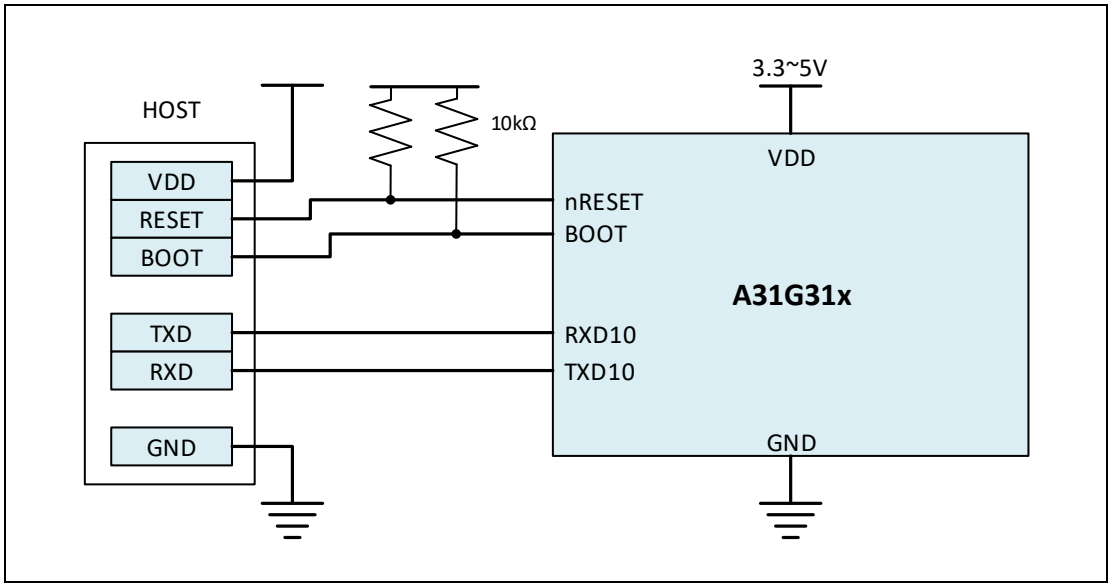
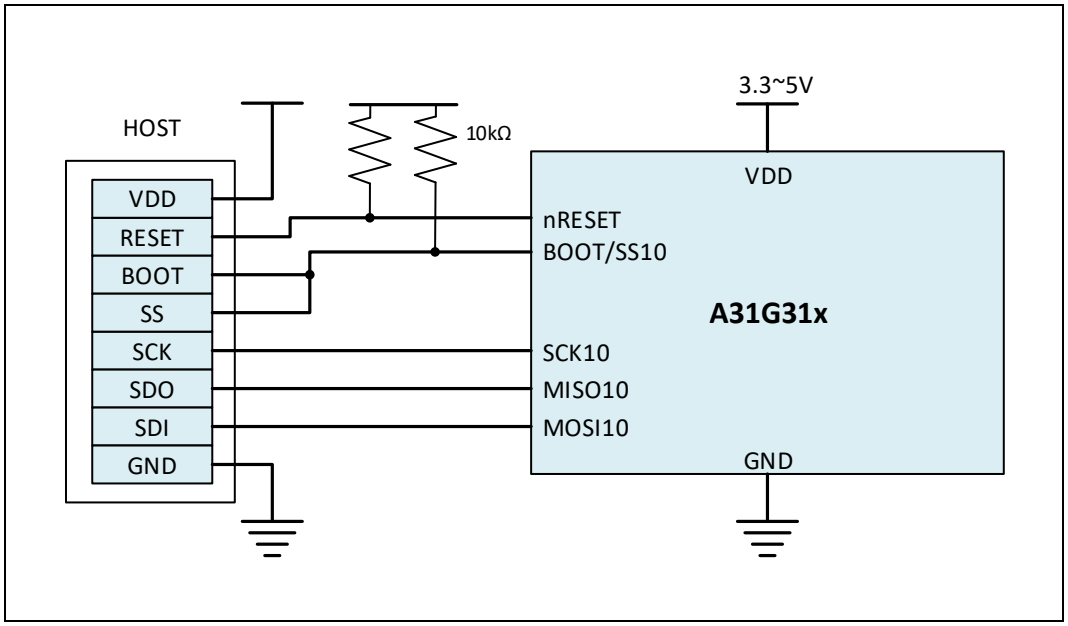


Figure 3.1 Connection diagram of UART Boot



NOTE) The MISO 10 and MOSI 10 exchange options are activated automatically in boot mode. MISO 10 must be HIGH level for using SPI Boot.

Figure 3.2 Connection diagram of SPI Boot

3.3 SWD Mode Connections

User can use the SWD mode for writing with E-PGM+.
This can be used for writing & debugging.

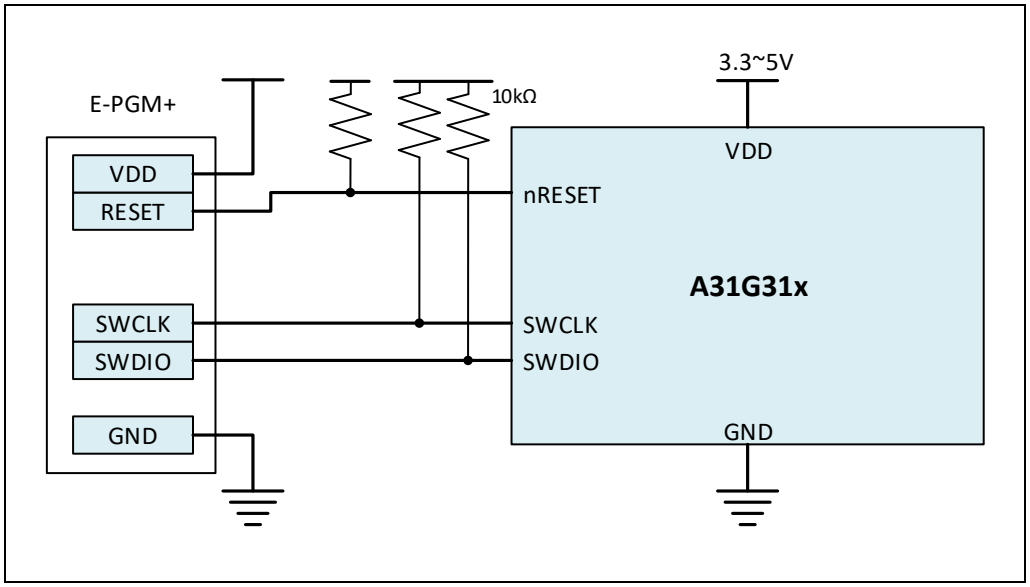


Figure 3.3 Connection diagram of E-PGM+ and SWD Port

CHAPTER 4. SYSTEM CONTROL UNIT (SCU)

4.1 OVERVIEW

The A31G31x has built-in intelligent power control block which manages system analog blocks and operating modes

Internal reset and clock signals are controlled by SCU block to maintain optimize system performance and power dissipation.

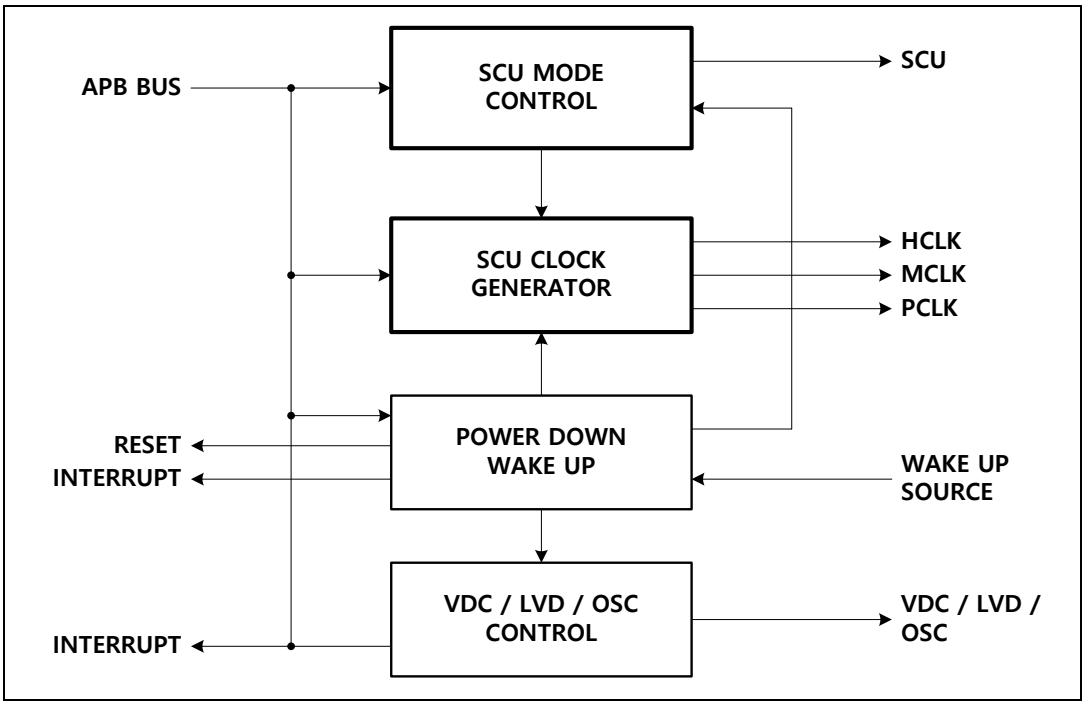


Figure 4.1 SCU Block Diagram

4.2 CLOCK SYSTEM

A31G31x has two main operating clocks. One is HCLK which supplies the clock to CPU and AHB bus system. The other one is PCLK which supplies the clock to Peripheral systems.

User can control the clock system variation by software. The below figure shows the clock system of the chip. And the below table shows clock source descriptions.

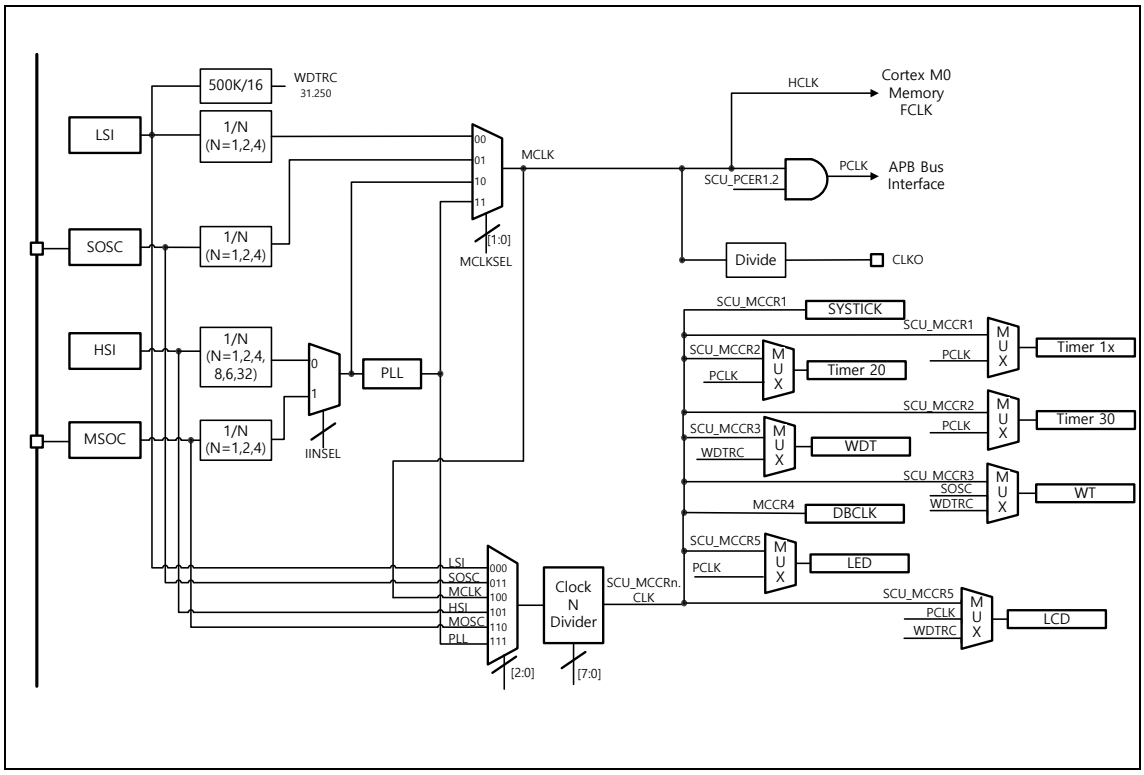


Figure 4.2 Clock Tree Configuration

All mux to switch clock source have a glitch-free circuit in each. So clock can be switched without glitch risks. When you try to change the clock mux control, both of clock sources should be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 4.1 Clock sources

Clock name	Frequency	Description
MOSC	2-16 MHz	External Crystal OSC
SOSC	32.768 kHz	External Sub Crystal OSC
HSI	48 MHz	High Speed Internal OSC
LSI	500 kHz	Low Speed Internal OSC

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks related with HCLK clock. FCLK and HCLK. FCLK is free running clock and it is always running except power down mode. HCLK can be stopped in the sleep mode and power down mode.

BUS system and memory systems operated by MCLK clock. Max bus operating clock speed is 48MHz.

4.2.2 PCLK clock domain

PCLK is master clock of all the peripheral. Each peripheral clocks enabled by SCU_PCER1 and SCU_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can't be accessible even reading its registers. It can be stopped in power down mode.

4.2.3 Clock configuration procedure

After power up, the default system clock is feed by LSI (500kHz) clock. LSI is default enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

HSI (48MHz) clock can be enabled by SCU_CSCR register.

MOSC (2-16MHz) clock can be enabled by SCU_CSCR register. Before enable MOSC block, the pin mux configuration should be set for XIN, XOUT function. PF1 and PF0 pins are shared with MOSC's XIN and XOUT function – PF.MOD and PF.AFSR1 registers should be configured properly. After enabling the MOSC block, you must wait for more than 5msec time to ensure stable operation of crystal oscillation.

SOSC (32.768kHz) clock can be enabled by SCU_CSCR register. Before enable SOSC block, the pin mux configuration should be set for SXIN, SXOUT function. PF2 and PF3 pins are shared with SOSC's SXIN and SXOUT function – PF_MOD and PF_AFSR1 registers should be configured properly. After enabling the SOSC block, you must wait for more than 10msec time to ensure stable operation of crystal oscillation.

You can change the MCLK by SCU_SCCR Register.

You can find an example flow chart to configure the system clock in below Figure.

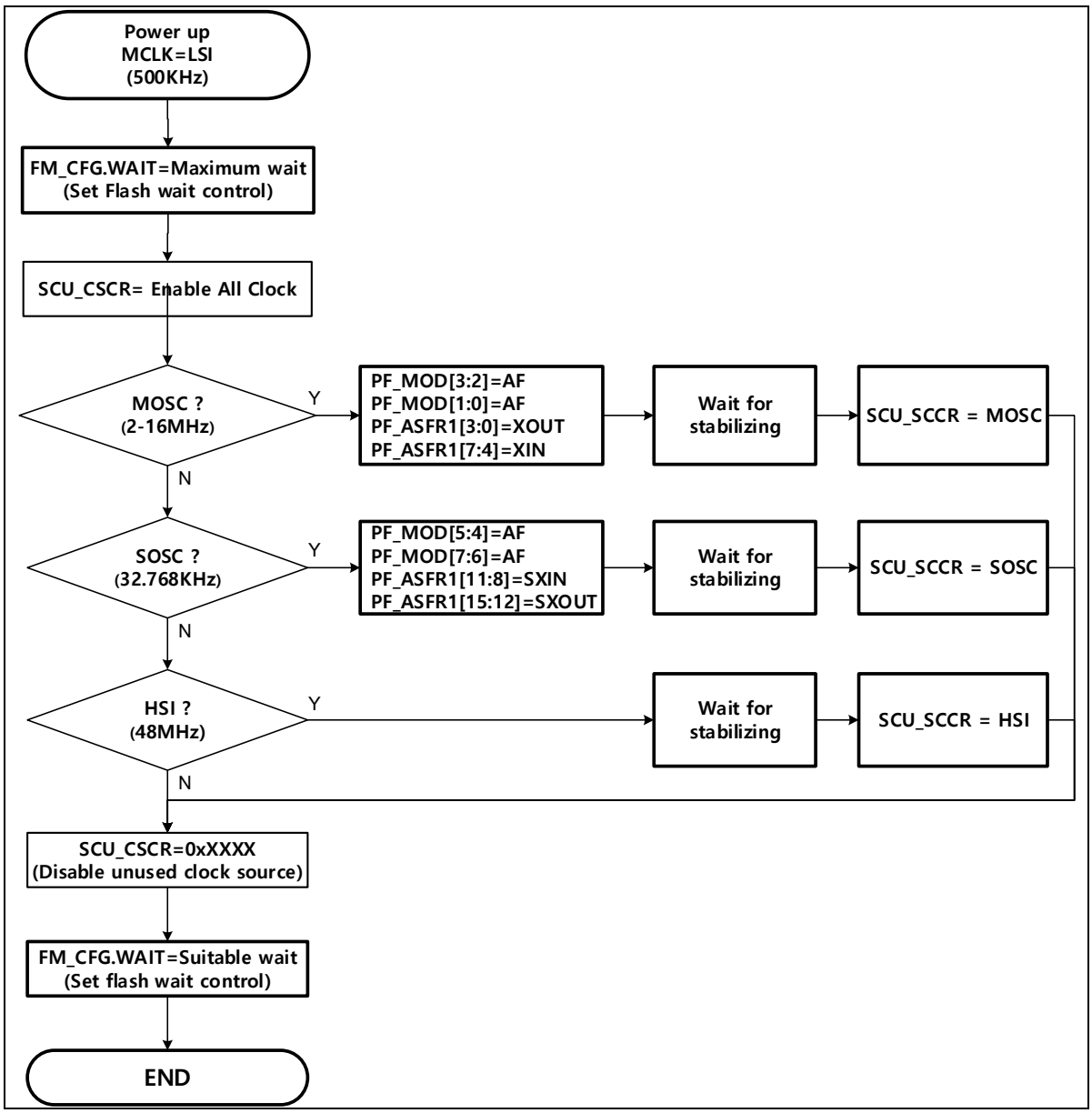


Figure 4.3 Clock change procedure

When you speed up the system clock until max operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for the performance. The wait control recommendation is provided in below table

Table 4.2 Flash wait control recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
00	0 clock wait	~20MHz
01	1 clock wait	~40MHz
10	2 clock wait	~48MHz

4.3 RESET

A31G31x has two system reset. One is the cold reset by POR which is effective during power up or down sequence. The other reset is the warm reset which is generated by several reset sources. The reset events make the chip to turn initial state.

The cold reset has only one reset source which is POR.

The warm reset has several reset sources as below

- nRESET pin
- WDT reset
- LVD reset
- MCLK Fail reset
- MOSC Fail reset
- S/W reset
- CPU request reset

4.3.1 The Cold Reset

The cold reset is important feature of the chip when power is up. This characteristic will globally affect the system boot. Internal VDC is enabled when VDDEXT power is turn on. Internal POR trigger level is 1.6V of VDDEXT voltage out level. At this time, boot operation is started. The LSI clock is enabled and counts 4.25msec time for internal VDC level stabilizing. In this time, VDDEXT voltage level should be over than initial LVD level (1.6V). After 4.25msec counting, the cold reset is released and counts 0.4msec time for warm reset synchronizing. After released cold and warm reset, BOOTROM and CPU are running.

The below figure shows power up sequence and internal reset waveform.

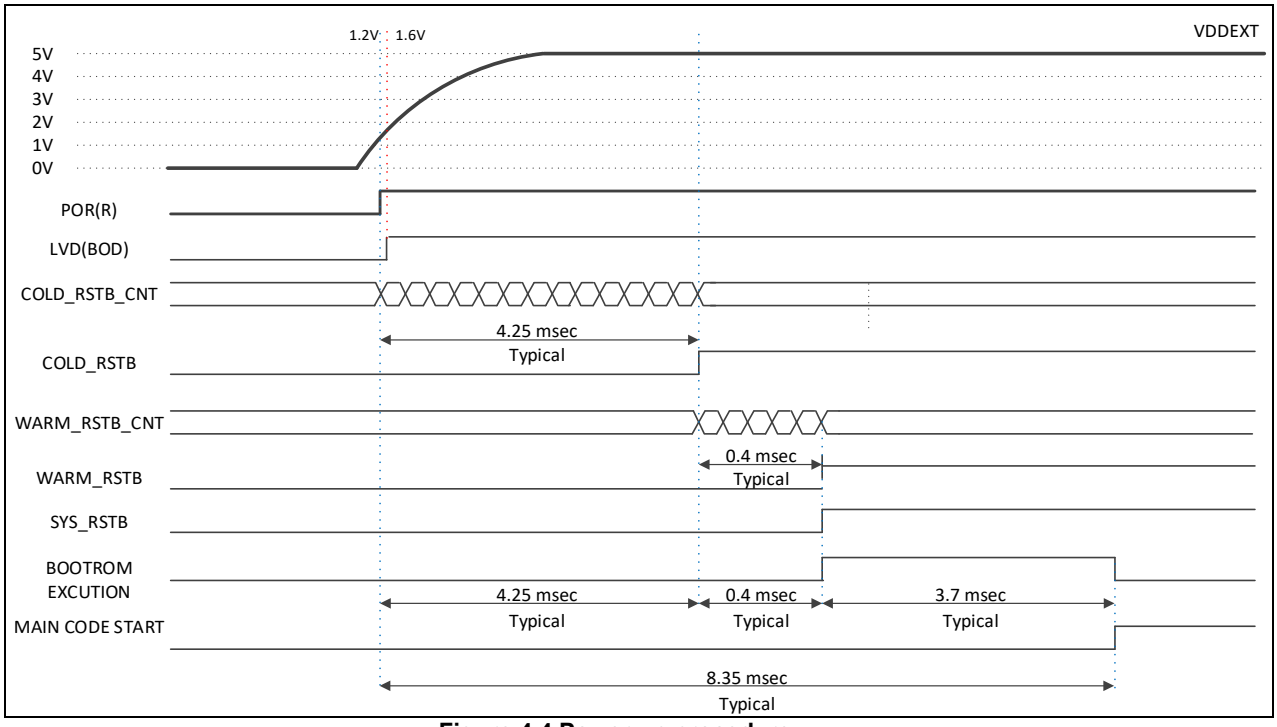


Figure 4.4 Power up procedure

4.3.2 The Warm Reset

The warm reset event has several reset sources and some parts of chip returns to initial state when warm reset condition is occurred.

The warm reset source is controlled by SCU_RSER register and the status is appeared in SCU_RSSR register. The reset for each peripheral blocks is controlled by SCU_PRER register. The reset can be masked independently.

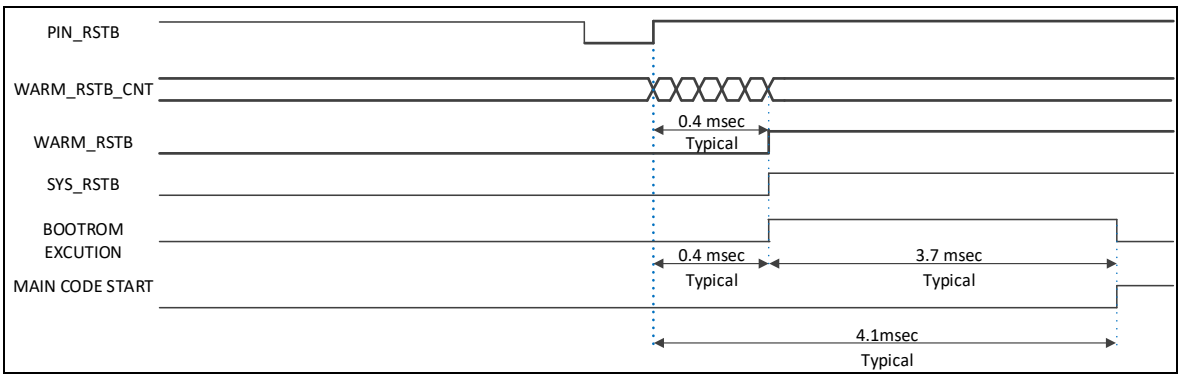


Figure 4.5 Warm reset diagram

4.3.3 The LVR Reset

The voltage level of LVR is set by the low voltage reset configuration register (SCULV_LVRCNFG).

The LVR reset status is appeared in SCU_RSSR register. The reset for LVR is controlled by SCULV_LVRCR register. The register is cleared to “0x00” on POR reset.

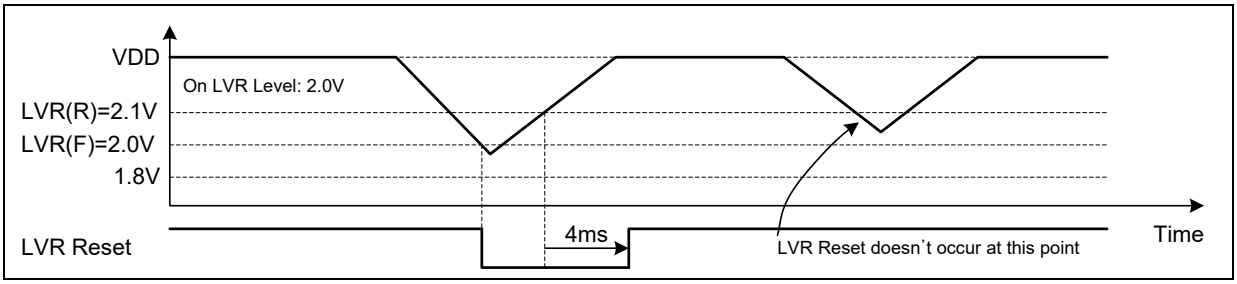


Figure 4.6 LVR Reset Timming Diagram

4.3.4 Reset Tree

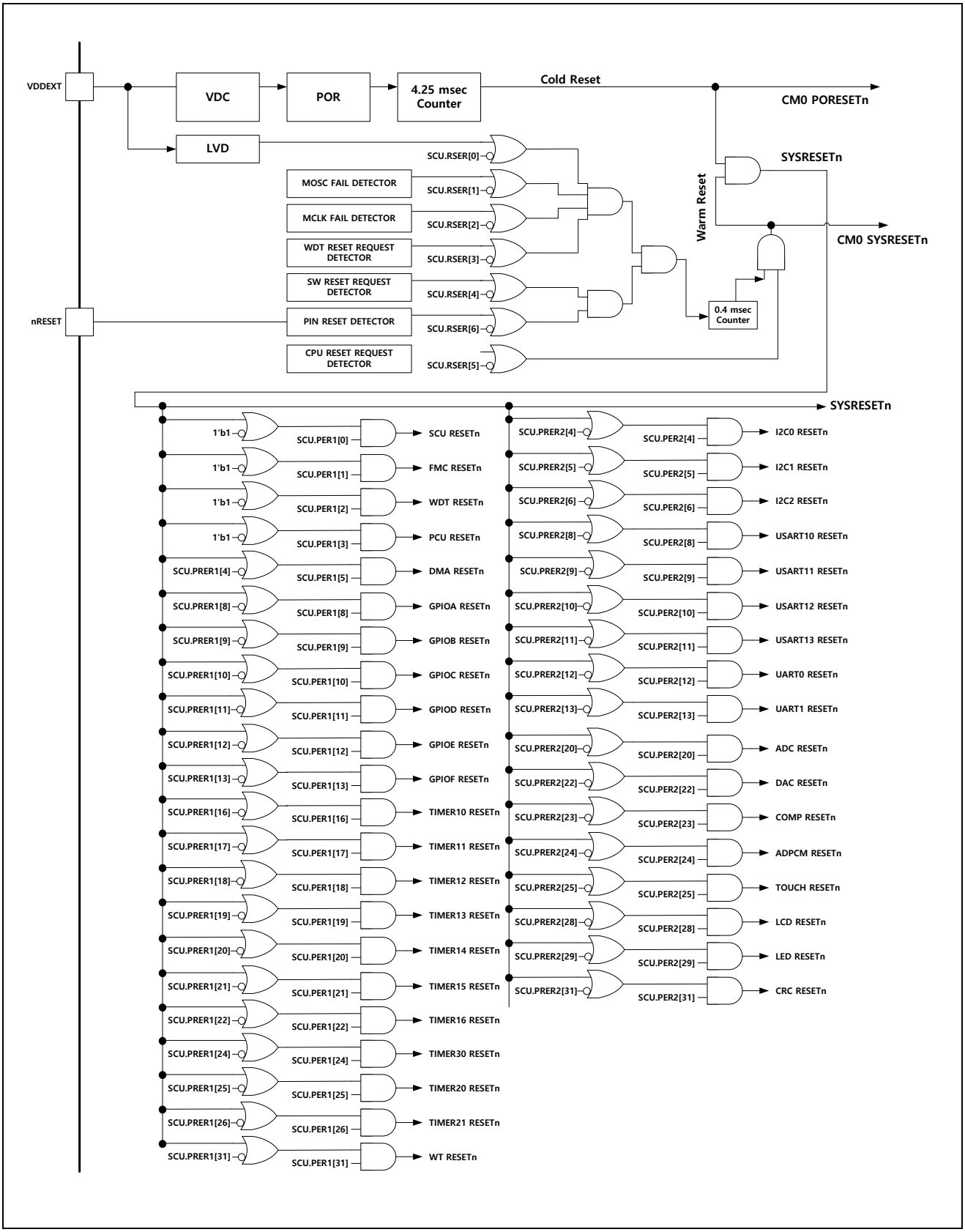


Figure 4.7 Reset tree configuration

4.4 Operation Mode

The INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP and the PD mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals.

Figure 4.8 shows the operation mode transition diagram.

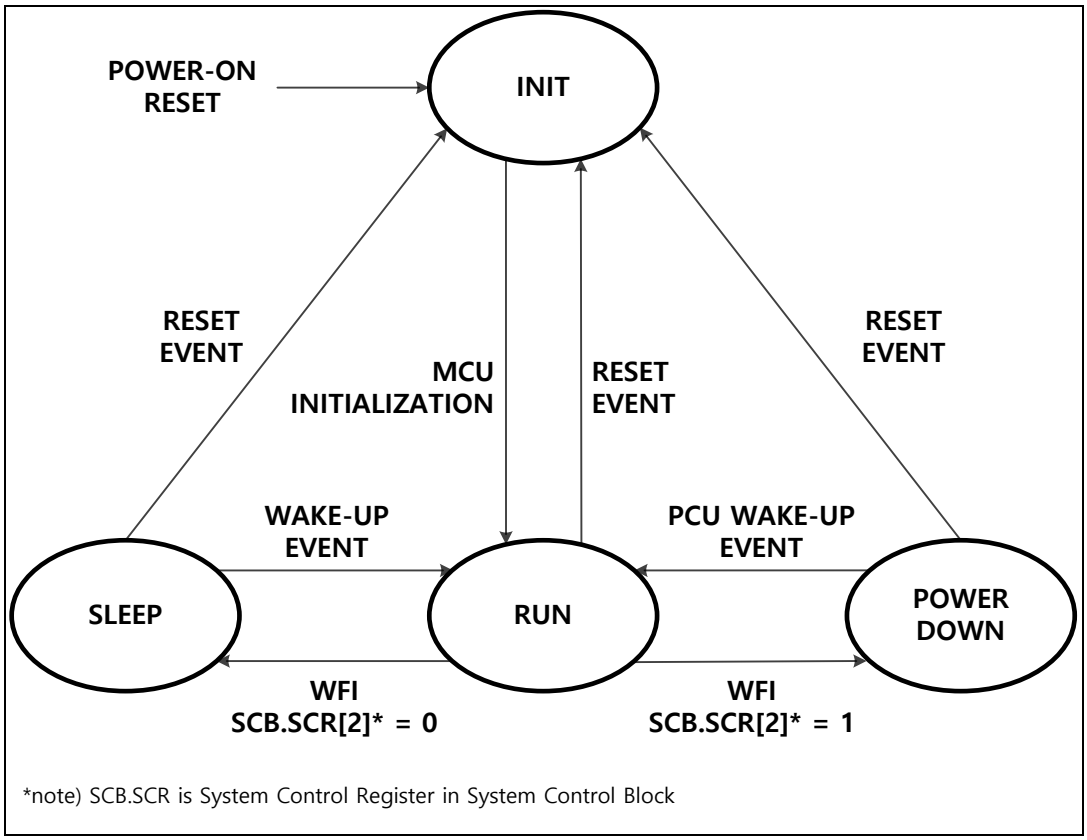


Figure 4.8 Operation Mode Block Diagram

4.4.1 RUN Mode

This mode is to operate the CPU and the peripheral hardware by using the high-speed clock. After reset followed by INIT state, it is entered into RUN mode.

4.4.2 SLEEP Mode

Only the CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the SCU_PER and SCU_PCER register.

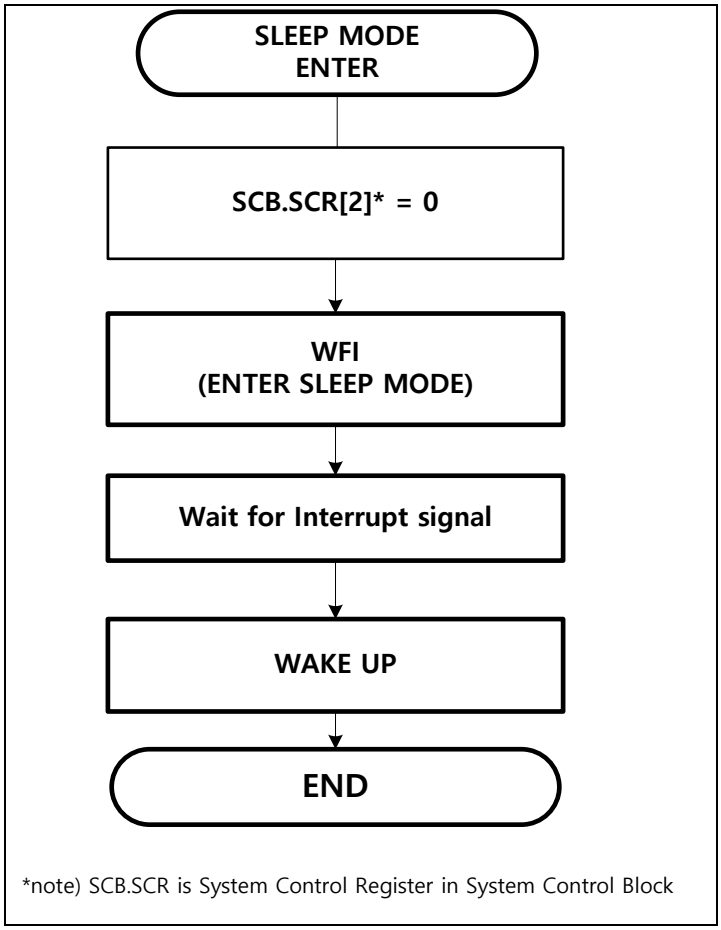


Figure 4.9 Sleep mode sequence

4.4.3 POWER-DOWN Mode

All the internal circuits are entered the stop state.

Power down operation has special power off sequence as below picture.

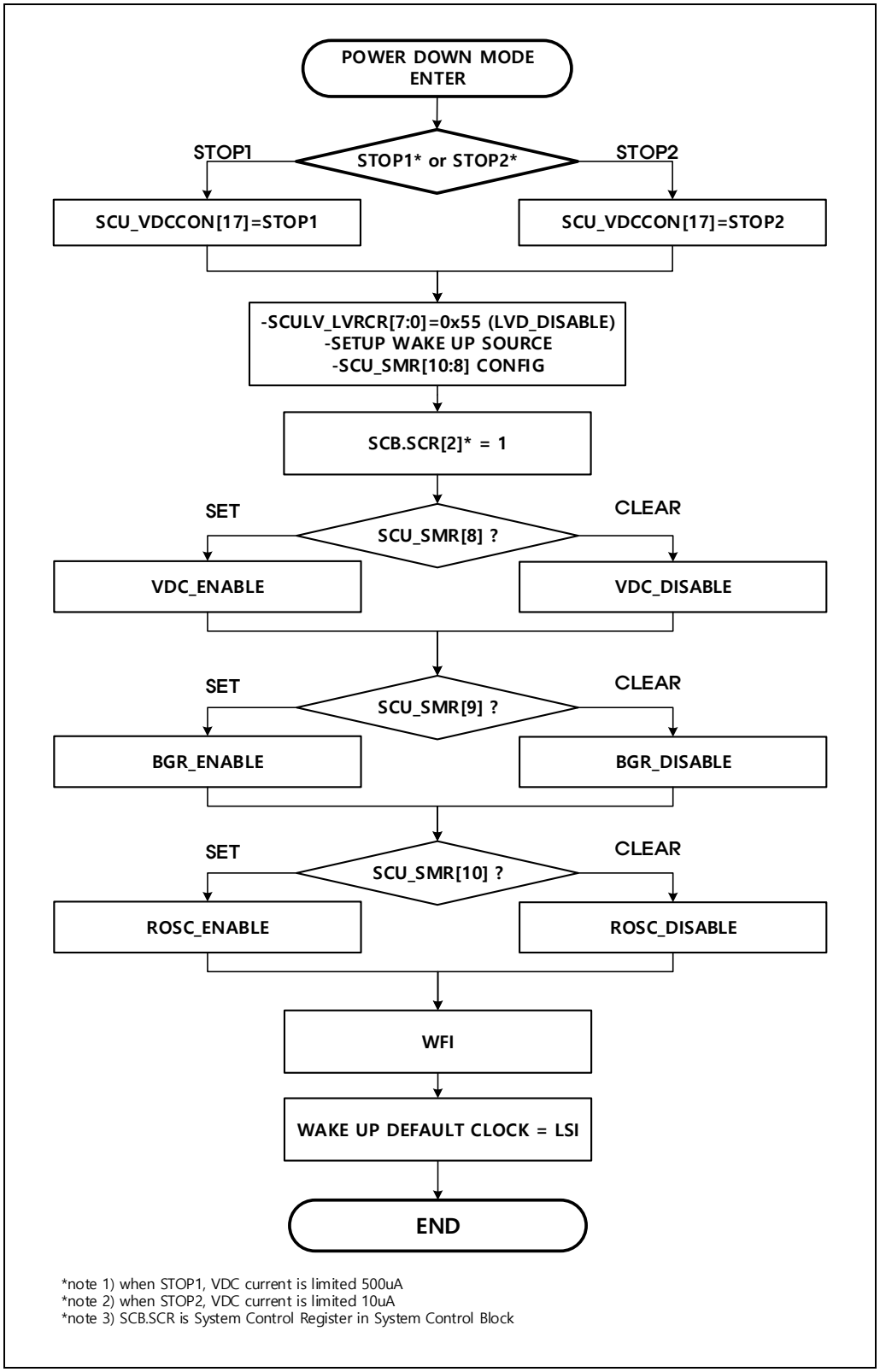


Figure 4.10 Power down mode Sequence

4.5 PIN DESCRIPTION

Table 4.3 SCU pins

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

CHAPTER 5. PORT CONTROL UNIT (PCU) & GPIO

5.1 OVERVIEW

PCU(Port Control Unit) controls the external I/Os as below

- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up/down register control and open drain control

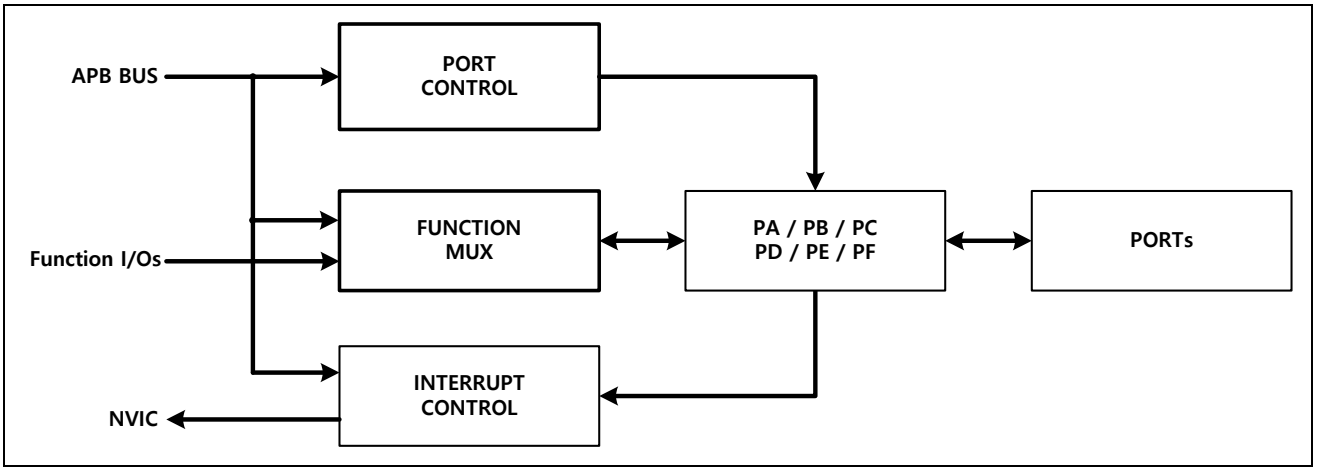


Figure 5.1 Port Control Uint Block Diagram m

Most of pins except dedicated function pins can be used general I/O ports. General input/output ports are controlled by GPIO block.

- Output signal level (H/L) select
- External interrupt interface
- Pull up/down enable or disable

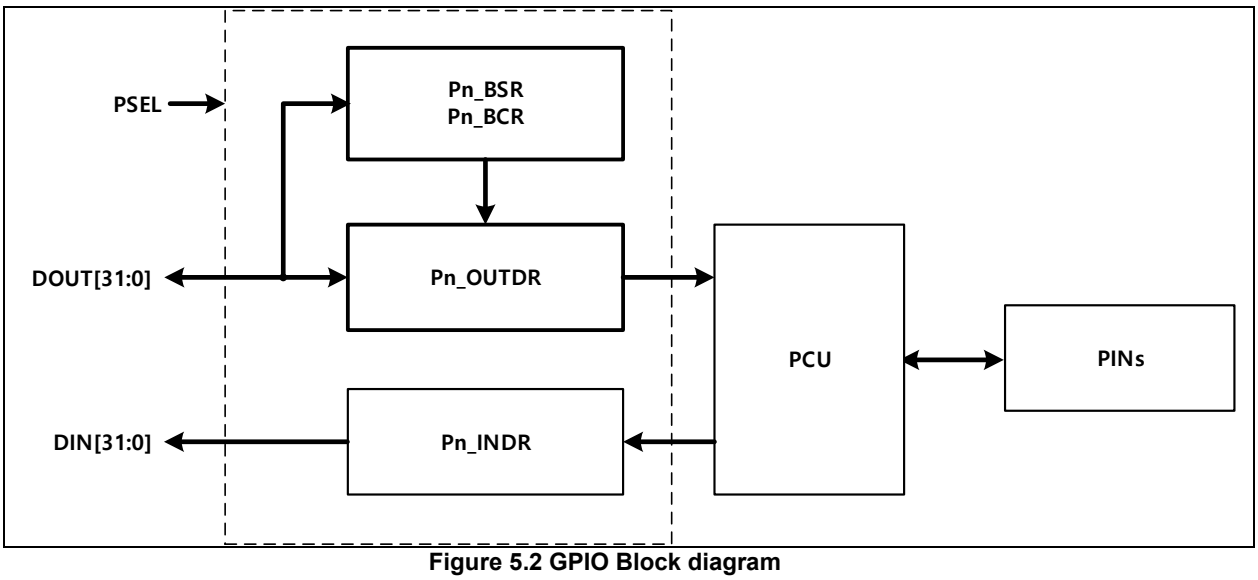


Figure 5.2 GPIO Block diagram

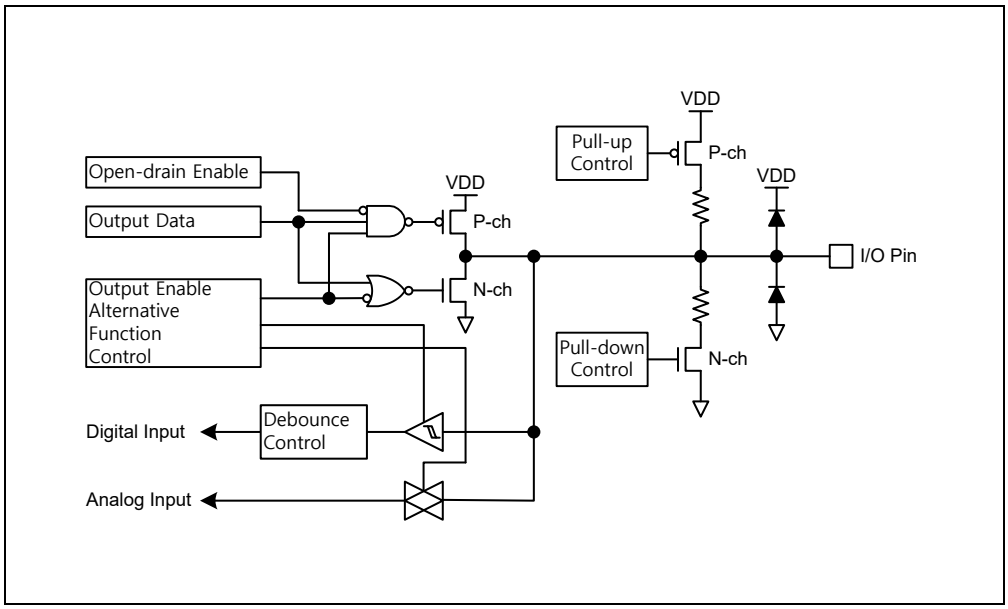


Figure 5.3 I/O Port Block Diagram (External Interrupt I/O pins)

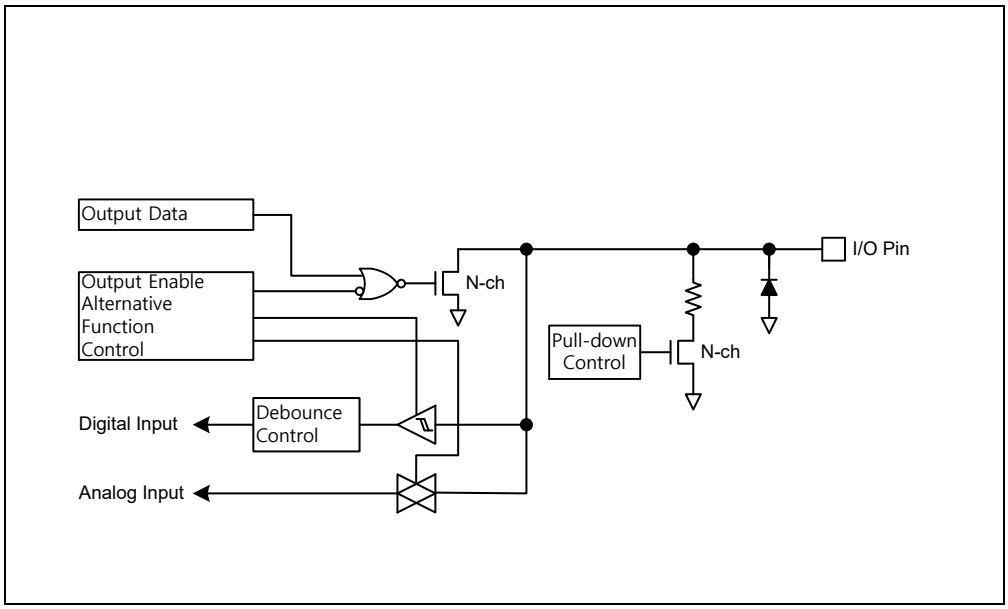


Figure 5.4 I/O Port Block Diagram (PF5, PF6, PF7 I/O pins)

5.2 Pin Multiplexing

GPIO pins have alternative function pins. Below table shows pin multiplexing information.

Table 5.1 GPIO Alternative function

Pin Names	Alternative Functions				
	AF0	AF1	AF2	AF3	AF4
PA0		SDA1		AN0	CS3/ISEG9
PA1		SCL1		AN1	CS4/ISEG8
PA2		EC12		AN2/AVREF/CP0	CS5/ISEG7
PA3				AN3/CP1C	CS6/ISEG6
PA4				AN4/CP1B	CS7/ISEG5
PA5		T12O	T12C	AN5/CP1A	ISEG4
PA6	SEG43			AN6/CREF1/DAO	ISEG3
PA7	SEG42			AN7/CREF0/DAVREF	ISEG2
-					
PA9				AN12	CS0
PA10				AN13	CS1
PA11				AN14	CS2
PB0	SEG41	TXD10	MOSI10	AN8	CS8/ICOM26/ISEG1
PB1	SEG40	RXD10	MISO10	AN9	CS9/ICOM25/ISEG0
PB2	SEG39		SCK10	AN10	CS10/ICOM24
PB3	SEG38	BOOT	SS10		ICOM23
PB4	SEG37	TXD0	SWCLK		ICOM22
PB5	SEG36	RXD0	SWDIO		ICOM21
PB6	SEG35	TXD1			ICOM20
PB7	SEG34	RXD1			ICOM19
PB8	SEG33	T15O	T15C	EC16	CS11/EC16
PB9	SEG32	T16O	T16C	EC15	CS12/EC15
PB10	SEG31	T16C	EC15	T16O	CS13/T16O
PB11	SEG30	T15C	EC16	T15O	CS14/T15O
PB12	SEG29				CS15
PB13	SEG28				CS16
PB14	SEG27				CS17
PB15	SEG26				CS18

Table 5.2 GPIO Alternative function

Pin Names	Alternative Functions				
	AF0	AF1	AF2	AF3	AF4
PC0	SEG25	T20O	T20C		CS19/ICOM18
PC1	SEG24	T21O	T21C		CS20/ICOM17
PC2	SEG23	EC20			CS21/ICOM16
PC3	SEG22	EC21			CS22/ICOM15
PC4	SEG21				CS23/ICOM14
PC5	SEG20	SDA2			
PC6	SEG19	SCL2			
PC7	SEG18				
PC8	SEG17				
PC9	SEG16				
PC10	SEG15				
PC11	SEG14	EC10			
PC12	SEG13	EC11			
PD0	SEG12	SCL0			ICOM13
PD1	SEG11	SDA0			ICOM12
PD2	SEG10	TXD11	MOSI11		ICOM11
PD3	SEG9	RXD11	MISO11		ICOM10
PD4	SEG8		SCK11		ICOM9
PD5	SEG7		SS11		ICOM8

Table5.3 GPIO Alternative function

Pin Names	Alternative Functions				
	AF0	AF1	AF2	AF3	AF4
PE0	COM0	PWM30AA			ICOM0
PE1	COM1	PWM30AB			ICOM1
PE2	COM2	PWM30BA			ICOM2
PE3	COM3/SEG0	PWM30BB			ICOM3
PE4	COM4/SEG1	PWM30CA			ICOM4
PE5	COM5/SEG2	PWM30CB			ICOM5
PE6	COM6/SEG3	T10O	T10C		ICOM6
PE7	COM7/SEG4	T11O	T11C		ICOM7
PE8		TXD13	MOSI13	VLC0	
PE9		RXD13	MISO13	VLC1	
PE10			SCK13	VLC2	
PE11			SS13	VLC3	
PE12		TXD12	MOSI12		
PE13		RXD12	MISO12		
PE14	SEG5		SCK12		
PE15	SEG6		SS12		
PF0		SCL1		XOUT	ISEG10
PF1		SDA1		XIN	
PF2		TXD1		SXIN	
PF3		RXD1		SXOUT	
PF4		CLKO		R-SET	
PF5		BLNK			
PF6		EC30	SCL0		
PF7		T30C	SDA0		
PF8		EC13			
PF9		EC14			
PF10		T13O	T13C		
PF11		T14O	T14C		

Notes)

1. On connection with debugger host, The SWCLK and SWDIO pins are always for SW-DP pins. So, the corresponding bits of PB_MOD/PB_TYP/PB_AFSR1/PB_PUPD registers may not be written by software.

5.3 PIN DESCRIPTION

Table 5.4 External signal

PIN NAME	TYPE	DESCRIPTION
PA	IO	PA0 – PA7, PA9 – PA11
PB	IO	PB0 – PB15
PC	IO	PC0 – PC12
PD	IO	PD0 – PD5
PE	IO	PE0 – PE15
PF	IO	PF0 – PF10

CHAPTER 6. FLASH MEMORY CONTROLLER

6.1 OVERVIEW

Flash Memory Controller is an internal flash memory interface controller.

- 0-wait, 1-wait, 2-wait(default)
- Read protection support
- Self Program support
- User option area
  - 3-page (each 512 Bytes)
  - Erase, Program in user mode

Item	Decription
Size	64KB / 128KB / 256KB
Start Address	0x0000_0000
End Address	0x0002_0000
Page Size	512-byte
Total Page Count	256 pages
PGM Unit	512-byte
Erase Unit	512-byte / 1KB / 4KB / bulk

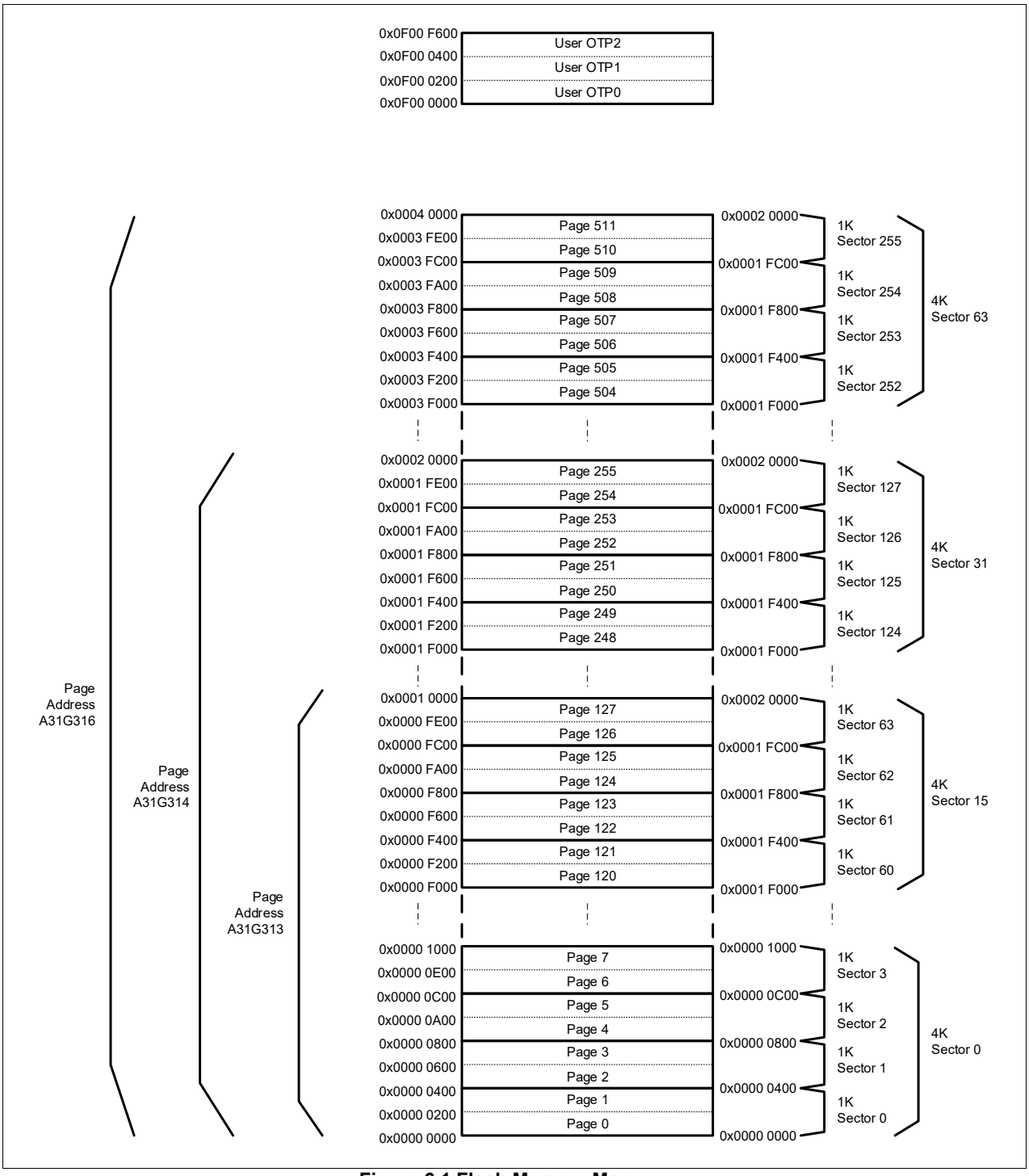


Figure 6.1 Flash Memory Map

CHAPTER 7. INTERNAL SRAM

7.1 OVERVIEW

The A31G31x has a block of 0-wait on-chip SRAM. The size of SRAM is 16KB.

The SRAM base address is 0x2000_0000

The SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/pgm operation.

This device does not support memory remap strategy. So jump and return is required to perform the code in SRAM memory area.

CHAPTER 8. DIRECT MEMORY ACCESS CONTROLLER (DMAC)

8.1 OVERVIEW

DMA is direct memory access controller

The A31G31x's DMA can access UART Tx & Rx and CRC blocks.

DMA transfers data from RAM to peripheral devices or transfers data from peripheral devices to RAM.

- 4 Channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through peripheral interrupt

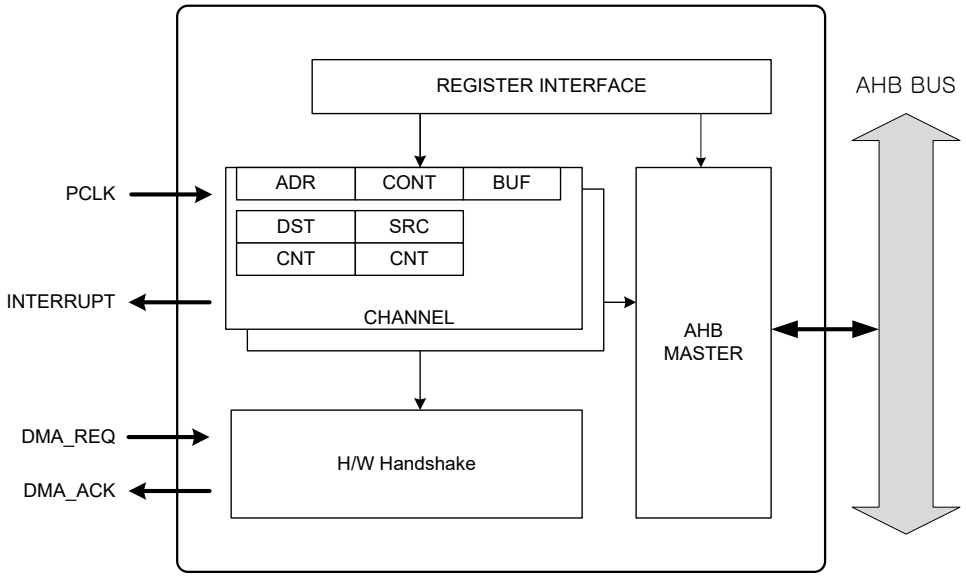


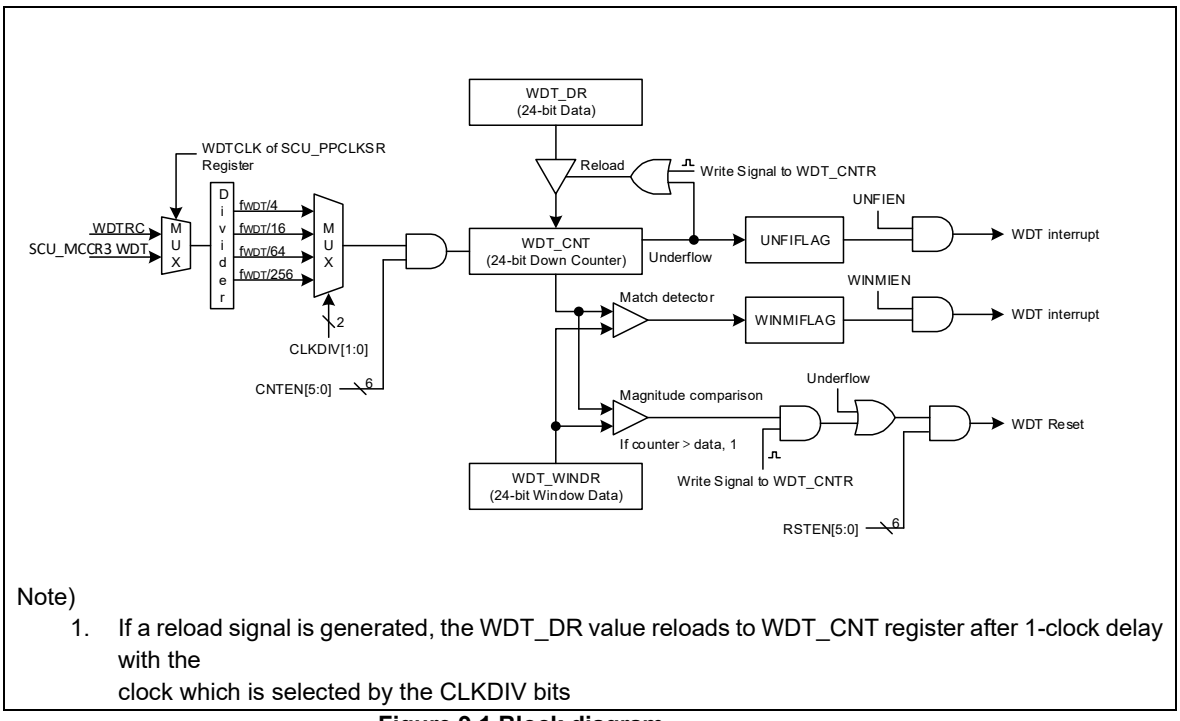
Figure 8.1. Block Diagram

CHAPTER 9. WATCH-DOG TIMER (WDT)

9.1 OVERVIEW

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. When WDT_CNT value is reached WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of the watchdog timer can set by WDT_DR. If an underflow occurs, an internal reset is generated. The watchdog timer operates on the WDTRC embedded RC oscillator clock.

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Include Conuter Window function



Note)

1. If a reload signal is generated, the WDT_DR value reloads to WDT_CNT register after 1-clock delay with the
   clock which is selected by the CLKDIV bits

Figure 9.1 Block diagram

CHAPTER 10. WATCH TIMER

10.1 OVERVIEW

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register. To operate the watch timer, determine the input clock source, output interval and set WTEN as '1' in watch timer control register (WT_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT_CR register. Even if CPU is STOP mode, sub clock is able to be alive and so WT can continue the operation. The watch timer counter circuits is composed of 26-bit counter. Low 14-bit is binary counter and high 12-bit is auto reload counter in order to raise resolution. In WTR, it can control WT clear and set Interval value at write time, and it can read 12-bit WT counter value at read time.

- 14-bit Divider
- 12-bit up-counter
- RTC function

Figure shows the block diagram of a watch timer block.

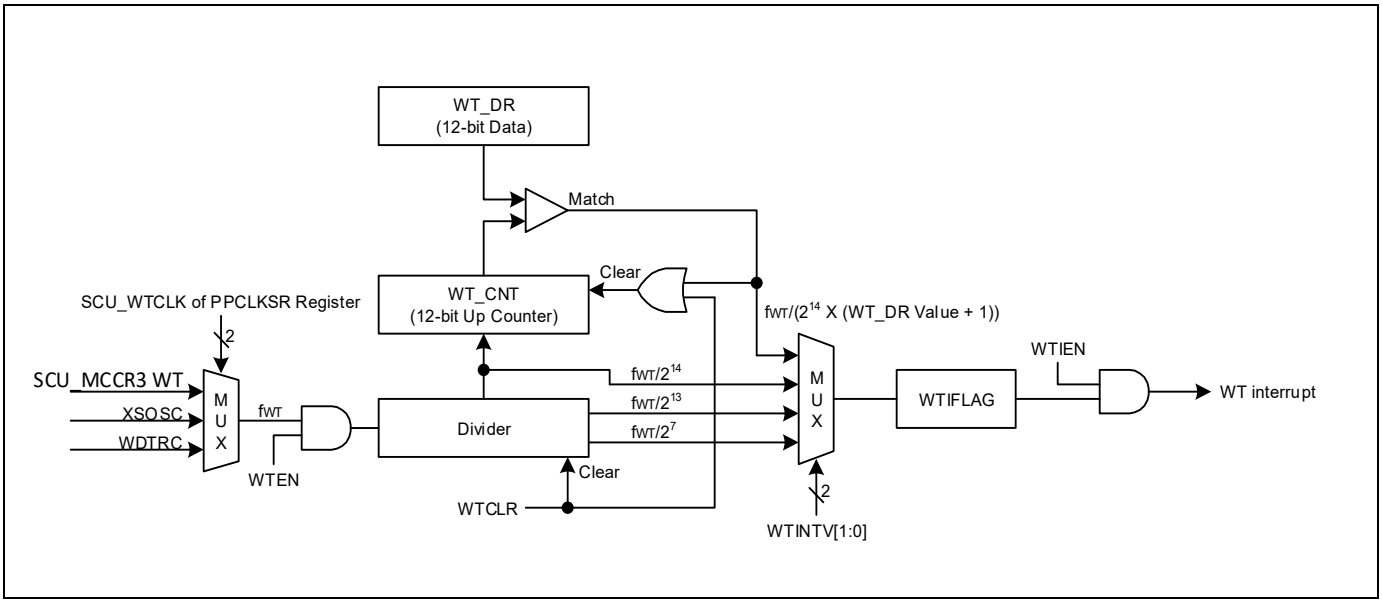


Figure 10.1 Block diagram

CHAPTER 11. 16-BIT TIMER

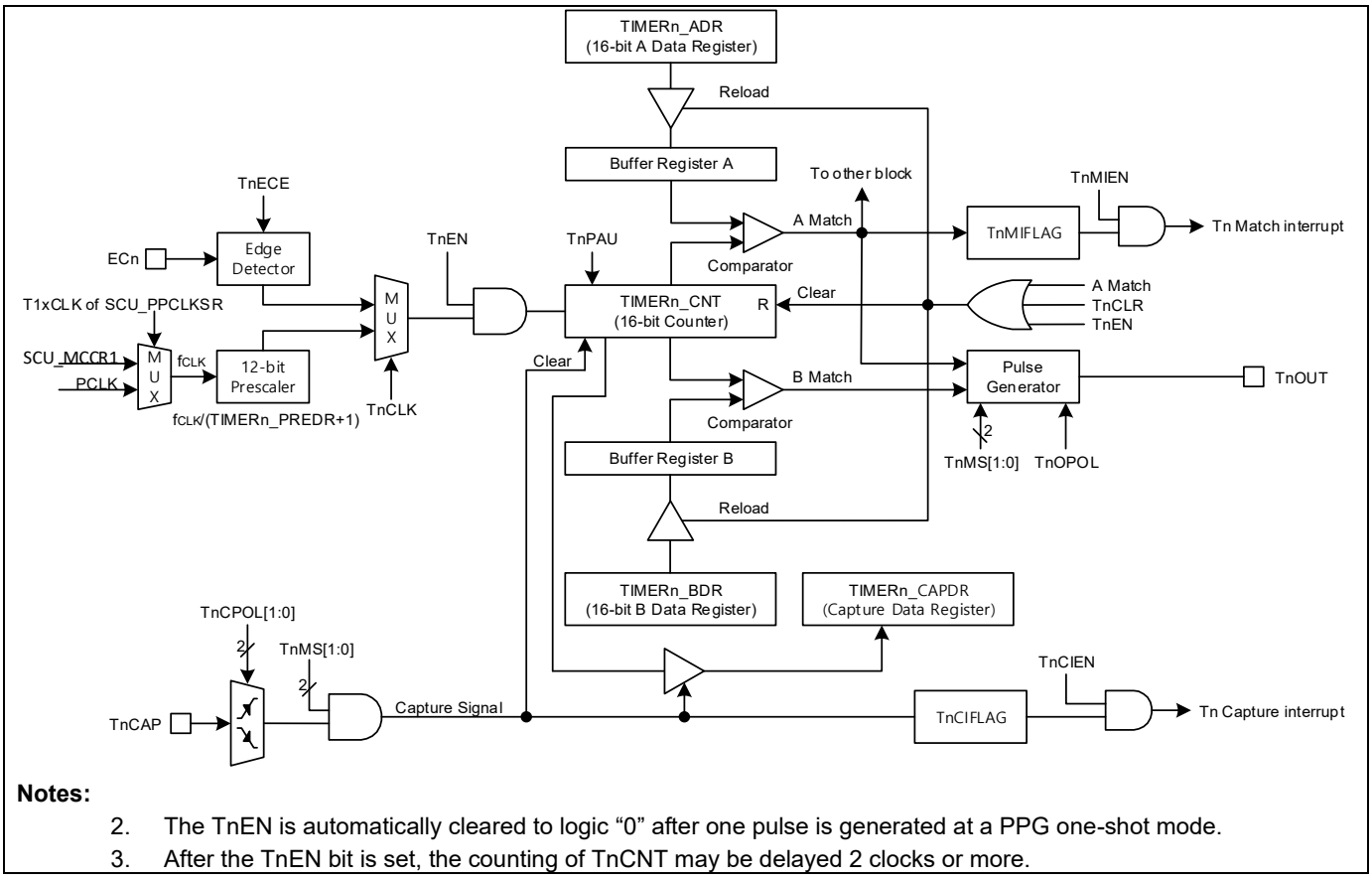
11.1 OVERVIEW

The timer block is consisted with 7 channels of 16 bit General purpose timers. They have independent 16 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Figure shows the block diagram of a unit timer block.



Notes:

2. The TnEN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
3. After the TnEN bit is set, the counting of TnCNT may be delayed 2 clocks or more.

Figure 11.1 Block diagram

11.2 Pin Description

Table 11.1 External pin (n = 10, 11, 12, 13, 14, 15 and 16)

PIN NAME	TYPE	DESCRIPTION
ECn	I	Timer 1n External clock input
TnC	I	Timer 1n Capture input
TnO	O	Timer 1n Output

CHAPTER 12. 32-BIT TIMER 20

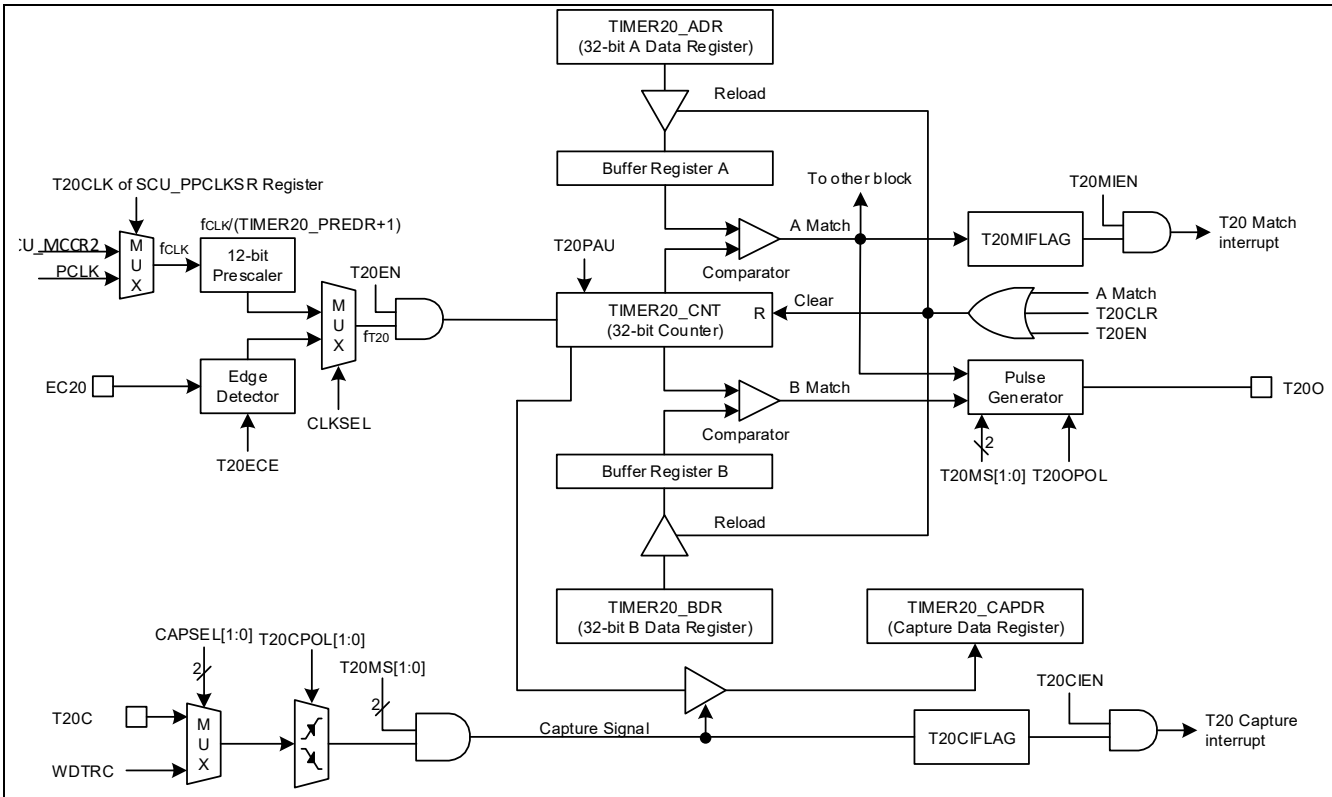
12.1 OVERVIEW

The timer block is consisted with 1 channel of 32 bit General purpose timers. They have independent 32 bit counter and dedicated prescaler feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer.

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Figure shows the block diagram of a unit timer block.



Notes:

1. The T20EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T20EN bit is set, the counting of T20_CNT may be delayed 2 clocks or more.

Figure 12.1 Block diagram

12.2 Pin Description

Table 12.1 External pin

PIN NAME	TYPE	DESCRIPTION
EC20	I	External Clock input
T20C	I	Capture input
T20O	O	Timer/PWM/one-shot output

CHAPTER 13. 32-BIT TIMER 21

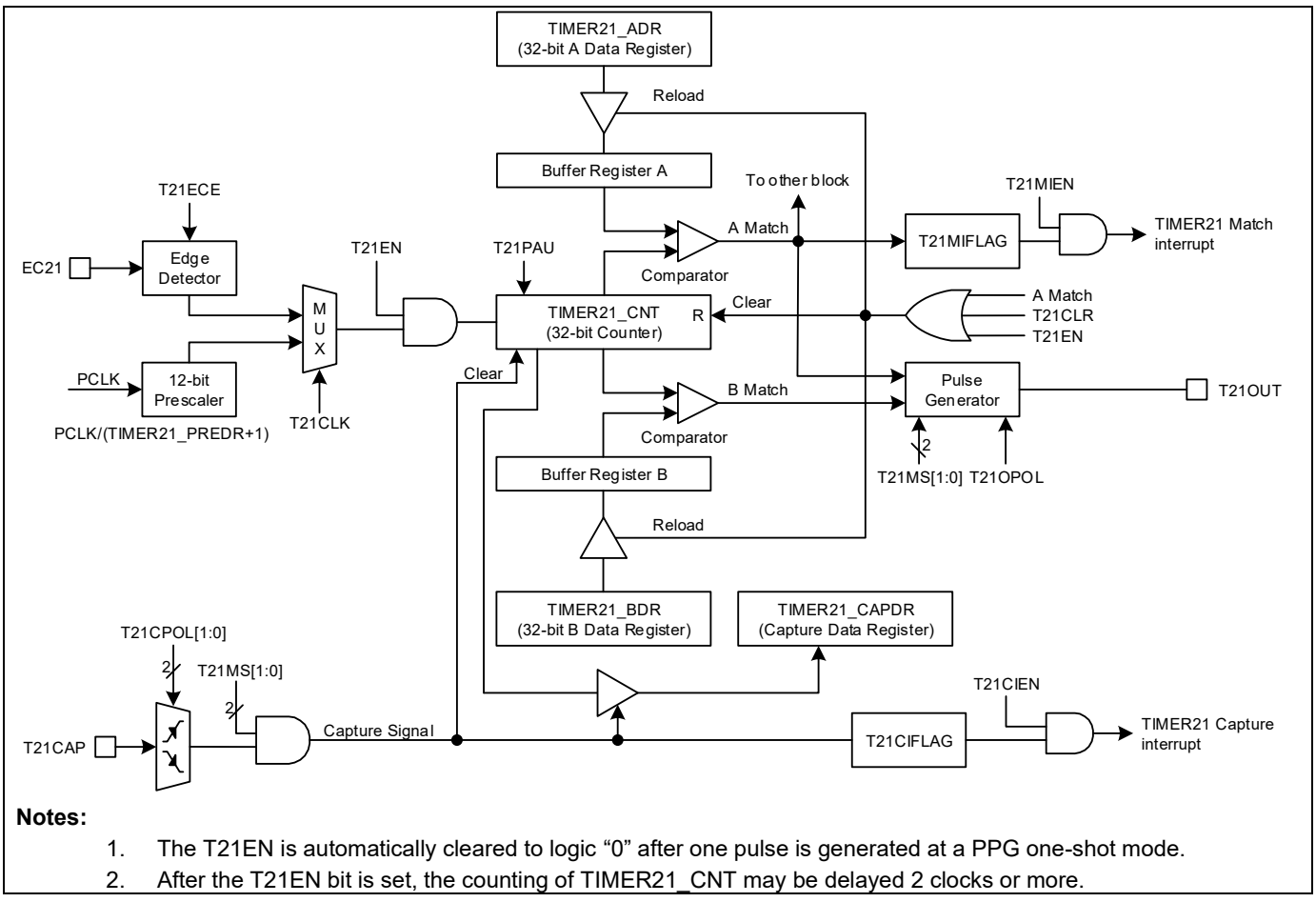
13.1 OVERVIEW

The timer block is consisted with 1 channel of 32 bit General purpose timers. They have independent 32 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Figure shows the block diagram of a unit timer block.



Notes:

1. The T21EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.
2. After the T21EN bit is set, the counting of TIMER21_CNT may be delayed 2 clocks or more.

Figure 13.1 Block diagram

13.2 Pin Description

Table 13.1 External pin

PIN NAME	TYPE	DESCRIPTION
EC21	I	External Clock input
T21C	I	Capture input
T21O	O	Timer/PWM/one-shot output

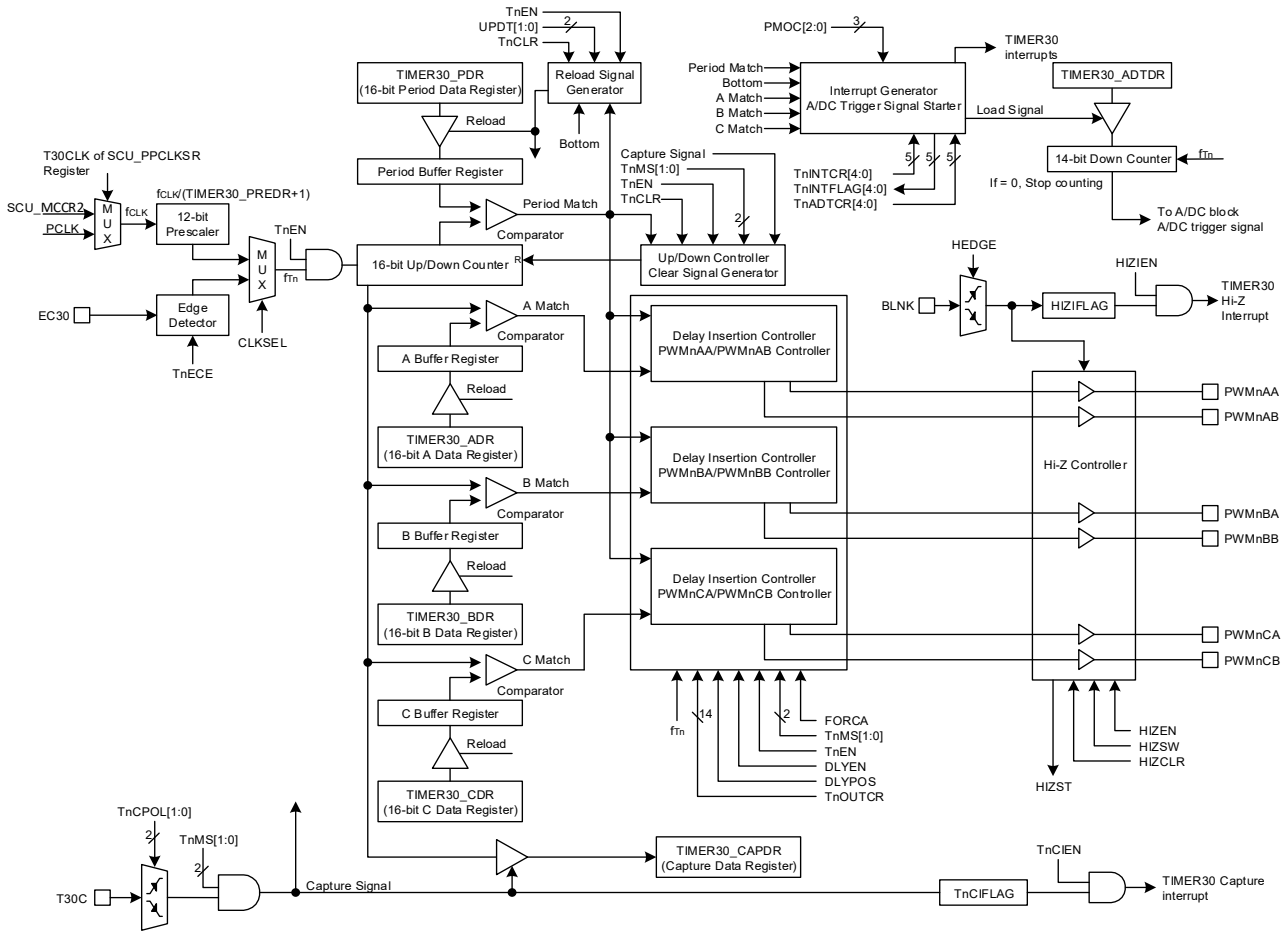
CHAPTER 14. TIMER COUNTER 30

14.1 OVERVIEW

The 16-bit timer 30 module has multiplexer, comparator, 16-bit timer data register A/B/C, 16-bit timer period data register, timer 30 output control register, timer 30 control register, timer 30 PWM output delay register, timer 30 interrupt control register, timer 30 interrupt flag register, timer 30 A/DC trigger control register, timer 30 A/DC trigger generator data register and timer 30 high-Impedance control register (T30ADR, T30BDR, T30CDR, T30PDR, T30OUTCR, T30CR, T30DLY, T30INTCR, T30INTFLAG, T30ADTCR, T30ADTDR, T30HIZCR).

- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

Figure shows the block diagram of a unit timer block.



Notes:

1. The Period/A/B/C match interrupts except for Bottom can occur in the interval mode.
2. The Period match interrupt only can occur in the capture mode.
3. The 16-bit up/down counter in the capture mode is cleared to “0000H” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
4. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, All TIMER30 PWM outputs can be high-impedance state with setting the HIZSW bit to ‘1’ by the UI of debugger.
5. After the TnEN bit is set, the counting of TIMER30_CNT may be delayed 2 clocks or more.

Figure 14.1 Block diagram

14.2 Pin Description

Table 14.1 External pin

PIN NAME	TYPE	DESCRIPTION
EC30	I	External clock input
T30C	I	Capture input
BLNK	I	External Sync Signal Input
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

CHAPTER 15. UNIVERSAL SYNCHRONOUS/ASYNCHRONOUS RECEIVER/TRANSMITTER (USART)

15.1 OVERVIEW

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data OverRun Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

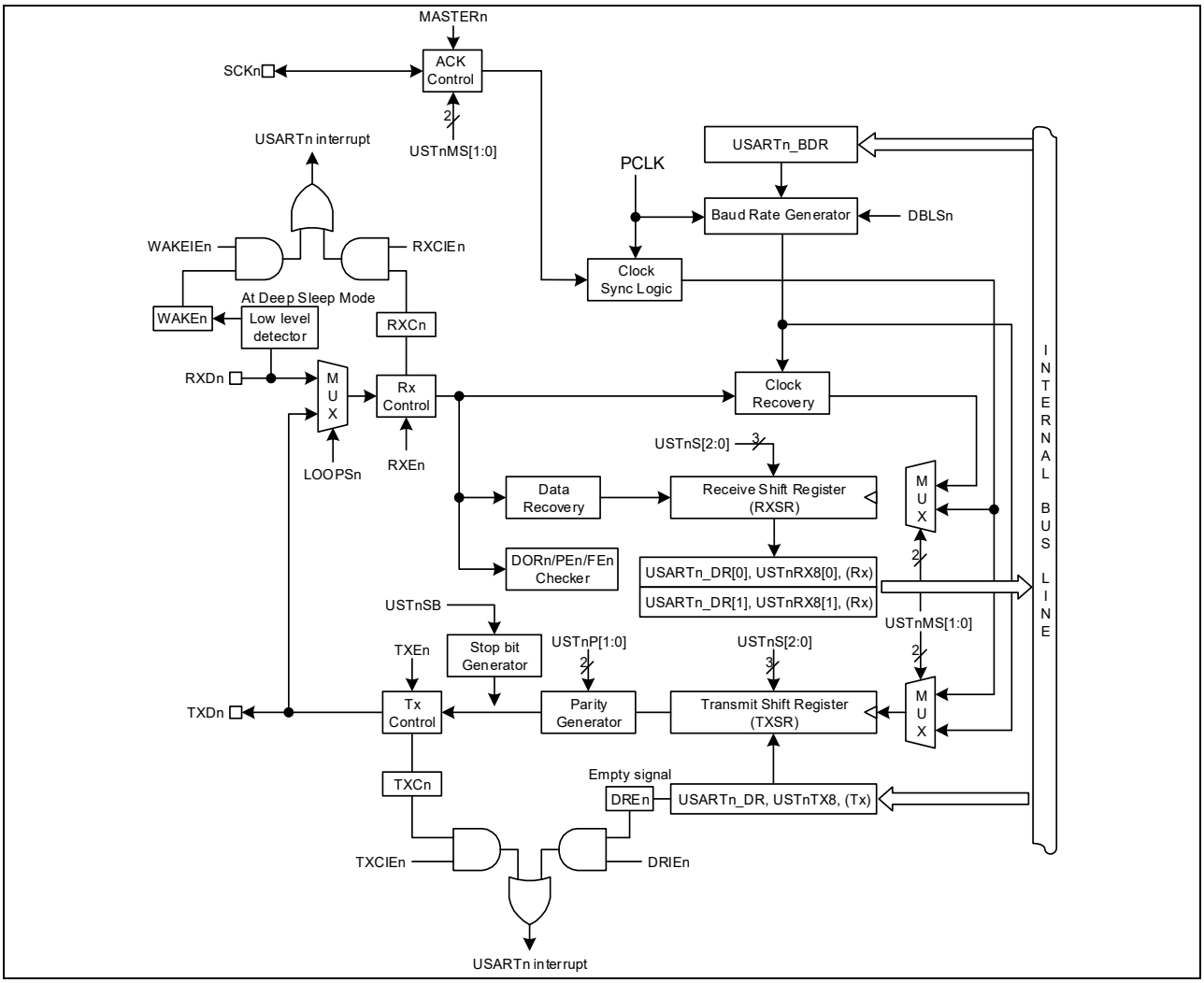


Figure 15.1. UART Block diagram (Where n = 10, 11, 12 and 13)

Figure shows the block diagram of a SPI block

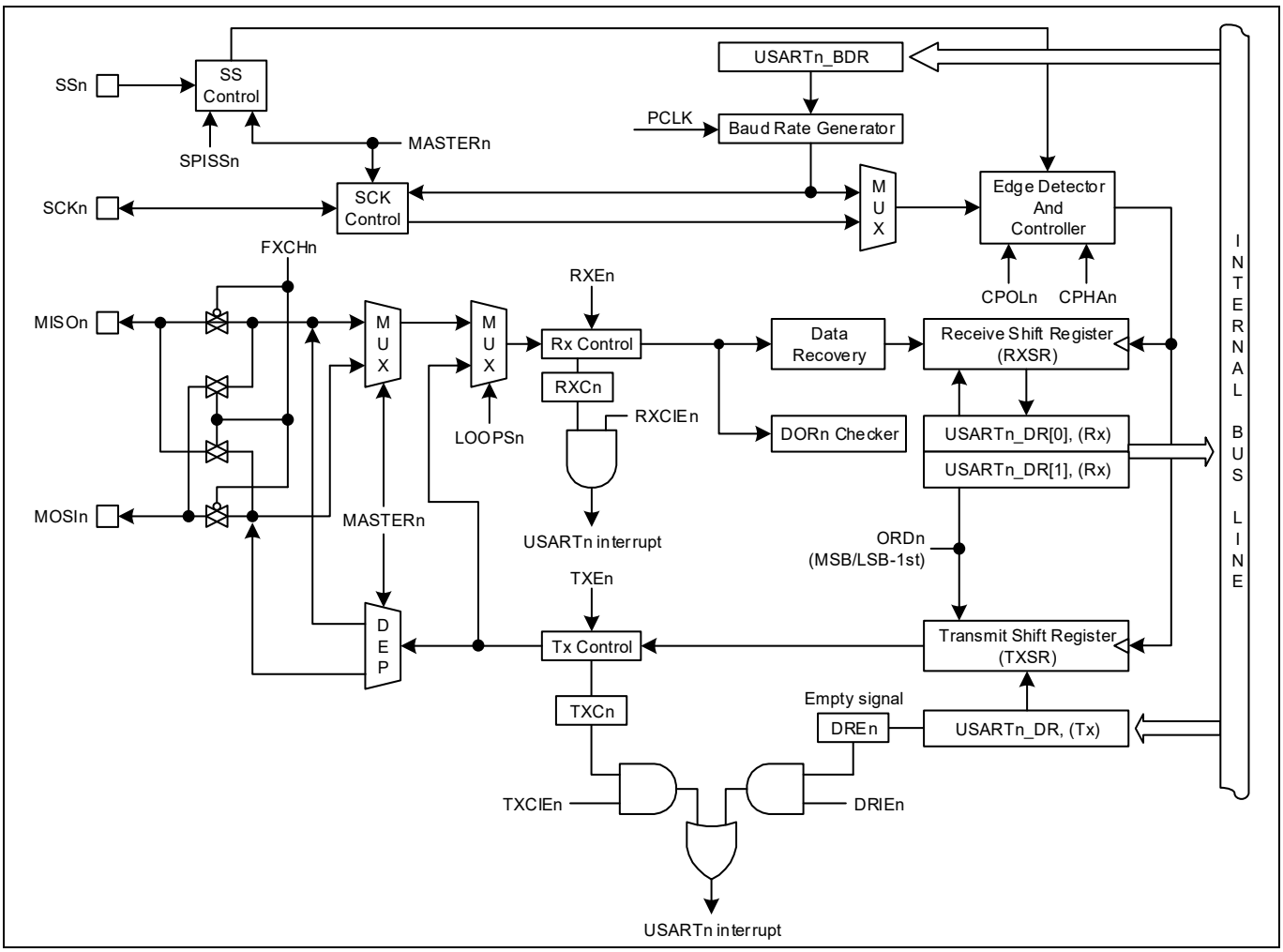


Figure15.2. SPIn Block diagram (Where n = 10, 11, 12, and 13)

15.2 Pin Description

Table 15.1 External pin (n = 10, 11, 12 and 13)

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

CHAPTER 16. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

16.1 OVERVIEW

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

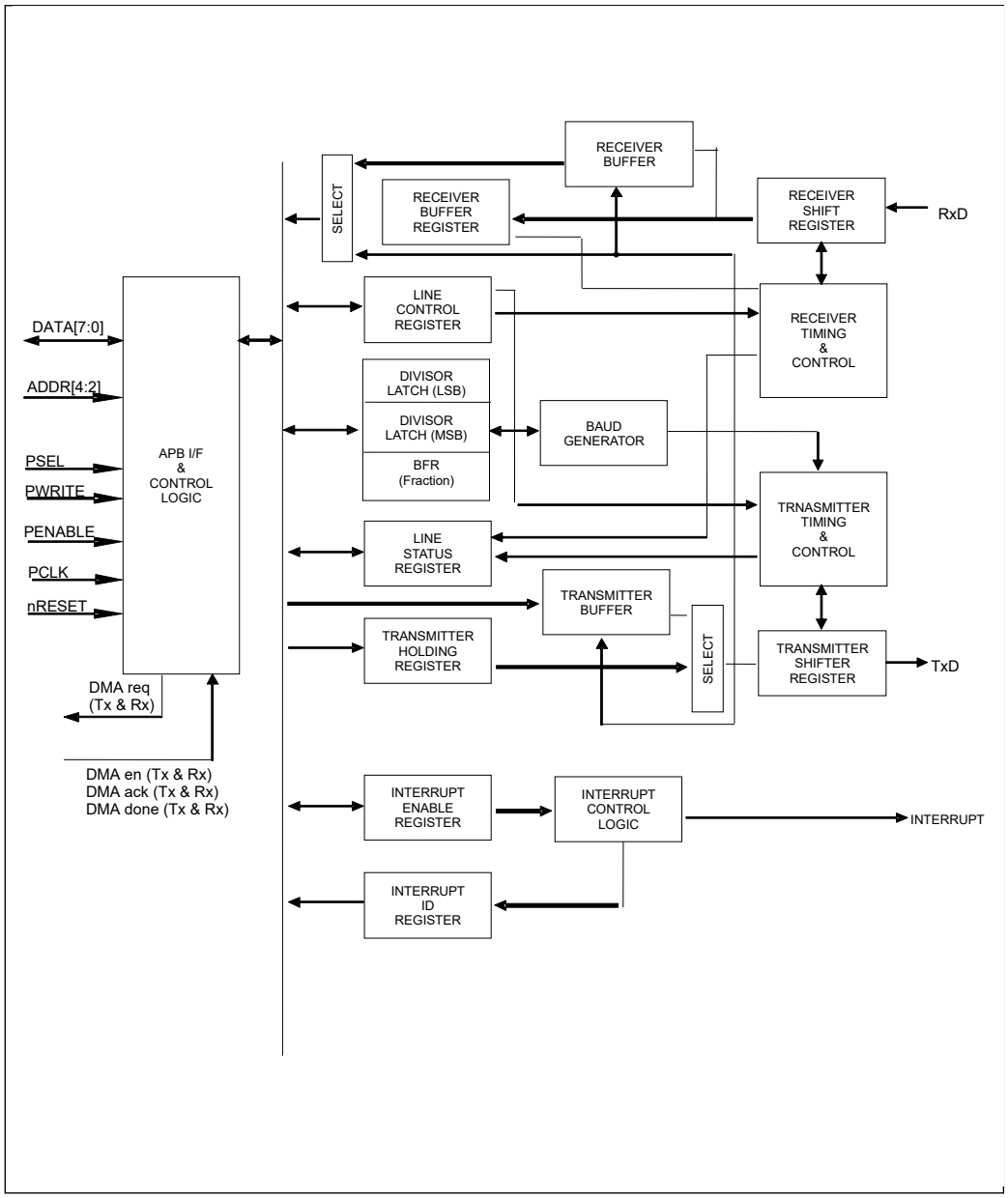


Figure16.1. Block diagram

16.2 Pin Description

Table 16.1 External pin (n = 0, 1)

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel 0 transmit output
RXDn	I	UART Channel 0 receive input

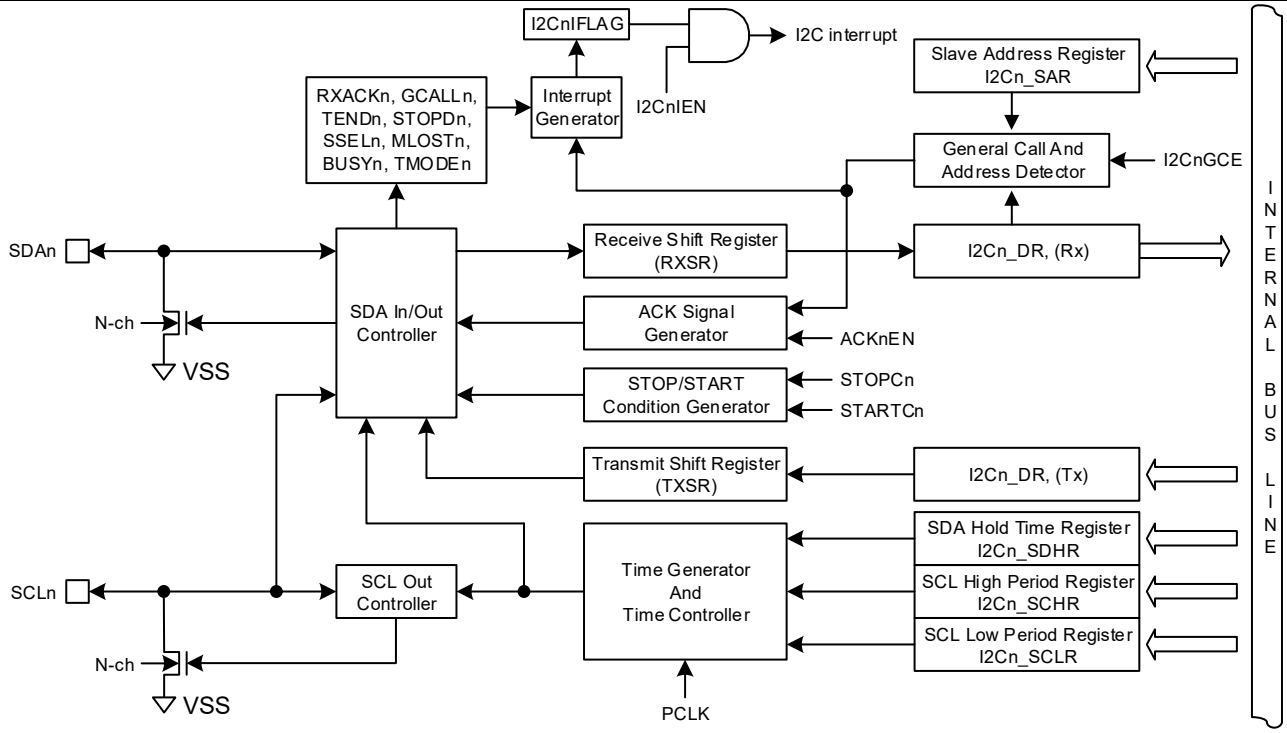
CHAPTER 17. I²C Interface

17.1 OVERVIEW

The I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. The features are as shown below. (n = 0 and 1)

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 400kHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Figure shows the block diagram of a I2C block



Note: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 17.1. I2C Block diagram

17.2 Pin Description

Table 17.1 External pin (n = 0, 1, 2)

PIN NAME	TYPE	DESCRIPTION
SCL0(PF6)	I/O	I2C channel 0 Serial clock bus line (open-drain)
SDA0(PF7)	I/O	I2C channel 0 Serial data bus line (open-drain)
SCLn	I/O	I2C channel n Serial clock bus line
SDAn	I/O	I2C channel n Serial data bus line

CHAPTER 18. 12-BIT A/D CONVERTER

18.1 OVERVIEW

The analog-to-digital converter (A/D) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has eleven analog inputs.The output of the multiplexer is the input into the converter which generates the result through successive approximation. The A/D module has three registers which are the A/D converter control register (ADC_CR), A/D converter data register (ADC_DR), and A/D converter prescaler data register (ADC_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC_DR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC_DR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

- 14 channels of analog inputs
- S/W (ADST) and Timer trigger (TIMER10/TIMER11/TIMER12 A match, ADC trigger signal from TIMER30) support
- Conversion time : 34 clock
- 6-bit Prescaler

Figure shows the block diagram of a A/D converter block.

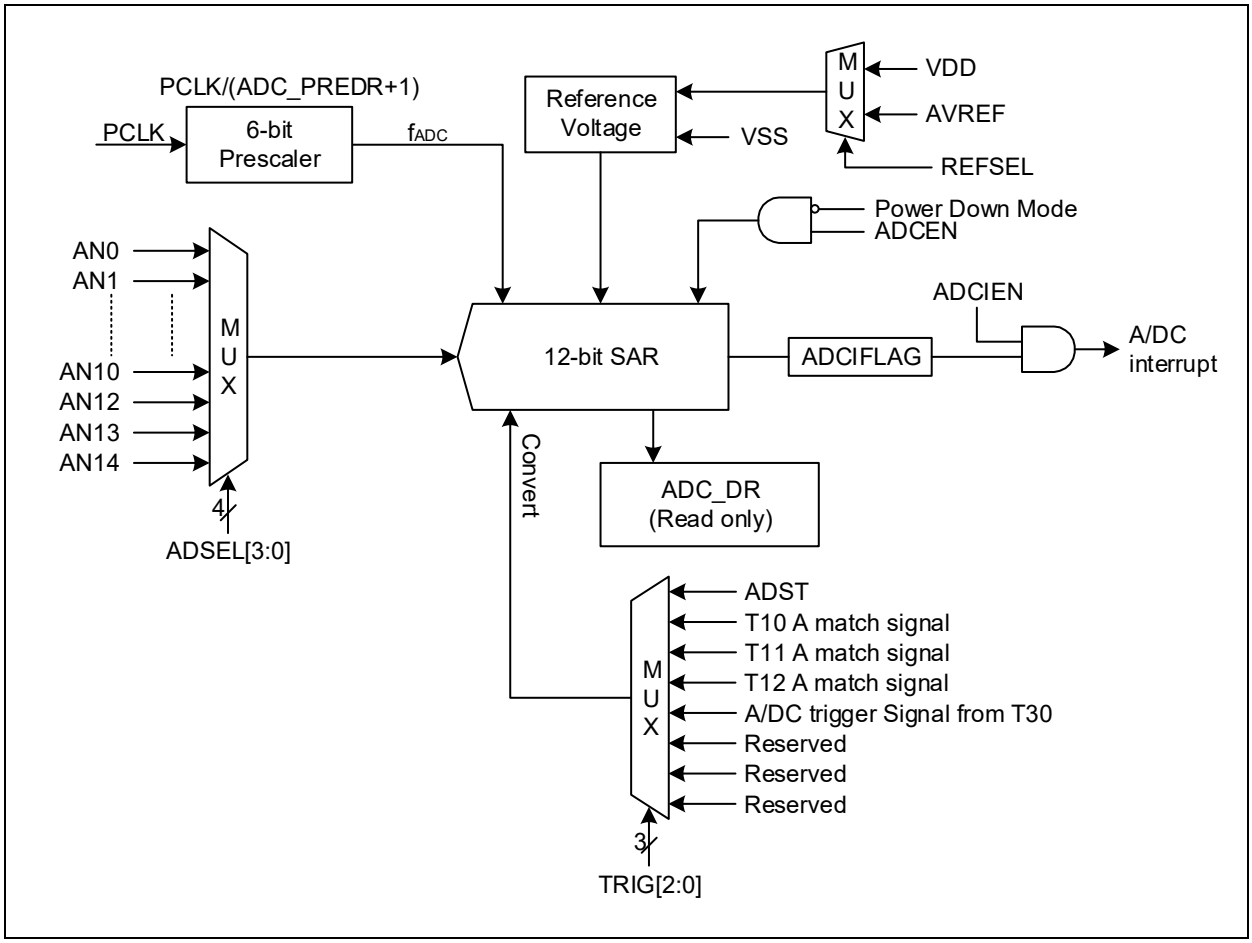


Figure 18.1. Block Diagram

18.2 Pin Description

Table 18.1 External pin

PIN NAME	TYPE	DESCRIPTION
VDD	P	Digital Power
VSS	P	Digital GND
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14

CHAPTER 19. ADPCM

19.1 OVERVIEW

The fine ADPCM decoder has the decoder block to play voice promt and the interface block to read data of a serial flash memory. The fine ADPCM has eighteen registers which are the decoder control register (ADPCM_DECCR), decoder FIFO register (ADPCM_DFIFOR), decoder sampling frequency data register (ADPCM_DECDR), decoder bundle register (ADPCM_DBDLR), decoder result output high/low register (ADPCM_DODRH/L), voice prompt control register (ADPCM_VPCR), serial flash dummy and data number register (ADPCM_SFDDNO), serial flash command register (ADPCM_SFCMD), voice prompt address register 1/2/3 (ADPCM_VPADDR1/2/3), voice prompt size register 1/2/3 (ADPCM_VPSIZE1/2/3) and voice prompt inform register 1/2 (ADPCM_VPINF1/2).

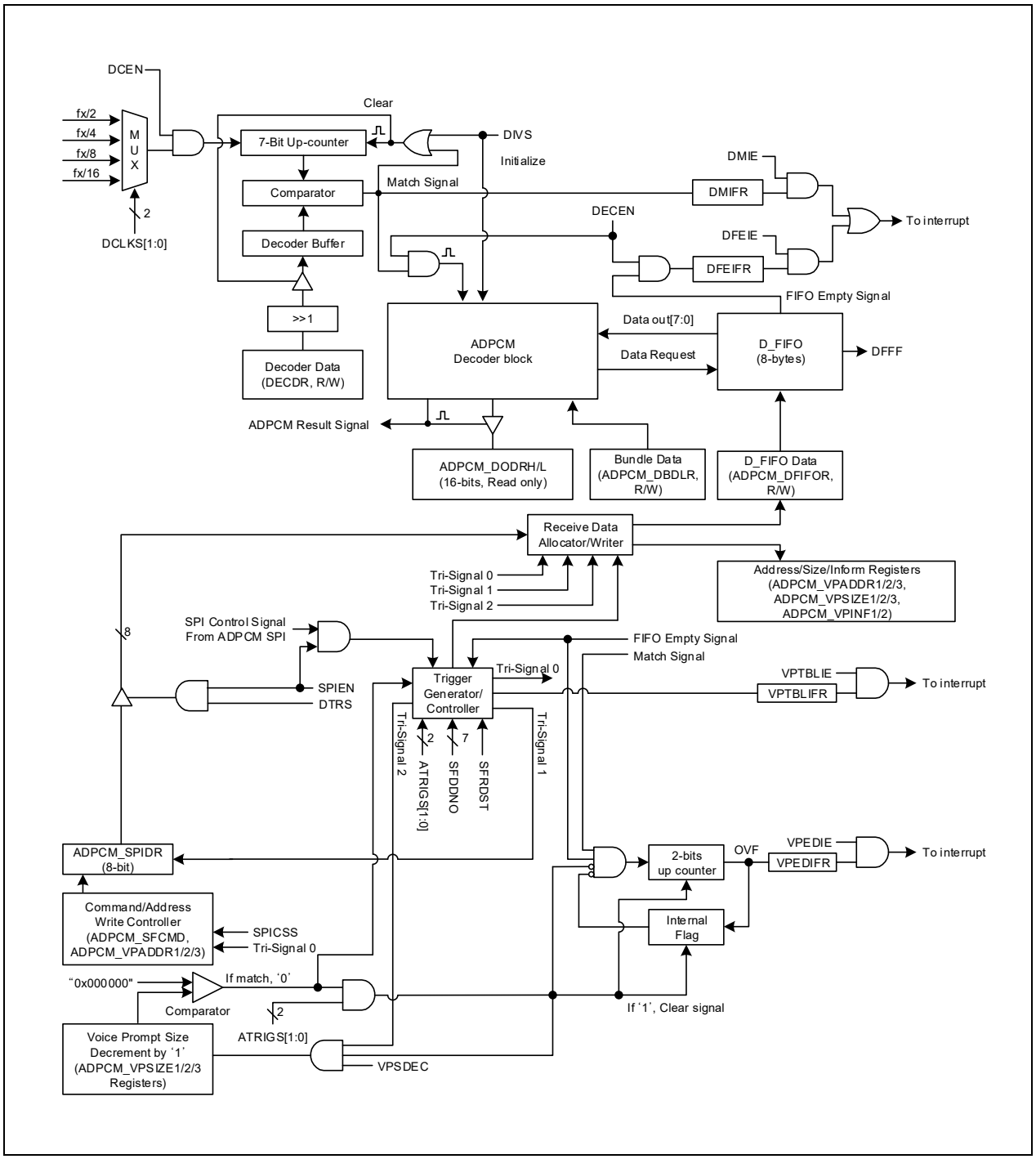


Figure 19.1. Block Diagram

CHAPTER 20. COMPARATOR

20.1 OVERVIEW

The Comparator compares one analogue voltage level with External reference voltage, or internal reference voltage, or DAC output voltage.

The Comparator has following features:

- 2 Comparators
- Internal BGR reference for comparator
- Comparator output de-bounce function
- Level and edge interrupt mode support for comparator

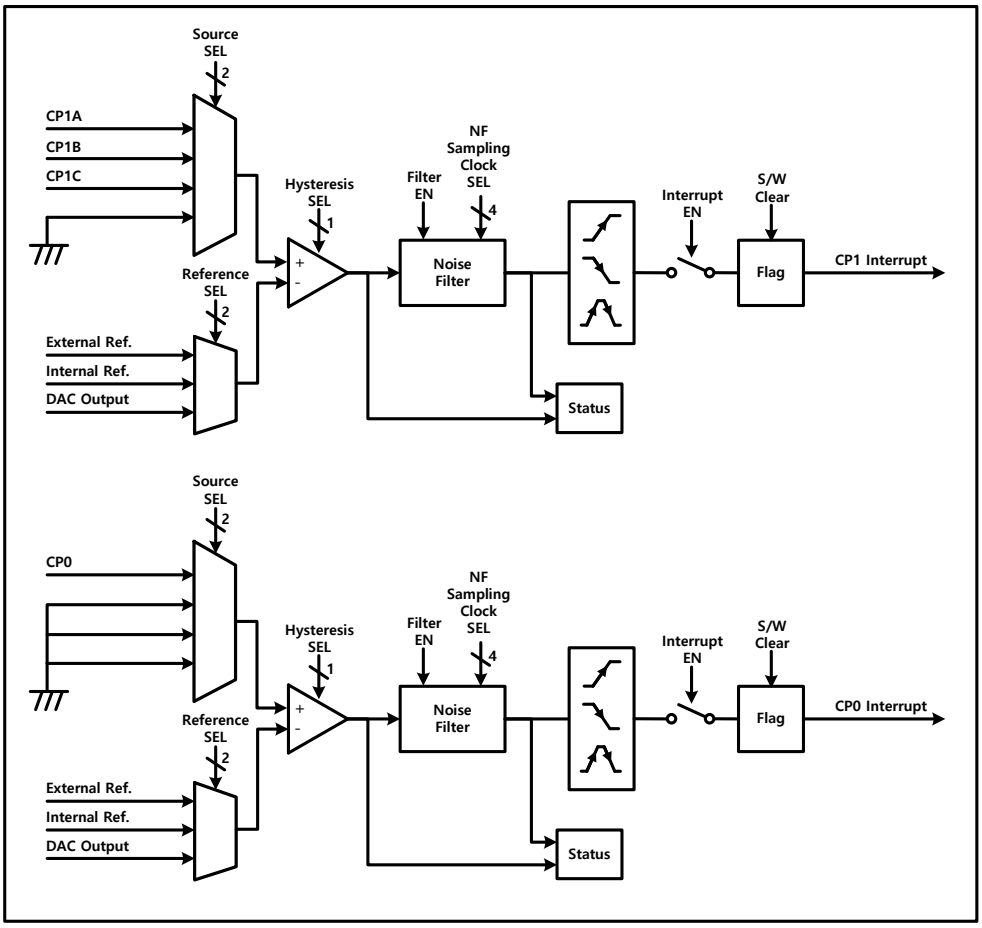


Figure 20.1. Block Diagram

20.2 Pin Description

Table 20.1 External pin

PIN NAME	TYPE	DESCRIPTION
CP0	A	Comparator input 0
CREF0	A	Comparator 0 Reference
CP1A	A	Comparator input 1A
CP1B	A	Comparator input 1B
CP1C	A	Comparator input 1C
CREF1	A	Comparator 1 Reference

CHAPTER 21. TOUCH

21.1 OVERVIEW

Capacitive touch sensor systems are typical human machine interfaces (HMI) which operate by detecting changes in electrostatic capacitance produced by the touch of a finger or other conductor.

The use of capacitive touch technology can easily improve reliability in product design, and enhance the end-user experience. It also enables manufacturing costs to be lowered in a wide range of fields such as household appliances (white goods), healthcare devices, and other electric and electronic equipment.

- . Self-Capacitive Touch Key Sensor.
- . Total 24-channel Touch Key Support.
- . 16-bits Sensing Resolutions.
- . Fast Initial Self Calibration.
- . Key Detection Mode : Single/Multi-Mode.
- . The Improvement of the SNR by Bias-Calibration in Analog Sensing Block

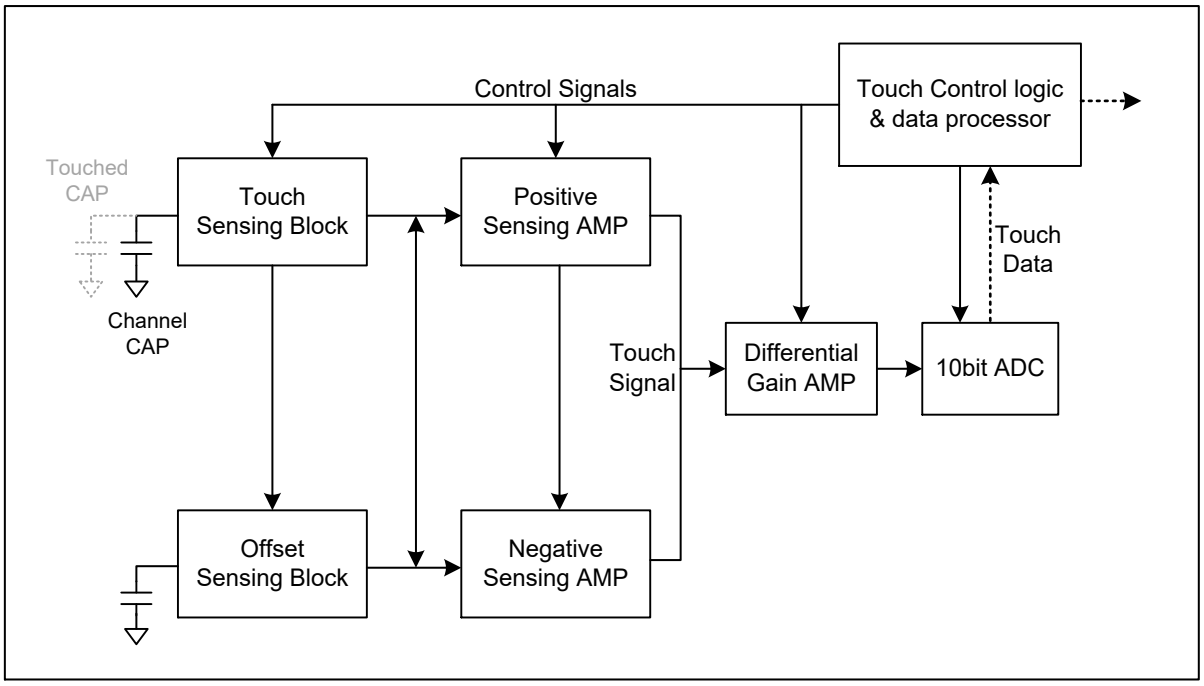


Figure 21.1 Block Diagram

21.2 Pin Description

Table 21.1 External pin

PIN NAME	TYPE	DESCRIPTION
CS0 ~ CS23	IA	Capacitive Touch switch input

CHAPTER 22. LCD DRIVER

22.1 OVERVIEW

The LCD driver is controlled by the LCD control register (LCD_CR) and LCD driver bias and contrast control register (LCD_BCCR). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCD_CR and LCD_BCCR values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCD_CR register data value is rewritten. So, don't rewrite LCD_CR frequently.

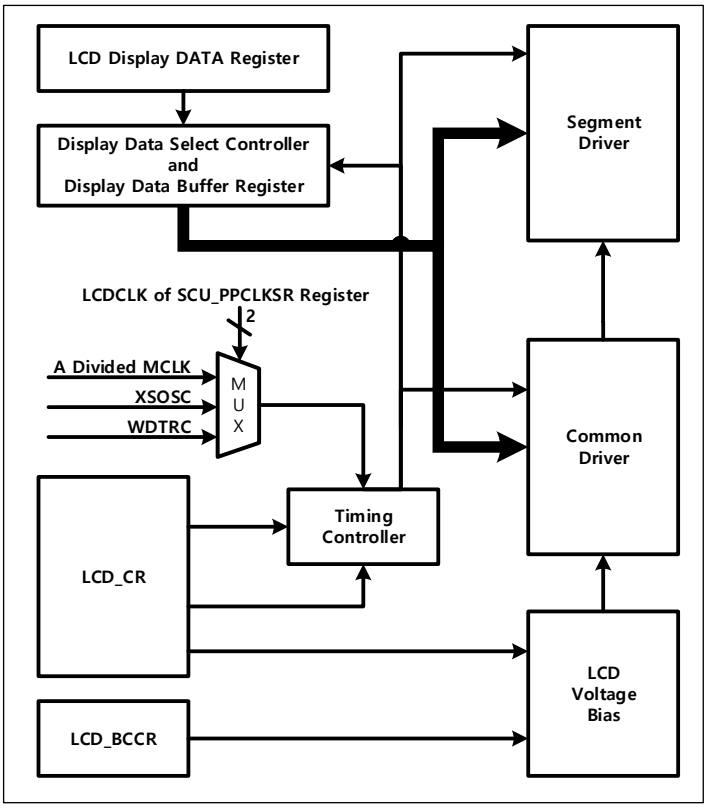


Figure 22.1 Block Diagram

22.2 Pin description

Table 22.1 LCD Driver External Signals

PIN NAME	TYPE	DESCRIPTION
VLC0~3	A	LCD External Bias volatage input
COM0 ~ 7	O	LCD common signal outputs
SEG0 ~ SEG43	O	LCD segment signal outputs

CHAPTER 23. LED DRIVER

23.1 OVERVIEW

LED drive contains a 27 ICOM X 11 ISEG output pin. It is also shared with Touch pin.
By setting LED CONTROL REGISTER1, there are two mode that can be shared with touch function.
The controller consists of display data RAM memory, COM and SEG generator.
ICOM0-ICOM26 and ISEG0-ISEG11 pin can also be used as I / O pins. COMOE1, COMOE2, COMOE3, COMOE4 and SEGOE1,SEGOE2 registers are used to select ISEG0-10, ICOM0 – ICOM26.
During the power-on reset , reset pin, low voltage reset or watchdog reset , LED is turned off

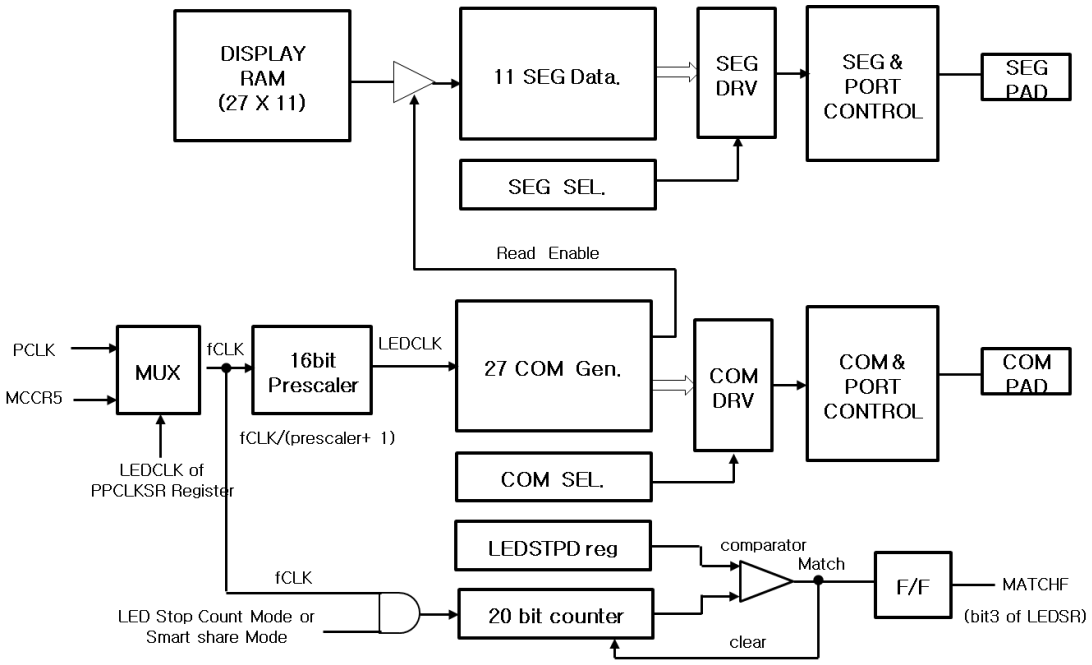


Figure 23.1. Block Diagram

23.2 Pin Description

Table 23.1 External pin

PIN NAME	TYPE	DESCRIPTION
ICOM0 ~ ICOM27	O	LED common signal outputs
ISEG0 ~ ISEG10	O	LED segment signal outputs
R-SET	A	LED Segment current setting

NOTE) For using the LED block, Resistor of 4.7 kOhm must be in between R-set and GND.

CHAPTER 24. CYCLIC REDUNDANCY CHECK AND CHECKSUM

24.1 OVERVIEW

The CRC (cyclic redundancy check) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. The CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

The CRC generator has following features:

- Auto CRC and User CRC Mode.
- Polynomial : CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$), CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC Mode and Checksum Mode.

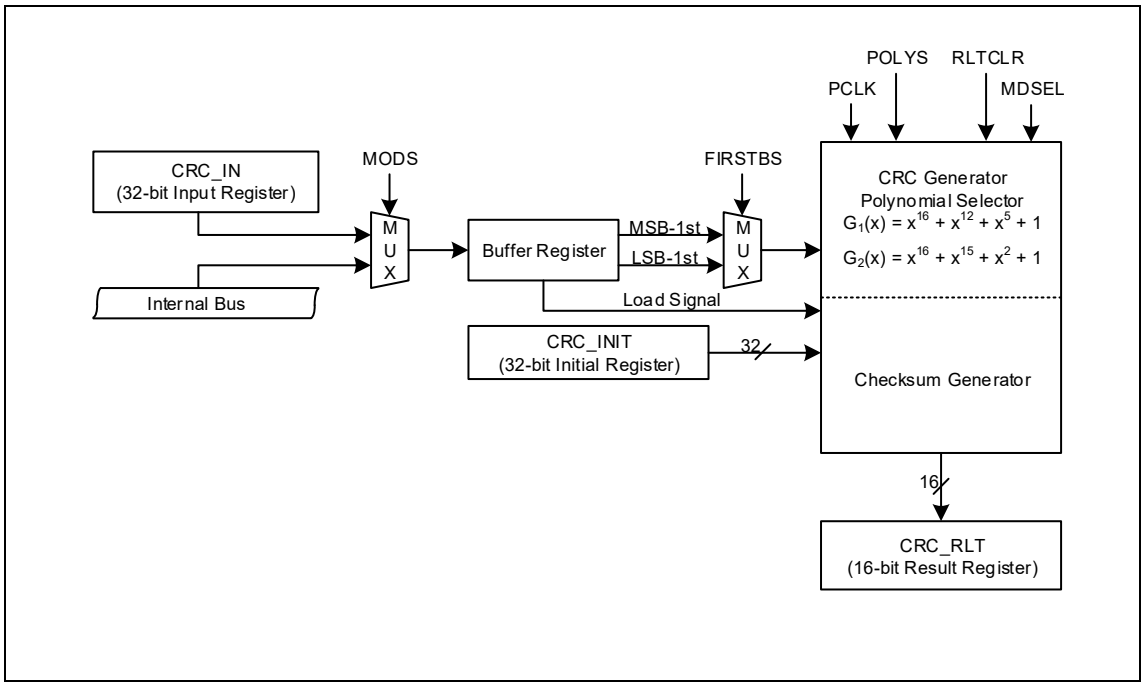


Figure 24.1 Block Diagram

CHAPTER 25. Electrical Characteristics

25.1 DC Characteristics

25.1.1 ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 25.1 Absolute maximum rating

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	–
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	5	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	40	mA	Maximum current (ΣI_{OH})
	I_{OL}	10	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	80	mA	Maximum current (ΣI_{OL})
Total Power Dissipation	T_P	300	mW	–
Storage Temperature	T_{STG}	-45 – +125	°C	–

25.1.2 RECOMMENDED OPERATING CONDITIONS

Table 25.2 Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD	-	1.8	-	5.5	V
		Touch	2.7	-	5.5	V
		LED	3.3	-	5.5	V
Operating Frequency	FREQ	MOSC	4	-	16	MHz
		SOSC	-	32.768	-	kHz
		HSI	46.32	48	49.68	MHz
		LSI	400	500	600	kHz
Operating Temperature	Top	Top	-40	-	+85	℃

25.1.3 A/D CONVERTER CHARACTERISTICS

Table 25.3 ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AVDD		2.4	5	5.5	V
Resolution				12		Bit
Operating Current	IDDA	VDD=5.0V		1	2	mA
Analog Input Range	VAN		VSS		AVREF	V
Conversion Rate	fCON			-	150	kSPS
Operating Frequency	ACLK				4.5	MHz
Integral Non-Linearity	INL	AVDD=2.4V < AVDD < 5.5V, T_A = 25 °C		±4	±10	LSB
Differential Non-Linearity	DNL			±1	±4	LSB
Top Offset Error(FSE)	TOE			±6	±12	LSB
Zero Offset Error	ZOE			±4	±8	LSB

25.1.4 POWER ON RESET CHARACTERISTICS

Table 25.4 POR Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Current	I_{DD}	–	-	60	-	uA
POR Set Level	V_{set}	–	1.05	1.2	1.35	V
POR Reset Level	V_{reset}	–	1.0	1.1	1.2	V

25.1.5 LOW VOLTAGE RESET CHARACTERISTICS

Table 25.5 Low Voltage Reset Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V_{LVR}	T_A = – 40 °C to + 85 °C, Falling Voltage (error rate 5%)		1.60		V
				1.69		
				1.78		
				1.90		
				1.99		
				2.12		
				2.30		
				2.47		
				2.67		
				3.04		
				3.18		
				3.59		
				3.72		
				4.03		
				4.20		
				4.48		
Hysteresis	-		-	100	200	mV
Noise cancelling time	-		-	2	-	us
Operation Current	I_{DD}		-	3.5	5	uA
Operation Current(STOP)	$I_{DD, STOP}$		-	2.5	3	nA

25.1.6 LOW VOLTAG INDICATOR CHARATERISTICS

Table 25.6 Low Voltage Indicator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V_{LVI}	T_A = – 20 °C to + 85 °C, Falling Voltage (error rate 5%)		1.60		V
				1.69		
				1.78		
				1.90		
				1.99		
				2.12		
				2.30		
				2.47		
				2.67		
				3.04		
				3.18		
				3.59		
				3.72		
				4.03		
				4.20		
				4.48		
Hysteresis	-		-	100	200	mV
Noise cancelling time	-		-	2	-	Us
Operation Current	I_{DD}		-	3.5	5	uA
Operation Current(STOP)	$I_{DD, STOP}$		-	2.5	3	nA

25.1.7 HIGH FREQUENCY INTERNAL RC OSCILLATOR CHARACTERISTICS

Table 25.7 High Frequency Internal RC Oscillator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HSI}	VDD = 1.8V to 5.5V	–	48	–	MHz
Tolerance		T_A = – 40 °C to + 85 °C	–	–	±3.5	%
Clock Duty Ratio	T_{OD}	–	–	50	–	%
Stabilization Time	t_{HFS}	–	–	–	100	us
IRC Current	I_{HSI}	Enable	–	190	–	uA
		Disable	–	1	–	uA

25.1.8 LOW FREQUENCY INTERNAL RC OSCILLATOR CHARACTERISTICS

Table 25.8 Low Frequency Internal RC Oscillator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{LIRC}	VDD = 1.8V to 5.5V	400	500	600	kHz
IRC Current	I_{LIRC}	Enable	–	1.5	2	uA
		Disable	–	1	20	nA

25.1.9 LCD VOLTAGE CHARACTERISTICS

Table 25.9 LCD Voltage Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD Voltage	VLC0	LCD contrast disabled, 1/4 bias					V
		LCD contrast enabled, 1/4 bias, No Panel load	VLCD[3:0]=00H	Typx0.94	VDDx16/31	Typx1.06	V
			VLCD[3:0]=01H		VDDx16/30		
			VLCD[3:0]=02H		VDDx16/29		
			VLCD[3:0]=03H		VDDx16/28		
			VLCD[3:0]=04H		VDDx16/27		
			VLCD[3:0]=05H		VDDx16/26		
			VLCD[3:0]=06H		VDDx16/25		
			VLCD[3:0]=07H		VDDx16/24		
			VLCD[3:0]=08H		VDDx16/23		
			VLCD[3:0]=09H		VDDx16/22		
			VLCD[3:0]=0AH		VDDx16/21		
			VLCD[3:0]=0BH		VDDx16/20		
			VLCD[3:0]=0CH		VDDx16/19		
			VLCD[3:0]=0DH		VDDx16/18		
			VLCD[3:0]=0EH		VDDx16/17		
			VLCD[3:0]=0FH		VDDx16/16		
LCD Mid Bias Voltage(note)	VLC1	VDD = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load		Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2			Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3			Typ-0.2	1/4xVLC0	Typ+0.2	
LCD Driver Output Impedance	R_{LO}	VLCD=3V		–	5	10	kΩ
LCD Bias Dividing Resistor	RLCD1	1/4 bias, T_A = 25°C		7.5	10	12.5	kΩ
	RLCD2			38	50	62	
	RLCD3			60	80	100	
	RLCD4			180	240	300	

Note)

1. It is middle output voltage when the VDD and the VLC0 node are connected.

25.1.10 TOUCH SWITCH CHARACTERISTICS

Table 25.10 Touch Switch Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{DD}	–	2.7	-	5.5	V
	V_{DDA}	–	2.7	-	5.5	V
VDC Voltage	V_{CCL}	From MCU	–	1.9	–	V
SNR(Signal-toNoise Ratio)	SNR	–	–	20	–	dB
Self-Calibration Time	T_{CAL}	–	–	10	–	ms
Scan Speed	T_{SCAN}	–	–	10	–	ms
Supply Current	I_{DD}	–	–	1	–	mA
Operation Temperature	T_{OPER}	–	-40	–	+85	℃

25.1.11 LED DRIVER CHARACTERISTICS

Table 25.11 LED Driver Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Operating Voltage	V_{Ddext}			3.3	–	5.5	V
Operating Temperature	T_A			-40	25	85	℃
COM output leakage	I_{CLKG}			-1		1	uA
SEG output leakage	I_{SLKG}			-1		1	uA
SEG Current Matching (I_{SEG}-I_{SEGAVR}) / I_{SEGAVR}	ITOSEG			-6	+/-1.5	6	%
SEG Current	I_{SEG}	@ RSET value (4.7kΩ)	V_{DDEXT} = 3.3V V_{OH_LED} = 3.05V	2.1	–	–	mA
			V_{DDEXT} = 5 V V_{OH_LED} = 3.73V	3.3[NOTE1)]	–	–	
COM Current	I_{COM}	V_{OL_LED} = 0.3V		23.1	–	–	mA

NOTE

1) V_{ddext} 3.3V is a worst case and proved by experiment. However, in case of V_{ddext} 5V condition, it is the value measured in simulation.

2) At minimum current conditions, The difference voltage between SEG and COM is 2.7V at least .

25.1.12 DC ELECTRICAL CHARACTERISTICS

Table 25.12 DC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins, nRESET	0.8VDD	-	VDD	V
	V_{IH2}	PF5,PF6,PF7 are input 1.8V level	0.9	-	VDD	
Input Low Voltage	V_{IL1}	All input pins, nRESET	0	-	0.2VDD	V
	V_{IL2}	PF5,PF6,PF7 are input 1.8V level	0	-	0.6	
Output High Voltage	V_{OH1}	VDD=5V, I_{OH1} = – 2.36mA PA0, PA1, PA2, PA3, PA4, PA5, PF0	0.8VDD	-	VDD	V
	V_{OH2}	VDD=5V, I_{OH2} = – 4.38mA PA6, PA7	0.8VDD	-	VDD	
	V_{OH3}	VDD=5V, I_{OH3} = – 4.38mA PB0, PB1	0.8VDD	-	VDD	
	V_{OH4}	VDD=5V, I_{OH4} = – 4.1mA PB2, PB3, PB4, PB5, PB6, PB7, PC0, PC1, PC2, PC3, PC4, PD0, PD1, PD2, PD3, PD4, PD5	0.8VDD	-	VDD	
	V_{OH5}	VDD=5V, I_{OH5} = – 10.9mA PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	0.8VDD	-	VDD	
	V_{OH6}	VDD=5V, I_{OH6} = – 2.93mA PA9, PA10, PA11, PF1, PF2, PF3, PF4, PF8, PF9, PF10, PF11, PE8, PE9, PE10, PE11, PE12, PE13	0.8VDD	-	VDD	
	V_{OH7}	VDD=5V, I_{OH7} = – 4.1mA PB8, PB9, PB10, PB11, PB12, PB13, PB14, PB15, PC5, PC6, PC7, PC8, PC9, PC10, PC11, PC12, PE15, PE14	0.8VDD	-	VDD	
Output Low Voltage	V_{OL1}	VDD=5V, I_{OL1} = 4.86mA PA0, PA1, PA2, PA3, PA4, PA5, PF0, PF5, PF6, PF7	0	-	0.2VDD	V
	V_{OL2}	VDD=5V, I_{OL2} = 19.1mA PA6, PA7	0	-	0.2VDD	
	V_{OL3}	VDD=5V, I_{OL3} = 19.1mA PB0, PB1	0	-	0.2VDD	
	V_{OL4}	VDD=5V, I_{OL4} = 19.1mA PB2, PB3, PB4, PB5, PB6, PB7, PC0, PC1, PC2, PC3, PC4, PD0, PD1, PD2, PD3, PD4, PD5	0	-	0.2VDD	
	V_{OL5}	VDD=5V, I_{OL5} = 19.1mA PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	0	-	0.2VDD	

	V_{OL6}	VDD=5V, I_{OL6} = 4.86mA PA9, PA10, PA11, PF1, PF2, PF3, PF4, PF8, PF9, PF10, PF11, PE8, PE9, PE10, PE11, PE12, PE13	0	-	0.2VDD	
	V_{OL7}	VDD=5V, I_{OL7} = 19.1mA PB8, PB9, PB10, PB11, PB12, PB13, PB14, PB15, PC5, PC6, PC7, PC8, PC9, PC10, PC11, PC12, PE15, PE14	0	-	0.2VDD	
Input high leakage current	I_{IH}	All Input ports	-4	-	-	uA
Input low leakage current	I_{IL}	All Input ports	-	-	+4	uA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, All Input ports	40	-	70	kΩ
		V_I=0V, T_A=25°C, nRESET PIN		250		
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, All Input ports	40	-	70	kΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=3.3V		1		MΩ

25.1.13 SUPPLY CURRENT CHARACTERISTICS

Table 25.13 Supply Current Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions		Typ	Max	Units
Supply Current	I_{DD1} (Run)	f_{XIN} = 8MHz	VDD=5V±10%	4.0	12.0	mA
		f_{HSI} = 48MHz		10.0	30.0	
		f_{HSI} = 12MHz		3.5	10.0	
		f_{LSI} = 500kHz		200	600	uA
		f_{SOSC} = 32.768kHz		140	300	
	I_{DD2} (Sleep)	f_{XIN} = 8MHz		5	15	mA
		f_{HSI} = 48MHz		6	18	
		f_{HSI} = 12MHz		2	6	
		f_{LSI} = 500kHz		180	500	uA
		f_{SOSC} = 32.768kHz		130	400	
	I_{DD3} (Deep Sleep)	WDT(WDTRC) = ON, LVD = ON T_A = 25 °C		17	-	uA
	I_{DD4} (Deep Sleep)	WDT(WDTRC) = ON, LVD = OFF NOTE3 T_A = 25 °C		15	-	
	I_{DD5} (Deep Sleep)	WDT(WDTRC) = OFF, LVD = ON, T_A = 25 °C		4	-	uA
	I_{DD6} (Deep Sleep)	WDT(WDTRC) = OFF, LVD = OFF NOTE3, T_A = 25 °C		2	-	

Notes)

1. All supply current items don't include the current of an low frequency internal RC oscillator and a peripheral block.
2. All supply current items include the current of the power-on reset (POR) block.
3. LVD = OFF indicates that LVR reset function , LVR block and LVI block are disabled.
   SCU_RSER<LVDRST> = 0
   SCULV_LVRCR<LVREN> = 0x55
   SCULV_LVICR< LVIEN> = 0

25.1.14 USART SPI CHARCTERISTICS

Table 25.14 SPI Characteristics (Temperature: -40 ~ +85℃, VDD = 2.7 – 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Clock Pulse Period	t_{SCK}	Internal SCK source	400	–	–	ns
Input Clock Pulse Period		External SCK source	400	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	180	–	–	
Input Clock High, Low Pulse Width		External SCK source	180	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	200	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	100	
Input Setup Time	t_{DIS}	–	180	–	–	
Input Hold Time	t_{DIH}	–	180	–	–	

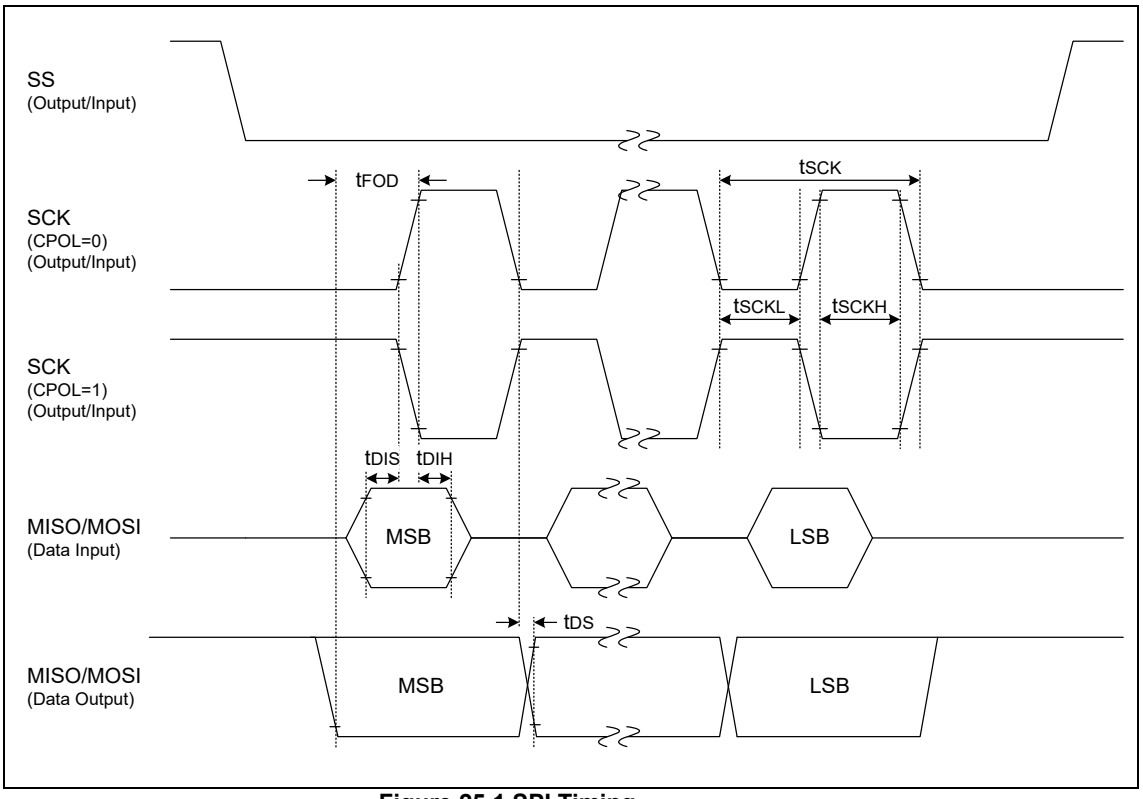


Figure 25.1 SPI Timing

25.1.15 I2C CHARACTERISTICS

Table 25.15 I2C Characteristics (Temperature: -40 ~ +85℃, VDD = 1.8 – 5.5V)

Parameter	Symbol	Min	Max	Units
Clock frequency	t_{SCL}	0	400	kHz
Clock High Pulse Width	t_{SCLH}	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	1.3	–	
Bus Free Time	t_{BF}	1.3	–	
Start Condition Setup Time	t_{STSU}	0.6	–	
Start Condition Hold Time	t_{STHD}	0.6	–	
Stop Condition Setup Time	t_{SPSU}	0.6	–	
Stop Condition Hold Time	t_{SPHD}	0.6	–	
Output Valid from Clock	t_{VD}	0	–	
Data Input Hold Time	t_{DIH}	0	1.0	
Data Input Setup Time	t_{DIS}	100	–	ns

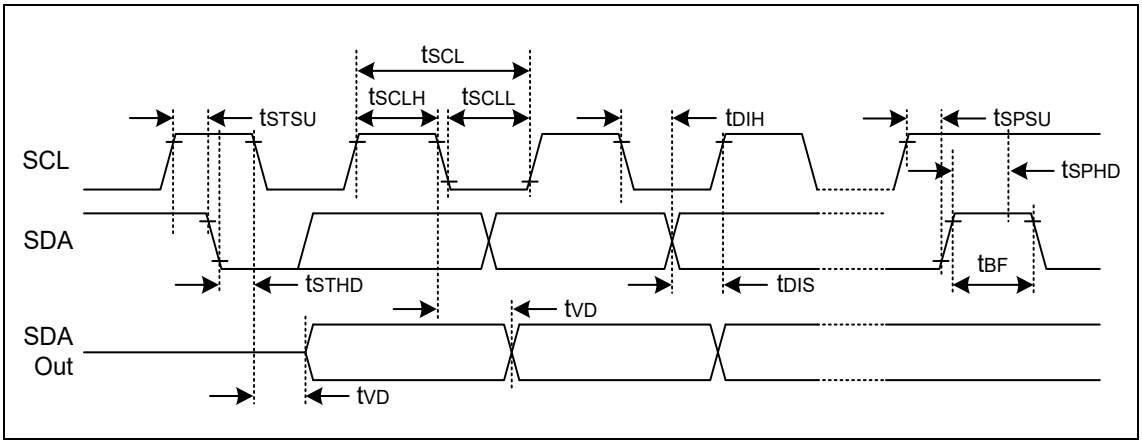


Figure 25.2 I2C Timing

25.1.16 USART UART TIMING CHARACTERISTICS

Table 25.16 UART Timing Characteristics (Temperature: -40 ~ +85℃, VDD = 1.8 – 5.5V)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

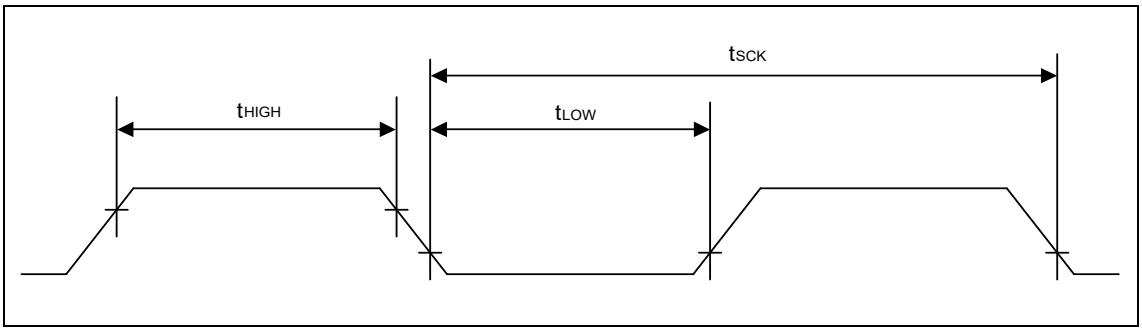


Figure 25.3 Waveform for UART Timing Characteristics

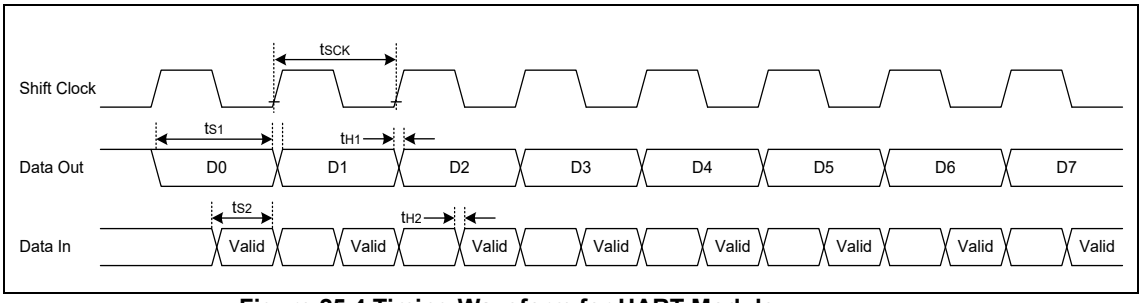


Figure 25.4 Timing Waveform for UART Module

25.1.17 INTERNAL FLASH ROM CHARACTERISTICS

Table 25.1 Internal Flash ROM Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Cycle Time	fRSTBUSY	–	5.6	8	10.4	us
Fuse Program Cycle Time	fFRDBUSY		4.2	6	7.8	
Normal Program Cycle Time	tPGMBUSY		21	30	42	
Normal Page Erase Cycle Time	tPERSBUSY		2.8	4	5.2	ms
Sector Erase Cycle Time	tSERSBUSY		2.8	4	5.2	
Chip Erase Cycle Time	tMERSBUSY	–	5.6	8	10.4	
Flash Program Voltage	V_{PGM}	On erase/write	2.7	–	3.6	V
Endurance of Write/Erase	N_{FWE}	T_A=25 °C, Page unit	10,000	–	–	Times
Retention Time	t_{FRT}		10	–	–	Years

25.1.18 MAIN OSCILLATOR CHARACTERISTICS

Table 25.17 Main Oscillator Characteristics (Temperature: -40 ~ +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	1.8 V – 5.5 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	1.8 V – 5.5 V	2.0	–	16.0	
External load capacitor	C1, C2	1MHz < fout ≤ 4MHz	18	30	35	pF
		4MHz < fout ≤ 12MHz	10	22	30	pF
		12MHz < fout ≤ 16MHz	7	18	22	pF

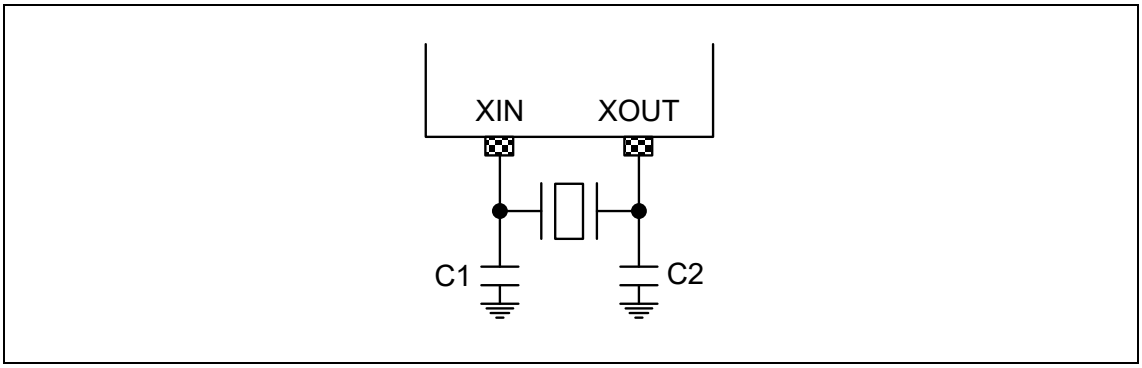


Figure 25.5 Crystal/Ceramic Oscillator

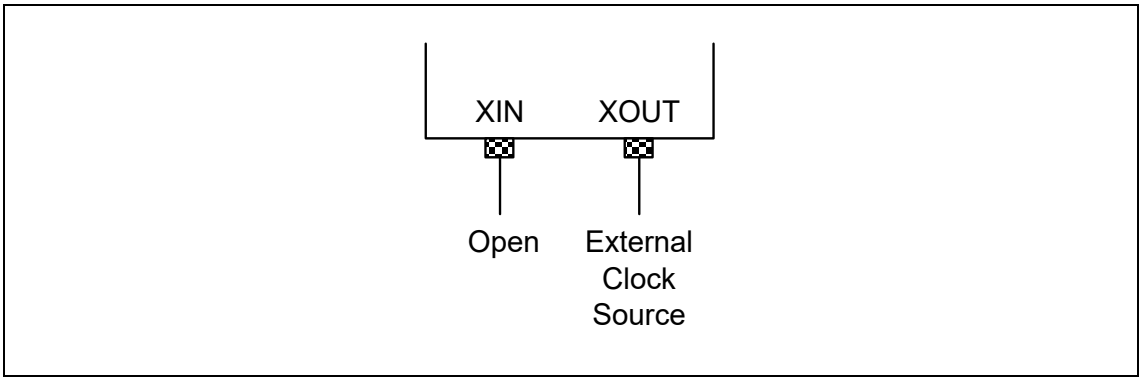


Figure 25.6 External Clock

25.1.19 SUB OSCILLATOR CHARACTERISTICS

Table 25.18 Sub Oscillator Characteristics (Temperature: -40 ~ +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 5.5 V	32	32.768	38	kHz
External load capacitor	C1, C2	1.8 V – 5.5 V	5	15	35	pF

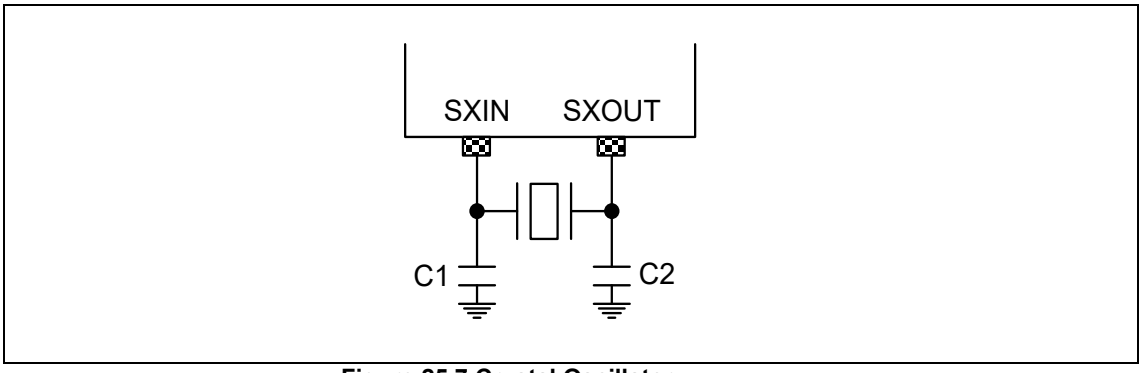


Figure 25.7 Crystal Oscillator

25.1.20 Operating Voltage Range

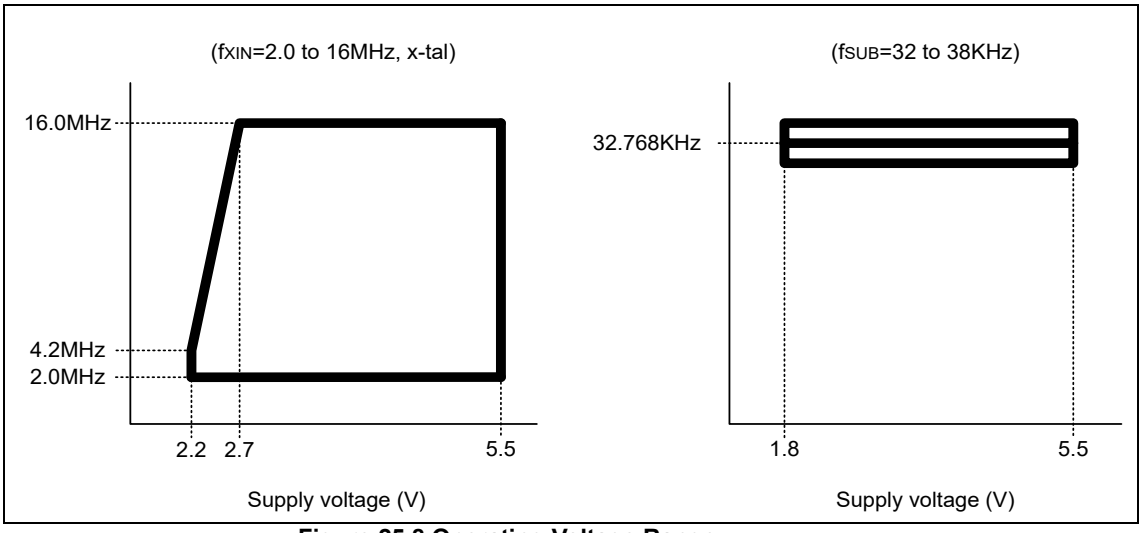


Figure 25.8 Operating Voltage Range

25.1.21 PLL ELECTRICAL CHARACTERISTICS

Table 25.19 PLL Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency	f_{OUT}	–	-	-	48	MHz
Operating Current	I_{DD}	@50MHz	–	-	1	mA
Duty	f_{DUTY}		40	–	60	%
VCO	f_{VCO}		0.8	–	192	MHz
Input Frequency	f_{IN}		2	8	16	MHz
Locking Time	t_{LOCK}				60	us

25.1.22 COMPARATOR CHARACTERISTICS

Table 25.20 Comparator Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	VDDEXT		2.0		5.5	V
Input Offset Voltage	VOS	VDDEDXT=5V, VIN=1/2 VDDEXT, Before Offset Calibration	-	±10	±20	mV
		VDDEDXT=5V, VIN=1/2 VDDEXT, After Offset Calibration			±5	mV
Propagation Delay	$t_{PD}(t_{PHL}, t_{PLH})$	V_{ov} > 10mV	-	0.5	2	us
Comparator Input Voltage	V_{CIN}		GND+50	-	VDDEXT-50	mV
Hysteresis	V_{OS}	VDDEDXT=5V, HYSSEL=0	-	±5	±25	mV
		VDDEDXT=5V, HYSSEL=1		±20	±60	mV
Comparator Current	$IDD_{(RMS)}$	V_{DD} =5V		70	100	uA

25.1.23 D/A CONVERTER CHARACTERISTICS

Table 25.21 D/A Converter Characteristics (Temperature: -40 ~ +85℃, V_{DD}=1.8-5.5V, V_{DD}=DAVREF, V_{ss}=0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution	-	-	-	-	12	Bit
Analog Output Voltage	D_{AOUT}		GND+0.1	-	AV_{DD}-0.1	V
Reference Input Voltage	EXTREF		2.7	-	AV_{DD}	V
Integral Nonlinearity	INL	@AVDD=5V or EXTREF_A=5V	-	-±6	±10	LSB
Differential Nonlinearity	DNL		-	±6	±10	LSB
D/AC Current	I_{DAC}		-	0.6	0.8	mA
Conversion Time	-		-	-	2	Us

CHAPTER 26. Package

26.1 **80LQFP14 Package dimension**

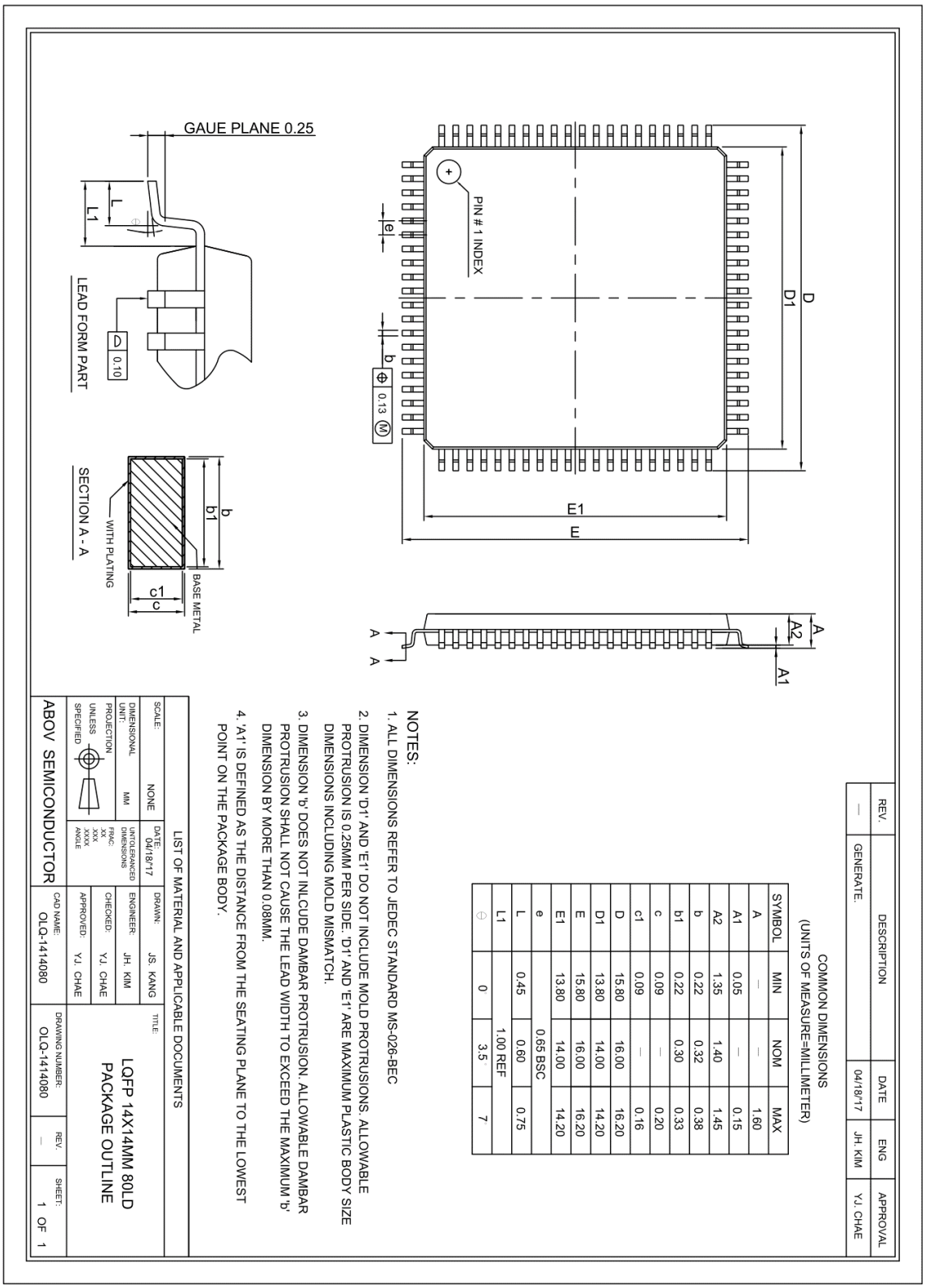


Figure 26.1 Package dimension (80LQFP14)

26.2 **80LQFP12 Package dimension**

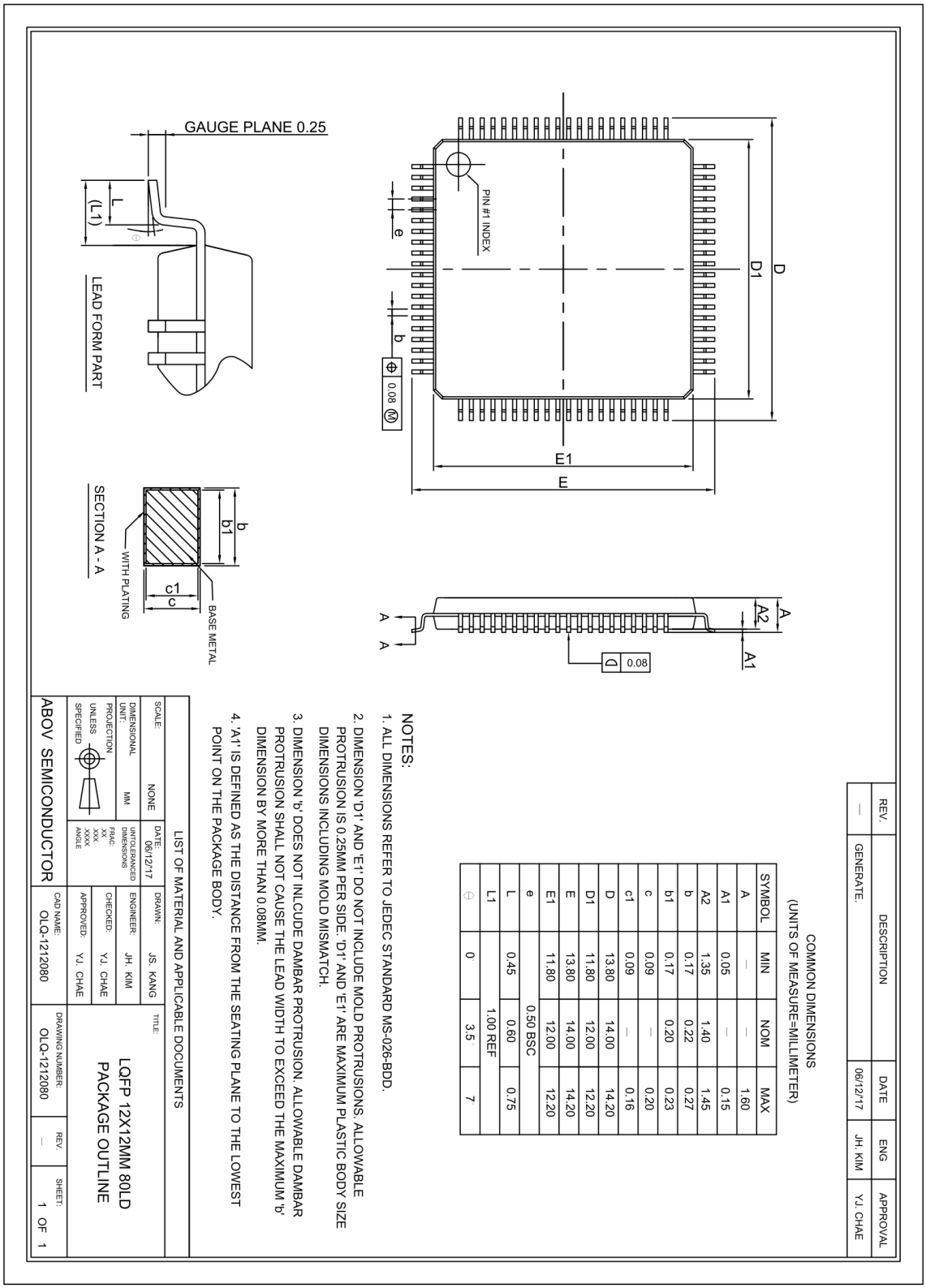
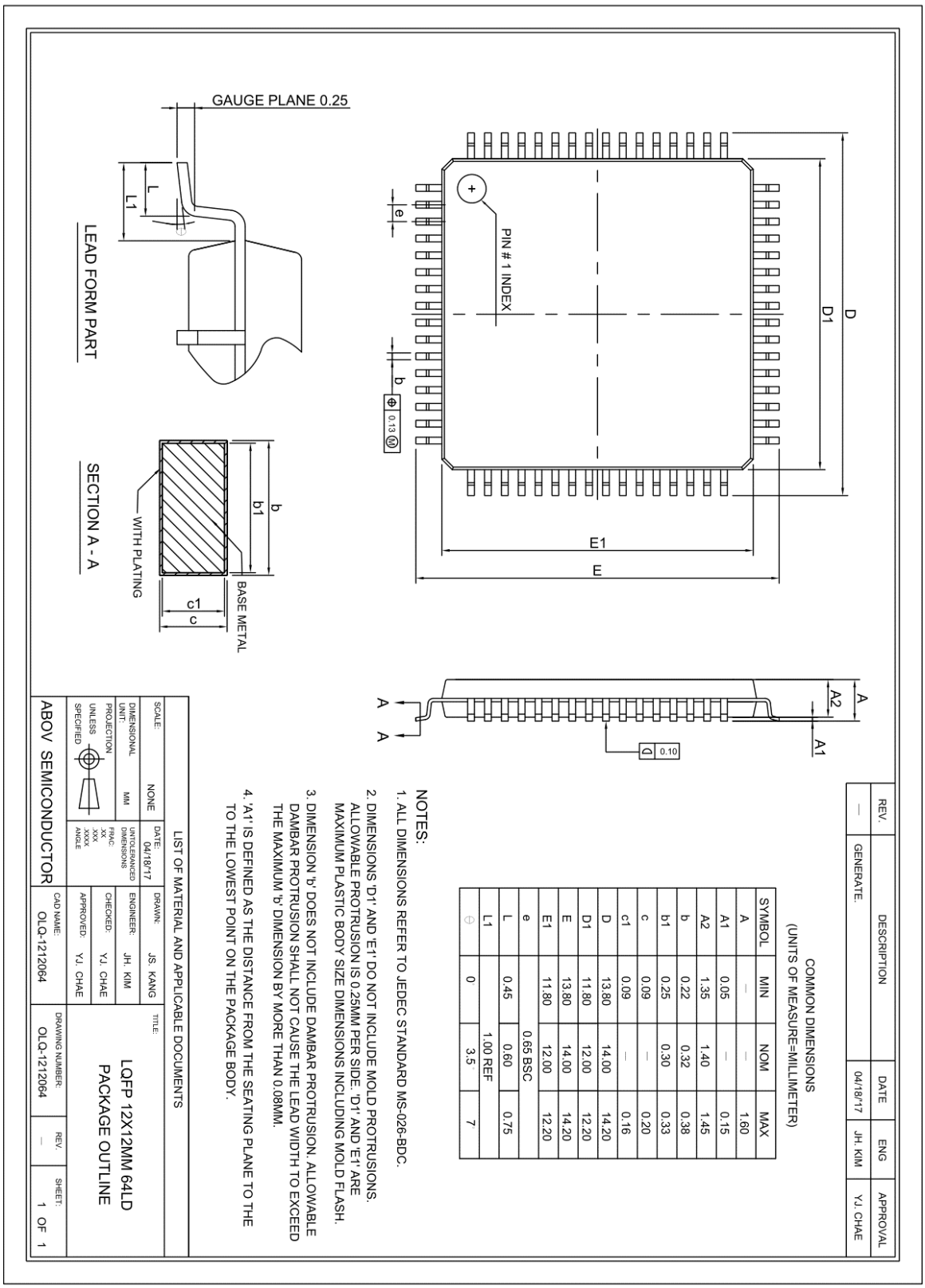


Figure 26.2 Package dimension (80LQFP12)

26.3 64LQFP12 Package dimension



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.25	0.30	0.33
c	0.09	—	0.20
c1	0.09	—	0.16
D	13.80	14.00	14.20
D1	11.80	12.00	12.20
E	13.80	14.00	14.20
E1	11.80	12.00	12.20
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BDC.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD FLASH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE: LQFP 12X12MM 64LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: XX .XX .XXX ANGLE	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1212064	APPROVED: YJ. CHAE	DRAWING NUMBER: OLQ-1212064 REV: — SHEET: 1 OF 1

Figure 26.3 Package dimension (64LQFP12)

26.4 64LQFP10 Package dimension

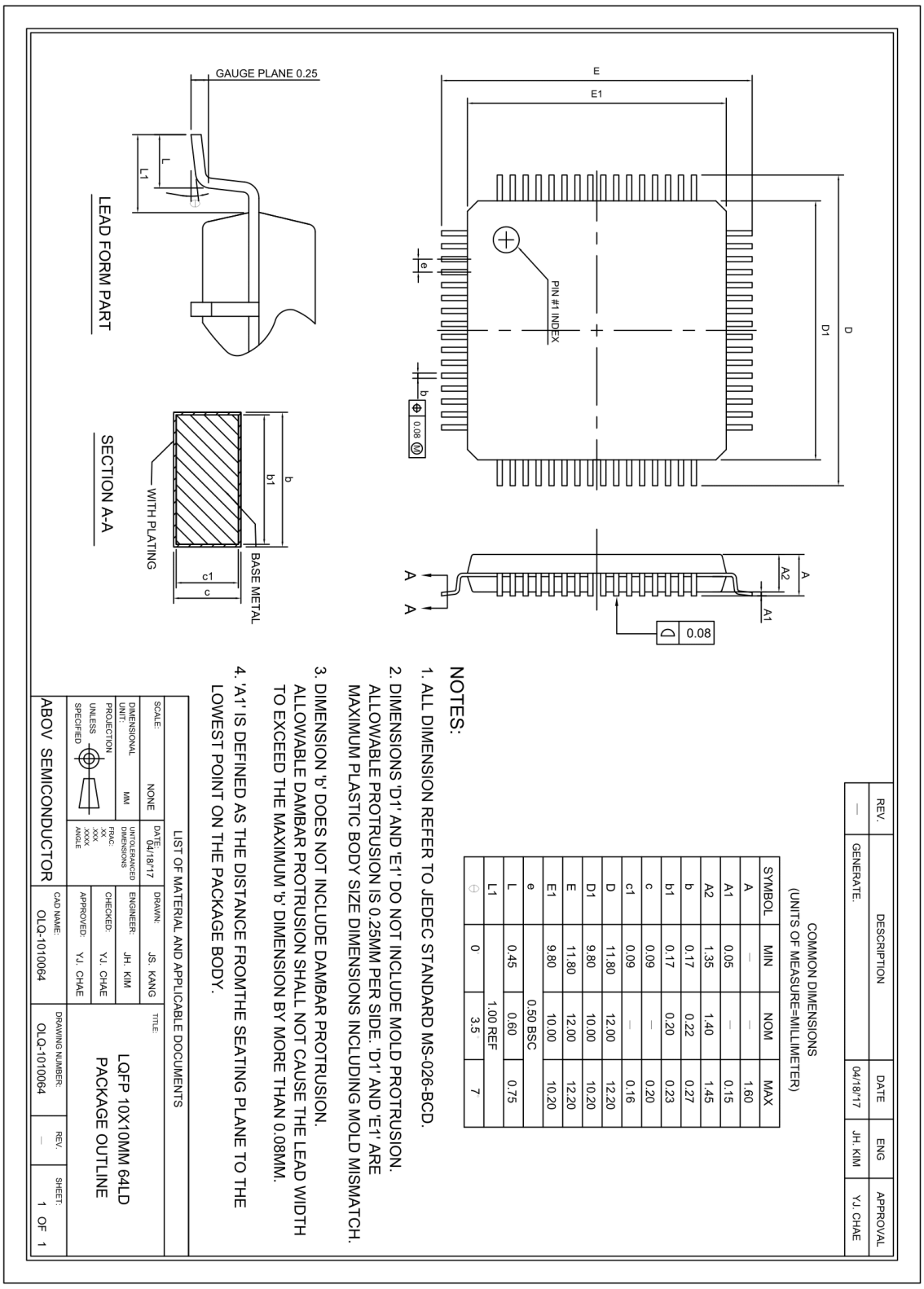


Figure 26.4 Package dimension (64LQFP10)

26.5 **48LQFP Package dimension**

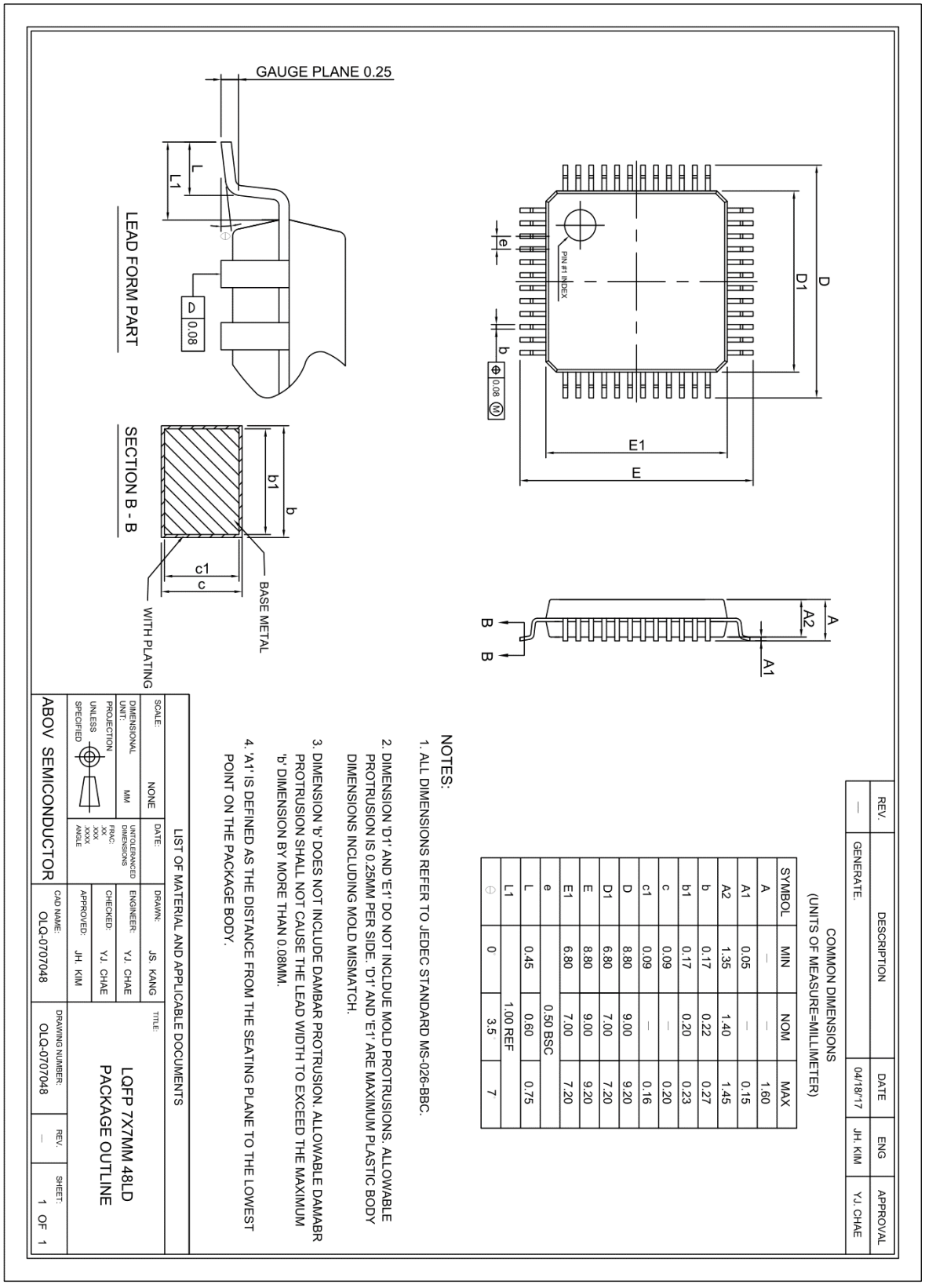


Figure 26.5 Package dimension (48LQFP)

26.6 48QFN Package dimension

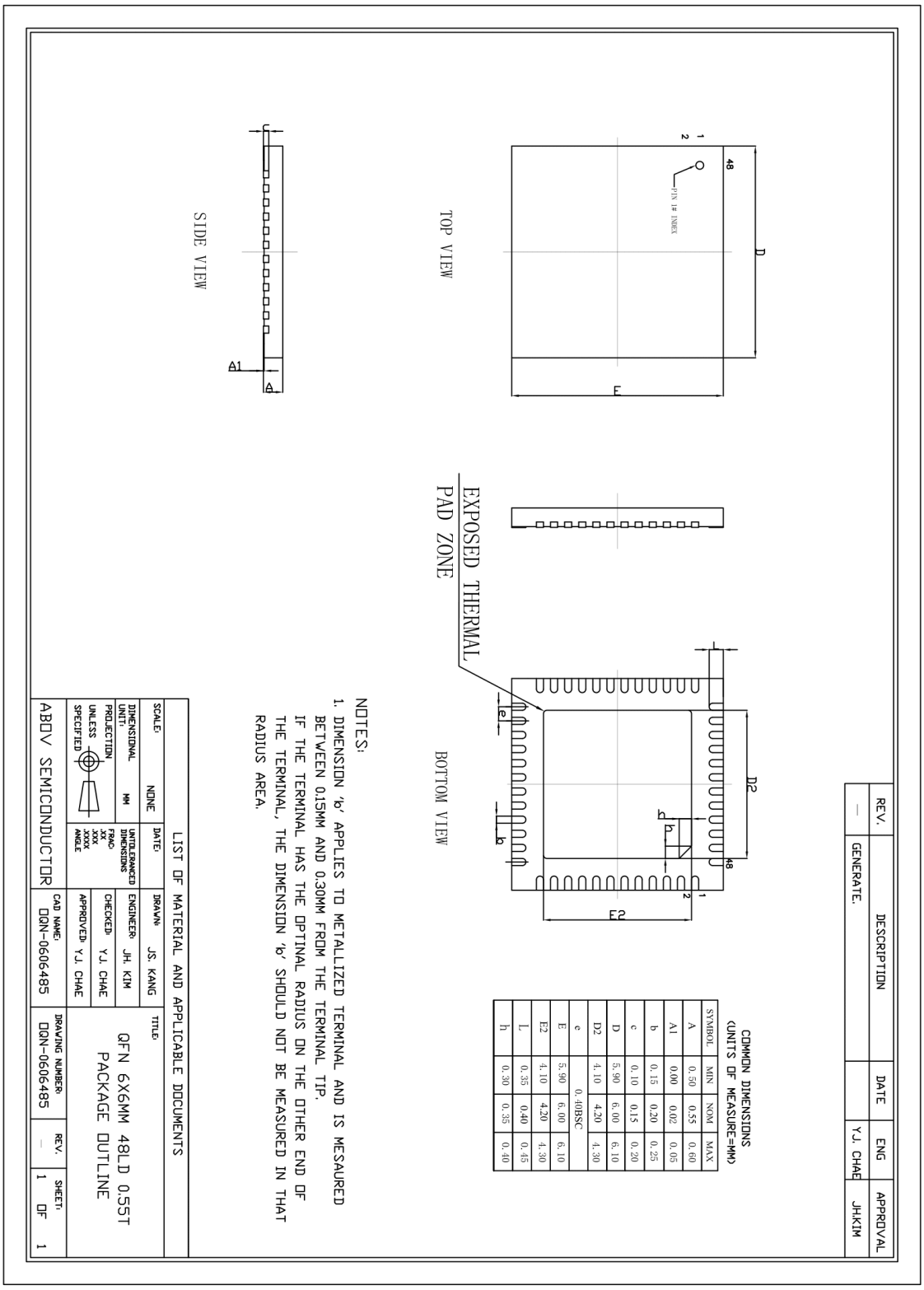
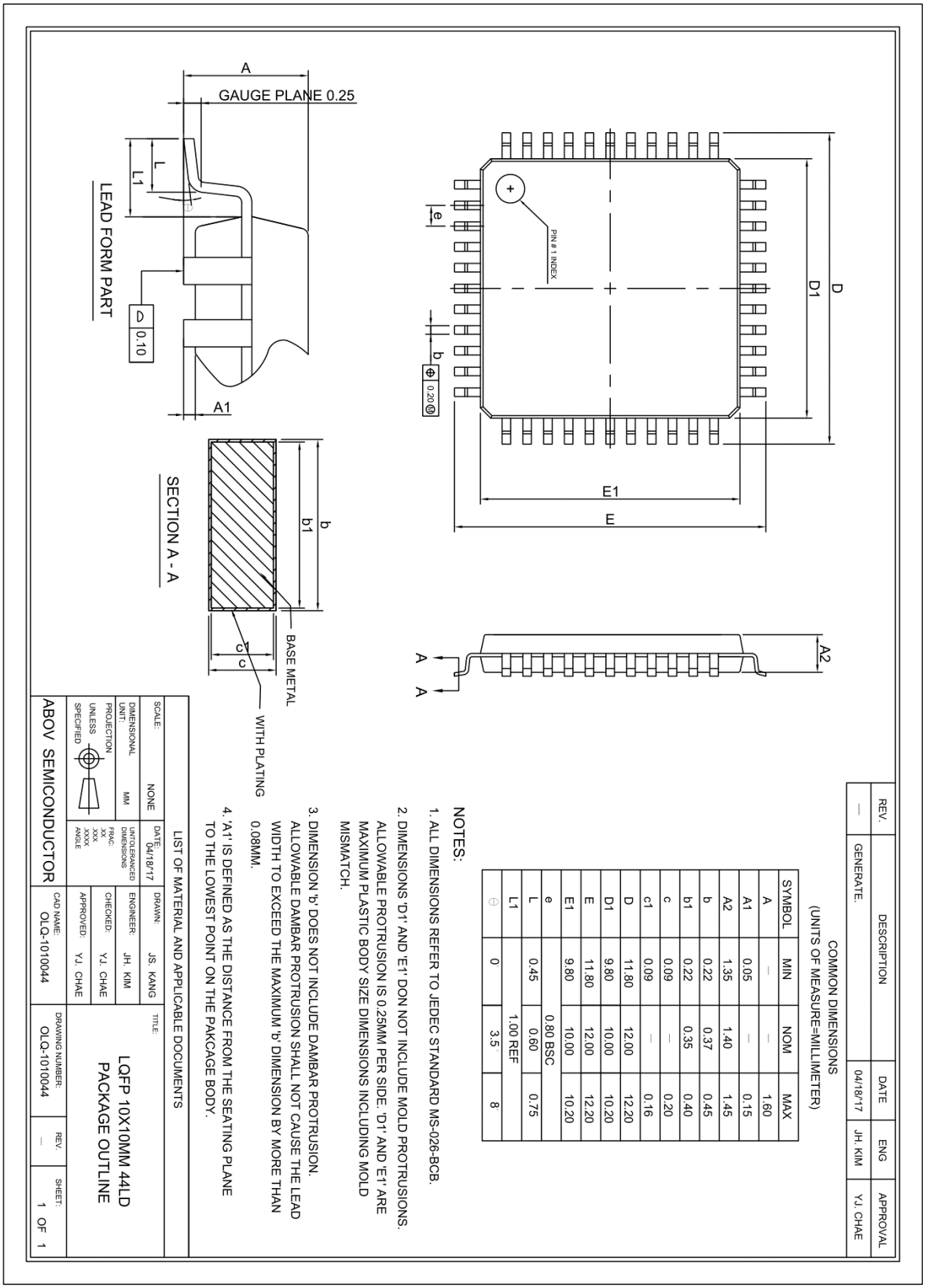


Figure 26.6 Package dimension (48QFN)

26.7 **44LQFP Package dimension**



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.37	0.45
b1	0.22	0.35	0.40
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e		0.80 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0	3.5	8

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BCB.
2. DIMENSIONS 'D1' AND 'E1' DON NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PAKCAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE: LQFP 10X10MM 44LD PACKAGE OUTLINE	
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM		
PROJECTION	FRAC: X XX XXX XXXX ANGLE	CHECKED: YJ. CHAE		
UNLESS SPECIFIED		APPROVED: YJ. CHAE	CAD NAME: OLQ-1010044	DRAWING NUMBER: OLQ-1010044
ABOV SEMICONDUCTOR				REV: —
				SHEET: 1 OF 1

Figure 26.7 Package dimension (44LQFP)