Ultra-Low Power Cortex-M0+ Microcontroller
Flash 128/64KB, SRAM 20KB, Data Flash 4KB, ADC, AES

DS Rev. 0.94

Features

- High performance Cortex-M0+ core
- 128/64KB Flash memory
- 20KB SRAM, 32-byte backup register
- 4KB Data Flash memory
- Watchdog Timer, Real Time Clock and Calendar
- Nine general purpose timers
  - Periodic, one-shot, PWM, capture
- 12-bit ADC, 16-channel, 1Msps, down to 1.71V
- Temperature Sensor
- Two comparators, down to 1.71V
- External communication ports
  - 2 x USART, 1 x UART, 2 x LPUART, 1 x SC
  - 3 x I2C up to 1Mbps
  - 4 x SPI up to 16Mbps
- AES 128-bit encryption/decryption
- True random number generator
- Clock monitoring function for system clock
- LCD driver for up to 8x39 segments
  - 16-step contrast control, resistor/cap bias
- 8/16/32-bit CRC unit, 128-bit unique ID
- Seven DMA channels
- SWD debug interface
- USART (UART) ISP supported
- Ultra-low power tech
  - 1.71V to 3.6V Supply voltage
  - 90uA/MHz in RUN mode
  - 13uA in RUN mode (32.768kHz, 40kHz)
  - 0.99uA DEEP SLEEP + RTCC + retention
  - 0.35uA DEEP SLEEP with power control
  - 45nA SHUT DOWN (DEEP SLEEP mode 3)
  - 5us wakeup time from power modes
- Five types of package options
  - LQFP80-1212
  - LQFP64-1010
  - LQFP48-0707
  - LQFP32-0707
  - QFN32-0505
- Operating temperature, -40℃ to +105℃
  - Commercial and Industrial grade

Applications

- Smart meters, Smart card readers
- Door lock, Building and Home control
- IoT devices, Wireless sensor networks
- Portable healthcare/consumer electronics

Product selection table

Table 1. Device Summary

Part Number	Flash	SRAM	USART	UART	LPUART	SC	I2C	SPI	TIMER	LCD	ADC	I/O	Package
A31L214ML	128KB	20KB	2	1	2	1	3	4	9	39x8	16ch	73	80LQFP-1212
A31L214RL*	128KB	20KB	2	1	2	1	3	4	9	27x8	16ch	57	64LQFP-1010
A31L214CL*	128KB	20KB	2	1	2	1	3	3	8	15x4	8ch	41	48LQFP-0707
A31L214KN*	128KB	20KB	2	1	2	1	3	1	3	–	8ch	28	32LQFP-0707
A31L214KU*	128KB	20KB	2	1	2	1	3	1	4	–	8ch	28	32QFN-0505
A31L213ML*	64KB	20KB	2	1	2	1	3	4	9	39x8	16ch	73	80LQFP-1212
A31L213RL*	64KB	20KB	2	1	2	1	3	4	9	27x8	16ch	57	64LQFP-1010
A31L213CL*	64KB	20KB	2	1	2	1	3	3	8	15x4	8ch	41	48LQFP-0707
A31L213KN*	64KB	20KB	2	1	2	1	3	1	3	–	8ch	28	32LQFP-0707
A31L213KU*	64KB	20KB	2	1	2	1	3	1	4	–	8ch	28	32QFN-0505

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

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1 Description

The A31L21x series is an ultra-low power microcontroller based on the high-performance ARM Cortex-M0+ core.

It has a Flash memory of up to 128KB, a Data Flash of 4KB, and an SRAM of 20KB. Operation voltage of the device is from 1.71V to 3.6V. It provides a highly flexible and cost-effective solution for many embedded control applications.

This device offers 16-bit timers, Real timer and calendar, 12-bit ADC, Comparator, CRC generator, UART, USART, LPUART, I2C, SPI, Smart card interface, LCD driver/controller, AES 128, True random number generator, DMA, etc. The A31L21x series also has a POR, LVR, LVI, and an internal RC oscillator.

The A31L21x series supports SLEEP mode and DEEP SLEEP mode to reduce power consumption, and these power saving modes allow the design of low power applications.

1.1 Device overview

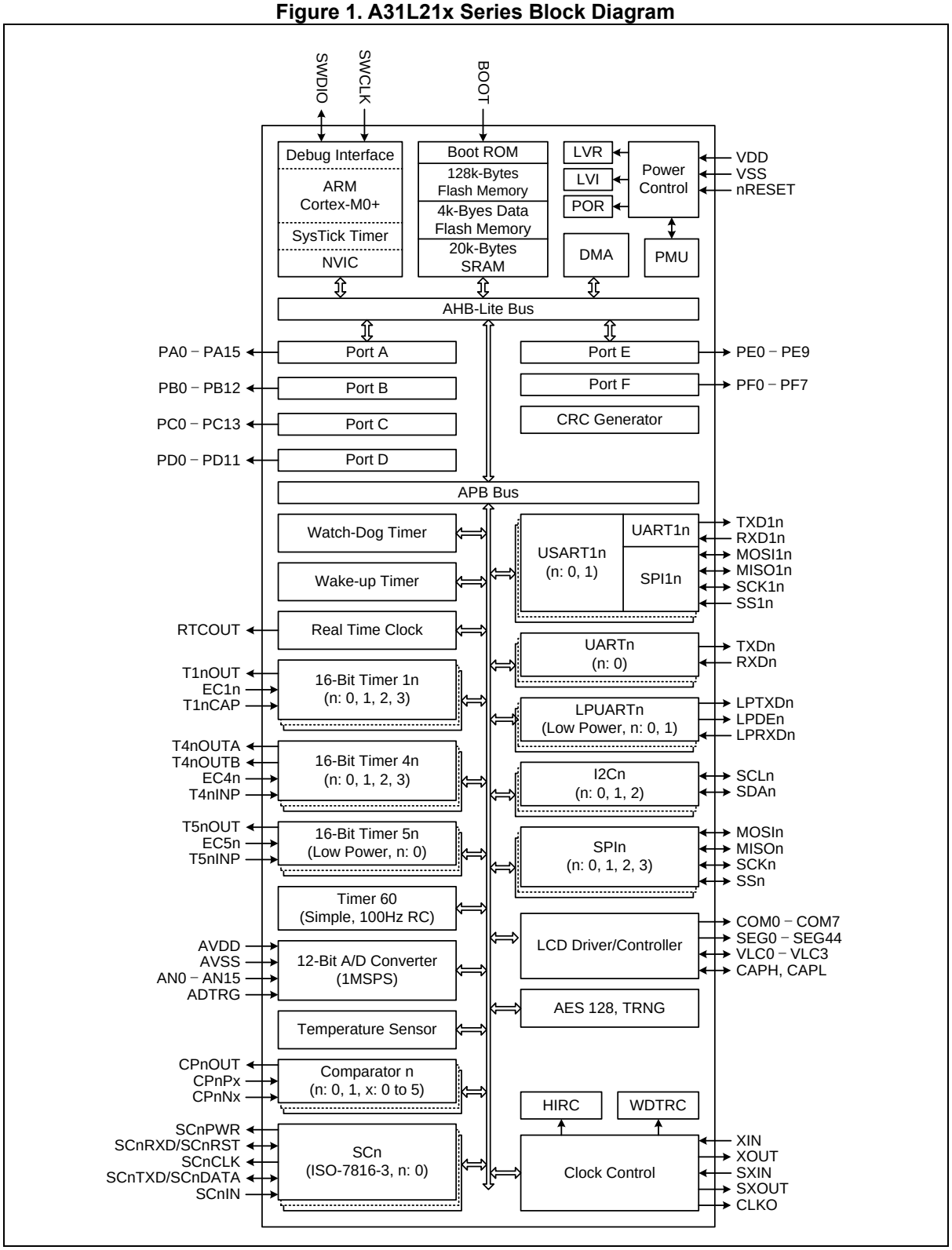
Table 2. A31L21x Series Features and Peripheral Counts

Peripheral	Description
CPU	Cortex-M0+
Memory	• Flash memory: 128/64 Kbytes • Data Flash: 4 Kbytes • SRAM: 20 Kbytes, 32-byte backup register
I/O	73 programmable
Timers	• Watchdog Timer, Real time clock and calendar • Eight general purpose timers and one low power timer — Periodic, one-shot, PWM, capture mode
LCD driver	• 39 segments and 8 commons • Resistor/cap bias, and 16-step contrast control
DMA	Seven DMA channels, ADC/USART/UART/I2C/SPI/SC/AES
ADC	16-channel input, 12-bit ADC with 1Msps, down to 1.71V
Comparator	Two comparators, down to 1.71V
Temperature sensor	Frequency variation: 3.2 kHz/℃
CRC generator	8/16/32-bit CRC generator, CRC-8/16/32, CRC-CCITT
Security	AES 128-bit encryption/decryption, True random number generator
External communication ports	• 2 USARTs (UART + SPI), 1 UART, 1 SC • 2 LPUARTs, up to 9600bps with 32.768kHz • 3 I^2Cs up to 1Mbps, 4 SPIs up to 16Mbps
128-bit Unique ID	Supported
System fail-safe function	Clock monitoring
Debug interface	SWD debug interface
Ultra-low power tech	• 1.71V to 3.6V supply voltage • 90uA/MHz in RUN mode, 13uA in RUN mode (32.768kHz, 40kHz) • 0.99uA DEEP SLEEP + RTCC + SRAM retention • 0.35uA DEEP SLEEP with power control • 45nA SHUT DOWN (DEEP SLEEP mode 3) • 5us wakeup time from all power modes
Packages	• LQFP 80-1212 (0.5mm pitch) • LQFP 64-1010 (0.5mm pitch) • LQFP 48-0707 (0.5mm pitch) • LQFP 32-0707 (0.8mm pitch), • QFN 32-0505 (0.5mm pitch)
Operating temperature	-40℃ to +85℃ (commercial grade)
	-40℃ to +105℃ (industrial grade)

1.2 Block diagram

Figure 1 shows a block diagram of the A31L21x series.

Figure 1. A31L21x Series Block Diagram



1.3 Functional description

The following sections provide a brief description of the features of the A31L21x series microcontroller.

1.3.1 ARM Cortex-M0+

The Cortex-M0+ processor has a very low gate count. It is a highly energy efficient processor for microcontrollers and deeply embedded applications that require an area-optimized, low-power processor.

In the core, the system timer (SYSTICK) provides a simple 24-bit timer that can be used as a real time operating system (RTOS) or as a simple counter.

The processor implements the ARMv6-M Thumb instruction set including a number of 32-bit instructions, which are introduced with Thumb-2 technology. Hardware single-cycle multiplication is available.

Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.

It also supports SWD debugging features.

1.3.2 Nested Vector-Interrupt Controller (NVIC)

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt.

The NVIC embedded in the Cortex-M0+ processor core achieves low latency interrupts processing and efficient processing of late arriving interrupts.

All NVIC registers can only be accessed through word transfers.

1.3.3 128KB Internal Flash memory

The A31L21x series has built-in 128KB Flash memory.

It supports self-programming feature. In addition, ISP and JTAG programming in boot or debug mode are supported.

1.3.4 20KB Internal SRAM

On-chip 20KB SRAM is used as a working memory space and as a program code area temporarily.

1.3.5 4KB Data Flash memory

The A31L21x series has 4KB Data Flash memory. It is used for temporary information storage purpose.

1.3.6 Boot logic

A boot logic supports Flash programming. The boot logic is activated when the external boot pin is set to boot mode.

1.3.7 System Control Unit (SCU)

An SCU block manages internal power, clock, reset and operation mode. It also controls the analog blocks (Oscillator block, VDC and LVR).

1.3.8 Power Management Unit (PMU)

A PMU block manages power of internal core, Code Flash, Data Flash, SRAM, logic, and peripheral blocks in RUN, SLEEP, and DEEP SLEEP modes.

It also controls the wake-up time from SLEEP and DEEP SLEEP modes.

1.3.9 24-bit Watchdog Timer (WDT)

A Watchdog Timer monitors the system. It generates internal resets or interrupts to detect abnormal status of the system.

1.3.10 Multi-purpose 16-bit timer

Eight-channel 16-bit timers and one-channel low power general-purposed 16-bit timer support the functions introduced below:

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

1.3.11 Real Time Clock and Calendar (RTCC)

A real time clock and a calendar can run in SLEEP and DEEP SLEEP modes. The RTCC is not reset by a system reset except in the event of a power-on reset.

1.3.12 USART (UART and SPI)

USART supports UART and SPI modes. The A31L21x series has 2 channel USART module.

Boot mode uses this USART10 block to download Flash program.

1.3.13 Inter-Integrated Circuit interface (I2C)

The A31L21x series has three channels of I2C block and supports up to 1MHz I2C communication.

Master and slave modes are available.

1.3.14 Serial Peripheral Interface (SPI)

The A31L21x series has four channels of SPI block and supports up to 16MHz communication.

Master and slave modes are available.

1.3.15 Universal Asynchronous Receiver/Transmitter (UART)

The A31L21x series has one channel of UART block.

For accurate baud rate control, a fractional baud-rate generation feature is supported.

1.3.16 Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

The A31L21x series has two channels of Low Power UART block. This LPUART is available at 32.768kHz sub oscillator with up to 9600bps.

1.3.17 Smartcard interface (SC)

The A31L21x series has one channel of SC block. This block supports UART and smartcard modes.

The SC block has also baud-rate compensation, receive time out data, and extra guard time registers.

1.3.18 General PORT I/Os

16-bit PA port, 13-bit PB port, 14-bit PC port, 12-bit PD port, 10-bit PE port, and 8-bit PF port are available and provide multiple functions.

- General I/O port
- External interrupt input port and on-chip input debounce filter
- Programmable pull-up, pull-down, and open-drain selection

1.3.19 12-bit Analog-to-Digital Converter (ADC)

ADC of the A31L21x series can convert analog signals to digital signals at a conversion rate of up to 1Msps. 20-channel analog MUX provides various combinations of data from external and internal analog signals.

1.3.20 Comparator

The A31L21x series has two comparator blocks. The block has an internal reference for channels.

1.3.21 LCD driver/controller

An LCD driver supports a resistor bias, capacitor bias with contrast control, and various duties.

1.3.22 Cyclic Redundancy Check (CRC) generator

The A31L21x series has four polynomials for the CRC generator: CRC-CCITT and CRC-8/-16/-32.

1.3.23 Advanced Encryption Standard (AES-128)

The AES-128 is used to encrypt and decrypt data (complies with FIPS PUB 197, 2001 November 26).

1.3.24 True Random Number Generator (RNG)

The RNG continuously provides 32-bit samples based on an analog noise source.

1.3.25 Temperature Sensor (TS)

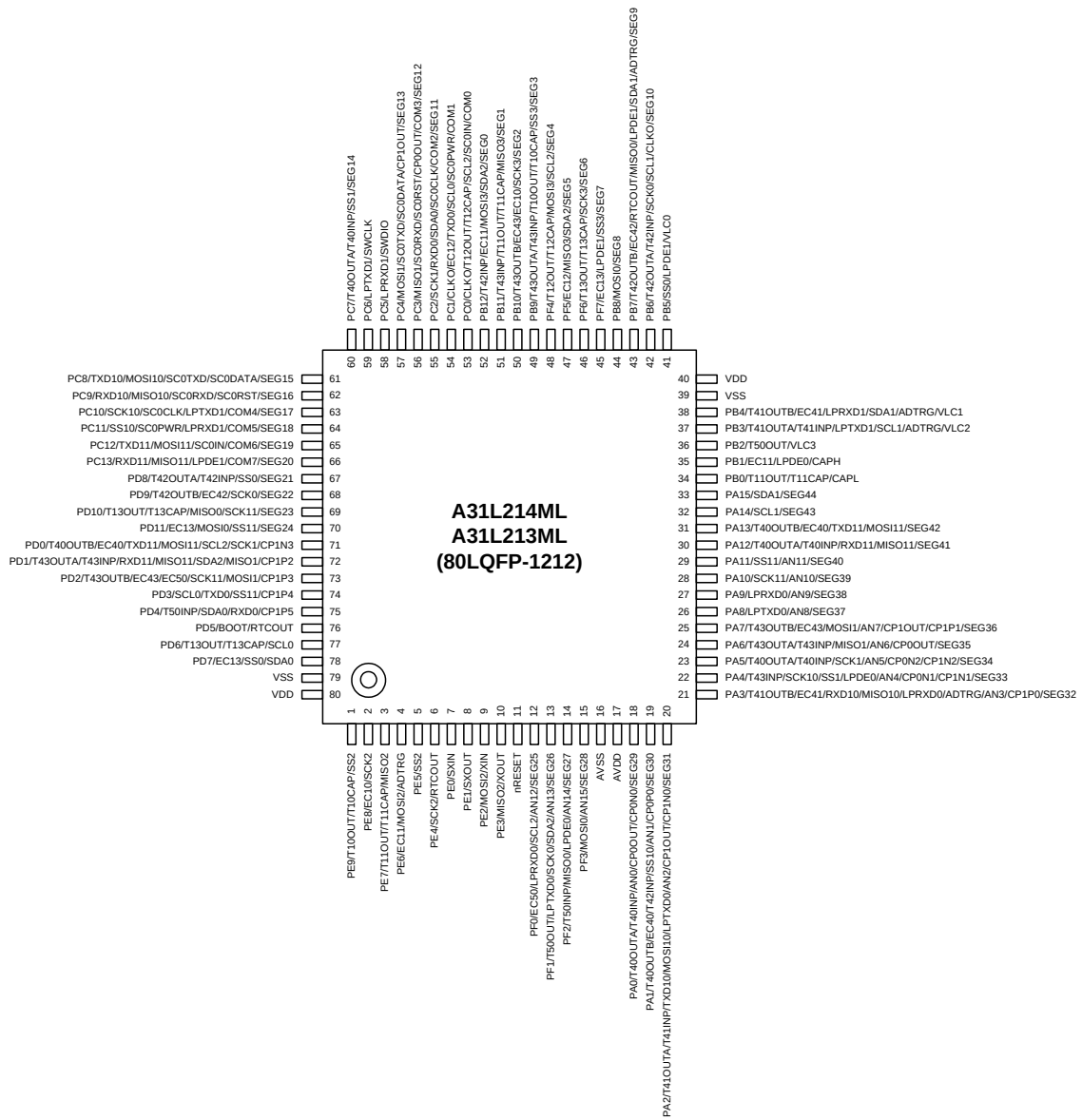
The temperature sensor consists of a ring-oscillator. Its frequency varies with temperature.

2 Pinouts and pin descriptions

In chapter 2, pinouts and pin descriptions of the A31L21x series are introduced.

2.1 Pinouts

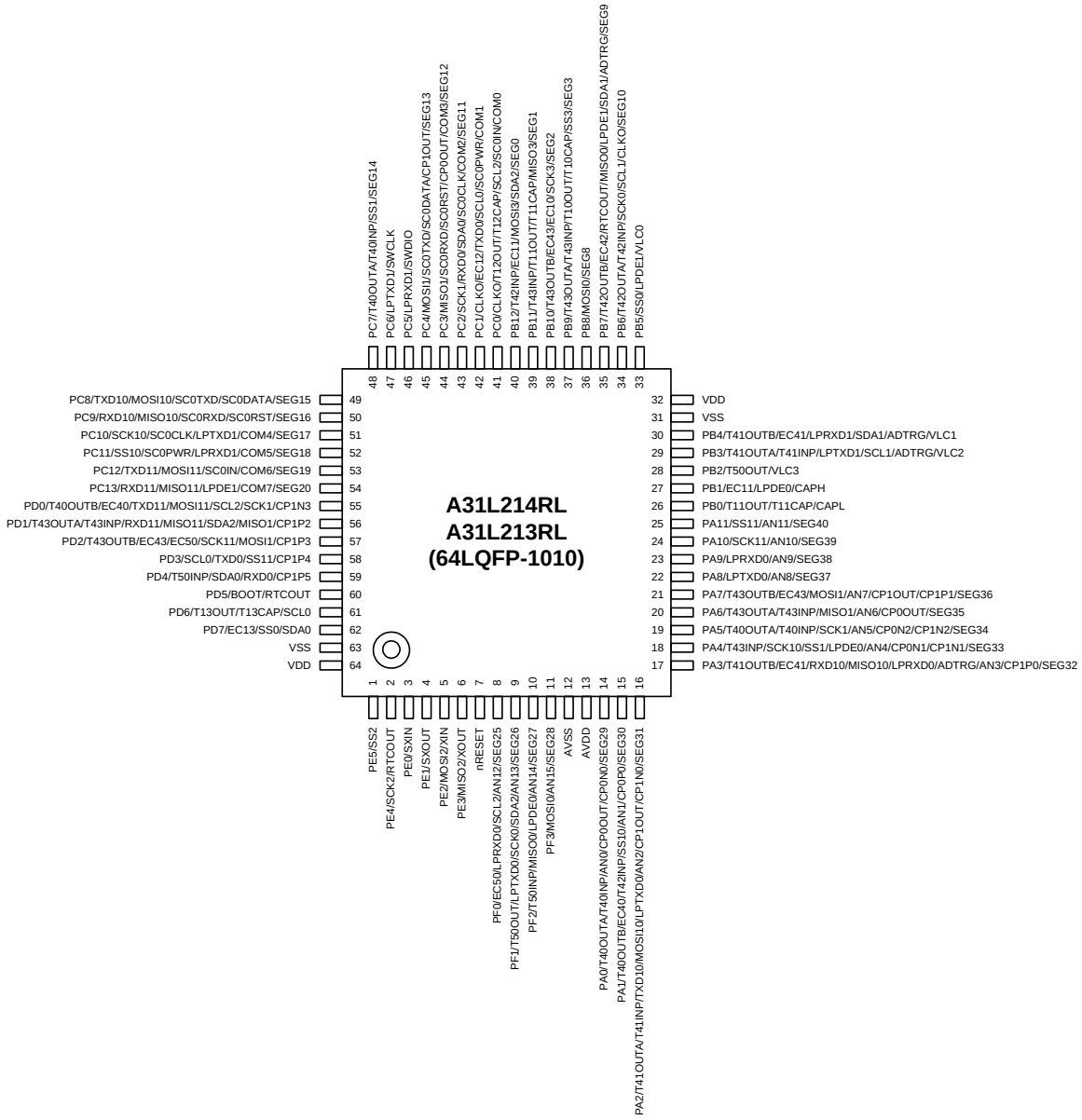
Figure 2. LQFP-80 Pinouts



NOTES:

1. PD[4:0] pins are 5V tolerant I/Os. The corresponding internal resistors of these pins must be disabled by S/W to use these pins as 5V I/Os. To use these pins as 5V tolerant outputs, external pull-up resistors must be used by applications and the corresponding pins must be configured as open-drain outputs by S/W.
2. The VDD should be greater than or equal to 2.0V and the corresponding pins are set to push-pull outputs by the PD_TYP[4:0] bits if CP1P[5:2] and CP1N3 are used as comparator pins for the alternative function.
3. The PA0, PA2, PE4, and PE6 pins can be wakeup sources from DEEP SLEEP with ALLPWR = 1/2/3.

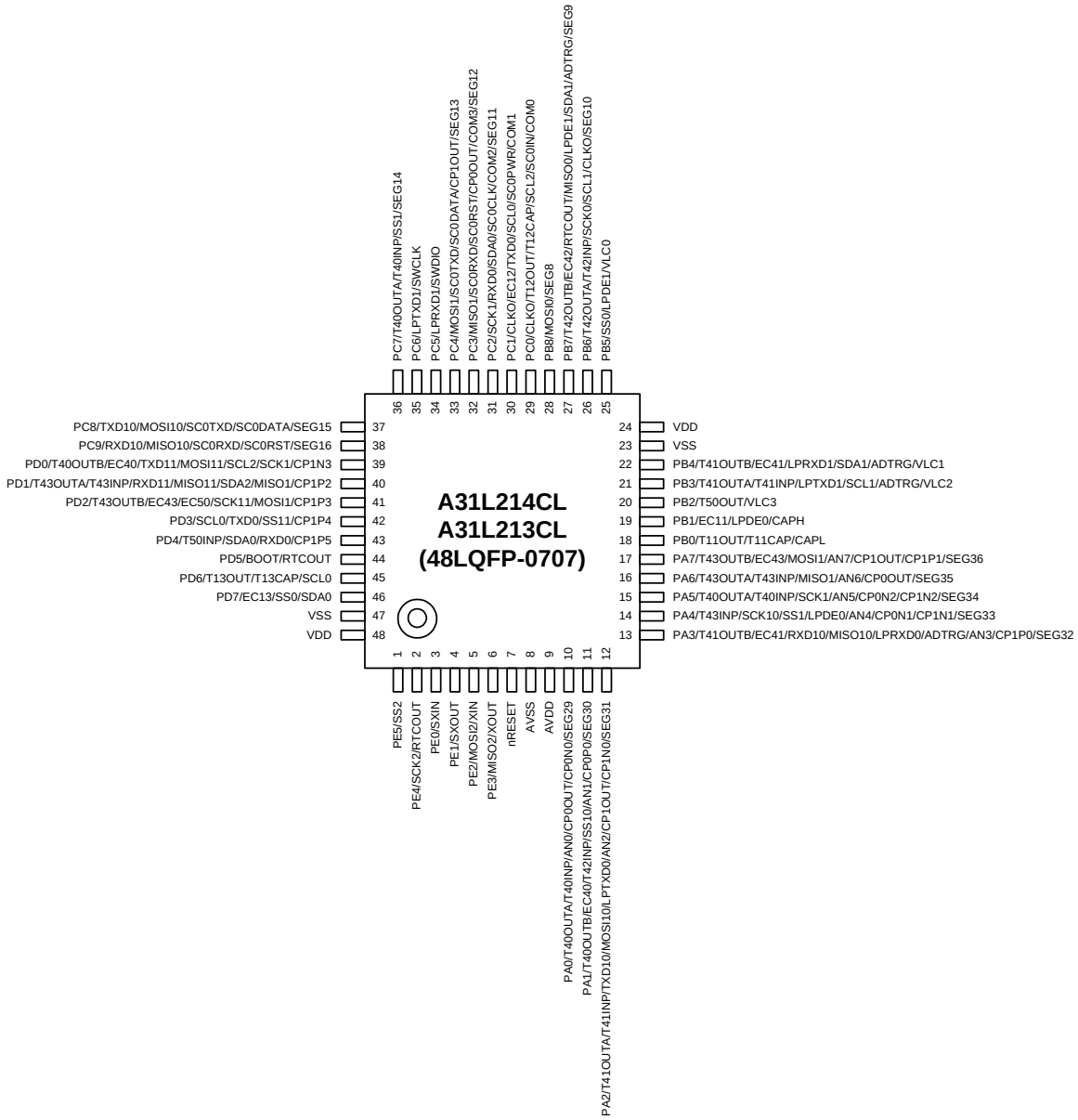
Figure 3. LQFP-64 Pinouts



NOTES:

1. Each of the PA[15:12], PD[11:8], PE[9:6] and PF[7:4] pins should be selected as a push-pull output or an input with pull-up or pull-down resistor by software control when the 64LQFP package is used.
2. PD[4:0] pins are 5V tolerant I/Os. The corresponding internal resistors of these pins must be disabled by S/W to use these pins as 5V I/Os. To use these pins as 5V tolerant outputs, external pull-up resistors must be used by applications and the corresponding pins must be configured as open-drain outputs by S/W
3. The VDD should be greater than or equal to 2.0V and the corresponding pins are set to push-pull outputs by the PD_TYP[4:0] bits if CP1P[5:2] and CP1N3 are used as comparator pins for the alternative function.
4. The PA0, PA2, and PE4 pins can be wakeup sources from DEEP SLEEP with ALLPWR = 1/2/3.

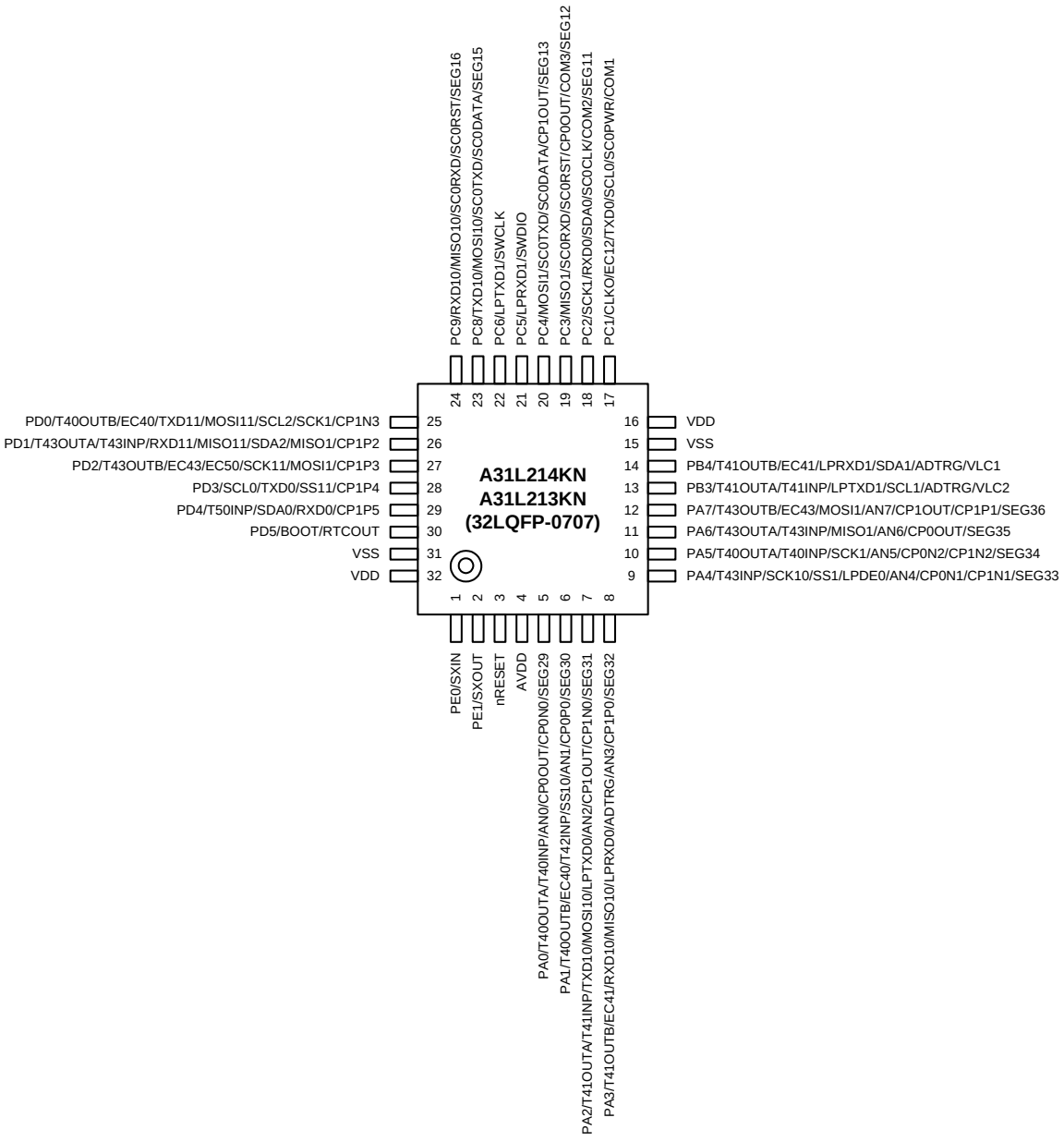
Figure 4. LQFP-48 Pinouts



NOTES:

1. Each of the PA[15:8], PB[12:9], PC[13:10], PD[11:8], PE[9:6] and PF[7:0] pins should be selected as a push-pull output or an input with pull-up or pull-down resistor by software control when the 48LQFP package is used.
2. PD[4:0] pins are 5V tolerant I/Os. The corresponding internal resistors of these pins must be disabled by S/W to use these pins as 5V I/Os. To use these pins as 5V tolerant outputs, external pull-up resistors must be used by applications and the corresponding pins must be configured as open-drain outputs by S/W
3. The VDD should be greater than or equal to 2.0V and the corresponding pins are set to push-pull outputs by the PD_TYP[4:0] bits if CP1P[5:2] and CP1N3 are used as comparator pins for the alternative function.
4. The PA0, PA2, and PE4 pins can be wakeup sources from DEEP SLEEP with ALLPWR = 1/2/3.

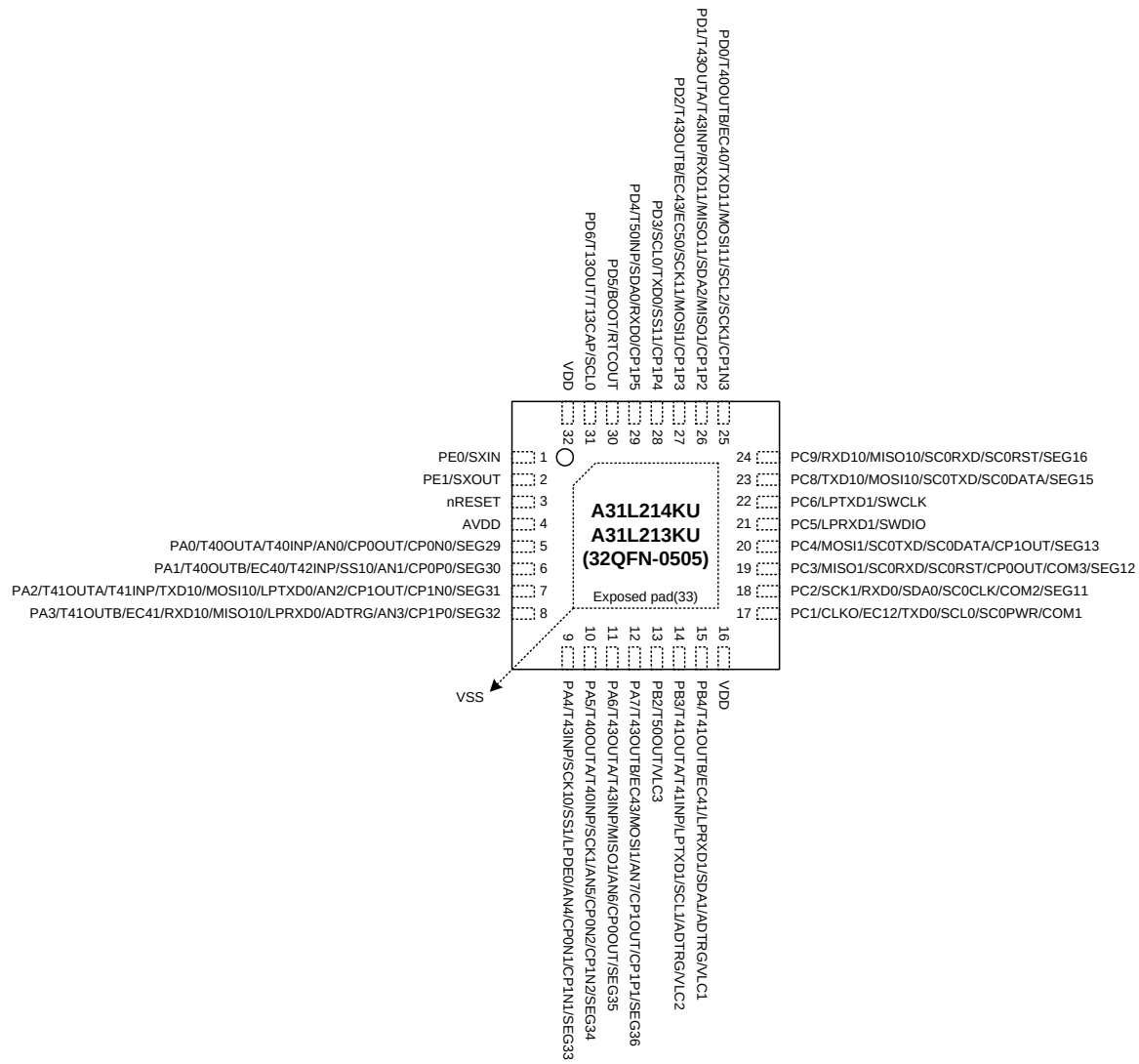
Figure 5. LQFP-32 Pinouts



NOTES:

1. Each of the PA[15:8], PB[12:5, 2:0], PC[13:10, 7, 0], PD[11:6], PE[9:2] and PF[7:0] pins should be selected as a push-pull output or an input with pull-up or pull-down resistor by software control when the 32LQFP package is used.
2. PD[4:0] pins are 5V tolerant I/Os. The corresponding internal resistors of these pins must be disabled by S/W to use these pins as 5V I/Os. To use these pins as 5V tolerant outputs, external pull-up resistors must be used by applications and the corresponding pins must be configured as open-drain outputs by S/W
3. The VDD should be greater than or equal to 2.0V and the corresponding pins are set to push-pull outputs by the PD_TYP[4:0] bits if CP1P[5:2] and CP1N3 are used as comparator pins for the alternative function.
4. The PA0 and PA2 pins can be wakeup sources from DEEP SLEEP with ALLPWR = 1/2/3.

Figure 6. QFN-32 Pinouts



NOTES:

1. Each of the PA[15:8], PB[12:5, 1:0], PC[13:10, 7, 0], PD[11:7], PE[9:2] and PF[7:0] pins should be selected as a push-pull output or an input with pull-up or pull-down resistor by software control when the 32QFN package is used.
2. PD[4:0] pins are 5V tolerant I/Os. The corresponding internal resistors of these pins must be disabled by S/W to use these pins as 5V I/Os. To use these pins as 5V tolerant outputs, external pull-up resistors must be used by applications and the corresponding pins must be configured as open-drain outputs by S/W
3. The VDD should be greater than or equal to 2.0V and the corresponding pins are set to push-pull outputs by the PD_TYP[4:0] bits if CP1P[5:2] and CP1N3 are used as comparator pins for the alternative function.
4. The PA0 and PA2 pins can be wakeup sources from DEEP SLEEP with ALLPWR = 1/2/3.

2.2 Pin description

Table 3 shows pin configuration containing several pairs of power/ground and other dedicated pins. Multi-function pins have up to nine selections of functions including GPIO.

Table 3. Pin Description

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
1	-	-	-	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
					T10OUT	O	Timer 10 pulse output	
					T10CAP	I	Timer 10 capture input	
					SS2	I	SPI slave select input	
2	-	-	-	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
					EC10	I	Timer 10 event count input	
					SCK2	I/O	SPI clock input/output	
3	-	-	-	-	PE7*	IOUDS	PORT E Bit 7 Input/Output	
					T11OUT	O	Timer 11 pulse output	
					T11CAP	I	Timer 11 capture input	
					MISO2	I/O	SPI master input, slave output	
4	-	-	-	-	PE6*	IOUDS	PORT E Bit 6 Input/Output	Wake-up possible from DEEP SLEEP with ALLPWR=1/2/3
					EC11	I	Timer 11 event count input	
					MOSI2	I/O	SPI master output, slave input	
					ADTRG	I	ADC trigger input	
5	1	1	-	-	PE5*	IOUDS	PORT E Bit 5 Input/Output	
					SS2	I	SPI slave select input	
6	2	2	-	-	PE4*	IOUDS	PORT E Bit 4 Input/Output	Wake-up possible from DEEP SLEEP with ALLPWR=1/2/3
					SCK2	I/O	SPI clock input/output	
					RTCOUT	O	Real time clock output	
7	3	3	1	1	PE0*	IOUDS	PORT E Bit 0 Input/Output	
					SXIN	IA	Sub Oscillator Input	
8	4	4	2	2	PE1*	IOUDS	PORT E Bit 1 Input/Output	
					SXOUT	OA	Sub Oscillator Output	
9	5	5	-	-	PE2*	IOUDS	PORT E Bit 2 Input/Output	
					MOSI2	I/O	SPI master output, slave input	
					XIN	IA	Main oscillator input	
10	6	6	-	-	PE3*	IOUDS	PORT E Bit 3 Input/Output	
					MISO2	I/O	SPI master input, slave output	
					XOUT	OA	Main oscillator output	
11	7	7	3	3	nRESET	Input	External Reset Input	Always pull-up

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
12	8	-	-	-	PF0*	IOUDS	PORT F Bit 0 Input/Output	
					EC50	I	Timer 50 event count input	
					LPRXD0	I	Low power UART data input	
					SCL2	I/O	I2C clock input/output	
					AN12	IA	A/D converter analog input channel	
					SEG25	OA	LCD segment signal output	
13	9	-	-	-	PF1*	IOUDS	PORT F Bit 1 Input/Output	
					T50OUT	O	Timer 50 pulse output	
					LPTXD0	O	Low power UART data output	
					SCK0	I/O	SPI clock input/output	
					SDA2	I/O	I2C data input/output	
					AN13	IA	A/D converter analog input channel	
					SEG26	OA	LCD segment signal output	
14	10	-	-	-	PF2*	IOUDS	PORT F Bit 2 Input/Output	
					T50INP	I	Timer 50 capture/clear input	
					MISO0	I/O	SPI master input, slave output	
					LPDE0	O	Low power UART DE signal output	
					AN14	IA	A/D converter analog input channel	
					SEG27	OA	LCD segment signal output	
15	11	-	-	-	PF3*	IOUDS	PORT F Bit 3 Input/Output	
					MOSI0	I/O	SPI master output, slave input	
					AN15	IA	A/D converter analog input channel	
					SEG28	OA	LCD segment signal output	
16	12	8	-	-	AVSS	PA	Analog Ground	
17	13	9	4	4	AVDD	PA	Analog Power	
18	14	10	5	5	PA0*	IOUDS	PORT A Bit 0 Input/Output	Wake-up possible from DEEP SLEEP with ALLPWR=1/2/3
					T40OUTA	O	Timer 40 pulse output	
					T40INP	I	Timer 40 capture/force input	
					AN0	IA	A/D converter analog input channel	
					CP0OUT	OA	Comparator 0 output	
					CP0N0	IA	Comparator 0 negative input	
					SEG29	OA	LCD segment signal output	
19	15	11	6	6	PA1*	IOUDS	PORT A Bit 1 Input/Output	
					T40OUTB	O	Timer 40 pulse output	
					EC40	I	Timer 40 event count input	
					T42INP	I	Timer 42 capture/force input	
					SS10	I	SPI slave select input	
					AN1	IA	A/D converter analog input channel	
					CP0P0	IA	Comparator 0 positive input	
					SEG30	OA	LCD segment signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
20	16	12	7	7	PA2*	IOUDS	PORT A Bit 2 Input/Output	Wake-up possible from DEEP SLEEP with ALLPWR=1/2/3
					T41OUTA	O	Timer 41 pulse output	
					T41INP	I	Timer 41 capture/force input	
					TXD10	O	UART data output	
					MOSI10	I/O	SPI master output, slave input	
					LPTXD0	O	Low power UART data output	
					AN2	IA	A/D converter analog input channel	
					CP1OUT	OA	Comparator 1 output	
					CP1N0	IA	Comparator 1 negative input	
					SEG31	OA	LCD segment signal output	
21	17	13	8	8	PA3*	IOUDS	PORT A Bit 3 Input/Output	
					T41OUTB	O	Timer 41 pulse output	
					EC41	I	Timer 41 event count input	
					RXD10	I	UART data input	
					MISO10	I/O	SPI master input, slave output	
					LPRXD0	I	Low power UART data input	
					ADTRG	I	ADC trigger input	
					AN3	IA	A/D converter analog input channel	
					CP1P0	IA	Comparator 1 positive input	
					SEG32	OA	LCD segment signal output	
22	18	14	9	9	PA4*	IOUDS	PORT A Bit 4 Input/Output	
					T43INP	I	Timer 43 capture/force input	
					SCK10	I/O	SPI clock input/output	
					SS1	I	SPI slave select input	
					LPDE0	O	Low power UART DE signal output	
					AN4	IA	A/D converter analog input channel	
					CP0N1	IA	Comparator 0 negative input	
					CP1N1	IA	Comparator 1 negative input	
					SEG33	OA	LCD segment signal output	
23	19	15	10	10	PA5*	IOUDS	PORT A Bit 5 Input/Output	
					T40OUTA	O	Timer 40 pulse output	
					T40INP	I	Timer 40 capture/force input	
					SCK1	I/O	SPI clock input/output	
					AN5	IA	A/D converter analog input channel	
					CP0N2	IA	Comparator 0 negative input	
					CP1N2	IA	Comparator 1 negative input	
					SEG34	OA	LCD segment signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
24	20	16	11	11	PA6*	IOUDS	PORT A Bit 6 Input/Output	
					T43OUTA	O	Timer 43 pulse output	
					T43INP	I	Timer 43 capture/force input	
					MISO1	I/O	SPI master input, slave output	
					AN6	IA	A/D converter analog input channel	
					CP0OUT	OA	Comparator 0 output	
					SEG35	OA	LCD segment signal output	
25	21	17	12	12	PA7*	IOUDS	PORT A Bit 7 Input/Output	
					T43OUTB	O	Timer 43 pulse output	
					EC43	I	Timer 43 event count input	
					MOSI1	I/O	SPI master output, slave input	
					AN7	IA	A/D converter analog input channel	
					CP1OUT	OA	Comparator 1 output	
					CP1P1	IA	Comparator 1 positive input	
					SEG36	OA	LCD segment signal output	
26	22	-	-	-	PA8*	IOUDS	PORT A Bit 8 Input/Output	
					LPTXD0	O	Low power UART data output	
					AN8	IA	A/D converter analog input channel	
					SEG37	OA	LCD segment signal output	
27	23	-	-	-	PA9*	IOUDS	PORT A Bit 9 Input/Output	
					LPRXD0	I	Low power UART data input	
					AN9	IA	A/D converter analog input channel	
					SEG38	OA	LCD segment signal output	
28	24	-	-	-	PA10*	IOUDS	PORT A Bit 10 Input/Output	
					SCK11	I/O	SPI clock input/output	
					AN10	IA	A/D converter analog input channel	
					SEG39	OA	LCD segment signal output	
29	25	-	-	-	PA11*	IOUDS	PORT A Bit 11 Input/Output	
					SS11	I	SPI slave select input	
					AN11	IA	A/D converter analog input channel	
					SEG40	OA	LCD segment signal output	
30	-	-	-	-	PA12*	IOUDS	PORT A Bit 12 Input/Output	
					T40OUTA	O	Timer 40 pulse output	
					T40INP	I	Timer 40 capture/force input	
					RXD11	I	UART data input	
					MISO11	I/O	SPI master input, slave output	
					SEG41	OA	LCD segment signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
31	-	-	-	-	PA13*	IOUDS	PORT A Bit 13 Input/Output	
					T40OUTB	O	Timer 40 pulse output	
					EC40	I	Timer 40 event count input	
					TXD11	O	UART data output	
					MOSI11	I/O	SPI master output, slave input	
					SEG42	OA	LCD segment signal output	
32	-	-	-	-	PA14*	IOUDS	PORT A Bit 14 Input/Output	
					SCL1	I/O	I2C clock input/output	
					SEG43	OA	LCD segment signal output	
33	-	-	-	-	PA15*	IOUDS	PORT A Bit 15 Input/Output	
					SDA1	I/O	I2C data input/output	
					SEG44	OA	LCD segment signal output	
34	26	18	-	-	PB0*	IOUDS	PORT B Bit 0 Input/Output	
					T11OUT	O	Timer 11 pulse output	
					T11CAP	I	Timer 11 capture input	
					CAPL	I	Capacitor terminal for voltage booster	
35	27	19	-	-	PB1*	IOUDS	PORT B Bit 1 Input/Output	
					EC11	I	Timer 11 event count input	
					LPDE0	O	Low power UART DE signal output	
					CAPH	I	Capacitor terminal for voltage booster	
36	28	20	-	13	PB2*	IOUDS	PORT B Bit 2 Input/Output	
					T50OUT	O	Timer 50 pulse output	
					VLC3	IA/OA	LCD bias voltage input/output	
37	29	21	13	14	PB3*	IOUDS	PORT B Bit 3 Input/Output	
					T41OUTA	O	Timer 41 pulse output	
					T41INP	I	Timer 41 capture/force input	
					LPTXD1	O	Low power UART data output	
					SCL1	I/O	I2C clock input/output	
					ADTRG	I	ADC trigger input	
					VLC2	IA/OA	LCD bias voltage input/output	
38	30	22	14	15	PB4*	IOUDS	PORT B Bit 4 Input/Output	
					T41OUTB	O	Timer 41 pulse output	
					EC41	I	Timer 41 event count input	
					LPRXD1	I	Low power UART data input	
					SDA1	I/O	I2C data input/output	
					ADTRG	I	ADC trigger input	
					VLC1	IA/OA	LCD bias voltage input/output	
39	31	23	15	-	VSS	P	Ground	
40	32	24	16	16	VDD	P	VDD	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
41	33	25	-	-	PB5*	IOUDS	PORT B Bit 5 Input/Output	
					SS0	I	SPI slave select input	
					LPDE1	O	Low power UART DE signal output	
					VLC0	IA/OA	LCD bias voltage input/output	
42	34	26	-	-	PB6*	IOUDS	PORT B Bit 6 Input/Output	
					T42OUTA	O	Timer 42 pulse output	
					T42INP	I	Timer 42 event count input	
					SCK0	I/O	SPI clock input/output	
					SCL1	I/O	I2C clock input/output	
					CLKO	O	System clock output	
					SEG10	OA	LCD segment signal output	
43	35	27	-	-	PB7*	IOUDS	PORT B Bit 7 Input/Output	
					T42OUTB	O	Timer 42 pulse output	
					EC42	I	Timer 42 event count input	
					RTCOUT	O	Real time clock output	
					MISO0	I/O	SPI master input, slave output	
					LPDE1	O	Low power UART DE signal output	
					SDA1	I/O	I2C data input/output	
					ADTRG	I	ADC trigger input	
					SEG9	OA	LCD segment signal output	
44	36	28	-	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
					MOSI0	I/O	SPI master output, slave input	
					SEG8	OA	LCD segment signal output	
45	-	-	-	-	PF7*	IOUDS	PORT F Bit 7 Input/Output	
					EC13	I	Timer 13 event count input	
					LPDE1	O	Low power UART DE signal output	
					SS3	I	SPI slave select input	
					SEG7	OA	LCD segment signal output	
46	-	-	-	-	PF6*	IOUDS	PORT F Bit 6 Input/Output	
					T13OUT	O	Timer 13 pulse output	
					T13CAP	I	Timer 13 capture input	
					SCK3	I/O	SPI clock input/output	
					SEG6	OA	LCD segment signal output	
47	-	-	-	-	PF5*	IOUDS	PORT F Bit 5 Input/Output	
					EC12	I	Timer 12 event count input	
					MISO3	I/O	SPI master input, slave output	
					SDA2	I/O	I2C data input/output	
					SEG5	OA	LCD segment signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
48	-	-	-	-	PF4*	IOUDS	PORT F Bit 4 Input/Output	
					T12OUT	O	Timer 12 pulse output	
					T12CAP	I	Timer 12 capture input	
					MOSI3	I/O	SPI master output, slave input	
					SCL2	I/O	I2C clock input/output	
					SEG4	OA	LCD segment signal output	
49	37	-	-	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
					T43OUTA	O	Timer 43 pulse output	
					T43INP	I	Timer 43 event count input	
					T10OUT	O	Timer 10 pulse output	
					T10CAP	I	Timer 10 capture input	
					SS3	I	SPI slave select input	
					SEG3	OA	LCD segment signal output	
50	38	-	-	-	PB10*	IOUDS	PORT B Bit 10 Input/Output	
					T43OUTB	O	Timer 43 pulse output	
					EC43	I	Timer 43 event count input	
					EC10	I	Timer 10 event count input	
					SCK3	I/O	SPI clock input/output	
					SEG2	OA	LCD segment signal output	
51	39	-	-	-	PB11*	IOUDS	PORT B Bit 11 Input/Output	
					T43INP	I	Timer 43 event count input	
					T11OUT	O	Timer 11 pulse output	
					T11CAP	I	Timer 11 capture input	
					MISO3	I/O	SPI master input, slave output	
					SEG1	OA	LCD segment signal output	
52	40	-	-	-	PB12*	IOUDS	PORT B Bit 12 Input/Output	
					T42INP	I	Timer 42 event count input	
					EC11	I	Timer 11 event count input	
					MOSI3	I/O	SPI master output, slave input	
					SDA2	I/O	I2C data input/output	
					SEG0	OA	LCD segment signal output	
53	41	29	-	-	PC0*	IOUDS	PORT C Bit 0 Input/Output	
					CLKO	O	System clock output	
					T12OUT	O	Timer 12 pulse output	
					T12CAP	I	Timer 12 capture input	
					SCL2	I/O	I2C clock input/output	
					SC0IN	I	Smartcard detection input	
					COM0	OA	LCD common signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
54	42	30	17	17	PC1*	IOUDS	PORT C Bit 1 Input/Output	
					CLKO	O	System clock output	
					EC12	I	Timer 12 event count input	
					TXD0	O	UART data output	
					SCL0	I/O	I2C clock input/output	
					SC0PWR	O	Smartcard power control output	
					COM1	OA	LCD common signal output	
55	43	31	18	18	PC2*	IOUDS	PORT C Bit 2 Input/Output	
					SCK1	I/O	SPI clock input/output	
					RXD0	I	UART data input	
					SDA0	I/O	I2C data input/output	
					SC0CLK	O	Smartcard clock output	
					COM2	OA	LCD common signal output	
					SEG11	OA	LCD segment signal output	
56	44	32	19	19	PC3*	IOUDS	PORT C Bit 3 Input/Output	
					MISO1	I/O	SPI master input, slave output	
					SC0RXD	I	SC0's UART data input	
					SC0RST	O	Smartcard reset output	
					CP0OUT	OA	Comparator 0 output	
					COM3	OA	LCD common signal output	
					SEG12	OA	LCD segment signal output	
57	45	33	20	20	PC4*	IOUDS	PORT C Bit 4 Input/Output	
					MOSI1	I/O	SPI master output, slave input	
					SC0TXD	O	SC0's UART data output	
					SC0DATA	I/O	Smartcard data input/output	
					CP1OUT	O	Comparator 1 output	
					SEG13	OA	LCD segment signal output	
58	46	34	21	21	PC5	IOUDS	PORT C Bit 5 Input/Output	
					LPRXD1	Input	Low power UART data input	
					SWDIO*	I/O	SWD data input/output	Pull-up when reset
59	47	35	22	22	PC6	IOUDS	PORT C Bit 6 Input/Output	
					LPTXD1	Output	Low power UART data output	
					SWCLK*	Input	SWD clock input	Pull-down when reset
60	48	36	-	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
					T40OUTA	O	Timer 40 pulse output	
					T40INP	I	Timer 40 event count input	
					SS1	I	SPI slave select input	
					SEG14	OA	LCD segment signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
61	49	37	23	23	PC8*	IOUDS	PORT C Bit 8 Input/Output	
					TXD10	O	UART data output	
					MOSI10	I/O	SPI master output, slave input	
					SC0TXD	O	SC0's UART data output	
					SC0DATA	I/O	Smartcard data input/output	
					SEG15	OA	LCD segment signal output	
62	50	38	24	24	PC9*	IOUDS	PORT C Bit 9 Input/Output	
					RXD10	I	UART data input	
					MISO10	I/O	SPI master input, slave output	
					SC0RXD	I	SC0's UART data input	
					SC0RST	O	Smartcard reset output	
					SEG16	OA	LCD segment signal output	
63	51	-	-	-	PC10*	IOUDS	PORT C Bit 10 Input/Output	
					SCK10	I/O	SPI clock input/output	
					SC0CLK	O	Smartcard clock output	
					LPTXD1	O	Low power UART data output	
					COM4	OA	LCD common signal output	
					SEG17	OA	LCD segment signal output	
64	52	-	-	-	PC11*	IOUDS	PORT C Bit 11 Input/Output	
					SS10	I	SPI slave select input	
					SC0PWR	O	Smartcard power control output	
					LPRXD1	I	Low power UART data input	
					COM5	OA	LCD common signal output	
					SEG18	OA	LCD segment signal output	
65	53	-	-	-	PC12*	IOUDS	PORT C Bit 12 Input/Output	
					TXD11	O	UART data output	
					MOSI11	I/O	SPI master output, slave input	
					SC0IN	I	Smartcard detection input	
					COM6	OA	LCD common signal output	
					SEG19	OA	LCD segment signal output	
66	54	-	-	-	PC13*	IOUDS	PORT C Bit 13 Input/Output	
					RXD11	I	UART data input	
					MISO11	I/O	SPI master input, slave output	
					LPDE1	O	Low power UART DE signal output	
					COM7	OA	LCD common signal output	
					SEG20	OA	LCD segment signal output	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
67	-	-	-	-	PD8*	IOUDS	PORT D Bit 8 Input/Output	
					T42OUTA	O	Timer 42 pulse output	
					T42INP	I	Timer 42 event count input	
					SS0	I	SPI slave select input	
					SEG21	OA	LCD segment signal output	
68	-	-	-	-	PD9*	IOUDS	PORT D Bit 9 Input/Output	
					T42OUTB	O	Timer 42 pulse output	
					EC42	I	Timer 42 event count input	
					SCK0	I/O	SPI clock input/output	
					SEG22	OA	LCD segment signal output	
69	-	-	-	-	PD10*	IOUDS	PORT D Bit 10 Input/Output	
					T13OUT	O	Timer 13 pulse output	
					T13CAP	I	Timer 13 capture input	
					MISO0	I/O	SPI master input, slave output	
					SCK11	I/O	SPI clock input/output	
					SEG23	OA	LCD segment signal output	
70	-	-	-	-	PD11*	IOUDS	PORT D Bit 11 Input/Output	
					EC13	I	Timer 13 event count input	
					MOSI0	I/O	SPI master output, slave input	
					SS11	I	SPI slave select input	
					SEG24	OA	LCD segment signal output	
71	55	39	25	25	PD0*	IOUDS	PORT D Bit 0 Input/Output	5V tolerant I/O (The internal pull-up resistor must be disabled to use 5V I/O) VDD ≥ 2.0V and PD_TYP[1:0]=00b when CP1N3, CP1P2
					T40OUTB	O	Timer 40 pulse output	
					EC40	I	Timer 40 event count input	
					TXD11	O	UART data output	
					MOSI11	I/O	SPI master output, slave input	
					SCL2	I/O	I2C clock input/output	
					SCK1	I/O	SPI clock input/output	
					CP1N3	IA	Comparator 1 negative input	
72	56	40	26	26	PD1*	IOUDS	PORT D Bit 1 Input/Output	
					T43OUTA	O	Timer 43 pulse output	
					T43INP	I	Timer 43 event count input	
					RXD11	I	UART data input	
					MISO11	I/O	SPI master input, slave output	
					SDA2	I/O	I2C data input/output	
					MISO1	I/O	SPI master input, slave output	
					CP1P2	IA	Comparator 1 positive input	

Table 3. Pin Description (continued)

Pin number					Pin name	Type	Description	Remark
LQFP-80	LQFP-64	LQFP-48	LQFP-32	QFN-32				
73	57	41	27	27	PD2*	IOUDS	PORT D Bit 2 Input/Output	5V tolerant I/O (The internal pull-up resistor must be disabled to use 5V I/O) VDD ≥ 2.0V and PD_TYP[4:2]=000b when CP1P3, CP1P4, CP1P5
					T43OUTB	O	Timer 43 pulse output	
					EC43	I	Timer 43 event count input	
					EC50	I	Timer 50 event count input	
					SCK11	I/O	SPI clock input/output	
					MOSI1	I/O	SPI master output, slave input	
					CP1P3	IA	Comparator 1 positive input	
74	58	42	28	28	PD3*	IOUDS	PORT D Bit 3 Input/Output	
					SCL0	I/O	I2C clock input/output	
					TXD0	O	UART data output	
					SS11	I	SPI slave select input	
					CP1P4	IA	Comparator 1 positive input	
75	59	43	29	29	PD4*	IOUDS	PORT D Bit 4 Input/Output	
					T50INP	I	Timer 50 capture/clear input	
					SDA0	I/O	I2C data input/output	
					RXD0	I	UART data input	
					CP1P5	IA	Comparator 1 positive input	
76	60	44	30	30	PD5	IOUDS	PORT D Bit 5 Input/Output	
					BOOT*	I	Boot mode input	Pull-up when reset
					RTCOUT	O	Real time clock output	
77	61	45	-	31	PD6*	IOUDS	PORT D Bit 6 Input/Output	
					T13OUT	O	Timer 13 pulse output	
					T13CAP	I	Timer 13 capture input	
					SCL0	I/O	I2C clock input/output	
78	62	46	-	-	PD7*	IOUDS	PORT D Bit 7 Input/Output	
					EC13	I	Timer 13 event count input	
					SS0	I	SPI slave select input	
					SDA0	I/O	I2C data input/output	
79	63	47	31	-	VSS	P	Ground	
80	64	48	32	32	VDD	P	VDD	
-	-	-	-	33	VSS	P	Ground (Exposed pad)	

NOTES:

1. Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. (*) Selected pin function after reset condition
3. Pin order may be changed with revision notice.

3 System and memory overview

Main system and memory of A31L21x series consist of the followings:

- ARM® Cortex® -M0+ core
- Seven channels of DMA
- Internal SRAM
- Internal Code Flash memory
- Internal Data Flash memory
- AHB (Advanced High Performance Bus) and APB (Advanced Peripheral Bus)

3.1 Cortex®-M0+ core

The Cortex-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

ARM's technical reference manual "DDI 0484C" provides detailed information on Cortex-M0+.

3.2 Interrupt controller

The Cortex-M0+ processor has an embedded interrupt controller named NVIC (Nested Vector Interrupt Controller). The A31L21x series has an additional interrupt control block for controlling 32 interrupt sources generated by internal peripherals.

To use interrupts from internal peripherals, both the NVIC and the interrupt control block must be configured properly.

This document only describes the peripheral interrupt controller, therefore for more information on NVIC inside the Cortex-M0+ processor, please refer to the technical reference manual “ARM DDI 0484C” on the ARM technical document site.

Table 4. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Exception
-13	0x0000_000C	Hard Fault Exception
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Exception
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Exception
-1	0x0000_003C	SysTick Exception
0	0x0000_0040	LVI Interrupt
1	0x0000_0044	WUT Interrupt
2	0x0000_0048	WDT Interrupt
3	0x0000_004C	EINT0 Interrupt
4	0x0000_0050	EINT1 Interrupt
5	0x0000_0054	EINT2 Interrupt
6	0x0000_0058	EINT3 Interrupt
7	0x0000_005C	TIMER40 Interrupt

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
8	0x0000_0060	TIMER41 Interrupt
9	0x0000_0064	TIMER42 Interrupt
10	0x0000_0068	I2C0 Interrupt
11	0x0000_006C	USART1[1:0] Interrupt
12	0x0000_0070	SPI[1:0] Interrupt
13	0x0000_0074	SPI[3:2] Interrupt
14	0x0000_0078	I2C1 Interrupt
15	0x0000_007C	TIMER50 Interrupt
16	0x0000_0080	SC0 Interrupt
17	0x0000_0084	Deep Sleep Mode 1 Wakeup Interrupt
18	0x0000_0088	ADC Interrupt
19	0x0000_008C	UART0 Interrupt
20	0x0000_0090	Temperature Sensor Interrupt
21	0x0000_0094	TIMER43 Interrupt
22	0x0000_0098	CMP[1:0] Interrupt
23	0x0000_009C	DMACH[3:0] Interrupt
24	0x0000_00A0	DMACH[6:4] Interrupt
25	0x0000_00A4	LPUART[1:0] Interrupt
26	0x0000_00A8	TIMER1[1:0] Interrupt
27	0x0000_00AC	TIMER1[3:2] Interrupt
28	0x0000_00B0	RTCC Interrupt TIMER60 Interrupt
29	0x0000_00B4	I2C2 Interrupt
30	0x0000_00B8	AES-128 Interrupt
31	0x0000_00BC	Random Number Generator Interrupt

3.3 Boot mode

3.3.1 Boot mode pin

The A31L21x series has Boot mode to program the internal Flash memory. Boot mode is activated when the BOOT pin is set to “Low” level at reset timing. (For normal operation mode, the BOOT pin is set to “High” level.)

Boot mode supports the UART boot using the TXD10/RXD10 ports.

Table 5 introduces pins used in Boot mode.

Table 5. Pin Description used in Boot Mode

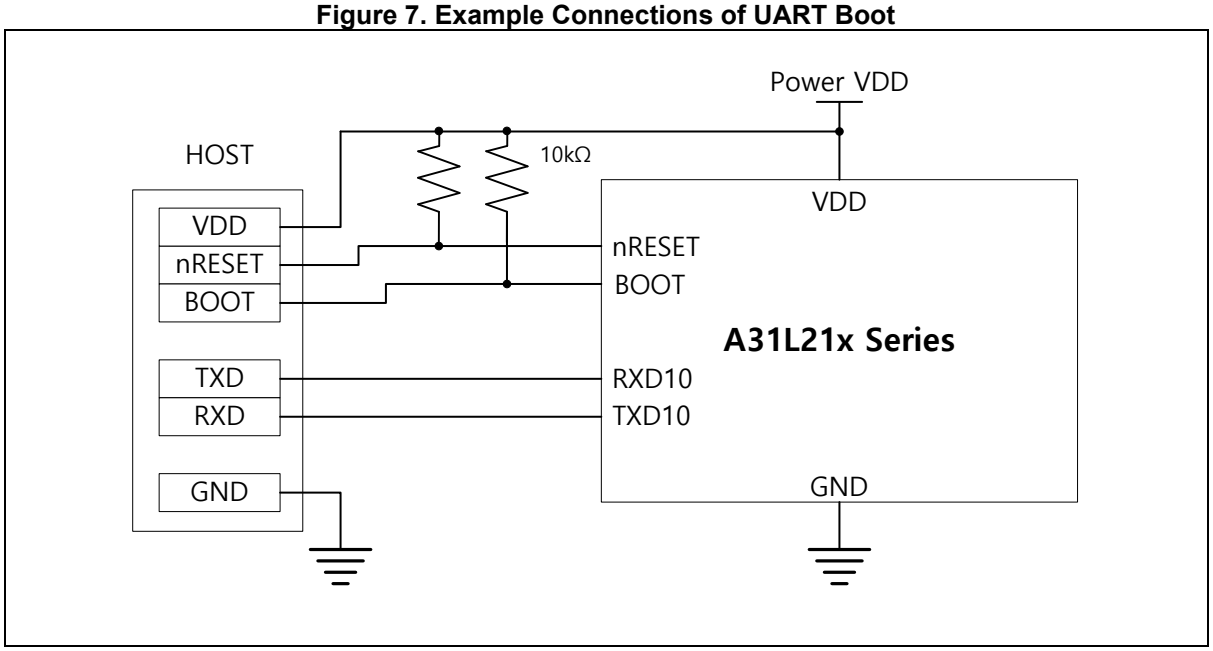
Block	Pin Name	Direction	Description
SYSTEM	nRESET	I	Reset Input signal
	BOOT/PD5	I	‘0’ to enter Boot mode
UART mode of USART10	RXD10/PA3	I	UART Boot Receive Data
	TXD10/PA2	O	UART Boot Transmit Data

3.3.2 Boot mode connections

Users can design the target board using Boot mode ports – UART mode of USART10.

Figure 7 shows an example diagram of connections in Boot mode.

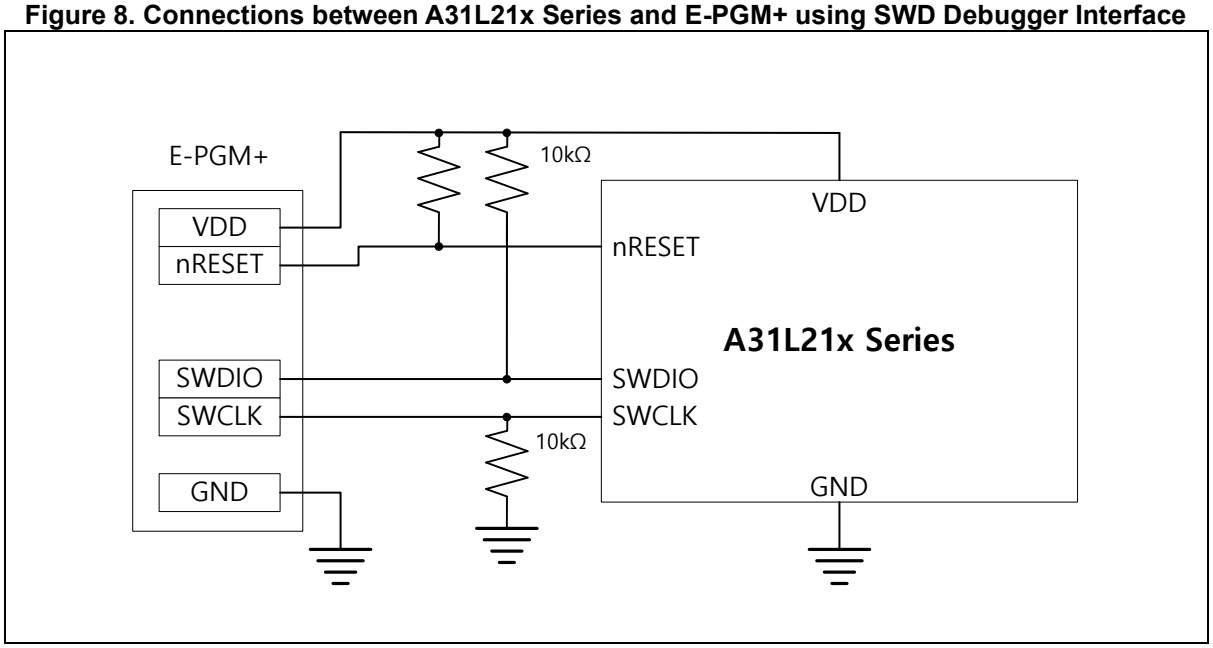
Figure 7. Example Connections of UART Boot



3.4 SWD debug mode and E-PGM+ connections

Figure 8 shows a diagram of connections for SWD debugger interface or E-PGM+.

Figure 8. Connections between A31L21x Series and E-PGM+ using SWD Debugger Interface

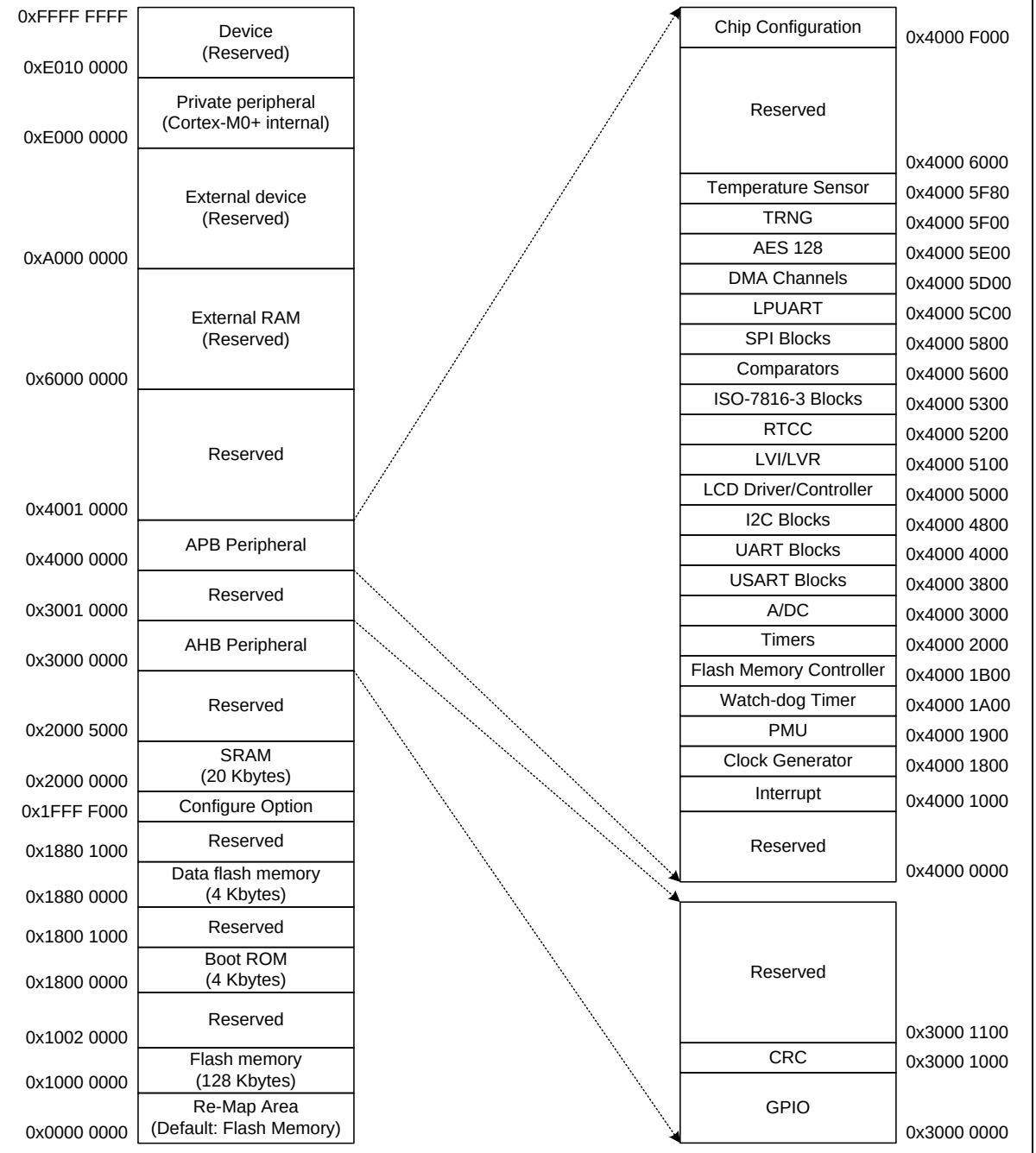


3.5 Memory organization

3.5.1 Memory map

Figure 9 shows addressable memory space in memory map.

Figure 9. Main Memory Map



NOTE: Access to the reserved area may cause a malfunction.

3.5.2 Internal SRAM

The A31L21x series has a block of 0-wait on-chip SRAM. Its size is 20KB, and its base address is 0x2000_0000. The SRAM's memory area is mainly used for data memory and stack memory. It is possible to locate code area in the SRAM memory for fast operation or for Flash erase or program operation for self-program.

This device does not support memory remapping. Therefore, the jump and return are required to process the code in SRAM memory area.

3.5.3 Flash memory

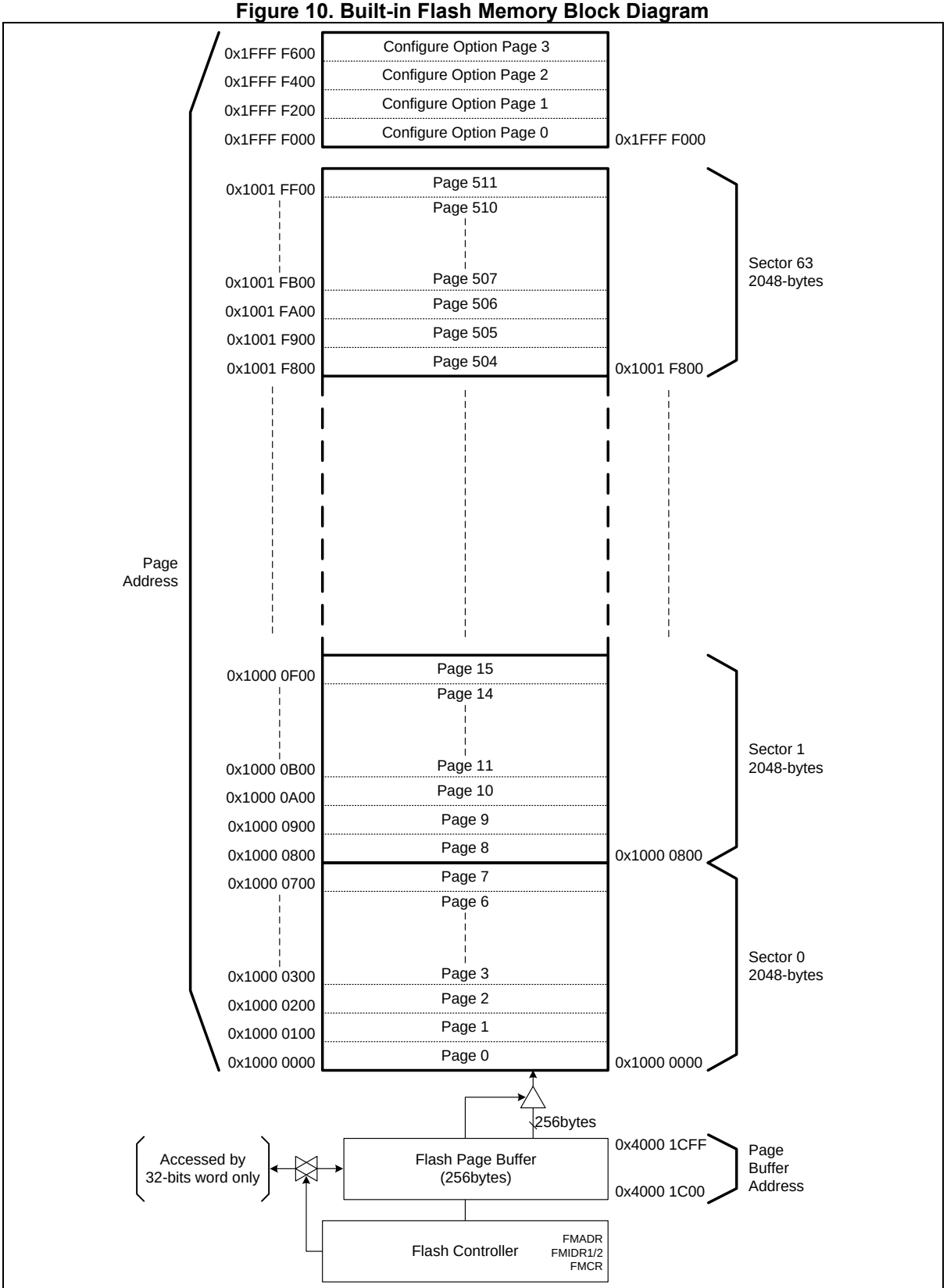
The A31L21x series has built-in Flash memory with the following features:

- 128 or 64KB Flash memory
- 32-bit wide read data bus
- 256-byte sized page
- Page erase and bulk erase
- programming in 256-byte units

Table 6. Built-in Flash Memory Specification

Item	Description
Size	128KB
Start address	0x1000_0000
End address	0x1001_FFFF
Page size	256-byte
Total page count	512 pages
PGM unit	256-byte
Erase unit	256-byte or bulk

Figure 10. Built-in Flash Memory Block Diagram



NOTES:

1. If an instruction of a size other than the 32-bit size is used to write data to the buffer, incorrect data is written.
2. Each of configure option pages (page0/1/2/3) is 256-byte size, respectively.

3.5.4 Data Flash memory

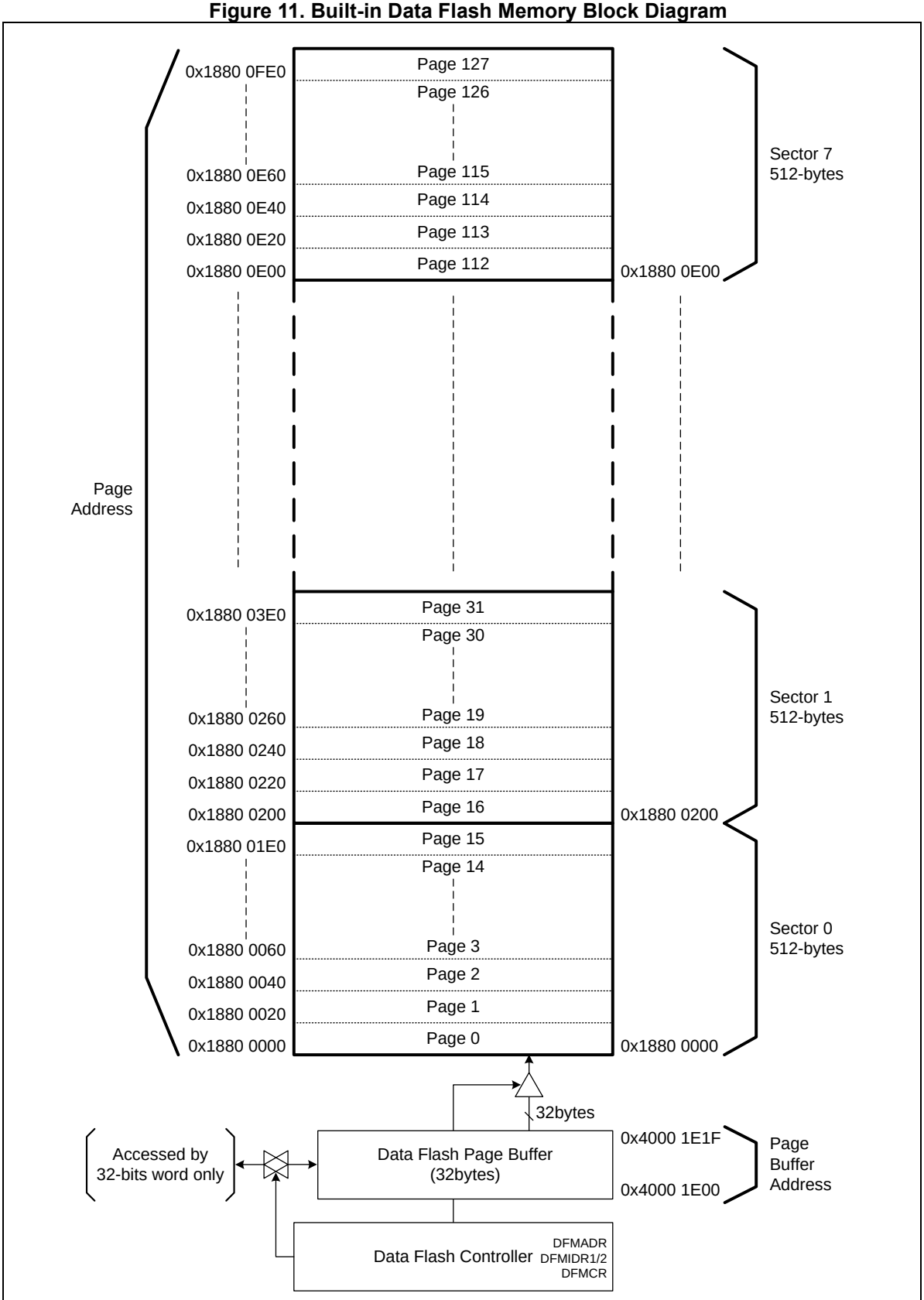
The A31L21x series has built-in Data Flash memory with the following features:

- 4KB Data Flash memory
- 32-bit wide read data bus
- 32-byte sized page
- Page erase and bulk erase
- Programming in 32-byte units

Table 7. Data Flash Memory Specification

Item	Description
Size	4KB
Start address	0x1880_0000
End address	0x1880_0FFF
Page size	32-byte
Total page count	128 pages
PGM unit	32-byte
Erase unit	32-byte or bulk

Figure 11. Built-in Data Flash Memory Block Diagram



NOTE: If an instruction of a size other than the 32-bit size is used to write data to the buffer, incorrect data is written.

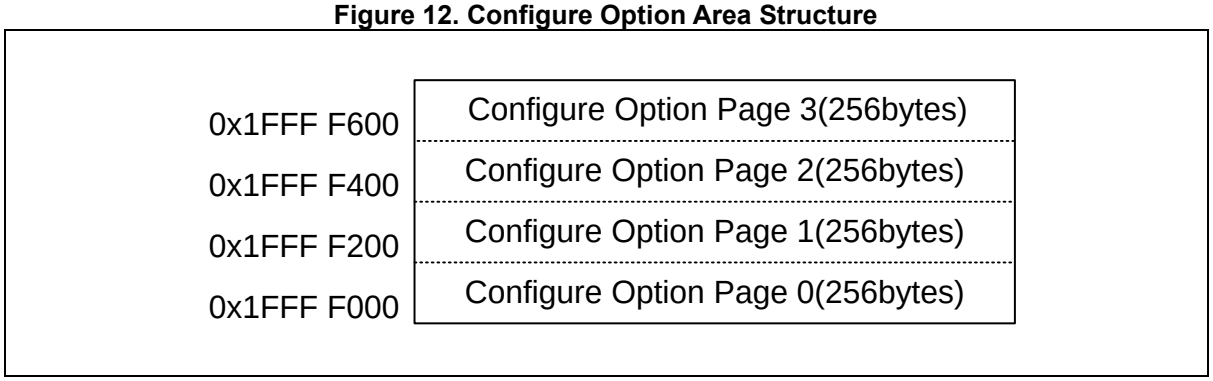
3.5.5 Configure option area

Configure option area of the A31L21x series is used for system related trimming values, user option, and user data. The configure option area consists of four pages in the Flash memory, which can be erased and written by the Flash memory controller. This area can be read by any instruction.

Four pages of the configure option area are listed below:

- Page 0: System related trimming values and 128-bit unique device ID registers
- Page 1: User option for Read Protection, Watchdog Timer, and LVR voltage level configurations
- Page 2: User data 0 area
- Page 3: User data 1 area

Figure 12. Configure Option Area Structure



3.5.5.1 Configure option pages

Base address of the configure option area ranges from 0x1FFF_F000 to 0x1FFF_F600.

The area map is shown in Table 8.

Table 8. Configure Option Area Map

Page	NAME	ADDRESS	DESCRIPTION
0	-	0x1FFF_F000 to 0x1FFF_F047 0x1FFF_F060 to 0x1FFF_F07F	System Trimming Values
	TS_FREQ_T30	0x1FFF_F048	Temperature Sensor Output Frequency acquired at 30℃ [Hz]
	TS_FREQ_T85	0x1FFF_F04C	Temperature Sensor Output Frequency acquired at 85℃ [Hz]
	TS_FREQ_T105	0x1FFF_F06C	Temperature Sensor Output Frequency acquired at 105℃ [Hz]
	CONF_MF1CNFIG	0x1FFF_F050	Manufacture Information 1 for 128-bit unique ID
	CONF_MF2CNFIG	0x1FFF_F054	Manufacture Information 2 for 128-bit unique ID
	CONF_MF3CNFIG	0x1FFF_F058	Manufacture Information 3 for 128-bit unique ID
	CONF_MF4CNFIG	0x1FFF_F05C	Manufacture Information 4 for 128-bit unique ID
1	CONF_RPCNFIG	0x1FFF_F200	Configuration for Read Protection
	CONF_WDTCNFIG	0x1FFF_F20C	Configuration for Watch-Dog Timer
	CONF_LVRCNFIG	0x1FFF_F210	Configuration for Low Voltage Reset
	CONF_CNFIGWTP1	0x1FFF_F214	Erase/Write Protection for configure option page 1/2/3
	CONF_FMWTP1	0x1FFF_F240	Erase/Write Protection 1 for Flash Memory
	CONF_FMWTP2	0x1FFF_F244	Erase/Write Protection 2 for Flash Memory
	CONF_DFMWTP1	0x1FFF_F270	Erase/Write Protection 1 for Data Flash Memory
2	-	0x1FFF_F400 to 0x1FFF_F4FF	User Data Area 0
3	-	0x1FFF_F600 to 0x1FFF_F6FF	User Data Area 1

4 System Control Unit (SCU)

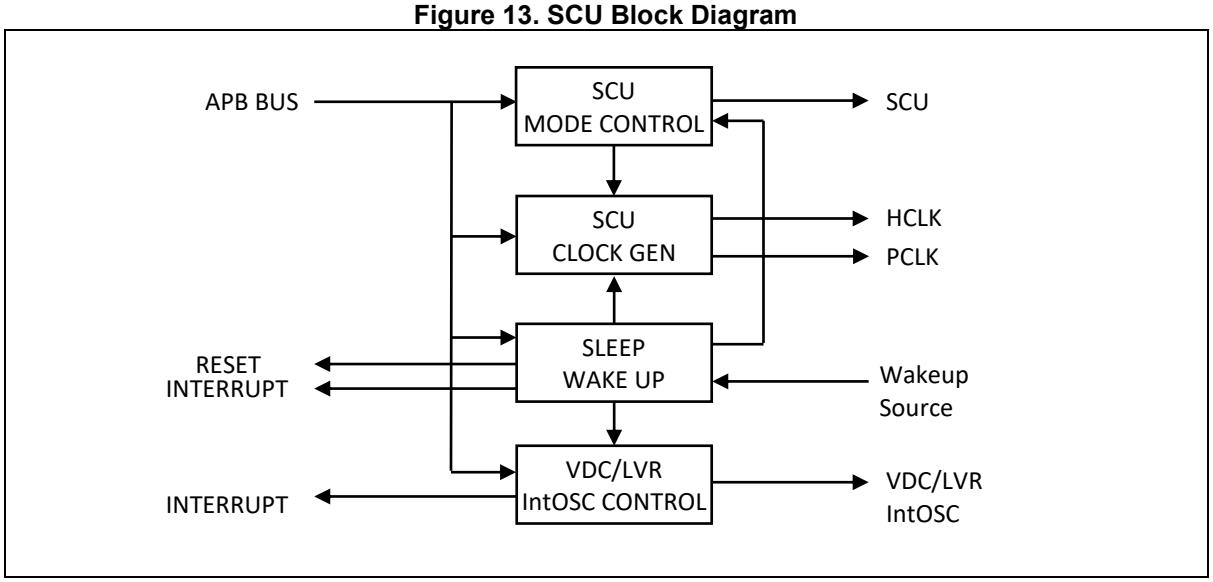
The A31L21x series has a built-in intelligent power control block, which manages analog blocks and operating modes.

This SCU block also controls internal reset and clock signals to maintain optimized system performance and power dissipation.

4.1 SCU block diagram

Figure 13 shows the SCU block diagram.

Figure 13. SCU Block Diagram

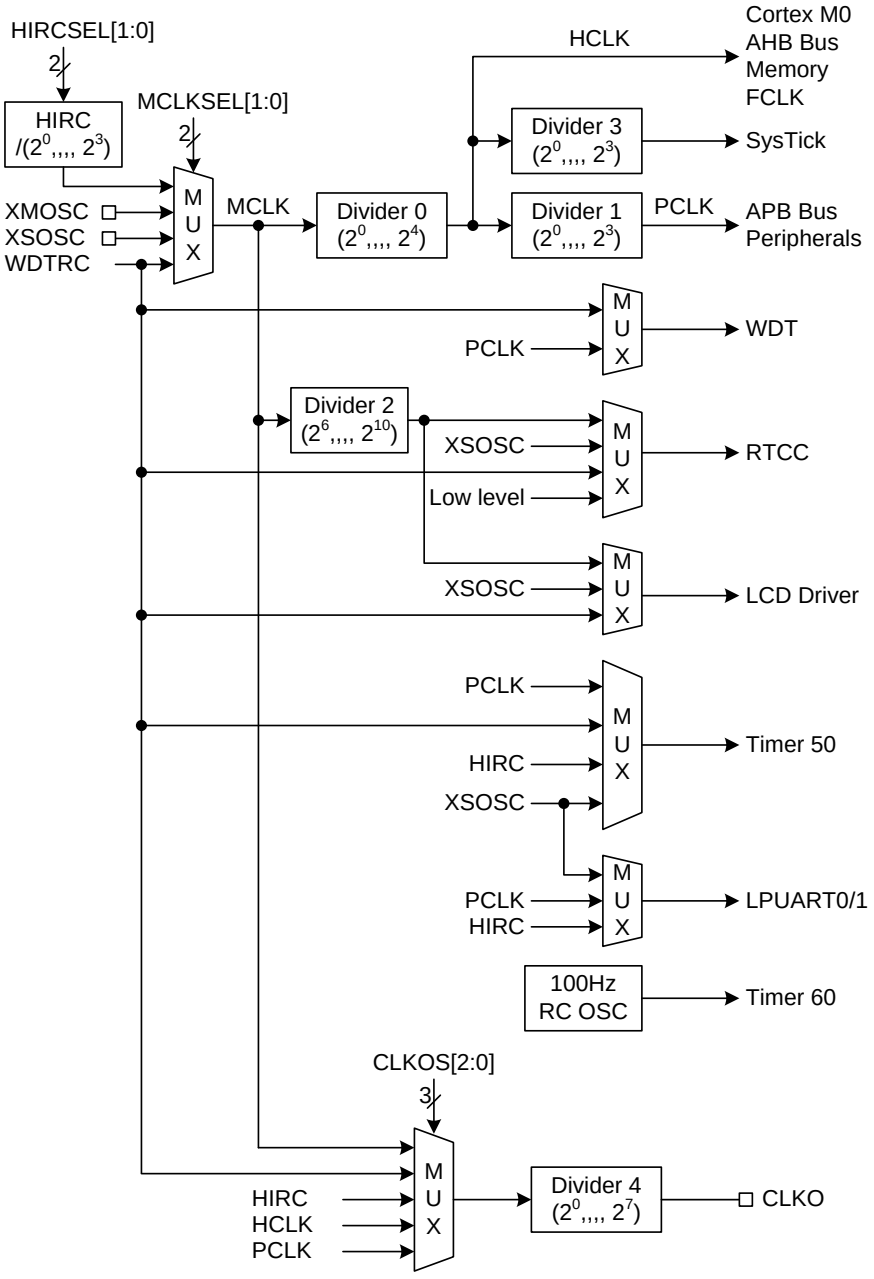


4.2 Clock system

The A31L21x series has two main operating clocks. One is the HCLK, which supplies clocks to the CPU and AHB bus system, and the other is the PCLK, which supplies clocks to the peripheral systems.

Users can control the clock system variation using software. Figure 14 shows the clock system of the A31L21x series and Table 9 shows the description for clock sources.

Figure 14. Clock Source Configuration



NOTE: If the WRCMF[11:0] bits of configuration are not equal to 0x96D, the WDTRC oscillation can't be disabled by the WDTRCEN bit of SCU_CLKSRCR register.

Each mux that switches the clock source has a glitch-free circuit. So a clock can be switched without glitch risks. When users change the clock mux control, be sure that both clock sources are alive. If either is not alive, the clock change operation stops and the system shuts down (and won't recover).

Table 9. Clock Sources

Clock name	Mnemonic	Frequency	Description
Main OSC	XMOSC	• X-TAL (2MHz to 16MHz) • External Clock (2MHz to 32MHz)	• External Main Crystal OSC • External Main Clock
Sub OSC	XSOSC	X-TAL (32.768kHz)	External Sub Crystal OSC
Internal RC OSC	HIRC	2MHz to 32MHz	High Frequency Internal RC OSC
WDT RC OSC	WDTRC	40kHz	Watchdog Timer RC OSC

4.2.1 HCLK clock domain

The HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks, FCLK and HCLK. The FCLK is a free running clock and is always running except during power down mode. The HCLK can be stopped during SLEEP mode.

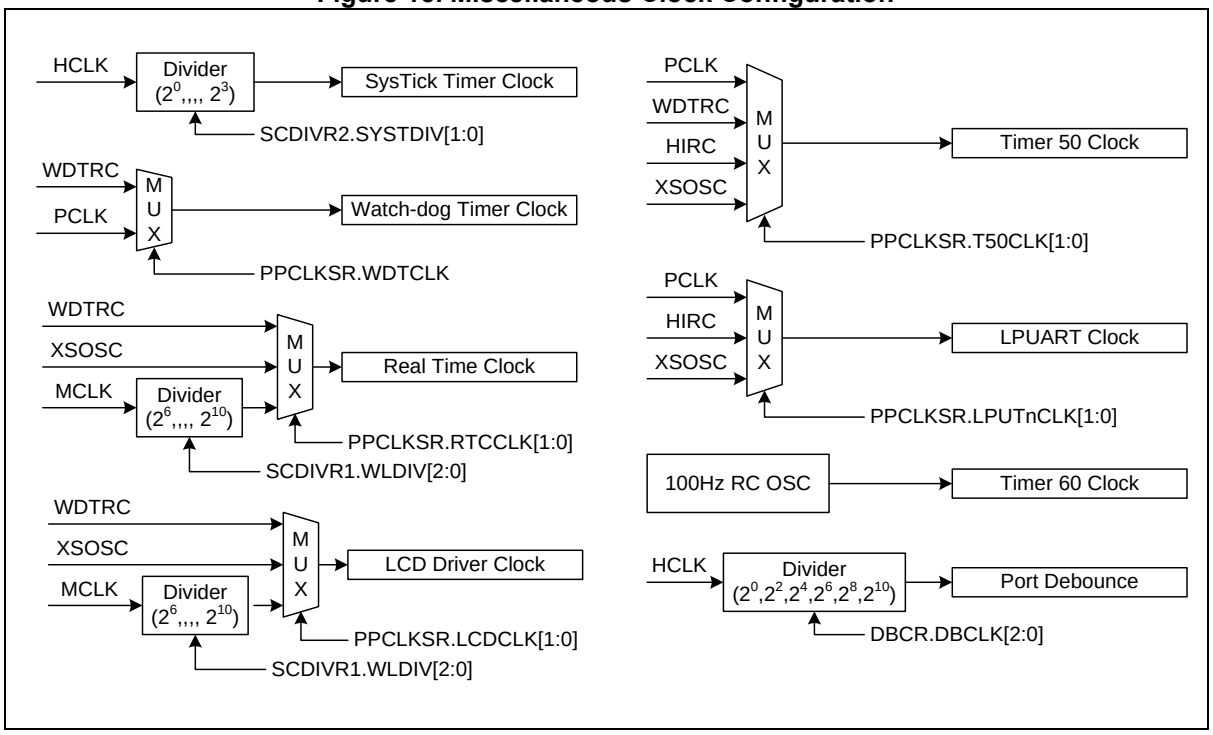
The HCLK clock operates the BUS system and memory systems. The maximum clock speed of the BUS operation is 32MHz. The HCLK frequency should be limited to 32MHz or lower.

4.2.2 Miscellaneous clock domain

Various clock sources are required for each functional block. The SCU provides clock source selectivity with dedicated pre-scaler for each functional block. The clock selection mux does not support glitch-free function, so the clock is unpredictable during clock selection.

Figure 15 shows the configurations of miscellaneous clocks.

Figure 15. Miscellaneous Clock Configuration



4.2.3 PCLK clock domain

The PCLK is the master clock for all peripherals except for the CRC generator and ports. It can shut down during power down modes. Each peripheral clock is generated by the SCU_PPCLKEN1 and SCU_PPCLKEN2 register set.

Figure 14 illustrates the PCLK clock distributions. Peripherals are not accessible until the PCLK clock of each block is enabled, and even by reading its registers.

4.2.4 Clock configuration procedure

When the device is powered on, a default system clock is generated by the HIRC (2MHz) clock. The HIRC is enabled by default during the power up sequence. Other clock sources are enabled by user controls and configuration options with a system clock.

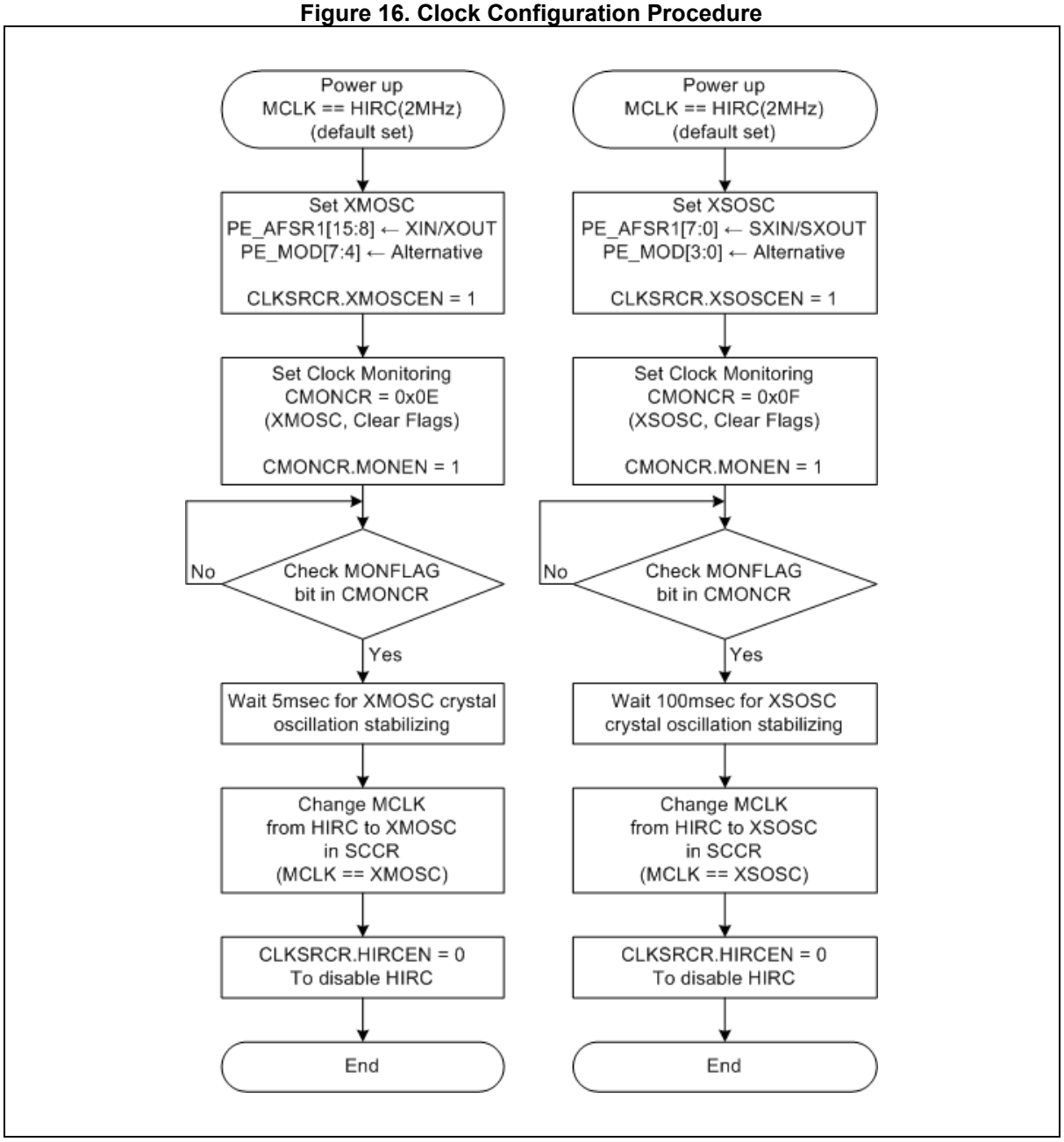
The XMOSC and XSOSC clocks are enabled by the XMOSCEN and XSOSCEN bits of the SCU_CLKSRCR register, respectively. Before enabling XMOSC and XSOSC blocks, the pin mux configuration should be set for XIN/XOUT and SXIN/SXOUT functions.

The PE2/PE3 and PE0/PE1 pins are shared by the XMOSC's XIN/XOUT function and XSOSC's SXIN/SXOUT function – The PE_MOD and PE_AFSR1 registers should be configured properly.

After enabling the XMOSC and XSOSC blocks, a user can check stability of crystal oscillation through the clock monitoring control register, SCU_CMONCR. It takes more than 1ms to ensure stable crystal oscillation before changing the system clock.

Figure 16 shows an example of a flow chart configuring the system clock as the XMOSC and XSOSC clocks.

Figure 16. Clock Configuration Procedure



4.3 Reset

The A31L21x series has two system resets. One is the cold reset by POR, which is effective during power up or down sequence, and the other is the warm reset, which is generated by several reset sources. The reset event makes the device to turn back to its initial state.

The cold reset has a single reset source (POR), and the warm reset has several reset sources listed below:

- nRESET pin
- WDT reset
- LVR reset
- MON reset
- S/W reset
- CPU request reset
- WAKUP3 reset

4.3.1 Cold reset

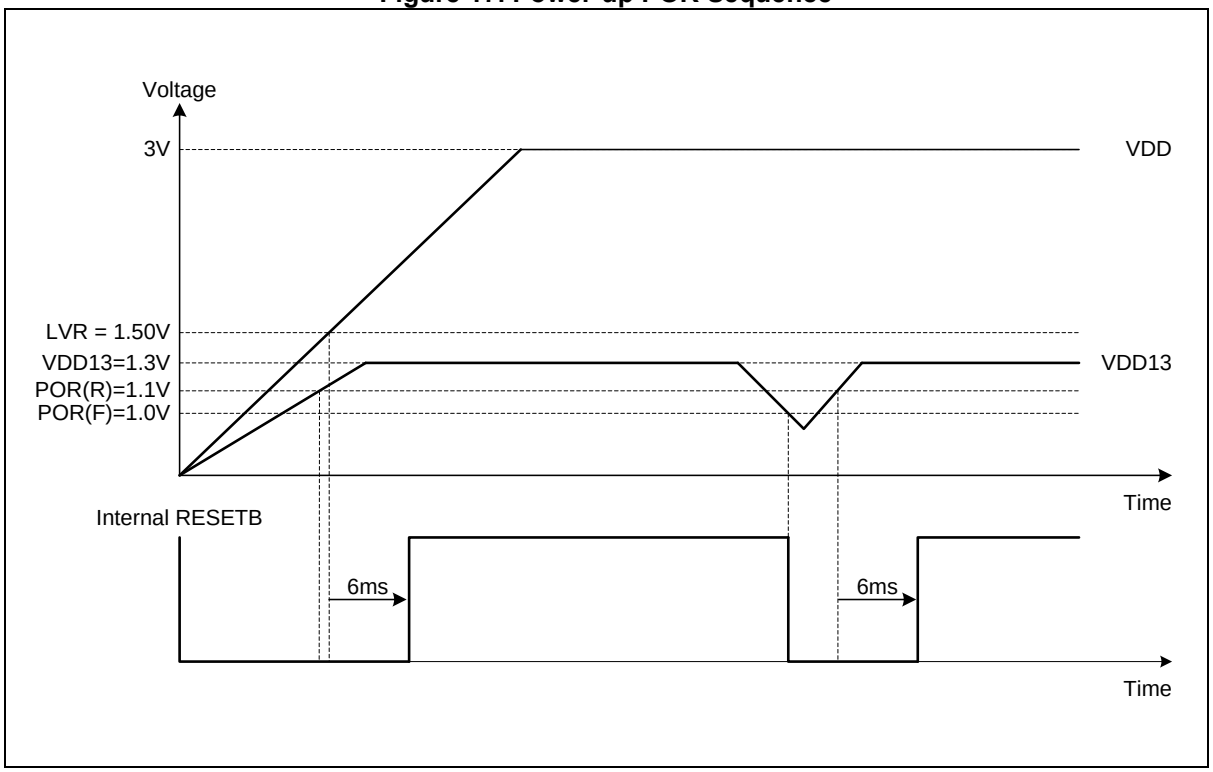
The cold reset is one of the important features of the A31L21x series when powered on. This characteristic globally affects the system boot.

The internal VDC is enabled when the VDD power is supplied. The internal VDD level slope follows the external VDD power slope.

The internal POR trigger level is at 1.1V of the internal VDC voltage. At this time, boot operation begins. The internal RC clock turns on and counts 6ms for the internal VDC level to stabilize. At this time, the external VDD voltage level should be bigger than the initial LVR level (1.50V). After 6ms of counting, the CPU reset is released and operation begins.

Figure 17 shows waveform of the power up sequence and internal reset.

Figure 17. Power-up POR Sequence



The register SCU_RSTSSR shows the POR reset status. The last reset comes from the POR.

The PORSTA bit in the SCU_RSTSSR register is set to ‘1’. After power on, this bit is always set to ‘1’ unless it is cleared by S/W. If abnormal internal voltage drop is detected during normal operation, the system is reset and this bit is set to ‘1’.

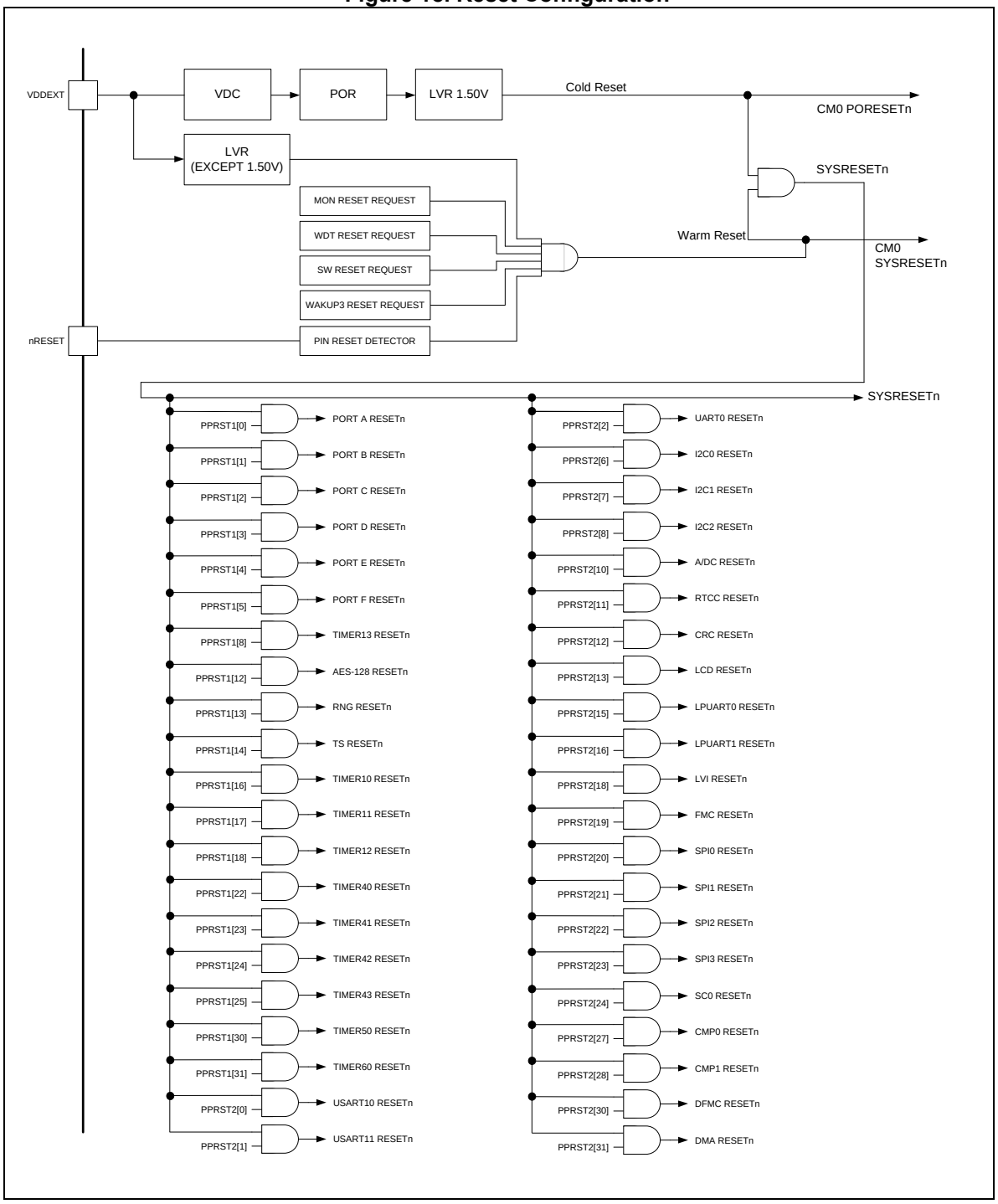
When the cold reset is applied, the entire device returns to its initial state.

4.3.2 Warm reset

The warm reset event has several reset sources and some parts of the device return to their initial states when the warm reset takes place.

The warm reset status appears in the register SCU_RSTSSR. A reset for each peripheral block is controlled by the register SCU_PPRST. The reset can be masked independently.

Figure 18. Reset Configuration

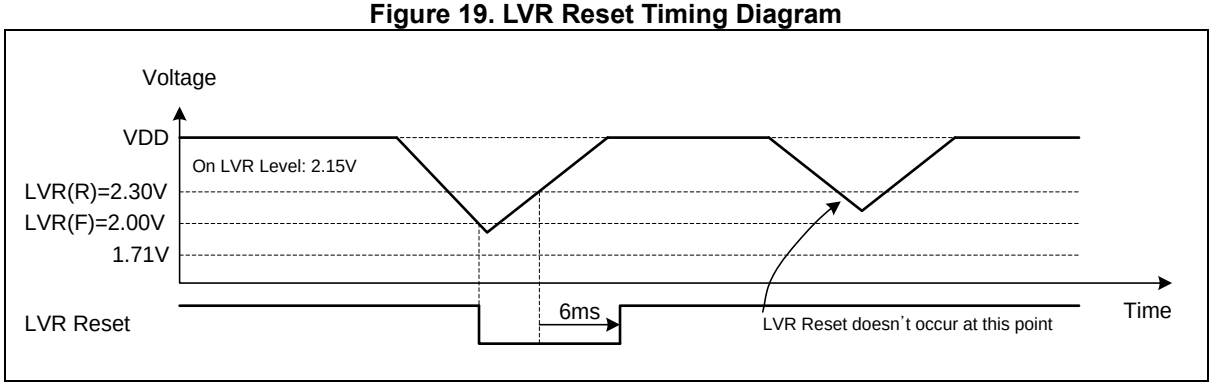


4.3.3 LVR reset

The LVR voltage level is set by a low voltage reset configuration register (CONF_LVRCNFIG) in the configure option page 1. The LVR reset status appears in the register SCU_RSTSSR.

The LVR reset is controlled by the register SCU_LVRCR. This register is cleared to “0x00” when the POR/WAKUP3 reset occurs.

Figure 19. LVR Reset Timing Diagram

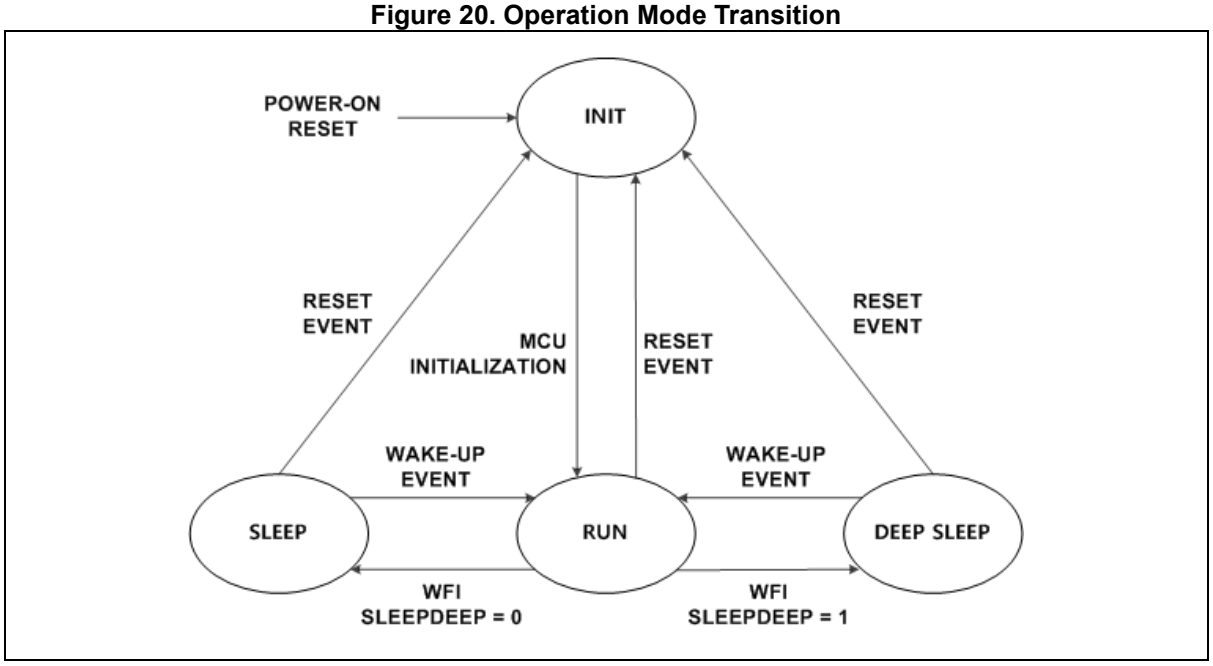


4.4 Operation mode

INIT mode is the initial state of the device when resetting. At RUN mode, the chip runs at its max CPU performance with a high-speed clock system. At SLEEP and DEEP SLEEP mode, the chip runs at a low power consumption mode. The system saves power by halting the processor core and unused peripherals.

Figure 20 shows a diagram of the operation mode transition.

Figure 20. Operation Mode Transition



4.4.1 RUN mode

This mode is to operate CPU core and peripheral hardware with a high-speed clock. The device enters the INIT state after resetting, and then enters the RUN mode.

4.4.2 SLEEP mode

In this mode, only the CPU is stopped. Each peripheral function is turned on by the function enable bit and the clock enable bit of the register SCU_PPCLKEN.

4.4.3 DEEP SLEEP mode

In this mode, not only the CPU but also a selected system clock (MCLK) are stopped. The RTCC with a sub clock, T60, and the Watchdog Timer with WDTRC still operate in DEEP SLEEP mode 0/1/2.

4.4.4 SHUT DOWN mode

In this mode (DEEP SLEEP mode 3), the CPU, a selected system clock (MCLK), and most of the peripherals are stopped. Only the T60 can operate in this mode.

4.5 Pins for SCU

Table 10. Pins and External Signals for SCU

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator for Main Clock
SXIN/SXOUT	OSC	External Crystal Oscillator for Sub Clock
CLKO	O	Clock Output Monitoring Signal

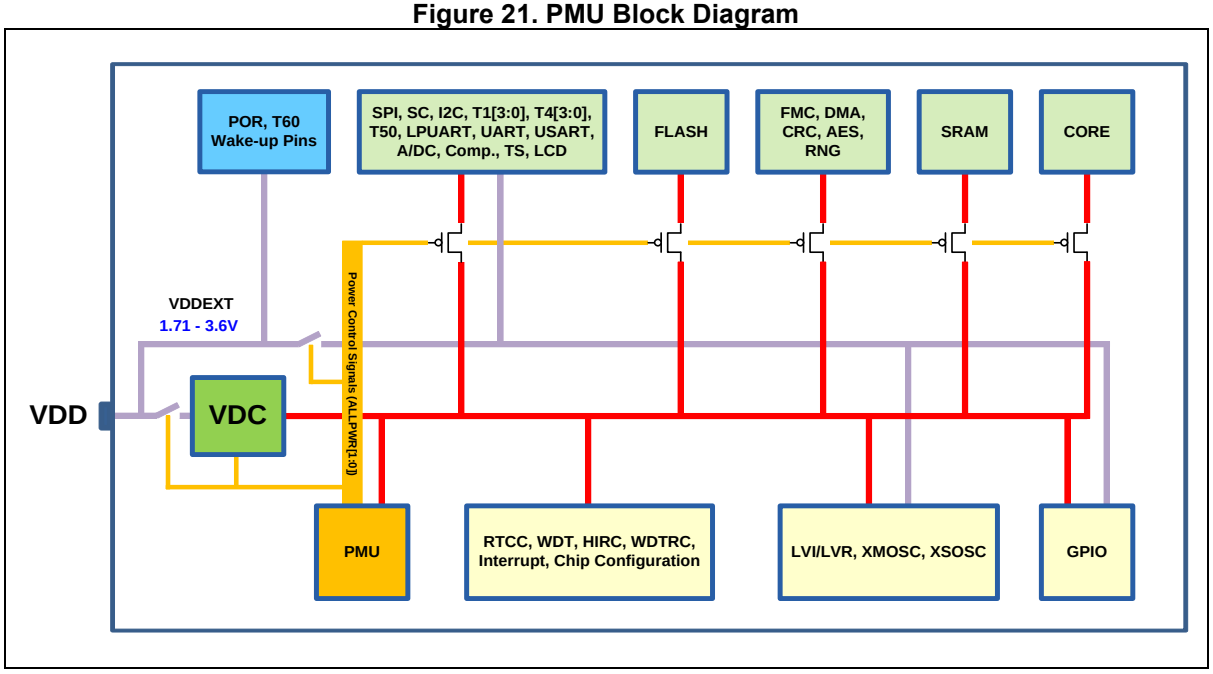
5 Power Management Unit (PMU)

The A31L21x series has a built-in Power Management Unit (PMU), which manages the internal power supply of the system control and peripheral parts and a wake-up time from SLEEP and DEEP SLEEP modes.

This PMU has 32-byte sized backup registers to retain data during DEEP SLEEP mode 0/1/2 except DEEP SLEEP mode 3 (SHUT DOWN mode).

5.1 PMU block diagram

Figure 21. PMU Block Diagram



6 Port Control Unit (PCU) and GPIO

The Port Control Unit (PCU) of the A31L21x series configures and controls external I/Os as shown below:

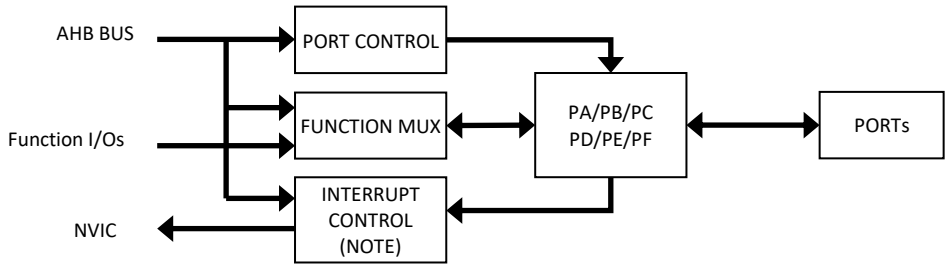
- Direction settings of the external signal on each pin
- Interrupt trigger mode settings for each pin
- Internal pull-up/down register control and open drain control settings

Most pins, except for dedicated function pins, can be used as GPIO (General Purpose I/O) ports. The GPIO block controls the GPIOs as shown below:

- Output signal level (H/L) selection
- External interrupt interface
- Pull-up/down enabling or disabling settings

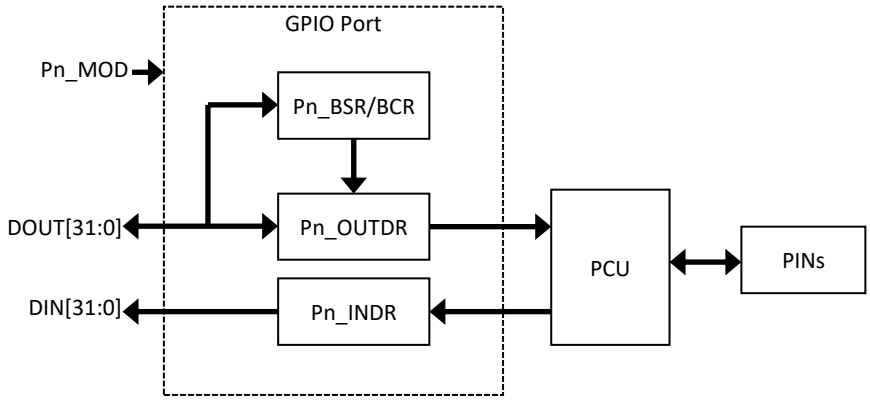
6.1 PCU and GPIO block diagrams

Figure 22. PCU Block Diagram



NOTE: Refer to the Chapter 3.2 Interrupt Controller.

Figure 23. GPIO Block Diagram



6.2 I/O port block diagram

Figure 24. I/O Port Block Diagram (General Purpose I/O Pins)

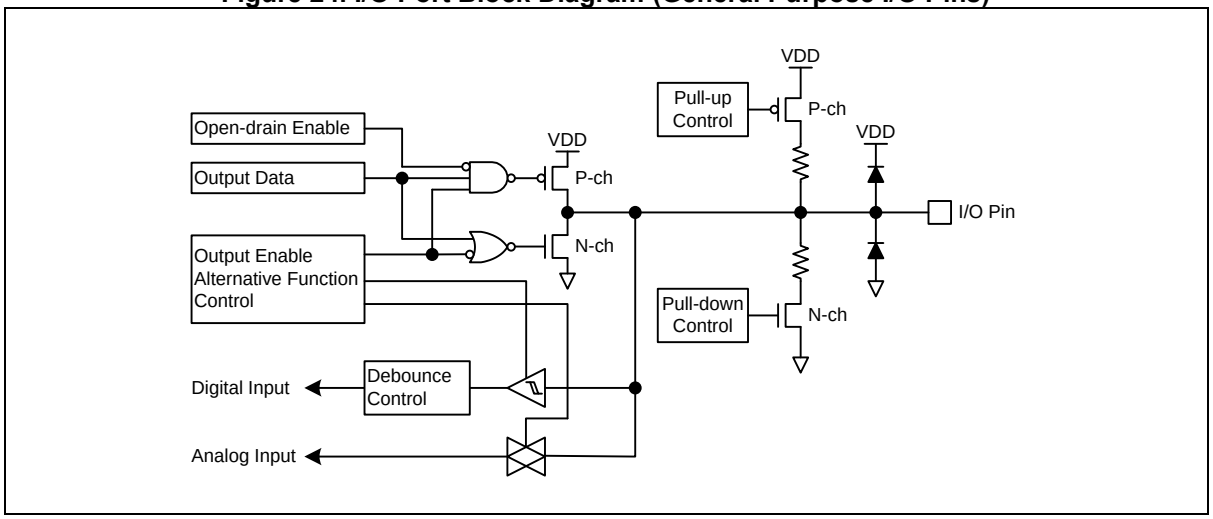
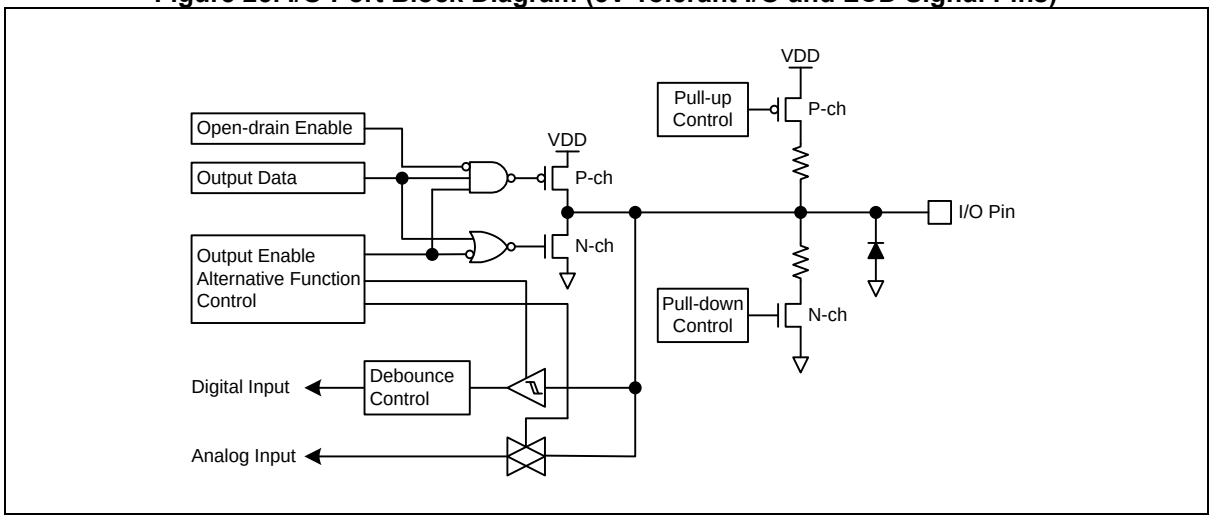


Figure 25. I/O Port Block Diagram (5V Tolerant I/O and LCD Signal Pins)



6.3 Pin multiplexing

The GPIO pins support alternative functions. Table 11 shows pin multiplexing information.

Table 11. GPIO Alternative Functions

Port	Pin	Function								
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PA	0	T40OUTA	T40INP	–	–	AN0	CP0N0	CP0OUT	SEG29	–
	1	T40OUTB	EC40	T42INP	SS10	AN1	CP0P0	–	SEG30	–
	2	T41OUTA	T41INP	TXD10	MOSI10	AN2	CP1N0	CP1OUT	SEG31	LPTXD0
	3	T41OUTB	EC41	RXD10	MISO10	AN3	CP1P0	ADTRG	SEG32	LPRXD0
	4	–	T43INP	SS1	SCK10	AN4	CP0N1	CP1N1	SEG33	LPDE0
	5	T40OUTA	T40INP	–	SCK1	AN5	CP0N2	CP1N2	SEG34	–
	6	T43OUTA	T43INP	–	MISO1	AN6	–	CP0OUT	SEG35	–
	7	T43OUTB	EC43	–	MOSI1	AN7	CP1P1	CP1OUT	SEG36	–
	8	–	–	LPTXD0	–	AN8	–	–	SEG37	–
	9	–	–	LPRXD0	–	AN9	–	–	SEG38	–
	10	–	–	–	SCK11	AN10	–	–	SEG39	–
	11	–	–	–	SS11	AN11	–	–	SEG40	–
	12	T40OUTA	T40INP	RXD11	MISO11	–	–	–	SEG41	–
	13	T40OUTB	EC40	TXD11	MOSI11	–	–	–	SEG42	–
	14	–	–	–	–	SCL1	–	–	SEG43	–
	15	–	–	–	–	SDA1	–	–	SEG44	–
PB	0	T11OUT	T11CAP	–	–	–	–	–	CAPL	–
	1	–	EC11	–	–	–	LPDE0	–	CAPH	–
	2	T50OUT	–	–	–	–	–	–	VLC3	–
	3	T41OUTA	T41INP	LPTXD1	–	SCL1	–	ADTRG	VLC2	–
	4	T41OUTB	EC41	LPRXD1	–	SDA1	–	ADTRG	VLC1	–
	5	–	–	–	SS0	–	LPDE1	–	VLC0	–
	6	T42OUTA	T42INP	CLKO	SCK0	SCL1	–	–	SEG10	–
	7	T42OUTB	EC42	RTCOUT	MISO0	SDA1	LPDE1	ADTRG	SEG9	–
	8	–	–	–	MOSI0	–	–	–	SEG8	–
	9	T43OUTA	T43INP	T10CAP	SS3	–	–	T10OUT	SEG3	–
	10	T43OUTB	EC43	EC10	SCK3	–	–	–	SEG2	–
	11	T43INP	–	T11CAP	MISO3	–	–	T11OUT	SEG1	–
	12	T42INP	–	EC11	MOSI3	–	SDA2	–	SEG0	–

Table 11. GPIO Alternative Functions (continued)

Port	Pin	Function							
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC	0	CLKO	T12CAP	–	–	SC0IN	SCL2	T12OUT	COM0
	1	CLKO	EC12	TXD0	–	SC0PWR	SCL0	–	COM1
	2	–	–	RXD0	SCK1	SC0CLK	SDA0	–	COM2/SEG11
	3	–	–	–	MISO1	SC0RST	SC0RXD	CP0OUT	COM3/SEG12
	4	–	–	–	MOSI1	SC0DATA	SC0TXD	CP1OUT	SEG13
	5	SWDIO	–	LPRXD1	–	–	–	–	–
	6	SWCLK	–	LPTXD1	–	–	–	–	–
	7	T40OUTA	T40INP	–	–	–	–	SS1	SEG14
	8	–	–	TXD10	MOSI10	SC0DATA	SC0TXD	–	SEG15
	9	–	–	RXD10	MISO10	SC0RST	SC0RXD	–	SEG16
	10	–	–	LPTXD1	SCK10	SC0CLK	–	–	COM4/SEG17
	11	–	–	LPRXD1	SS10	SC0PWR	–	–	COM5/SEG18
	12	–	–	TXD11	MOSI11	SC0IN	–	–	COM6/SEG19
	13	–	–	RXD11	MISO11	–	LPDE1	–	COM7/SEG20
PD	0	T40OUTB	EC40	SCL2	SCK1	MOSI11	CP1N3	–	TXD11
	1	T43OUTA	T43INP	SDA2	MISO1	MISO11	–	CP1P2	RXD11
	2	T43OUTB	EC43	EC50	MOSI1	SCK11	–	CP1P3	–
	3	–	–	TXD0	–	SS11	SCL0	CP1P4	–
	4	–	T50INP	RXD0	–	–	SDA0	CP1P5	–
	5	BOOT	–	RTCOUT	–	–	–	–	–
	6	T13OUT	T13CAP	–	–	SCL0	–	–	–
	7	–	EC13	–	SS0	SDA0	–	–	–
	8	T42OUTA	T42INP	–	SS0	–	–	–	SEG21
	9	T42OUTB	EC42	–	SCK0	–	–	–	SEG22
	10	T13OUT	T13CAP	–	MISO0	SCK11	–	–	SEG23
	11	–	EC13	–	MOSI0	SS11	–	–	SEG24

Table 11. GPIO Alternative Functions (continued)

Port	Pin	Function							
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE	0	SXIN	–	–	–	–	–	–	–
	1	SXOUT	–	–	–	–	–	–	–
	2	XIN	–	–	MOSI2	–	–	–	–
	3	XOUT	–	–	MISO2	–	–	–	–
	4	RTCOUT	–	–	SCK2	–	–	–	–
	5	–	–	–	SS2	–	–	–	–
	6	–	EC11	–	MOSI2	–	–	ADTRG	–
	7	T11OUT	T11CAP	–	MISO2	–	–	–	–
	8	–	EC10	–	SCK2	–	–	–	–
	9	T10OUT	T10CAP	–	SS2	–	–	–	–
PF	0	–	EC50	LPRXD0	–	AN12	SCL2	–	SEG25
	1	T50OUT	–	LPTXD0	SCK0	AN13	SDA2	–	SEG26
	2	–	T50INP	–	MISO0	AN14	LPDE0	–	SEG27
	3	–	–	–	MOSI0	AN15	–	–	SEG28
	4	T12OUT	T12CAP	–	MOSI3	–	SCL2	–	SEG4
	5	–	EC12	–	MISO3	–	SDA2	–	SEG5
	6	T13OUT	T13CAP	–	SCK3	–	–	–	SEG6
	7	–	EC13	–	SS3	–	LPDE1	–	SEG7

NOTES:

1. The PC[13:10] and PC[3:2] are automatically configured as common or segment signal according to the duty of the LCD control register when the pins are selected as alternative functions for common/segment.
2. The SWCLK and SWDIO pins shouldn't be changed as other alternative functions by software during the pins are connected with debugger host.
3. The VDD should be greater than or equal to 2.0V if the CP1N3, CP1P2, CP1P3, CP1P4, and CP1P5 are used as comparator pins for alternative function.

7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) quickly detects the CPU malfunctions such as endless loops caused by noise, and recovers the CPU to the normal state. The WDT signal for detecting the malfunction can be used as either a CPU reset or an interrupt request.

When the WDT is not used for detecting malfunction, it can be used as a timer to generate interrupts at fixed time intervals. When the WDT_CNT value reaches the WDT_WINDR value, a watchdog interrupt can be generated.

The underflow time of the WDT can be set by configuring the WDT_DR register. If the underflow occurs, an internal reset may be generated.

The WDT operates at a 40kHz clock of the embedded RC oscillator.

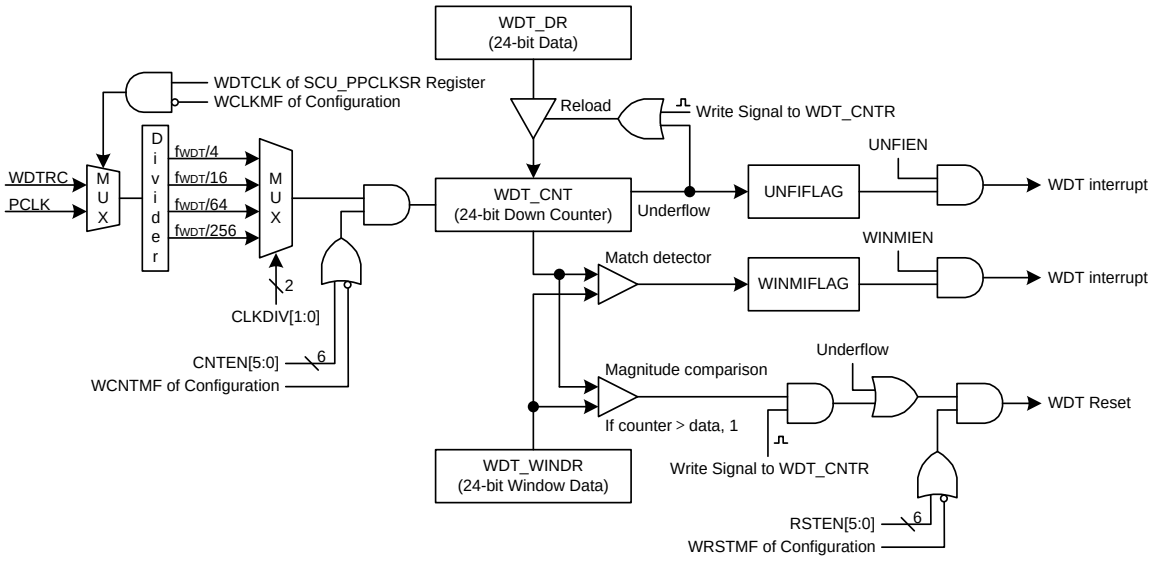
The WDT operations are listed below:

- 24-bit down counter (WDT_CNT)
- Reset or periodic interrupt selection
- Count clock selection
- Watchdog overflow output signal generation
- Counter window function

7.1 WDT block diagram

Figure 26 shows a block diagram of the WDT.

Figure 26. WDT Block Diagram



NOTE: When a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register, after 1-clock delay, with the clock selected by the CLKDIV bits.

8 Real Timer Clock and Calendar (RTCC)

The Real Timer Clock and Calendar (RTCC) has a function for RTC (Real Time Clock) and calendar operations.

The internal structure of the RTCC is implemented with the clock source select circuit, second/minute/hour/day/week/month/year counter circuits, alarm circuit, output select circuit, and error correction circuit.

The RTCC is an independent BCD counter. The RTCC circuitry and the related control bits are not reset by the system reset other than the POR/WAKUP3.

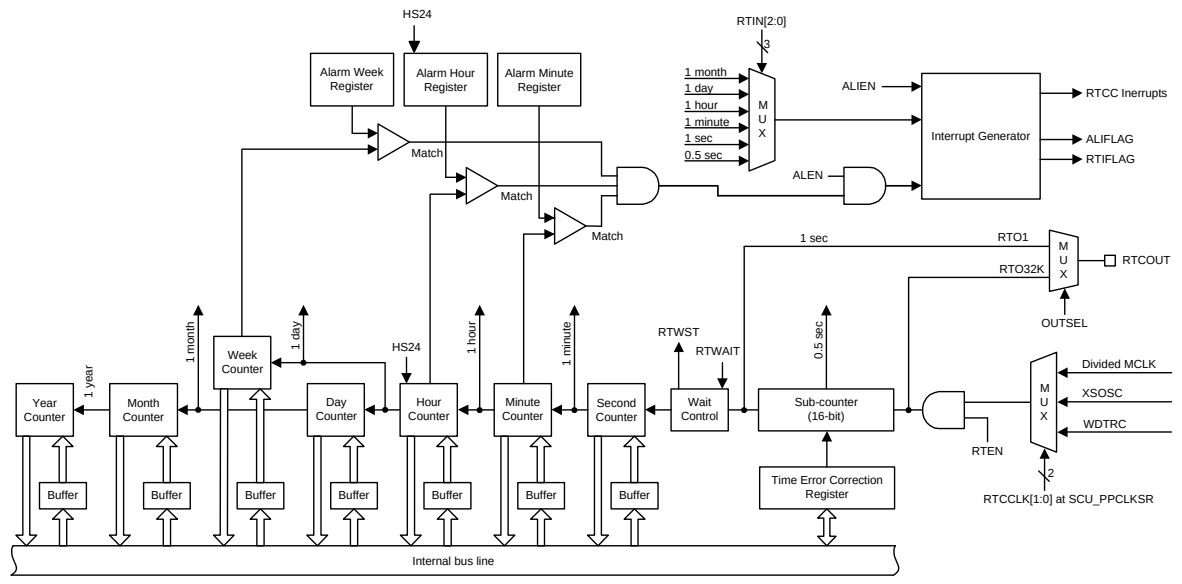
The main operations of the RTCC include the followings:

- Calendar counting 0.5 seconds, seconds, minutes, hours, days, weeks, months, and years up to the year 2099
- Time error correction function
- Alarm function with interrupt
- Wake-up possibility from DEEP SLEEP mode

8.1 RTCC block diagram

Figure 27 shows a block diagram of the RTCC.

Figure 27. RTCC Block Diagram



NOTE: Time in the block diagram is based on 32.768 kHz.

9 Timer counters

9.1 Timer counter 10/11/12/13

The timer block comprises 4 channels of 16-bit general purpose timers. Each has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. They support periodic timer, PWM pulse, one-shot and capture mode. Optionally, one more free-run timer is provided.

The main purpose of this timer is a periodical tick timer or a wake-up source.

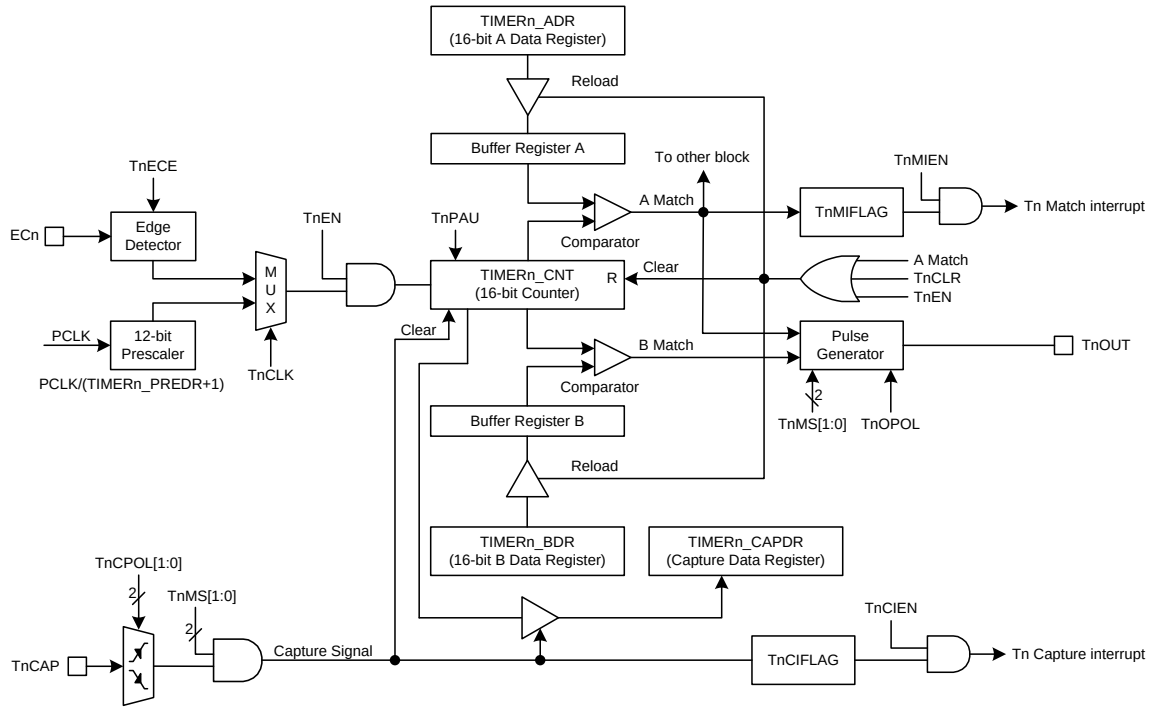
The timer counters 10/11/12/13 feature the followings:

- 16-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function

9.1.1 Timer counter 10/11/12/13 block diagram

Figure 28 shows a block diagram of the timer block unit.

Figure 28. Timer Counter n Block Diagram (n = 10, 11, 12, and 13)



NOTES:

1. The TnEN bit is automatically cleared to logic “0b” after one pulse is generated in PPG one-shot mode.
2. After the TnEN bit is set, counting of the TIMERn_CNT may be delayed 2 clocks or more.

9.1.2 Pin description for timer counter 10/11/12/13

Table 12. Pins and External Signals for Timer Counter n (n = 10, 11, 12, and 13)

Pin name	Type	Description
ECn	I	External clock input
TnCAP	I	Capture input
TnOUT	O	PWM/one-shot output

9.2 Timer counter 40/41/42/43

Each of the Timer counters 40/41/42/43 is a 16-bit general purpose timer with two outputs. It has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. It supports periodic timers, PWM pulses, one-shot and capture modes.

The main purpose of this timer is to work as a periodical tick timer or to provide a wake-up source.

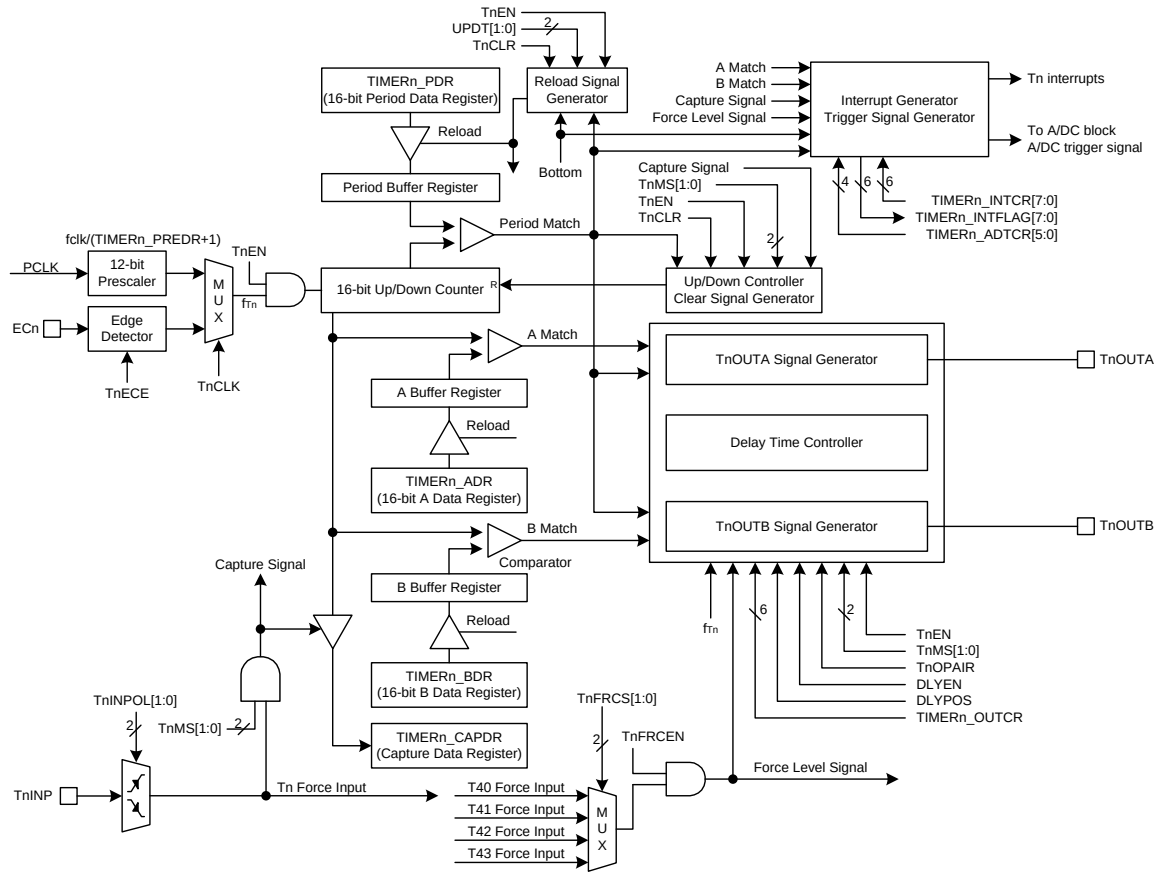
The operations of the timer counters 40/41/42/43 include the followings:

- 12-bit prescaler and 16-bit up-counter
- Interval timer, One-shot timer, Back-to-back, and Capture modes
- Counter sharing function to connect each other
- Synchronous start and clear function

9.2.1 Timer counter 40/41/42/43 block diagram

Figure 29 shows a block diagram of the timer block unit.

Figure 29. Timer Counter n Block Diagram (n = 40, 41, 42, and 43)



NOTES:

1. Period/A/B match interrupts except for bottom can occur in interval mode.
2. Period match interrupt only can occur in capture mode.
3. 16-bit up/down counter in capture mode is cleared to “0000H” after the counter value is loaded to the TIMERn_CAPDR register at a valid edge.
4. The TnEN bit is automatically cleared to logic “0b” after one pulse is generated at one-shot interval mode.
5. After the TnEN bit is set, the counting of the TIMERn_CNT may be delayed by 2 clocks or more.
6. The high/low level width of the ECn clock should be longer than the PCLK clock period.

9.2.2 Pins for timer counter 40/41/42/43

Table 13. Pins and External Signals for Timer Counter n (n = 40, 41, 42, and 43)

Pin name	Type	Description
ECn	I	External clock input
TnINP	I	Capture or force input
TnOUTA	O	Timer A output
TnOUTB	O	Timer B output

9.3 Timer counter 50

A timer block includes a single channel 16-bit general purpose timer. This timer has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode. Additional free-run timer is optionally provided.

Main purpose of this timer is to work as a periodical tick timer or to provide a wake-up source.

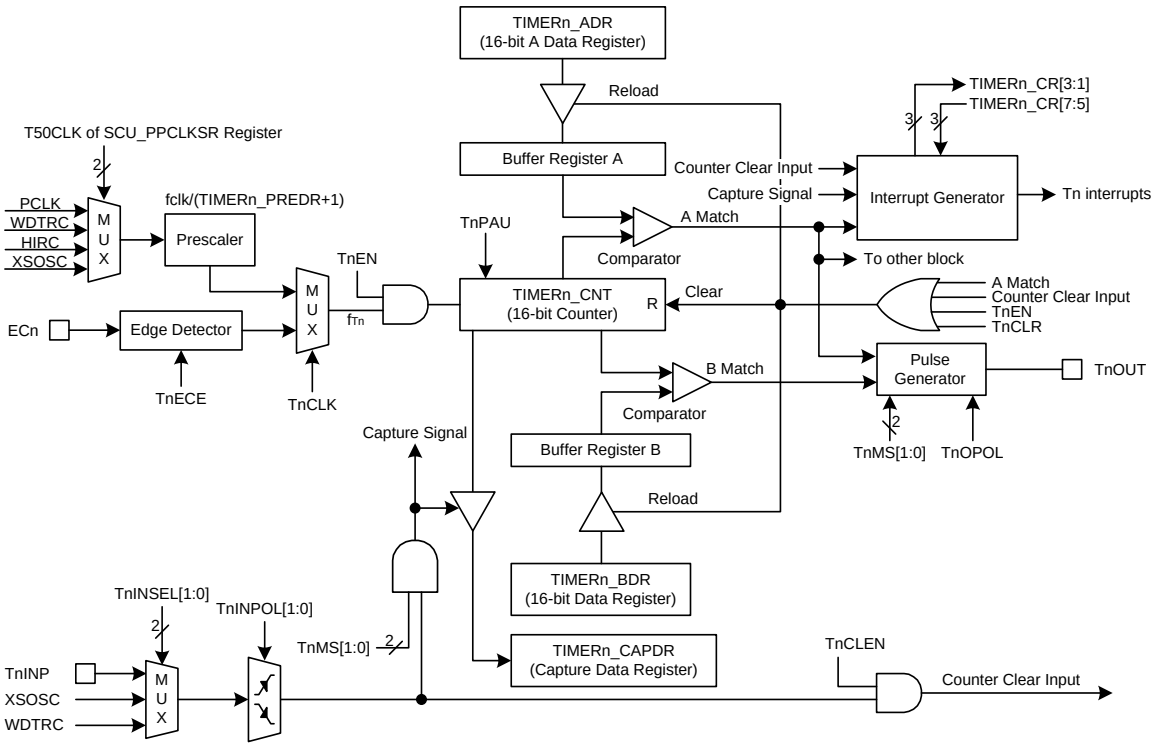
The timer counter 50 features the followings:

- 16-bit up-counter and 8-bit prescaler
- Interval timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function
- Low power operation with WDTRC or XSOSC

9.3.1 Timer counter 50 block diagram

Figure 30 shows a block diagram of the timer block unit.

Figure 30. Timer Counter n Block Diagram (n = 50)



NOTES:

1. TnEN is automatically cleared to logic ‘0’ after one pulse is generated in PPG one-shot interval mode.
2. After the TnEN bit is set, the counting of the TIMERn_CNT may be delayed by 2 clocks or more.
3. The counter clear input can control the wake-up operation in SLEEP mode by suppressing A-match interrupt.
4. The high/low level width of the ECn clock should be longer than the PCLK clock period.
5. The capture and counter clear input interrupts cannot be used as a wake-up source in DEEP SLEEP mode. That is, these interrupts will not be generated in DEEP SLEEP mode.

9.3.2 Pins for timer counter 50

Table 14. Pins and External Signals for Timer Counter 50 (n = 50)

Pin name	Type	Description
ECn	I	External clock input
TnINP	I	Capture/Clear input
TnOUT	O	PWM/one-shot output

9.4 Timer counter 60

A timer block includes a single channel 16-bit general purpose timer. This timer has an independent 16-bit counter and 100Hz RC oscillator that feeds a counting clock. It supports only a periodic timer.

Main purpose of this timer is to provide a wake-up source in DEEP SLEEP mode 3 (SHUT DOWN).

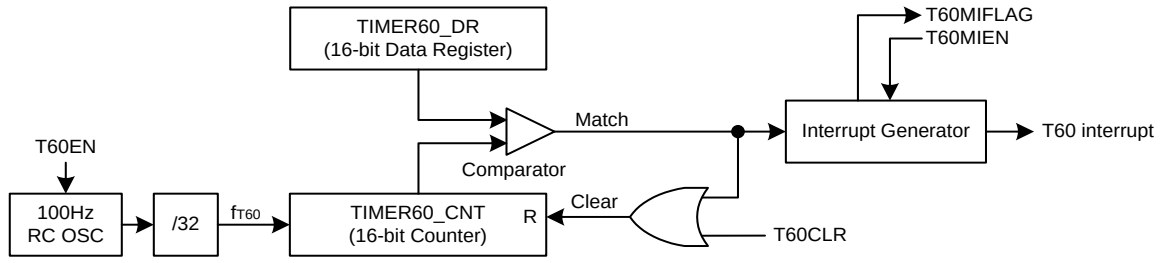
The timer counter 60 features the followings:

- 16-bit up-counter and interval timer mode
- Synchronous start and clear function
- Low power operation with an internal 100Hz RC oscillator

9.4.1 Timer counter 60 block diagram

Figure 31 shows a block diagram of the timer counter 60.

Figure 31. Timer Counter 60 Block Diagram



NOTES:

1. The TIMER60_DR register must be written while the timer counter 60 is disabled.
2. This timer is primarily intended to be used as a wake-up source in DEEP SLEEP mode 3 (SHUT DOWN).
3. When this timer is used in RUN mode, pay attention to the frequency deviation of 100Hz RC oscillator.

10 High speed 12-bit ADC

Analog-to-Digital Converter (ADC) of the A31L21x series allows conversion of an analog input signal to a corresponding 12-bit digital value. Its A/D module has sixteen analog inputs as shown in Figure 32.

Output of the multiplexer is the input into the converter, which generates the result through successive approximation.

The A/D module includes seven registers: control register (ADC_CR), data register (ADC_DR), prescaler data register (ADC_PREDR), oversampling control register (ADC_OVSCR), interrupt enable and status register (ADC_IESR), sampling time register (ADC_SAMR), and channel selection register (ADC_CHSELR).

The A/D module supports single, sequential, and continuous conversion modes.

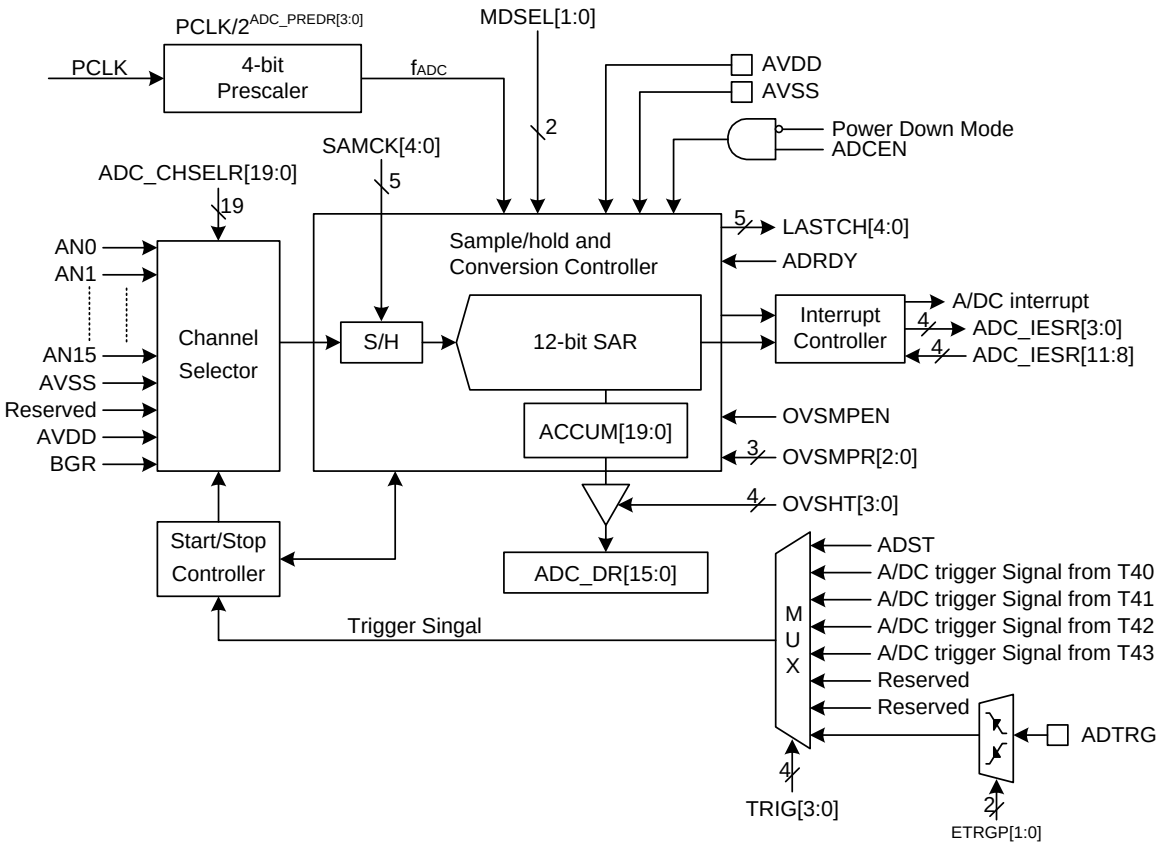
Main features of the ADC are listed in the followings:

- 16-channel of analog inputs
- S/W (ADST), timer trigger (T40/41/42/43 ADC trigger signal), and external trigger supported
- Conversion time: Up to 1us with 12 clocks + at least 4 sample/hold clocks
- 4-bit Prescaler and 16-bit data registers
- Up to 256 over sampling
- Single, sequential, and continuous conversion modes

10.1 12-bit ADC block diagram

Figure 32 shows a block diagram of the ADC block.

Figure 32. 12-bit ADC Block Diagram



NOTE: The external trigger input signal, ADTRG, should be slower than a system clock frequency.

10.2 Pins for 12-bit ADC

Table 15. Pins and External Signals for 12-bit ADC

Pin name	Type	Description
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14
AN15	A	ADC Input 15
AVSS	AP	Analog GND
AVDD	AP	Analog Power

NOTE: A=Analog, AP= Analog Power

11 Comparator 0/1

The A31L21x series includes two comparator modules.

Each comparator module has three registers: control register (CMP_CR), status register (CMP_SR), and reference control register (CMP_RCR). This comparator module has an internal reference circuit too.

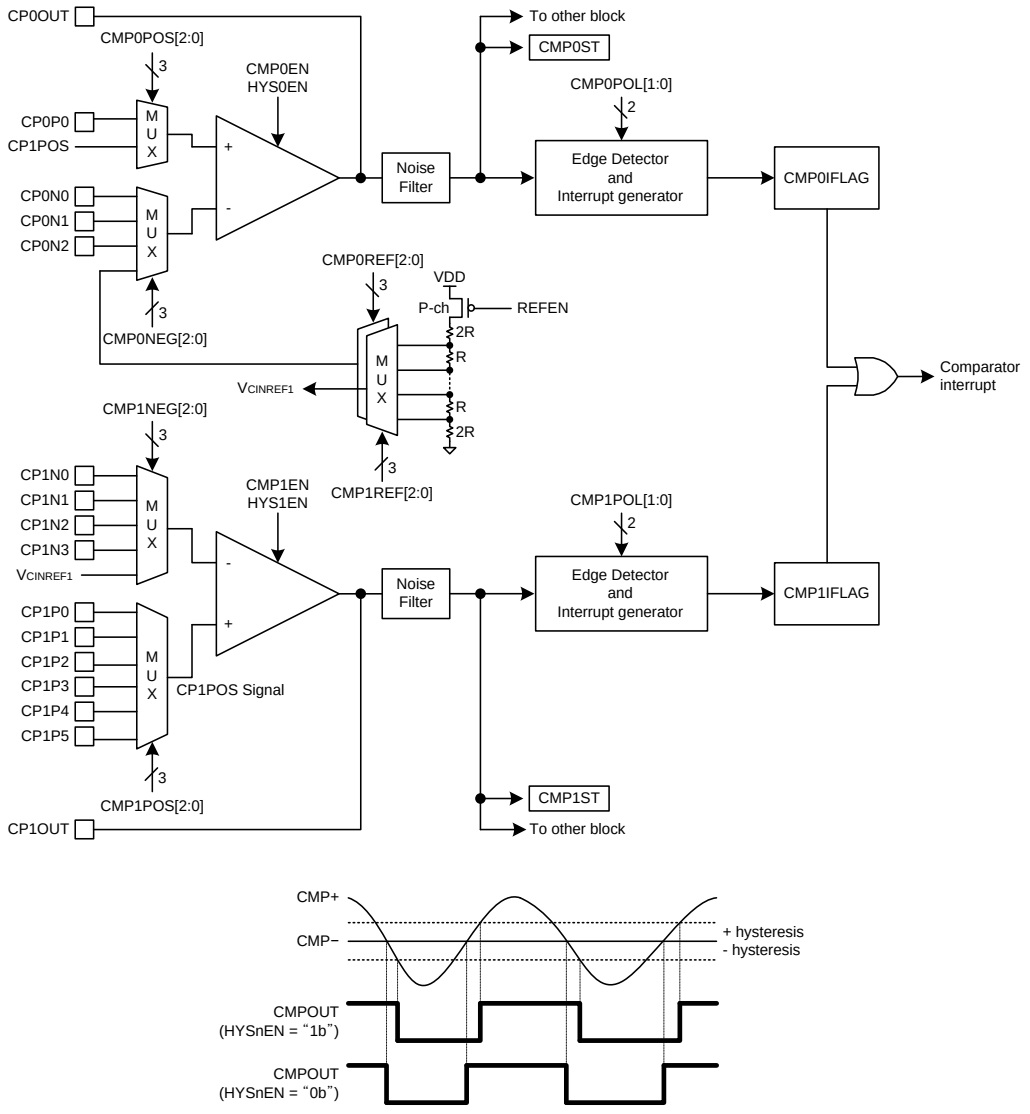
The comparator module features the followings:

- External analog inputs
- Hysteresis function
- Low and fast speed selectable
- Wake-up possible from DEEP SLEEP mode

11.1 Comparator 0/1 block diagram

Figure 33 shows a block diagram of the comparator block.

Figure 33. Comparator 0/1 Block Diagram



NOTE: The VDD should be greater than or equal to 2.0V and the corresponding pins are set to push-pull output by the PD_TYP[4:0] bits if the CP1P[5:2] and CP1N3 are used as comparator pins for the alternative function.

11.2 Pins for comparator 0/1

Table 16. Pins and External Signals for Comparator 0/1

Pin name	Type	Description
CP0P0	A	Comparator 0 positive input
CP0N0	A	Comparator 0 negative input
CP0N1	A	Comparator 0 negative input
CP0N2	A	Comparator 0 negative input
CP0OUT	A	Comparator 0 output
CP1P0	A	Comparator 1 positive input
CP1P1	A	Comparator 1 positive input
CP1P2	A	Comparator 1 positive input
CP1P3	A	Comparator 1 positive input
CP1P4	A	Comparator 1 positive input
CP1P5	A	Comparator 1 positive input
CP1N0	A	Comparator 1 negative input
CP1N1	A	Comparator 1 negative input
CP1N2	A	Comparator 1 negative input
CP1N3	A	Comparator 1 negative input
CP1OUT	A	Comparator 1 output

12 USART 10/11, UART 0, and LPUART 0/1

12.1 USART 10/11

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device.

The USART 10/11 of the A31L21x series features the followings:

- Full duplex operation. (independent serial receive and transmit registers)
- Asynchronous or synchronous operation
- Baud rate generator
- Supports serial frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or even parity generation, and parity check supported by hardware.
- Supports receive character detection and receive time out function
- Supports Local Interconnection Network (LIN)
- Data OverRun Detection
- Framing Error Detection
- Three separate interrupts on TX completion, TX data register empty and RX completion
- Double Speed Asynchronous communication mode
- Up to 16MHz data transfer for SPI

12.1.1 USART 10/11 block diagram

Figure 34 shows a block diagram of the UART block.

Figure 34. UART Block Diagram of USART and LIN (n = 10 and 11)

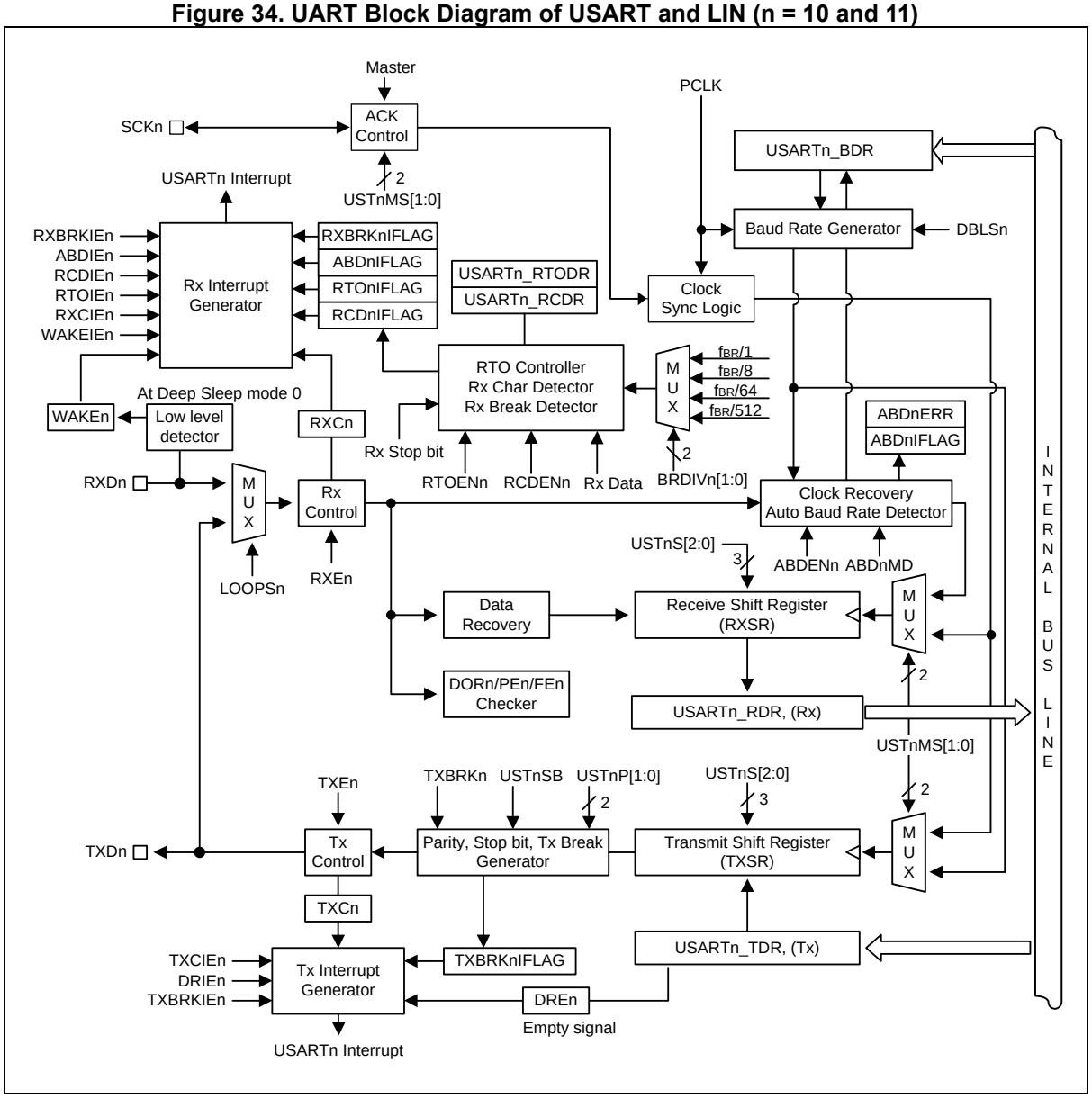
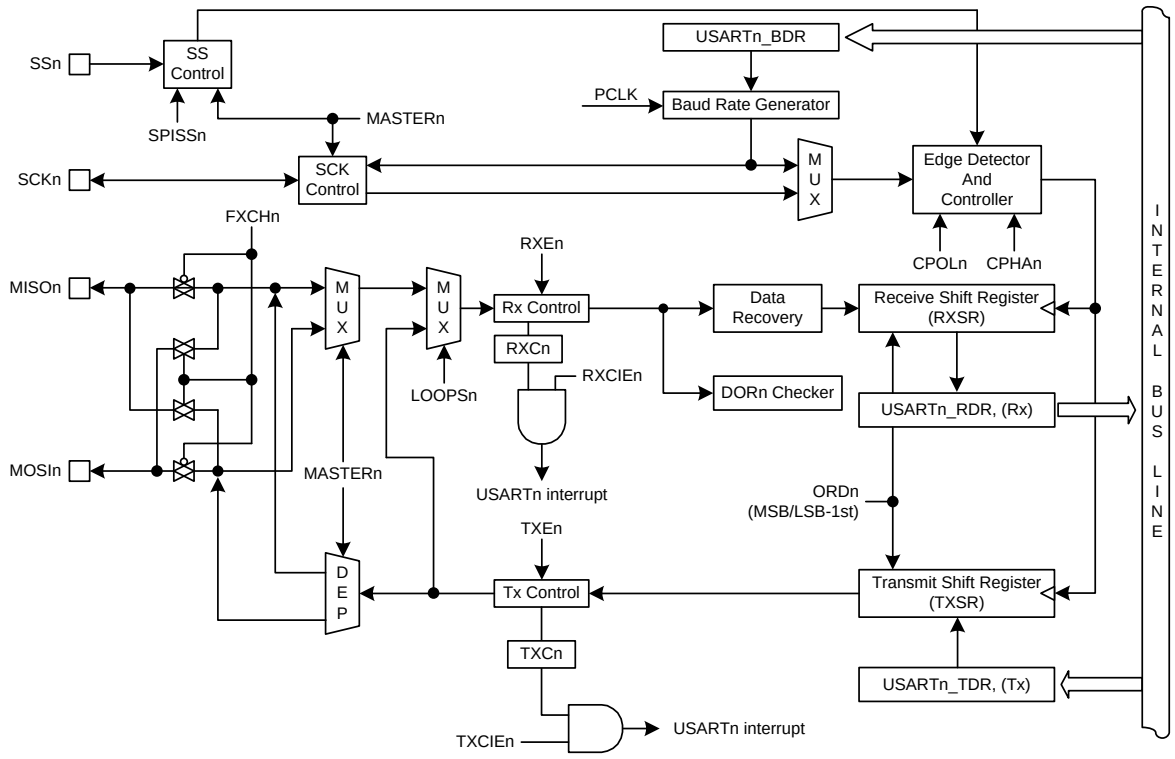


Figure 35 shows a block diagram of the SPI block.

Figure 35. SPIn Block Diagram of USART (n = 10 and 11)



NOTES:

1. The clock frequency of SCKn should be less than or equal to PCLK/2.
2. When DMA is used, the interval of data to be received requires at least 32 clock of PCLK.

12.1.2 Pins for USART 10/11

Table 17. Pins and External Signals for USART 10/11

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

12.2 UART 0

The A31L21x series has built-in 1-channel of UART modules (Universal Asynchronous Receiver/Transmitter).

Users can read the UART operation status including the error status from the status register.

A baud rate generator, which generates proper baud rate, exists for each UART channel. This baud rate generator divides down the PCLK to the frequency ranging from 1 to 65536. Then, the baud rate is generated using a 1:16 clock and an 8-bit precision clock tuning function.

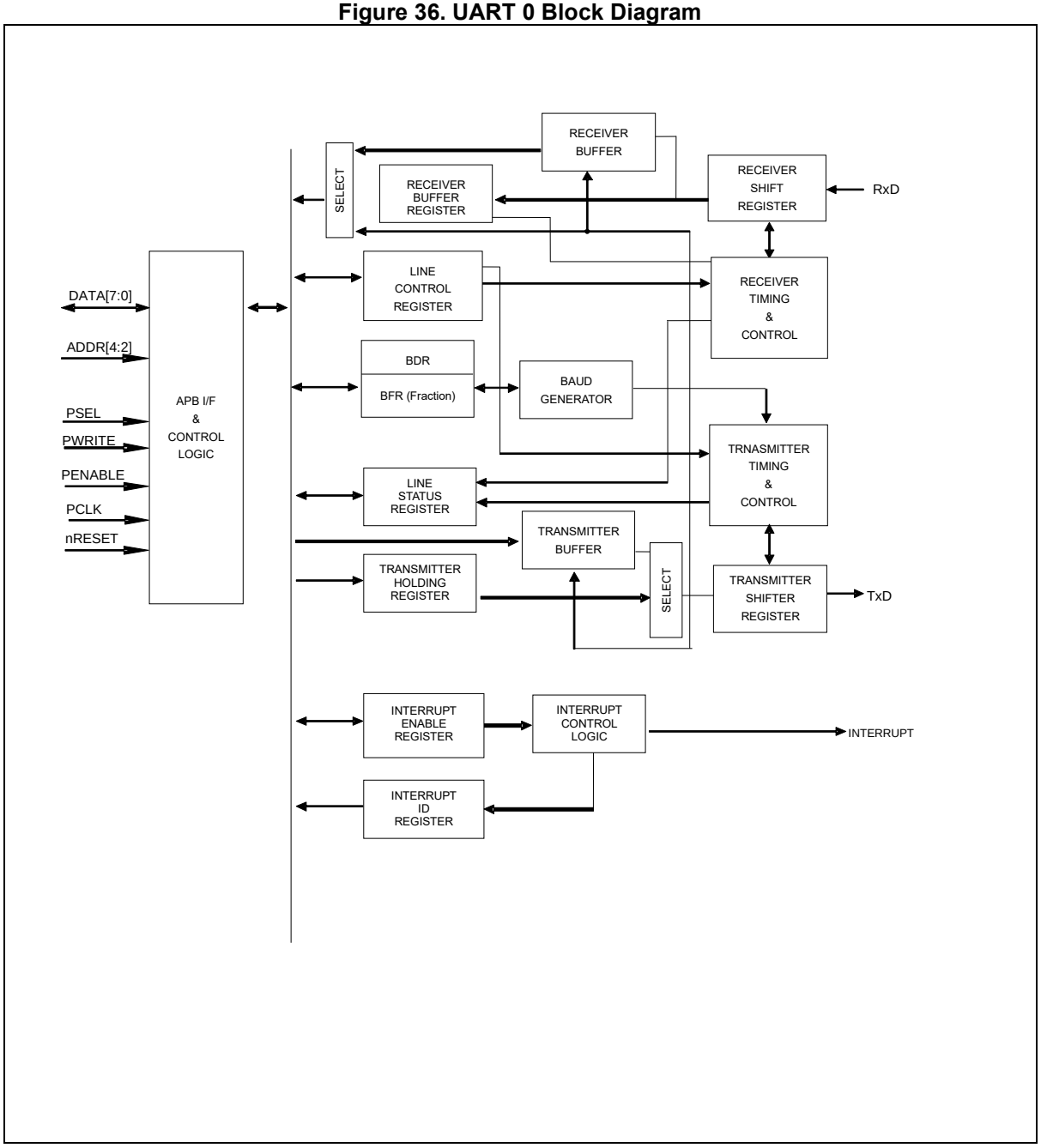
The UART 0 of the A31L21x series features the followings:

- Compatible with 16450 UART
- Configurable standard asynchronous control bit (Start, Stop, and Parity)
- Programmable 16-bit fractional baud rate generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-Stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

12.2.1 UART 0 block diagram

Figure 36 shows a block diagram of the UART block.

Figure 36. UART 0 Block Diagram



12.2.2 Pins for UART 0

Table 18. Pins and External Signals for UART 0 (n = 0)

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input

12.3 LPUART 0/1

The A31L21x series has built-in 2-channel of low power UART modules (Universal Asynchronous Receiver/Transmitter).

This LPUART (Low Power UART) supports asynchronous serial communication up to 9600bps in DEEP SLEEP mode when using a 32.768kHz sub-oscillator. It also supports 1-wire half-duplex communication.

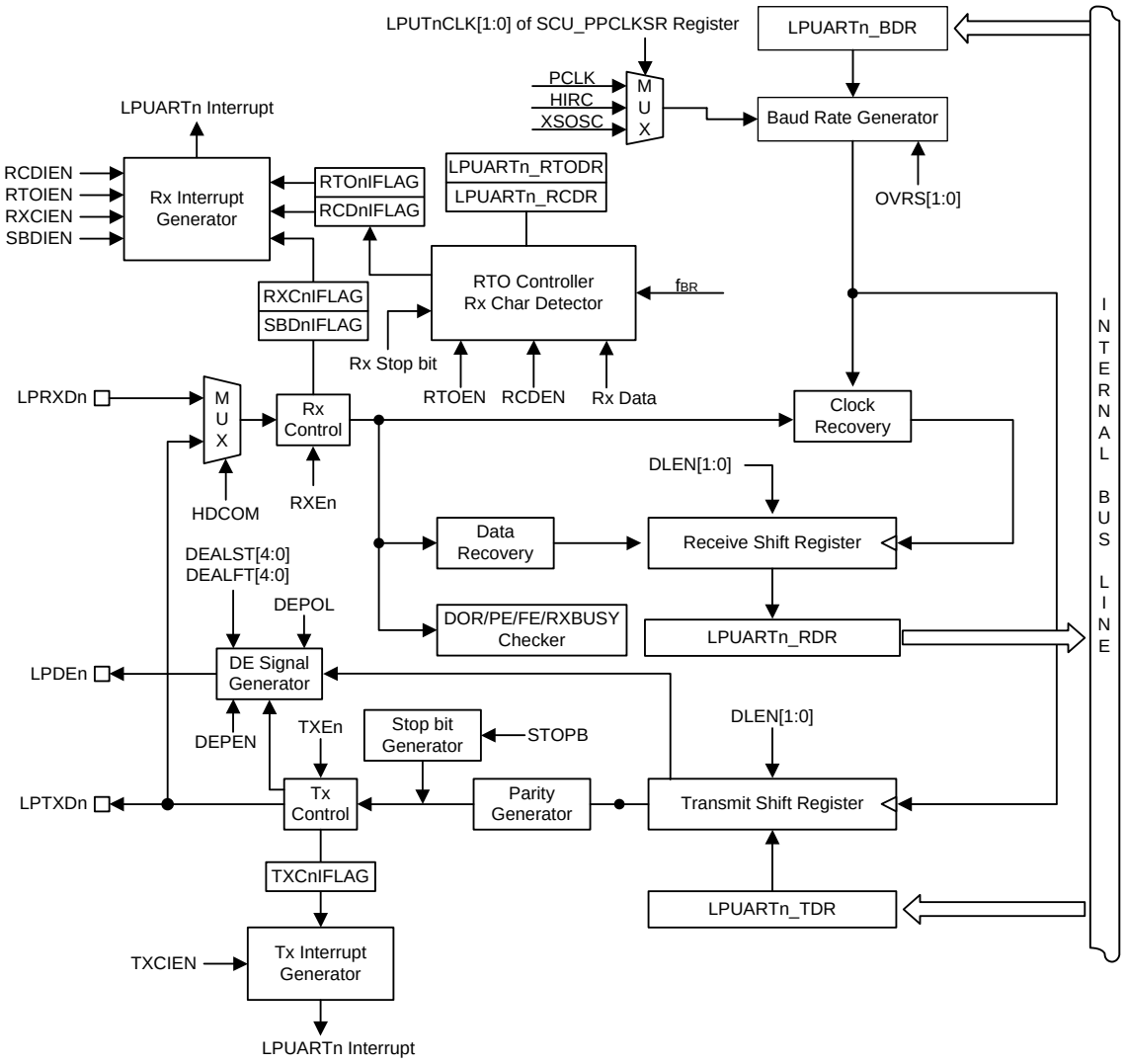
The LPUART 0/1 of the A31L21x series features the followings:

- Full-duplex and half-duplex operations
- Baud rate generator
- Supports serial frames with 5,6,7, or 8 Data bits and 1 or 2 Stop bits
- Odd or even parity generation, and parity check supported by hardware
- Supports receive character detection and receive time out function
- Baud rate compensation function
- Supports up to 9600pbs with 32.768kHz sub-oscillator
- Data OverRun Detection
- Framing Error Detection
- Double speed asynchronous communication mode

12.3.1 LPUART 0/1 block diagram

Figure 37 shows a block diagram of the LPUART block.

Figure 37. LPUART Block Diagram (n = 0 and 1)



NOTES:

1. If the XSOSC (32.768kHz) is used for a clock of the LPUARTn, the maximum baud rate can be up to 9600bps.
2. A clock of PCLK should be faster than or equal to a clock of the LPUARTn.
3. Data to be transmitted should be written to the LPUARTn_TDR register after checking if the TXCIFLAG bit is set to “1b”.

12.3.2 Pins for LPUART

Table 19. Pins and External Signals for LPUART 0/1

Pin name	Type	Description
LPTXDn	O	Low Power UART n transmit output
LPRXDn	I	Low Power UART n receive input
LPDEn	O	Low Power UART n DE signal output

13 I2C 0/1/2, SPI 0/1/2/3, and smartcard 0 interface

13.1 I2C 0/1/2 interface

I2C is one of industrial standard serial communication protocols, which uses 2 bus lines, Serial Data Line (SDAn) and Serial Clock Line (SCLn). These are used to exchange data.

Because both of the SDAn and SCLn lines are open-drain outputs, each line needs a pull-up resistor (n = 0, 1, and 2).

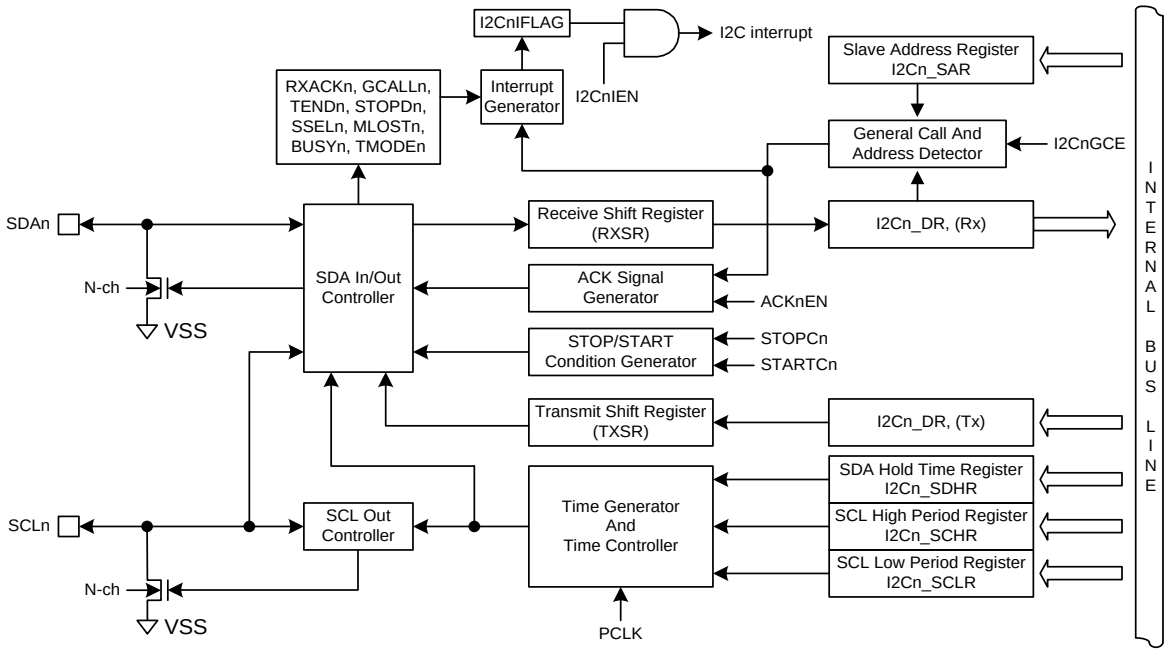
The I2C interface 0/1/2 of A31L21x series features the followings:

- Compatible with I2C bus standard
- Multi-master operation
- Up to 1MHz data transfer read speed
- 7-bit address
- Two slave addresses supported
- Master and slave operations
- Bus busy detection

13.1.1 I2C 0/1/2 block diagram

Figure 38 shows a block diagram of the I2C block.

Figure 38. I2C Block Diagram (n = 0, 1, and 2)



NOTE: When the corresponding port of I2C is a sub-function for the SCLn/SDAn pin, the SCLn/SDAn pins are automatically set as N-channel open-drain outputs and the input latch is read when reading the pins. The corresponding pull-up resistor is determined by the control register.

13.1.2 Pins for I2C 0/1/2

Table 20. Pins and External Signals for I2C (n = 0, 1, and 2)

Pin name	Type	Description
SCLn	I/O	I2C Channel n Serial clock bus line (open-drain)
SDAn	I/O	I2C Channel n Serial data bus line (open-drain)

13.2 SPI 0/1/2/3 interface

The SPI interface enables synchronous serial data transfer between external serial devices. It allows full-duplex communication using 4-wires (MOSIn, MISOn, SCKn, SSn).

It supports master and slave modes, and selects serial clock (SCKn) polarity. In addition, for the data transmission, it selects whether to transfer LSB first or MSB first.

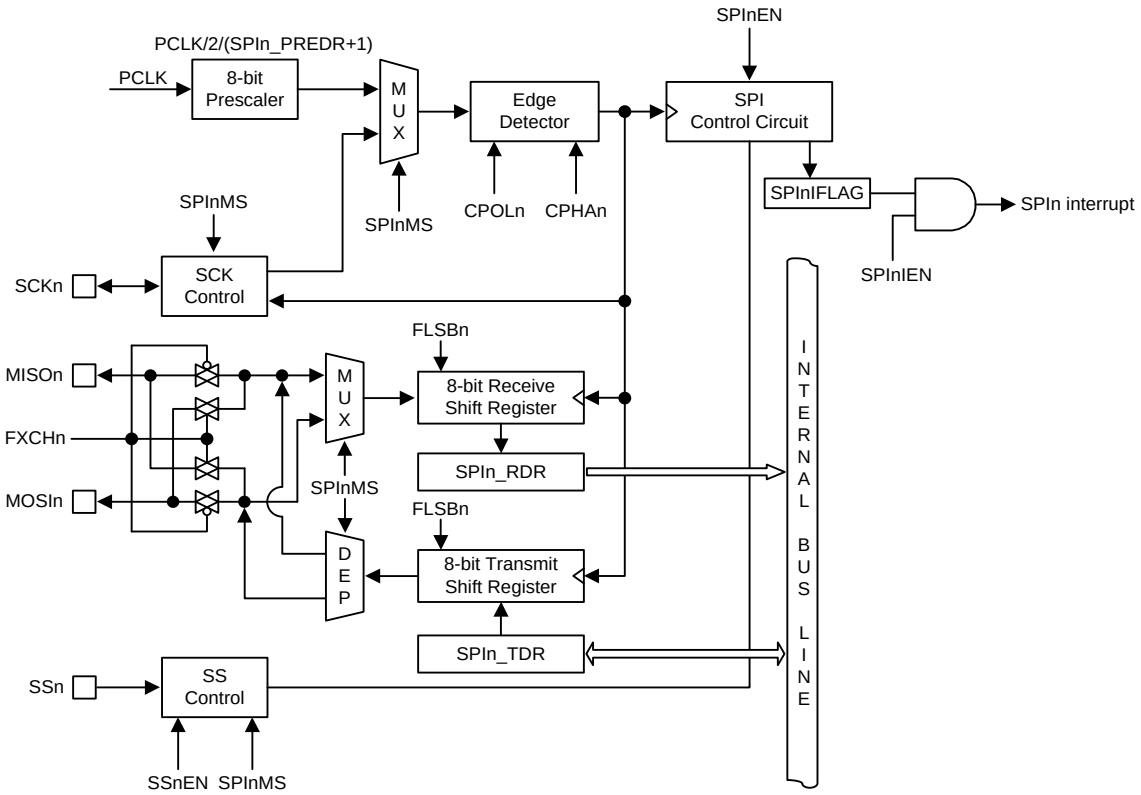
The SPI 0/1/2/3 of the A31L21x series features the followings:

- Master and slave modes supported
- Clock polarity selection
- Up to 16MHz data transmission
- Exchangeable MOSIn and MISOn functions

13.2.1 SPI 0/1/2/3 block diagram

Figure 39 shows a block diagram of the SPI block.

Figure 39. SPI Block Diagram (n = 0, 1, 2, and 3)



NOTES:

1. The clock frequency of the SCKn should be less than or equal to the PCLK/2.
2. Interrupts of the SPIn occur only when one byte transmission/reception finishes. So, the status (SPInMS and SSnHIGH) bits should be checked by S/W.
3. When DMA is used, at least 32 clocks of PCLK are required for the interval between data-receptions.

13.2.2 Pins for SPI 0/1/2/3

Table 21. Pins and External Signals for SPI (n = 0, 1, 2, and 3)

Pin name	Type	Description
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

13.3 Smartcard interface 0

A smartcard interface block of the A31L21x series is based on ISO/IEC 7816-3 standard. It supports UART mode to communicate with others.

This smartcard interface block has thirteen registers such as control registers (SCn_CR1, SCn_CR2, SCn_CR3), receive data register (SCn_RDR), transmit data register (SCn_TDR), and baud-rate data register (SCn_BDR).

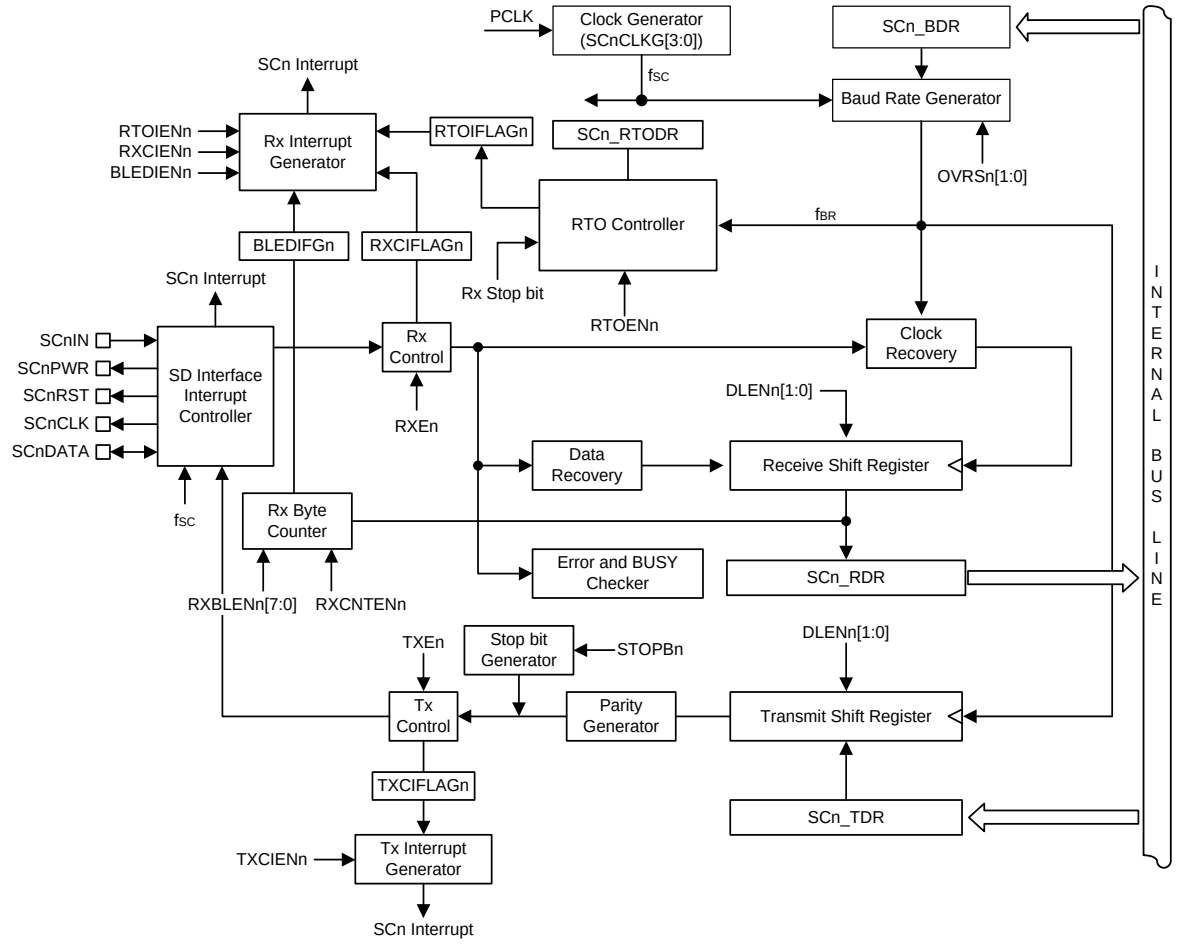
The smartcard interface 0 of the A31L21x series features the followings:

- ISO-7816-3 T = 0, T = 1 compatible
- DMA transfer supported
- Programmable guard time
- Auto activation sequence supported
- Auto warm reset sequence supported
- Auto deactivation sequence supported
- Auto convention detection sequence supported
- Baud rate compensation function
- UART mode selection
- Full duplex asynchronous operation
- Programmable baud-rate generation
- Even, odd, or no parity bit generation and detection selection
- 1 or 2 Stop bit generation selection
- Programmable data delay time after stop bit

13.3.1 Smartcard interface 0 block diagram

Figure 40 shows a block diagram of the Smartcard interface block.

Figure 40. Smartcard Interface Block Diagram (n = 0)



NOTE: After checking that the TXCIFLAGn bit is set to '1', write the data to be transmitted to the SCn_TDR register.

13.3.2 Pins for smartcard interface 0

Table 22. Pins and External Signals for Smartcard Interface (n = 0)

Pin name	Type	Description
SCnPWR	O	Smartcard power control output
SCnDATA	I/O	Smartcard data input/output
SCnRST	O	Smartcard reset output
SCnCLK	O	Smartcard clock output
SCnIN	I	Smartcard detection input
SCnTXD	O	SCn's UART data output
SCnRXD	I	SCn's UART data input

14 LCD driver

The LCD driver of the A31L21x series includes the LCD control register (LCD_CR) and the LCD contrast control register (LCD_CCR).

The LCLK[1:0] bits of the LCD_CR register determine the frequency of the COM signal scanning each segment output.

A RESET clears the LCD_CR register, and sets the LCD_CCR register to logic '0'.

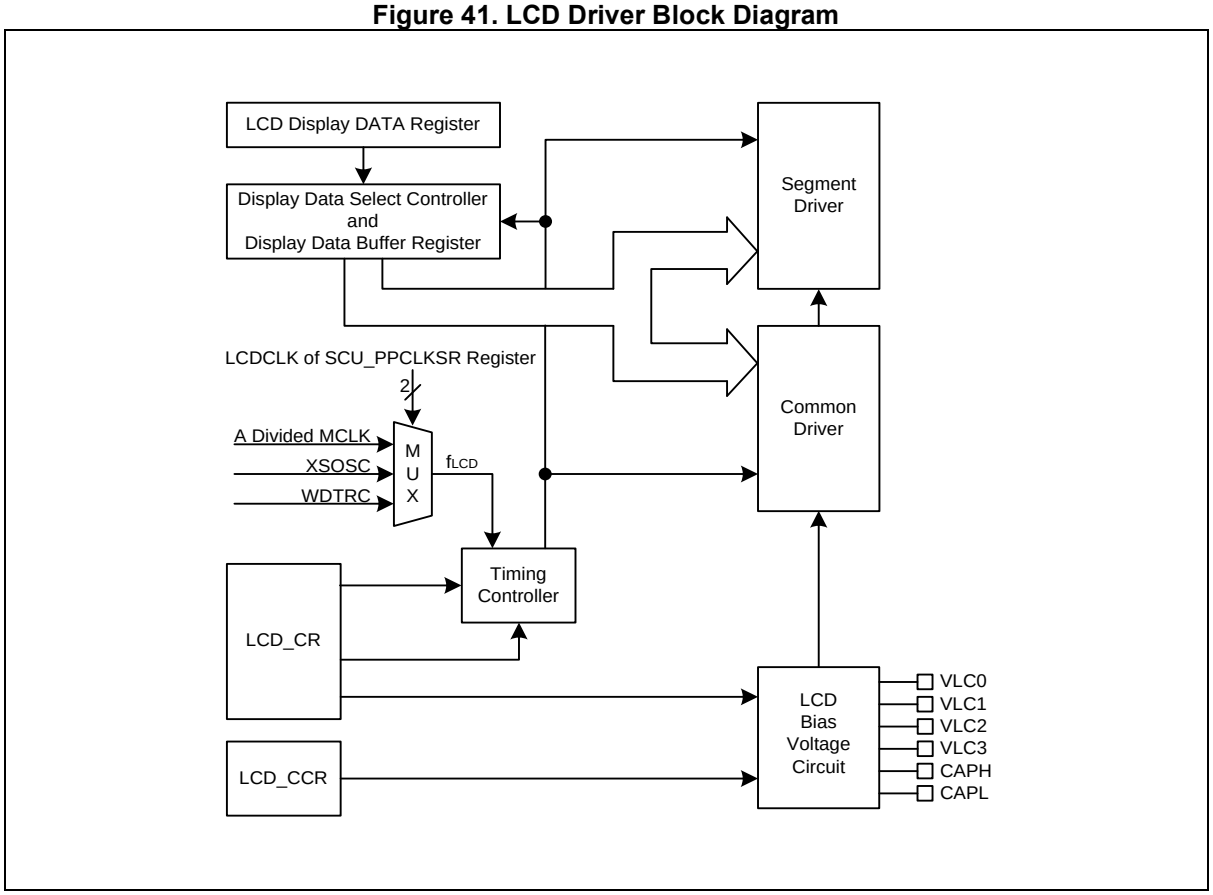
The LCD display can be continued even during SLEEP mode and DEEP SLEEP mode 0, if it uses a selected clock for the LCD driver.

A clock and duty of the LCD driver are initialized by hardware whenever a value is written to the control register. Therefore, it is recommended not to rewrite the LCD_CR register too often.

14.1 LCD driver block diagram

Figure 41 shows a block diagram of the LCD driver block.

Figure 41. LCD Driver Block Diagram



14.2 Pins for LCD driver

Table 23. Pins and External Signals for LCD Driver

Pin name	Type	Description
COM0 - COM7	O	LCD common signal outputs
SEG0 - SEG44	O	LCD segment signal outputs
VLC0/1/2/3	I/O	LCD bias voltage input/output
CAPH/L	O	Capacitor terminal for voltage booster

15 CRC and checksum

A CRC (Cyclic Redundancy Check) generator is used to obtain 8/16/32-bit CRC code of Flash ROM and any data stream.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of functional safety standards, they offer means of verifying Flash memory's integrity.

The CRC generator helps computing the signature of the software during runtime, comparing with a reference signature.

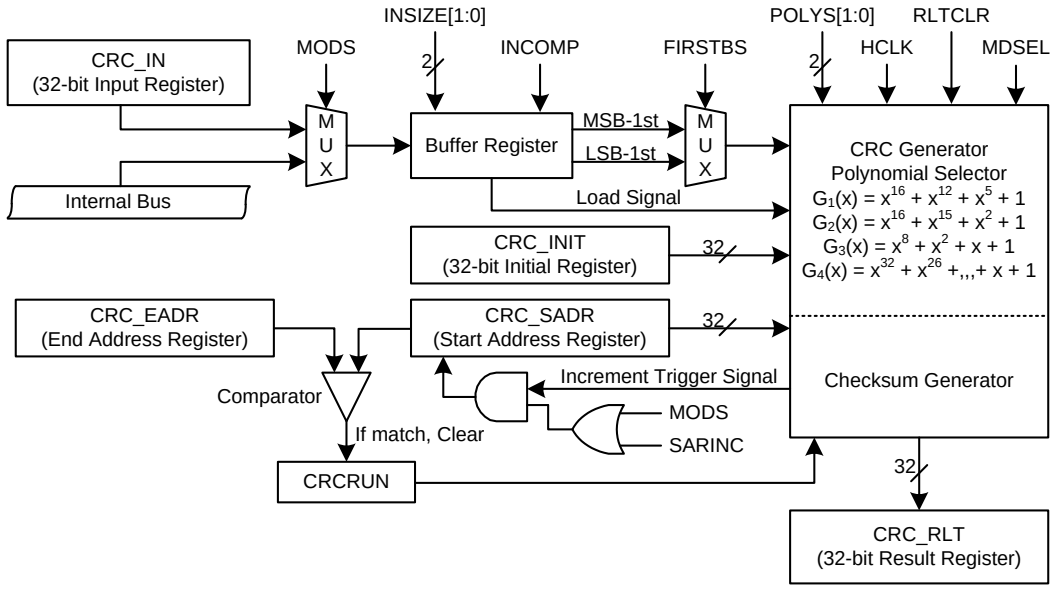
The CRC generator of the A31L21x series has following features:

- Auto CRC and user CRC mode
- CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$) supported
- CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$) supported
- CRC-8 ($G_3(x) = x^8 + x^2 + x + 1$) supported
- CRC-32 ($G_4(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$) supported
- CRC and checksum mode
- CRC/checksum start address auto increment (User mode only)

15.1 CRC and checksum block diagram

Figure 42 shows a block diagram of the CRC and checksum interface block.

Figure 42. CRC and Checksum Block Diagram



NOTES:

1. The operation is finished after calculating from the address specified by the CRC_SADR to the address specified by the CRC_EADR, in auto mode or when SARINC=1.
2. The CRC_SADR and CRC_EADR have the same value after finishing the operation.
3. The end address in the CRC_EADR must be greater than the start address in CRC_SADR.
4. The end address must be at least 0x7C from the start address in “Auto mode”.
5. The CRC_SADR/CRC_EADR in “Auto mode” should have any value in Flash memory area (0x10000000 to 0x1001FFFF).
6. The CPU will be held at “Auto mode” if the CPU is in the Flash memory, and global interrupts should be disabled by software.
7. Users must set the HCLK frequency to be less than or equal to 20MHz in “Auto mode” by configuring the MODS bit of the CRC_CR register.
8. In Auto mode, the CRC_CR can’t be written and the CRC_RLT can’t be read.

16 Advanced Encryption Standard (AES-128)

The AES-128 module encrypts and decrypts data using the AES algorithm. It complies with “The advanced encryption standard as defined by Federal Information Processing Standards Publication” (FIPS PUB 179, 2001 November 26).

The AES-128 module encrypts and decrypts a 128-bit sized block using a 128-bit long key. It supports key expansion function for decryption, and DMA transfer for the incoming and outcoming data.

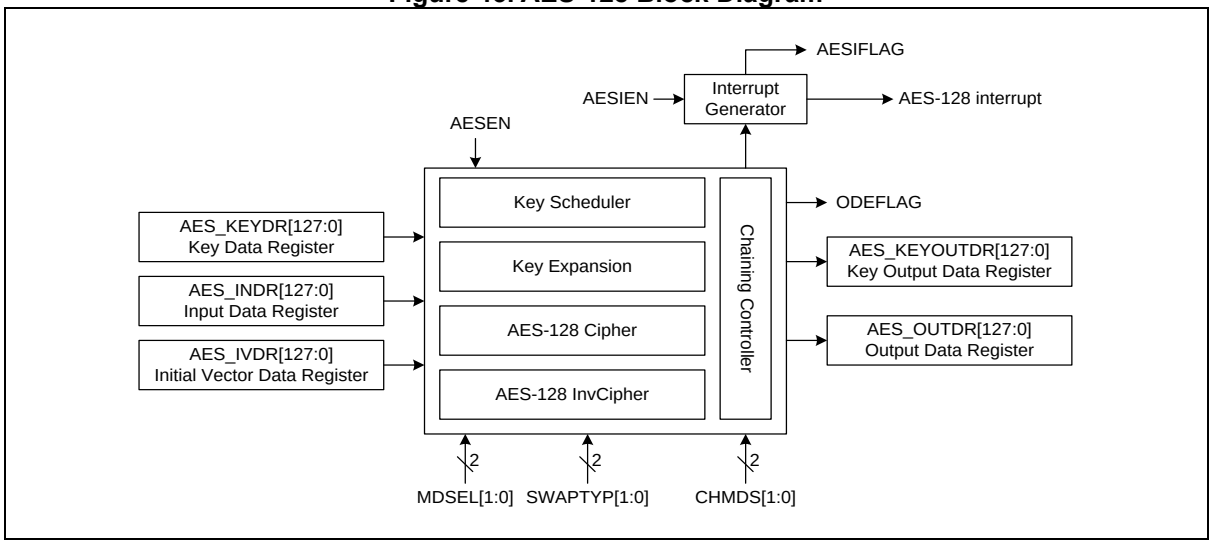
The AES-128 module of the A31L21x series has following features:

- Encryption and decryption using AES Rijndael block cipher algorithm
- NIST FIPS 197 compatible
- Key scheduler and key expansion for decryption
- 128-bit data block processing
- 128-bit long key
- 211 cycles of PCLK required (to encrypt/decrypt one 128-bit block)
- Electronic codebook (ECB), cipher block chaining (CBC), and counter mode (CTR) supported
- 32-bit input and output buffers
- Automatic data flow control with DMA support using 2 channels

16.1 AES-128 block diagram

Figure 43 shows a block diagram of the AES-128.

Figure 43. AES-128 Block Diagram



17 True Random Number Generator (RNG)

The Random Number Generator (RNG) continuously provides 32-bit entropy samples based on an analog noise source. The RNG in the device makes non-deterministic randomness that cannot be predicted with any physical source.

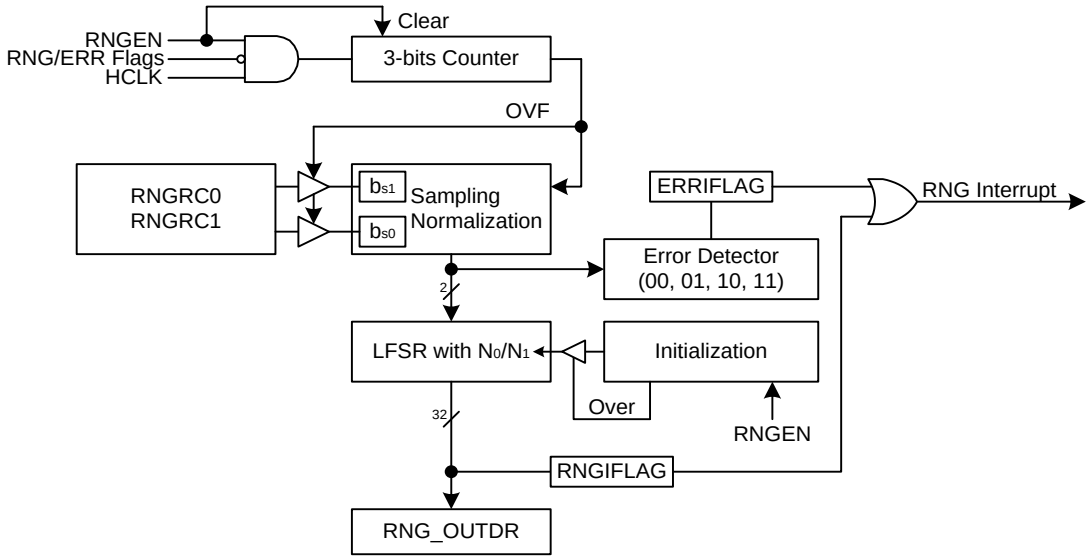
The RNG of the A31L21x series has following features:

- 32-bit non-deterministic random numbers produced by an analog entropy source post-processed with linear-feedback shift registers (LFSR)
- A 32-bit random sample generation every 20 - 50 RNG clock cycles
- Error detector (to check whether the same pattern is repeated more than 16 times in a row)
- Disable function (to reduce power consumption)

17.1 RNG block diagram

Figure 44 shows a block diagram of the RNG block.

Figure 44. RNG Block Diagram



NOTE: The error detector checks whether the same pattern (00b, 01b, 10b, or 11b) is repeated 16 times or more continuously.

18 Temperature Sensor (TS)

The temperature sensor is a ring-oscillator type and can be used to measure the junction temperature of the device. The nominal frequency at 30℃ is about 0.9MHz and it varies from 0.6 to 1.25 [MHz] as the temperature changes from -20℃ to +105℃.

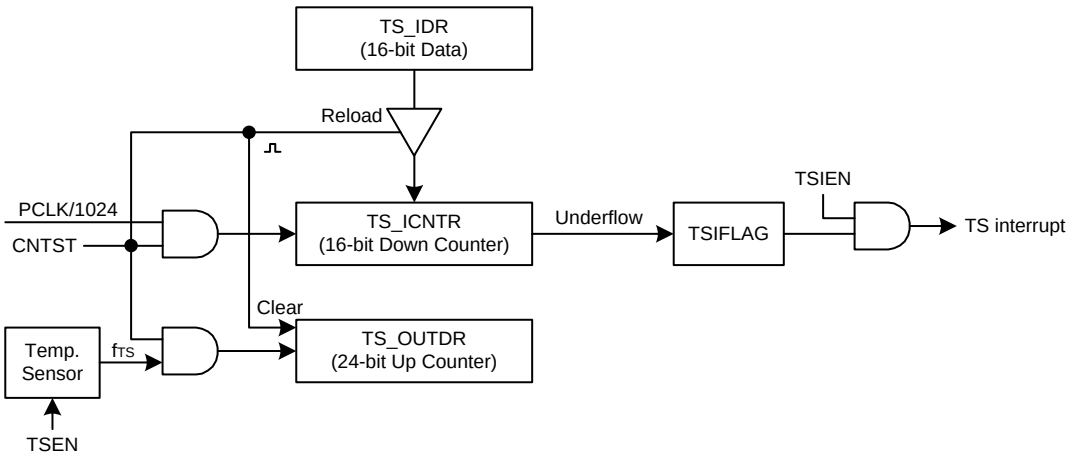
The temperature sensor of the A31L21x series has the following features:

- -20℃ to 105℃, wide range of operating temperature
- 16-bit interval down counter (to count the frequency of temperature sensor)
- 24-bit data register (to save the counted value of temperature sensor frequency)

18.1 TS block diagram

Figure 45 shows a block diagram of the temperature sensor block.

Figure 45. Temperature Sensor Block Diagram



NOTE: The CNTST bit will be cleared to “0b” after the underflow of TS_ICNTR.

19 Direct Memory Access (DMA) controller

Direct Memory Access (DMA) controller transfers data without s/w asserts. The DMA of the A31L21x series has 7 channels, and the DMA controller has four registers such as control register (DMACHn_CR), peripheral address register (DMACHn_PAR), memory address register (DMACHn_MAR), and interrupt enable and status register (DMACHn_IESR).

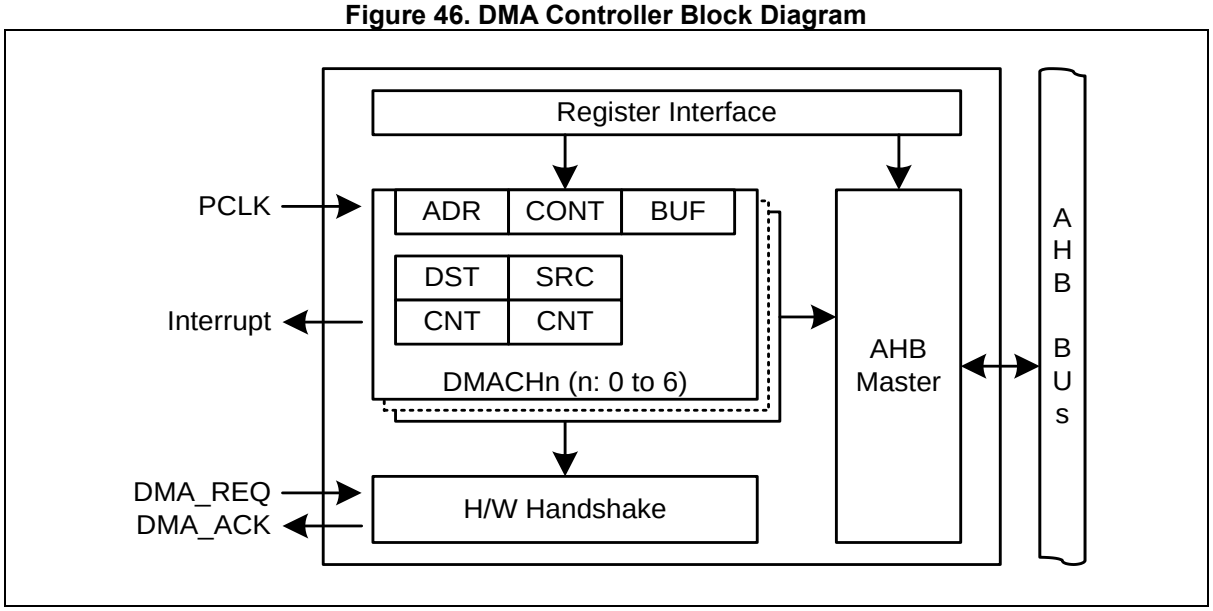
The DMA controller of the A31L21x series features the followings:

- 7 channels supported
- 8/16/32-bit data size supported
- Memory to peripheral transmission
- Peripheral to memory transmission

19.1 DMA controller block diagram

Figure 46 shows a block diagram of the DMA controller block.

Figure 46. DMA Controller Block Diagram



20 Electrical characteristics

Unless otherwise specified, test conditions for DC characteristics are as follows:

- T_A = - 40 °C to +85°C (Commercial grade) or T_A = - 40 °C to + 105°C (Industrial grade)
- VDD = 1.71V to 3.6V

NOTE: Refer to **Figure 70. A31L21x Series Numbering Nomenclature** for device part number by Commercial and Industrial grade.

20.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions, which should not be exceeded under the worst possible conditions.

Table 24. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage	VDD	-0.3 to +4.0	V	–
Normal pin	V_I	-0.3 to VDD +0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD +0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-60	mA	Maximum current (ΣI_{OH})
	I_{OL}	20	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	160	mA	Maximum current (ΣI_{OL})
5V tolerant pin	VI	-0.3 to +6.0	V	Voltage on any pin with respect to VSS
Total power dissipation	P_T	600	mW	–
Storage temperature	T_{STG}	-65 to +150	°C	–

20.2 Recommended operating conditions

Table 25. Recommended Operating Conditions

Parameter	Symbol	Conditions			Min	Max	Units
Operating voltage	VDD	fx = 32 to 38kHz	Sub Clock		1.71	3.6	V
		fx = 2.0 to 4.2MHz	Main clock	Ceramic	1.8	3.6	
		fx = 2.0 to 16MHz		Crystal	2.7	3.6	
		fx = 2.0 to 32MHz	External clock		3.0	3.6	
		fx = 40kHz	Internal RC		1.71	3.6	
		fx = 2.0 to 32MHz			1.71	3.6	
Input voltage	V_{IN}	Normal pin			-0.3	VDD+0.3	V
		5V tolerance pins, PD[4:0]	2.0V ≤ VDD ≤ 3.6V		-0.3	5.5	
			1.71V ≤ VDD < 2.0V		-0.3	5.0	
Operating temperature	T_{OPR}	VDD = 1.71 to 3.6V (Commercial grade)			-40	85	°C
		VDD = 1.71 to 3.6V (Industrial grade)			-40	105	

20.3 ADC characteristics

Table 26. ADC Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral non-linearity	INL	AVDD=1.8V – 3.6V		–	–	±6	LSB
Differential non-linearity	DNL			–	±1	±2	
Zero offset error	ZOE			–	–	±5	
Full scale error	FSE			–	–	±5	
Integral non-linearity	INL	AVDD=1.71V – 3.6V		–	–	±6	LSB
Differential non-linearity	DNL			–	±1	±2.5	
Conversion time	t_{CONV}	AVDD=2.7V – 3.6V		1	–	–	μs
		AVDD=1.71V – 3.6V		2	–	–	
Analog input voltage	V_{AN}	–		VSS	–	AVDD	V
Analog voltage	AVDD	–		VDD-0.3	VDD	VDD+0.3	V
ADC stabilization time	t_{STAB}	–		–	–	16	$1/f_{ADC}$
Band gap reference buffer voltage	V_{ADCBUF}	Conversion time: 8us		870	920	970	mV
ADC input leakage current	I_{AN}	AVDD=3.0V		–	–	2	μA
ADC current	I_{ADC}	Enable	AVDD=3.0V, f_{ADC}=16MHz	–	400	800	μA
		Disable		–	–	10	nA

NOTES:

1. Zero offset error is the difference between 0x000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 0xFFF and the converted output for top input voltage (VDD).

20.4 Power-on Reset characteristics

Table 27. Power-on Reset Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset release level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.1	–	V
VDD voltage rising time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	21	40	nA

20.5 Comparator characteristics

Table 28. Comparator Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input offset voltage	VOF	VDD=3.0V, VIN=1/2VDD		–	±4	±20	mV
Operating voltage	VDD	All comparator pins except below		1.71	–	3.6	V
		CP1N3, CP1P2, CP1P3, CP1P4, CP1P5		2.0	–	3.6	
Startup time	t_{START}	Fast speed		–	15	20	µs
		Slow speed		–	20	25	
Propagation delay	t_{DELAY}	1.71V ≤ VDD ≤ 2.7V	Fast speed	–	1.2	4	µs
		2.7V ≤ VDD ≤ 3.6V		–	0.8	2	
		1.71V ≤ VDD ≤ 2.7V	Slow speed	–	2.5	6	
		2.7V ≤ VDD ≤ 3.6V		–	1.8	3.5	
Hysteresis	△V+	VDD=3.0V, VIN- = 1/2VDD, HYSnEN=1		5	10	20	mV
	△V-			-20	-10	-5	
Minimum input level	V_{INMIN}	HYSnEN=1		50	–	–	mVp-p
Reference resistors	R_{REF}	VDD=3.0V		21	30	39	kΩ
Comparator current	ICMP	Enable, fast speed	VDD=3.0V	–	3.5	5	µA
		Enable, slow speed		–	1.0	2	
		Disable		–	–	0.02	

20.6 Temperature Sensor characteristics

Table 29. Temperature Sensor Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Temp. linearity	T_{LIN}	Down to -20℃		–	±4	–	℃
Frequency variation	△F	(F(T2) – F(T1)) ÷ (T2 – T1)		1.8	3.2	5.7	kHz/℃
Frequency deviation	–	△F ÷ F(30)		0.25	0.35	0.45	%
Sensor current	I_{TS}	Enable	VDD = 3.0V	–	10	20	uA
		Disable		–	–	10	nA
Startup time	t_{START}	–		–	–	500	μs

NOTE: Temperature = {(F(T) – F(30)) ÷ △F} + 30 [℃]

Where, T1 = 30℃, T2 = 85℃(Commercial grade) or 105℃(Industrial grade)

F(T1) [kHz] is the temperature sensor output frequency acquired at 30℃.

F(T2) [kHz] is the temperature sensor output frequency acquired at 85℃ (Commercial grade) or 105℃ (Industrial grade).

F(T) [kHz] is the temperature sensor output frequency acquired at an arbitrary temperature.

20.7 Low Voltage Reset/Indicator characteristics

Table 30. Low Voltage Reset/Indicator Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection level	V_{LVR} V_{LVI}	LVR: All levels, LVI: Other levels except 1.50V, 1.50V level: rising edge voltage, Other levels: falling edge voltage		–	1.50	1.70	V
				1.71	1.85	2.00	
				1.85	2.00	2.15	
				2.00	2.15	2.30	
				2.15	2.30	2.45	
				2.25	2.45	2.65	
				2.40	2.60	2.80	
				2.55	2.75	2.95	
Hysteresis	△V	–		–	40	150	mV
Minimum pulse width	t_{LVRW} t_{LVIW}	–		100	–	–	μs
LVR/LVI current	$I_{LVR/LVI}$	Enable, one of two	VDD = 3V	–	200	400	nA
		Enable, both		–	250	500	
		Disable		–	–	10	

20.8 High frequency internal RC oscillator characteristics

Table 31. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HIRC}	VDD = 1.71V to 3.6V	–	32	–	MHz
Accuracy	–	T_A = -40 °C to +85 °C (commercial grade)	–	–	±2.0	%
		T_A = -40 °C to +105 °C (industrial grade)	–	–	±3.0	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	2	µs
IRC current	I_{HIRC}	Enable	–	300	450	µA
		Disable	–	–	10	nA

20.9 Internal Watchdog Timer RC oscillator characteristics

Table 32. Internal Watchdog Timer RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	34	40	46	kHz
Stabilization time	t_{WDTS}	–	–	–	100	µs
WDTRC current	I_{WDTRC}	Enable	–	450	650	nA
		Disable	–	–	10	

20.10 Timer 60 RC oscillator characteristics

Table 33. Timer 60 RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{T60RC}	–	50	100	200	Hz
Stabilization time	t_{T60S}	–	–	–	100	µs
T60 Current	I_{T60RC}	Enable	–	200	350	nA
		Disable	–	–	10	

20.11 LCD voltage characteristics

Table 34. LCD Voltage Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LCD voltage	VLC3	• Voltage booster enabled • 1/3 bias: All levels • 1/2 and 1/4 bias: Up to 0.825V	Typx0.93	0.725 0.750 0.775 0.800 0.825 0.850 0.875 0.900 0.925 0.950 0.975 1.000 1.025 1.050 1.075 1.100	Typx1.07	V
LCD mid bias voltage	VLC0/1	• Voltage booster enabled • 1/3 bias, No panel load • VDD=3.0V	Typ x 0.9	3xVLC3	Typ x 1.1	V
	VLC2		Typ x 0.9	2xVLC3	Typ x 1.1	
	VLC0	• Voltage booster enabled • 1/2 and 1/4 bias, No panel load • VDD=3.0V	Typ x 0.9	4xVLC3	Typ x 1.1	
	VLC1		Typ x 0.9	3xVLC3	Typ x 1.1	
	VLC2		Typ x 0.9	2xVLC3	Typ x 1.1	
	VLC1	• LCD dividing register • 1/4 bias, No panel load • VDD=2.7V to 3.6V, VLC0=VDD	Typ - 0.2	3/4xVLC3	Typ + 0.2	V
	VLC2		Typ - 0.2	2/4xVLC3	Typ + 0.2	
	VLC3		Typ - 0.2	1/4xVLC3	Typ + 0.2	
LCD driver output impedance	R_{LO}	VLCD=3V, ILOAD = ±10uA	–	5	10	kΩ
LCD bias dividing resistor	RLCD1	• Internal resistor mode • T_A = 25℃	20	30	40	kΩ
	RLCD2		40	60	80	
	RLCD3		80	120	160	
LCD block current	I_{LCD}	• Voltage booster mode • VDD=3V, VLCD=3.15V, 1/3bias	–	3	6	uA

20.12 DC electrical characteristics

Table 35. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH}	All input pins, nRESET	0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, nRESET	–	–	0.2VDD	V
Input hysteresis	△V	All input pins, nRESET, VDD=3V	100	200	–	mV
Output High Voltage	V_{OH}	VDD=3V, I_{OH} = – 10mA, T_A=25°C	VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=3V, I_{OL1} = 10mA, T_A=25°C, All output ports except V_{OL2}	–	–	1.0	V
	V_{OL2}	VDD=3V, I_{OL2} = 15mA, T_A=25°C, PB[7:0]	–	–	1.0	
Input high leakage current	I_{IH}	All Input ports	–	–	1	µA
Input low leakage current	I_{IL}	All Input ports	– 1	–	–	µA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, VDD=3V All Input ports	25	50	100	kΩ
		V_I=0V, T_A=25°C, VDD=3V RESETB	150	250	400	
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, VDD=3V All Input ports	25	50	100	kΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=3V	0.6	1.2	2.0	MΩ
	R_{X2}	T_A=25°C, VDD=3V	4.0	7.0	14.0	MΩ

20.13 Supply current characteristics

Table 36. Supply Current Characteristics

Parameter	Symbol	Conditions			Typ	Max	Units
Supply current	I_{DD1} (main run)	f_{HIRC} = 32MHz		VDD=3V, Code executed from Flash	2.9	4.0	mA
		f_{HIRC} = 16MHz			1.9	2.7	
		f_{XIN} = 16MHz			1.8	2.5	
		f_{HIRC} = 32MHz		VDD=3V, Code executed from RAM, Flash power off	2.6	3.6	mA
		f_{HIRC} = 16MHz			1.8	2.5	
		f_{XIN} = 16MHz			1.7	2.4	
	I_{DD2} (main sleep)	f_{HIRC} = 32MHz		VDD=3V, SLEEP in Flash	1.4	2.0	mA
		f_{HIRC} = 16MHz			0.9	1.3	
		f_{XIN} = 16MHz			0.9	1.3	
		f_{HIRC} = 32MHz		VDD=3V, SLEEP in RAM, Flash power off	1.3	1.8	mA
		f_{HIRC} = 16MHz			0.8	1.1	
		f_{XIN} = 16MHz			0.8	1.1	
	I_{DD3} (sub run)	f_{SUB} = 32.768kHz (C_L: 7pF), or f_{WDTRC} = 40kHz	T_A=25˚C	VDD=3V Code executed from Flash	13.0	23.0	uA
			T_A=85˚C		21.0	32.0	
			T_A=105˚C		30.0	45.0	
			T_A=25˚C	VDD=3V, Code executed from RAM, Flash power off	10.0	19.0	uA
			T_A=85˚C		19.0	35.0	
			T_A=105˚C		28.0	45.0	
	I_{DD4} (sub sleep)	f_{SUB} = 32.768kHz (C_L: 7pF) or f_{WDTRC} = 40kHz	T_A=25˚C	VDD=3V, SLEEP in Flash	2.2	5.6	uA
			T_A=85˚C		6.0	21.0	
			T_A=105˚C		12.0	28.0	
	I_{DD5}	VDD=3V DEEP SLEEP mode 0	T_A=25˚C	RTCC/f_{SUB} Off	0.39	0.99	uA
			T_A=85˚C		2.24	7.9	
			T_A=105˚C		5.0	18.9	
			T_A=25˚C	RTCC/f_{SUB} On	0.99	1.6	uA
			T_A=85˚C		2.9	9.9	
			T_A=105˚C		6.4	24.0	
	I_{DD6}	VDD=3V DEEP SLEEP mode 1	T_A=25˚C	RTCC/f_{SUB} Off	0.35	0.9	uA
			T_A=85˚C		1.5	6.9	
			T_A=105˚C		3.5	15.9	
	I_{DD7}	VDD=3V DEEP SLEEP mode 2	T_A=25˚C	RTCC/f_{SUB} Off	0.32	0.7	uA
			T_A=85˚C		0.8	2.9	
			T_A=105˚C		1.7	6.8	
	I_{DD8}	VDD=3V DEEP SLEEP mode 3 (SHUT DOWN)	T_A=25˚C	All Off	45	90	nA
			T_A=85˚C		0.35	2.1	uA
			T_A=105˚C		0.95	3.1	

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator (ISET_I[2:0] = 0x5), and the f_{HIRC} is a high frequency internal RC oscillator.
2. All supply current items don't include the current of WDTRC oscillator and a peripheral block except when explicitly mentioned. However, it does include the current of the power-on reset (POR) block.
3. There is thing to watch out for before entering a deep sleep mode 1. Refer to "functional table on current mode" in the PMU block.

Figure 47. IDD4 (SLEEP mode, fSUB = 32.768 kHz) at VDD = 3V

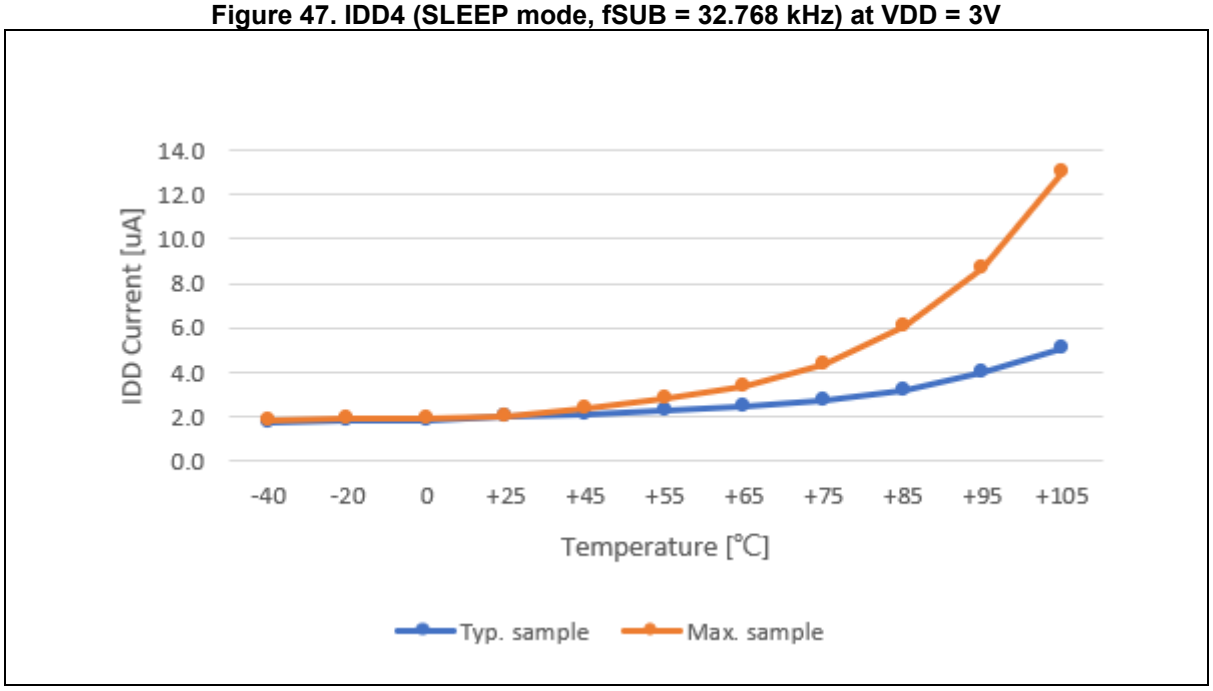


Figure 48. IDD4 (SLEEP mode, fWDTRC = 40 kHz) at VDD = 3V

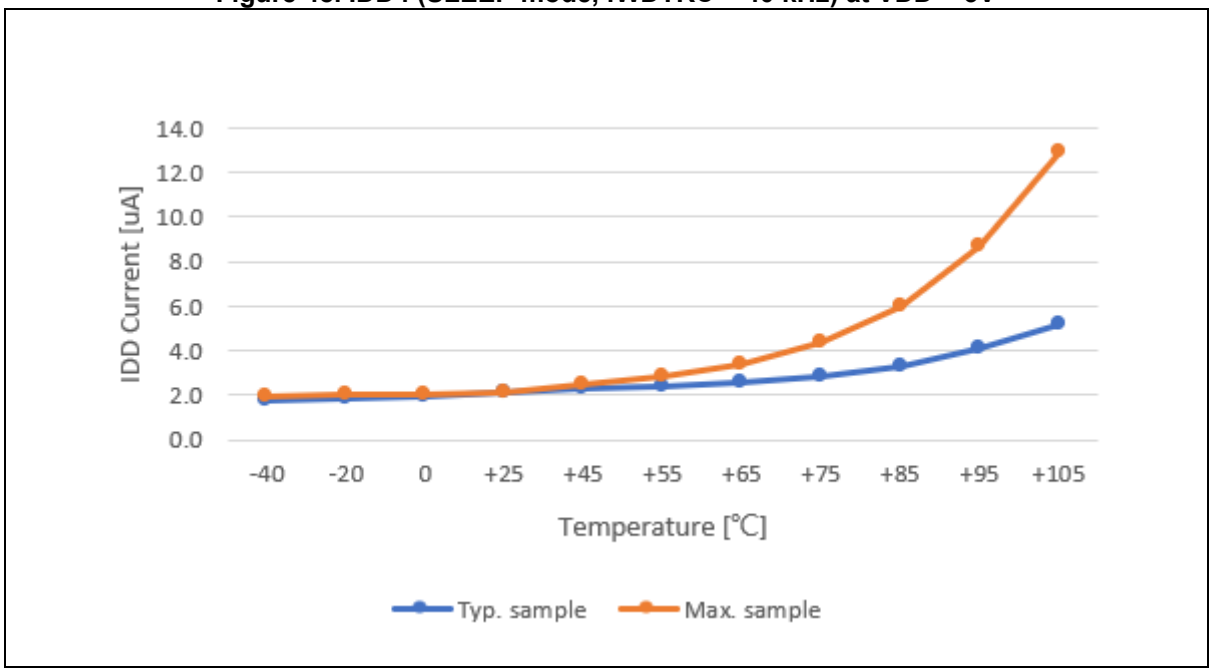


Figure 49. IDD5 (DEEP SLEEP mode 0, RTCC/fSUB Off) at VDD = 3V

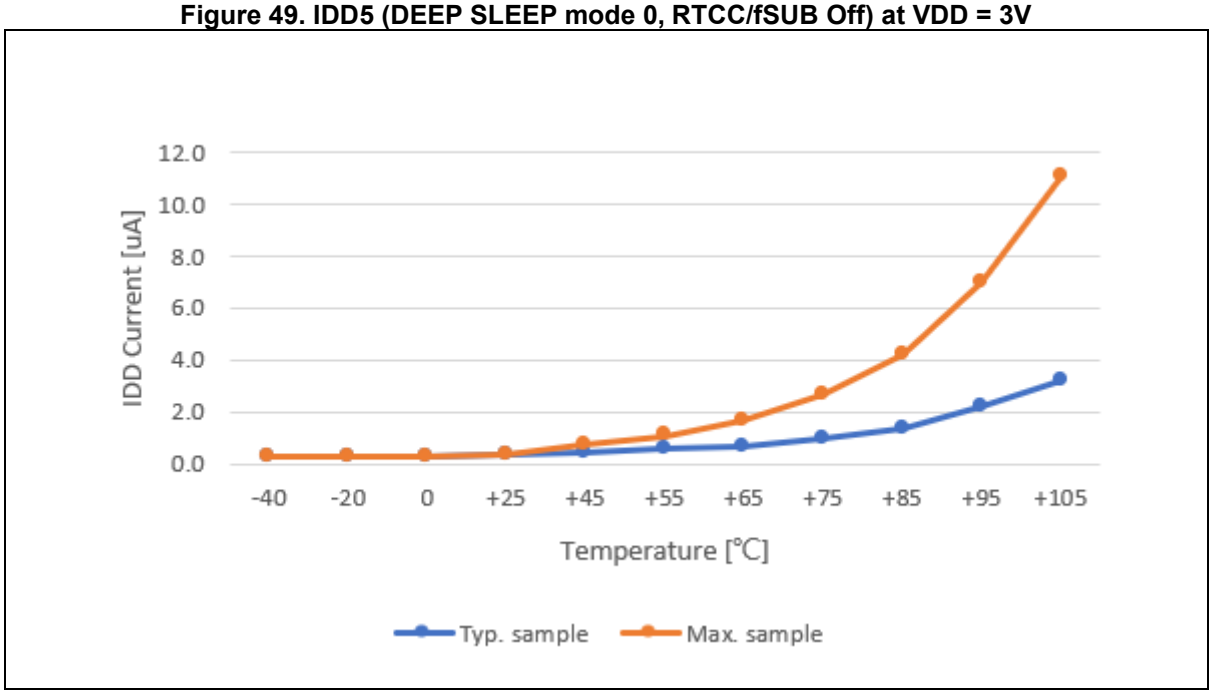


Figure 50. IDD5 (DEEP SLEEP mode 0, RTCC/fSUB On) at VDD = 3V

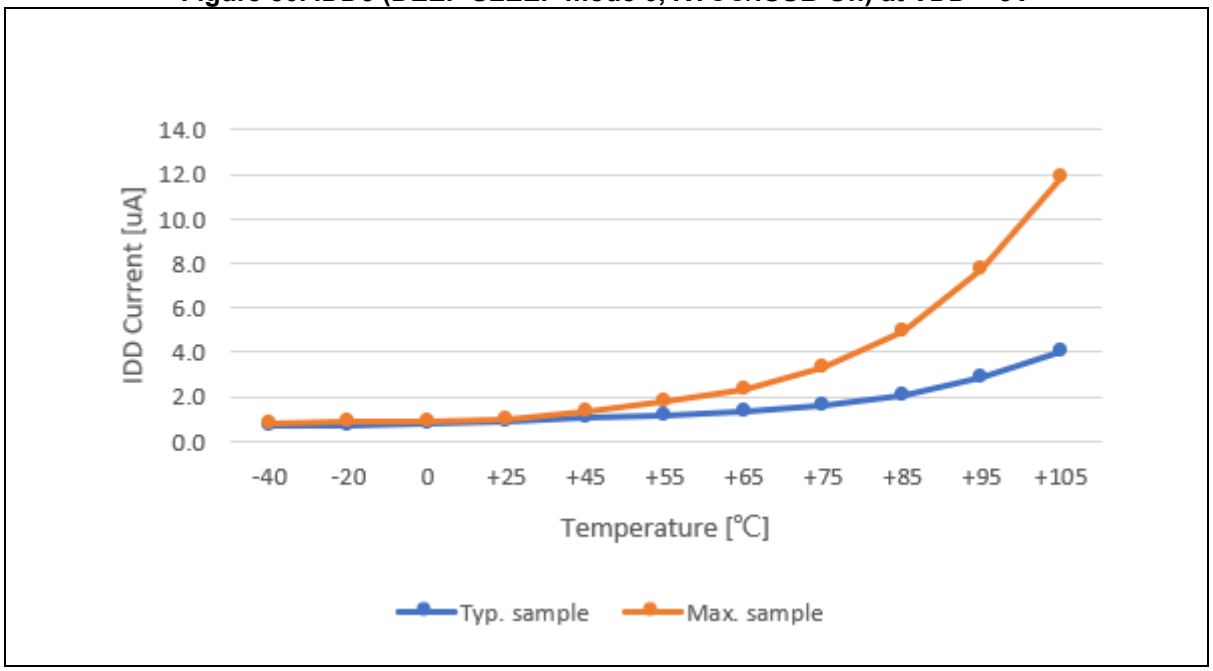


Figure 51. IDD6 (DEEP SLEEP mode 1) at VDD = 3V

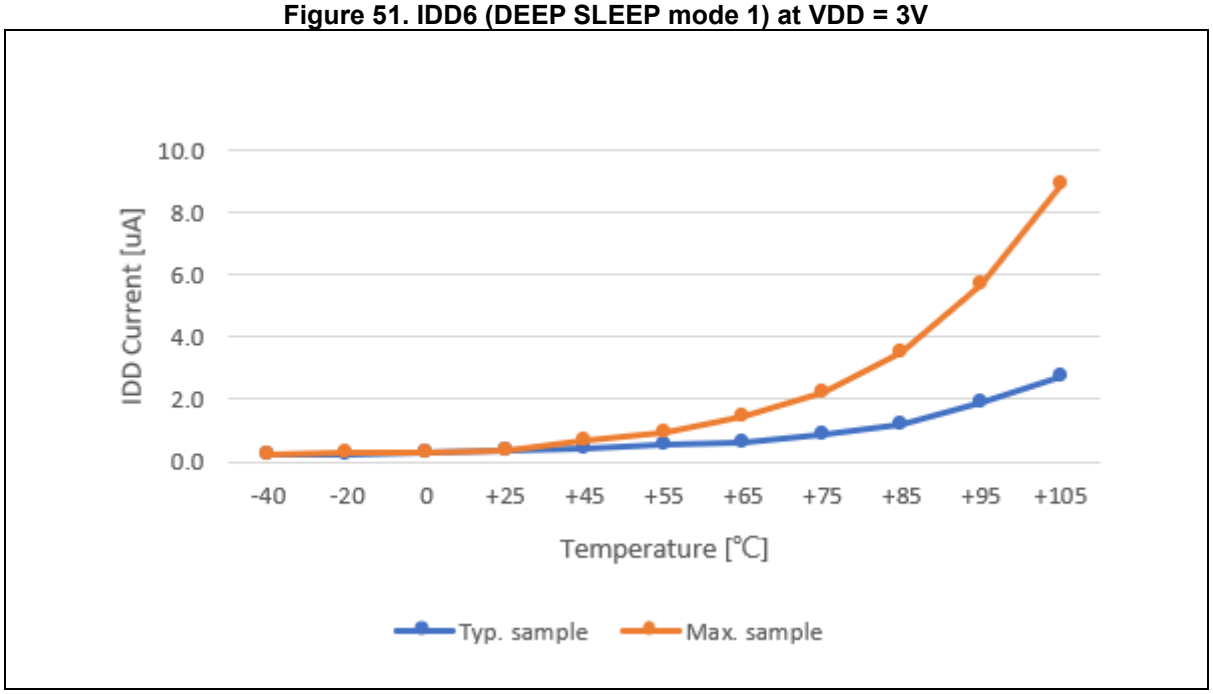
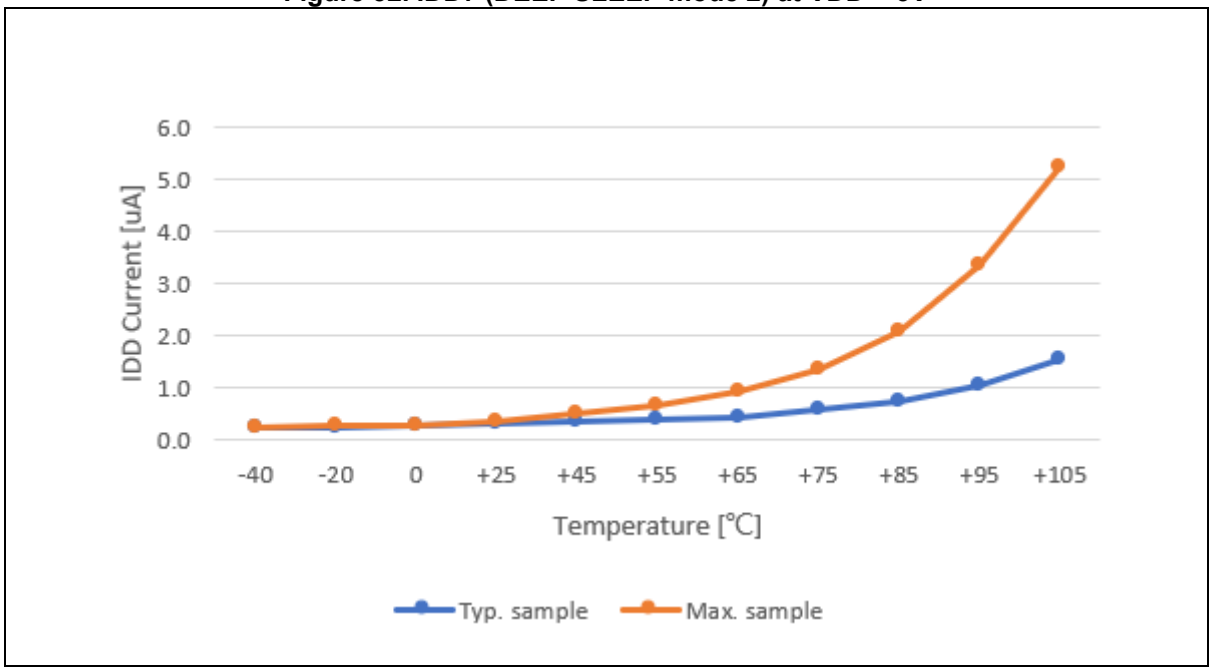


Figure 52. IDD7 (DEEP SLEEP mode 2) at VDD = 3V

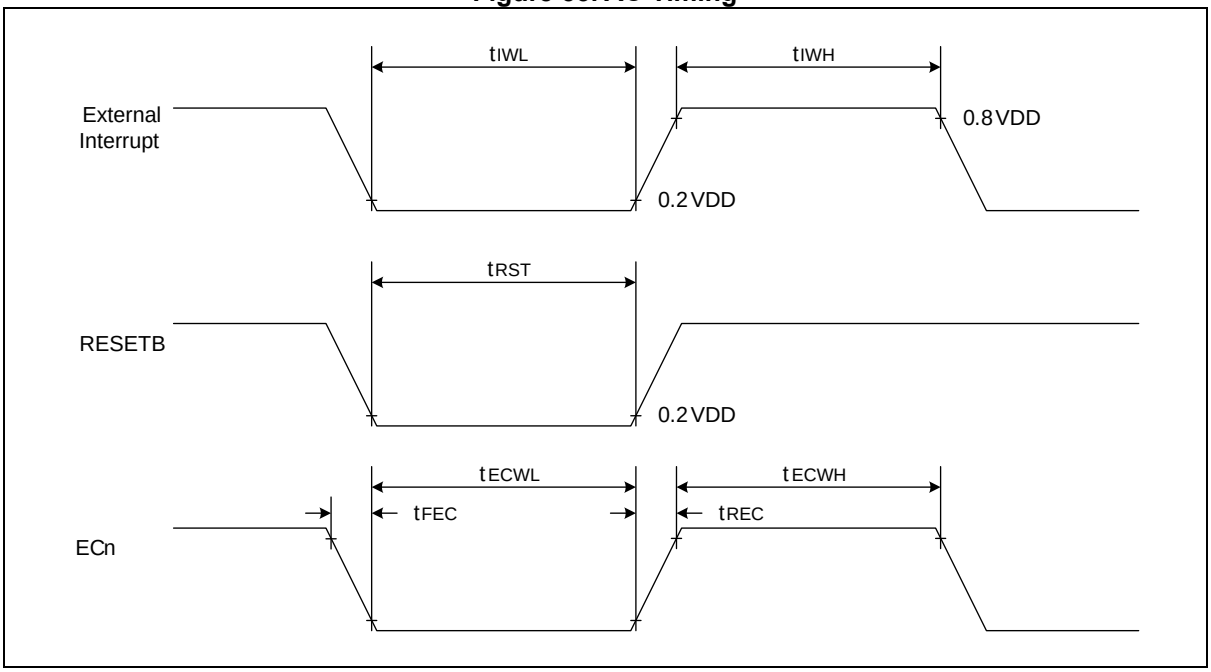


20.14 AC characteristics

Table 37. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 3 V	20	–	–	μs
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 3 V	50	–	–	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	VDD = 3 V All external counter input	1	–	–	$1/f_{PCLK}$
External counter transition time	t_{REC}, t_{FEC}	ECn, VDD = 3 V All external counter input	–	–	10	ns
I/O frequency	f_{IO1}	VDD = 3.0V, C_L = 30pF, All except f_{IO2}	–	–	10	MHz
	f_{IO2}	VDD = 2.7V, C_L = 30pF, SPI pins	–	–	16	

Figure 53. AC Timing

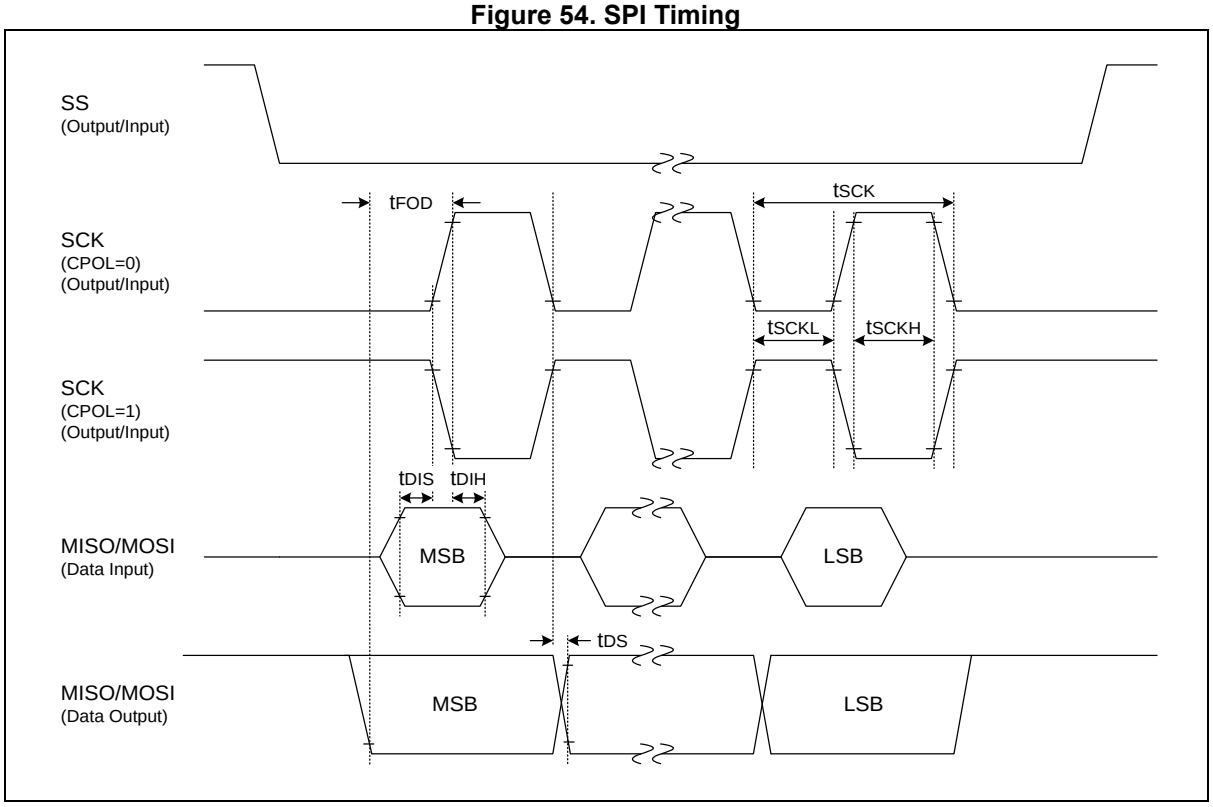


20.15 SPI characteristics

Table 38. SPI Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
SPI clock frequency	f_{SCK}	VDD ≥ 2.7V	Internal SCK source	–	–	16	MHz
			External SCK source				
	f_{SCK}	VDD ≥ 1.71V	Internal SCK source	–	–	12	
			External SCK source				
Input/output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal/External SCK source		0.8*Typ	t_{SCK}/2	1.2*Typ	ns
First output clock delay time	t_{FOD}	Internal/External SCK source, CPHA = 0		0.4*t_{SCK}	–	–	
Output clock delay time	t_{DS}	–		–	–	18	
Input setup time	t_{DIS}			13	–	–	
Input hold time	t_{DIH}			15	–	–	

Figure 54. SPI Timing

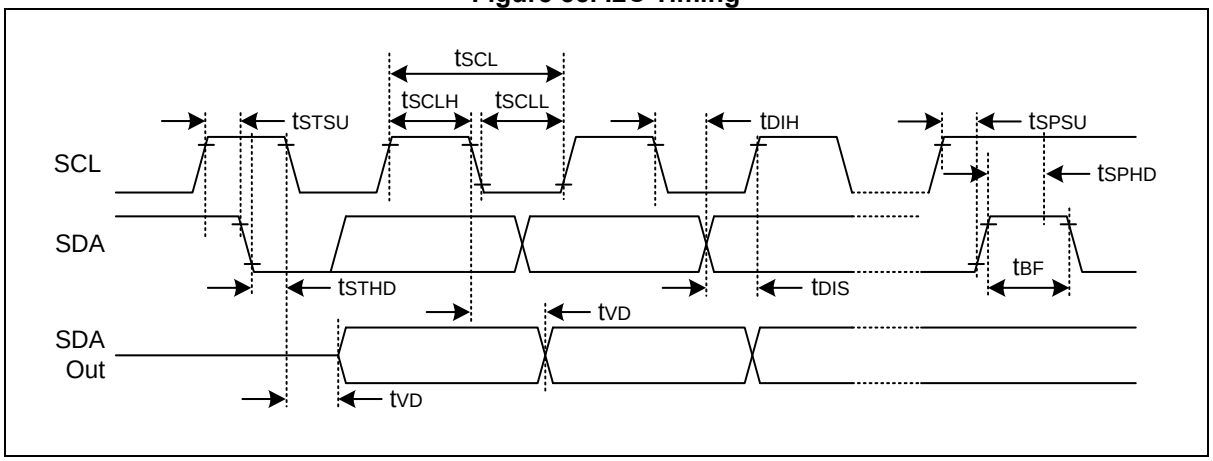


20.16 I2C characteristics

Table 39. I2C Characteristics

Parameter	Symbol	Standard		Fast		Fast Plus		Units
		Min	Max	Min	Max	Min	Max	
I2C operating voltage	–	VDD ≥ 1.71V		VDD ≥ 2V		VDD ≥ 2.7V		–
Clock frequency	t_{SCL}	0	100	0	400	0	1000	kHz
Clock high pulse width	t_{SCLH}	4.0	–	0.6	–	0.26	–	µs
Clock low pulse width	t_{SCLL}	4.7	–	1.3	–	0.5	–	
Bus free time	t_{BF}	4.7	–	1.3	–	0.5	–	
Start condition setup time	t_{STSU}	4.7	–	0.6	–	0.26	–	
Start condition hold time	t_{STHD}	4.0	–	0.6	–	0.26	–	
Stop condition setup time	t_{SPSU}	4.0	–	0.6	–	0.26	–	
Stop condition hold time	t_{SPHD}	4.0	–	0.6	–	0.26	–	
Output valid from clock	t_{VD}	0	–	0	–	0	–	
Data input hold time	t_{DIH}	0	–	0	1.0	0	0.45	
Data input setup time	t_{DIS}	250	–	100	–	50	–	ns

Figure 55. I2C Timing



20.17 UART timing characteristics

Table 40. UART Timing Characteristics (PCLK=32MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	–	–	2000	kHz
Output data setup to clock rising edge	t_{S1}	t_{SCK} x 12/16	–	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	t_{SCK} x 13/16	
Output data hold after clock rising edge	t_{H1}	–	–	50	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	t_{SCK} x 6/16	t_{SCK} x 8/16	t_{SCK} x 10/16	

Figure 56. UART Timing Characteristics

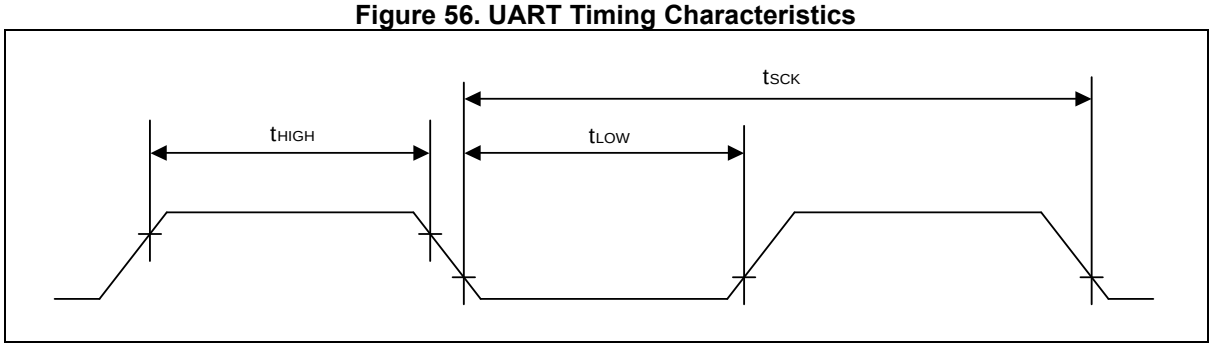
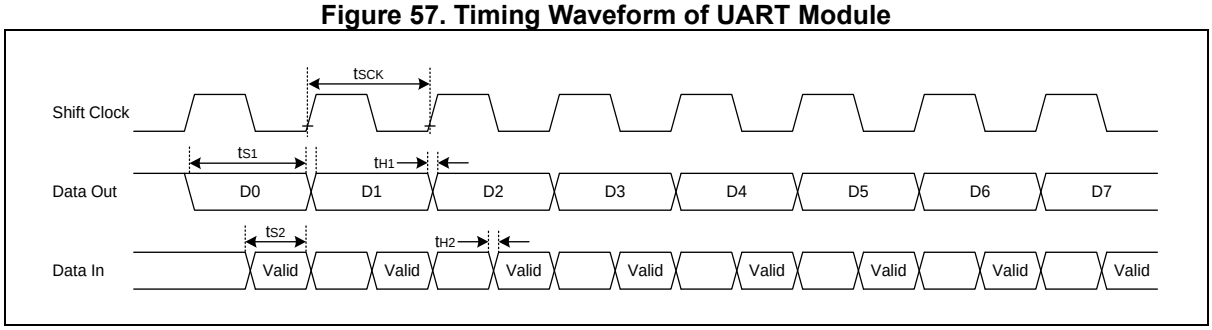


Figure 57. Timing Waveform of UART Module



20.18 Data retention voltage in DEEP SLEEP mode 0/1

Table 41. Data Retention Voltage in DEEP SLEEP Mode 0/1

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.71	–	3.6	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.71V (T_A=25°C) DEEP SLEEP mode 0/1	–	–	1	μA

20.19 Internal Flash memory and Data Flash memory characteristics

Table 42. Internal Flash Memory and Data Flash Memory Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Page write time	t_{FSW}	–		–	3.0	3.5	ms
Page erase time	t_{FSE}	–		–	3.0	3.5	
Chip erase time	t_{FCE}	–		–	3.0	3.5	
Program voltage	V_{PGM}	On erase/write		2.0	–	3.6	V
System clock frequency	f_{HCLK}	–		2.0	–	–	MHz
Flash memory endurance of write/Erase	NF_{FWE}	Page 0 to 511 Configure option page 1	T_A=25 °C, Page unit	10,000	–	–	Cycles
		Configure option page 2/3		100,000			
Data Flash memory endurance of write/erase	NF_{DFWE}	Page 0 to 127	T_A=25 °C, Page unit	100,000	–	–	Cycles
Retention time	t_{FRT}			10	–	–	Years

20.20 Input/ output capacitance

Table 43. Input/ Output Capacitance

(VDD = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input capacitance	C_{IN}	f=1MHz Unmeasured pins are connected VSS	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

20.21 Main oscillator characteristics

Table 44. Main Oscillator Characteristics

(VDD = 1.8V to 3.6V)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	2.7 V to 3.6 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	1.8 V to 3.6 V	2.0	–	4.2	
		2.7 V to 3.6 V	2.0	–	16.0	
External Clock	XIN input frequency	3.0 V to 3.6 V	2.0	–	32.0	MHz
	External Clock Duty Ratio	–	45	50	55	%

Figure 58. Crystal/Ceramic Oscillator

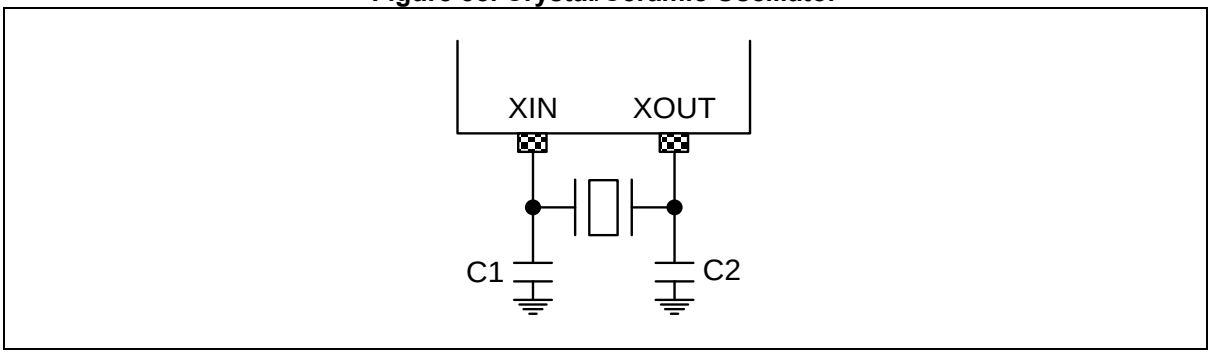
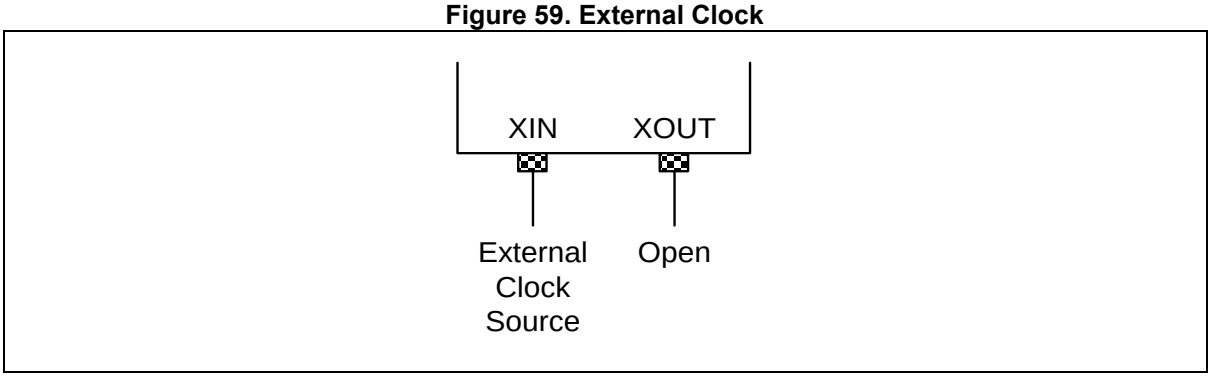


Figure 59. External Clock

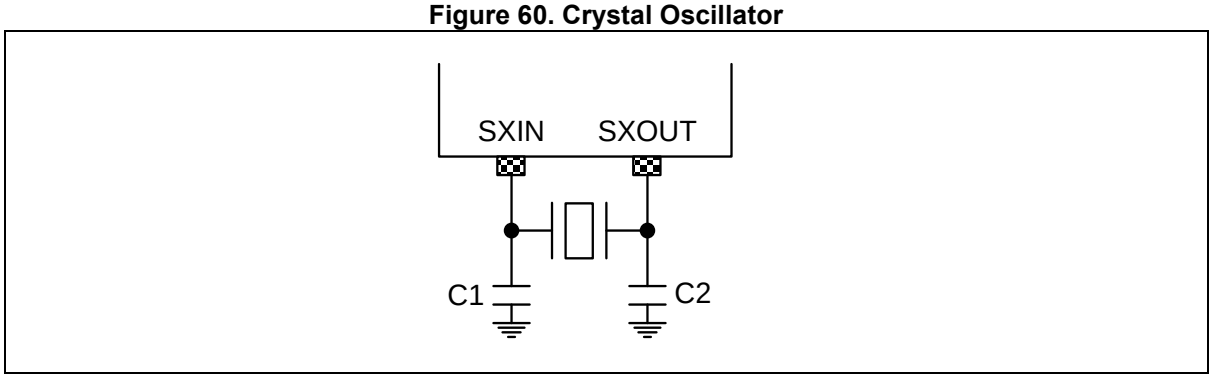


20.22 Sub-oscillator characteristics

Table 45. Sub-oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	1.71 V to 3.6 V	32	32.768	38	kHz

Figure 60. Crystal Oscillator



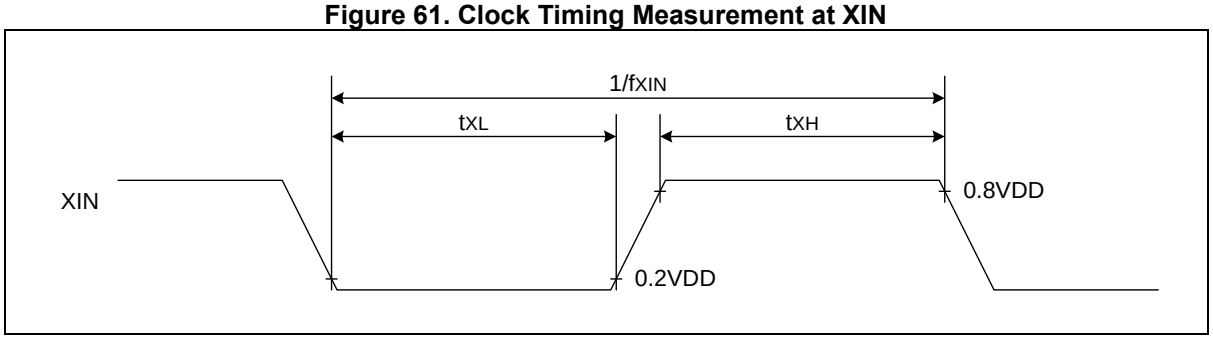
20.23 Main oscillation stabilization time

Table 46. Main Oscillation Stabilization Time

(VDD = 1.8V to 3.6V)

Oscillator	Conditions		Min	Typ	Max	Units
Crystal	f_{XIN} ≥ 2 MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	VDD = 2.7V to 3.6V	–	–	60	ms
Ceramic		VDD = 1.8V to 3.6V	–	–	10	
external clock	f_{XIN} = 2.0 to 32 MHz XIN input high and low width (t_{XL}, t_{XH})		12.5	–	250	ns

Figure 61. Clock Timing Measurement at XIN



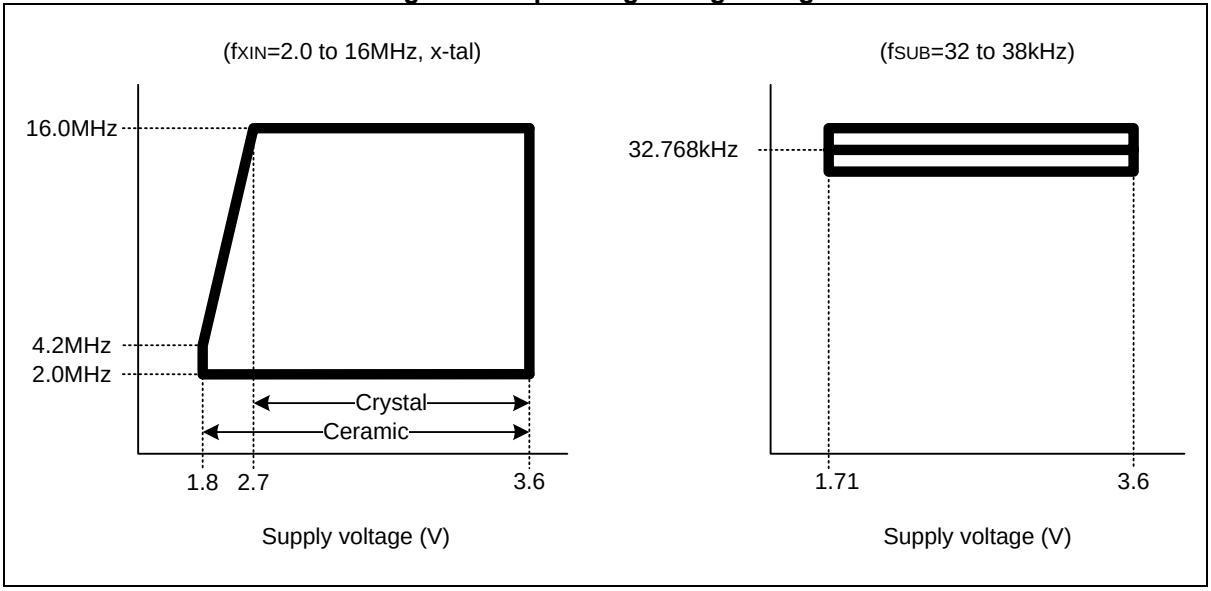
20.24 Sub-oscillation stabilization time

Table 47. Sub-oscillation Stabilization Time

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD=3V, T_A=25 °C, ISET_I[2:0] = 0x7	–	0.7	1.5	

20.25 Operating voltage range

Figure 62. Operating Voltage Range



20.26 Recommended circuit and layout

Figure 63. Recommended Circuit and Layout

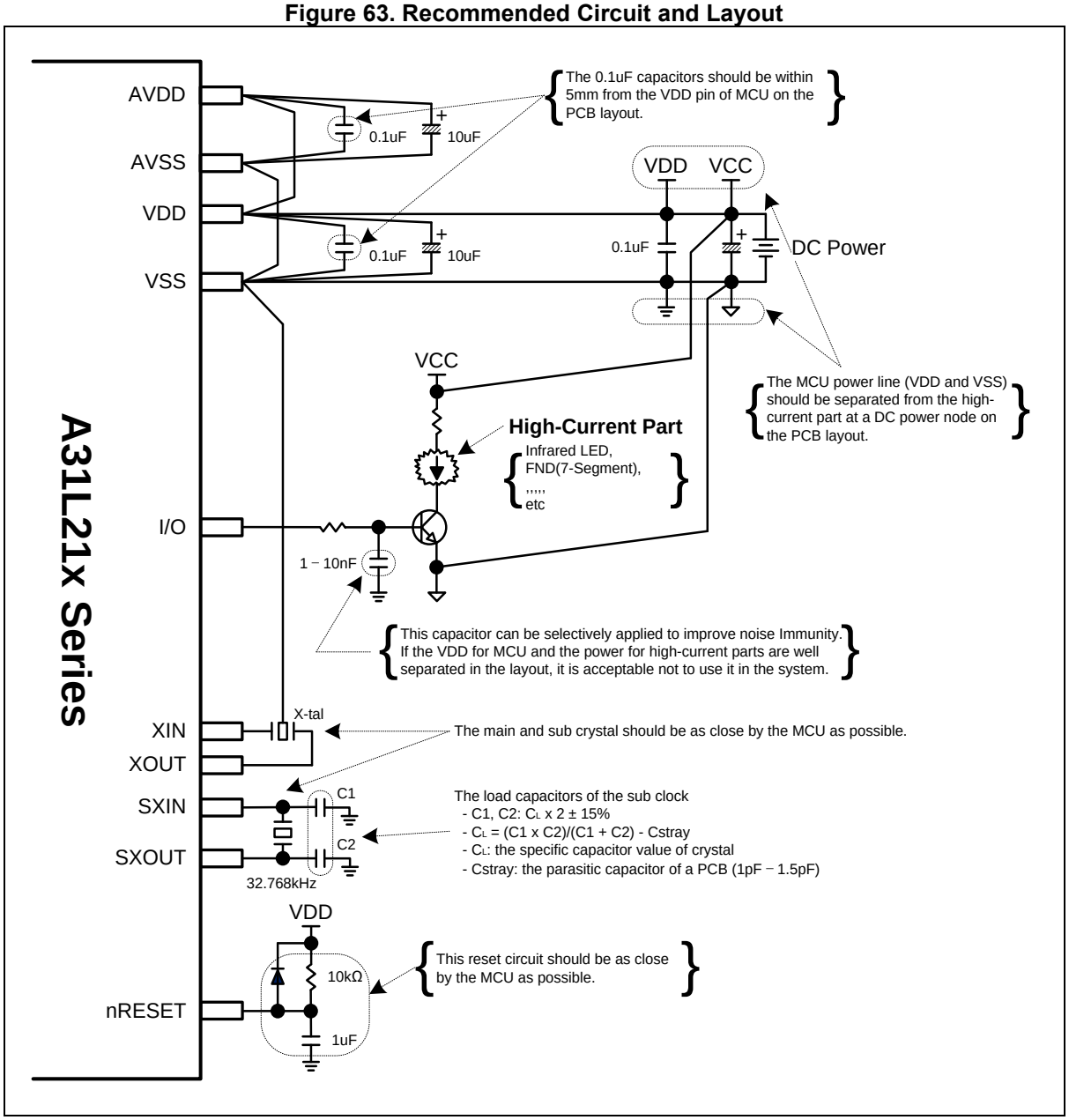
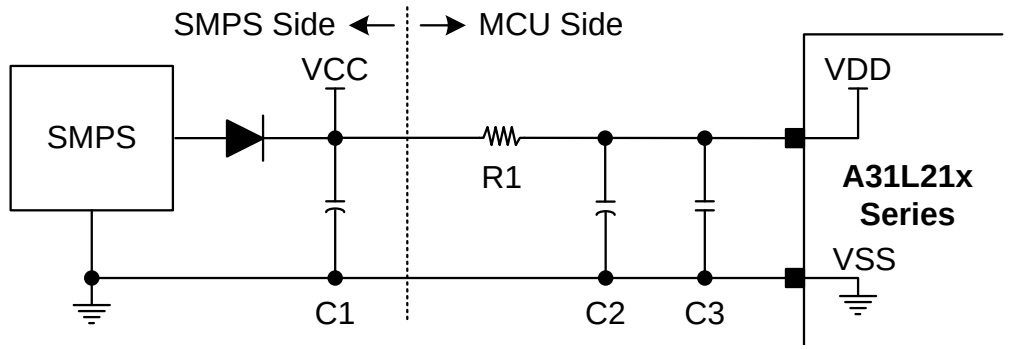


Figure 64. Recommended Circuit and Layout with SMPS Power



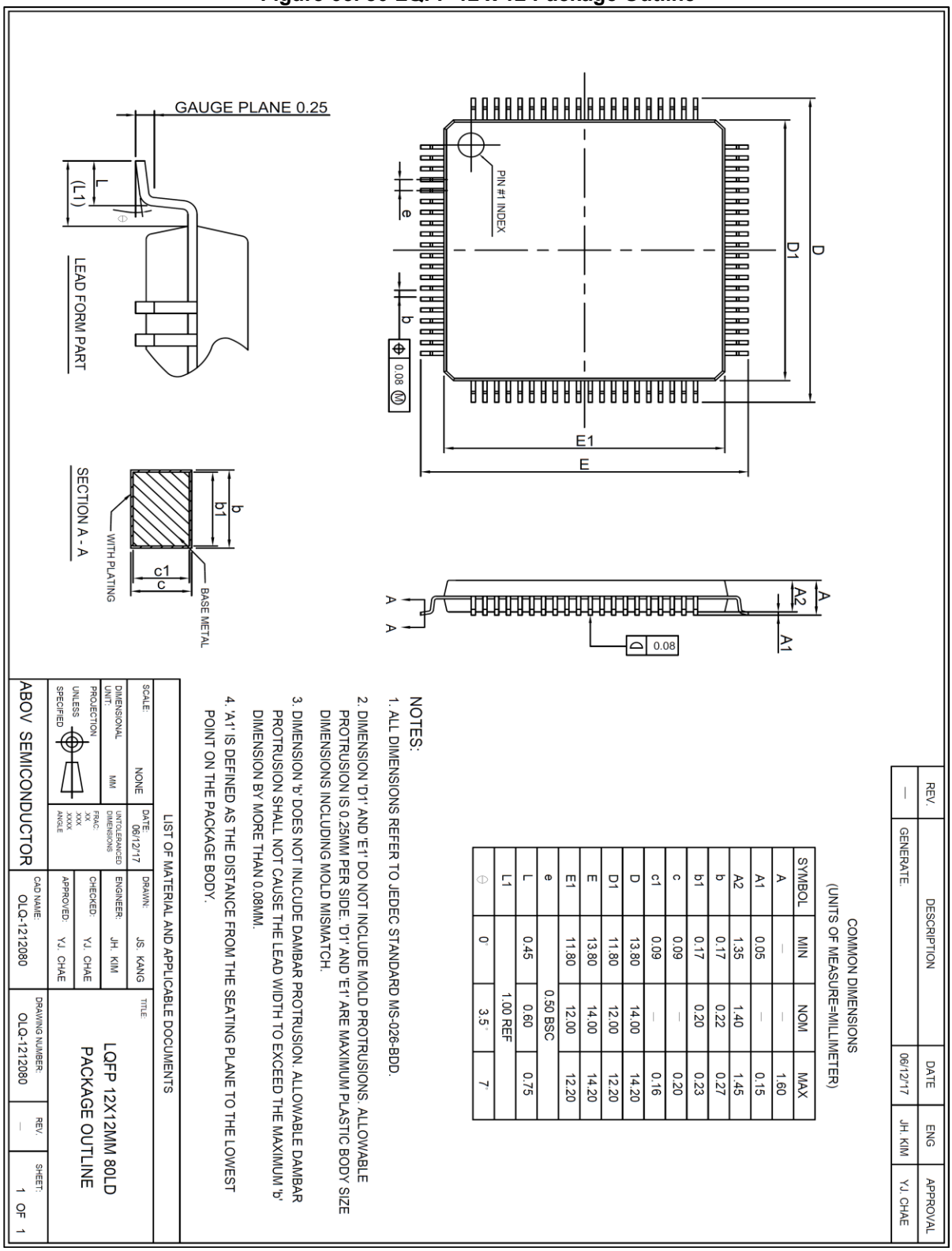
NOTES:

1. The capacitor C1 is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470uF/25V more
2. The resistor R1 and capacitor C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10Ω - 20Ω
   - Recommended C2: 47uF/25V more
   - The R1 and C2 should be as close by the C3 as possible.
3. The capacitor C3 is used for temperature compensation because an electrolytic capacitor becomes worse in characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2uF more.
   - The C3 should be within 1cm from the VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of MCU.

21 Package information

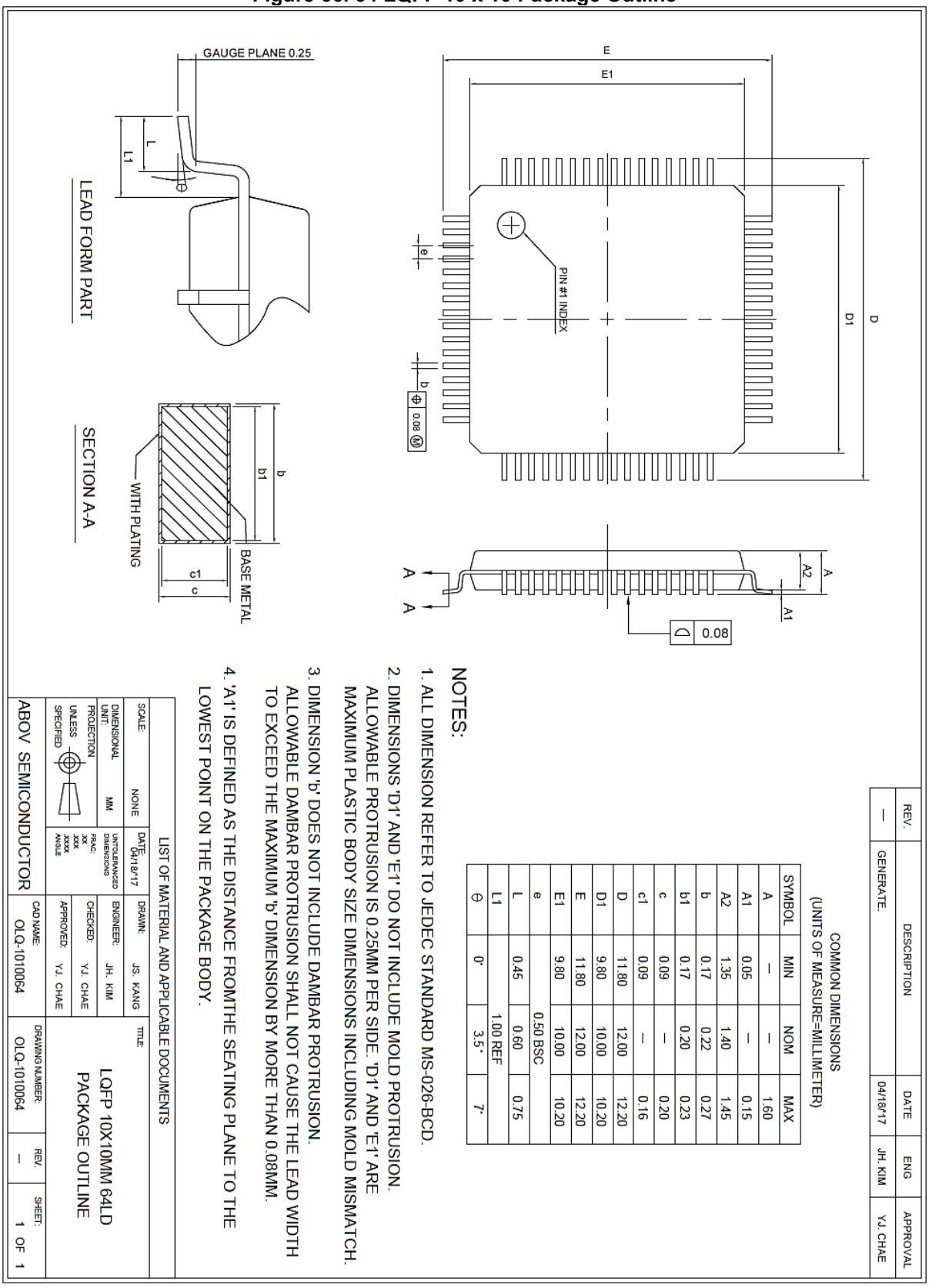
21.1 80 LQFP package information

Figure 65. 80 LQFP 12 x 12 Package Outline



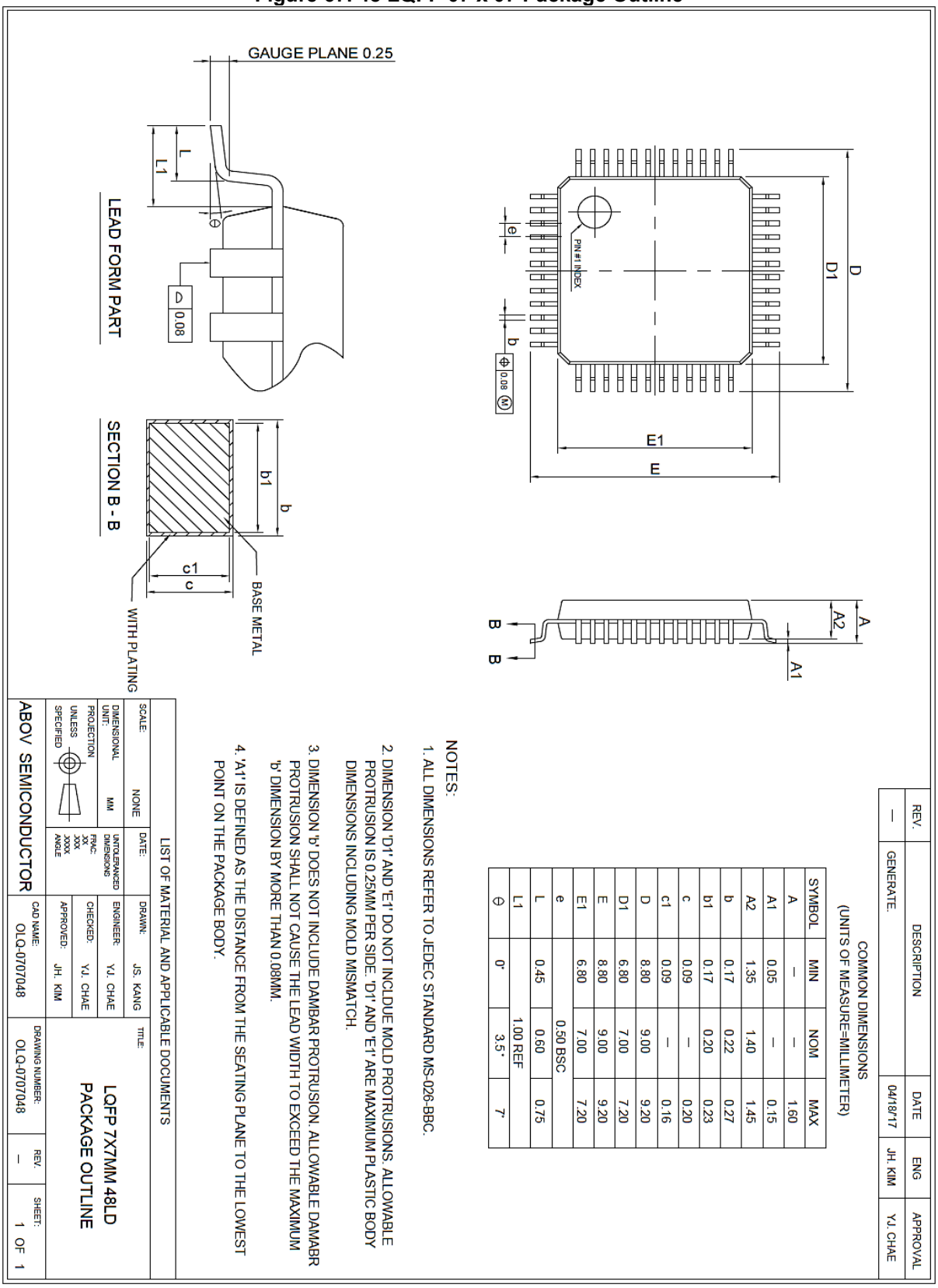
21.2 64 LQFP package information

Figure 66. 64 LQFP 10 x 10 Package Outline



21.3 48 LQFP package information

Figure 67. 48 LQFP 07 x 07 Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

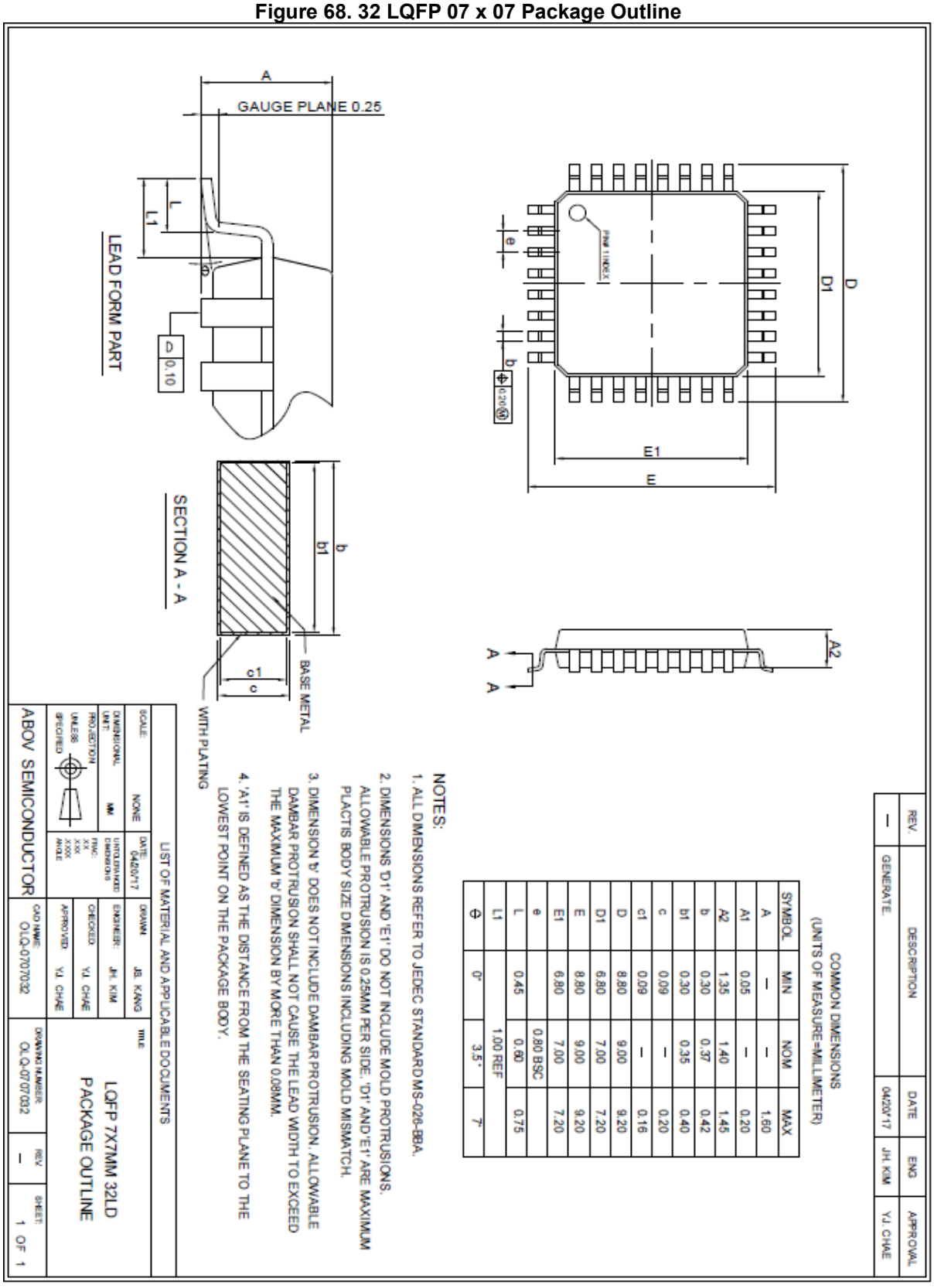
REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: YJ. CHAE	
PROJECTION	FRAC: XX .XX .XXX ANGLE	CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: JH. KIM	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-0707048	DRAWING NUMBER: OLQ-0707048	REV: —
			SHEET: 1 OF 1

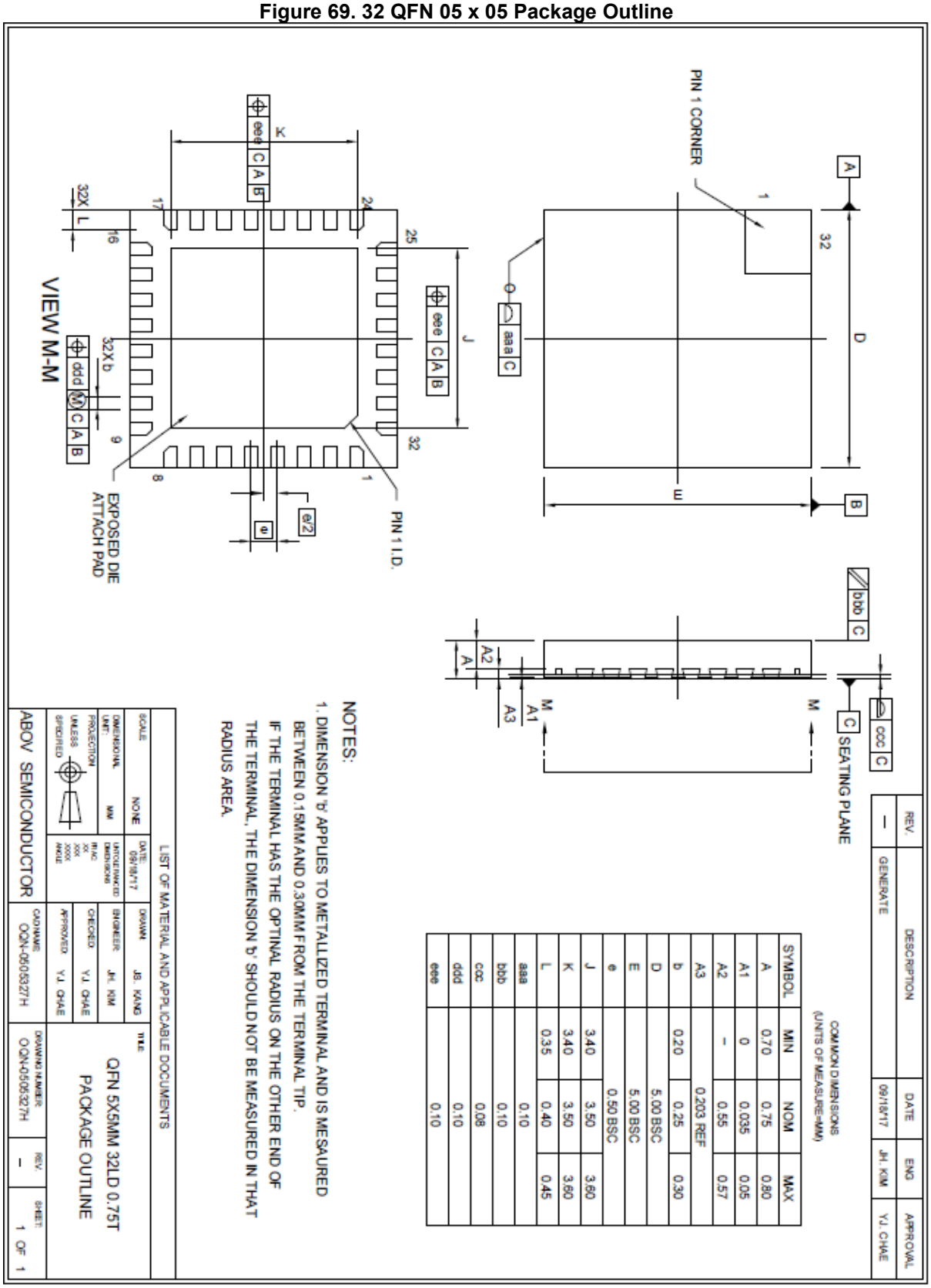
21.4 32 LQFP package information

Figure 68. 32 LQFP 07 x 07 Package Outline



21.5 32 QFN package information

Figure 69. 32 QFN 05 x 05 Package Outline



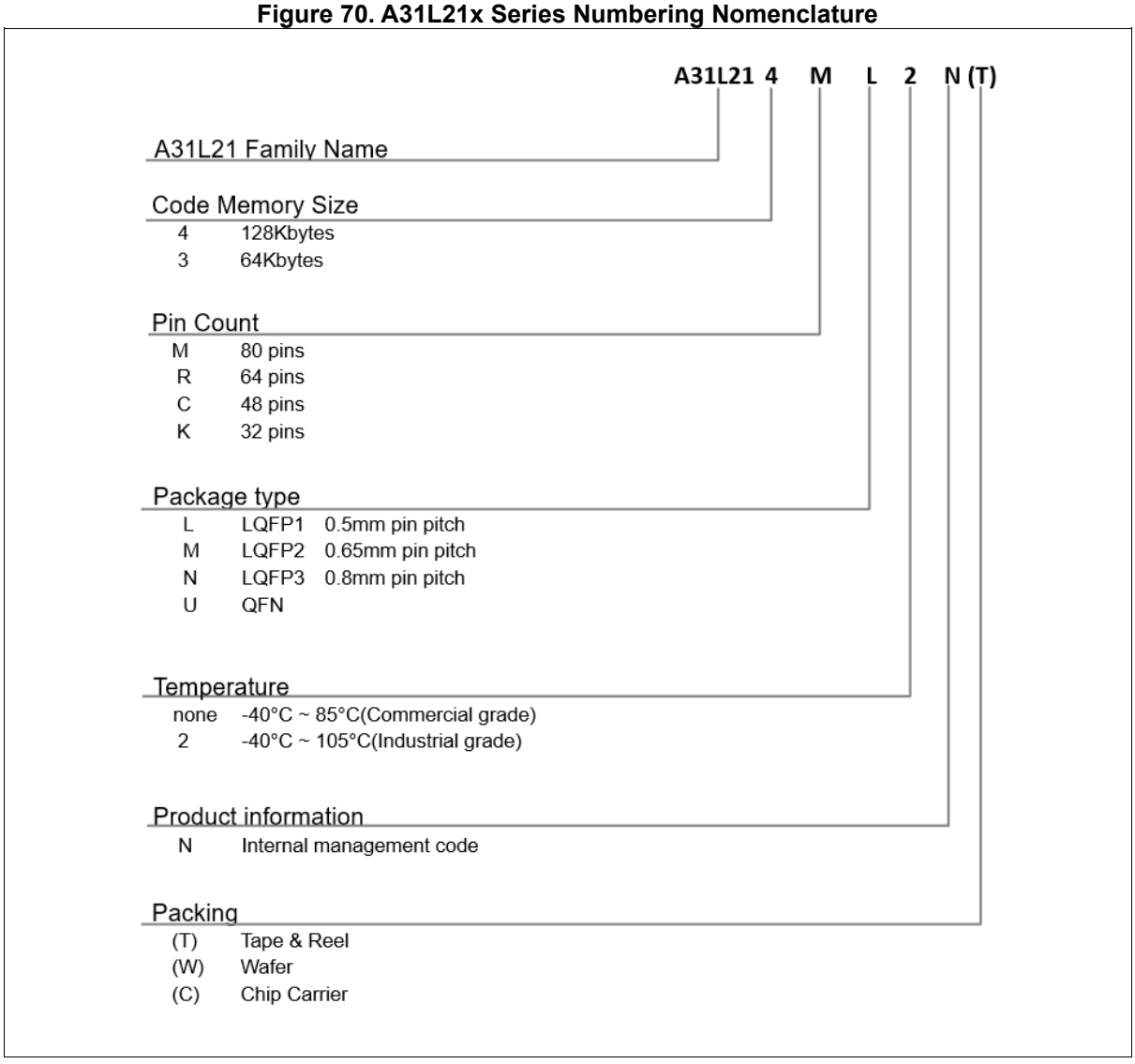
22 Ordering information

Table 48. A31L21x Series Ordering Information

Part Number	Flash	SRAM	USART	UART	LPUART	SC	I2C	SPI	TIMER	LCD	ADC	I/O	Package
A31L214ML	128KB	20KB	2	1	2	1	3	4	9	39x8	16ch	73	80LQFP-1212
A31L214RL*	128KB	20KB	2	1	2	1	3	4	9	27x8	16ch	57	64LQFP-1010
A31L214CL*	128KB	20KB	2	1	2	1	3	3	8	15x4	8ch	41	48LQFP-0707
A31L214KN*	128KB	20KB	2	1	2	1	3	1	3	–	8ch	28	32LQFP-0707
A31L214KU*	128KB	20KB	2	1	2	1	3	1	4	–	8ch	28	32QFN-0505
A31L213ML*	64KB	20KB	2	1	2	1	3	4	9	39x8	16ch	73	80LQFP-1212
A31L213RL*	64KB	20KB	2	1	2	1	3	4	9	27x8	16ch	57	64LQFP-1010
A31L213CL*	64KB	20KB	2	1	2	1	3	3	8	15x4	8ch	41	48LQFP-0707
A31L213KN*	64KB	20KB	2	1	2	1	3	1	3	–	8ch	28	32LQFP-0707
A31L213KU*	64KB	20KB	2	1	2	1	3	1	4	–	8ch	28	32QFN-0505

* For available options or further information on the devices with “*” marks, please contact the ABOV sales offices.

Figure 70. A31L21x Series Numbering Nomenclature



Revision history

Revision	Date	Notes
0.80	Nov. 04, 2021	1st creation
0.90	May. 30, 2022	Preliminary version
0.91	Jul. 4, 2022	Preliminary version
0.92	Aug. 5, 2022	Preliminary version
0.93	Oct. 19, 2022	Preliminary version
0.94	Nov. 1, 2022	Preliminary version

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