32-bit Cortex-M0+ based Microcontroller

FLASH 512KB / SRAM 48KB

A31R118

USER MANUAL

Version 1.0.22

2022.10.31.

SECTION 1. INTRODUCTION

CHAPTER 1. OVERVIEW

1.1 INTRODUCTION

A31R118 is Bluetooth® LE MCU of aBLE product line with competitive edge in power efficiency and various functions essential for Internet-of-Things. The product provides an outstanding Bluetooth® LE wireless communication performance through its advanced patent-pending receiver architecture.
It integrates a 32MHz ARM Cortex-M0+ core, 512KB FLASH, and 48KB RAM to enhance an application performance together with Bluetooth® LE v4.2. Qualified Bluetooth® LE controller stack resides in 128KB ROM and 512KB FLASH is fully dedicated for user applications. As a result, effective usable NVM and RAM size are larger than other conventional Bluetooth® LE MCUs which has whole stack code in NVM.
A31R118 is a member of aBLE product lines and its alias is “Economic BLE.” (aBLE : ABOV Semiconductor Bluetooth Low Energy)

Device Name	Core	Speed	FLASH	SRAM	Package
A31R118	ARM Cortex-M0+	32MHz	512KB	48KB	48 QFN (6x6)

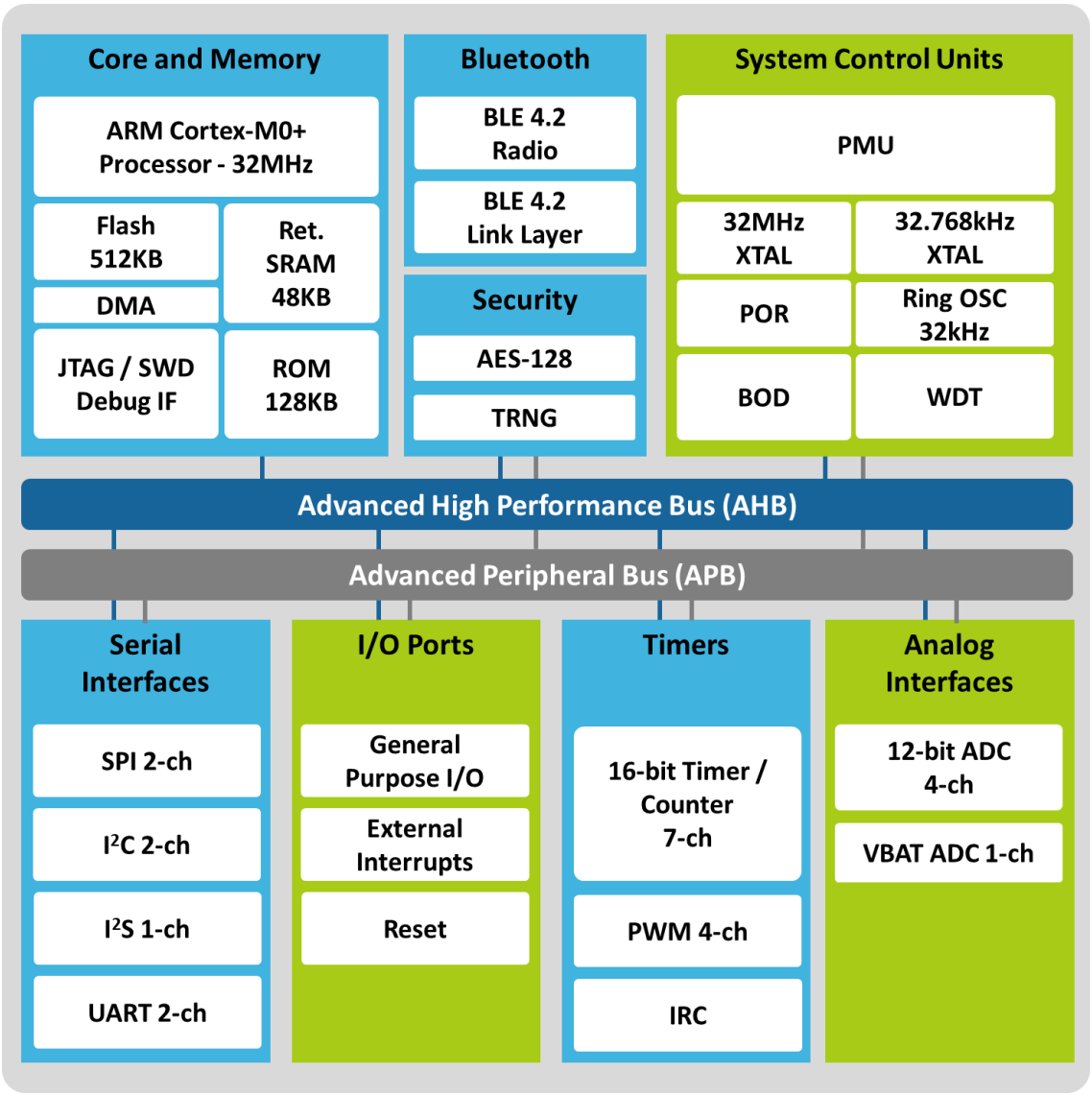


Figure 1.1 Block Diagram

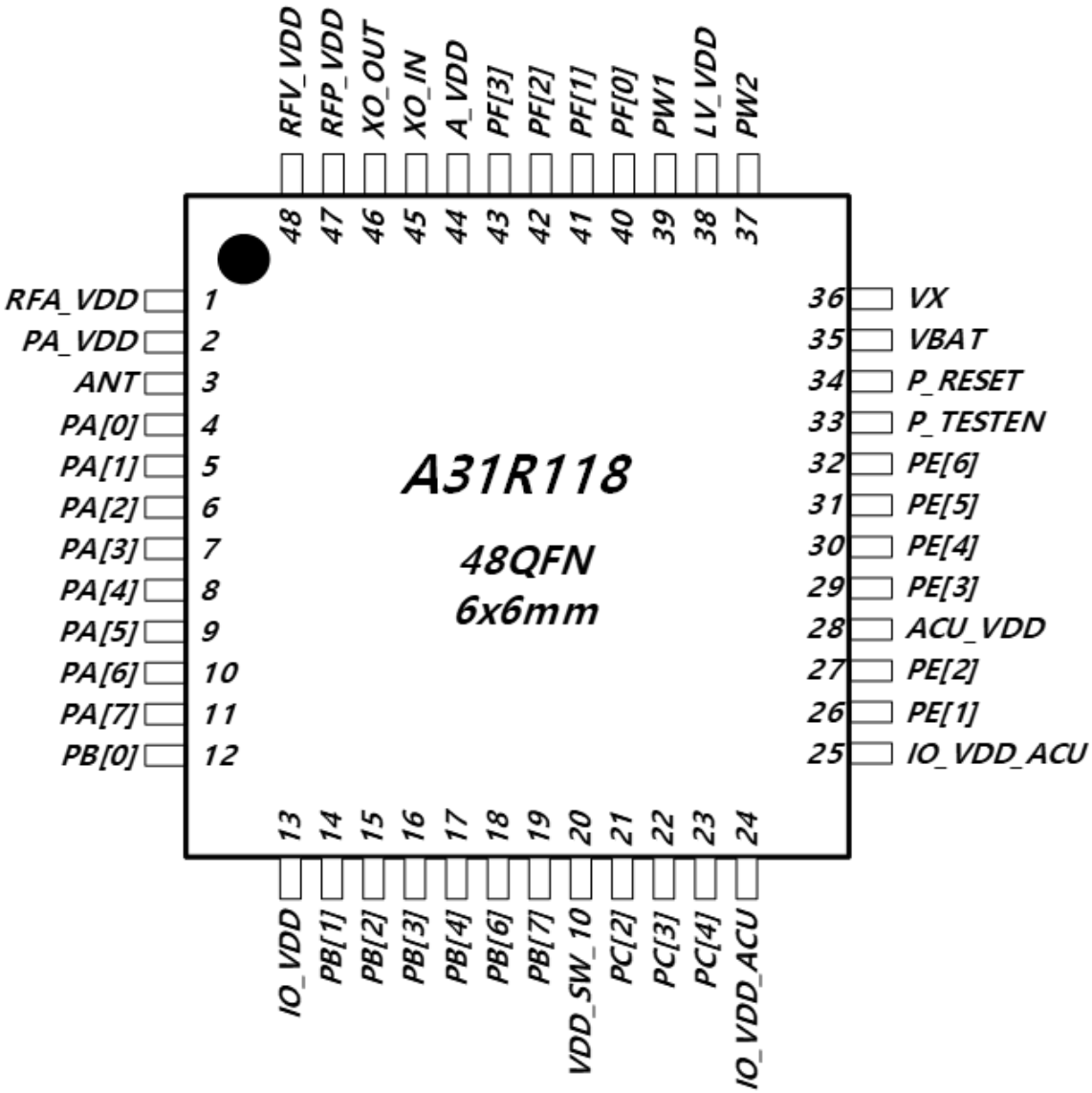


Figure 1.2 Pin layout (48 QFN)

1.2 Product Features

Product features of A31R118 are as below.

- **Microcontroller**
  - **32-bit ARM Cortex-M0+**
  - **32MHz Clock Speed**
  - **48KB Ultra-Low Leakage SRAM (Support Retention Feature)**
  - **512KB FLASH**
  - **128KB ROM (Bluetooth Smart Stack and built-in functions)**
  - **2-Pin SWD**
- **Bluetooth Smart**
  - **Bluetooth® LE v4.2 compliant**
  - **Flexible Transmit power**
    - ✓ **Power mode : up to 0dBm**
  - **Excellent Receiver sensitivity : -94dBm**
    - ✓ **Patent pending advanced receiver architecture**
- **aBLE SDK (Software Development Kit)**
  - **Bluetooth Qualified Host Sub-system**
  - **Flexible application targeting**
    - ✓ **Standalone normal mode**
    - ✓ **Standalone DTM(HCI) mode**
    - ✓ **Core Interface Mode**
    - ✓ **X86 Host emulation mode**
  - **Various example codes and profiles**
  - **aBLE GUI Tool**
- **Power configuration**
  - **Built-in high efficiency DC/DC convertor**
    - ✓ **Buck mode**
  - **Built-in PMU controlling embedded DC/DC and LDOs**
  - **Flexible battery configuration**
    - ✓ **2x 1.5V Battery mode : 1.9~3.6V**
    - ✓ **1x 3V Coin Battery mode : 1.9~3.6V,**
  - **BLE Tx : 9.5mA @ 3V, 0dBm**
  - **BLE Rx : 9.5mA @ 3V**
  - **Deep Sleep : 1300nA @ 3V (RAM retention, 32kHz RC OSC on)**
  - **Hibernate : 900nA @ 3V (RAM retention, CLK off)**
  - **Dormant : 700nA @ 3V (Memory off, CLK off)**
- **Flexible Power down mode**
  - **BLE Idle**
  - **MCU Idle**
  - **Deep Sleep / Hibernate / Dormant**
  - **Stop**
- **High precision analog interface**
  - **12-bit 128ksps SAR-ADC : 5-ch (1-ch dedicated to VBAT monitoring)**
- **Digital MIC interface**

- I2S : PCM MIC
- SPI : PDM MIC with built-in decimation filter

- Digital Audio Output
  - 16-bit PWM audio output
- General Purpose I/O
  - 28 GPIO ports @ 48QFN
  - Key Scan
  - Quadrature Decoder
- Timer / Counter
  - 4-ch 16 bit timer
  - 2-ch 32 bit free run timer
  - 1-ch 32 bit Watch Dog timer
  - 1-ch IR carrier generator
  - 1-ch IR capture
- Peripherals
  - 2-ch UART
  - 2-ch I2C
  - 2-ch SPI
  - 1-ch 16-bit PWM
- Security
  - True Random Number Generator (TRNG)
    - ✓ FIPS 140-2/AIS.31/NIST SP800-22/NIST SP800-90B compliant
  - AES 128-bit Accelerator
- Power On Reset
  - Power On Reset (POR)
  - Brown Out Detection (BOD)
- On-Chip Oscillator
  - 32kHz ROSC
- Crystal Oscillator
  - 32MHz Crystal (mandatory)
  - 32.768kHz Crystal (optional)
- Operating Temperature
  - -30℃ ~ +85℃
- Package Type
  - 6mm x 6mm 48 QFN
  - Available Pb free package

1.3 ARCHITECTURE

1.3.1 Block Diagram

Block diagram of A31R118 is shown as following.

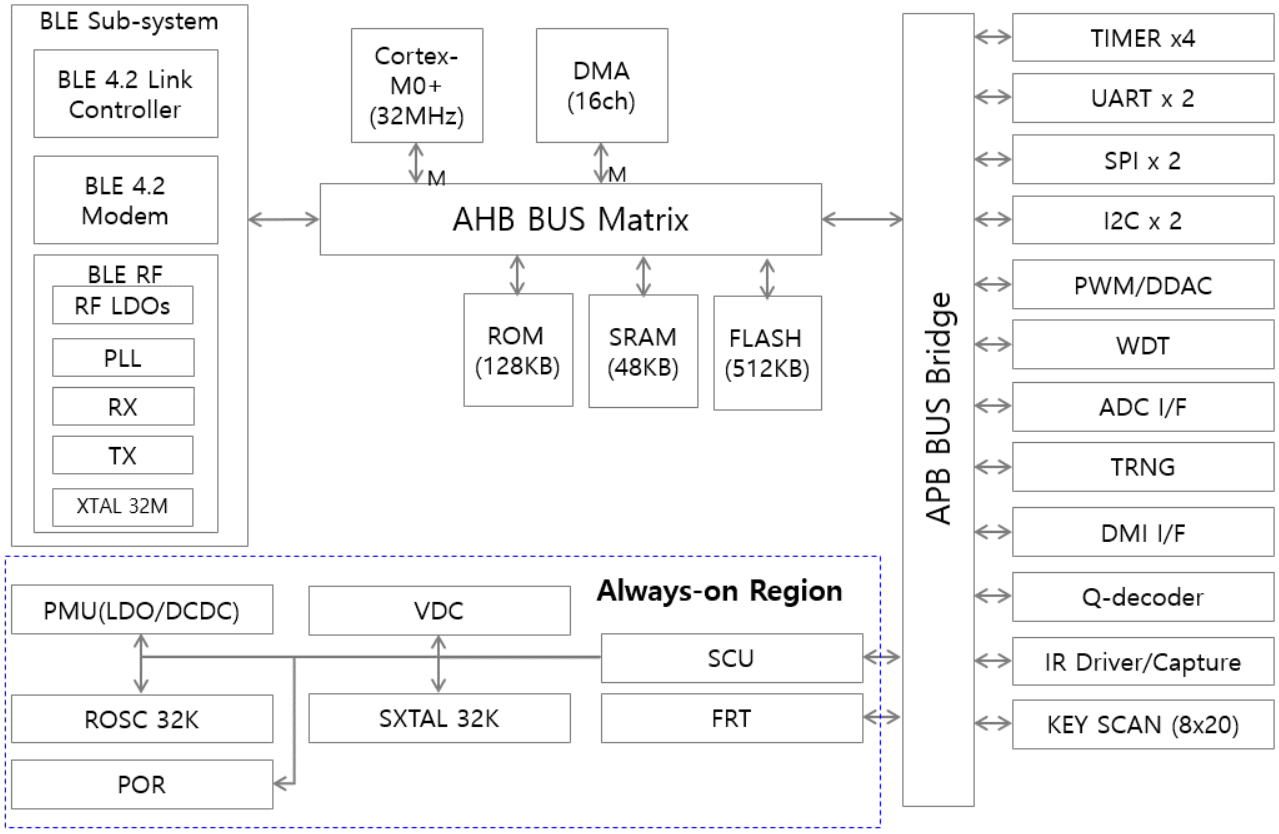


Figure 1.3 Internal Block Diagram

1.3.2 Functional Description

The following section provides an overview of the features of A31R118 microcontroller.

ARM Cortex-M0+

The Cortex-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor.
On core system timer (SYSTICK) provides a simple 24 bit timer to use as a real time operating system (RTOS) or as a simple counter. The processor implements the ARMv6-M Thumb instruction set, including a number of 32-bit instructions that use Thumb-2 technology. Hardware single-cycle multiplication is present.
Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.
SWD debugging features are provided.

Nested Vector-Interrupt Controller (NVIC)

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupts processing and efficient processing of late arriving interrupts.
All NVIC registers are only accessible using word transfers. The result of an attempt to read or write a half word or byte individually is unpredictable.
NVIC registers are always little-endian. Processor accesses are correctly handled regardless of the endian configuration of the processor.

512KB FLASH

A31R118 provides internal 512KB FLASH memory and its controller, dedicated for user applications.

128KB Internal ROM (ROM)

A31R118 provides internal 128KB ROM for qualified Bluetooth Smart controller stack and SW part of link controller.

48KB Internal SRAM (SRAM)

On chip 48KB SRAM can be used for working memory space and program code can be loaded on this SRAM. SRAM consists of 3x16KB SRAM and these can be in retention mode when it is in DEEP_SLEEP.

Direct Memory Access (DMA)

A31R118 provides 16 ch DMA. One channel can be dedicated for memory-to-memory transfer and other channels can be dedicated for each peripheral such as UART, SPI, ADC I/F and QSPI.

BLE Sub-system

BLE sub-system consists of BLE 4.2 link controller, BLE 4.2 RX modem and BLE 4.2 RF. It provides an outstanding Bluetooth® LE wireless communication performance through its advanced patent-pending receiver architecture.

Multi-purpose 16-bit Timer (TIMER)

A31R118 has 4 channels TIMER blocks. They are 16-bit general-purpose timers and support below modes.

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

Universal Asynchronous Receiver/Transmitter (UART)

A31R118 has 2 channels UART blocks. For accurate baud rate control, the fractional baud rate generator is provided.
In addition, UART blocks support up to 1M baud rate and hardware flow control with CTS and RTS.

Serial Peripheral Interface (SPI)

A31R118 has 2 channels SPI blocks, which are used to provide serial communications with external peripherals. SPI blocks support both the master and the slave mode. 4 signals will be used for SPI communication – SS, SCK, MOSI, and MISO.

Inter-Integrated Circuit Interface (I^2C)

A31R118 has 2 channel I^2C blocks and they support standard data rates from 100Kbsp to 400Kbps I^2C communication. The master and the slave modes are supported.

1 Channel PWM

The PWM block is consisted with 2 PWM outputs as a complementary pairs. It can support Dead Time Operation.

Digital DAC (DDAC)

1 channel DDAC (=Digital DAC) module is provided. It can generate 16 bit PWM audio output and internal 16 FIFOs.

32-bit Watchdog Timer (WDT)

The watchdog timer performs system monitoring function. It generates internal reset or interrupt to notice abnormal status of the system.

12-bit Analog-to-Digital Converter (ADC) and It's Interface (ADC I/F)

The ADC can convert analog signal up to 128ksps conversion rate. 5-channel analog MUX provides various combinations from external analog signals, but only 4 externals analog signals can be supported by A31R118.

The ADC I/F can configure ADC analog block and support programmable sample rate and 4 operation mode of Single/Continuous/Burst/All channel mode.

TRNG

FIPS 140-2/AIS.31/NIST SP800-22/NIST SP800-90B compliant

Digital MIC Interface (DMI)

A31R118 provide Digital MIC interface for external digital mic. It support both I2S I/F and PDM I/F, and it has a built-in decimation filter for PDM MIC.

Quadrature Decoder (Quadrature Encoder Interface, QEI)

A31R118 provide one quadrature decoder. The quadrature decoder, known as 2-channel incremental encoder, converts the linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of two signals, it can track the position and the direction. The QEI consists of decoder logic to interpret the Phase A (PhA) and Phase B (PhB) signal and an up/down counter to accumulate the count.

IR Carrier Generator /Capture Control (IR Driver/Capture)

A31R118 provide IR carrier generator and capture block for remocon applications.

Key Scanner (KEY SCAN)

The key scanner supports 8x20 key matrix. It can generate 8 driving pulse signals with the specified timing to driving lines and support 20 sensing inputs.

System Control Unit (SCU)

The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (Oscillator Block, VDC, OSC, BOD and DCDC)

Free-running Timer (FRT)

A31R118 provides two FRTs. One resides in TIMER block and the other resides in Always-on region. FRT support 32 bit timer and the one in AON region can be used in Power-down mode.

General PORT I/Os

PA, PB, PC, PE, and PF ports are available and provide multiple functionalities.

- General I/O port
- Independent bit set/clear function
- External interrupt
- Programmable pull-up, pull-down (except PE and PF), and open-drain selection
- On-chip input de-bounce filter for interrupt ports

Buck DCDC and LDOs

A31R118 provides Buck mode DCDC converter for supporting wide-range of the battery voltages and several LDOs for the lowest sleep-mode current consumption.

Clocks and Resets

A31R118 supports two XTALs of both 32MHz and 32.768kHz(Optional) and one RC Oscillator of 32kHz. In Sleep mode, either of 32.768kHz XTAL or 32kHz RC Oscillator can be used and 32MHz XTAL can be disabled. A31R118 provides internal POR blocks.

1.4 Pin Description

Below pin configuration contains one pair of power/ground and other dedicated pins. The multi-function pins have up to five selections of functions including GPIO.

Table 1.1 Pin Description

Pin No						Pin Name	Type	Description	Remark
48 QFN									
1						RFA_VDD	AP	BLE RF Power (1.0V)	
2						PA_VDD	AP	BLE RF Power (1.9V ~ 3.6V)	
3						ANT	AIO	RF I/O	
4						PA[0]	DIOUDR	Port A Bit 0 Input/Output (Note 1)	Retention I/O
						BB_OUT	AIO	RF Test Output (Debug Purpose)	
5						PA[1]	DIOUDR	Port A Bit 1 Input/Output (Note 1)	Retention I/O
						BB_OUTB	AIO	RF Test Output (Debug Purpose)	
6						PA[2]	DIOUDR	Port A Bit 2 Input/Output (Note 1)	Retention I/O
7						PA[3]	DIOUDR	Port A Bit 3 Input/Output (Note 1)	Retention I/O
8						PA[4]	DIOUDR	Port A Bit 4 Input/Output (Note 1)	Retention I/O
9						PA[5]	DIOUDR	Port A Bit 5 Input/Output (Note 1)	Retention I/O
10						PA[6]	DIOUDR	Port A Bit 6 Input/Output (Note 1)	Retention I/O
11						PA[7]	DIOUDR	Port A Bit 7 Input/Output (Note 1)	Retention I/O
12						PB[0]	DIOUD	Port B Bit 0 Input/Output (Note 1)	
						ADC_3V_CH[0]	AI	ADC 3V Channel Input (Note 2)	
13						IO_VDD	DP	Digital IO Power (1.9V ~ 3.6V) - PA[*] , PB[*] and PC[1:0] are driven by IO_VDD	
14						PB[1]	DIOUD	Port B Bit 1 Input/Output (Note 1)	
						ADC_3V_CH[1]	AI	ADC 3V Channel Input (Note 2)	
15						PB[2]	DIOUD	Port B Bit 2 Input/Output (Note 1)	
						ADC_3V_CH[2]	AI	ADC 3V Channel Input (Note 2)	
16						PB[3]	DIOUD	Port B Bit 3 Input/Output (Note 1)	
						ADC_3V_CH[3]	AI	ADC 3V Channel Input (Note 2)	
17						PB[4]	DIOUD	Port B Bit 4 Input/Output (Note 1)	
18						PB[6]	DIOUD	Port B Bit 6 Input/Output (Note 1)	
19						PB[7]	DIOUD	Port B Bit 7 Input/Output (Note 1)	
20						VDD_SW_10	AP	BLE Analog Power (1.0V)	
21						PC[2]	DIOUD	Port C Bit 2 Input/Output (Note 1)	
22						PC[3]	DIOUD	Port C Bit 3 Input/Output (Note 1)	
23						PC[4]	DIOUD	Port C Bit 4 Input/Output (Note 1)	
24						IO_VDD_ACU	DP	Secondary Digital IO Power (connect to ACU_VDD) - PC[4:2] and PD[*] are driven by IO_VDD_ACU	
25						IO_VDD_ACU	DP	Secondary Digital IO Power	

								(connect to ACU_VDD) - PC[4:2] and PD[*] are driven by IO_VDD_ACU	
26						PE[1]	DIOU	Port E Bit 1 Input/Output (Note 1)	Always-on I/O
						32K_XTAL_IN	AIO	32KHz XTAL I/O	
27						PE[2]	DIOU	Port E Bit 2 Input/Output (Note 1)	Always-on I/O
						32K_XTAL_OUT	AIO	32KHz XTAL I/O	
28						ACU_VDD	DP	ACU LDO Output (1.8V), Flash Power	
29						PE[3]	DIOU	Port E Bit 3 Input/Output (Note 1)	Always-on I/O
30						PE[4]	DIOU	Port E Bit 4 Input/Output (Note 1)	Always-on I/O
31						PE[5]	DIOU	Port E Bit 5 Input/Output (Note 1)	Always-on I/O
32						PE[6]	DIOU	Port E Bit 6 Input/Output (Note 1)	Always-on I/O
33						P_TESTEN	DI	Test Enable (ATE purpose)	
34						P_RESET	DI	External Reset	
35						VBAT	DP	Battery Power (1.9V~3.6V) - PE[*] and PF[*] are driven by VBAT	
36						VX	AIO	DCDC I/O	
37						PW2	AP	DCDC I/O	
38						LV_VDD	AP	DCDC I/O	
39						PW1	AP	DCDC I/O	
40						PF[0]	DIOU	Port F Bit 0 Input/Output (Note 1)	Always-on I/O
41						PF[1]	DIOU	Port F Bit 1 Input/Output (Note 1)	Always-on I/O
42						PF[2]	DIOU	Port F Bit 2 Input/Output (Note 1)	Always-on I/O
43						PF[3]	DIOU	Port F Bit 3 Input/Output (Note 1)	Always-on I/O
44						A_VDD	AP	BLE RF Power (1.0V)	
45						XO_IN	AIO	32MHz XTAL I/O	
46						XO_OUT	AIO	32MHz XTAL I/O	
47						RFP_VDD	AP	BLE RF Power (1.0V)	
48						RFV_VDD	AP	BLE RF Power (1.0V)	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, R=Retention
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, D=Digital, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice
Note 1: Digital Port I/O can be multiplexed with internal function I/O like UART, SPI, … I2C. For details, refer to “Port Control Unit : Function Port Assignment” section.
Note 2: PB[3:0] IOs are shared with Analog IP input signals, so these should not be forced to High input before power-up. If so, it may result in abnormal power-up and mal-function.

1.5 Memory Map

Table 1.2 Main Memory MAP

Start Address	End Address	Size	Description
0x0000_0000	0x0FFF_FFFF	256MB	User Remapped Space. This space will be configured by "REMAP[3:0]" parameter, which will be defined automatically by CHIP operation scenarios. (Please refer to "Mode" sheet) if REMAP = "0000", This space will be mapped to "Boot ROM" region. if REMAP = "0001", This space will be mapped to "OTP" region. if REMAP = "001X", This space will be mapped to "QSPI Slave" region. if REMAP = "01XX", This space will be mapped to "SRAM" region.
0x1000_0000	0x1001_FFFF	128KB	Boot ROM.
0x1002_0000	0x1FFF_FFFF	Reserved	
0x2000_0000	0x2000_3FFF	16KB	SRAM Bank0
0x2000_4000	0x2000_7FFF	16KB	SRAM Bank1
0x2000_8000	0x2000_BFFF	16KB	SRAM Bank2
0x2000_C000	0x2FFF_FFFF	Reserved	
0x3000_0000	0x3000_7FFF	Reserved	
0x3000_8000	0x300F_FFFF	Reserved	
0x3010_0000	0x3010_00FF	Reserved	
0x3010_0100	0x3FFF_FFFF	Reserved	
0x4000_0000	0x4000_00FF	256B	SCU
0x4000_0100	0x4000_01FF	256B	FRT
0x4000_0200	0x4000_02FF	Reserved	
0x4000_0300	0x4000_03FF	Reserved	
0x4000_0400	0x4000_04FF	256B	Port Mux Control PORT E (PMC_PE)
0x4000_0500	0x4000_05FF	256B	Port Mux Control PORT F (PMC_PF)
0x4000_0600	0x4000_0FFF	Reserved	
0x4000_1000	0x4000_10FF	256B	Port Mux Control PORT A (PMC_PA)
0x4000_1100	0x4000_11FF	256B	Port Mux Control PORT B (PMC_PB)
0x4000_1200	0x4000_12FF	256B	Port Mux Control PORT C (PMC_PC)
0x4000_1300	0x4000_13FF	256B	Port Mux Control PORT D (PMC_PD)
0x4000_1500	0x4000_2FFF	Reserved	
0x4000_3000	0x4000_30FF	256B	CORESYS
0x4000_3100	0x4000_31FF	256B	DMA controller
0x4000_3200	0x4000_321F	32B	TIMER0 : 16 bit TIMER
0x4000_3220	0x4000_323F	32B	TIMER1 : 16 bit TIMER
0x4000_3240	0x4000_325F	32B	TIMER2 : 16 bit TIMER
0x4000_3260	0x4000_327F	32B	TIMER3 : 16 bit TIMER
0x4000_32E0	0x4000_32FF	32B	TIMER7 : FRT
0x4000_3300	0x4000_33FF	256B	Watch-dog Timer
0x4000_3400	0x4000_7FFF	Reserved	
0x4000_8000	0x4000_80FF	256B	UART0
0x4000_8100	0x4000_81FF	256B	UART1
0x4000_8200	0x4000_82FF	256B	PWM IP
0x4000_8300	0x4000_83FF	256B	Digital DAC
0x4000_8400	0x4000_8FFF	Reserved	
0x4000_9000	0x4000_90FF	256B	SPI0
0x4000_9100	0x4000_91FF	256B	SPI1
0x4000_9200	0x4000_9FFF	Reserved	
0x4000_A000	0x4000_A0FF	256B	I2C0

0x4000_A100	0x4000_A1FF	256B	I2C1
0x4000_A200	0x4000_AFFF	Reserved	
0x4000_B000	0x4000_B0FF	256B	ADC IP
0x4000_B100	0x4000_B1FF	256B	TRNG IP
0x4000_B200	0x4000_B2FF	Reserved	
0x4000_B300	0x4000_B3FF	256B	DMI(=Digital MIC Interface) IP - PDM Input I/F or I2S Input I/F
0x4000_B400	0x4000_BFFF	Reserved	
0x4000_C000	0x4000_C0FF	256B	Q-Decoder
0x4000_C100	0x4000_CFFF	Reserved	
0x4000_D000	0x4000_D0FF	256B	Key Scan
0x4000_D100	0x4000_D1FF	256B	IR Carrier Generator/Capture Control
0x4000_D400	0x4000_FFFF	Reserved	
0x5000_0000	0x5000_1FFF	8KB	BLE Link Controller
0x5000_2000	0x5000_3FFF	8KB	BLE Modem
0x5000_4000	0x5FFF_FFFF	Reserved	
0x6000_0000	0x6007_FFFF	512KB	QSPM Slave A31R118 : Flash Memory Region
0x6008_0000	0x600F_FFFF	Reserved	
0x6010_0000	0x6EFF_FFFF	Reserved	
0x6F00_0000	0x6FFF_FFFF	16MB	QSPM Control Register
0x7000_0000	0xDFFF_FFFF	Reserved	
0xE000_0000	0xE00F_FFFF	1MB	Private Peripheral Bus (CM0+ internal)
0xE010_0000	0xFFFF_FFFF	Reserved	

CHAPTER 2. CPU

2.1 Cortex-M0+ Core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0 processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

2.2 Interrupt Controller

Table 2.1 Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Exception
-13	0x0000_000C	Hard Fault Exception
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Exception
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Exception
-1	0x0000_003C	SysTick Exception
0	0x0000_0040	Reserved
1	0x0000_0044	Clock Fail Interrupt
2	0x0000_0048	DMA Interrupt
3	0x0000_004C	WDT Interrupt
4	0x0000_0050	TIMER0 Interrupt
5	0x0000_0054	TIMER1 Interrupt
6	0x0000_0058	TIMER2 Interrupt
7	0x0000_005C	TIMER3 Interrupt
8	0x0000_0060	PWM Interrupt
9	0x0000_0064	Key Scanner Interrupt
10	0x0000_0068	DDAC Interrupt
11	0x0000_006C	TIMER7(=FRT at TIMER) Interrupt
12	0x0000_0070	FRT(at Always-on) Interrupt
13	0x0000_0074	QSPI Interrupt
14	0x0000_0078	DMI Interrupt
15	0x0000_007C	PortA Interrupt
16	0x0000_0080	PortB Interrupt
17	0x0000_0084	PortC Interrupt
18	0x0000_0088	PoerD Interrupt
19	0x0000_008C	PortE Interrupt
20	0x0000_0090	PortF Interrupt
21	0x0000_0094	QEI Interrupt
22	0x0000_0098	UART0 Interrupt
23	0x0000_009C	UART1 Interrupt
24	0x0000_00A0	BLE Interrupt

25	0x0000_00A4	IR Interrupt
26	0x0000_00A8	SPI0 Interrupt
27	0x0000_00AC	SPI1 Interrupt
28	0x0000_00B0	I2C0 Interrupt
29	0x0000_00B4	I2C1 Interrupt
30	0x0000_00B8	ADC I/F Interrupt
31	0x0000_00BC	TRNG Interrupt

CHAPTER 3. Boot Mode

3.1 Boot Mode Pins

The A31R118 has 3 boot mode pins and they are described below.

Table 3.1 Boot mode pin list

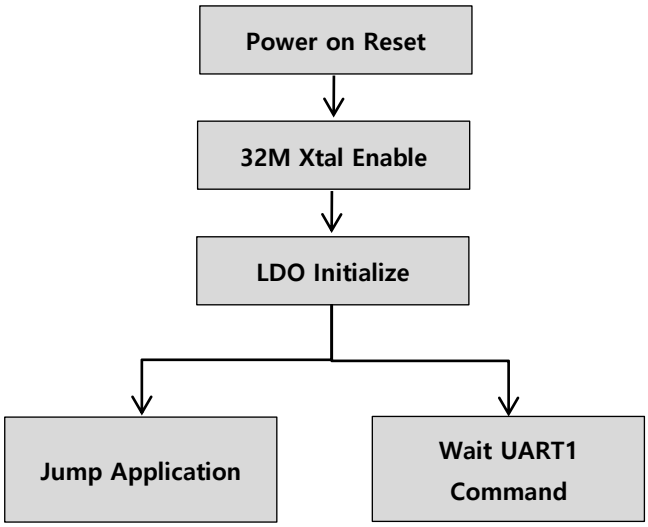
Pin Name	Dir	Description
P_TESTEN	I	Test Enable 0 : Function Mode 1 : Test Mode (reserved)
PF[3]	I	When P_TESTEN is “LOW”, PE[3] = 0 : External Battery voltage ranged in 1.9V~3.6V and DCDC operate in BUCK mode. PE[3] = 1 : Reserved
PE[6]	I	When P_TESTEN is “LOW”, PF[6] = 0 : Normal Booting PF[6] = 1 : Debug Booting

3.2 Boot Mode Description

The following section provides an overview of boot mode of A31R118 microcontroller.

Normal Booting
After power on reset, bootloader runs as in the following flowchart.

Debug Booting
In debug booting mode, it does not jump to application and waits for UART1 command.



Note: PB[3:0] IOs are shared with Analog IP input signals, so these should not be forced to High input before power-up. If so, it may result in abnormal power-up and mal-function.

CHAPTER 4. Low Power Mode

4.1 Low Power State

The following figure shows A31R118's Low Power State Diagram, which consists of 6 states.

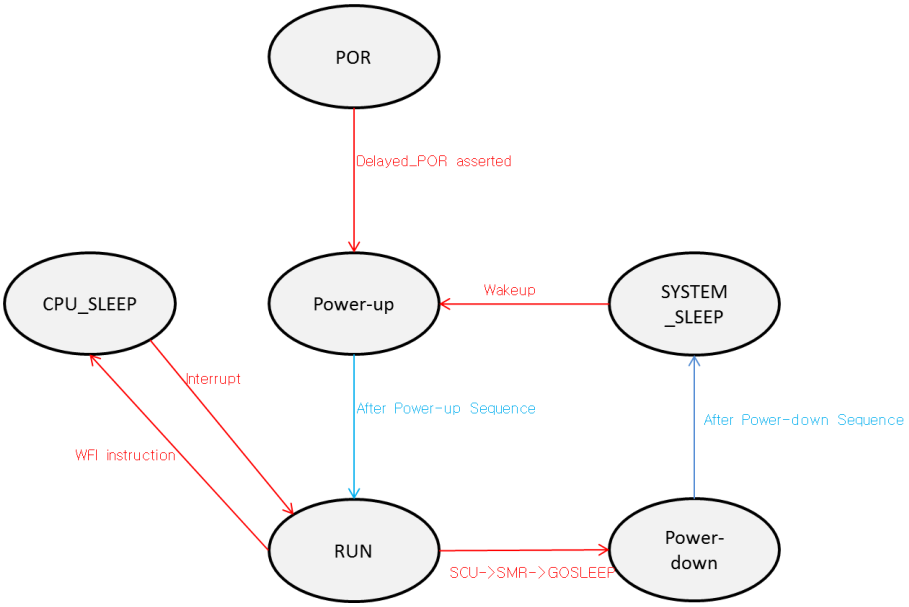
On power-up, internally generated POR signal causes the device to be in the "POR" state. POR signals need to be delayed by internal low power clocks, before being used for digital reset signal. After some delay, the device enters the "Power-up" state and then transitions to the "RUN" state. During "Power-up" state, the internal dedicated HW logic performs the power-up procedures including the enablement of DCDC/LDO/32M_XTAL. After completing the power-up procedures, the device will enters the "RUN" state and stays until SW-driven low-power mode request.

There are two major low power modes: CPU_SLEEP and SYSTEM_SLEEP.

SW can make the device to enter the "CPU_SLEEP" state by invoking "WFI" instruction, which is supported by CortexM0+ processor. Any interrupt will make the device to exit the "CPU_SLEEP" state and go back to "RUN" State. It takes very short time to enter into and exit from the "CPU_SLEEP" state, because all of DCDC/LDO/XTAL is always on during the "CPU_SLEEP" state.

SW can also make the device to enter the "SYSTEM_SLEEP" state by setting "SCU->SMR->GOSLEEP" parameter. (= GOSLEEP parameter at SMR register in SCU Block). Before entering the "SYSTEM SLEEP" state, the device goes through the "Power-down" state and in which the internal dedicated HW logic performs power-down procedures like DCDC/LDO/32M_XTAL disabling. After completing power-down procedure, the device will enter the "SYSTEM SLEEP" state.

There are several options when entering the "SYSTEM_SLEEP" State. Users can make the internal SRAM in retention mode and disable all the clocks including low-power clock for the lowest power consumption (in this case, only external Port I/O can wake-up the system). Refer to SMR registers in SCU block for details. Any of the wakeup or external reset signal makes the device to exit from "SYSTEM SLEEP" state. In order for the device to transition from the "SYSTEM_SLEEP" to the "RUN" state, power-up procedure is required. It takes much longer time to enter into and exit from the "SYSTEM_SLEEP" state compared to the "CPU_SLEEP", because of the settling time of DCDC/LDO/XTAL IPs. This wake-up time must be evaluated at system-level and then need to be tuned by PWRCON0/1/2/3 registers at SCU block.



4.2 Low Power Mode

The following table shows “Low Power Mode” supported by A31R118 and the corresponding hardware blocks that are powered-on or powered-off.

When the device is in “RUN” state, “NORMAL” and “BLE_IDLE” modes are supported at A31R118.
“NOMAL” mode is normal operation mode and all the blocks are powered-on. When “BLE_IDLE” mode, BLE sub-system is in SLEEP state, which means that BLE RF module is powered-off and other BLE modem/link controller are in idle state (=clock-off).

When the device is in “CPU_SLEEP” state, only “MCU_IDLE” mode is possible. As described before, MCU_IDLE mode is invoked by “WFI" instruction, supported by CortexM0+, and is terminated by any interrupts.

Low Power State	Low Power Mode	BLE RF	Logic			SRAM	OSC (Low frequency)	External Battery
			Power-off Region	MCU	Always-on			
RUN	NORMAL	ON	ON	ON	ON	ON	ON	ON
	BLE_IDLE	OFF	ON(CLK OFF)	ON	ON	ON	ON	ON
CPU_SLEEP	MCU IDLE	OFF	ON(CLK OFF)	ON(CLK OFF)	ON	ON	ON	ON
SYSTEM_SLEEP	DEEP_SLEEP	OFF	OFF	OFF	ON	RETENTION	ON	ON
	HIBERNATE	OFF	OFF	OFF	ON	OFF	ON	ON
	DORMANT	OFF	OFF	OFF	ON	OFF	OFF	ON
POR	STOP	OFF	OFF	OFF	OFF	OFF	OFF	OFF

When the device is in the “SYSTEM_SLEEP” state, there are 3 possible modes: “DEEP_SLEEP”, ”HIBERNATE”, and ”DORMANT” mode. The following table shows the additional descriptions for these modes. Wake-up time and Current Consumption will be filled later)
In “DEEP SLEEP” mode, all parts except for always-on block, low power retention LDO, 32KHz low power clock, and retention SRAM will be off. Always-on GPIO and always-on Timer can wake up the device.
In “HIBERNATE” mode, all parts except for always-on block, low power retention LDO and 32KHz low power clock will be off. The effective wake-up time from “HIBERNATE” will be longer than “DEEP_SLEEP” mode, because SW needs to restore SRAM contents after wake-up. As similar to “DEEP_SLEEP”, Always-on GPIO and always-on timer can wake up the device.
When “DORMANT” state, all parts except for Always-on block and low power retention will be off and the current consumption will be the smallest. Only GPIO can wakeup the device. The effective wake-up time will be longer than “HIBERNATE” mode, because it needs low power clock settling time.

Power Mode	Description	Wake-up Source	Wake-up time	Current Consumption
DEEP_SLEEP	wake up by wake-up pin (GPIOs) or by the wake-up timer Always-on block & Low power retention LDO ON SRAM in Retention Mode 32K OSC(or XTAL) ON, Other Clocks Off	GPIO pin & Wake-up Timer	Max 5 ms	- 1300 nA
HIBERNATE	wake up by wake-up pin or by the wake-up timer Always-on block & Low power retention LDO OFF 32K OSC(or XTAL) ON, Other Clocks Off	GPIO pin & Wake-up Time	Max 5 ms	- 900 nA

DORMANT	Wake-up by wake-up pin (GPIOs) Always-on block & Low power retention LDO OFF All clocks off.	GPIO pin	Max 5 ms	- 700 nA

SECTION 2. PERIPHERALS

CHAPTER 1. SYSTEM CONTROL UNIT (SCU)

1.1 OVERVIEW

The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (VDC, OSC, BOD and DCDC)

1.2 REGISTERS

The base Address of SCU is 0x4000_0000 and register map is described in Table 1.1

Table 1.1 SCU Register Map

Name	Offset	R/W	Description	Reset
CIDR	0x0000	R	CHIP ID Register	0xA3101120
SMR	0x0004	R/W	System Mode Register	0x00000002
SCR	0x0008	R/W	System Control Register	0x00000000
WSER	0x0010	R/W	Wake up source enable register	0x00000000
WSSR	0x0014	R/W	Wake up source status register	0x00000000
RSER	0x0018	R/W	Reset source enable register	0x00000069
RSSR	0x001C	R/W	Reset source status register	0x00000080
PRER1	0x0020	R/W	Peripheral reset enable register 1	0x000000C5
PER1	0x0028	R/W	Peripheral enable register 1	0x000000C5
PCER1	0x0030	R/W	Peripheral clock enable register 1	0x000000C5
CSCR	0x0040	R/W	Clock Source Control register	0x00000008
SCCR	0x0044	R/W	System Clock Control register	0x00000002
CMR	0x0048	R/W	Clock Monitoring register	0x00000009
PMUCON1	0x0060	R/W	PMU Control register	0x00004202
ACUCON	0x0074	R/W	ACU Control register	0x00000049
BLECON	0x007C	R/W	BLE Control Register	0x00000000
EMODR	0x0084	R/W	External mode pin read register	0x00000100
MCCR1	0x0090	R/W	Miscellaneous Clock Control register 1	0x00000022
SWREG	0x00B4	R/W	SW Always-on Register	0x00000000

1.2.1 CIDR Chip ID Register

CHIP ID Register shows chip identification information. This register is 32-bit read-only register.

CIDR=0x4000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID																															
0xA310_1120																															
RO																															

31 0	CHIP ID	Device ID 0xA310_1120

1.2.2 SMR System Mode Register

SMR=0x4000_0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				RCLKOFF	Reserved			Reserved			GOSLEEP	Reserved	CURMODE		
0x00000																				0	0x0			0x0			0	0	0	1	0
-																				RW	-			-			RW	-	RO	RO	RO

11	RCLKOFF	Low clock frequency control when entering SYSTEM SLEEP	
		0	RCLK will be on
		1	RCLK will be off
4	GOSLEEP	When writing this parameter by '1' and CURMODE is RUN mode, System will be entering into SYSTEM SLEEP.	
2 0	CURMODE	Current Power State	
		0	POR State
		1	Power-up State
		2	RUN State
		4	Power Down State
		5	SYSTEM SLEEP State

1.2.3 SCR System Control Register

SCR=0x4000_0008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											DS_IND	Reserved			SWRST
0x0000000																											0	0x0			0
-																											RW	-			RW

4	DS_IND	Deep Sleep Indicator Control	
		0	DS_IND signal will be HIGH, when chip is in both Power-down and SYSETM_SLEEP state
		1	DS_IND signal will be LOW, when chip is in both Power-down and SYSETM_SLEEP state
0	SWRST	Internal soft reset activation bit	
		0	Normal operation
		1	Internal soft reset is applied and auto cleared

1.2.4 WSER Wakeup Source Enable Register

Enable wakeup source when the chip is in the SYSETE_SLEEP mode. Wakeup sources which will be used the source of chip wakeup should be enabled in each bit field. Writing ‘1’ enables the corresponding wakeup source, and writing “0” disables it.

WUER=0x4000_0010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		GPIOFWUE	GPIOEWUE	Reserved							BLEWUE	FRTWUE	Reserved		
0x00000																		0	0	0x00							0	0	0x0		
-																		RW	RW	-							RW	RW	-		

13	GPIOFWUE	Enable wakeup source of GPIOF port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
12	GPIOEWUE	Enable wakeup source of GPIOE port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
4	BLEWUE	Enable wakeup source of BLE Sleep Timer event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
3	FRTWUE	Enable wakeup source of FRT Timer event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation

1.2.5 WUSR Wakeup Source Status Register

When the system wakes up by any of the wakeup sources, they are identified by reading this register. When the bit is set to "1", the related wakeup source issues the wakeup to the SCU. The bit is cleared when the event is cleared by the software.

WUSR=0x4000_0014

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11 10 9 8	7 6 5	4	3	2 1 0
Reserved			PINRST	GPIOFWU	GPIOEWU	Reserved		BLEWU	FRTWU	Reserved
0x00000			0	0	0	0x00		0	0	0x0
-			RO	RO	RO	-		RO	RO	-

14	PINRST	Status of wakeup source of PIN Reset Event
	0	No wakeup event
	1	Wakeup event was generated
13	GPIOFWU	Status of wakeup source of GPIOF port pin change event
	0	No wakeup event
	1	Wakeup event was generated
12	GPIOEWU	Status of wakeup source of GPIOE port pin change event
	0	No wakeup event
	1	Wakeup event was generated
4	BLEWU	Status of wakeup source of BLE Sleep timer event Note) This bit will be cleared by writing WSER->BLEWUE by '0'.
	0	No wakeup event
	1	Wakeup event was generated
3	FRTWU	Status of wakeup source of FRT timer event
	0	No wakeup event
	1	Wakeup event was generated

1.2.6 RSER Reset Source Enable Register

The reset source, which generates the reset event, can be selected by RSER register. When writing “1” in the bit field of each reset source, the reset source event will be transferred to the reset generator. When writing “0” in the bit field of each reset source, the reset source event is masked and will not generate the reset event.

RSER=0x4000_0018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									PINRST	CPURST	SWRST	WDTRST	Reserved	MCKFRST	LVDRST
0x0000000																									1	1	0	1	0	0	1
-																									RW	RW	RW	RW		RW	RW

6	PINRST	External pin reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
5	CPURST	CPU request reset enable bit Note) CPURST can only reset CPU sub-system.
		0 Reset from this event is masked
		1 Reset from this event is enabled
4	SWRST	Software reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
3	WDTRST	Watchdog Timer reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
1	MCKFRST	MCLK(=32MHz XTAL) Clock fail reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
0	LVDRST	LVD reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled

1.2.7 RSSR Reset Source Status Register

The RSSR shows the reset source information when reset event occurs. “1” indicates reset event exists and “0” indicates reset event does not exist for corresponding reset source. Writing “1” into the corresponding bit will clear the reset status. This register is 8-bit register.

RSSR=0x4000_001C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			PORST	PINRST	CPURST	SWRST	WDTRST	Reserved	MCKFRST	LVDRST
0x000000			1	0	0	0	0	0	0	0
-			RC1	RC1	RC1	RC1	RC1		RC1	RC1

7	PORST	Power on reset status bit
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status
6	PINRST	External pin reset status bit
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status
5	CPURST	CPU request reset status bit Note) CPURST can only reset CPU sub-system.
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status
4	SWRST	Software reset status bit
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status
3	WDTRST	Watchdog Timer reset status bit
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status
1	MCKFRST	MCLK Clock fail reset status bit
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status
0	LVDRST	LVD reset status bit
	0	Read : Reset from this event was not exist Write : no effect
	1	Read :Reset from this event was occurred Write : Clear the status

1.2.8 PRER1 Peripheral Reset Enable Register 1

The reset of each peripheral by reset event, can be masked by user setting. PRER register will control the enable of the event reset. If the corresponding bit is '1', the peripheral corresponded with this bit, accepts the reset event. Otherwise, the specific peripheral is protected from reset event and maintains the current operation.

PRER1=0x4000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								GPIOF	GPIOE	Reserved	RFC	BLE_SLEEP	PORTCON	FRT	SCU
0x000000																								1	1	0	0	0	1	0	1
-																								RW	RW	RW	RW	RW	RW	RW	RW

7	GPIOF	GPIOF reset mask
6	GPIOE	GPIOE reset mask
4	RFC	RF Controller reset mask
3	BLE_SLEEP	BLE Sleep Timer reset mask
2	PORTCON	Port controller reset mask
1	FRT	FRT Timer reset mask
0	SCU	System Control Unit reset mask

1.2.9 PER1 Peripheral Enable Register 1

To use peripheral unit, it should be activated by writing “1”to the correspond bit in the PER0/1 register. Before the activation, the peripheral will stay in reset state.
All the peripherals enabled by default. To disable the peripheral unit, write “0” to the correspond bit in the PER0/1 register, and then the peripheral enter the reset state.

PER1=0x4000_0028

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			GPIOF	GPIOE	Reserved	RFC	BLE_SLEEP	PORTCON	FRT	SCU
0x000000			1	1	0	0	0	1	0	1
-			RW	RW	RW	RW	RW	RO	RW	RO

7	GPIOF	GPIOF function enable
6	GPIOE	GPIOE function enable
4	RFC	RF Controller function enable
3	BLE_SLEEP	BLE Sleep Timer function enable
2	PORTCON	Port controller function enable
1	FRT	FRT Timer function enable
0	SCU	System Control Unit function enable

1.2.10 PCER1 Peripheral Clock Enable Register 1

To use peripheral unit, its clock should be activated by writing '1'to the correspond bit in the PCER0/1 register. Before enabling its clock, the peripheral will not operate properly.

To stop the clock of the peripheral unit, write '0'to the correspond bit in the PCER0/1 register, and then the clock of the peripheral is stopped.

PCER1=0x4000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								GPIOF	GPIOE	Reserved	RFC	BLE_SLEEP	PORTCON	FRT	SCU
0x000000																								1	1	0	0	0	1	0	1
-																								RW	RW	RW	-	RW	RO	RW	RO

7	GPIOF	GPIOF clock enable
6	GPIOE	GPIOE clock enable
4	RFC	RF Controller clock enable
3	BLE_SLEEP	BLE Sleep Timer clock enable
2	PORTCON	Port controller clock enable
1	FRT	FRT Timer clock enable
0	SCU	System Control Unit clock enable

1.2.11 CSCR Clock Source Control Register

The ADKREF has multiple clock sources to generate internal operating clocks. Each clock sources can be controlled by CSCR register. This register is 8-bit register.

CSCR=0x4000_0040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										SUBOSCCON		RINGOSCCON		EOSCCON	
0x0000000																										00		10		00	
-																										RW		RW		RW	

5 4	SUBOSCCON	Low frequency external XTAL control (32.768kHz)	
		0X	Stop external sub oscillator
		1X	Enable external sub oscillator
3 2	RINGOSCCON	Low frequency Internal ring oscillator control (32.768kHz)	
		0X	Stop internal sub oscillator
		1X	Enable internal sub oscillator
1 0	EOSCCON	External 32MHz XTAL control, when SYSTEM SLEEP mode	
		00	Disable external oscillator LDO & external oscillator
		01	Enable external oscillator LDO & Disable external oscillator
		10	Enable external oscillator
		11	Reserved

1.2.12 SCCR System Clock Control Register

The ADKREF has multiple clock sources to generate internal operating clocks. Each clock sources can be controlled by SCUCSCR register.

SCCR=0x4000_0044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													CLKDBLSEL	MCLKSEL	LCLKSEL
0x00000000																													0	1	0
-																													RW	RW	RW

2	CLKDBLSEL (Note 1)	Clock Doubler Select	
		0	Not use clock doubler
		1	Use clock doubler
1	MCLKSEL	System clock (MCLK) select register	
		0	MCLK = RCLK
		1	MCLK = External crystal oscillator (32MHz)
0	LCLKSEL	Low Power Clock Select Register	
		0	LCLK = Internal ring oscillator (32.768kHz)
		1	LCLK = External sub oscillator (32.768kHz)

Note 1 : Clock doubler block must be enabled before setting CLKDBLSEL parameter by '1'.

1.2.13 CMR Clock Monitoring Register

Internal clock can be monitored by internal sub oscillator for safety purpose.
Clock Monitoring Register is 16-bit register.

CMR=0x4000_0048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																MCLKREC	Reserved			SOSCEN	SOSCFIEN	SOSCFAIL	SOSCSTS	Reserved				MAINOSCEN	MAINOSCFIEN	MAINOSCFAIL	MAINOSCSTS
0x0000																0	0x0			0	0	0	0	0x0				1	0	0	1
-																RO	-			RW	RW	RC1	RC1	-				RW	RW	RC1	RC1

15	MCLKREC	MCLK fail auto recovery
		0 MCLK is changed to RINGOSC by default when MCLKFAIL issued
		1 MCLK auto recovery is disabled
11	SOSCEN	SOSC(32K XTAL) monitoring enable
		0 SOSC monitoring disabled
		1 SOSC monitoring enabled
10	SOSCFIEN	SOSC(32K XTAL) fail interrupt enable
		0 SOSC fail interrupt disabled
		1 SOSC fail interrupt enabled
9	SOSCFAIL	SOSC(32K XTAL) fail interrupt
		0 SOSC fail interrupt not occurred
		1 Read : SOSC fail interrupt is pending Write : Clear pending interrupt
8	SOSCSTS	SOSC(32K XTAL) clock status
		0 No clock is present on SOSC
3	MAINOSCEN	External main oscillator(32M XTAL) monitoring enable
		0 External main oscillator monitoring disabled
		1 External main oscillator monitoring enabled
2	MAINOSCFIEN	External main oscillator(32M XTAL) fail interrupt enable
		0 External main oscillator fail interrupt disabled
		1 External main oscillator fail interrupt enabled
1	MAINOSCFAIL	External main oscillator(32M XTAL) fail interrupt
		0 External main oscillator fail interrupt not occurred
		1 Read : External main oscillator fail interrupt is pending Write : Clear pending interrupt
0	MAINOSCSTS	External main oscillator(32M XTAL) status
		0 Not oscillate
		1 External main oscillator is working normally

1.2.14 PMUCON1 PMU IP Control Register 1

PRER1=0x4000_0060

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11 10	9 8	7	6	5	4	3	2	1 0
Reserved		NBGR_ST	PBGR_ST	PMU_DLO_BYPS	DCDC_SET_BYP	Reserved	INT_LDO_CONT	Reserved	PMU_LDO_PEN	PBGR_PEN	DCDC_LDO_PEN	DCDC_PEN	DCDC_BOB	DCDC_PSW_CONT
0x0000		0	1	0	0	0x0	1 0	0	0	0	0	0	0	1
-		RW	RW	RW	RW	-	RW RW	-	RW	RW	RW	RW	RW	RW

15	NBGR_ST (RSV[13])	(NBGR_ST) External BGR Soft-start control bit when SYSTEM SLEEP mode
14	PBGR_ST (RSV[12])	(PBGR_ST) External BGR Soft-start control Note) Not used because it is Reserve bit
13	PMU_LDO_BYPS (RSV[11])	(PMU_LDO_BYPS) PMU_LDO Bypass bit
12	DCDC_SET_BYPS (RSV[7])	Assignment to "DCDC_SET_BYPS" 0 DCDC_SET = DCDC_PEN 1 After the Initial Start-Up, set DCDC_SET to High
9 8	INT_LDO_CONT (RSV[2:1])	DCDC External Load control bits when System Sleep mode 00 Turn-off 01 100 uA 10 400 uA 11 500 uA
6	PMU_LDO_PEN	PMU LDO Power Enable when SYSTEM SLEEP mode 0 Disable 1 Enable
5	PBGR_PEN	PMU BGR Power Enable when SYSTEM SLEEP mode 0 Disable 1 Enable
4	DCDC_LDO_PEN	DCDC Internal LDO PEN when SYSTEM SLEEP mode 0 Disable 1 Enable
3	DCDC_PEN	DCDC Converter Power Enable when SYSTEM SLEEP mode 0 Disable 1 Enable
2	DCDC_BOB	DC-DC Converter Mode Selection when SYSTEM SLEEP mode 0 Buck Mode 1 Reserved
1 0	DCDC_PSW_CONT	PSW Mode Selection when SYSTEM SLEEP mode 00 Short 01 LDO Connect 10 DC-DC Connect 11 Open

1.2.15 ACUCON ACU Control Register

PRER1=0x4000_0074

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9	8	7	6 5	4	3	2	1	0
Reserved			POC	RESET	LDO_CONT	2P3V_EN	1P8V_EN	1P5V_EN	BYPASS	LDO_PEN
0x000000			0	0	10	0	1	0	0	1
-			RW	RW	RW	RW	RW	RW	RW	RW

8	POC	POC Signal for remocon ACU Note) This Pin must be HIGH when ACU power-down
7	RESET	RESET Signal for remocon ACU Low Active
6 5	LDO_CONT	ACU LDO output trimming
4	2P3V_EN	ACU LDO output 2.3V mode
3	1P8V_EN	ACU LDO output 1.8V mode
2	1P5V_EN	ACU LDO output 1.5V mode
1	BYPASS	ACU LDO Bypass
0	LDO_PEN	ACU LDO enable control

1.2.16 BLECON BLE Control Register

PRER1=0x4000_007C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															WKUP_REQ
0x00000000																															0
-																															RW

0	WKUP_REQ	Wakeup Signal for BLE Sleep Timer

1.2.17 EMODR External Mode Status Register

External Mode Status Register shows external mode pin status while booting.
This register is 8-bit register.

EMODR=0x4000_0084

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FPGA	Reserved																										TEST_EN	BOOT			
0x0000000																															
RO	-																										RO	RO			

31	FPGA	0 : ASIC, 1 : FPGA
4	TEST_EN	TEST_EN pin level
3 0	BOOT	BOOT pin level BOOT[3] = PF[3] BOOT[2] = PF[2] BOOT[1] = PE[6] BOOT[0] = PE[5]

TEST_EN	PF[3]	PE[6]	Chip Type	PWR mode
0	0	0	Normal	Buck
0	0	1	Debug	

1.2.18 MCCR1 Miscellaneous Clock Control Register 1

The ADKREF can drive the clock from internal MCLK clock with dedicated post divider. This register is 32-bit register.

MCCR1=0x4000_0090

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved			PORTSEL	PORTDIV
0x000000			0x1	0x00
-			RW	RW

9 8	PORTSEL	PORT E/F DEBOUNCE Clock source select bit	
		00	MCLK (AHB clock)
		01	PCLK (APB clock)
		10	SUB Clock (32.768kHz)
		11	Reserved
7 0	PORTDIV	PORT E/F DEBOUNCE Clock N divider	
		8'h0	Clock disabled
		8'h1	PORT E/F DEBOUNCE clock /2
		8'h2	PORT E/F DEBOUNCE clock /4
		8'h3	PORT E/F DEBOUNCE clock /8
		8'h4	PORT E/F DEBOUNCE clock /16
		8'h5	PORT E/F DEBOUNCE clock /32
		8'h6	PORT E/F DEBOUNCE clock /64
		Default	PORT E/F DEBOUNCE clock /128

1.2.19 **SWREG** Always-on SW Register

PRER1=0x4000_00B4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW_REG1																															
0x00000000																															
RW																															

31 0	SW_REG1	

CHAPTER 2. PORT CONTROL UNIT (PCU) & GPIO

2.1 OVERVIEW

PCU(Port Control Unit) controls the external I/Os as below

- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up/down register control and open drain control

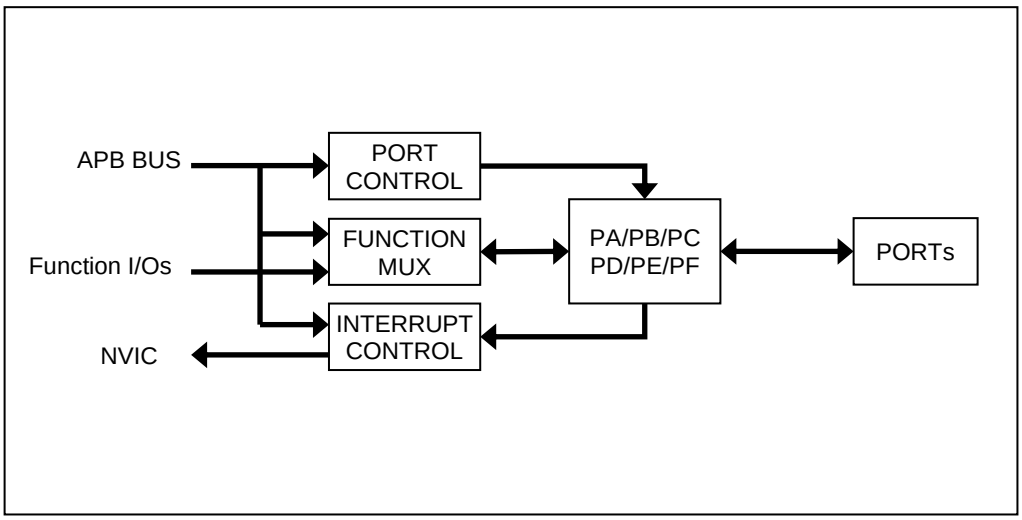


Figure 2.1. Block Diagram

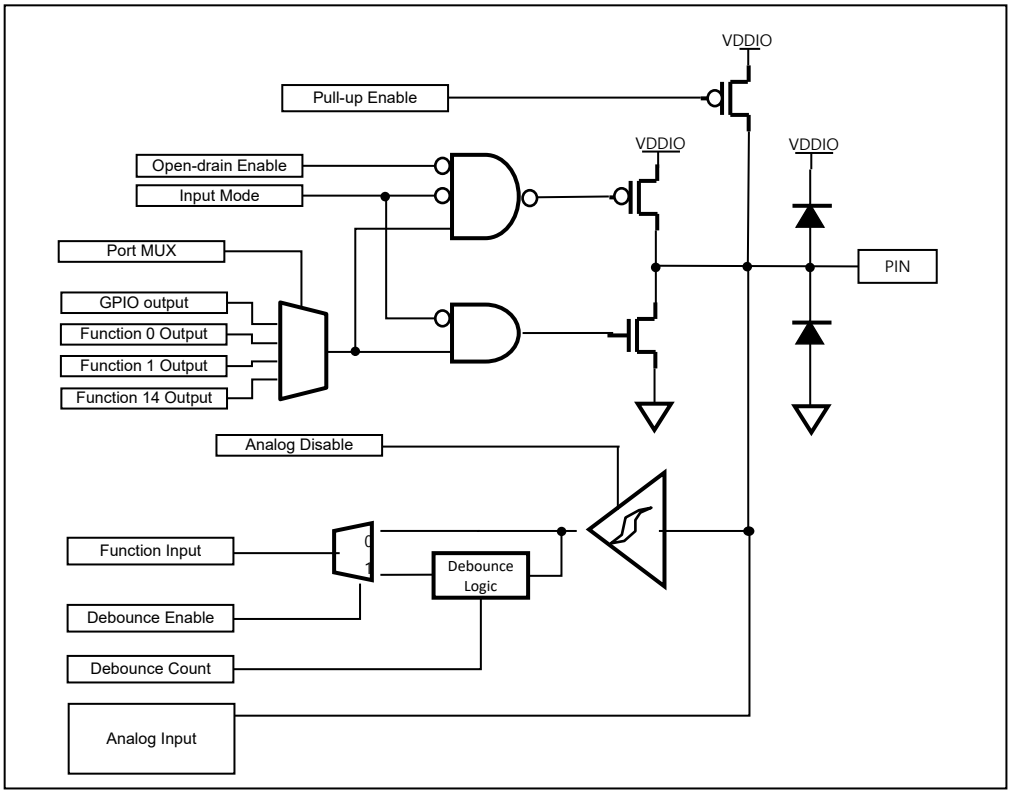


Figure 2.2. I/O Port Block Diagram

2.2 REGISTERS

The base address of PCU & GPIO block is 0x4000_1000.

Table 2.1 Base Address of Port

PORT NAME	ADDRESS RANGE	SIZE (Bytes)	DESCRIPTION
PA	0x4000 1000 – 0x4000 10FF	256	General Port A
PB	0x4000 1100 – 0x4000 11FF	256	General Port B
PC	0x4000 1200 – 0x4000 12FF	256	General Port C
PE	0x4000 0400 – 0x4000 04FF	256	General Port E
PF	0x4000 0500 – 0x4000 05FF	256	General Port F

Table 2.2 PCU & GPIO Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
PnMOD	0x0000	RW	Port *n* Mode Register	-
PnTYP	0x0004	RW	Port *n* Output Type Selection Register	0x00000000
PnAFSR0	0x0008	RW	Port *n* Alternative Function Selection Register 0	-
PnPUPD	0x0010	RW	Port *n* Pull-up/down Resistor Selection Register	0x00000000
PnINDR	0x0014	RO	Port *n* Input Data Register	-
PnOUTDR	0x0018	RW	Port *n* Output Data Register	0x00000000
PnBSR	0x001C	WO	Port *n* Output Bit Set Register	0x00000000
PnBCR	0x0020	WO	Port *n* Output Bit Clear Register	0x00000000
PnOUTDMSK	0x0024	RW	Port *n* Output Data Mask Register	0x00000000
PnDBCR	0x0028	RW	Port *n* Debounce Control Register	0x00000000
PnIER	0x002C	RW	Port *n* Interrupt Enable Register	0x00000000
PnISR	0x0030	RW	Port *n* Interrupt Status Register	0x00000000
PnICR	0x0034	RW	Port *n* Interrupt Control Register	0x00000000

Notes)
1. Where n = A, B, C, E, and F.
2. Exceptionally, the reset value of PBMOD/PBAFSR0/PBPUPD/PBDBCR register is 0x0A80/0x00221000/0x0640/0x0008, respectively.

2.2.1 Pn.MOD Port n Mode Register

Input or output control of each port pin. Each pin can be configured as input pin, output pin or Alternative Function pin. Port n Mode Register is 16-bit register. (n = A to F)

PA.MOD=0x4000_1000, PC.MOD=0x4000_1200, PF.MOD=0x4000_0500

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
0x0000		00	00	00	00	00	00	00	00
-		RW	RW	RW	RW	RW	RW	RW	RW

PB.MOD=0x4000_1100

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
0x0000		00	00	00	00	00	00	10	10
-		RW	RW	RW	RW	RW	RW	RW	RW

PE.MOD=0x4000_0400

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
0x0000		00	00	10	00	00	00	00	10
-		RW	RW	RW	RW	RW	RW	RW	RW

2x+	MODEx	Port n Mode Selection bits, x: 0 to 15	
1		00	Input mode
2x		01	Output mode
		10	Alternative function mode
		11	Reserved

2.2.2 Pn.TYP Port n Output Type Selection Register

Push-pull output or Open-drain output control of each port pin.

Port n Output Type Selection Register is 8-bit register. (n = A to F)

PA.TYP=0x4000_1004, PB.TYP=0x4000_1104, PC.TYP=0x4000_1204
PE.TYP=0x4000_0404, PF.TYP=0x4000_0504

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								TYP7	TYP6	TYP5	TYP4	TYP3	TYP2	TYP1	TYP0
0x0000																								0	0	0	0	0	0	0	0
–																								RW	RW	RW	RW	RW	RW	RW	RW

x	TYPx	Port n Output Type Selection bit, x: 0 to 7
		0 Push-pull output
		1 Open-drain output

2.2.3 PA.AFSR Port A Alternative Function Selection Register

A port Alternative Function selection register. This register must be set properly before using the port. Otherwise, the port cannot guarantee its functionality.

Port n Alternative Function Selection Register 0 is 32-bit register.

PA.AFSR=0x4000_1008

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	AFSR6	AFSR5	AFSR4	AFSR3	AFSR2	AFSR1	AFSR0
0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port A Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		0101	Alternative Function 5 (AF5)
		0110	Alternative Function 6 (AF6)
		0111	Alternative Function 7 (AF7)
		1000	Alternative Function 8 (AF8)
		1001	Alternative Function 9 (AF9)
		1010	Alternative Function 10 (AF10)
		1011	Alternative Function 11 (AF11)
		1100	Alternative Function 12 (AF12)
		1101	Alternative Function 13 (AF13)
		1110	Alternative Function 14 (AF14)
		1111	Key SCAN Function Mode

2.2.4 PB.AFSR Port B Alternative Function Selection Register

B port Alternative Function selection register. This register must be set properly before using the port. Otherwise, the port can't guarantee its functionality.

Port n Alternative Function Selection Register 0 is 32-bit register.

PB.AFSR =0x4000_1108

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	AFSR6	AFSR5	AFSR4	AFSR3	AFSR2	AFSR1	AFSR0
0000	0000	0000	0000	0000	0000	1011	1011
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port A Alternative Function Selection bits, x: 0 to 7
	0000	Alternative Function 0 (BF0)
	0001	Alternative Function 1 (BF1)
	0010	Alternative Function 2 (BF2)
	0011	Alternative Function 3 (BF3)
	0100	Alternative Function 4 (BF4)
	0101	Alternative Function 5 (BF5)
	0110	Alternative Function 6 (BF6)
	0111	Alternative Function 7 (BF7)
	1000	Alternative Function 8 (BF8)
	1001	Alternative Function 9 (BF9)
	1010	Alternative Function 10 (BF10)
	1011	Alternative Function 11 (BF11)
	1100	Alternative Function 12 (BF12)
	1101	Alternative Function 13 (BF13)
	1110	Alternative Function 14 (BF14)
	1111	Key SCAN Function Mode

2.2.5 PC.AFSR Port C Alternative Function Selection Register

C port Alternative Function selection register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

Port n Alternative Function Selection Register 0 is 32-bit register.

PC.AFSR =0x4000_1208

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Resrved	Resrved	Resrved	AFSR4	AFSR3	AFSR2	Resrved	Resrved
0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port A Alternative Function Selection bits, x: 0 to 7
	0000	Alternative Function 0 (CF0)
	0001	Alternative Function 1 (CF1)
	0010	Alternative Function 2 (CF2)
	0011	Alternative Function 3 (CF3)
	0100	Alternative Function 4 (CF4)
	0101	Alternative Function 5 (CF5)
	0110	Reserved
	0111	Reserved
	1000	Reserved
	1001	Reserved
	1010	Reserved
	1011	Reserved
	1100	Reserved
	1101	Reserved
	1110	Reserved
	1111	Key SCAN Function Mode

2.2.6 PE.AFSR Port E Alternative Function Selection Register

E port Alternative Function selection register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

Port n Alternative Function Selection Register 0 is 32-bit register.

PE.AFSR =0x4000_0408

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

Reserved	AFSR6	AFSR5	AFSR4	AFSR3	AFSR2	AFSR1	Reserved
0000	1100	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port A Alternative Function Selection bits, x: 0 to 7
	0000	Alternative Function 0 (EF0)
	0001	Alternative Function 1 (EF1)
	0010	Alternative Function 2 (EF2)
	0011	Alternative Function 3 (EF3)
	0100	Alternative Function 4 (EF4)
	0101	Alternative Function 5 (EF5)
	0110	Alternative Function 6 (EF6)
	0111	Alternative Function 7 (EF7)
	1000	Alternative Function 8 (EF8)
	1001	Alternative Function 9 (EF9)
	1010	Alternative Function 10 (EF10)
	1011	Alternative Function 11 (EF11)
	1100	Alternative Function 12 (EF12)
	1101	Reserved
	1110	Reserved
	1111	Key SCAN Function Mode

Notes)
1. AFSR1 and AFSR2 use only Key SCAN Function Mode

2.2.7 PF.AFSR Port F Alternative Function Selection Register

E port Alternative Function selection register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

Port n Alternative Function Selection Register 0 is 32-bit register.

PB.AFSR =0x4000_0408

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Reserved	Reserved	Reserved	Reserved	AFSR3	AFSR2	AFSR1	AFSR0

0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port A Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (EF0)
		0001	Alternative Function 1 (EF1)
		0010	Alternative Function 2 (EF2)
		0011	Alternative Function 3 (EF3)
		0100	Alternative Function 4 (EF4)
		0101	Alternative Function 5 (EF5)
		0110	Alternative Function 6 (EF6)
		0111	Alternative Function 7 (EF7)
		1000	Alternative Function 8 (EF8)
		1001	Alternative Function 9 (EF9)
		1010	Alternative Function 10 (EF10)
		1011	Alternative Function 11 (EF11)
		1100	Alternative Function 12 (EF12)
		1101	Reserved
		1110	Reserved
		1111	Key SCAN Function Mode

2.2.8 Pn.PUPD Port n Pull-up/down Resistor Selection Register

Every pin in the port has on-chip pull-up/down resistor which can be configured by PnPUPD registers.

Port n Pull-up/down Resistor Selection Register is 16-bit register. (n = A to F)

PA.PUPD=0x4000_1010, PB.PUPD=0x4000_1110, PC.PUPD=0x4000_1210

PE.PUPD=0x4000_0410, PF.PUPD=0x4000_0510

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		PUPD7	PUPD6	PUPD5	PUPD4	PUPD3	PUPD2	PUPD1	PUPD0
0x0000		00	00	00	00	00	00	00	00
-		RW	RW	RW	RW	RW	RW	RW	RW

2x+ 1	PUPDx	Port n Pull-up/down Resistor Selection bits, x: 0 to 15	
2x		00	Disable pull-up/down resistor
		01	Enable pull-up resistor
		10	Enable pull-down resistor Pull-down resistor enable is valid for Port A/B/C/D. Port E and F don't have pull-down resistor, but do have pull-up resistor.
		11	Enable high driving strength mode

Notes)
1. The pull-up resistor of PF0 – PF3 is automatically disabled regardless of the corresponding PUPDx value if the pins are configured as the alternative function for xtal (XIN, XOUT, SXIN, and SXOUT).

2.2.9 Pn.INDR Port n Input Data Register

Each pin level status can be read in the PnINDR register. Even if the pin configure for alternative mode, the pin level can be detected in the PnINDR register.

Port n Input Data Register is 8-bit register. (n = A to F)

PA.INDR=0x4000_1014, PB.INDR=0x4000_1114, PC.INDR=0x4000_1214
PE.INDR=0x4000_0414, PF.INDR=0x4000_0514

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								INDR7	INDR6	INDR5	INDR4	INDR3	INDR2	INDR1	INDR0
0x000000																								0	0	0	0	0	0	0	0
																								RO	RO	RO	RO	RO	RO	RO	RO

x	INDRx	Port n Input Data bit, x: 0 to 7

2.2.10 Pn.OUTDR Port n Output Data Register

When the pin is set as output and GPIO mode, the pin output level is defined by PnOUTDR registers.
Port n Output Data Register is 8-bit register. (n = A to F)

PA.OUTDR=0x4000_1018, PB.OUTDR=0x4000_1118, PC.OUTDR=0x4000_1218
PE.OUTDR=0x4000_0418, PF.OUTDR=0x4000_0518

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								OUTDR7	OUTDR6	OUTDR5	OUTDR4	OUTDR3	OUTDR2	OUTDR1	OUTDR0
0x000000																								0	0	0	0	0	0	0	0
-																								RW	RW	RW	RW	RW	RW	RW	RW

x	OUTDRx	Port n Output Data bit, x: 0 to 7 The OUTDR bits can be individually set/cleared by writing to the PnBSR/PnBCR register.

2.2.11 Pn.BSR Port n Output Bit Set Register

PnBSR is a register for control each bit of PnOUTDR register. Writing a '1' into the specific bit will set a corresponding bit of PnOUTDR to '1'. Writing '0' in this register has no effect.
Port n Output Bit Set Register is 8-bit register. (n = A to F)

PA.BSR=0x4000_101C, PB.BSR=0x4000_111C, PC.BSR=0x4000_121C
PE.BSR=0x4000_041C, PF.BSR=0x4000_051C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
0x000000																								0	0	0	0	0	0	0	0
-																								WO	WO	WO	WO	WO	WO	WO	WO

x	BSRx	Port n Output Set bit, x: 0 to 7. These bits are always read to 0x00.	
		0	No effect
		1	Set the corresponding OUTDRx bit (Automatically cleared to 0)

2.2.12 Pn.BCR Port n Output Bit Clear Register

PnBCR is a register for control each bit of PnOUTDR register. Writing a '1' into the specific bit will set a corresponding bit of PnOUTDR to '0'. Writing '0' in this register has no effect.

Port n Output Bit Clear Register is 8-bit register. (n = A to F)

PA.BCR=0x4000_1020, PB.BCR=0x4000_1120, PC.BCR=0x4000_1220
PE.BCR=0x4000_0420, PF.BCR=0x4000_0520

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
0x000000																								0	0	0	0	0	0	0	0
-																								WO	WO	WO	WO	WO	WO	WO	WO

x	BCRx	Port n Output Clear bit, x: 0 to 7. These bits are always read to 0x00.	
		0	No effect
		1	Clear the corresponding OUTDRx bit (Automatically cleared to 0)

2.2.13 Pn.OUTDMSK Port n Output Data Mask Register

PnOUTDMSK is a register for protection each bit of PnOUTDR register. Writing a '1' into the specific bit will protect a corresponding bit of PnOUTDR. Writing '0' in this register is unmasked.

Port n Output Data Mask Register is 8-bit register. (n = A to F)

PA.OUTDMSK=0x4000_1024, PB.OUTDMSK=0x4000_1124, PC.OUTDMSK=0x4000_1224
PE.OUTDMSK=0x4000_0424, PF.OUTDMSK=0x4000_0524

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								OUTDMSK7	OUTDMSK6	OUTDMSK5	OUTDMSK4	OUTDMSK3	OUTDMSK2	OUTDMSK1	OUTDMSK0
0x000000																								0	0	0	0	0	0	0	0
-																								RW	RW	RW	RW	RW	RW	RW	RW

x	OUTDMSK x	Port n Output Data Mask bit, x: 0 to 7.	
		0	Unmask. The corresponding OUTDRx bit can be changed.
		1	Mask. The corresponding OUTDRx bit is protected.

2.2.14 Pn.DBCR Port n Debounce Control Register

Port n Debounce Control Register is 8-bit register. (n = A to E)

PA.DBCR=0x4000_1028, PB.DBCR=0x4000_1128, PC.DBCR=0x4000_1228
PE.DBCR=0x4000_0428, PF.DBCR=0x4000_0528

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			DBEN7	DBEN6	DBEN5	DBEN4	DBEN3	DBEN2	DBEN1	DBEN0
0x000000			0	0	0	0	0	0	0	0
-			RW	RW	RW	RW	RW	RW	RW	RW

x	DBENx	Port n Debounce Enable bit, x: 0 to 7.	
		0	Disable debounce filter
		1	Enable debounce filter

Notes)
1 . Level is not detected on an enabled pin three or more times in a row at the sampling clock, the signal is eliminated as noise.
2. The port debounce control should be disabled before entering the deep sleep mode.

2.2.15 Pn.IER PORT n Interrupt Enable Register

The entire pin can be an external interrupt source. Both of the edge trigger interrupt and the level trigger interrupt are supported. The interrupt mode can be configured by setting PnIER registers

PA.IER=0x4000_102C, PB.IER=0x4000_112C, PC.IER =0x4000_122C
PE.IER =0x4000_042C, PF.IER =0x4000_052C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		PIE7	PIE6	PIE5	PIE4	PIE3	PIE2	PIE1	PIE0
0x0000		00	00	00	00	00	00	00	00
-		RW	RW	RW	RW	RW	RW	RW	RW

PIEn	Pin interrupt enable	
	00	Interrupt disabled
	01	Enable interrupt as level trigger mode
	10	Reserved
	11	Enable interrupt as edge trigger mode

2.2.16 Pn.ISR PORT n Interrupt Status Register

When an interrupt is delivered to the CPU, the interrupt status can be detected by reading PnISR register. PnISR register will report a source pin of interrupt and a type of interrupt.

PA.ISR=0x4000_1030, PB. ISR =0x4000_1130, PC. ISR =0x4000_1230
PE. ISR =0x4000_0430, PF. ISR =0x4000_0530

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		PIS7	PIS6	PIS5	PIS4	PIS3	PIS2	PIS1	PIS0
0x00		00	00	00	00	00	00	00	00
-		RW	RW	RW	RW	RW	RW	RW	RW

PISn	Pin interrupt status
00	No interrupt event
01	Low level interrupt or Falling edge interrupt event is present
10	High level interrupt or rising edge interrupt event is present
11	Both of rising and falling edge interrupt event is present in edge trigger interrupt mode. Not available in level trigger interrupt mode

2.2.17 Pn.ICR PORT n Interrupt Control Register

Interrupt mode control register.

PA.ICR=0x4000_1034, PB. ICR =0x4000_1134, PC. ICR =0x4000_1234
PE. ICR =0x4000_0434, PF. ICR =0x4000_0534

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved		PIC7	PIC6	PIC5	PIC4	PIC3	PIC2	PIC1	PIC0
0x0000		00	00	00	00	00	00	00	00
-		RW	RW	RW	RW	RW	RW	RW	RW

PICn	Pin interrupt mode
00	Prohibit external interrupt
01	Low level interrupt or Falling edge interrupt mode
10	High level interrupt or rising edge interrupt mode
11	Both of rising and falling edge interrupt mode. Not support for level trigger mode

2.3 FUNCTION PORT ASSIGNMENT

PORT A Alternative Function

	PA[0]	PA[1]	PA[2]	PA[3]	PA[4]	PA[5]	PA[6]	PA[7]
AF0	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD
AF1	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS
AF2	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD
AF3	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA
AF4	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA
AF5	SPI0_CLK	SPI0_SS	SPI0_MOSI	SPI0_MISO	SPI0_CLK	SPI0_SS	SPI0_MOSI	SPI0_MISO
AF6	SPI1_CLK	SPI1_SS	SPI1_MOSI	SPI1_MISO	SPI1_CLK	SPI1_SS	SPI1_MOSI	SPI1_MISO
AF7	TIMER_PWM0	TIMER_PWM1	TIMER_PWM2	TIMER_PWM3	TIMER_PWM0	TIMER_PWM1	TIMER_PWM2	TIMER_PWM3
AF8	TIMER_CAP0	TIMER_CAP1	TIMER_CAP2	TIMER_CAP3	TIMER_CAP0	TIMER_CAP1	TIMER_CAP2	TIMER_CAP3
AF9	PWMP	PWMN	DDAC_PWMH	DDAC_PWML	PWMP	PWMN	DDAC_PWMH	DDAC_PWML
AF10	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B
AF11	SWTCK	SWD	SWTCK	SWD	SWTCK	SWD	SWTCK	SWD
AF12	DS_IND	DS_IND	DS_IND	DS_IND	WAKEUP_REQ	WAKEUP_REQ	WAKEUP_REQ	WAKEUP_REQ
AF13	DEBUG0	DEBUG1	DEBUG2	DEBUG3	DEBUG4	DEBUG5	DEBUG6	DEBUG7
AF14	UART1_CTS	UART1_RTS	UART1_CTS	UART1_RTS	UART1_CTS	UART1_RTS	UART1_CTS	UART1_RTS

PORT B Alternative Function

	PB[0]	PB[1]	PB[2]	PB[3]	PB[4]	PB[5]	PB[6]	PB[7]
AF0	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD
AF1	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS
AF2	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD
AF3	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA
AF4	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA
AF5	SPI0_CLK	SPI0_SS	SPI0_MOSI	SPI0_MISO	SPI0_CLK	SPI0_SS	SPI0_MOSI	SPI0_MISO
AF6	SPI1_CLK	SPI1_SS	SPI1_MOSI	SPI1_MISO	SPI1_CLK	SPI1_SS	SPI1_MOSI	SPI1_MISO
AF7	TIMER_PWM0	TIMER_PWM1	TIMER_PWM2	TIMER_PWM3	TIMER_PWM0	TIMER_PWM1	TIMER_PWM2	TIMER_PWM3
AF8	TIMER_CAP0	TIMER_CAP1	TIMER_CAP2	TIMER_CAP3	TIMER_CAP0	TIMER_CAP1	TIMER_CAP2	TIMER_CAP3
AF9	PWMP	PWMN	DDAC_PWMH	DDAC_PWML	PWMP	PWMN	DDAC_PWMH	DDAC_PWML
AF10	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B
AF11	SWTCK	SWD	SWTCK	SWD	SWTCK	SWD	SWTCK	SWD
AF12	CLK_OUT	CLK_OUT	CLK_OUT	CLK_OUT	CLK_OUT	CLK_OUT	CLK_OUT	CLK_OUT
AF13	DEBUG7	DEBUG6	DEBUG5	DEBUG4	DEBUG3	DEBUG2	DEBUG1	DEBUG0

AF14	UART1_CTS	UART1_RTS	UART1_CTS	UART1_RTS	UART1_CTS	UART1_RTS	UART1_CTS	UART1_RTS

PORT C Alternative Function

	PC[0]	PC[1]	PC[2]	PC[3]	PC[4]	PC[5]	PC[6]	PC[7]
AF0			IR_CGIN	IR_CGIN	IR_CGIN			
AF1			IR_COMP	IR_COMP	IR_COMP			
AF2			DMI_CLK	DMI_CLK	DMI_CLK			
AF3			DMI_LRCLK	DMI_LRCLK	DMI_LRCLK			
AF4			DMI_DATA	DMI_DATA	DMI_DATA			
AF5			ACU_RSTB	ACU_RSTB	ACU_RSTB			
AF6								
AF7								
AF8								
AF9								
AF10								
AF11								
AF12								
AF13								
AF14								

PORT E Alternative Function

	PE[0]	PE[1]	PE[2]	PE[3]	PE[4]	PE[5]	PE[6]	PE[7]
AF0				UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD	
AF1				UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS	
AF2				UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD	
AF3				I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA	
AF4				I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	
AF5				SPI0_CLK	SPI0_SS	SPI0_MOSI	SPI0_MISO	
AF6				SPI1_CLK	SPI1_SS	SPI1_MOSI	SPI1_MISO	
AF7				TIMER_PWM0	TIMER_PWM1	TIMER_PWM2	TIMER_PWM3	
AF8				TIMER_CAP0	TIMER_CAP1	TIMER_CAP2	TIMER_CAP3	
AF9				PWMP	PWMN	DDAC_PWMH	DDAC_PWML	
AF10				QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B	
AF11				IR_CGIN	IR_COMP	IR_CGIN	IR_COMP	
AF12				DS_IND	DS_IND	DS_IND	DS_IND	
AF13								
AF14								

PORT F Alternative Function

	PF[0]	PF[1]	PF[2]	PF[3]	PF[4]	PF[5]	PF[6]	PF[7]
AF0	UART0_RXD	UART0_TXD	UART0_RXD	UART0_TXD				
AF1	UART0_CTS	UART0_RTS	UART0_CTS	UART0_RTS				
AF2	UART1_RXD	UART1_TXD	UART1_RXD	UART1_TXD				
AF3	I2C0_SCL	I2C0_SDA	I2C0_SCL	I2C0_SDA				
AF4	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA				
AF5	SPI0_CLK	SPI0_SS	SPI0_MOSI	SPI0_MISO				
AF6	SPI1_CLK	SPI1_SS	SPI1_MOSI	SPI1_MISO				
AF7	TIMER_PWM0	TIMER_PWM1	TIMER_PWM2	TIMER_PWM3				
AF8	TIMER_CAP0	TIMER_CAP1	TIMER_CAP2	TIMER_CAP3				
AF9	PWMP	PWMN	DDAC_PWMH	DDAC_PWML				
AF10	QDEC0_A	QDEC0_B	QDEC0_A	QDEC0_B				
AF11	IR_CGIN	IR_COMP	IR_CGIN	IR_COMP				
AF12	WAKEUP_REQ	WAKEUP_REQ	WAKEUP_REQ	WAKEUP_REQ				
AF13								
AF14								

CHAPTER 3. CORE SYSTEM REGISTER

3.1 OVERVIEW

CSR Block (=Core System Register) reside in power-off domain. It manages clock/reset in power-off domain and support several features like address re-map, rom patch and debug output muxing.

3.2 REGISTERS

The base Address of CORE System Register is 0x4000_3000 and register map is described in Table 3.1

Table 3.1 SCU Register Map

Name	Offset	R/W	Description	Reset
PCER1	0x0000	R/W	Peripheral clock enable register 1	0x0007800F
PRER1	0x0008	R/W	Peripheral reset register 1	0x0007800F
PER1	0x0010	R/W	Peripheral enable register 1	0x0007800F
MCCR1	0x0020	R/W	Miscellaneous Clock Control register 1	0x00000100
MCCR2	0x0024	R/W	Miscellaneous Clock Control register 2	0x00000100
MCCR3	0x0028	R/W	Miscellaneous Clock Control register 3	0x00000100
MCCR4	0x002C	R/W	Miscellaneous Clock Control register 4	0x00000100
MCCR5	0x0030	R/W	Miscellaneous Clock Control register 5	0x00000100
BLECLK	0x0040	R/W	BLE Clock Setting register	0x00000010
CLKDBLCON	0x0050	R/W	Clock Doubler Control register	0x00000000
COR	0x0060	R/W	Clock Output Control register	0x0000000F
REMAP	0x0070	R/W	REMAP Register	0x00000002
ARMSYSTICK	0x0080	R/W	ARM System TICK Control register	0x00000000
ROMPAT_VALID	0x0090	R/W	ROM Patch Valid Register	0x00000000
ROMPAT_ADDR0	0x00A0	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA0	0x00A4	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR1	0x00A8	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA1	0x00AC	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR2	0x00B0	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA2	0x00B4	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR3	0x00B8	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA3	0x00BC	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR4	0x00C0	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA4	0x00C4	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR5	0x00C8	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA5	0x00CC	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR6	0x00D0	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA6	0x00D4	R/W	ROM Patch Data Register	0x00000000
ROMPAT_ADDR7	0x00D8	R/W	ROM Patch Address Register	0x00000000
ROMPAT_DATA7	0x00DC	R/W	ROM Patch Data Register	0x00000000

3.2.1 PCER1 Peripheral Clock Enable Register 1

To use peripheral unit, its clock should be activated by writing '1'to the correspond bit in the PCER0/1 register. Before enabling its clock, the peripheral won't operate properly.

To stop the clock of the peripheral unit, write '0'to the correspond bit in the PCER0/1 register, and then the clock of the peripheral is stopped.

PCER1=0x4000_3000

31	30	29	28	27	26	25	24	23	22	21	20 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRNG	ADC	I2C1	I2C0	SPI1	SPI0	Reserved	BLE	UART1	UART0	IR	Reserved	GPIOD	GPIOC	GPIOB	GPIOA	KEY SCAN	DMI	QEI	TIMER7	DDAC	PWM	TIMER3	TIMER2	TIMER1	TIMER0	WDT	DMA	PMC	QSPM	OTP
0	0	0	0	0	0	0	0	0	0	0	0x0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

31	TRNG	Block Clock enable
30	ADC	Block Clock enable
29	I2C1	Block Clock enable
28	I2C0	Block Clock enable
27	SPI1	Block Clock enable
26	SPI0	Block Clock enable
24	BLE	Block Clock enable
23	UART1	Block Clock enable
22	UART0	Block Clock enable
21	IR	Block Clock enable
18	GPIOD	Block Clock enable
17	GPIOC	Block Clock enable
16	GPIOB	Block Clock enable
15	GPIOA	Block Clock enable
14	KEY SCAN	Block Clock enable
13	DMI	Block Clock enable
12	QEI	Block Clock enable
11	TIMER7	Block Clock enable
10	DDAC	Block Clock enable
9	PWM	Block Clock enable
8	TIMER3	Block Clock enable
7	TIMER2	Block Clock enable
6	TIMER1	Block Clock enable
5	TIMER0	Block Clock enable
4	WDT	Block Clock enable
3	DMA	Block Clock enable
2	PMC	Block Clock enable
1	QSPM	Block Clock enable
0	OTP	Block Clock enable

3.2.2 PRER1 Peripheral Reset Enable Register 1

The reset of each peripheral by event reset, can be masked by user setting. PRER register will control the enable of the event reset. If the corresponding bit is '1', the peripheral corresponded with this bit, accepts the reset event. Otherwise, the peripheral is protected from reset event and maintain current operation.

PRER1=0x4000_3008

31	30	29	28	27	26	25	24	23	22	21	20 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRNG	ADC	I2C1	I2C0	SPI1	SPI0	Reserved	BLE	UART1	UART0	IR	Reserved	GPIOD	GPIOC	GPIOB	GPIOA	KEY SCAN	DMI	QEI	TIMER7	DDAC	PWM	TIMER3	TIMER2	TIMER1	TIMER0	WDT	DMA	PMC	QSPM	OTP
0	0	0	0	0	0	0	0	0	0	0	0x0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

31	TRNG	Block Reset enable
30	ADC	Block Reset enable
29	I2C1	Block Reset enable
28	I2C0	Block Reset enable
27	SPI1	Block Reset enable
26	SPI0	Block Reset enable
24	BLE	Block Reset enable
23	UART1	Block Reset enable
22	UART0	Block Reset enable
21	IR	Block Reset enable
18	GPIOD	Block Reset enable
17	GPIOC	Block Reset enable
16	GPIOB	Block Reset enable
15	GPIOA	Block Reset enable
14	KEY SCAN	Block Reset enable
13	DMI	Block Reset enable
12	QEI	Block Reset enable
11	TIMER7	Block Reset enable
10	DDAC	Block Reset enable
9	PWM	Block Reset enable
8	TIMER3	Block Reset enable
7	TIMER2	Block Reset enable
6	TIMER1	Block Reset enable
5	TIMER0	Block Reset enable
4	WDT	Block Reset enable
3	DMA	Block Reset enable
2	PMC	Block Reset enable
1	QSPM	Block Reset enable
0	OTP	Block Reset enable

3.2.3 PER1 Peripheral Enable Register 1

To use peripheral unit, it should be activated by writing “1”to the correspond bit in the PER0/1 register. Before the activation, the peripheral will stay in reset state.

All the peripherals enabled by default. To disable the peripheral unit, write “0” to the correspond bit in the PER0/1 register, and then the peripheral enter the reset state.

PER1=0x4000_3010

31	30	29	28	27	26	25	24	23	22	21	20 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRNG	ADC	I2C1	I2C0	SPI1	SPI0	Reserved	BLE	UART1	UART0	IR	Reserved	GPIOD	GPIOC	GPIOB	GPIOA	KEY SCAN	DMI	QEI	TIMER7	DDAC	PWM	TIMER3	TIMER2	TIMER1	TIMER0	WDT	DMA	PMC	QSPM	OTP
0	0	0	0	0	0	0	0	0	0	0	0x0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

31	TRNG	Block enable
30	ADC	Block enable
29	I2C1	Block enable
28	I2C0	Block enable
27	SPI1	Block enable
26	SPI0	Block enable
24	BLE	Block enable
23	UART1	Block enable
22	UART0	Block enable
21	IR	Block enable
18	GPIOD	Block enable
17	GPIOC	Block enable
16	GPIOB	Block enable
15	GPIOA	Block enable
14	KEY SCAN	Block enable
13	DMI	Block enable
12	QEI	Block enable
11	TIMER7	Block enable
10	DDAC	Block enable
9	PWM	Block enable
8	TIMER3	Block enable
7	TIMER2	Block enable
6	TIMER1	Block enable
5	TIMER0	Block enable
4	WDT	Block enable
3	DMA	Block enable
2	PMC	Block enable
1	QSPM	Block enable
0	OTP	Block enable

3.2.4 MCCR1 Miscellaneous Clock Control Register 1

MCCR1=0x4000_3020

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved			TIMERESEL	TIMEREDIV
0x000000			0x1	0x00
-			RW	RW

9 8	TIMERESEL	TIMER	Clock source select bit
		00	MCLK (AHB clock)
		01	PCLK (APB clock)
		10	SUB Clock (32.768kHz)
		11	Reserved
7 0	TIMEREDIV	TIMER	Clock N divider
		8'h0	Clock disabled
		8'h1	TIMER clock /2
		8'h2	TIMER clock /4
		8'h3	TIMER clock /8
		8'h4	TIMER clock /16
		8'h5	TIMER clock /32
		8'h6	TIMER clock /64
		Default	TIMER clock /128

3.2.5 MCCR2 Miscellaneous Clock Control Register 2

MCCR2=0x4000_3024

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved			WDTESEL	WDTEDIV
0x000000			0x1	0x00
-			RW	RW

9 8	WDTESEL	WDT	Clock source select bit
		00	MCLK (AHB clock)
		01	PCLK (APB clock)
		10	SUB Clock (32.768kHz)
		11	Reserved
7 0	WDTEDIV	WDT	Clock N divider
		8'h0	Clock disabled
		8'h1	WDT clock /2
		8'h2	WDT clock /4
		8'h3	WDT clock /8
		8'h4	WDT clock /16
		8'h5	WDT clock /32
		8'h6	WDT clock /64
		Default	WDT clock /128

3.2.6 MCCR3 Miscellaneous Clock Control Register 3

MCCR3=0x4000_3028

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved			SYSTICKESEL	SYSTICKEDIV
0x000000			0x1	0x00
-			RW	RW

9 8	SYSTICKESEL	SYSTICK Clock source select bit	
		00	MCLK (AHB clock)
		01	PCLK (APB clock)
		10	SUB Clock (32.768kHz)
		11	Reserved
7 0	SYSTICKEDIV	SYSTICK Clock N divider	
		8'h0	Clock disabled
		8'h1	SYSTICK clock /2
		8'h2	SYSTICK clock /4
		8'h3	SYSTICK clock /8
		8'h4	SYSTICK clock /16
		8'h5	SYSTICK clock /32
		8'h6	SYSTICK clock /64
		Default	SYSTICK clock /128

3.2.7 MCCR4 Miscellaneous Clock Control Register 4

MCCR4=0x4000_302C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved			PORTACSEL	PORTACDIV
0x000000			0x1	0x00
-			RW	RW

9 8	PORTACSEL	POR A/C DEBOUNCE	Clock source select bit
		00	MCLK (AHB clock)
		01	PCLK (APB clock)
		10	SUB Clock (32.768kHz)
		11	Reserved
7 0	PORTACDIV	POR A/C DEBOUNCE	Clock N divider
		8'h0	Clock disabled
		8'h1	POR A/C DEBOUNCE clock /2
		8'h2	POR A/C DEBOUNCE clock /4
		8'h3	POR A/C DEBOUNCE clock /8
		8'h4	POR A/C DEBOUNCE clock /16
		8'h5	POR A/C DEBOUNCE clock /32
		8'h6	POR A/C DEBOUNCE clock /64
		Default	POR A/C DEBOUNCE clock /128

3.2.8 MCCR5 Miscellaneous Clock Control Register 5

MCCR5=0x4000_3030

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved			PORTBDSEL	PORTBDDIV
0x000000			0x1	0x00
-			RW	RW

9 8	PORTBDSEL	PORT B/D DEBOUNCE Clock source select bit
		00 MCLK (AHB clock)
		01 PCLK (APB clock)
		10 SUB Clock (32.768kHz)
		11 Reserved
7 0	PORTBDDIV	POR B/D DEBOUNCE Clock N divider
		8'h0 Clock disabled
		8'h1 POR B/D DEBOUNCE clock /2
		8'h2 POR B/D DEBOUNCE clock /4
		8'h3 POR B/D DEBOUNCE clock /8
		8'h4 POR B/D DEBOUNCE clock /16
		8'h5 POR B/D DEBOUNCE clock /32
		8'h6 POR B/D DEBOUNCE clock /64
		Default POR B/D DEBOUNCE clock /128

3.2.9 BLECLK BLE Clock Setting Register

BLECLK=0x4000_3040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
0x0000000																										0x10					
-																										RW					

5 0	BLECLK	BLE Clock Setting

3.2.10 CLKDBLCON Clock Doubler Control Register

PRER1=0x4000_3050

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											LOCK	FR_EN	DC_EN	PD_EN	EN
0x0000000																											0	0	0	0	0
-																											RO	RW	RW	RW	RW

4	LOCK	Clock Doubler Lock Status
		0
		1
3	FR_EN	Reserved. Should be set to 0
2	DC_EN	Reserved. Should be set to 0
1	PD_EN	Reserved. Should be set to 1
0	EN	Clock Doubler enable

3.2.11 COR Clock Output Register

The ADKREF can drive the clock from internal MCLK clock with dedicated post divider. Clock Output Register is 8-bit register.

COR=0x4000_3060

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											CLKOEN	CLKODIV		
0x0000000																											0	0xF		
-																											RW	RW		

4	CLKOEN	Clock output enable 0 CLKO is disabled and stay “L” output 1 CLKO Is enabled
3 0	CLKODIV	Clock output divider value CLKO = MCLK/(CLKODIV+1)/2 Note) When CLKODIV = 0, CLKO will be disabled

3.2.12 REMAP REMAP Control Register

EMODR=0x4000_0070

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												POC_SW	REMAP		
0x0000000																												0	0x2		
-																												RW			

3	POC_SW	POC Control To enable retention I/O, before entering SYSTEM SLEEP, it must be set this bit by ‘1’.
2 0	REMAP	REMAP “0000” : Boot ROM “0001” : OTP “001X” : QSPI Master “01XX” : SRAM Others : Reserved

3.2.13 ARMSYSTICK ARM SYSTICK Control Register

ARMSYSTICK=0x4000_3080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ARM_SYSTIK																							
0x00								0x0000000																							
-								RW																							

25 0	ARM_SYSTIK	Connected to STCALIB pins at Cortex M0+

3.2.14 ROMPAT_VALID ROM Patch Valid Register

ROMPAT_VALID=0x4000_3090

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								VALID							
0x000000																								0x00							
-																								RW							

7 0	VALID	Indicates which patch entry is valid. For example, when bit 0 is high it indicates that entry 0 is valid, i.e. the values of ROMPAT_ADDR0 / ROMPAT_DATA0, are effective.

3.2.15 ROMPAT_ADDR0~7 ROM Patch Address Register

PROMPAT_ADDR0=0x4000_30A8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																ADDR														Reserved	
0x0000																0x00000														0x0	
-																RW														-	

17 2	ADDR	This is the value which will be compared to the address on the AHB. If a match occurs, the data bus willl be filled with the value in the respective ROMPAT_DATAx Register. Bits [1:0] and Bits[31:18] are read-only and always read as "0".

3.2.16 ROMPAT_DATA0~7 ROM Patch Data Register

ROMPAT_DATA0=0x4000_30A4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
0x00000000																															
RW																															

31 0	DATA	This is the value which will be injected into the data bus if there is a match on the comparison of the address with the respective ROMPAT_ADDRx Registers

CHAPTER 4. FREE RUN TIMER (FRT)

4.1 OVERVIEW

The FRT block is a 32-bit Free Run Timer. It can be used in Power-down Mode

- 32-bit up-counter with SOSC, MOSC, LSI
- Matched Interrupt

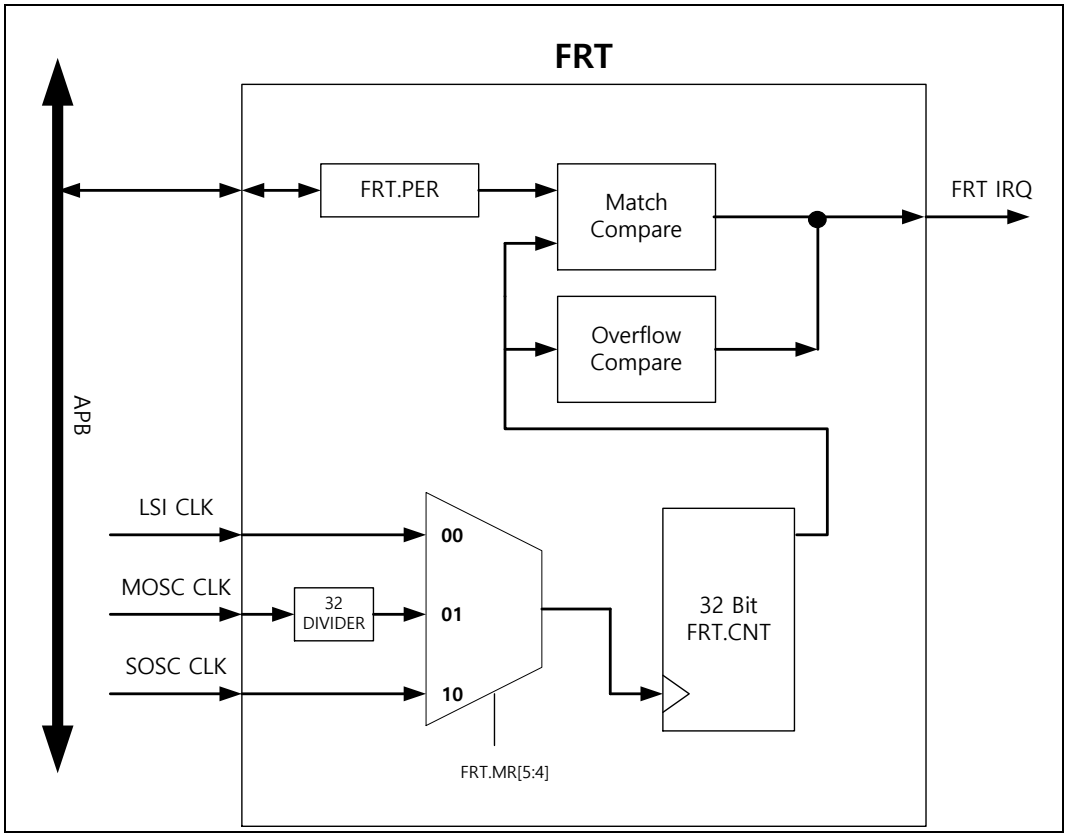


Figure 4.1 FRT block diagram

4.2 REGISTERS

The base Address of FRT is 0x4000_0100 and Timer7 is 0x4000_32E0. The register map is described in Table 4.1 and Table 4.2.

Table 4.1 Base Address of FRT and Timer7

NAME	BASE ADDRESS
FRT	0x4000_0100
TIMER7	0x4000_32E0

Table 4.2 FRT, Timer7 Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
FRT.MR	0x0000	RW	FRT mode register	0x00000000
FRT.CR	0x0004	RW	FRT control register	0x00000000
FRT.PER	0x0008	RW	FRT period match register	0x00000000
FRT.CNT	0x000C	RO	FRT counter register	0x00000000
FRT.SR	0x0010	RW	FRT status register	0x00000000

4.2.1 FRT.MR FRT Mode Register

FRT is a 32-bit up counter. It can be used in power down mode when using SUB OSC. The SUB OSC clock is directly connected to FRT. Timer Control Register is 8-bit register.

FRT.MR=0x4000_0100, TIMER7.MR=0x4000_32E0

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4	3	2	1	0
Reserved				CLKSEL	Reserved	MCD	OVIE	MIE
0x0000000				0x0	0	0	0	0
-				RW	-	RW	RW	RW

5 4	CLKSEL	FRT counter clock source control
		0 LCLK (32.768kHz)
		1 PCLK divided by 32 (FRT - 500 kHz) MCLK divided by 32 (TIMER7 - 1MHz)
		2 Reserved
		3 Reserved
2	MCD	Counter Match Clear Disable bit
		0 Counter Match Clear function is enabled. Whenever the counter matches FRT.PER, the counter will be set zero and waiting for MF to be cleared.
		1 Counter Match Clear function is disabled. The counter will keep countering without set zero
1	OVIE	Over Flow Interrupt Enable bit
		0 Not effect
		1 Interrupt enabled
0	MIE	Match Interrupt Enable bit
		0 Not effect
		1 Interrupt enabled

4.2.2 FRT.CR FRT Control Register

FRT Control Register is 8-bit register.

FRT.CR=0x4000_0104, TIMER7.CR=0x4000_32E4

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3	2	1	0
Reserved				RREN	CLR	HOLD	EN
0x0000000				0	0	0	0
-				RW	WO	RW	RW

3	RREN	FRT Counter read enable bit
	0	No action
	1	Data at FRTn.CNT will be valid.
2	CLR	FRT Counter register clear bit
	0	No action
	1	Clear the counter
1	HOLD	FRT Counter register hold bit
	0	No action
	1	Hold the counter
0	EN	FRT enable bit
	0	FRT Disabled
	1	FRT Enabled

4.2.3 FRT.PER FRT Period Match Register

FRT Period Match Register is 32-bit register

FRT.PER=0x4000_0108, , TIMER7.PER=0x4000_32E8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PERIOD																															
0x00000000																															
RW																															

32 0	PERIOD	FRT Period Match Data

4.2.4 FRT.CNT FRT Counter Register

FRT Counter Register is 32-bit register

FRT.CNT=0x4000_010C, , TIMER7.CNT=0x4000_32EC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT																															
0x00000000																															
RO																															

32 0	CNT	FRT Counter

4.2.5 FRT.SR FRT Status Register

FRT Status Register is 8-bit register.

FRT.SR=0x4000_0110, , TIMER7.SR=0x4000_32F0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														OVF	MF
0x00000000																														0	0
-																														WC1	WC1

1	OVF	Overflow Interrupt flag bit	
		0	Overflow interrupt did not occur
		1	Overflow interrupt occurred
0	MF	Interrupt flag bit	
		0	Match interrupt did not occur.
		1	Match Interrupt occurred In Counter Match Clear mode, this bit should be cleared for restarting the counter.

CHAPTER 5. DMA CONTROLLER

5.1 OVERVIEW

DMA support 8 channels. Each channel can be dedicated for each peripheral such as UART, SPI, ADC and QSPI. Table 5.3 describes each assignment for peripherals. When multiple channels are enabled, higher number of channel has higher priority. For example, channel 7 has higher priority than other channels. Channel 0 has the lowest priority.

5.2 REGISTERS

The base address of DMA Controller is 0x4000_3100 ~ 0x4000_3170 and the register map is described in Table 5.1 and Table 5.2

Table 5.1 Base Address of Each Channel

CHANNEL	BASE ADDRESS
0	0x4000_3100
1	0x4000_3110
2	0x4000_3120
3	0x4000_3130
4	0x4000_3140
5	0x4000_3150
6	0x4000_3160
7	0x4000_3170

Table 5.2 DMA Controller Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
DCn.CR	0x0000	RW	DMA CH.n Configuration Register	0x00000000
DCn.SR	0x0004	RW	DMA CH.n Status Register	0x00000080
DCn.SAR	0x0008	RW	DMA CH.n Source Address Register	0x00000000
DCn.DAR	0x000C	RW	DMA CH.n Destination Address Register	0x00000000

5.2.1 DCn.CR DMA Controller n Configuration Register

DC0.CR=0x4000_3100, DC1.CR=0x4000_3110, DC2.CR=0x4000_3120, DC3.CR=0x4000_3130, DC4.CR=0x4000_3140, DC5.CR=0x4000_3150, DC6.CR=0x4000_3160, DC7.CR=0x4000_3170.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TRANSCNT								Reserved				PERISEL				Reserved				SIZE		DADIR	SADIR
00								0x0000								0000				0000				0000				00		0	0
-								RW								-				RW				-				RW		RW	RW

29 16	TRANSCNT	Remained DMA Transfer Count Transfer count should be written before enable of DMA transfer.
11 8	PERISEL	Peripheral Selection, See the table 6.1. 0 Memory to Memory operation N Associated peripheral selection
3 2	SIZE	DMA Transfer Size 00 Byte Size Transfer 01 Half Word Size Transfer 10 Word Size Transfer 11 Reserved
1	DADIR	Destination Address Direction 0 Hold 1 Increment
0	SADIR	Source Address Direction 0 Hold 1 Increment

DMA channel can be dedicated to each peripheral. For this dedication, PERISEL field of DCnCR register should be set for each proper peripheral. The default value of PERSEL is 0, which means that any peripheral is not dedicated and this channel supports memory to memory DMA operation. The PERISEL value for each peripheral is described in Table 5.2.

Table 5.3 PERISEL Value for Each Peripheral Dedication

PERISEL	Peripheral	PERISEL	Peripheral
0	Memory to Memory operation	**8**	SPI1_TX
1	UART0_RX	**9**	ADC_CH0
2	UART0_TX	**10**	ADC_CH1
3	UART1_RX	**11**	QSPI Master
4	UART1_TX	**12**	DMI_CH0
5	SPI0_RX	**13**	DMI_CH1
6	SPI0_TX	**14**	Reserved
7	SPI1_RX	**15**	Reserved

5.2.2 DCn.SR DMA Controller n Status Register

DC0.SR=0x4000_3104, DC1.SR=0x4000_3114, DC2.SR=0x4000_3124, DC3.SR=0x4000_3134, DC4.SR=0x4000_3144, DC5.SR=0x4000_3154, DC6.SR=0x4000_3164, DC7.SR=0x4000_3174.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						INTST	INTEN	EOT	Reserved						CHEN
0x000000																						0	0	0	0x00						0
-																						RW	RW	RW	-						RW

9	INTST	Interrupt Status, this bit is set to 1 when INTEN=1, PERSEL=0, and EOT transition from low to high. This bit is cleared when DCnSR register is read.
		0 No interrupt
		1 Interrupt
8	INTEN	Interrupt Enable
		0 Disable
		1 Enable
7	EOT	End of Transfer
		0 Under transfer
		1 End of transfer
0	CHEN	Channel Enable, this bit is cleared automatically when DMA transfer is finished.
		0 Enable
		1 Disable

5.2.3 DCn.SAR DMA Controller n Source Address Register

DC0.SAR=0x4000_3108, DC1.SAR=0x4000_3118, DC2.SAR=0x4000_3128, DC3.SAR=0x4000_3138, DC4.SAR=0x4000_3148, DC5.SAR=0x4000_3158, DC6.SAR=0x4000_3168, DC7.SAR=0x4000_3178.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRCADR																															
0																															
RW																															

31 0	SRCADR	Channel n Source Address Register

5.2.4 DCn.DAR DMA Controller n Destination Address Register

DC0.DAR=0x4000_310C, DC1.DAR=0x4000_311C, DC2.DAR=0x4000_312C, DC3.DAR=0x4000_313c, DC4.DAR=0x4000_314C, DC5.DAR=0x4000_315C, DC6.DAR=0x4000_316C, DC7.DAR=0x4000_317C.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSTADR																															
0																															
RW																															

31 0	DSTADR	Channel n Destination Address Register

CHAPTER 6. TIMER

6.1 OVERVIEW

The timer block is consisted with 10 channels of 16 bit General purpose timers. They have independent 16 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.
One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 10-bit prescaler
- Synchronous start and clear function

Figure 6.1 shows the block diagram of a unit timer block.

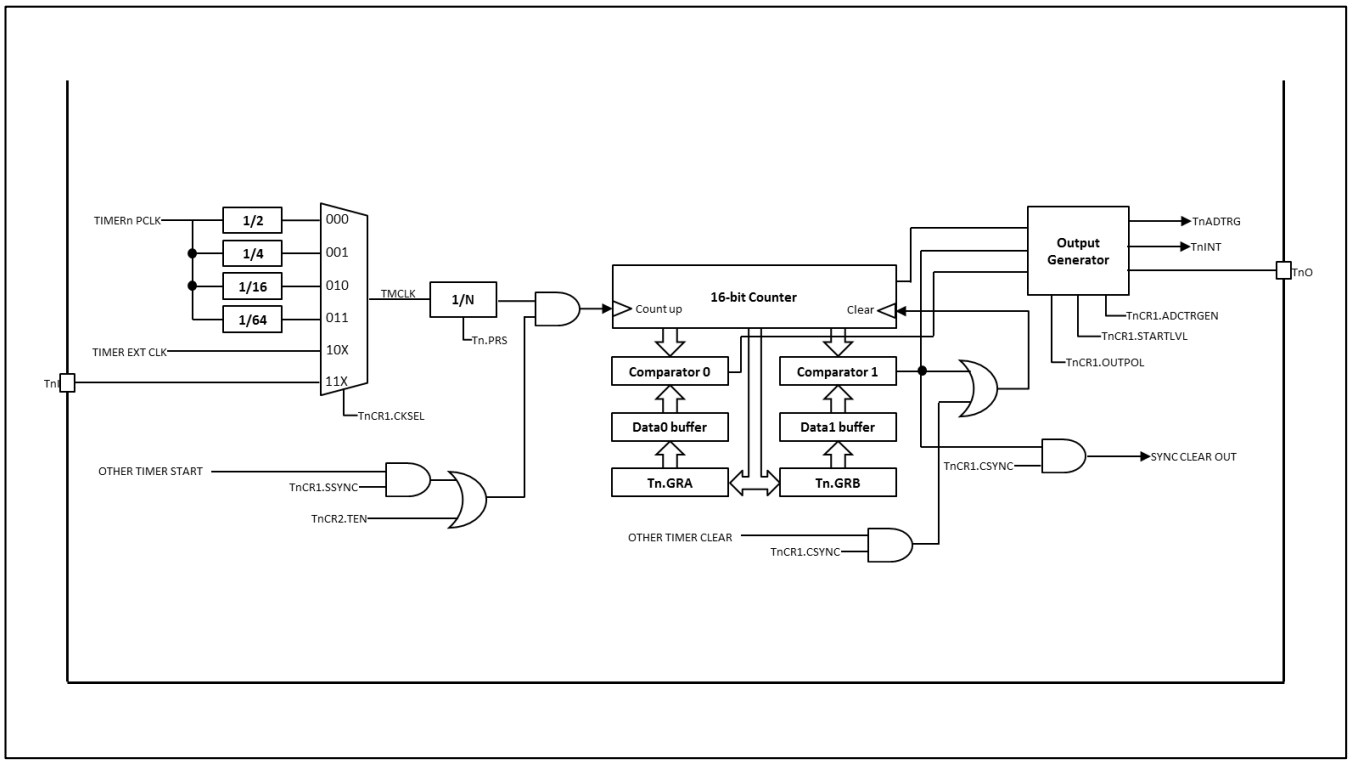


Figure 6.1 Timer Block Diagram

6.2 PIN DESCRIPTION

Table 6.1 External Pin

PIN NAME	TYPE	DESCRIPTION
TnIO	I/O	External clock / capture input and PWM/one-shot output

6.3 REGISTERS

The Base Address of TIMER0/1/2/3 is 0x4000_3200, 0x4000_3220, 0x4000_3240 and 0x4000_3260. The register map is described in Table 6.2 and Table 6.3.

Table 6.2 Base Address of Each Channel

CHANNEL	BASE ADDRESS
T0	0x4000_3200
T1	0x4000_3220
T2	0x4000_3240
T3	0x4000_3260

Table 6.3 Timer Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
T*n*.CR1	0x0000	RW	Timer control register 1	0x00000000
T*n*.CR2	0x0004	RW	Timer control register 2	0x00000000
T*n*.PRS	0x0008	RW	Timer prescaler register	0x00000000
T*n*.GRA	0x000C	RW	Timer general data register A	0x00000000
T*n*.GRB	0x0010	RW	Timer general data register B	0x00000000
T*n*.CNT	0x0014	RW	Timer counter register	0x00000000
T*n*.SR	0x0018	RW	Timer status register	0x00000000
T*n*.IER	0x001C	RW	Timer interrupt enable register	0x00000000

6.3.1 Tn.CR1 Timer n Control Register 1

Timer Control Register 1 is 16-bit register.

Timer module should be configured properly before running. After configuring this register, the timer can be started or stopped by Tn.CR2 register.

T0.CR1=0x4000_3200, T1.CR1=0x4000_3220,
T2.CR1=0x4000_3240, T3.CR1=0x4000_3260.

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11 10 9	8	7	6 5 4	3 2	1 0
Reserved		SYNC	CSYNC	UAO	OUTPOL	Reserved	ADCTRGEN	STARTLVL	CKSEL	CLRMOD	MODE
0x0000		0	0	0	0	0x0	0	0	0x0	0x0	0
-		RW	RW	RW	RW	-	RW	RW	RW	RW	RW

15	SSYNC	Synchronize start counter with other synchronized timers	
		0	Single counter mode
		1	Synchronized counter start mode
14	CSYNC	Synchronize clear counter with other synchronized timers	
		0	Single counter mode
		1	Synchronized counter clear mode
13	UAO	Select GRA, GRB update mode	
		0	Writing GRA or GRB takes effect after current period
		1	Writing GRA or GRB takes effect in current period
12	OUTPOL	Timer output polarity	
		0	Normal output
		1	Negated output
8	ADCTRGEN	ADC Trigger enable control	
		0	Disable ADC trigger
		1	Enable ADC trigger at same time of GRA match
7	STARTLVL	Timer output polarity control	
		0	Default output level is HIGH
		1	Default output level is LOW
6 4	CKSEL[2:0]	Counter clock source select	
		000	PCLK/2
		001	PCLK/4
		010	PCLK/16
		011	PCLK/64
		10X	MCCR3 clock setting
		11X	TnIO pin input (TnIO pin must be set as input mode)
3 2	CLRMD	Clear select when capture mode	
		00	Rising edge clear mode
		01	Falling edge clear mode
		10	Both edge clear mode
		11	None clear mode
1 0	MODE[1:0]	Timer operation mode control	
		00	Normal periodic operation mode
		01	PWM mode
		10	One shot mode
		11	Capture mode

6.3.2 Tn.CR2 Timer n Control Register 2

Timer Control Register 2 is 8-bit register.

T0.CR2=0x4000_3204, T1.CR2=0x4000_3224,
T2.CR2=0x4000_3244, T3.CR2=0x4000_3264.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														TCLR	TEN
0x00000000																														0	0
-																														WO	RW

1	TCLR	Timer register clear	
		0	Normal operation
		1	Clear count register. (This bit will be cleared after next timer clock)
0	TEN	Timer enable bit	
		0	Stop timer counting
		1	Start timer counting

It is recommended to start timer with TCLR bit setting to be ‘1’.

6.3.3 Tn.PRS Timer n Prescaler Register

Timer Prescaler Register is 16-bit register in order to prescale the counter input clock.

T0.PRS=0x4000_3208, T1. PRS=0x4000_3228,
T2.PRS=0x4000_3248, T3. PRS=0x4000_3268.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						PRS									
0x000000																						0x000									
-																						RW									

9 0	PRS	Pre-scale value of count clock TCLK = CLOCK_IN/(PRS+1) (*CLOCK_IN* is a selected timer input clock)

6.3.4 Tn.GRA Timer n General Register A

Timer General Register A is 16-bit register.

T0.GRA=0x4000_320C, T1.GRA=0x4000_322C,
T2.GRA=0x4000_324C, T3.GRA=0x4000_326C.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																GRA															
0x0000																0x0000															
-																RW															

15 0	GRA	General Register A (Duty/Interrupt Register) Periodic mode / PWM / One-shot mode - In PWM mode this register is used as duty value. - When the counter value is matched with this value, GRA Match interrupt is requested Capture mode - Falling edge of TnIO port will capture the count value when rising edge clear mode - Rising edge of TnIO port will capture the count value when falling edge clear mode

6.3.5 Tn.GRB Timer n General Register B

Timer General Register B is 16-bit register.

T0.GRB=0x4000_3210, T1.GRB=0x4000_3230,
T2.GRB=0x4000_3250, T3.GRB=0x4000_3270.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																GRB															
0x0000																0x0000															
-																RW															

15 0	GRB	General Register B (Period Register) Periodic mode / PWM / One-shot mode - In periodic mode or PWM mode, this register is used as Period value. The counter will count up to (GRB-1) value. - When the counter value is matched with this value, GRB Match interrupt is requested only in PWM and one-shot modes. Capture mode - Rising edge of TnIO port will capture the count value when rising edge clear mode - Falling edge of TnIO port will capture the count value when falling edge clear mode

6.3.6 Tn.CNT Timer n Count Register

Timer Count Register is 16-bit register.

T0.CNT=0x4000_3214, T1.CNT=0x4000_3234,
T2.CNT=0x4000_3254, T3.CNT=0x4000_3274.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRECLR																CNT															
0x0000																0x0000															
WO																RW															

31 16	PRECLR	Prescaler initialize when timer count value write operation	
		0x0000	Prescaler will be initialized when write timer count value on TnCNT[15:0]. After writing the count value, prescaler restarted from initial state to make accurate period for first count.
		others	Prescaler will not be initialized and maintain current conditions when writing timer count value on TnCNT[15:0]. First count period is not accurate depending on its status when writing operation.
15 0	CNT	Timer count value register	
		R	Read current timer count value
		W	Set count value

6.3.7 Tn.SR Timer n Status Register

Timer Status Register is 8-bit register.

This register indicates the current status of timer module

T0.SR=0x4000_3218, T1.SR=0x4000_3238,
T2.SR=0x4000_3258, T3.SR=0x4000_3278.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													MFA	MFB	OVF
0x0000000																													0	0	0
-																													RW	RW	RW

2	MFA	GRA Match flag
		0 No direction change
		1 Match flag with GRA
1	MFB	GRB Match flag
		0 No direction change
		1 Match flag with GRB
0	OVF	Counter overflow flag
		0 No direction change
		1 Counter overflow flag

6.3.8 Tn.IER Timer n Interrupt Enable Register

Timer Interrupt Enable Register is 8-bit register.

Each status flag of the timer block can issue the interrupt. To enable the interrupt, write “1” in correspondent bit in the TnIER register.

T0.IER=0x4000_321C, T1.IER=0x4000_323C,
T2.IER=0x4000_325C, T3.IER=0x4000_327C.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													MAIE	MBIE	OVIE
0x0000000																													0	0	0
-																													WO	RW	WO

2	MAIE	GRA Match interrupt enable	
		0	Not effect
		1	Enable match register A interrupt
1	MBIE	GRB Match interrupt enable	
		0	Not effect
		1	Enable match register B interrupt
0	OVIE	Counter overflow interrupt enable	
		0	Not effect
		1	Enable counter overflow interrupt

6.4 Functional Description

6.4.1 Timer basic operation

TMCLK in Figure 6.2 is reference clock for operation of the timer. This clock will be divided by the prescaler setting and the counting clock will work. Below figures show the starting point of the counter and the ending of the period point of the counter in normal periodic mode.

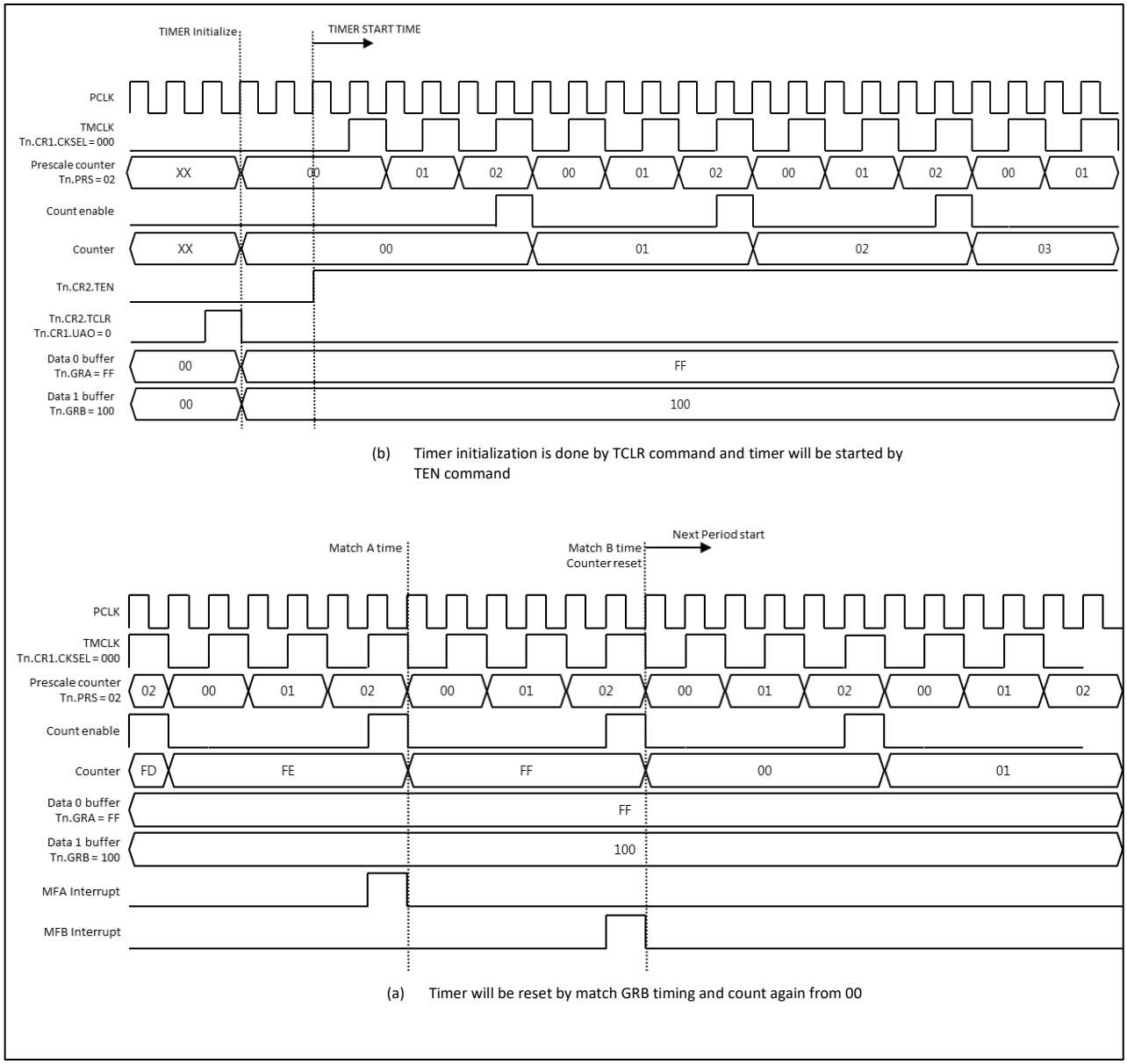


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Figure 6.2 Basic Start and Match Operation

The period = TMCLK Period * Tn.GRB value.

Match A interrupt time = TMCLK Period * Tn.GRA value.

If Tn.CR1.UAO bit is “0”. Tn.CR2.TCLR command will initialize all the registers in timer block and load the GRA and GRB value into Data0 and Data1 buffer. When setting and restarting the timer with new configuration, it is recommended that CR2.TCLR command should be written before CR2.TEN command.

The update timing of Data0 and Data1 buffer in dynamic operation, is different in each operating mode and depends on the Tn.CR1.UAO bit.

6.4.2 Normal Periodic Mode

Figure 6.3 shows the timing diagram in normal periodic mode. Tn.GRB value decides the timer period. One more compare point is provided with Tn.GRA register value.

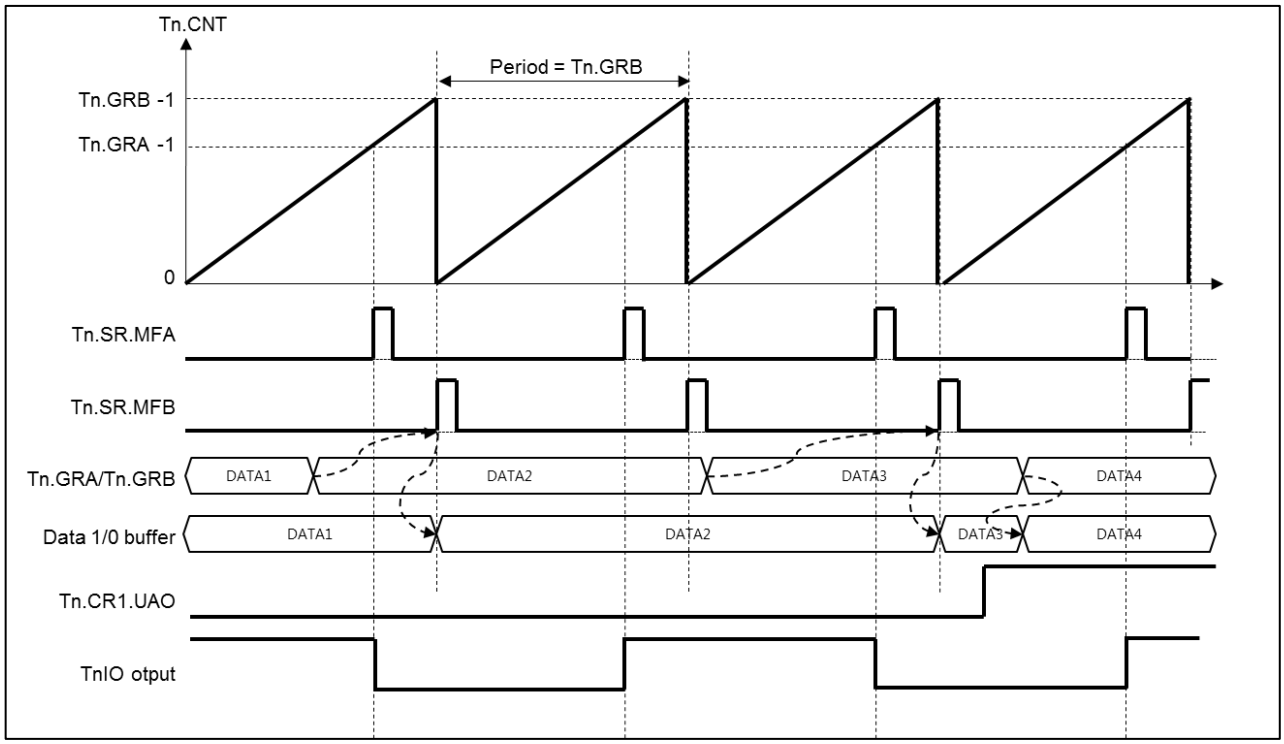


Figure 6.3 Normal Periodic Mode Operation

The period of timer count can be calculated as below equation.
The period = TMCLK Period * Tn.GRB value.
Match A interrupt time = TMCLK Period * Tn.GRA value.
If Tn.GRB = 0, the timer cannot be started even TnCR2.TEN is “1” because the period is “0”.
The value in Tn.GRA and Tn.GRB is loaded into internal compare data buffer 0 and 1 when the loading condition occurs. In this periodic mode with TnCR1.UAO =0, Tn.CR2.TCLR write operation will load the data buffer and the next GRB match event will load the data buffer.
When TnCR1.UAO is 1, The internal compare data buffer is updated whenever the Tn.GRA or Tn.GRB data is updated.
TnIO output signal will be toggled at every Match A condition time. If TnGRA is 0 value, the TnIO output is not change its previous level. If TnGRA is same as TnGRB, the TnIO ouput will toggle at same time as counter start time. The initial level of TnIO signal is decided by TnCR1.STARTLVL value.

6.4.3 One shot Mode

Figure 6.4 shows the timing diagram in one shot mode. Tn.GRB value decides the one shot period. One more compare point is provided with Tn.GRA register value.

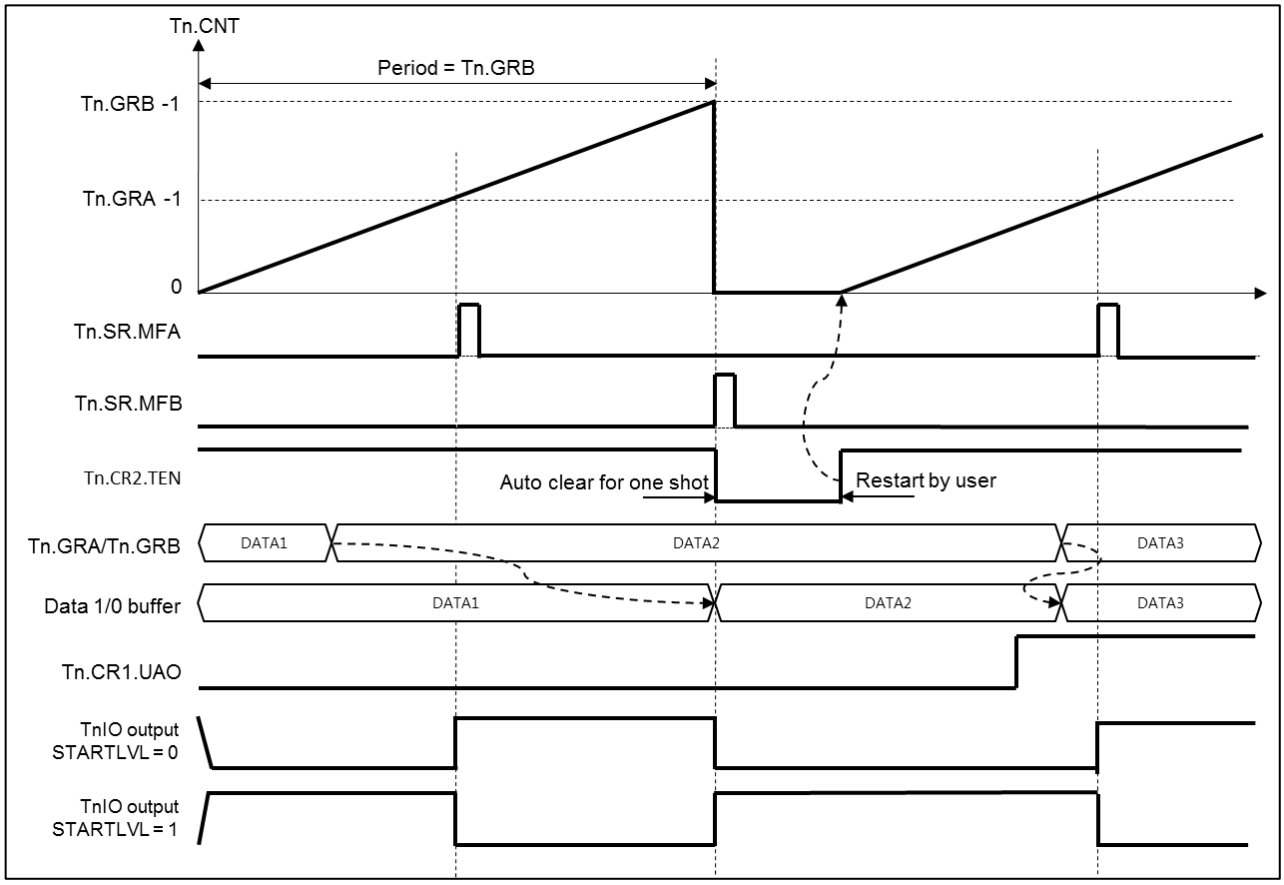


Figure 6.4 One Shot Mode Operation

The period of one-shot count can be calculated as below equation.
The period = TMCLK Period * Tn.GRB value.
Match A interrupt time = TMCLK Period * Tn.GRA value.
If Tn.GRB = 0, the timer cannot be started even TnCR2.TEN is “1” because the period is “0”.
The value in Tn.GRA and Tn.GRB is loaded into internal compare data buffer 0 and 1 when the loading condition occurs. In this periodic mode with TnCR1.UAO =0, Tn.CR2.TCLR write operation will load the data buffer and the next GRB match event will load the data buffer.
When TnCR1.UAO is 1, The internal compare data buffer is updated whenever the Tn.GRA or Tn.GRB data is updated.
TnIO output signal format is same as pwm mode. Tn.GRB value defines the output pulse period and Tn.GRA value defines the pulse width of one-shot pulse.

6.4.4 PWM Timer output examples

Figure 6.5 shows the timing diagram of the pwm output mode. Tn.GRB value decides the pwm pulse period. One more compare point is provided with Tn.GRA register value which defines pulse width of pwm output.

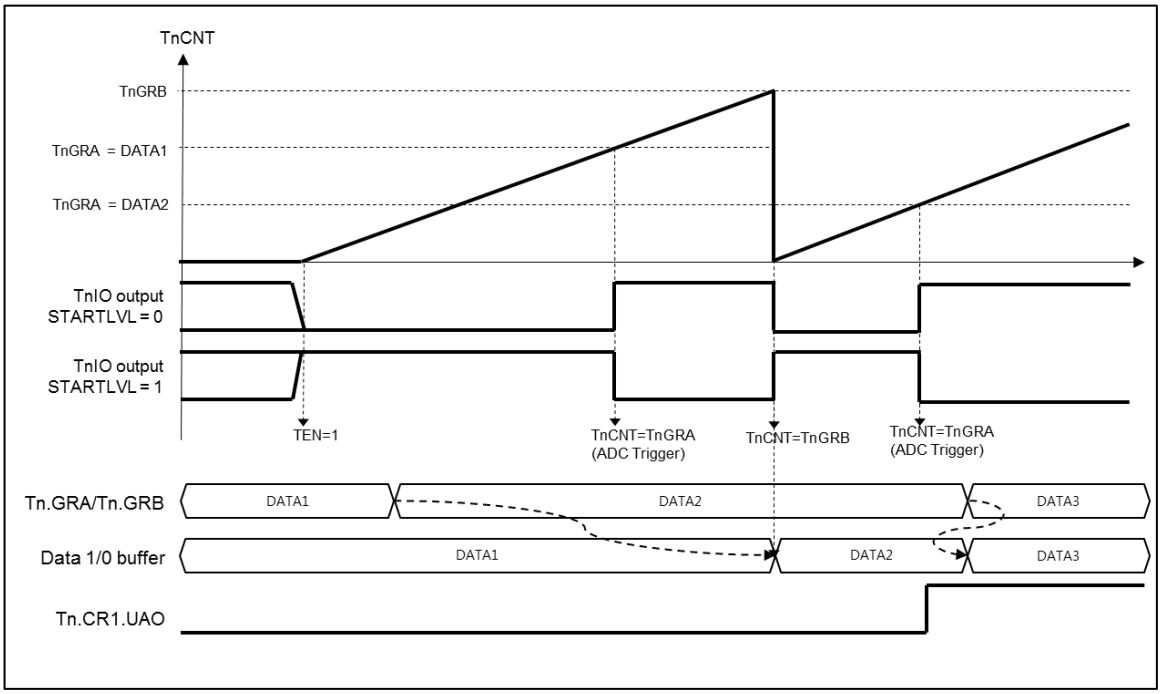


Figure 6.5 PWM Output Example

The period of pwm pulse can be calculated as below equation.
The period = TMCLK Period * Tn.GRB value.
Match A interrupt time = TMCLK Period * Tn.GRA value.
If Tn.GRB = 0, the timer cannot be started even TnCR2.TEN is “1” because the period is “0”.
The value in Tn.GRA and Tn.GRB is loaded into internal compare data buffer 0 and 1 when the loading condition occurs. In this periodic mode with TnCR1.UAO =0, Tn.CR2.TCLR write operation will load the data buffer and the next GRB match event will load the data buffer.
When TnCR1.UAO is 1, The internal compare data buffer is updated whenever the Tn.GRA or Tn.GRB data is updated.
TnIO output signal generates pwm pulse. Tn.GRB value defines the output pulse period and Tn.GRA value defines the pulse width of one shot pulse. The active level of pwm pulse can be control by Tn.CR1.STARTLVL bit value.
ADC Trigger generation is available at Match A interrupt time.

6.4.5 PWM Synchronization function

2 PWM outputs usually used as synchronous pwm signal control. This function is provided with synchronous start function. Figure 6.6 and Figure 6.7 show synchronous pwm generation function.

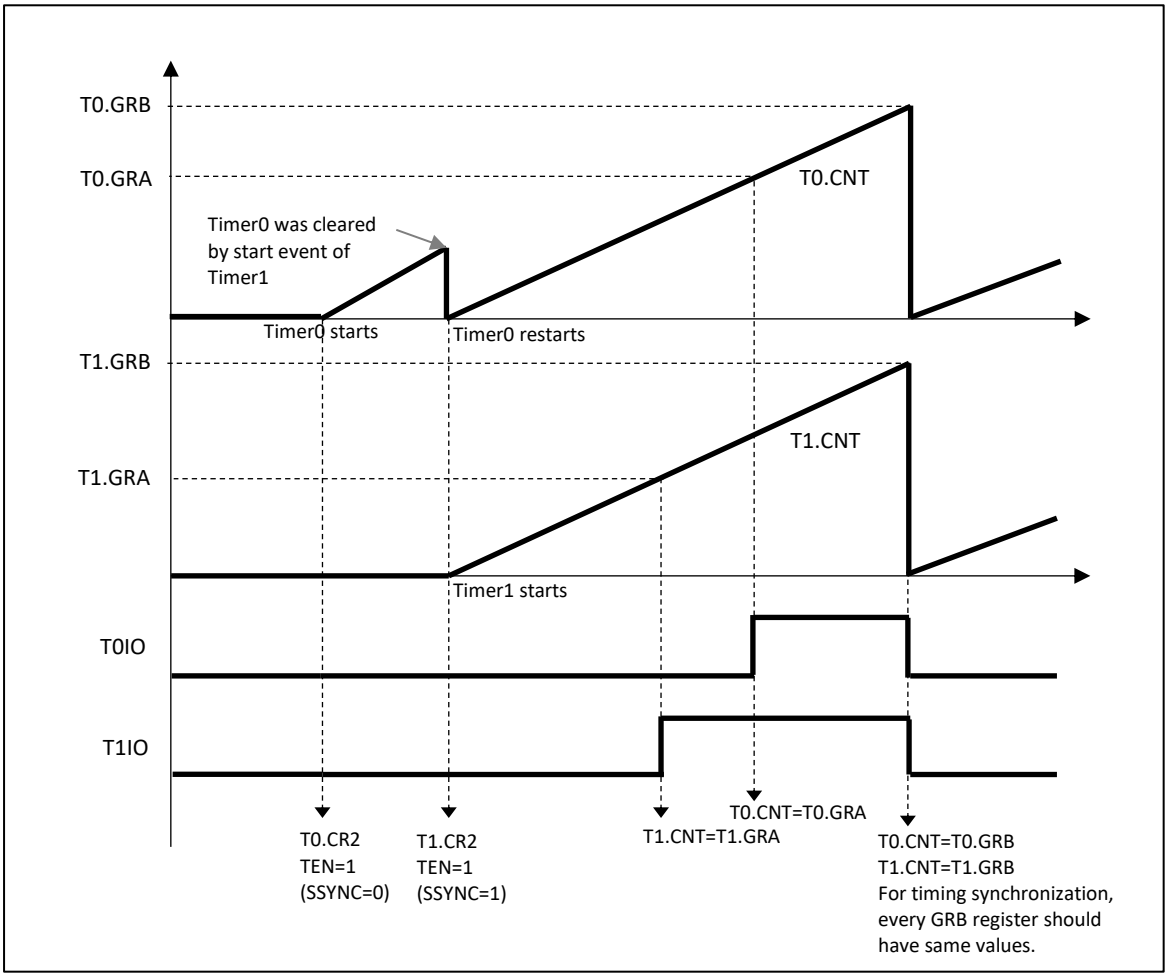


Figure 6.6 A Example of Timer Synchronization Function (SSYNC='0')

TnCR1.SSYNC bit controls start sync with other timer blocks. TnCR1.CSYCN bit controls clear sync with other timer blocks. This bit is effective at least 2 more timers are set these sync control bits.

For example, timer0 and timer1 set SSYNC and CCSYNC bit in each CR1 registers, both timers will start whenever one of them is enabled. Both of the timers will cleared with short period match value. Others are not affected by these 2 timers, and they can be operated independently because their SYNC control bit is 0.

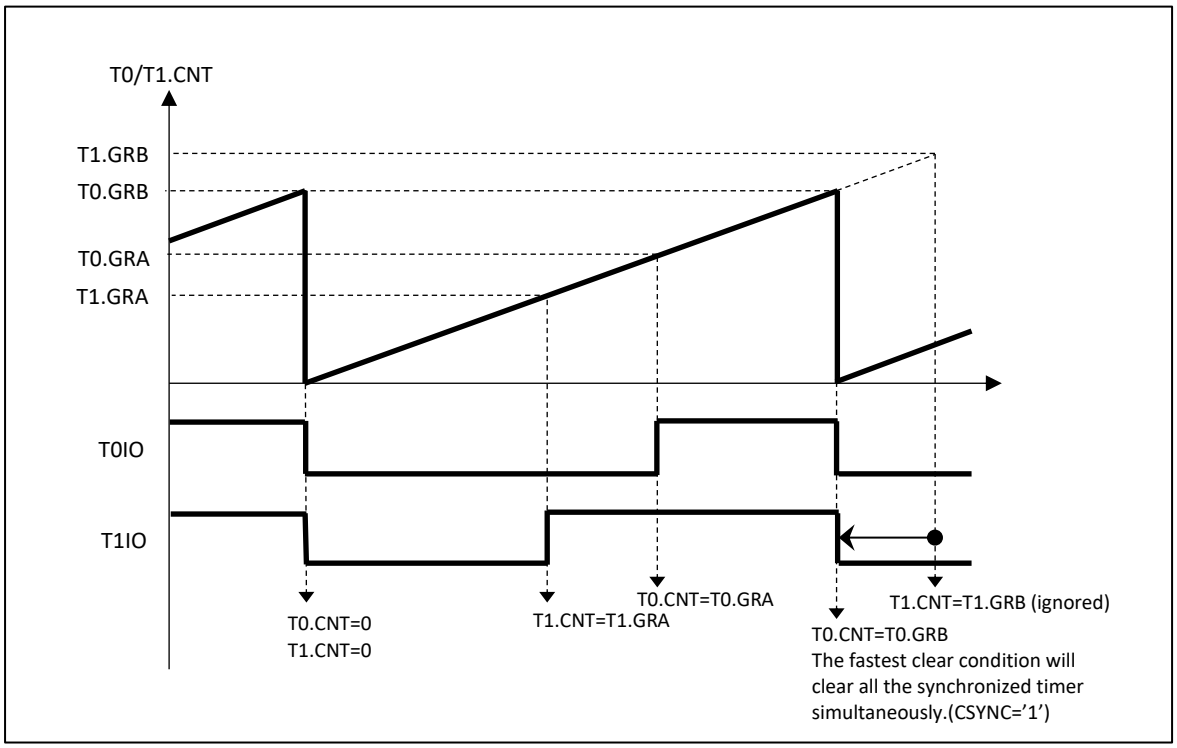


Figure 6.7 A Example of Timer Synchronization Function (CSYNC='1')

6.4.6 Capture mode

Figure 6.8 shows the timing diagram in capture mode operation. TnIO input signal is used for capture pulse. Both of rising and falling edge can capture the counter valued in each capture conditions.

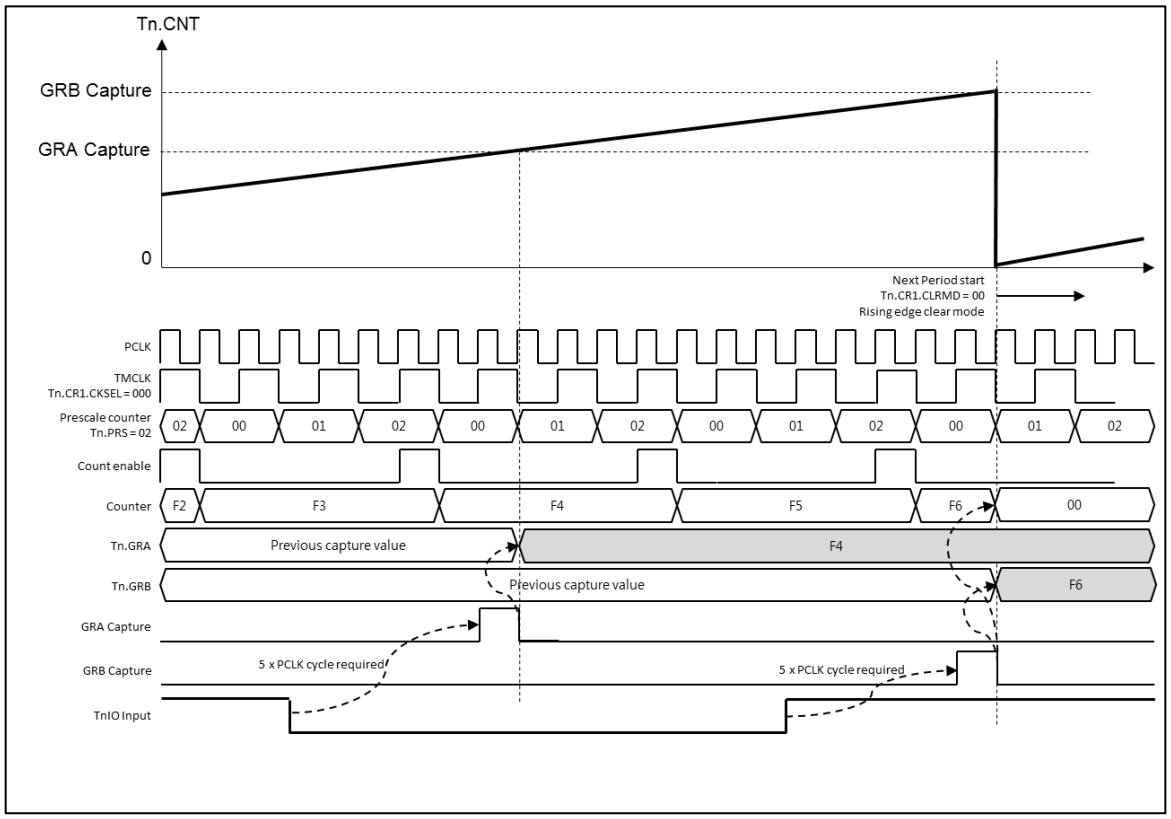


Figure 6.8 ADC trigger function timing diagram

5 PCLK clock cycle is required internally. So capture point is after 5 PCLK clock cycles from rising or falling edge of TnIO input signal.

Internal counter can be cleared in various mode. TnCR1.CLRMD field controls the counter clear mode. Rising edge clear mode, Falling edge clear mode, Both edge clear mode and none clear mode are supported.

Figure 7.8 case is rising edge clear mode.

6.4.7 ADC trigger function

Timer module can generate ADC start trigger signals. One timer can be one trigger source of ADC block. Trigger source control is done by ADC control register.

Figure 6.9 shows ADC trigger function.

The conversion rate must be shorter than timer period. If it is not a case, overrun situation can be happened. ADC acknowledge is not required , because trigger signal will be cleared automatically after 3 pclk clock pulses.

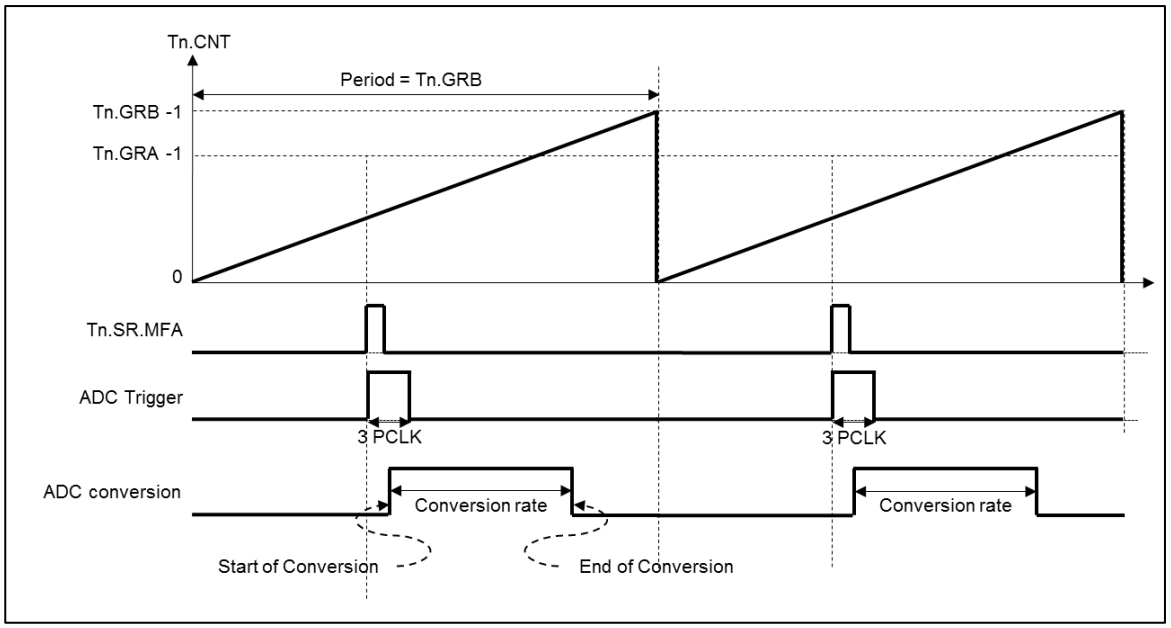


Figure 6.9 ADC trigger function timing diagram

CHAPTER 7. WATCH DOG TIMER

7.1 OVERVIEW

The Watchdog timer can monitor the system and generate an interrupt or a reset. It has 32-bit down-counter.

- 32-bit down counter (WDTCNT)
- Select reset or periodic interrupt
- Count clock selection
- Dedicated pre-scaler
- Watchdog underflow output signal

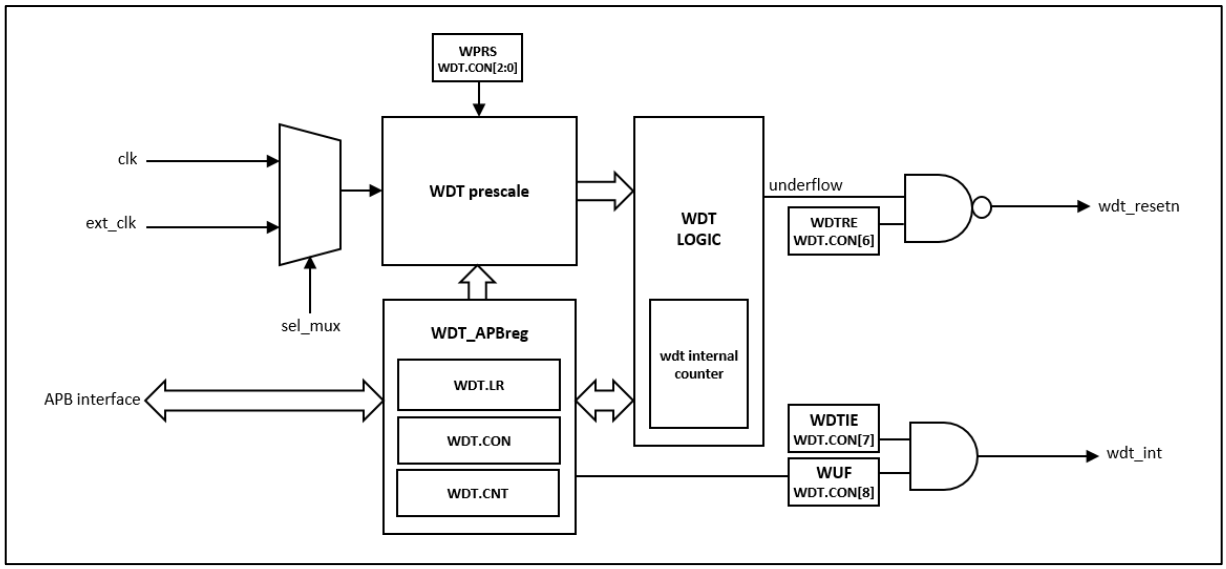


Figure 7.1 Block Diagram

7.2 REGISTERS

The base Address of watchdog timer is 0x4000_3300 and register map is described in Table 7.1 and Table 7.2 .
Initial watchdog time-out period is set to 2,000-milisecond.

Table 7.1 Base Address of WDT

NAME	BASE ADDRESS
WDT	0x4000_3300

Table 7.2 Watchdog Timer Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
WDT.LR	0x0000	RW	WDT Load register	0x00000000
WDT.CNT	0x0004	RW	WDT Current counter value register	0x0000FFFF
WDT.CON	0x0008	RW	WDT Control register	0x0000805C

7.2.1 WDT.LR Watchdog Timer Load Register

The WDTLR register is used to update WDTCNT register. To update WDTCNT register, the WDTEN bit of WDTCON should be set to '1' and write into WDTLR register with target value of WDTCNT. It needs at least 5 WDT counter clocks to update WDTLR to WDTCNT.

WDT.LR=0x4000_3300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTLR																															
0xFFFFFFFF																															
RW																															

31 0	WDTLR	Watchdog timer load value register Keeping WDTEN bit as '1', write WDTLR register will update WDTCNT value with written value

7.2.2 WDT.CNT Watchdog Timer Current Counter Value Register

The WDTCNT register represents the current count value of 32-bit down counter. When the counter value reach to 0, the interrupt or reset will be asserted.

WDT.LR=0x4000_3304

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTCNT																															
0x00000000																															
RW																															

31 0	WDTCNT	Watchdog timer current counter value register 32-bit down counter will run from the written value.

7.2.3 WDT.CON Watchdog Timer Control Register

WDT module should be configured properly before running. WDT module can make reset event or assert interrupt signal to system. If user don't use both reset and interrupt functions, WDT can be used like a loadable down-counter. WUF flag will be set when WDT counts down to 0.

WDT.CONT=0x4000_3308

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14 13 12 11 10 9	8	7	6	5	4	3	2 1 0
Reserved		WDBG	Reserved	WUF	WDTIE	WDTRE	Reserved	WDTEN	CKSEL	WPRS
0x0000		1	0x00	0	0	1	0	1	1	100
-		RW	-	RW	RW	RW	-	RW	RW	RW

15	WDBG	Watchdog operation control in debug mode	
		0	Watchdog counter running when debug mode
		1	Watchdog counter stopped when debug mode
8	WUF	Watchdog timer underflow flag	
		0	No underflow
		1	Underflow is pending
7	WDTIE	Watchdog timer counter underflow interrupt enable	
		0	Disable interrupt
		1	Enable interrupt
6	WDTRE	Watchdog timer counter underflow reset enable	
		0	Disable reset
		1	Enable reset
4	WDTEN	Watchdog Counter enable	
		0	Watch dog counter disabled
		1	Watch dog counter enabled
3	CKSEL	WDTCLKIN clock source select	
		0	PCLK
		1	External clock
2 0	WPRS[2:0]	Counter clock prescaler WDTCLK = WDTCLKIN/WPRS	
		000	WDTCLKIN
		001	WDTCLKIN / 4
		010	WDTCLKIN / 8
		011	WDTCLKIN / 16
		100	WDTCLKIN / 32
		101	WDTCLKIN / 64
		110	WDTCLKIN / 128
		111	WDTCLKIN / 256

7.3 Functional Description

The watchdog timer Count can be enabled by WDTEN (WDT.CON[4]) to 1. As watchdog timer is enabled, the down counter will start counting from the Load Value. If WDTRE (WDT.CON[6]) is set as 1, WDT reset would be asserted when the WDT counter value reached to 0(underflow event) from WDTLR value. Before WDT counter down to 0, software can write a certain value to register WDTLR to reload WDT counter.

7.3.1 Timing Diagram

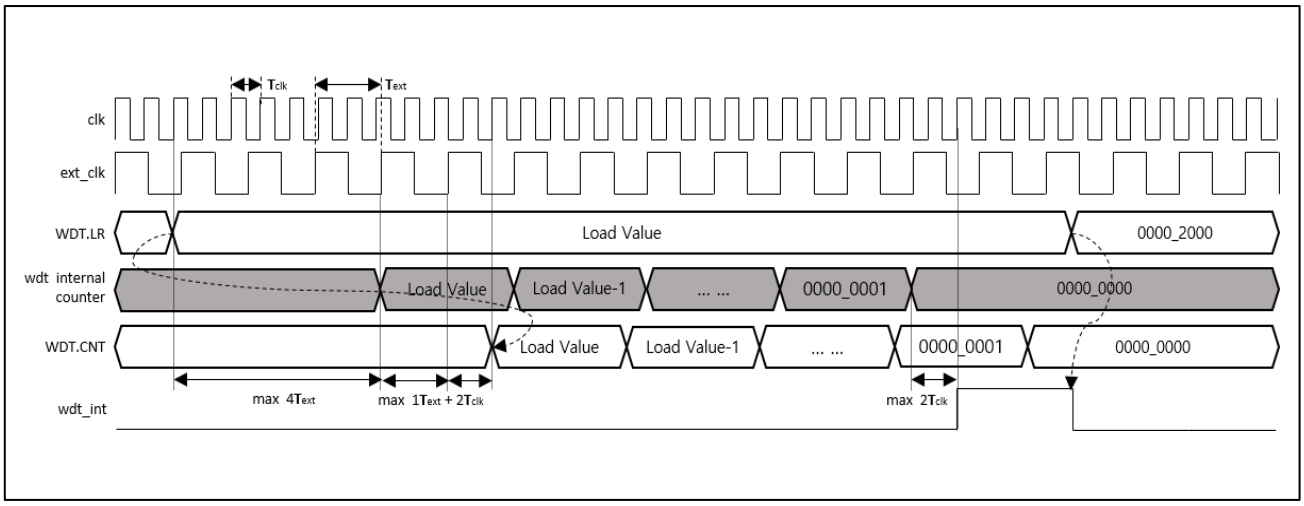


Figure 7.2 Timing diagram in interrupt mode operation when WDT clock is external clock

In WDT interrupt mode, once WDT underflow occurred then a certain count value would be reloaded to prevent next WDT interrupt in short time period and this reloading action only be activated when the watchdog timer counter set to be Interrupt mode(set WDTIE of WDT.CON). It takes up to 5 cycle from Load value to the CNT value. The WDT interrupt signal and CNT value data might be delayed maximum by 2 system bus clocks in synchronous logic.

7.3.2 Prescale Table

The WDT includes a 32-bit down counter with programmable pre-scaler to define different time-out intervals.

The clock sources of watchdog timer can be peripheral clock (PCLK) or one of 5external clock sources. External clock source can be enable by CKSEL (WDT.CON[3]) set to '1' and External clock source was chosen in MCCR3 register of SCU(system control unit) block.

To make WDT counter base clock, user can control 3-bit pre-scaler WPRS [2:0] in WDT.CON register and the maximum pre-scaled value is "clock source frequency/256". The pre-scaled WDT counter clock frequency values are listed in following table.

Selectable clock source (40 kHz ~ 16 MHz) and the time out interval when 1 count

Time out period = {(Load Value) * (1/pre-scaled WDT counter clock frequency) + max 5Text} + max 4Tclk

*Time out period (time out period from load Value to interrupt set '1')

Table 7.3 Pre-scaled WDT Counter Clock Frequency

External Clock source (WDTCLKIN)	WDTCLKIN	WDTCLKIN / 4	WDTCLKIN / 8	WDTCLKIN / 16	WDTCLKIN / 32	WDTCLKIN / 64	WDTCLKIN / 128	WDTCLKIN / 256
LSI	40kHz	10kHz	5kHz	2.5kHz	1.25kHz	0.625kHz	0.3125kHz	0.15625kHz
MCLK	Bus clock	MCLK/4	MCLK/8	MCLK/16	MCLK/32	MCLK/32	MCLK/128	MCLK/256
HSI	40MHz	10MHz	5MHz	2.5MHz	1.25MHz	0.625MHz	0.3125MHz	0.15625MHz
EMOSC	XTAL frequency (1MHz~ 16MHz)	XTAL/4	XTAL/8	XTAL/16	XTAL/32	XTAL/64	XTAL/128	XTAL/256
ESOSC	32.768kHz	8.192kHz	4.096kHz	2.048kHz	1.024kHz	0.512kHz	0.256kHz	0.128kHz

CHAPTER 8. UART

8.1 OVERVIEW

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 3 to 65535. Baud rate generation is done by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication
  - 5-, 6-, 7- or 8- bit data transfer
  - Even, odd, or no-parity bit insertion and detection
  - 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register
- Support up to 1M baudrate
- Support hardware flow control with CTS and RTS

8.2 PIN DESCRIPTION

UART module provide 16450 UART compatible pins such as TXD, RXD, RTS and CTS. Refer to chapter 8.4 function description for the detail timing of pins.

Table 8.1 External PIN

PIN NAME	TYPE	DESCRIPTION
UART_TXD	O	TX Data
UART_RXD	I	RX Data
UART_RTS	O	Flow Control Output
UART_CTS	I	Flow Control Input

8.3 REGISTERS

The base address of UART0/1 is 0x4000_8000 and 0x4000_8100. The register map is described in Table 8.2 and Table 8.3

Table 8.2 Base Address of UART

NAME	BASE ADDRESS
UAR0	0x4000_8000
UAR1	0x4000_8100

Table 8.3 Timer Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
Un.RHR	0x0000	RO	UART n Receive Data Hold Register	0x00000000
Un.THR	0x0000	RW	UART n Transmit Data Hold Register	0x00000000
Un.IER	0x0004	RW	UART n Interrupt Enable Register	0x00000000
Un.IIR	0x0008	RO	Interrupt Pending Bit	0x00000001
Un.LCR	0x000C	RW	UART n Line Control Register	0x00000000
Un.MCR	0x0010	RO	UART n Modem Control Register	0x00000000
Un.LSR	0x0014	RO	UART n Line Status Register	0x00000060
Un.MSR	0x0018	RO	UART n Modem Status Register	0x00000000
Un.BDR	0x0020	RW	Baud Rate divisor value	0x00000000
Un.BFR	0x0024	RW	Baud Rate fraction value	0x00000000
Un.DTR	0x0030	RW	Interval value	0x00000000

8.3.1 Un.RHR UART n Receive Data Hold Register

U0.RHR=0x4000_8000, U1.RHR=0x4000_8100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								RHR							
																								0x00							
																								R							

7 0	RHR	UART n Receive Data Hold Register

8.3.2 Un.THR UART n Transmit Data Hold Register

U0.THR=0x4000_8000, U1.THR=0x4000_8100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								THR							
																								0x00							
																								W							

7 0	THR	UART n Transmit Data Hold Register

8.3.3 Un.IER UART n Interrupt Enable Register

U0.IER=0x4000_8004, U1.IER=0x4000_8104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										TXIEN	RXIEN	MSIE	RLSIE	THREIE	DRIE
																										0	0	0	0	0	0
																										RW	RW	RW	RW	RW	RW

5	TXIEN	Transmit Done Interrupt Enable
		0 Disable
		1 Enable
4	RXIEN	Receiver Done Interrupt Enable
		0 Disable
		1 Enable
3	MSIE	Modem Status Interrupt Enable
		0 Disable
		1 Enable
2	RLSIE	Receiver Line Status Interrupt Enable
		0 Disable
		1 Enable
1	THREIE	Transmit Holding Register Empty Interrupt Enable
		0 Disable
		1 Enable
0	DRIE	Data Receive Interrupt Enable
		0 Disable
		1 Enable

8.3.4 Un.IIR Interrupt Pending Bit

U0.IIR=0x4000_8008, U1.IIR=0x4000_8108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												IID			
																												0x1			
																												R			

3	IID	Data Receive Interrupt Enable
0		IID[0] : Interrupt Pending Bit
	0	Interrupt is pending.
	1	No interrupt is pending.
		UART n Interrupt ID Register
	011X	Rx line status error
	010X	Rx data available
	001X	Tx empty
	000X	Modem status
	110X	Rx done
	101X	Tx done

8.3.5 Un.LCR UART n Line Control Register

U0.LCR=0x4000_800C, U1.LCR=0x4000_810C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DLAB	BREAK	STICKP	PARITY	PEN	STOPBIT	DLEN	
																								0	0	0	0	0	0	0x0	
																								RW	RW	RW	RW	RW	RW	RW	

7	DLAB	Reserved
		0
		1
6	BREAK	Set break
		0
		1
5	STICKP	Stick parity select
		0
		1
4	PARITY	Even parity select
		0
		1
3	PEN	Parity enable
		0
		1
2	STOPBIT	Number of stop bit
		0
		1
1	DLEN	Data length
0		00
		01
		10
		11

8.3.6 Un.MCR UART n Modem Control Register

U0.MCR=0x4000_8010, U1.MCR=0x4000_8110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																					HFC_RTSTIM	HFC_CTSEN	HFC_RTSEN	Reserved			LBON	RXINV	TXINV	RTS	DTR
																					0	0	0				0	0	0	0	0
																					RW	RW	RW				RW	RW	RW	RW	RW

10	HFC_RTSTIM	RTS Timing Control
		0 RTS goes high at stop bit state 1 RTS goes high when receiving data
9	HFC_CTSEN	Hardware Flow Control CTS Enable
		0 Disable 1 Enable
8	HFC_RTSEN	Hardware Flow Control RTS Enable
		0 Disable 1 Enable
4	LBON	Loopback Mode On
		0 Disable 1 Enable
3	RXINV	Rx Data Inversion
		0 Disable 1 Enable
2	TXINV	Tx Data Inversion
		0 Disable 1 Enable
1	RTS	Request To Send
		0 1
0	DTR	Data Terminal Ready
		0 1

8.3.7 Un.LSR UART n Line Status Register

U0.LSR=0x4000_8014, U1.LSR=0x4000_8114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									TEMP	THRE	BI	FE	PE	OE	DR
																									1	1	0	0	0	0	0
																									R	R	R	R	R	R	R

6	TEMT	Transmit empty
		0
		1
5	THRE	Transmit hold empty
		0
		1
4	BI	Break interrupt
		0
		1
3	FE	Framing error
		0
		1
2	PE	Parity error
		0
		1
1	OE	Overrun error
		0
		1
0	DR	Receive data ready
		0
		1

8.3.8 Un.MSR UART n Modem Status Register

U0.MSR=0x4000_8018, U1.MSR=0x4000_8118

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								MSR							
																								0x00							
																								R							

7 0	MSR	DCD, NRI, DSR, CTS status

8.3.9 Un.BDR Baud Rate Divisor Value

U0.BDR=0x4000_8020, U1.BDR=0x4000_8120

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																DLM								DLL							
																0x00								0x00							
																RW								RW							

15 8	DLM	DCD, NRI, DSR, CTS status divisor = DLM
7 0	DLL	DCD, NRI, DSR, CTS status divisor = DLL

8.3.10 Un.BFR Baud Rate Fraction Value

U0.BFR=0x4000_8024, U1.BFR=0x4000_8124

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																					FCNT										
																					0x000										
																					RW										

10	FCNT	Baud Rate Fraction Value
0		

8.3.11 Un.IDTR Interval value

U0.IDTR=0x4000_8030, U1.IDTR=0x4000_8130

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													WAITVAL		
																													0x0		
																													RW		

2 0	WAITVAL	Interval Value

8.4 Functional Description

The UART module is compatible with 16450 UART. Additionally the dedicated DMA channels and fractional baud rate compensation logic are provided.

It doesn't have internal FIFO block. So data transfers will establish interactively or using DMA support. The DMA operation is described here. 2 DMA channels provided for each UART module, one channel is for TX transfer and the other one is for RX transfer. Each channel has a 32-bit memory address register and a 16bit transfer counter register. Before DMA operation, DMA memory address register and transfer count register should be configured. For the RX operation, the memory address will be destination memory address and for the TX operation, the memory address will be source memory address.

The transfer counter register will store the number of transfer data. Whenever a single transfer done, the counter will decremented by 1. When the counter reaches zero, the DMA done flag will delivered to UART control block. If the interrupt is enabled, this flag will generate the interrupt.

The UART module provides RTS and CTS for hardware flow control function. RTS can be used to prevent receive data overflow. The UART module hold RTS high, transmitter doesn't send data during RTS is high. Otherwise UART module detect CTS high, it cannot transmit any data. Figure 9.1. describes signal connection and Figure 9.2 describes RTS timing diagram.

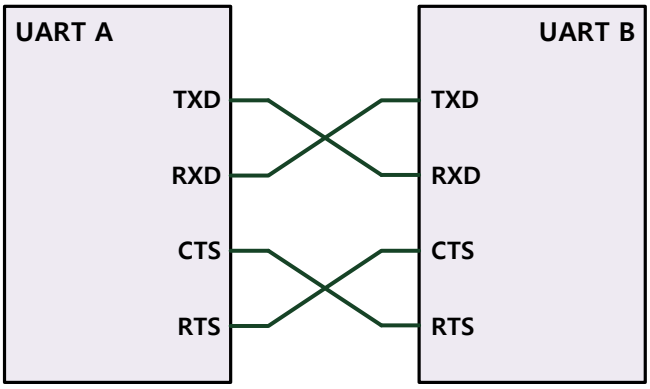


Figure 9.1 UART signal connection

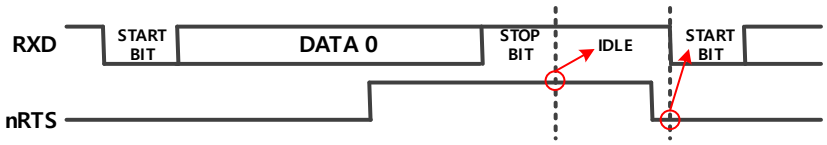


Figure 9.2 RTS Flow Control

CHAPTER 9. PWM

9.1 OVERVIEW

The PWM block is consisted with 2 PWM outputs as a complementary pairs. It can support Dead Time Operation.

- 16-bit up-counter
- Dead Time Generator
- 8-bit prescaler

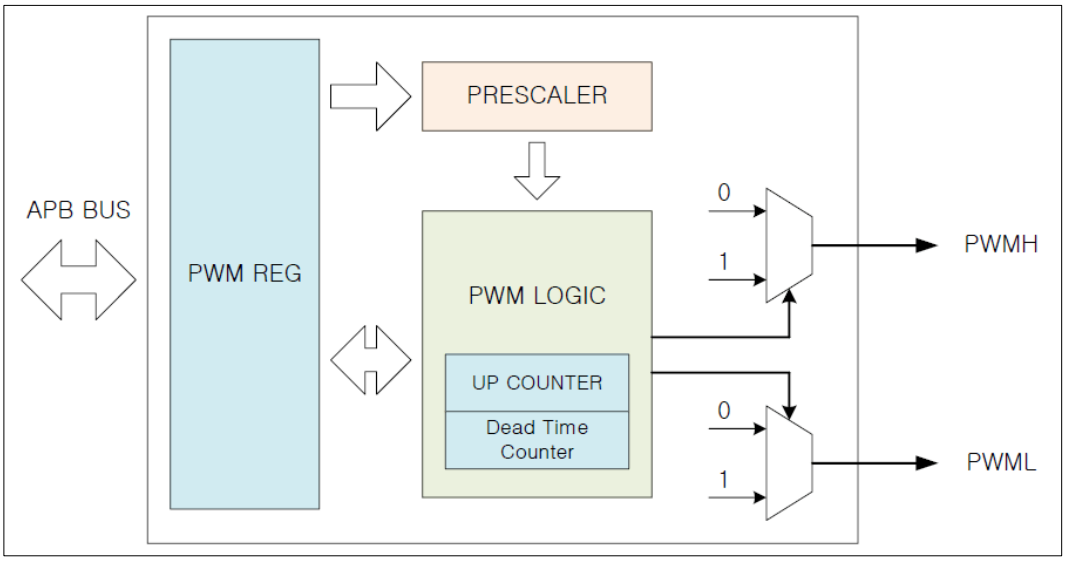


Figure 9.1 Port Control Unit Block Diagram

9.2 PIN DESCRIPTION

Table 9.1 External pin

PIN NAME	TYPE	DESCRIPTION
PWMH	O	PWM output
PWML	O	PWM output

9.3 REGISTERS

The base address of PWM is 0x4000_8200 and register map is described in Table 9.2 and Table 9.3

Table 9.2 Base address of PWM

NAME	BASE ADDRESS
PWM	0x4000_8200

Table 9.3 PWM register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
PWM.CON	0x0000	RW	PWM control register	0x00000000
PWN.CMD	0x0004	RW	PWM command register	0x00000000
PWM.SR	0x0008	RW	PWM status register	0x00000000
PWM.PRS	0x000C	RW	PWM prescale register	0x00000000
PWM.PRD	0x0010	RW	PWM period register	0x00000000
PWM.CNT	0x0014	RO	PWM current counter register	0x0000FFFF
PWM.DCNT	0x0018	RW	PWM down counter register	0x00000000
PWM.DTZ	0x001C	RW	PWM dead time zone counter register	0x00000000
PWM.UCNT	0x0020	RW	PWM up counter register	0x00000000

9.3.1 PWM.CON PWM n Control Register

PWM Control Register is 16-bit register.

PWM module should be configured properly before running. When target purpose is defined, the timer can be configured in the TnCR1 register

PWM.CON=0x4000_8200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SYNCMOD	INTEN	MASK		CLKSEL			PWMEN
																								0	0	00		000			00
																								RW	RW	RW		RW			RW

7	SYNCMODE	PWM synchronous start enable bit with PWM0 start
		0 Synchronous start disabled
		1 Synchronous start enabled
6	INTEN	PWM interrupt enable bit
		0 Interrupt enabled
		1 Interrupt disabled
5 4	MASK	Mask PWM outputs
		00 No mask
		X1 Mask PWMH
		1X Mask PWML
3 1	CLKSEL	PWM clock select Timer operation mode control CLK : prescaled clock
		000 CLK
		001 CLK/2
		010 CLK/4
		011 CLK/8
		100 CLK/16
		101 CLK/32
		110 CLK/32
0	PWMEN	PWM Enable bit
		0 PWM enabled
		1 PWM disabled

9.3.2 PWM.CMD PWM n Command Register

PWM Status Control Register is 8-bit register.

PWM.CMD=0x4000_8204

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														HOLD	START
																														0	0
																														RW	WO

1	HOLD	PWM hold bit	
		0	No action
		1	Holds PWM counter
0	START	PWM Enable bit	
		0	No action
		1	Starts PWM

9.3.3 PWM.SR PWM n Status Register

PWM Status Control Register is 8-bit register.

PWM.SR=0x4000_8208

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															INTFLAG
																															0
																															RC

0	INTFLAG	Interrupt flag bit	
		0	No interrupt occurred Starts PWM
		1	Interrupt occurred when 1 cycle is done

9.3.4 PWM.PRS PWM n Prescaler Register

PWM Prescaler Register is 16-bit register in order to prescale the counter input clock.

PWM.PRS=0x4000_820C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								PRS							
																								0x00							
																								RW							

7	PRS	Pre-scale value of count clock
0		TCLK = PCLK/(PRS+1)

9.3.5 PWM.PRD PWM n Period Counter Register

PWM Period Register A is 16-bit register.

PWM.PRD=0x4000_8210

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																PRD															
																0x0000															
																RW															

15 0	PRD	PWM n Period register Note: PRD > 1

9.3.6 PWM.CNT PWM n Current Counter Register

PWM Current Counter Register is 16-bit register.

PWM.CNT=0x4000_8214

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CNT															
																0x0000															
																RW															

15 0	CNT	PWM n Current Counter register (CNT = 16'hFFFF when PWMEN is low)

9.3.7 PWM.DCNT PWM n Down Counter Register

PWM Down Counter Register is 16-bit register.

PWM.DCNT=0x4000_8218

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																DCNT															
																0x0000															
																RW															

15 0	DCNT	PWM Down Counter register (DCNT > UCNT)

9.3.8 PWM.DTZ PWM n Dead Zone Time Register

PWM n Dead Zone Time Register is 15-bit register.

PWM.DTZ=0x4000_821C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																	DTZ														
																	0x0000														
																	RW														

14 0	DTZ	PWM Dead Time Zone Counter register

9.3.9 PWM.UCNT PWM n UP Counter Register

PWM n UP Counter Register is 16-bit register.

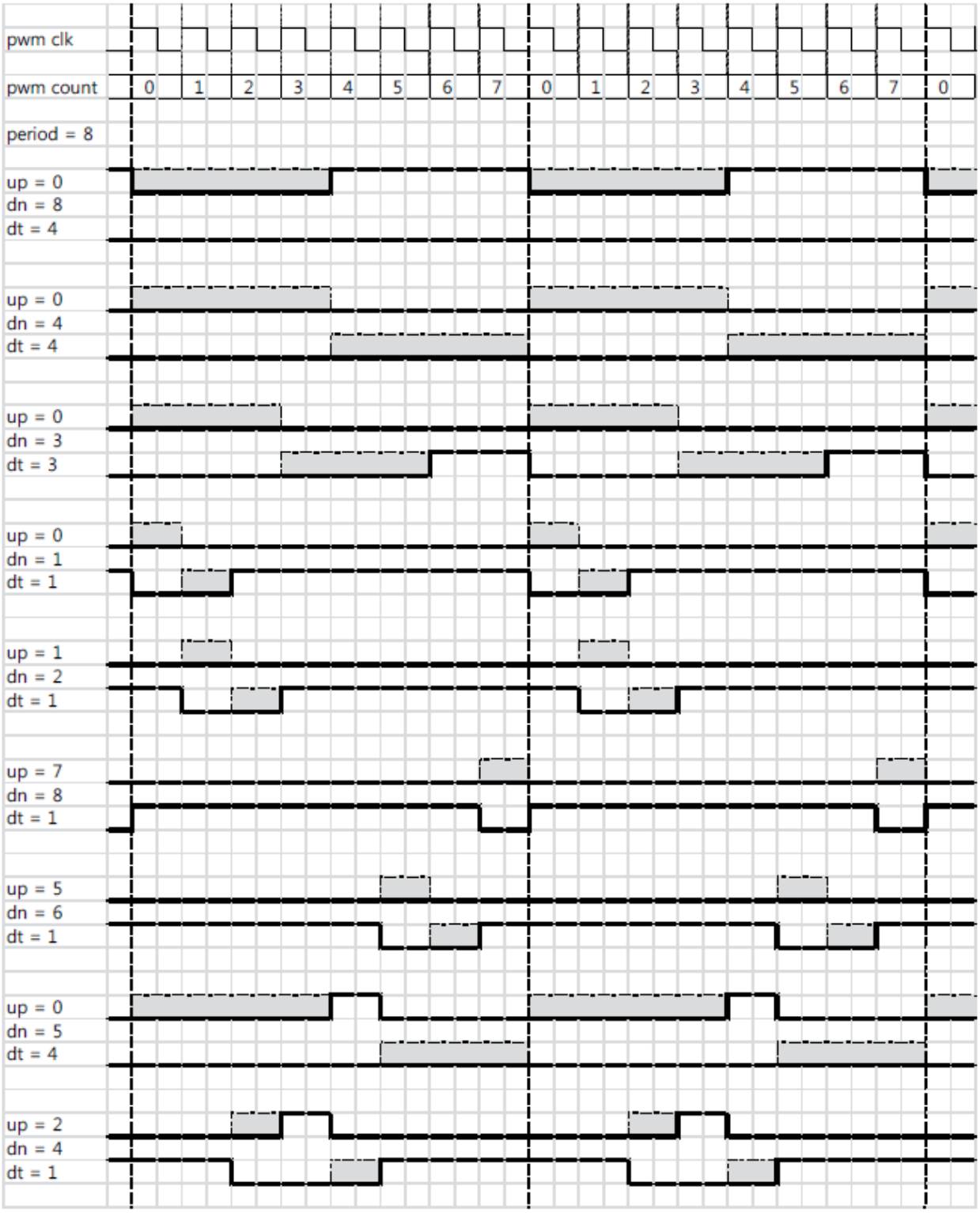
PWM.UCNT=0x4000_8020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																UCNT															
																0x0000															
																RW															

14 0	UCNT	PWM Up Counter register (UCNT < DCNT)

9.4 FUNCTIONAL DESCRIPTION

Example for PWM



CHAPTER 10. DIGITAL DAC

10.1 OVERVIEW

1-Channel DDAC (Digital DAC) modules are provided. 16 FIFOs are supported.

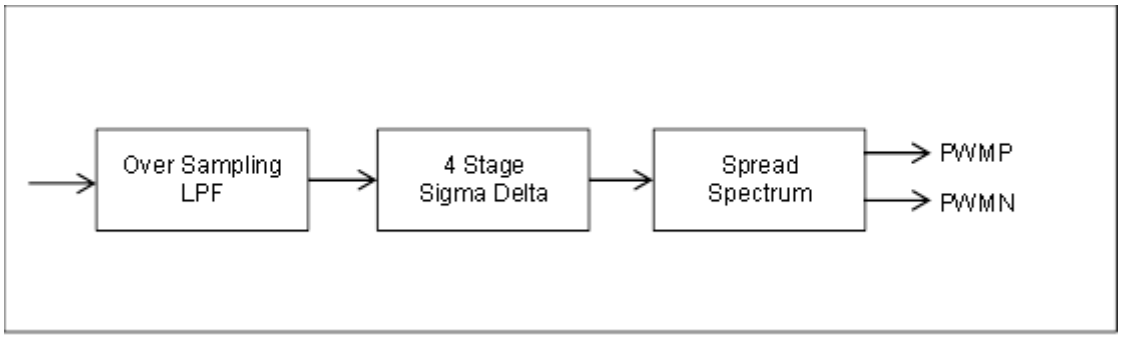


Figure 10.1 Block Diagram

10.2 PIN DESCRIPTION

Table 10.1 External signal

PIN NAME	TYPE	DESCRIPTION
PWMP	O	PWM p
PWMN	O	PWM n

10.3 REGISTERS

The base Address of DDAC is 0x4000_8300 and register map is described in Table 10.2 and Table 10.3.

Table 10.2 Base address of DDAC

NAME	Address
DDAC	0x4000_8300

Table 10.3 DDAC Register Map

Name	Offset	R/W	Description	Reset
DDAC.CON	0x00	R/W	Control Register	0x00000001
DDAC.DATA	0x04	W	Data Register	0x00000000
DDAC.ISR	0x08	R/W	Interrupt Register	0x00000000

10.3.1 DDAC.CON Digital DAC Control Register

DDAC.CTRL=0x4000_8300

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_N					SS_FREQ				SS_MODE		SD_MODE	DIV_2_3	DIV_1_2	OV8X	EN CLK
0x00					0x00				0x00		0	0	0	0	
R/W					R/W				R/W		R/W	R/W	R/W	R/W	R/W

15 11	FIFO_N		Interrupt Generation FIFO samples
10 7	SS_FREQ		N.A.
6 5	SS_MODE		N.A.
4	SD_MODE	1	4 stage sigma delta modulation
		0	2 stage sigma delta modulation
3	DIV_2_3	1	1/2 down sampling
		0	
2	DIV_1_2	1	2/3 down sampling
		0	
1	OV8X	1	8x oversampling
		0	16x oversampling
0	CLK	R	CLK
		W	Enable

$$\text{Sampling Clock} = \text{System Clock} \times \frac{2^{OV8X}}{1024} \times \left(\frac{1}{2}\right)^{DIV\_1\_2} \times \left(\frac{2}{3}\right)^{DIV\_2\_3}$$

10.3.2 DDAC.DATA Digital DAC DATA Register

DDAC.CTRL=0x4000_8304

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
0x0000															
R/W															

15 0	DATA	Data

10.3.3 DDAC.ISR Digital DAC Interrupt Status Register

DDAC.CTRL=0x4000_8304

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															ISR
0x00															0
															R/W

0	ISR	1	# of samples in FIFO is less than FIFO_N
		0	Enable

CHAPTER 11. SPI

11.1 OVERVIEW

One Channel serial Interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. 4 signals will be used for SPI communication – SS, SCK, MOSI, and MISO.

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

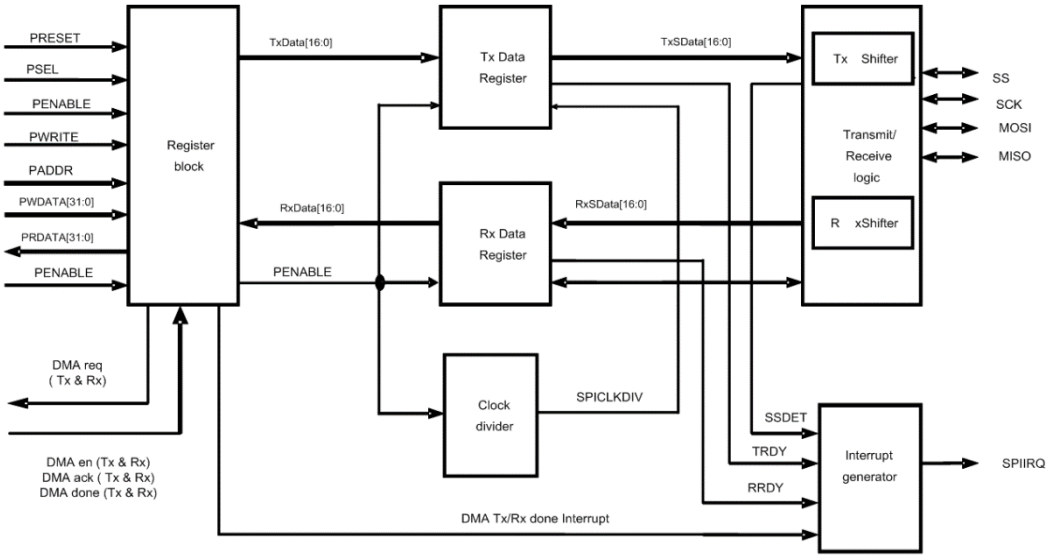


Figure 11.1 Block Diagram

11.2 PIN DESCRIPTION

Table 11.1 External Pins

PIN NAME	TYPE	DESCRIPTION
SS0	I/O	SPI0 Slave select input / output
SCK0	I/O	SPI0 Serial clock input / output
MOSI0	I/O	SPI0 Serial data (Master output, Slave input)
MISO0	I/O	SPI0 Serial data (Master input, Slave output)

11.3 REGISTERS

The base address of SPI0/1 is 0x4000_9000 and 0x4000_9100. The register map is described in Table 11.2 and Table 11.3

Table 11.2 Base Address of SPI

NAME	Base address
SPI0	0x4000_9000
SPI1	0x4000_9100

Table 11.3 SPI Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
SPn.TDR	0x00	W	SPI0 Transmit Data Register	-
SPn.RDR	0x00	R	SPI0 Receive Data Register	0x00000000
SPn.CR	0x04	RW	SPI0 Control Register	0x00001020
SPn.SR	0x08	RW	SPI0 Status Register	0x00000006
SPn.BR	0x0C	RW	SPI0 Baud rate Register	0x0000FFFF
SPn.EN	0x10	RW	SPI0 Enable register	0x00000000
SPn.LR	0x14	RW	SPI0 delay Length Register	0x00010101

11.3.1 SPn.TDR SPI Transmit Data Register

SP0.TDR is a 17-bits read/write register. It contains serial transmit data.

SP0.TDR=0x4000_9000, SP0.TDR=0x4000_9100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																TDR															
0x000																0x00000															
-																RW															

16 0	TDR	Transmit Data Register

11.3.2 SPn.RDR SPI Receive Data Register

SP0.RDR is a 17-bits read/write register. It contains serial receive data.

SP0.RDR=0x4000_9000, SP1.RDR=0x4000_9000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																RDR															
0x000																0x00000															
-																RW															

16 0	RDR	Receive Data Register	

11.3.3 SPn.CR SPI Control Register

SP0.CR is a 20-bits read/write register and can be set to configure SPI operation mode.

SP0.CR=0x4000_9004, SP1.CR=0x4000_9104

31 30 29 28 27 26 25 24	23 22 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		TXBC	RXBC	DTXIE	DRXIE	SSCIE	TXIE	RXIE	SSMOD	SSOUT	LBE	SSMARK	SS0MO	SS0POL			MS	MSBF	CPHA	CPOL	BITSZ	
0x00		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	00	
		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	

20	TXBC	Tx buffer clear bit. 0 No action 1 Clear Tx buffer
19	RXBC	Rx buffer clear bit 0 No action 1 Clear Rx buffer
18	TXDIE	DMA Tx Done Interrupt Enable bit. 0 DMA Tx Done Interrupt is disabled. 1 DMA Tx Done Interrupt is enabled.
17	RXDIE	DMA Rx Done Interrupt Enable bit. 0 DMA Rx Done Interrupt is disabled. 1 DMA Rx Done Interrupt is enabled.
16	SSCIE	SS Edge Change Interrupt Enable bit. 0 nSS interrupt is disabled. 1 nSS interrupt is enabled for both edges (L→H, H→L)
15	TXIE	Transmit Interrupt Enable bit. 0 Transmit Interrupt is disabled. 1 Transmit Interrupt is enabled.
14	RXIE	Receive Interrupt Enable bit. 0 Receive Interrupt is disabled. 1 Receive Interrupt is enabled.
13	SSMOD	SS Auto/Manual output select bit. 0 SS output is not set by SSOUT (SPnCR[12]). - SS signal is in normal operation mode. 1 SS output signal is set by SSOUT.
12	SSOUT	SS output signal select bit. 0 SS output is 'L.' 1 SS output is 'H'.
11	LBE	Loop-back mode select bit in master mode. 0 Loop-back mode is disabled. 1 Loop-back mode is enabled.
10	SSMASK	SS signal masking bit in slave mode. 0 SS signal masking is disabled. - Receive data when SS signal is active. 1 SS signal masking is enabled. - Receive data at SCLK edges. SS signal is ignored.
9	SSMO	SS output signal select bit. 0 SS output signal is disabled. 1 SS output signal is enabled.
8	SSPOL	SS signal Polarity select bit. 0 SS signal is Active-Low. 1 SS signal is Active-High.
7 6		Reserved
5	MS	Master/Slave select bit.

		0	SPI is in Slave mode.
		1	SPI is in Master mode.
4	MSBF	MSB/LSB Transmit select bit.	
		0	LSB is transferred first.
		1	MSB is transferred first.
3	CPHA	SPI Clock Phase bit.	
		0	Sampling of data occurs at odd edges (1,3,5,…,15).
		1	Sampling of data occurs at even edges (2,4,6,…,16).
2	CPOL	SPI Clock Polarity bit.	
		0	Active-high clocks selected.
		1	Active-low clocks selected.
1	BITSZ	Transmit/Receive Data Bits select bit.	
		00	8 bits
		01	9 bits
		10	16 bits
0		11	17 bits

CPOL=0, CPHA=0 : data sampling at rising edge, data changing at falling edge
CPOL=0, CPHA=1 : data sampling at falling edge, data changing at rising edge
CPOL=1, CPHA=0 : data sampling at falling edge, data changing at rising edge
CPOL=1, CPHA=1 : data sampling at rising edge, data changing at falling edge

11.3.4 SPn.SR SPI Status Register

SP0.SR is a 10-bits read/write register. It contains the status of SPI interface.

SP0.SR=0x4000_9008, SP1.SR=0x4000_9108

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						TXDMAF	RXDMAF		SSDET	SSON	OVRF	UDRF	TXIDLE	TRDY	RRDY
						0	0	0	0	0	0	0	1	1	0
						RC1	RC1		RC1	RC1	RC1	RC1	R	R	R

9	TXDMAF	DMA Transmit Operation Complete flag. (DMA to SPI)
		0 DMA Transmit Op is working or is disabled.
		1 DMA Transmit Op is done.
8	RXDMAF	DMA Receive Operation Complete flag. (SPI to DMA)
		0 DMA Receive Operation is working or is disabled.
		1 DMA Transmit Op is done.
7		Reserved
6	SSDET	The rising or falling edge of SS signal Detect flag.
		0 SS edge is not detected.
		1 SS edge is detected.
		- The bit is cleared when it is written as “0”.
5	SSON	SS signal Status flag.
		0 SS signal is inactive.
		1 SS signal is active.
4	OVRF	Receive Overrun Error flag.
		0 Receive Overrun error is not detected.
		1 Receive Overrun error is detected.
		- This bit is cleared by writing or reading SPnRDR.
3	UDRF	Transmit Underrun Error flag.
		0 Transmit Underrun is not occurred.
		1 Transmit Underrun is occurred.
		- This bit is cleared by writing or reading SPnTDR.
2	TXIDLE	Transmit/Receive Operation flag.
		0 SPI is transmitting data
		1 SPI is in IDLE state.
1	TRDY	Transmit buffer Empty flag.
		0 Transmit buffer is busy.
		1 Transmit buffer is ready.
		- This bit is cleared by writing data to SPnTDR.
0	RRDY	Receive buffer Ready flag.
		0 Receive buffer has no data.
		1 Receive buffer has data.
		- This bit is cleared by writing data to SPnRDR.

11.3.5 SPn.BR SPI Baud Rate Register

SP0.BR is an16-bits read/write register. Baud rate can be set by writing the register.

SP0.BR=0x4000_900C, SP1.BR=0x4000_910C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR															
0x00FF															
RW															

15	BR	Baud rate setting bits Baud Rate = PCLK / (BR + 1)
0		(BR must be bigger than “0”, BR >= 2)

SPI Baud Rate	SPn.BR
8MHz	1
4MHz	3
2MHz	7
1MHz	15
500KHz	31
250KHz	63
125KHz	127

11.3.6 SPn.EN SPI Enable register

SP0.EN is a bit read/write register. It contains SPI enable bit.

SP0.EN=0x4000_9010, SP1.EN=0x4000_9110

7	6	5	4	3	2	1	0
Reserved							ENABLE
0x0							0
							RW

0	ENABLE	SPI Enable bit	
		0	SPI is disabled. - SPnSR is initialized by writing “0” to this bit but other registers aren’t initialized.
		1	SPI is enabled. - When this bit is written as “1”, the dummy data of transmit buffer will be shifted. To prevent this, write data to SPTDR before this bit is active.

11.3.7 SPn.LR SPI Delay Length Register

SP0.LR is a 24-bits read/write register. It contains start, burst, and stop length value.

SP0.LR=0x4000_9014, SP1.LR=0x4000_9114

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	SPL	BTL	STL
0x00	0x01	0x01	0x01
	RW	RW	RW

23	SPL	StoPLength value
16		0x01 ~ 0xFF : 1 ~ 255 SCLKs. (SPL ≥ 1)
15	BTL	BursTLength value
8		0x01 ~ 0xFF : 1 ~ 255 SCLKs. (BTL ≥ 1)
7	STL	STart Length value
0		0x01 ~ 0xFF : 1 ~ 255 SCLKs. (STL ≥ 1)

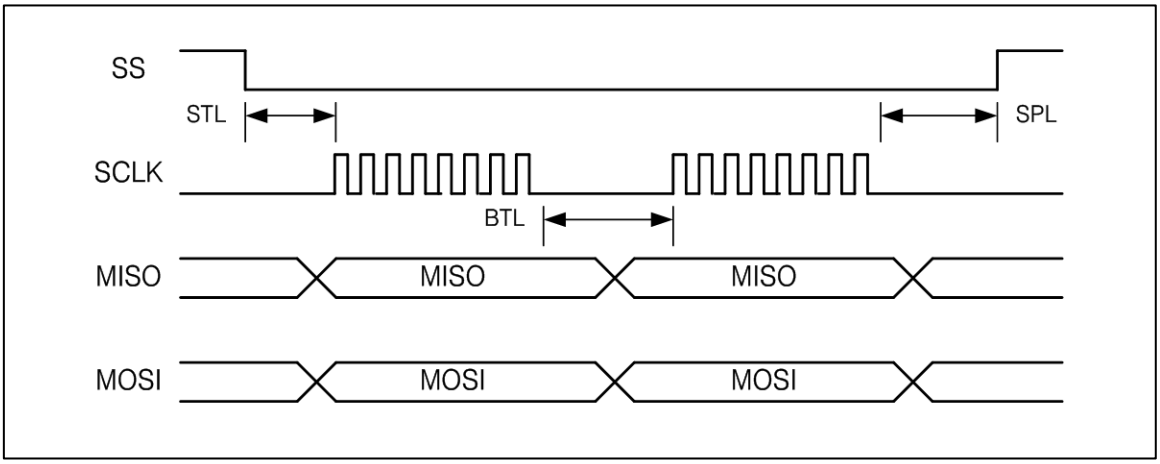


Figure 11.2 SPI wave form (STL, BTL and SPL)

11.4 FUNCTIONAL DESCRIPTION

SPI Transmit block and Receive block share Clock Gen Block but they are independent each other. Transmit block and Receive block have double buffers and SPI is available for back to back transfer operation.

11.4.1 SPI timing

The SPI has four modes of operation. These modes essentially control the way data is clocked in or out of an SPI device. The configuration is done by two bits in the SPI control register (SPnCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock. The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats. To ensure a proper communication between master and slave both devices have to run in the same mode. This can require a reconfiguration of the master to match the requirements of different peripheral slaves.
The clock polarity has no significant effect on the transfer format. Switching this bit causes the clock signal to be inverted (active high becomes active low and idle low becomes idle high). The settings of the clock phase, however, selects one of the two different transfer timings, which are described closer in the next two chapters. Since the MOSI and MISO lines of the master and the slave are directly connected to each other, the diagrams show the timing of both device, master and slave. The nSS line is the slave select input of the slave. The nSS pin of the master is not shown in the diagrams. It has to be inactive by a high level on this pin (if configured as input pin) or by configuring it as an output pin.
The timing of a SPI transfer where CPHA is zero is shown in Figure 10.3 and 10.4. Two wave forms are shown for the SCK signal -one for CPOL equals zero and another for CPOL equals one.
When the SPI is configured as a slave, the transmission starts with the falling edge of the /SS line. This activates the SPI of the slave and the MSB of the byte stored in its data register (SPnTDR) is output on the MISO line. The actual transfer is started by a software write to the SPnTDR of the master. This causes the clock signal to be generated. In cases where the CPHA equals zero, the SCLK signal remains zero for the first half of the first SCLK cycle. This ensures that the data is stable on the input lines of both the master and the slave. The data on the input lines is read with the edge of the SCLK line from its inactive to its active. The edge of the SCLK line from its active to its inactive state (falling edge if CPOL equals zero and rising edge if CPOL equals one) causes the data to be shifted one bit further so that the next bit is output on the MOSI and MISO lines.

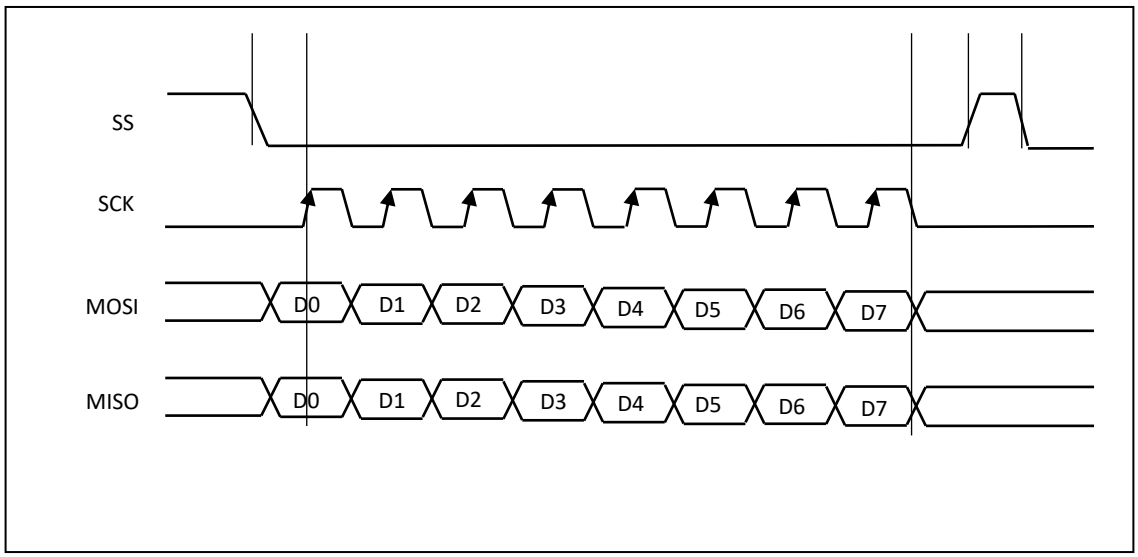


Figure 11.3 SPI Transfer Timing 1/4 (CPHA=0, CPOL=0, MSBF=0)

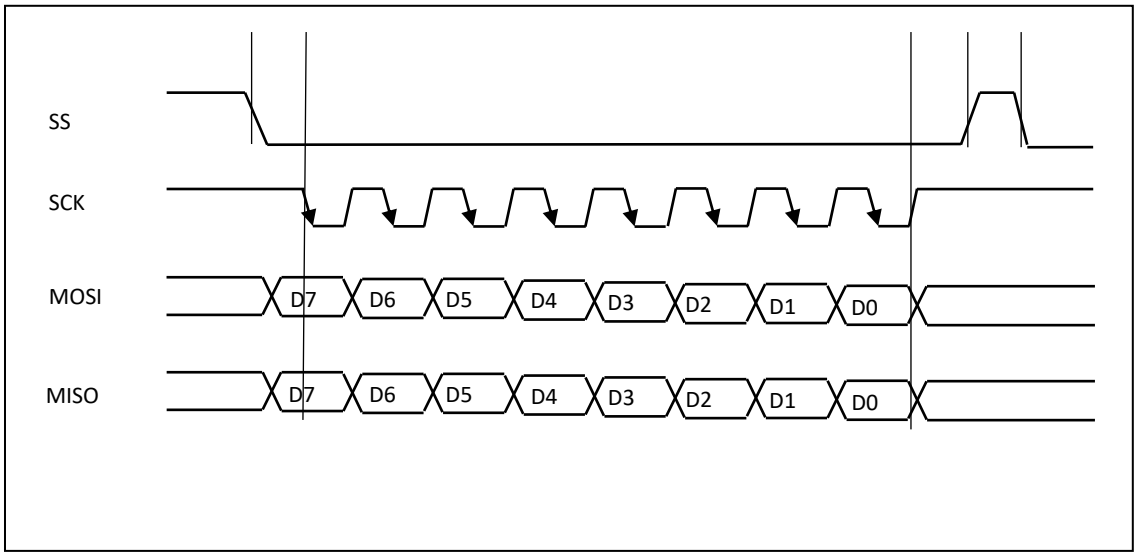


Figure 11.4 SPI Transfer Timing 2/4 (CPHA=0, CPOL=1, MSBF=1)

The timing of a SPI transfer where CPHA is one is shown in Figure 10.5 and 10.6.Two wave forms are shown for the SCLK signal -one for CPOL equals zero and another for CPOL equals one.

Like in the previous cases the falling edge of the nSS lines selects and activates the slave. Compared to the previous cases, where CPHA equals zero, the transmission is not started and the MSB is not output by the slave at this stage. The actual transfer is started by a software write to the SPnTDR of the master what causes the clock signal to be generated. The first edge of the SCLK signal from its inactive to its active state (rising edge if CPOL equals zero and falling edge if CPOL equals one) causes both the master and the slave to output the MSB of the byte in the SPnTDR.

As shown in Figure 10.3 and 10.4, there is no delay of half a SCLK-cycle. The SCLK line changes its level immediately at the beginning of the first SCLK-cycle. The data on the input lines is read with the edge of the SCLK line from its active to its inactive state (falling edge if CPOL equals zero and rising edge if CPOL equals one). After eight clock pulses the transmission is completed.

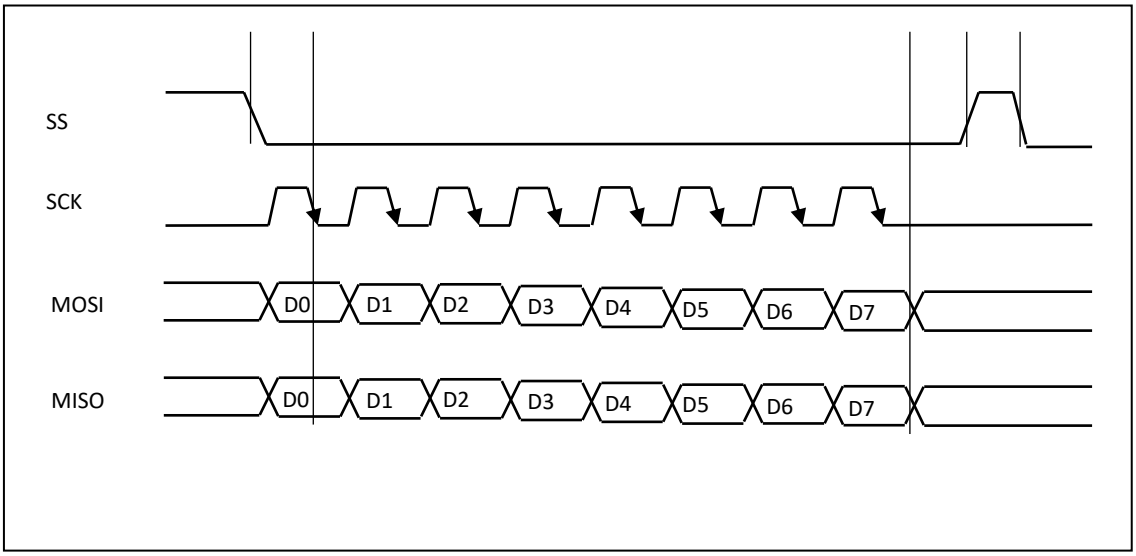


Figure 11.5 SPI Transfer Timing 3/4 (CPHA=1, CPOL=0, MSBF=0)

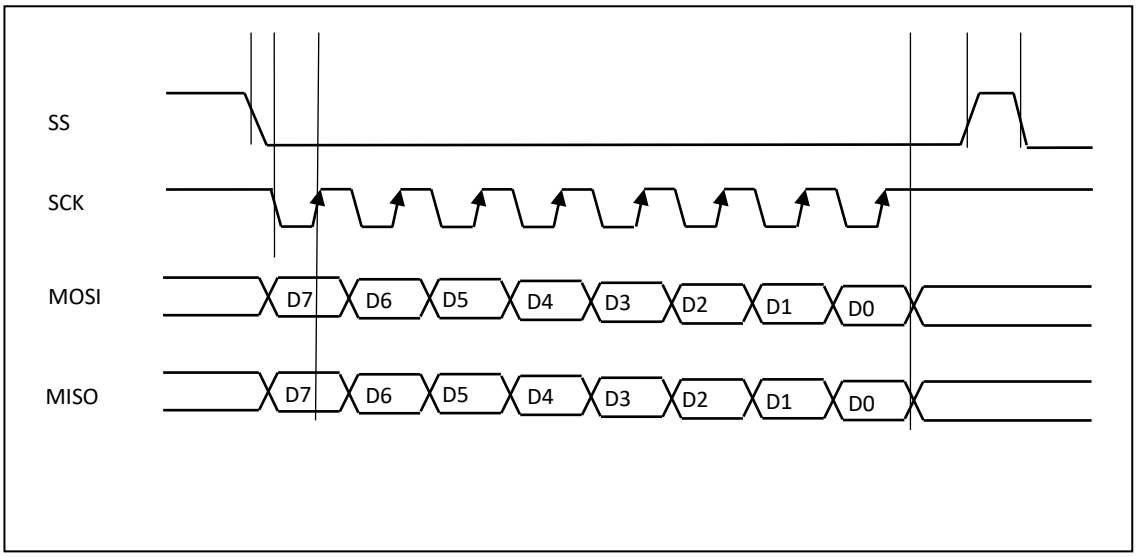


Figure 11.6 SPI transfer timing 4/4 (CPHA=1, CPOL=1, MSBF=1)

11.4.2 DMA Handshake

SPI supports DMA handshaking operation. In order to operate DMA handshake, DMA registers should be set first. (See Chapter 6. DMA Controller). As Transmitter and Receiver are independent each other, SPI can operate the two channels at the same time.

After DMA channel for receiver is enabled and receive buffer is filled, SPI sends Rx request to DMA to empty the buffer and waits ACK signal from DMA. If Receive buffer is filled again after ACK signal, SPI sends Rx request. If DMA Rx DONE becomes high, SP0.SP.RXDMAF (SP0.SR[8]) goes “1” and an interrupt is serviced when SP0.CR.RXDIE (SP0.CR[17]) is set.

Likewise, if transmit buffer is empty after DMA channel for transmitter is enabled, SPI sends Tx request to DMA to fill the buffer and waits ACK signal from DMA. If transmit buffer is empty again after ACK signal, SPI sends Tx request. If DMA Tx DONE becomes high, SP0.SR.TXDMAF(SP0.SR[9]) goes “1” and an interrupt is serviced when SP0.CR.TXDIE(SP0.CR[18]) is set. Slave transmitter sends dummy data at the first transfer (8~17 SCLKs) in DMA handshake mode.

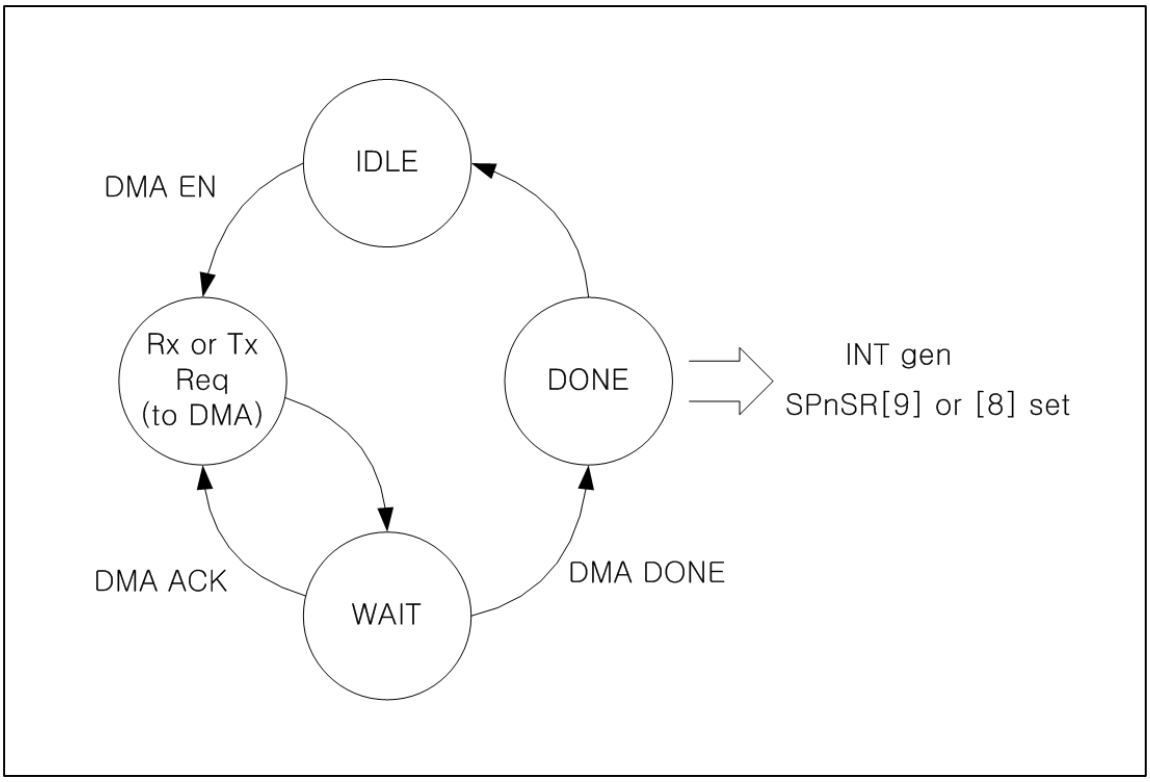


Figure 11.7 DMA Handshake Flow chart

CHAPTER 12. I2C

12.1 OVERVIEW

I²C(Inter-Integrated Circuit) bus serves as an interface between the microcontroller and the serial I²C bus. It provides two wires, serial bus interface to a large number of popular devices and allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

- Master and slave operation
- Programmable communication speed
- Multi-master bus configuration
- 7-bit addressing mode
- Standard data rate of 100/400 kbps
- STOP signal generation and detection
- START signal generation
- ACK bit generation and detection

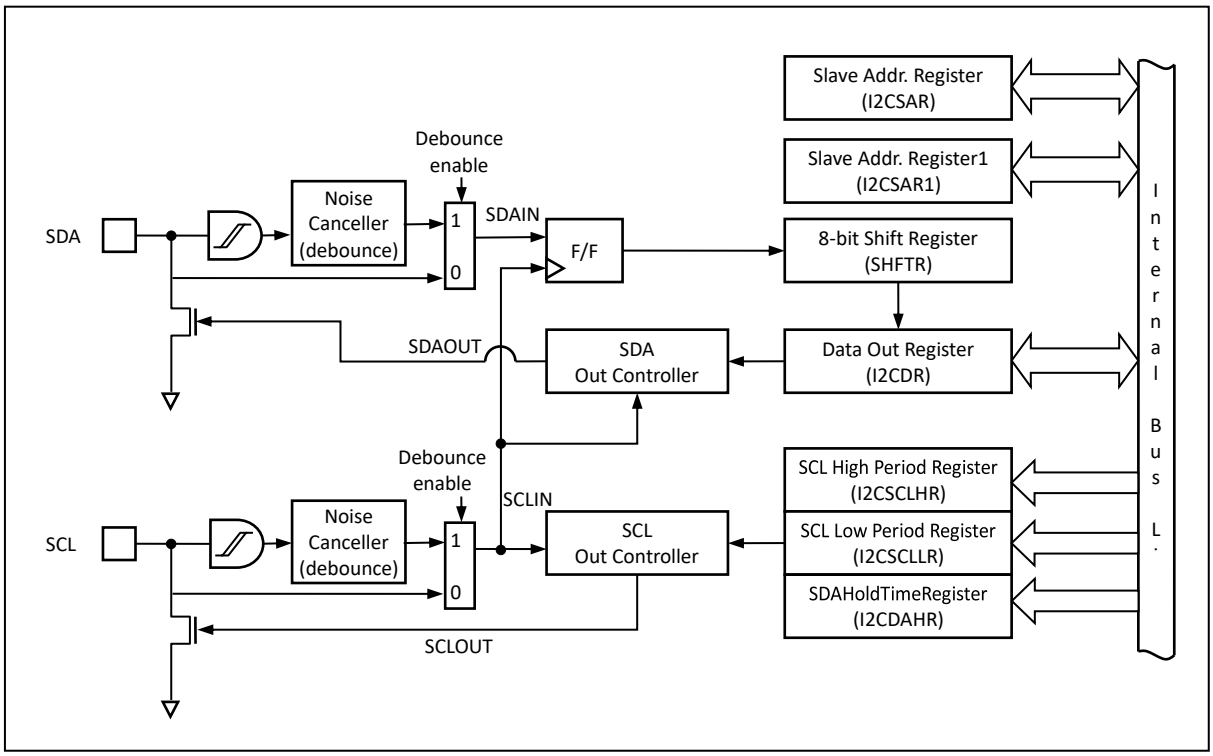


Figure 12.1.I²C Block diagram

12.2 PIN DESCRIPTION

Table 12.1. I²C interface external pins

PIN NAME	TYPE	DESCRIPTION
SCL0	I/O	I²C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I²C channel 0 Serial data bus line (open-drain)

12.3 REGISTERS

The base address of I2C0/1 is 0x4000_A000 and 0x4000_A100. The register map is described in T able 12.2 and Table 12.3

T able 12.2 I2C interface base address

NAME	BASE ADDRESS
I2C0	0x4000_A000
I2C1	0x4000_A100

Table 12.3 I2C register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
IC*n*.DR	0x00	RW	I^2C0 Data Register	0x000000FF
IC*n*.SR	0x08	R, RW	I^2C0 Status Register	0x00000000
IC*n*.SAR	0x0C	RW	I^2C0 Slave Address Register	0x00000000
IC*n*.CR	0x14	RW	I^2C0 Control Register	0x00000000
IC*n*.SCLL	0x18	RW	I^2C0 SCL LOW duration Register	0x0000FFFF
IC*n*.SCLH	0x1C	RW	I^2C0 SCL HIGH duration Register	0x0000FFFF
IC*n*.SDH	0x20	RW	I^2C0 SDA Hold Register	0x00007FFF

12.3.1 ICn.DR I²C Data Register

ICn.DR is an 8-bits read/write register. It contains a byte of serial data to be transmitted or a byte which has just been received.

IC0.DR=0x4000_A000, IC1.DR=0x4000_A100

7	6	5	4	3	2	1	0
ICDR							
0xFF							
RW							

7 0	ICDR	The most recently received data or data to be transmitted.

12.3.2 ICn.SR I²C Status Register

ICn.SR is an 8-bit read/write register. It contains the status of I²C bus interface. Writing to the register clears the status bits except for IMASTER.

IC0.SR=0x4000_A008, IC1.SR=0x4000_A108

7	6	5	4	3	2	1	0
GCALL	TEND	STOP	SSEL	MLOST	BUSY	TMOD	RXACK
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

7	GCALL	General call flag
	0	General call is not detected.
	1	General call detected or slave address (ID byte) was sent.
6	TEND	1 Byte transmission complete flag
	0	The transmission is working or not completed.
	1	The transmission is completed.
5	STOP	STOP flag
	0	STOP is not detected.
	1	STOP is detected.
4	SSEL	Slave flag
	0	Slave is not selected.
	1	Slave is selected.
3	MLOST	Mastership lost flag
	0	Mastership is not lost.
	1	Mastership is lost.
2	BUSY	BUSY flag
	0	I²C bus is in IDLE state.
	1	I²C bus is busy.
1	TMODE	Transmitter/Receiver mode flag
	0	Receiver mode.
	1	Transmitter mode.
0	RXACK	Rx ACK flag
	0	Rx ACK is not received.
	1	Rx ACK is received.

12.3.3 ICn.SAR I²C Slave Address Register

ICn.SAR is an 8-bits read/write register. It shows the address in slave mode.

IC0.SAR=0x4000_A00C, IC1.SAR=0x4000_A10C

7	6	5	4	3	2	1	0
SVAD							GCEN
0x00							0
RW							RW

7 1	SVAD	7-bit Slave Address
0	GCEN	General call enable bit
	0	General call is disabled.
	1	General call is enabled.

12.3.4 ICn.CR I²C Control Register

ICn.CR is an 8-bits read/write register. The register can be set to configure I2C operation mode and simultaneously allowed for I2C transactions to be kicked off.

IC0.CR=0x4000_A014, IC1.CR=0x4000_A114

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						INTDEL		IIF		SOFTRST	INTEN	ACKEN		STOP	START
0	0	0	0	0	0	00		0	0	0	0	0	0	0	0
						RW		R		RW	RW	RW		RW	RW

9 8	INTDEL	Interval delay value between address and data transfer (or DATA and DATA)
		0 1 * ICnSCLL
		1 2 * ICnSCLL
		2 4 * ICnSCLL
		3 8 * ICnSCLL
7	IIF	Interrupt status bit
		0 Interrupt is inactive
		1 Interrupt is active
5	SOFTRST	Soft Reset enable bit.
		0 Soft Reset is disabled.
		1 Soft Reset is enabled.
4	INTEN	Interrupt enabled bit.
		0 Interrupt is disabled.
		1 Interrupt is enabled.
3	ACKEN	ACK enable bit in Receiver mode.
		0 ACK is not sent after receiving data.
		1 ACK is sent after receiving data.
1	STOP	Stop enable bit. When this bit is set as “1” in transmitter mode, next transmission will be stopped even though ACK signal has been received.
		0 Stop is disabled.
		1 Stop is enabled. When this bit is set, transmission will be stopped.
0	START	Transmission start bit in master mode.
		0 Waits in slave mode.
		1 Starts transmission in master mode.

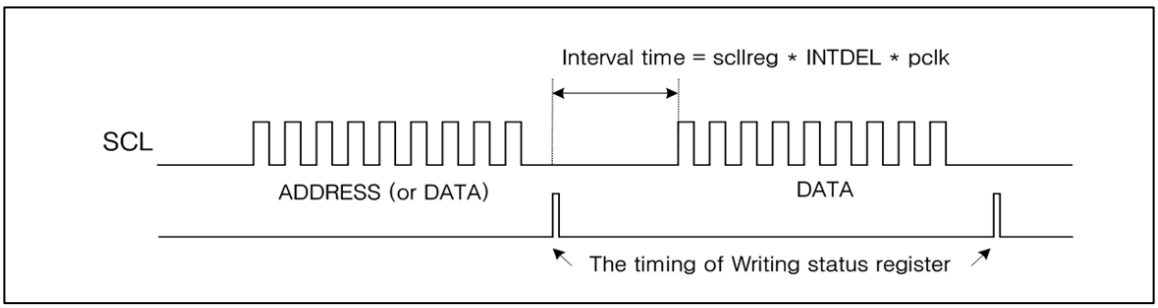


Figure 12.2 INTDEL in Master mode

12.3.5 ICn.SCLL I²C SCL LOW duration Register

ICnSCLL is a 16-bit read/write register. SCL LOW time can be set by writing this register in master mode.

IC0.SDLL=0x4000_A018, IC1.SDLL=0x4000_A118

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLL															
0xFFFF															
RW															

15	SCLL	SCL LOW duration value. SCLL = (PCLK * SCLL[15:0]) + 2*PCLKs
0		Default value is 0xFFFF.

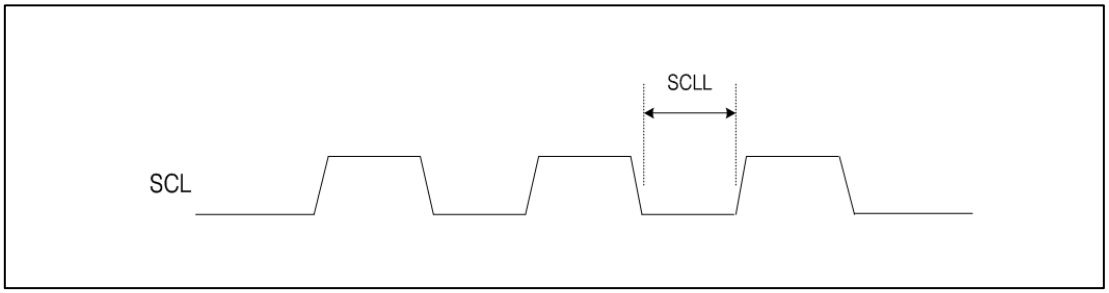


Figure 12.3 SCL LOW Timing

12.3.6 ICn.SCLH I²C SCL HIGH duration Register

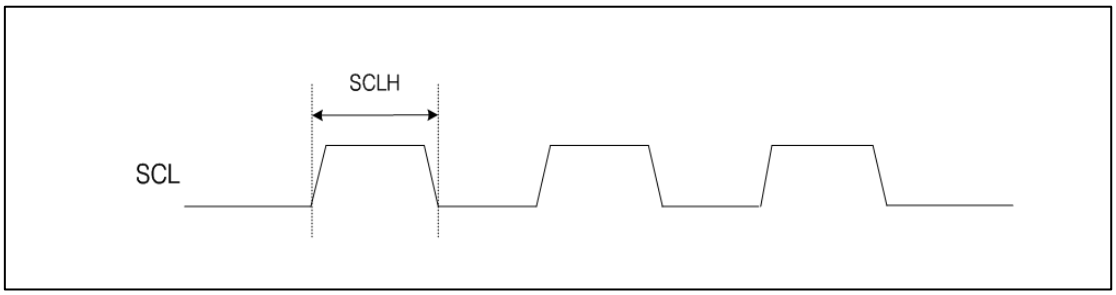
ICnSCLH is a 16-bit read/write register. SCL HIGH time will be set by writing this register in master mode.

IC0.SDLH=0x4000_A01C, IC1.SDLH=0x4000_A11C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLH															
0xFFFF															
RW															

15	SCLH	SCL HIGH duration value. SCLH = (PCLK * SCLH[15:0]) + 3 PCLKs
0		Default value is 0xFFFF.

Figure 12.4 SCL HIGH Timing



12.3.7 ICn.SDH SDA Hold Register

ICnSDH is a 15-bit read/write register. SDA HOLD time will be set by writing this register in master mode.

IC0.SDH=0x4000_A020, IC1.SDH=0x4000_A120

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SDH														
0x3FFF															
RW															

14	SDH	SDA HOLD time setting value. SDH = (PCLK * SDH[14:0]) + 4 PCLKs
0		Default value is 0x3FFF.

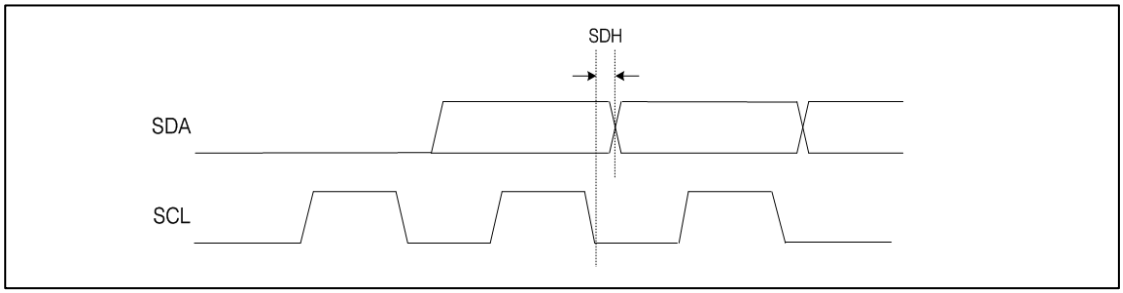


Figure 12.5 SDA HOLD Timing

12.4 FUNTIONAL DESCRIPTION

12.4.1 I²C bit transfer

The data on the SDA line must be stable during the “H” period of the clock. The “H” or “L” state of the data line can only change when the clock signal on the SCL line is “L” (see Fig 13.6).

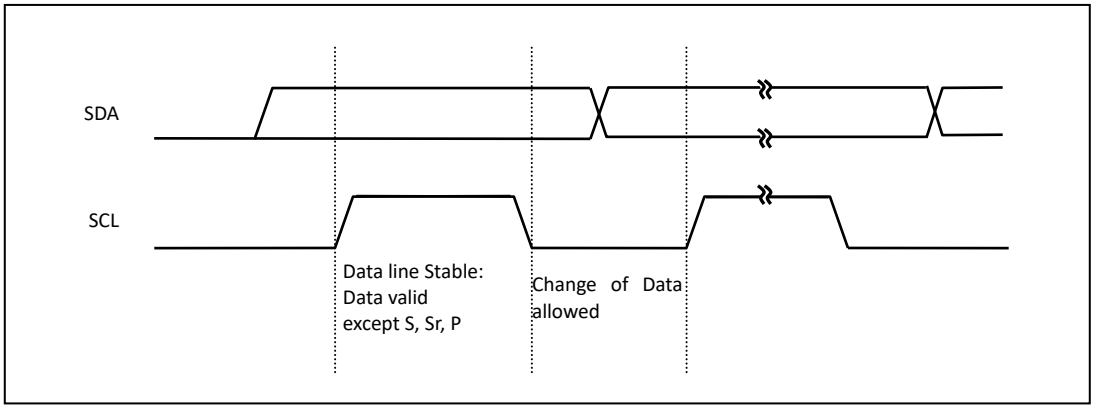


Figure 12.6 I²C Bus bit transfer

12.4.2 START/Repeated START/STOP

Within the procedure of the I²C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions (see Figure 13.7).

i) An “H” to “L” transition on the SDA line while SCL is “H” is one such unique case. This situation indicates a START condition.

ii) A “L” to “H” transition on the SDA line while SCL is “H” defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus is busy if a repeated START(Sr) is generated instead of a STOP condition. In this respect, the START(S) and repeated START(Sr) conditions are functionally identical. For the remainder of this document therefore, the S symbol will be used as a generic term to represent both the START and repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

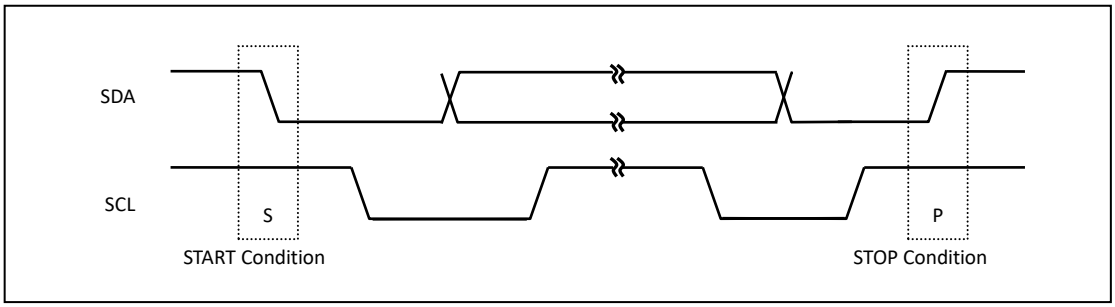


Figure 12.7 START and STOP condition

12.4.3 Data Transfer

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see Figure 13.8). If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL "L" to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

A message which starts with such an address can be terminated by generation of a STOP conditions, even during the transmission of a byte. In this case, no acknowledge is generated.

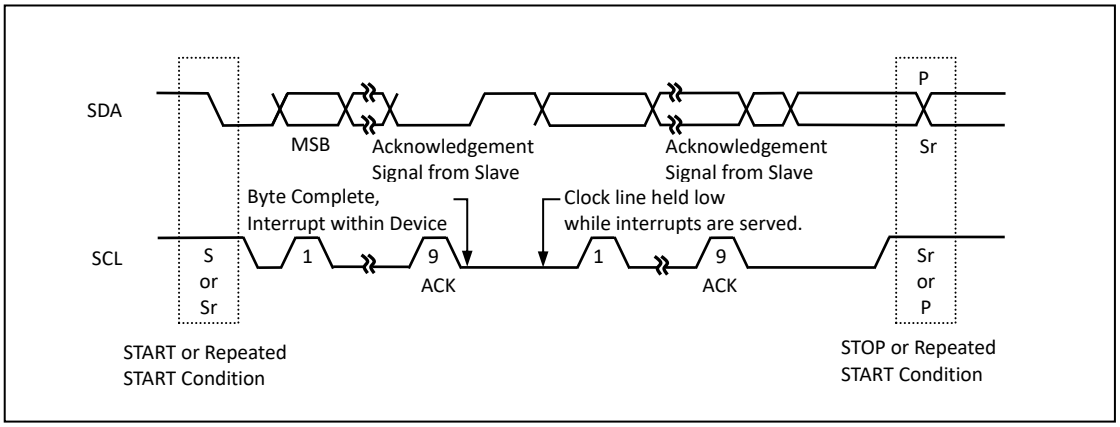


Figure 12.8 I²C Bus data transfer

12.4.4 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

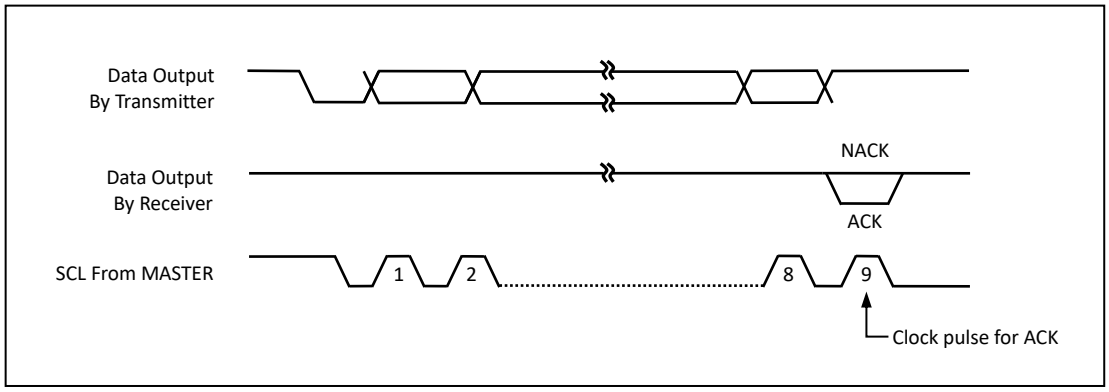
The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable “L” during the “H” period of this clock pulse (see Figure 13.9). Of course, set-up and hold times must also be taken into account.

When a slave doesn’t acknowledge the slave address (for example, it’s unable to receive or transmit because it’s performing some real-time function), the data line must be left “H” by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a slave-receiver does acknowledge the slave address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not-acknowledge on the first byte to follow. The slave leaves the data line “H” and the master generates a STOP or a repeated START condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

Figure 12.9 I²C bus acknowledge



12.4.5 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the “H” period of the clock. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that an “H” to “L” transition on the SCL line will cause the devices concerned to start counting off their “L” period and, once a device clock has gone “L”, it will hold the SCL line in that state until the clock “H” state is reached (see Figure 13.10). However, the “L” to “H” transition of this clock may not change the state of the SCL line if another clock is still within its “L” by the device with the longest “L” period. Devices with shorter “L” periods enter an “H” wait-state during this time.

When all devices concerned have counted off their “L” period, the clock line will be released and go “H”. There will then be no difference between the device clocks and the state of the SCL line, and the devices will start counting their “H” periods. The first device to complete its “H” period will again pull the SCL line “L”.

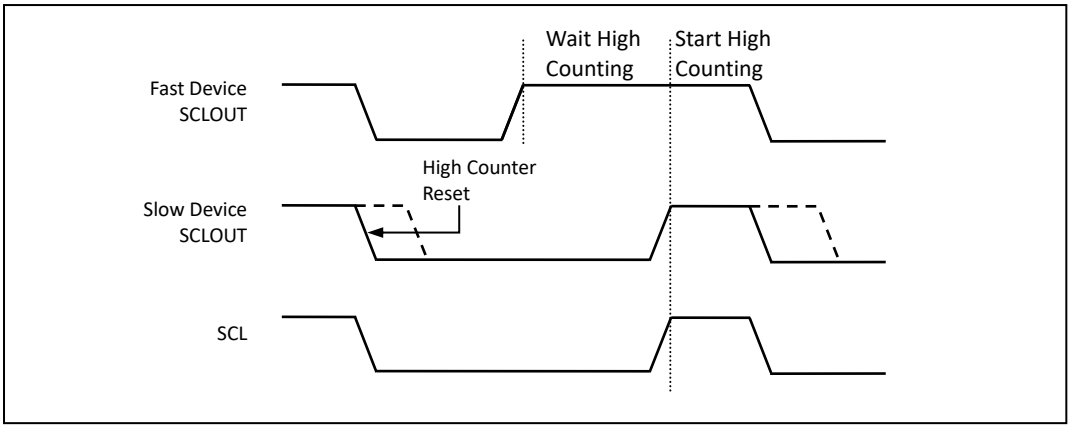


Figure 12.10 Clock synchronization during the arbitration procedure

12.4.6 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the “H” level, in such a way that the master which transmits “H” level, while another master is transmitting “L” level will switch off its DATA output stage because the level on the bus doesn’t correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits. If the masters are each trying to address the same device, arbitration continues with comparison of the data-bits if they are master-transmitter or acknowledge-bits if they are master-receiver. Because address and data information on the I^2C-bus is determined by the winning master, no information is lost during the arbitration process.

A master that loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it’s possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave mode.

Figure 13.11 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating Device1 Dataout and the actual level on the SDA line, its data output is switched off, which means that a “H” output level is then connected to the bus. This will not affect the data transfer initiated by the winning master.

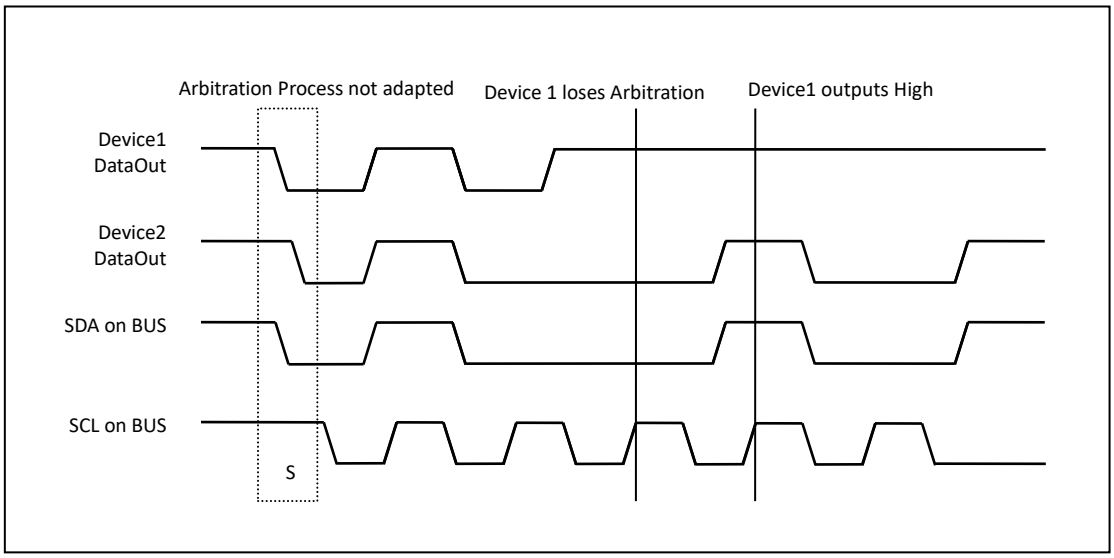


Figure 12.11 Arbitration procedure between two masters

12.5 I²C OPERATION

I²C supports interrupt operation. Once interrupt is serviced, IIF(ICnSR[10]) flag is set. ICnSR shows I²C-bus status information and SCL line stays “L” before the register is written as a certain value. The status register can be cleared by writing

12.5.1 Master Transmitter

It shows the flow of transmitter in master mode (see Figure 13.12).

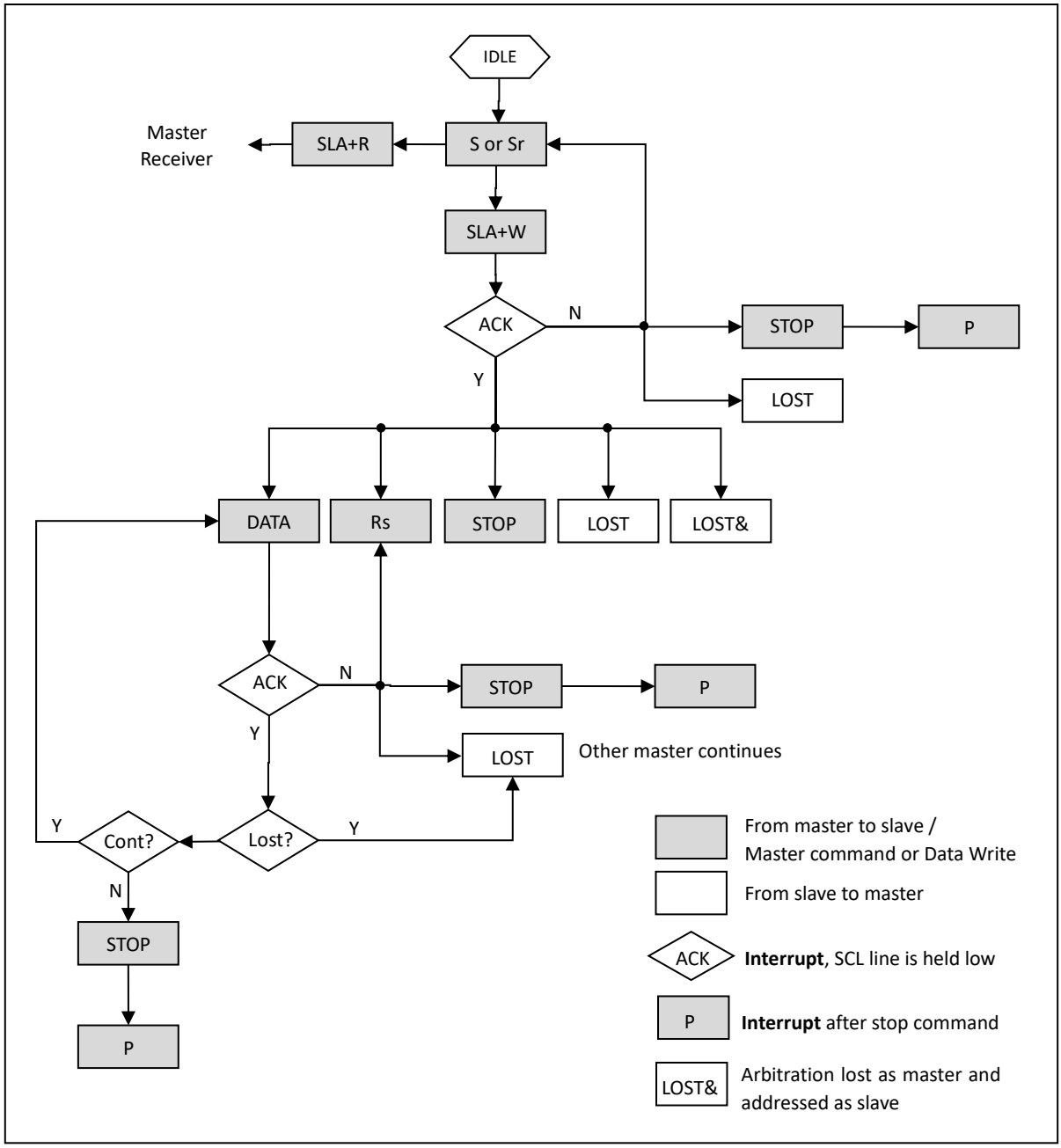


Figure 12.12 Transmitter Flowchart in Master mode

12.5.2 Master Receiver

It shows the flow of receiver in master mode (see Figure 13.13).

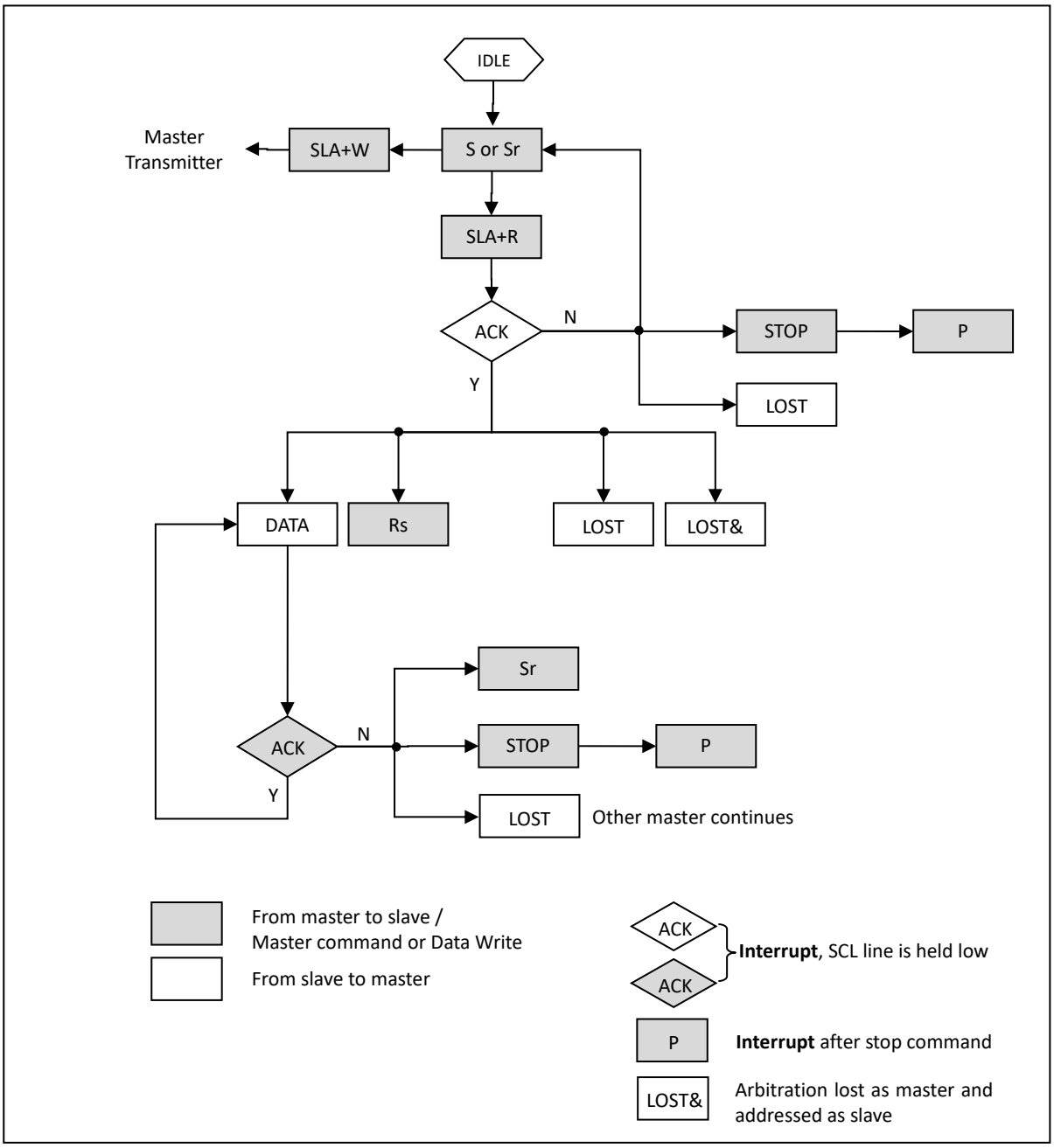
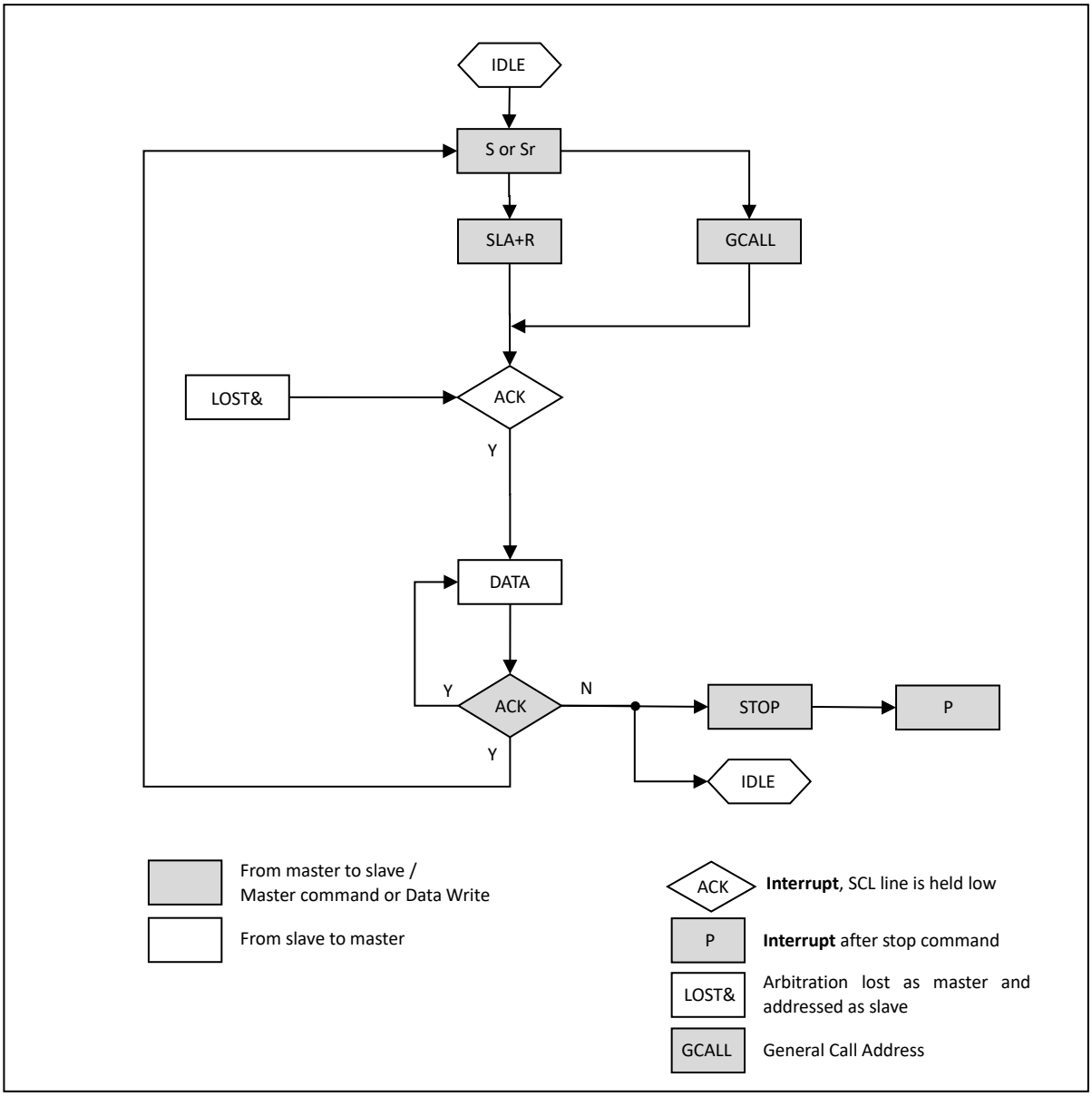


Figure 12.13 Receiver Flowchart in Master mode

12.5.3 Slave Transmitter

It shows the flow of transmitter in slave mode (see Figure 13.14).

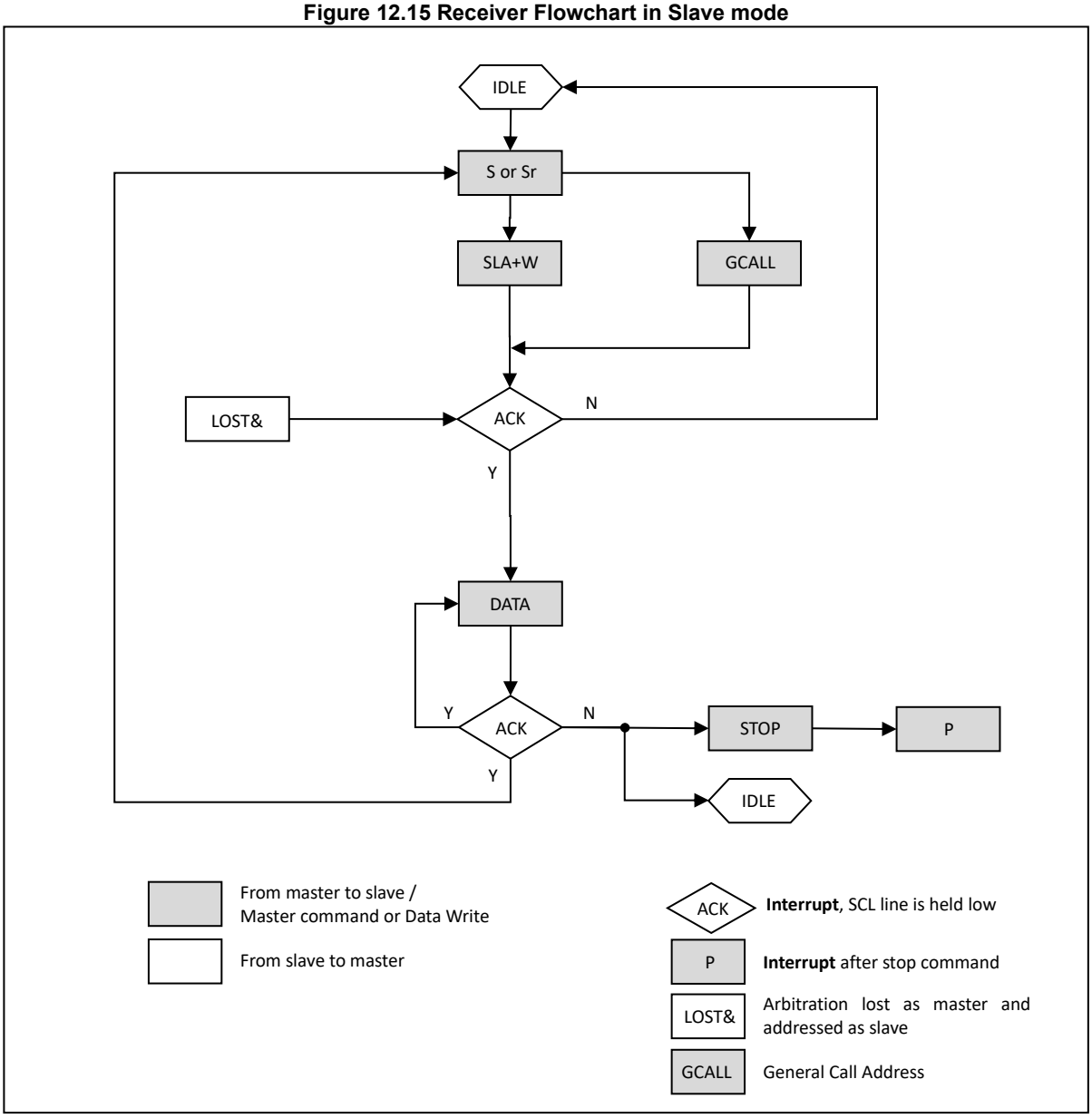
Figure 12.14 Transmitter Flowchart in Slave mode



12.5.4 Slave Receiver

It shows the flow of receiver in slave mode (see Figure 13.15).

Figure 12.15 Receiver Flowchart in Slave mode



CHAPTER 13. ADC Interface

13.1 OVERVIEW

The ADC I/F can configure ADC analog block and support programmable sample rate and 4 operation mode of Single/Continuous /Burst/All channel mode.

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13.2 REGISTERS

The base address of ADC IP is 0x4000_B000 and register map is described in Table 13.1 and Table 13.2

Table 13.1 Base address of ADC

NAME	BASE ADDRESS
ADC	0x4000_B000

Table 13.2 ADC IP register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
ADC.CTRL	0x00	RW	ADC Control Register	0x00000000
ADC.CFG	0x04	RW	ADC Configuration Register	0x00000000
ADC.BST_CTRL	0x08	RW	ADC BUSRT Mode Control Register	0x00000000
ADC.TRIG_CTRL	0x0C	RW	ADC TRIGGER Mode Control Register	0x00000000
ADC.DMA_CTRL	0x20	RW	DMA Control Register	0x00000000
ADC.DATAOUT0	0x24	RO	Data Output Register	-
ADC.DATAOUT1	0x28	RO	Data Output Register	-
ADC.DATA_FIFO_STATUS	0x2C	RO	Data FIFO Status Register	0x00000000
ADC.INT_RAW	0x80	RO	Interrupt RAW Register	0x00000000
ADC.INT_STS	0x84	RO	Interrupt Status Register	0x00000000
ADC.INT_EN	0x88	RW	Interrupt Enable Register	0x00000000
ADC.INT_ACK	0x8C	RW	Interrupt ACK Register	0x0000003F
ADC.FPGA_GAIN	0xF0	RW	FPGA Gain Register	0x0000003F

13.2.1 ADC.CTRL ADC Control Register

ADC.CTRL=0x4000_B000

31 30 29 28 27 26	25	24	23 22 21 20 19 18 17 16	15	14 13	12	11 10 9 8	7 6 5 4	3 2 1	0
Reserved	ADC_STS	SAMPLE_RATE_F	BWAIT	BWAITEN	MODE	MSB_INV	SAMPLE_RATE_I		MCLK_DIV	ADC_EN
	0	0	0x00	0	0	0	0x00		0x0	0
	RO	RW	RW	RW	RW	RW	RW		RW	RW

25	ADC_STS	ADC Status 0 Idle 1 Busy
24	SAMPLE_RATE_F	1 bit fractional part of SAMPLE_RATE parameter
23 16	BWAIT	Burst Wait count value MCLK tick delay (BWAIT+1)
15	BWAITEN	Burst Wait Enable 0 Disable 1 Enable
14 13	MODE	ADC mode configuration 00 Single Run Mode : uses ADC_CFG Register 01 Continuous Mode : uses ADC_CFG Register 10 Continuous Burst Mode : uses ADC_BURST_CTRL 11 Register Continuous All Channel Burst Mode : auto selected by HW
12	MSB_INV	MSB inversion 0 ADC[11:0] = {~ADC[11], ADC[10:0]}, signed to unsigned 1 ADC = ADC
11 4	SAMPLE_RATE_I	8 bit integral part of SAMPLE_RATE SAMPLE_RATE = (SAMPLE_RATE_I) + 1 + (SAMPLE_RATE_F / 2) Sampling Rate = MCLK Frequency / (SAMPLE_RATE) Note : SAMPLE_RATE must be greater than or equal to 2.
3 1	MCLK_DIV	MCLK Divider Value 000 MCLK Disabled 001 MCLK frequency = System APB Bus clock / (MCLK_DIV 010 +1) 011 MCLK frequency = System APB Bus clock / (MCLK_DIV 100 +1) 101 MCLK frequency = System APB Bus clock / (MCLK_DIV 110 +1) 111 MCLK frequency = System APB Bus clock / (MCLK_DIV +1) MCLK frequency = System APB Bus clock / (MCLK_DIV +1) MCLK frequency = System APB Bus clock / (MCLK_DIV +1) MCLK frequency = System APB Bus clock / (MCLK_DIV +1)
0	ADC_EN	ADC Enable 0 Disable 1 Enable

13.2.2 ADC.CFG ADC Configuration Register

ADC.CFG=0x4000_B004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									LDO_EN_I		REFSEL_I		AMUXEN_I		CH_SEL	
																									0		0		0		0x0	
																									RW		RW		RW		RW	

6	LDO_EN_I	LDO1V Enable Signal	
		0	ADC Disable
		1	ADC Enable
5	REFSEL_I	ADC Reference Voltage Selection Pin	
		0	Reference Voltage = VDD1V_ADC
		1	Reference Voltage = EXTREF_A
4	AMUXEN_I	AMUXOUT_A(Selected ADC Input Export) Pin Enable	
		0	AMUXOUT Floating
		1	AMUXOUT output Enable
3 0	CH_SEL	ADC Channel Selection	
		0000	ADC 3V Channel 0
		0001	ADC 3V Channel 1
		0010	ADC 3V Channel 2
		0011	ADC 3V Channel 3
		0100	ADC 3V Channel 4
		0101	ADC 3V Channel 5
		0110	ADC 3V Channel 6
		0111	ADC 3V Channel 7
		1000	ADC 1V Channel 0
		1001	ADC 1V Channel 1
		1010	ADC 1V Channel 2
		1011	ADC 1V Channel 3
		1100	ADC 1V Channel 4
		1101	ADC 1V Channel 5
		1110	ADC 1V Channel 6
		1111	ADC BAT Channel

13.2.3 ADC.BST_CTRL ADC BUSRT Mode Control Register

ADC.BST_CTRL=0x4000_B008

31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10	9 8	7 6 5	4 3 2 1 0
Reserved		BST3_SEL	BST2_SEL	BST1_SEL		BST0_SEL
		0x00	0x00	0x00		0x00
		RW	RW	RW		RW

19 15	BST3_SEL	Burst Mode Selection BIT3_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel BIT3_SEL[4] 0 Disable 1 Enable
14 10	BST2_SEL	Burst Mode Selection BIT2_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel BIT2_SEL[4] 0 Disable 1 Enable
9 5	BST1_SEL	Burst Mode Selection BIT1_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel BIT1_SEL[4] 0 Disable 1 Enable
4 0	BST0_SEL	Burst Mode Selection BIT0_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel BIT0_SEL[4] 0 Disable 1 Enable

13.2.4 ADC.TRIG_CTRL ADC TRIGGER Mode Control Register

ADC.TRIG_CTRL=0x4000_B00C

31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10	9 8	7 6 5	4 3 2 1 0
Reserved		TRIG3_SEL	TRIG2_SEL	TRIG1_SEL		TRIG0_SEL
		0x00	0x00	0x00		0x00
		RW	RW	RW		RW

19 15	TRIG3_SEL	Trigger Mode Selection TRIG3_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel TRIG3_SEL[4] 0 Disable 1 Enable
14 10	TRIG2_SEL	Trigger Mode Selection TRIG2_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel TRIG2_SEL[4] 0 Disable 1 Enable
9 5	TRIG1_SEL	Trigger Mode Selection TRIG1_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel TRIG1_SEL[4] 0 Disable 1 Enable
4 0	TRIG0_SEL	Trigger Mode Selection TRIG0_SEL[3:0] 0-7 ADC 3V Channel 0/1/2/3/4/5/6/7 8-14 ADC 1V Channel 0/1/2/3/4/5/6 15 ADC BAT Channel TRIG0_SEL[4] 0 Disable 1 Enable

13.2.5 ADC.DMA_CTRL DMA Control Register

ADC.DMA_CTRL=0x4000_B020

31 30 29 28 27 26 25 24	23 22 21 20	19	18	17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2	1	0
Reserved		CH1_STS	CH0_STS	CH1_TRCNT		CH0_TRCNT		DMA_CH_SEL	DMA_EN
		0	0	0x00		0x00		0	0
		RO	RO	RW		RW		RW	RW

19	CH1_STS	CH1 DMA Channel Status
		0 Idle
		1 Processing
18	CH0_STS	CH0 DMA Channel Status
		0 Idle
		1 Processing
17 10	CH1_TRCNT	CH1 Transfer Count Note : Transfer Size is always Word size
		CNT CNT + 1
9 2	CH0_TRCNT	CH0 Transfer Count Note : Transfer Size is always Word size
		CNT CNT + 1
1	DMA_CH_SEL	DMA Channel Select when DMA init
		0 Start with CH0
		1 Start with CH1
0	DMA_EN	DMA Transfer enable
		0 Disable
		1 Enable

13.2.6 ADC.DATAOUT0 Data Output Register

ADC.DATAOUT0=0x4000_B024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA1																DATA0															
0x0000																0x0000															
RO																RO															

31 16	DATA1	4bit ADC channel + 12bit ADC Data Note) IF ADC_EN is 1, DATA is 16bit filter outputs. Note) Data0 is latest data.
15 0	DATA0	4bit ADC channel + 12bit ADC Data Note) IF ADC_EN is 1, DATA is 16bit filter outputs. Note) Data0 is latest data.

13.2.7 ADC.DATAOUT1 Data Output Register

ADC.DATAOUT1=0x4000_B028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA3																DATA2															
0x0000																0x0000															
RO																RO															

31 16	DATA3	4bit ADC channel + 12bit ADC Data Note) IF ADC_EN is 1, DATA is 16bit filter outputs. Note) Data0 is latest data.
15 0	DATA2	4bit ADC channel + 12bit ADC Data Note) IF ADC_EN is 1, DATA is 16bit filter outputs. Note) Data0 is latest data.

13.2.8 ADC.DATA_FIFO_STATUS Data FIFO Status Register

ADC.DATA_FIFO_STATUS=0x4000_B02C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						RPTR		Reserved		WPTR		Reserved		CNT	
																						0x0				0x0				0x0	
																						RO				RO				RO	

9 8	RPTR	Read Pointer to FIFO of 16 x 4bits size
5 4	WPTR	Write Pointer to FIFO of 16 x 4bits size
2 0	CNT	Count

13.2.9 ADAC.INT_RAW Interrupt RAW Register

ADC.INT_RAW=0x4000_B080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											RAW				
																											0x00				
																											RO				

4	RAW	Interrupt RAW Register	
0		0000	DMA CH0 Transfer Done Interrupt
		1	DMA CH1 Transfer Done Interrupt
		0001	ALC_HOLD_END Interrupt
		0	ALC_CHNG_END Interrupt
		0010	ADC Done Interrupt
		0	
		0100	
		0	
		1000	
		0	

13.2.10 ADC.INT_STS Interrupt Status Register

ADC.INT_STS=0x4000_B084

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											STATUS			
																											0x00			
																											RO			

4	STATUS	Interrupt STATUS Register	
0		0000	DMA CH0 Transfer Done Interrupt
		1	DMA CH1 Transfer Done Interrupt
		0001	ALC_HOLD_END Interrupt
		0	ALC_CHNG_END Interrupt
		0010	ADC Done Interrupt
		0	
		0100	
		0	
		1000	
		0	

13.2.11 ADC.INT_EN Interrupt Enable Register

ADC.INT_STS=0x4000_B088

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											ENABLE			
																											0x00			
																											RW			

4	ENABLE	Interrupt ENABLE Register	
0		0000	DMA CH0 Transfer Done Interrupt
		1	DMA CH1 Transfer Done Interrupt
		0001	ALC_HOLD_END Interrupt
		0	ALC_CHNG_END Interrupt
		0010	ADC Done Interrupt
		0	
		0100	
		0	
		1000	
		0	

13.2.12 ADC.INT_ACK Interrupt ACK Register

ADC.INT_ACK=0x4000_B088

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											CLEAR			
																											0x00			
																											WC			

4	CLEAR	Interrupt ENABLE Register	
0		0000	DMA CH0 Transfer Done Interrupt
		1	DMA CH1 Transfer Done Interrupt
		0001	ALC_HOLD_END Interrupt
		0	ALC_CHNG_END Interrupt
		0010	ADC Done Interrupt
		0	
		0100	
		0	
		1000	
		0	

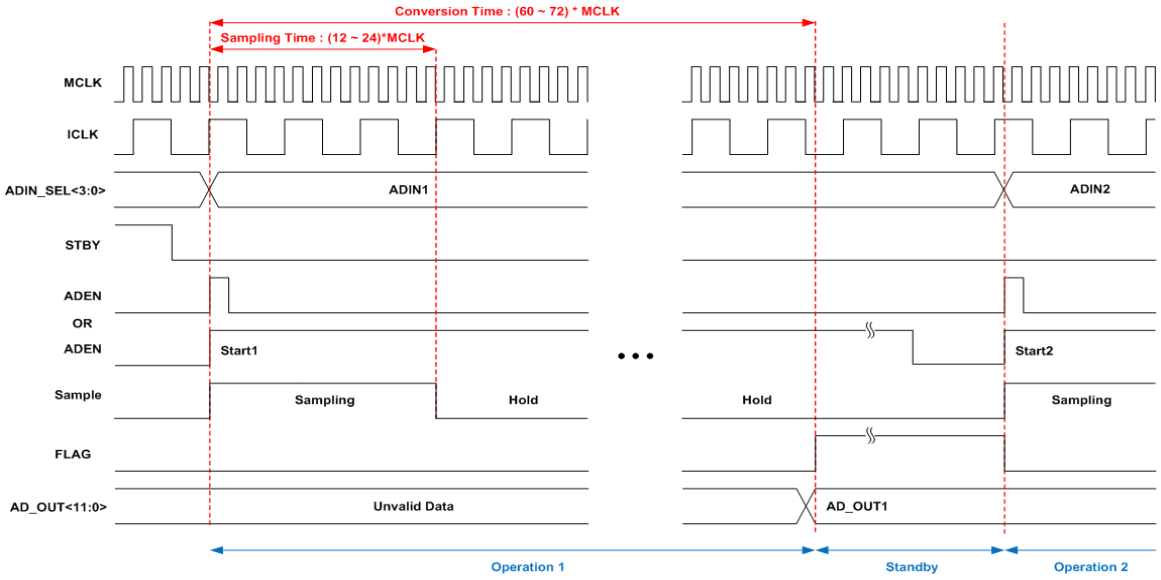
13.3 ADC Channel Configuration

Even though there are 16 channels in ADC IPs, it is recommended that only 5 channels can be used at applications. The following table shows ADC channel configuration.

3V Channel 0	Internal Debug Purpose (VDD_DC)
3V Channel 1	Internal Debug Purpose (VDD_SW)
3V Channel 2	Internal Debug Purpose (VDD_10)
3V Channel 3	Internal Debug Purpose (VDD_SW)
3V Channel 4	Connected to PB[3]
3V Channel 5	Connected to PB[2]
3V Channel 6	Connected to PB[1]
3V Channel 7	Connected to PB[0]
1V Channel 0	Not Used
1V Channel 1	Not Used
1V Channel 2	Not Used
1V Channel 3	Not Used
1V Channel 4	Not Used
1V Channel 5	Not Used
1V Channel 6	Probe Test Only (ADIN1V_S0)
VBAT Channel	Connected VBAT Power

13.4 FUNCTIONAL DESCRIPTION

ADC Interface



CHAPTER 14. DMI (Digital MIC Interface)

14.1 OVERVIEW

This document contains detailed target descriptions about DMI(digital microphone interface) for voice recognition. It's compose of PDM(pulse density modulation) I/F, digital decimation filter and I2S I/F.

14.2 PIN DESCRIPTION

Table14.1 External pin

PIN NAME	TYPE	DESCRIPTION
DMI_CLK	O	Clock for I2S/PDM mode
DMI_LRCLK	O	LR CLK for I2S mode
DMI_DATA	I	Data for I2s/PDM mode

14.3 REGISTERS

The base address of DMI is 0x4000_B300 and register map is described in Table 14.2 and Table 14.3

Table 14.2 Base address of DMI

NAME	BASE ADDRESS
DMI	0x4000_B300

Table 14.3 DMI IP register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
DMI.IF_CTRL	0x00	RW	DMI IF Control Register	0x00000000
DMI.FILT_CTRL	0x10	RW	Filter Mode Control Register	0x00000000
DMI.DMA_CTRL	0x20	RW	DMA Transfer Control Register	0x00000000
DMI.PCM_DATA	0x24	RO	16-bit PCM Output Data Register	-
DMI.INT_RAW	0x80	RW	DMA Transfer Interrupt Register	0x00000000
DMI.INT_STS	0x84	RW	DMA Transfer Interrupt Register	0x00000000
DMI.INT_EN	0x88	RW	DMA Transfer Interrupt Register	0x00000000
DMI.INT_ACK	0x8C	RW	DMA Transfer Interrupt Register	0x00000000

14.3.1 DMI.IF_CTRL DMI IF Control Register

DMI.IF_CTRL=0x4000_B300

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12	11 10 9 8	7 6 5 4 3 2	1	0
Reserved		I2S_SHT	I2S_LRSEL	EDGE_SEL	CLK_DIV		DMI_MODE	DMI_EN
		0x0	0	0	0x000		0	0
		RW	RW	RW	RW		RW	RW

16 14	I2S_SHT	Data Shift Amount Note: valid when DMI_MODE = 1.
		SHT PCM DATA[15:0] = (I2S_DATA[23:0] >> (8- SHT)
13	I2S_LRSEL	I2S Latch Data Selection Note: Valid when DMI_MODE = 1
		0 Latch Left channel Data 1 Latch Right channel Data
12	EDGE_SEL	Latch Data Selection
		0 Latch Data at the rising edge of DMI_CLK 1 Latch Data at the falling edge of DMI_CLK
11 2	CLK_DIV	Clock Frequency Definition Note : APB Bus clock frequency is 16MHz for A31R118. Note : CLK_DIV[11:4] must be greater than or equal to 2. When CLK_DIV[11:4] is equal to 0, CLK is disabled.
		CLK CLK Frequency = (APB Bus clock (=16MHz) x 16) / (CLK + 16)
1	DMI_MODE	DMI Mode selection
		0 PDM Mode 1 I2S Mode
0	DMI_EN	DMI IF Enable
		0 Disable 1 Enable

14.3.2 DMI.FILT_CTRL Filter Mode Control Register

DMI.FILT_CTRL=0x4000_B310

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													HPF_EN	RATE	FILT_EN
																													1	1	1
																													RW	RW	RW

2	HPF_EN	High pass Filter Enable Note: Cutoff Frequency is 4.7Hz
	0	Disable
	1	Enable
1	RATE	PDM Data Rate Selection
	0	1.024Mbps (Decimation by 64)
	1	2.048Mbps (Decimation by 128)
0	FILT_EN	Decimation Filter Enable. When DMI_MODE = 1, FILT_EN must be '0'.
	0	Disable
	1	Enable

14.3.3 DMI.DMA_CTRL DMA Transfer Control Register

DMI.DMA_CTRL=0x4000_B320

31 30 29 28 27 26 25 24	23 22 21 20	19	18	17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2	1	0
		CH1_STS	CH0_STS	CH1_TRCNT		CH0_TRCNT		DMA_CH_SEL	DMA_EN
		0	0	0x00		0x00		0	0
		RO	RO	RW		RW		RW	RW

19	CH1_STS	CH1 DMA Channel Status
		0 0 1 1
18	CH0_STS	CH0 DMA Channel Status
		0 0 1 1
17 10	CH1_TRCNT	CH1 Transfer Count Note : Transfer Size is always Word size
9 2	CH0_TRCNT	CH0 Transfer Count Note : Transfer Size is always Word size
1	DMA_CH_SEL	DMA Channel Select when DMA initialize
		0 0 1 1
0	DMA_EN	DMA Transfer Enable
		0 Disable 1 Enable

14.3.4 DMI.PCM_DATA 16-bit PCM Output Data Register

DMI.PCM_DATA=0x4000_B324

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA1																DATA0															
0x0000																0x0000															
RO																RO															

31 16	DATA1	16-bit PCM Output Data Register
15 0	DATA0	16-bit PCM Output Data Register

14.3.5 DMI.INT_RAW DMA Transfer Interrupt Register

DMI.INT_RAW=0x4000_B380

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														RAW	
																														0x0	
																														RO	

1	RAW	Interrupt RAW Register	
0		01	DMA CH0 Transfer Done Interrupt
		10	DMA CH1 Transfer Done Interrupt

14.3.6 DMI.INT_STS DMA Transfer Interrupt Register

DMI.INT_STS=0x4000_B384

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														STATUS	
																														0x0	
																														RO	

1	STATUS	Interrupt RAW Register	
0		01	DMA CH0 Transfer Done Interrupt
		10	DMA CH1 Transfer Done Interrupt

14.3.7 DMI.INT_EN DMA Transfer Interrupt Register

DMI.INT_EN=0x4000_B388

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														ENABLE	
																														0x0	
																														RW	

1	ENABLE	Interrupt RAW Register	
0		01	DMA CH0 Transfer Done Interrupt
		10	DMA CH1 Transfer Done Interrupt

14.3.8 DMI.INT_ACKDMA Transfer Interrupt Register

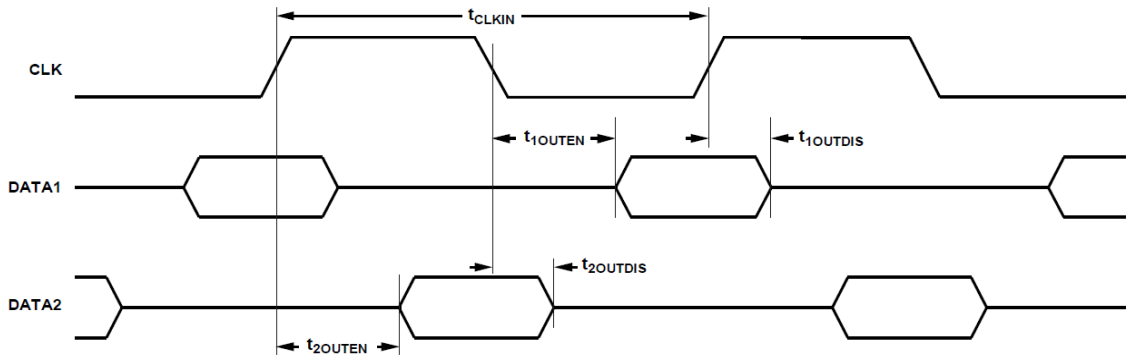
DMI.INT_ACK=0x4000_B38C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														CLEAR	
																														0x0	
																														WC	

1	CLEAR	Interrupt RAW Register	
0		01	DMA CH0 Transfer Done Interrupt
		10	DMA CH1 Transfer Done Interrupt

14.4 FUNCTIONAL DESCRIPTION

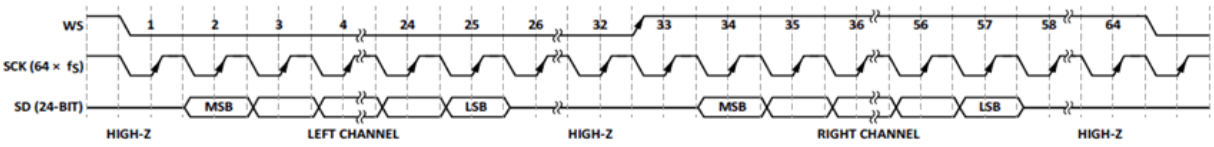
PDM Interface



PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SLEEP MODE						
Sleep Time	Time from CLK falling < 1 kHz		30		µs	1
Wake-Up Time	Time from CLK rising > 1 kHz to output within 3 dB of final sensitivity, power on		10		ms	1
INPUT						
t_{CLKIN}	Input clock period	270		1000	ns	
Clock Frequency (CLK)		1.0	3.072	3.6	MHz	1
Clock Duty Cycle		40		60	%	
OUTPUT						
T_{1OUTEN}	DATA1 (right) driven after falling clock edge	31			ns	
$T_{1OUTDIS}$	DATA1 (right) disabled after rising clock edge	5		23	ns	
T_{2OUTEN}	DATA2 (left) driven after rising clock edge	31			ns	
$T_{2OUTDIS}$	DATA2 (left) disabled after falling clock edge	5		26	ns	

Note 1: The microphone operates at any clock frequency between 1.0 MHz and 3.6 MHz. Some specifications may not be guaranteed at frequencies other than 3.072 MHz.

I2S Timing Interface (from ICS43432)



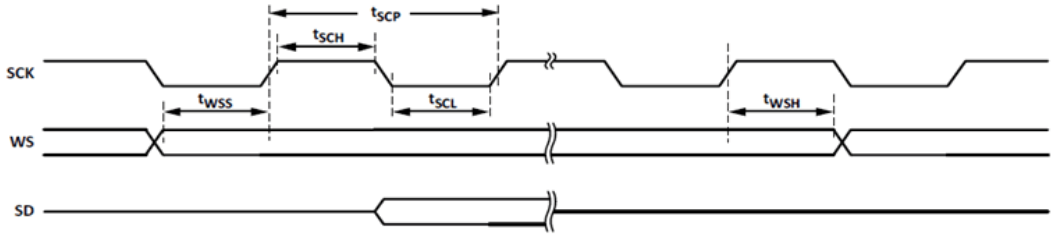
Serial Data Port Timing Specification

SERIAL DATA PORT TIMING SPECIFICATION

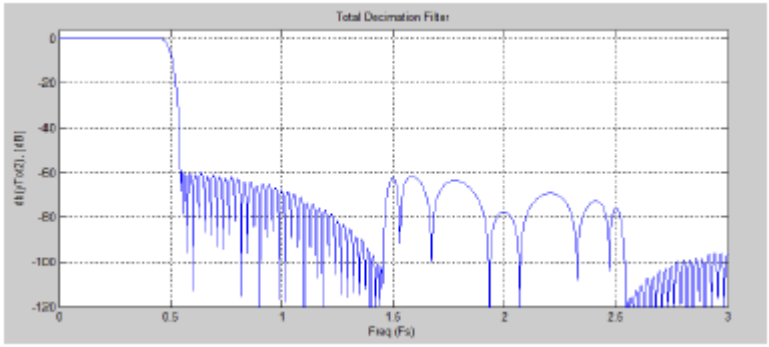
–40°C < TA < +85°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.

PARAMETER	MIN	MAX	UNITS	NOTES
SCK high (t_{SCH})	50		ns	
SCK low (t_{SCL})	50		ns	
SCK period (t_{SCP})	296		ns	
SCK frequency (f_{SCK})	0.460	3.379	MHz	
WS setup (t_{WSS})	0		ns	
WS hold (t_{WSH})	20		ns	
WS frequency (f_{WS})	7.19	52.8	kHz	

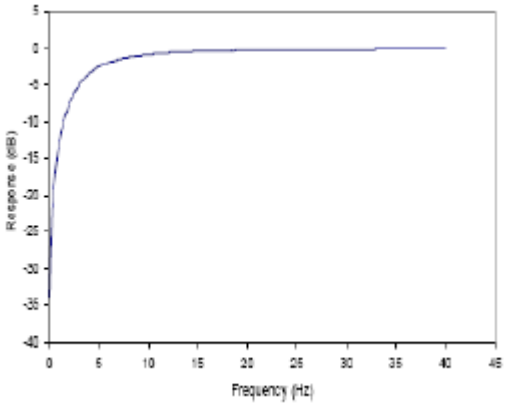
TIMING DIAGRAM



Low pass Filter Response



High pass Filter Response



CHAPTER 15. Q-DECODER

15.1 OVERVIEW

The quadrature encoder, known as 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses the relative phase of two signals, position can be tracked, direction and speed. The QEI consists of decoder logic to interpret the Phase A (PhA) and Phase B (PhB) signal and an up/down counter to accumulate the count.

- Two phase signals, phase a and phase b
- Programmable noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- 32-bit up/down position counter
- Increments / decrements depending on direction

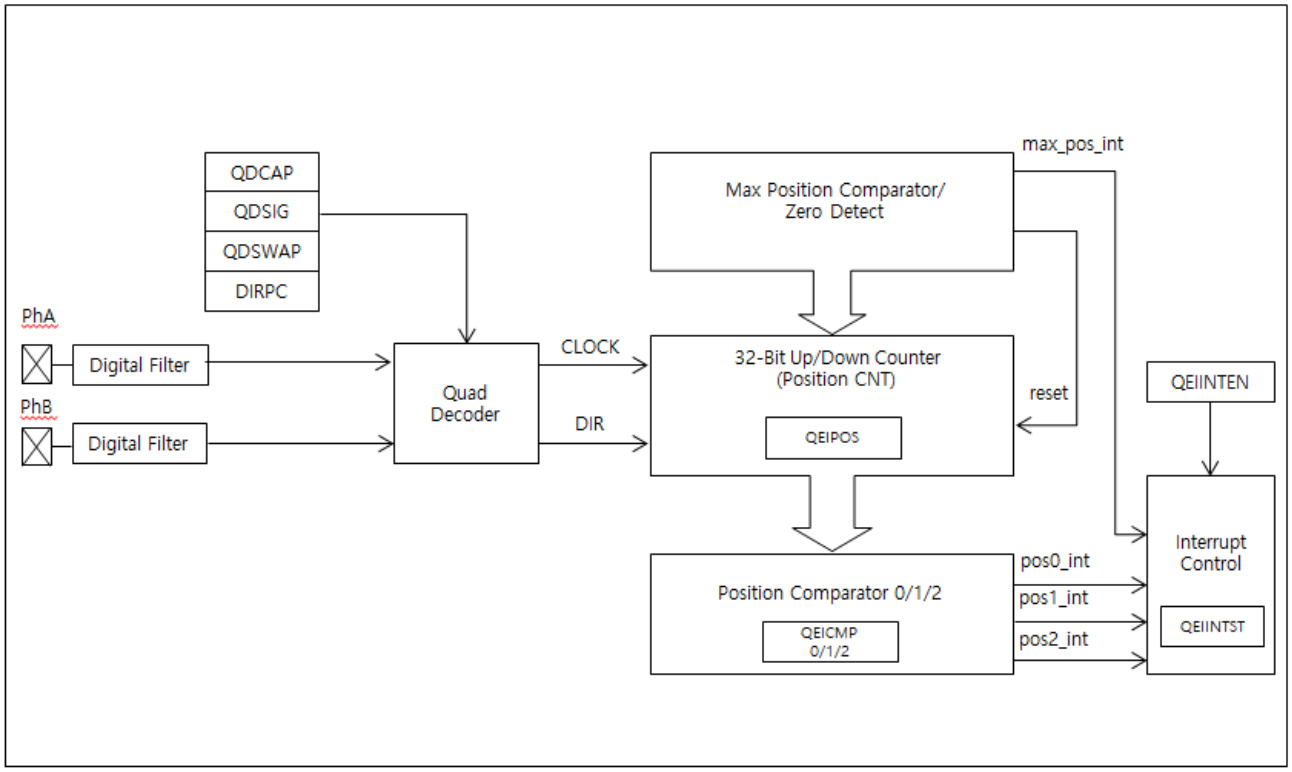


Figure 16.1 Block diagram

15.2 PIN DESCRIPTION

Table 15.1 The External Pins

PIN NAME	TYPE	DESCRIPTION
PhaseA	I	Input of QEI PhaseA
PhaseB	I	Input of QEI PhaseB

15.3 REGISTERS

The base address of QEI is 0x4000_C000 and register map is described in Table 15.2 and Table 15.3

Table 15.2 QEI Base Addresses

NAME	BASE ADDRESS
QEI	0x4000_C000

Table 15.3 The Register List of QEI

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
QEI.MR	0x0000	R/W	QEI Mode Register	0x0000F000
QEI.CON	0x0004	R/W	QEI Control Register	0x00000000
QEI.SR	0x0008	R	QEI Status Register	0x00000000
QEI.POS	0x000C	R/W	QEI Position count Register	0x00000000
QEI.MAX	0x0010	R/W	QEI Maximum Position Register	0xFFFFFFFF
QEI.CMP0	0x0014	R/W	QEI Position Compare Register 0	0xFFFFFFFF
QEI.CMP1	0x0018	R/W	QEI Position Compare Register 1	0xFFFFFFFF
QEI.CMP2	0x001C	R/W	QEI Position Compare Register 2	0xFFFFFFFF
QEI.ISR	0x0050	R/W	QEI Interrupt Enable Register	0x00000000

15.3.1 QEI.MR QEI Mode Register

This register contains bits which control the operation of the position and revolution counters of the QEI module.

QEI.MOD=0x4000_C000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				QECK				Reserved	Reserved	DIRPC	Reserved	QDCAP	QDSIG	QDSWAP	QDMOD
0000				0000				0	0	0	0	0	0	0	0
-				RW				RW	RW	RW	RW	RW	RW	RW	RW

15 12	Reserved	
11 8	QECK[3:0]	Digital Filter Clock Divide Select
		0000 1:1 Clock divide for PhA/PhB/IDX
		0001 1:2 Clock divide for PhA/PhB/IDX
		0010 1:4 Clock divide for PhA/PhB/IDX
		0011 1:16 Clock divide for PhA/PhB/IDX
		0100 1:32 Clock divide for PhA/PhB/IDX
		0101 1:64 Clock divide for PhA/PhB/IDX
		0110 1:128 Clock divide for PhA/PhB/IDX
		0111 1:256 Clock divide for PhA/PhB/IDX
		1000 1:512 Clock divide for PhA/PhB/IDX
		1001 1:1024 Clock divide for PhA/PhB/IDX
7 6	Reserved	
5	DIRPC	Position counter direction control
		0 DIR status not affect to the counter
		1 DIR status will change count direction
4	Reserved	Reserved
3	QDCAP	Capture mode (X2, X4)
		0 Only PhA edge is counted
		1 PhA and PhB edges are counted
2	QDSIG	Signal mode
		0 Quadrature phase signal (PhA, PhB)
		1 Clock and Direction signal (Pha, PhB)
1	QDSWAP	Swap Quadrature decoder input
		0 No swap
		1 Swap PhA and PhB
0	QDMOD	Enable Quadrature decoder
		0 Disable Quadrature decoder
		1 Enable Quadrature decoder

15.3.2 QEI.ON QEI Control Register

This register contains bits which control the operation of the position and revolution counters of the QEI module.

QEI.CON=0x4000_C004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															RESP
0															0

		RW	RW

0	RESP	Reset position counter	
		0	None
		1	Reset position counter to all zeros and reload timer

15.3.3 QEI.SR QEI Status Register

This register provides the status of the encoder interface.

QEI.SR=0x4000_C008

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														Direction	Error
														0	0
														RO	RO

1	Direction	Direction of rotation	
		0	Forward rotation
		1	Reverse rotation
0	Error	Error was detected in the gray code sequence (both signals are changed)	

15.3.4 QEI.POS QEI Position Count Register

This register contains the current value of the encoder position.

QEI.POS=0x4000_C00C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEIPOS																															
0x0000_0000																															
RW																															

31 0	QEIPOS	Current position value

15.3.5 QEI.MAX QEI Maximum Position Register

This register contains the maximum value of the encoder position.

QEI.MAX=0x4000_C010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEIMAX																															
0xFFFF_FFFF																															
RW																															

31 0	QEIMAX	Maximum position value

15.3.6 QEI.CMP0 QEI Position Compare Register 0

This register contains a position compare value.

QEI.CMP0=0x4000_C014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEICMP0																															
0xFFFF_FFFF																															
RW																															

31 0	QEICMP0	Position compare value 0

15.3.7 QEI.CMP1 QEI Position Compare Register 1

This register contains a position compare value.

QEI.CMP1=0x4000_C018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEICMP1																															
0xFFFF_FFFF																															
RW																															

31 0	QEICMP1	Position compare value 1

15.3.8 QEI.CMP2 QEI Position Compare Register 2

This register contains a position compare value.

QEI.CMP2=0x4000_C01C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEICMP2																															
0xFFFF_FFFF																															
RW																															

31 0	QEICMP2	Position compare value 2

15.3.9 QEI.IER QEI Interrupt Enable Register

This register contains enables for each of the QEI module's interrupts.

QEI.INTEN=0x4000_C050

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MAXEN	POS2EN	POS1EN	POS0EN	ENCLKEN	ERREN	DIREN	Reserved
0000								0	0	0	0	0	0	0	0
-								RW	RW	RW	RW	RW	RW	RW	RW

7	MAXEN	Enable that the current position count goes through the QEIMAX value to zero in forward direction or backward direction.
6	POS2EN	Enable that position 2 compare value is equal to the current position
5	POS1EN	Enable that position 1 compare value is equal to the current position
4	POS0EN	Enable that position 0 compare value is equal to the current position
3	ENCLKEN	Enable that decoder clock pulse was detected
2	ERREN	Enable that an decoder phase error was detected
1	DIREN	Enable that a change of direction was detected
0	Reserved	

15.3.10 QEI.ISR QEI Interrupt Status Register

This register contains enables for each of the QEI module's interrupts.

QEI.INTST=0x4000_C054

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MAX	POS2	POS1	POS0	ENCLK	ERR	DIR	Reserved
0000								0	0	0	0	0	0	0	0
-								RW	RW	RW	RW	RW	RW	RW	RW

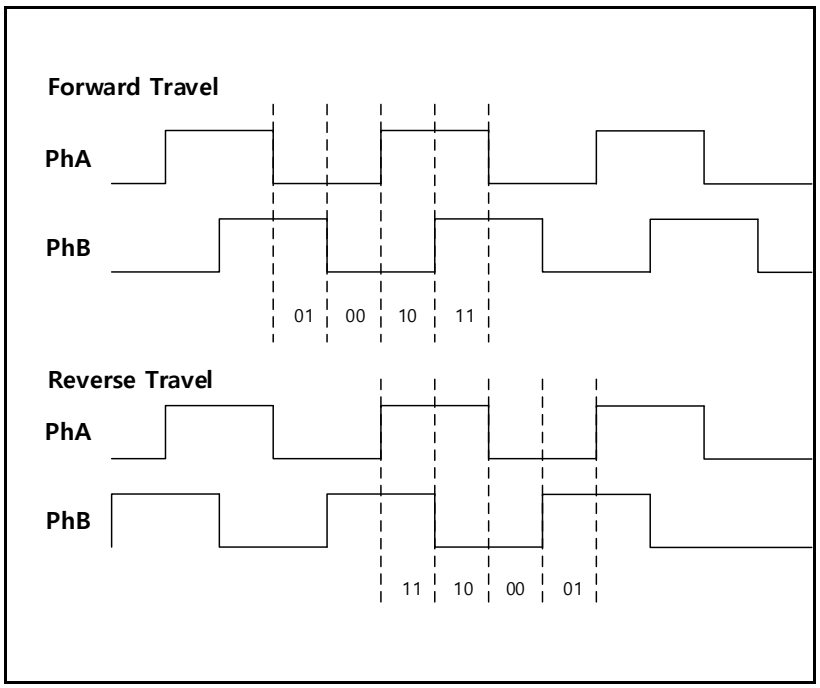
7	MAX	The current position count goes through the QEIMAX value to zero in forward direction or backward direction.
6	POS2	Position 2 compare value is equal to the current position
5	POS1	Position 1 compare value is equal to the current position
4	POS0	Position 0 compare value is equal to the current position
3	ENCLK	Decoder clock pulse was detected
2	ERR	Decoder phase error was detected
1	DIR	Change of phase direction was detected
0	Reserved	

15.4 Functional Description

15.4.1 Quadrature input signals

Quadrature Encoder Interface (QEI) module has two modes of signal operation: quadrature phase mode and Clock/Direction mode. In quadrature phase mode, the edge relationship between PhaseA and PhaseB is used to determine the direction of rotation. In Clock/Direction mode, the encoder produces a clock signal to indicate steps and direction signal to indicate the direction of rotation.

When QEI module receive Phase A edge in front of Phase B edge, the position counter is incremented. And Phase B edge in front Phase A edge, the position counter is decremented.



Encoder state transition

Phase A	Phase B	State
0	1	1
0	0	2
1	0	3
1	1	4

Encoder states

from state	to state	Direction
1	2	Forward
2	3	
3	4	
4	1	

Encoder state transition 1

from state	to state	Direction
4	3	Reverse
3	2	
2	1	
1	4	

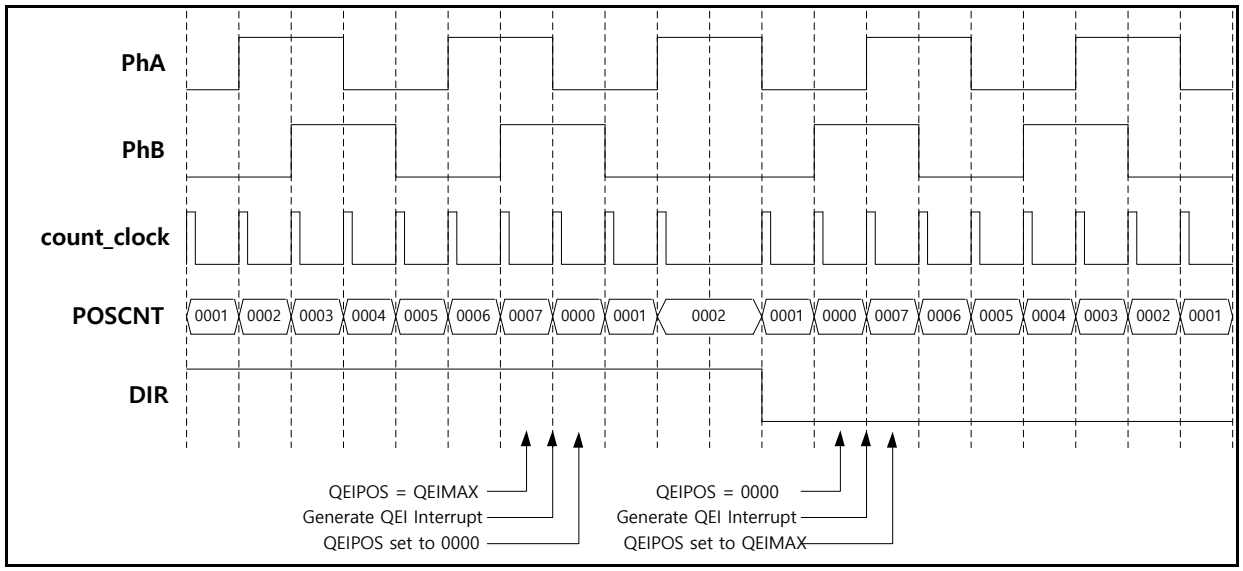
Encoder state transition 2

15.4.2 Position capture

The position capture mode can be set to update the position counter on every edge of the Phase A signal or

to update on every edge of both Phase A and Phase B. Updating the position counter on every Phase A and Phase B provides more positional resolution at the cost of less range in the positional counter.

1. **Using QEIMAX to reset the position counter**
   If the encoder is travelling in the forward direction (Phase A leads Phase B), and QEIPOS (position count value) matches QEIMAX register, QEIPOS resets to zero on the next occurring quadrature pulse edge that increments QEIPOS.



CHAPTER 16. KEY SCANNER

16.1 OVERVIEW

The key scanner supports 8x20 key matrix. It can generate 8 driving pulse singles with specified timing to driving line and support 20 sensing inputs. See the Figure 17.1 for driving and sensing line structure. If any button is not pushed, all sensing lines go high by pull-up resistor. When the K01C button is pushed, sensing line '01' is connected with driving line 'C' and sensing line '01' goes low at the timing of driving 'C' line. The key scanner can detect the change of sensing lines and generate interrupt request signal.

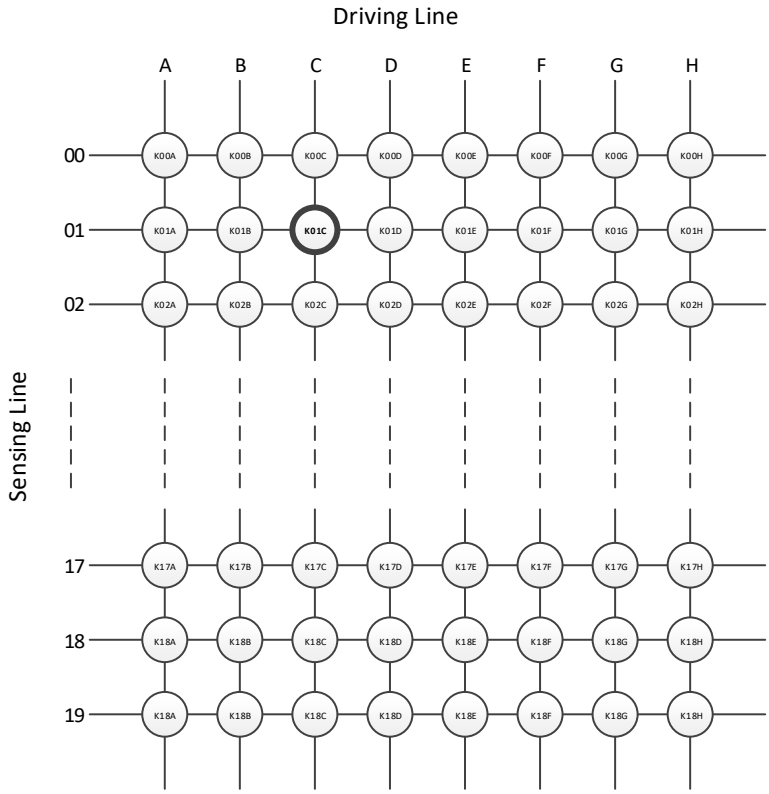
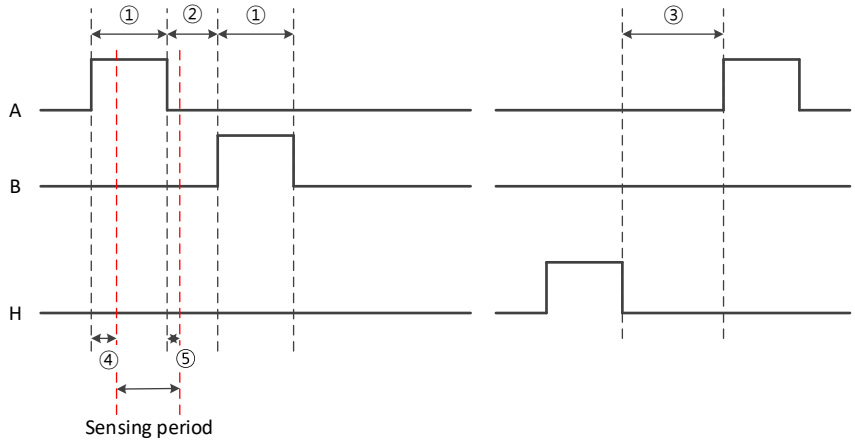


Figure 17.1 8x20 key matrix

The key scanner provides the below configuration. Refer to the Figure 17.2 and register description.

- PIO pin numbers to be used for drive and sensing lines
- Scan rate with active and idle period for driving lines.



① DPPERIOD in DCTIM register, Driving Pulse Period, 12bit pre-scale, 8 bit counter

② DPINTERVAL in DCTIM register, Driving Pulse Interval

③ SINTERVAL in DCTIM register, Scan Interval

④ SSOFFSET in SCTIM register, Sensing Start Offset

⑤ SEOFFSET in SCTIM register, Sensing End Offset

Figure 17.2 Driving and Sensing Timing

16.2 REGISTERS

The base address of Key Scan is 0x4000_D000 and register map is described in Table 16.1 and Table 16.2

.

Table 16.1 Base address of Key Scan

NAME	BASE ADDRESS
KSC	0x4000_D000

Table 16.2 Key Scan Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
KSC.CON	0x0000	RW	Configuration Register	0x00000000
KSC.DCTIM	0x0004	RW	Driving Channel Timing Register	0x00000000
KSC.SCTIM	0x0008	RW	Sensing Channel Timing Register	0x00000000
KSC.CHEN	0x000C	RW	Channel Enable Register	0x00000000
KSC.DCHM0	0x0010	RW	Driving Channel Mapping 0	0x88888888
KSC.DCHM1	0x0014	RW	Driving Channel Mapping 1	0x88888888
KSC.DCHM2	0x0018	RW	Driving Channel Mapping 2	0x88888888
KSC.DCHM3	0x001C	RW	Driving Channel Mapping 3	0x88888888
KSC.SCHM0	0x0020	RW	Sensing Channel Mapping 0	0x00000000
KSC.SCHM1	0x0024	RW	Sensing Channel Mapping 1	0x00000000
KSC.SCHM2	0x0028	RW	Sensing Channel Mapping 2	0x00000000
KSC.SCHM3	0x002C	RW	Sensing Channel Mapping 3	0x00000000
KSC.STATUS_D0	0x0030	RC	Key Status for Driving Channel 0	0x00000000
KSC.STATUS_D1	0x0034	RC	Key Status for Driving Channel 1	0x00000000
KSC.STATUS_D2	0x0038	RC	Key Status for Driving Channel 2	0x00000000
KSC.STATUS_D3	0x003C	RC	Key Status for Driving Channel 3	0x00000000
KSC.STATUS_D4	0x0040	RC	Key Status for Driving Channel 4	0x00000000
KSC.STATUS_D5	0x0044	RC	Key Status for Driving Channel 5	0x00000000
KSC.STATUS_D6	0x0048	RC	Key Status for Driving Channel 6	0x00000000
KSC.STATUS_D7	0x004C	RC	Key Status for Driving Channel 7	0x00000000

16.2.1 KSC.CON Configuration Register

KSC.CON=0x4000_D000

31 30 29 28 27 26 25 24	23 22 21 20	19 18 17	16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1	0
Reserved		INTMODE	INTEN	ITVCLKPRES	DPCLKPRES	Reserved	EN
0x000		0x0	0	0x0	0x0	0x00	0
-		RW	RW	RW	RW	-	RW

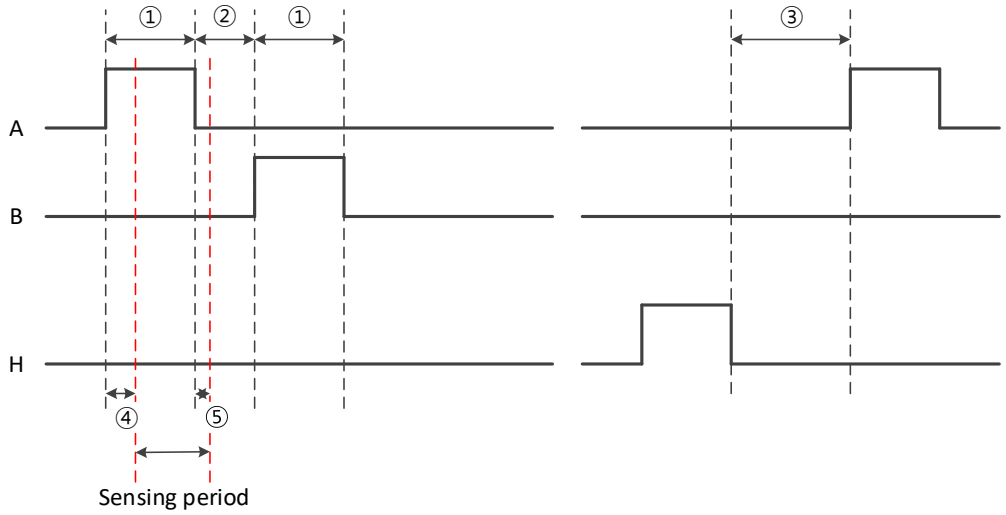
19 17	INTMODE	Key Scanner Interrupt Mode 0 Every key press N At the end of 2^(N-1) scan frame if key press exit
16	INTEN	Key Scanner Interrupt Enable 0 Disable 1 Enable
15 12	ITVCLKPRES	Clock Prescale for Interval or Offset Interval Clock Frequency(ITVCLK) = System Clock Frequency / (2^ITVCLKPRES)
11 8	DPCLKPRES	Clock Prescale for Driving Pulse Driving Pulse Clock Frequency(DPCLK) = System Clock Frequency / (2^DPCKPRES)
0	EN	Key Scanner Enable 0 Disable 1 Enable

16.2.2 KSC.DCTIM Driving Channel Timing Register

KSC.DCTIM=0x4000_D004

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
SINTERVAL	DPINTERVAL	Reserved	DPPERIOD	
0x00	0x00	0x0	0	
RW	RW	-	RW	

31 24	SINTERVAL	Scan Interval Driving Pulse Scan Interval Time = (SINTERVAL + 1) * ITVCLK Period
23 16	DPINTERVAL	Driving Pulse Interval Driving Pulse Interval Time = (DPINTERVAL + 1) * ITVCLK Period
11 0	DPPERIOD	Driving Pulse Period Driving Pulse Period = (DPPERIOD + 1) * DPCLK Period



① DPPERIOD in DCTIM register, Driving Pulse Period, 12bit pre-scale, 8 bit counter

② DPINTERVAL in DCTIM register, Driving Pulse Interval

③ SINTERVAL in DCTIM register, Scan Interval

④ SSOFFSET in SCTIM register, Sensing Start Offset

⑤ SEOFFSET in SCTIM register, Sensing End Offset

16.2.3 KSC.SCTIM Sensing Channel Timing Register

KSC.SCTIM=0x4000_D008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																SEOFFSET								SSOFFSET							
0x0000																0x00								0x00							
-																RW								RW							

15 8	SEOFFSET	Sensing End Offset (System Clock Count) 0~255 : offset clock cycle from driving end point
7 0	SSOFFSET	Sensing Start Offset (System Clock Count) 0~255 : offset clock cycle from driving start point

16.2.4 KSC.CHEN Channel Enable Register

KSC.CHEN=0x4000_D00C

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	SCHEN			DCHEN
0x0	0x00000			0x00
-	RW			RW

27:8	SCHEN	Sensing Channel Enable (Sensing Channel 0 ~ 19)
7:0	DCHEN	Driving Channel Enable (Driving Channel 0 ~ 7)

16.2.5 KSC.DCHM0 Driving Channel Mapping 0 Register

KSC.DCHM0=0x4000_D010

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
GPIO07M	GPIO06M	GPIO05M	GPIO04M	GPIO03M	GPIO02M	GPIO01M	GPIO00M
0x8	0x8	0x8	0x8	0x8	0x8	0x8	0x8
RW	RW	RW	RW	RW	RW	RW	RW

31 28	GPIO07M	GPIO Output Mapping for Driving Channel 7	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
27 24	GPIO06M	GPIO Output Mapping for Driving Channel 6	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
23 20	GPIO05M	GPIO Output Mapping for Driving Channel 5	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
19 16	GPIO04M	GPIO Output Mapping for Driving Channel 4	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
15 12	GPIO03M	GPIO Output Mapping for Driving Channel 3	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]

		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
11 8	GPIO02M	GPIO Output Mapping for Driving Channel 2 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
7 4	GPIO01M	GPIO Output Mapping for Driving Channel 1 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
3 0	GPIO00M	GPIO Output Mapping for Driving Channel 0 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]

16.2.6 KSC.DCHM1 Driving Channel Mapping 1 Register

KSC.DCHM1=0x4000_D014

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
GPIO15M	GPIO14M	GPIO13M	GPIO12M	GPIO11M	GPIO10M	GPIO09M	GPIO08M
0x8	0x8	0x8	0x8	0x8	0x8	0x8	0x8
RW	RW	RW	RW	RW	RW	RW	RW

31 28	GPIO15M	GPIO Output Mapping for Driving Channel 15	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
27 24	GPIO14M	GPIO Output Mapping for Driving Channel 14	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
23 20	GPIO13M	GPIO Output Mapping for Driving Channel 13	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
19 16	GPIO12M	GPIO Output Mapping for Driving Channel 12	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
15 12	GPIO11M	GPIO Output Mapping for Driving Channel 11	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]

		0x6	DP[6]
		0x7	DP[7]
11 8	GPIO10M	GPIO Output Mapping for Driving Channel 10 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
7 4	GPIO09M	GPIO Output Mapping for Driving Channel 9 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
3 0	GPIO08M	GPIO Output Mapping for Driving Channel 8 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]

16.2.7 KSC.DCHM2 Driving Channel Mapping 2 Register

KSC.DCHM2=0x4000_D018

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
GPIO23M	GPIO22M	GPIO21M	GPIO20M	GPIO19M	GPIO18M	GPIO17M	GPIO16M
0x8	0x8	0x8	0x8	0x8	0x8	0x8	0x8
RW	RW	RW	RW	RW	RW	RW	RW

31 28	GPIO23M	GPIO Output Mapping for Driving Channel 23 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
27 24	GPIO22M	GPIO Output Mapping for Driving Channel 22 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
23 20	GPIO21M	GPIO Output Mapping for Driving Channel 21 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
19 16	GPIO20M	GPIO Output Mapping for Driving Channel 20 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
15 12	GPIO19M	GPIO Output Mapping for Driving Channel 19 0x0 0x1 0x2 0x3 0x4 0x5	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5]

		0x6	DP[6]
		0x7	DP[7]
11 8	GPIO18M	GPIO Output Mapping for Driving Channel 18 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
7 4	GPIO17M	GPIO Output Mapping for Driving Channel 17 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
3 0	GPIO16M	GPIO Output Mapping for Driving Channel 16 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]

16.2.8 KSC.DCHM3 Driving Channel Mapping 3 Register

KSC.DCHM3=0x4000_D01C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
GPIO31M	GPIO30M	GPIO29M	GPIO28M	GPIO27M	GPIO26M	GPIO25M	GPIO24M
0x8	0x8	0x8	0x8	0x8	0x8	0x8	0x8
RW	RW	RW	RW	RW	RW	RW	RW

31 28	GPIO31M	GPIO Output Mapping for Driving Channel 31	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
27 24	GPIO30M	GPIO Output Mapping for Driving Channel 30	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
23 20	GPIO29M	GPIO Output Mapping for Driving Channel 29	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
19 16	GPIO28M	GPIO Output Mapping for Driving Channel 28	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]
		0x6	DP[6]
		0x7	DP[7]
15 12	GPIO27M	GPIO Output Mapping for Driving Channel 27	
		0x0	DP[0]
		0x1	DP[1]
		0x2	DP[2]
		0x3	DP[3]
		0x4	DP[4]
		0x5	DP[5]

		0x6	DP[6]
		0x7	DP[7]
11 8	GPIO26M	GPIO Output Mapping for Driving Channel 26 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
7 4	GPIO25M	GPIO Output Mapping for Driving Channel 25 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]
3 0	GPIO24M	GPIO Output Mapping for Driving Channel 24 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	 DP[0] DP[1] DP[2] DP[3] DP[4] DP[5] DP[6] DP[7]

16.2.9 KSC.SCHM0 Sensing Channel Mapping 0 Register

KSC.SCHM0=0x4000_D020

31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	SCH05M	SCH04M	SCH03M	SCH02M	SCH01M	SCH00M
0x0	0x00	0x00	0x00	0x00	0x00	0x00
-	RW	RW	RW	RW	RW	RW

29 25	SCH05M	Sensing Channel 5 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
24 20	SCH04M	Sensing Channel 4 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
19 15	SCH03M	Sensing Channel 3 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
14 10	SCH02M	Sensing Channel 2 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14:

		PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.
9 5	SCH01M	Sensing Channel 1 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.
4 0	SCH00M	Sensing Channel 0 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.

16.2.10 KSC.SCHM1 Sensing Channel Mapping 1 Register

KSC.SCHM1=0x4000_D024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		SCH11M						SCH10M				SCH09M				SCH08M						SCH07M						SCH06M			
0x0		0x00						0x00				0x00				0x00						0x00						0x00			
-		RW						RW				RW				RW						RW						RW			

29 25	SCH11M	Sensing Channel 11 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
24 20	SCH10M	Sensing Channel 10 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
19 15	SCH09M	Sensing Channel 9 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
14 10	SCH08M	Sensing Channel 8 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14:

		PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.
9 5	SCH07M	Sensing Channel 7 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.
4 0	SCH06M	Sensing Channel 6 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.

16.2.11 KSC.SCHM2 Sensing Channel Mapping 2 Register

KSC.SCHM2=0x4000_D028

31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved	SCH17M	SCH16M	SCH15M	SCH14M	SCH13M	SCH12M
0x0	0x00	0x00	0x00	0x00	0x00	0x00
-	RW	RW	RW	RW	RW	RW

29 25	SCH17M	Sensing Channel 17 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
24 20	SCH16M	Sensing Channel 16 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
19 15	SCH15M	Sensing Channel 15 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
14 10	SCH14M	Sensing Channel 14 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14:

		PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.
9 5	SCH13M	Sensing Channel 13 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.
4 0	SCH12M	Sensing Channel 12 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3]
		Note) The same GPIO value must not be written for each valid DCHM and SCHM.

16.2.12 KSC.SCHM3 Sensing Channel Mapping 3 Register

KSC.SCHM3=0x4000_D02C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						SCH19M					SCH18M				
0x0																						0x00					0x00				
-																						RW					RW				

9 5	SCH19M	Sensing Channel 19 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.
4 0	SCH18M	Sensing Channel 18 Mapping Sensing Channel is mapped with the below GPIO mapping value. 0: PA[0], 1: PA[1], 2: PA[2], 3: PA[3],4: PA[4], 5: PA[5], 6: PA[6], 7: PA[7], 8: PB[0], 9: PB[1], 10: PB[2], 11: PB[3],12: PB[4], 13: PB[5], 14: PB[6], 15: PB[7], 16: PC[0], 17: PC[1], 18: PC[2], 19: PC[3], 20: PC[4], 21: PE[0], 22: PE[1], 23: PE[2], 24: PE[3],25: PE[4], 26: PE[5], 27: PE[6], 28: PF[0], 29: PF[1], 30: PF[2], 31: PF[3] Note) The same GPIO value must not be written for each valid DCHM and SCHM.

16.2.13 KSC.STATUS_D0 Key Status for Driving Channel 0 Register

KSC.STATUS_D0=0x4000_D030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D0																			
0x000												0x00000																			
-												RC																			

19 0	STATUS_D0	Key Status for Driving Channel 0 Each bit shows key status for driving channel 0

16.2.14 KSC.STATUS_D1 Key Status for Driving Channel 1 Register

KSC.STATUS_D0=0x4000_D034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D1																			
0x000												0x00000																			
-												RC																			

19	STATUS_D1	Key Status for Driving Channel 1
0		Each bit shows key status for driving channel 1

16.2.15 KSC.STATUS_D2 Key Status for Driving Channel 2 Register

KSC.STATUS_D2=0x4000_D038

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D2																			
0x000												0x00000																			
-												RC																			

19	STATUS_D2	Key Status for Driving Channel 2
0		Each bit shows key status for driving channel 2

16.2.16 KSC.STATUS_D3 Key Status for Driving Channel 3 Register

KSC.STATUS_D3=0x4000_D03C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D3																			
0x000												0x00000																			
-												RC																			

19	STATUS_D3	Key Status for Driving Channel 3
0		Each bit shows key status for driving channel 3

16.2.17 KSC.STATUS_D4 Key Status for Driving Channel 4 Register

KSC.STATUS_D4=0x4000_D040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D4																			
0x000												0x00000																			
-												RC																			

19	STATUS_D4	Key Status for Driving Channel 4
0		Each bit shows key status for driving channel 4

16.2.18 KSC.STATUS_D5 Key Status for Driving Channel 5 Register

KSC.STATUS_D5=0x4000_D044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D5																			
0x000												0x00000																			
-												RC																			

19	STATUS_D5	Key Status for Driving Channel 5
0		Each bit shows key status for driving channel 5

16.2.19 KSC.STATUS_D6 Key Status for Driving Channel 6 Register

KSC.STATUS_D6=0x4000_D048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D6																			
0x000												0x00000																			
-												RC																			

19	STATUS_D6	Key Status for Driving Channel 6
0		Each bit shows key status for driving channel 6

16.2.20 KSC.STATUS_D7 Key Status for Driving Channel 7 Register

KSC.STATUS_D7=0x4000_D04C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STATUS_D7																			
0x000												0x00000																			
-												RC																			

19	STATUS_D7	Key Status for Driving Channel 7
0		Each bit shows key status for driving channel 7

CHAPTER 17. IR Carrier Generator / Capture Control

17.1 OVERVIEW

This section contains detailed target descriptions about IR Carrier Generator and Capture Control.

17.2 PIN DESCRIPTION

Table17.1 External pin

PIN NAME	TYPE	DESCRIPTION
IR_CGIN	O	Carrier Generator output
IR_COMPOUT	I	Input(digital) for IR-learning

17.3 REGISTERS

The base address of IR Carrier is 0x4000_D100 and register map is described in Table 17.2 and Table 17.3

Table 17.2 Base address of IR

NAME	BASE ADDRESS
IR	0x4000_D100

.

Table 17.3 The Register List of IR Carrier Generator and Capture Control

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
RMR	0x00	RW	Remocon Mode Register	0x00000000
CFR	0x04	RW	Carrier Frequency Register	0x00FF00FF
RDD0	0x08	RW	Remocon Data Duration 0 Register	0x00FF00FF
RDD1	0x0C	RW	Remocon Data Duration 1 Register	0x00FF00FF
RODB0	0x10	RW	Remocon Output Data Buffer 0 Register	0x00000000
RODB1	0x14	RW	Remocon Output Data Buffer 1Register	0x00000000
DBSIZE	0x18	RW	Data Bit Size Register	0x00000000
CAPCON	0x20	RW	Capture Control Register	0x0000FF00
STATUS	0x30	RC	Capture Status	0x00000000

17.3.1 RMR Remocon Mode Register

RMR=0x4000_D100

31 30 29	28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4	3	2	1	0
Reserved	INTEN	Reserved			CCK	DCK	Reserved	CEN	DOINV	OUTEN
	0				0x0	0x0		0	0	0
	RW				RW	RW		RW	RW	RW

28	INTEN	Data Transfer / Capture Completion Interrupt Enable
		0 Disable
		1 Enable
10 8	CCK	Carrier counter Note: Capture timer1 clock source (0~7)
		CCK Carrier counter clock frequency = (PCLK clock) / 2^(CCK)
7 4	DCK	Data count Note: Capture timer2 clock source (0~10, 11~15 : Reserved)
		DCK Data counter clock frequency = (PCLK clock) / 2^(DCK)
2	CEN	Carrier Frequency Enable Note: This bit enables CCK counter.
		0 Disable
		1 Enable
1	DOINV	Output Data Inversion
		0 Normal Output
		1 Output Data Inversion
0	OUTEN	Remocon Data Out Enable
		0 Disable
		1 Enable

17.3.2 CFR Carrier Frequency Register

CFR=0x4000_D104

31 30 29 28 27 26	25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
Reserved		CHI	Reserved		CLI
		0x0FF			0x0FF
		RW			RW

25 16	CHI		Carrier High Interval Note: Carrier Frequency = CCLK frequency / (CLI + CHI + 2)
		CHI	Interval = (CHI + 1) * CCLK period Note: CCLK period = PCLK period * (2^CCK)
9 0	CLI		Carrier Low Interval Note: Carrier Frequency = CCLK frequency / (CLI + CHI + 2)
		CLI	Interval = (CLI + 1) * CCLK period Note: CCLK period = PCLK period * (2^CCK)

17.3.3 RDD0 Remocon Data Duration 0 Register

RDD0=0x4000_D108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDDH0																RDDL0															
0x00FF																0x00FF															
RW																RW															

31 16	RDDH0	Data High Duration Note: In capture mode, RDDL is C6 register.	
		RDDH0	Duration = (RDDH0+ 1) * DCLK period Note: DCLK period = PCLK period * (2^DCK)
15 0	RDDL0	Data Low Duration Note: In capture mode, RDDL is C5 register.	
		RDDL0	Duration = (RDDL0 + 1) * DCLK period Note: DCLK period = PCLK period * (2^DCK)

17.3.4 RDD1 Remocon Data Duration 1 Register

RDD1=0x4000_D10C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDDH1																RDDL1															
0x00FF																0x00FF															
RW																RW															

31 16	RDDH1		Data High Duration Note: In capture mode, RDDH is C6 register.
		RDDH1	Duration = (RDDH1+ 1) * DCLK period Note: DCLK period = PCLK period * (2^DCK)
15 0	RDDL1		Data Low Duration Note: In capture mode, RDDL is C5 register.
		RDDL1	Duration = (RDDL1 + 1) * DCLK period Note: DCLK period = PCLK period * (2^DCK)

17.3.5 RODB0 Remocon Output Data Buffer 0 Register

RODB0=0x4000_D110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RODB0																															
0x00000000																															
RW																															

31 0	RODB0	Remocon Output Data Buffer 0
	[31:16]	In capture mode (CAPEN = 1), RODB0[31:16] is C2 register
	[15:0]	In capture mode (CAPEN = 1), RODB0[15:0] is C1 register

17.3.6 RODB1 Remocon Output Data Buffer 1 Register

RODB1=0x4000_D114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RODB1																															
0x00000000																															
RW																															

31	RODB1	Remocon Output Data Buffer 1
0		[31:16] In capture mode (CAPEN = 1), RODB0[31:16] is C4 register
		[15:0] In capture mode (CAPEN = 1), RODB0[15:0] is C3 register

17.3.7 DBSIZE Data Bit Size Register

DBSIZE=0x4000_D118

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		DB1SIZE						Reserved		DB0SIZE					
																		0x00								0x00					
																		RW								RW					

13 8	DB1SIZE	RODB1 register data bit size to be transferred Note: If DB1SIZE is 0, data transfer is finished after RODB0 data transfer.
5 0	DB0SIZE	RODB0 register data bit size to be transferred Note: If DB1SIZE is 0, data transfer is finished after RODB0 data transfer.

17.3.8 CAPCON Capture Control Register

CAPCON=0x4000_D120

31 30 29 28 27 26 25 24	23 22	21 20	19	18	17	16	15 14 13 12	11 10 9 8	7 6 5 4 3 2	1	0
Reserved		T1CMOD	Reserved	T2CLRM	T2INTEN	T1INTEN	T2OVF	T1OVF	Reserved	DIINV	CAPEN
		0x0		0	0	0	0xF	0xF		0	0
		RW		RW	RW	RW	RW	RW		RW	RW

21 20	T1CMOD	Timer 1 average mode 00 No average, 1 pulse count value is saved to C1 ~ C4 01 register 10 2 pulse count average value is saved to C1 ~ C4 register 11 4 pulse count average value is saved to C1 ~ C4 register 8 pulse count average value is saved to C1 ~ C4 register
18	T2CLRM	Timer 2 Clear Mode 0 cleared under Timer 2 overflow or C6 capture condition 1 cleared under Timer 1/2 overflow or C6 capture condition
17	T2INTEN	Timer 2 interrupt enable, Interrupt on C5, C6 capture or Timer2 overflow 0 Disable 1 Enable
16	T1INTEN	Timer 1 interrupt enable, Interrupt on C2, C4 capture or Timer1 overflow 0 Disable 1 Enable
15 12	T2OVF	Timer2 Overflow Value 0~4 overflow when Timer2 is 0x001f 5 overflow when Timer2 is 0x003f 6 overflow when Timer2 is 0x007f 7 overflow when Timer2 is 0x00ff 8 overflow when Timer2 is 0x01ff 9 overflow when Timer2 is 0x03ff 10 overflow when Timer2 is 0x07ff 11 overflow when Timer2 is 0x0fff 12 overflow when Timer2 is 0x1fff 13 overflow when Timer2 is 0x3fff 14 overflow when Timer2 is 0x7fff 15 overflow when Timer2 is 0xffff
11 8	T1OVF	Timer1 Overflow Value 0~4 overflow when Timer1 is 0x001f 5 overflow when Timer1 is 0x003f 6 overflow when Timer1 is 0x007f 7 overflow when Timer1 is 0x00ff 8 overflow when Timer1 is 0x01ff 9 overflow when Timer1 is 0x03ff 10 overflow when Timer1 is 0x07ff 11 overflow when Timer1 is 0x0fff 12 overflow when Timer1 is 0x1fff 13 overflow when Timer1 is 0x3fff 14 overflow when Timer1 is 0x7fff 15 overflow when Timer1 is 0xffff
1	DIINV	Input Data Inversion in IR Capture Mode 0 Normal Output 1 Output Data Inversion

0	CAPEN	Remocon Data Capture Enable	
		0	Disable
		1	Enable

17.3.9 STATUS Capture Status

STATUS=0x4000_D130

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																							CGCOM	T1OV	T2OV	C6ST	C5ST	C4ST	C3ST	C2ST	C1ST
																							0	0	0	0	0	0	0	0	0
																							RC	RC	RC	RC	RC	RC	RC	RC	RC

8	CGCOM	Carrier Generation Completion for RODB0
7	T1OV	Timer 1 overflow error during data high phase
6	T2OV	Timer 2 overflow, End of capture operation
5	C6ST	Timer 2 C6 count capture with RDDH
4	C5ST	Timer 1 overflow & Timer 2 C5 count capture with RDDL
3	C4ST	Timer1 C4 count completion with RODB1[31:16]
2	C3ST	Timer1 C3 count completion with RODB1[15:0]
1	C2ST	Timer1 C2 count completion with RODB0[31:16]
0	C1ST	Timer1 C1 count capture with RODB0[15:0]

17.4 FUNCTIONAL DESCRIPTION

17.4.1 IR Signal Driving (IR TX)

A31R118 provides flexible IR signal driving function. When OUTEN in RMR register is enabled, RODB0 register data is driven out bit by bit from LSB through REMOUT port. The number of driving bit of RODB0 is DB0SIZE in DBSIZE register. When all bits are driven, RODB1 register value is shifted to RODB0 register if DB1SIZE is not zero. DB1SIZE value is shifted to DB0SIZE as well. And then new RODB0 register data is driven out continuously. When CEN is enabled, driven data goes out with carrier frequency which is configured by CLI, CHI, and CCK. The output data duration is determined by DCK, RDDL0, RDDH0. RDDL1 and RDDH1 are shifted to RDDL0 and RDDH0 after all of RODB0 bit is transferred.

17.4.2 IR Signal Capture (IR RX)

A31R118 provides an enhanced IR signal capture function. REMOUT IO is used for IR capture as well as IR driving. When CAPEN is set, C1, C2, C3, C4, C5, and C6 timing is provided. Please refer to Figure 18.1, Figure 18.2, and Figure 18.3 for the detail timing.

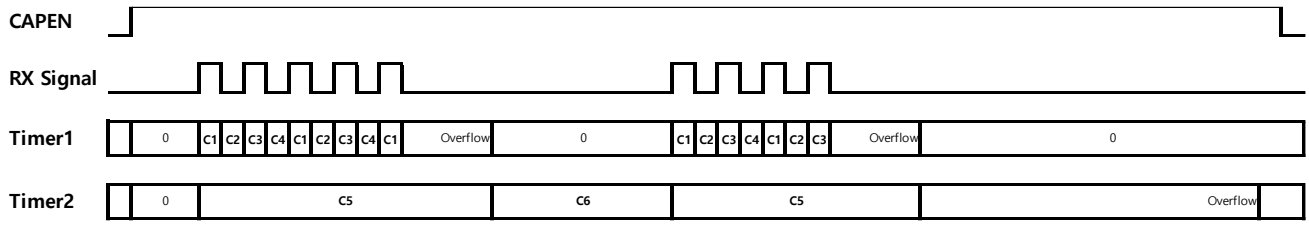


Figure 18.1 IR Capture Timing when T1CMOD = 0

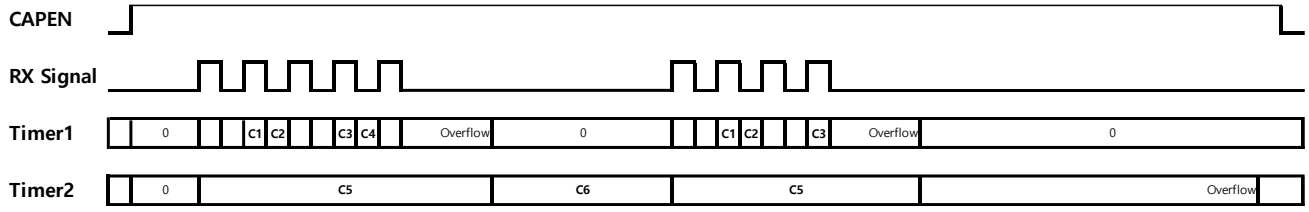


Figure 18.2 IR Capture Timing when T1CMOD = 1

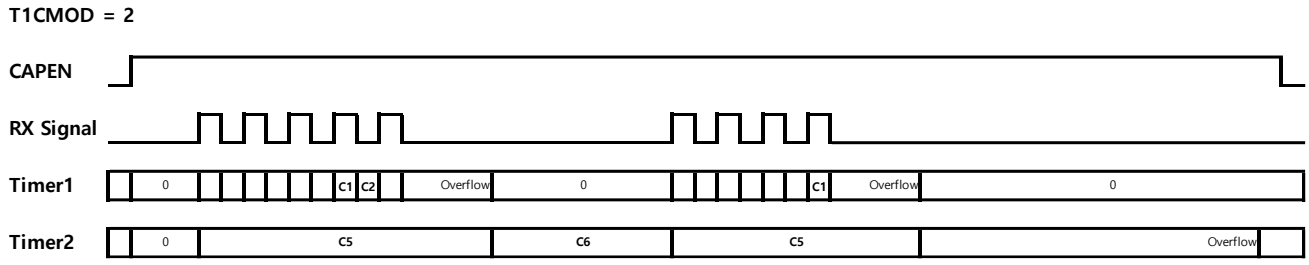


Figure 18.3 IR Capture Timing when T1CMOD = 2

IR signal capture logic uses two timers for counting. Timer1 counts C1, C2, C3, and C4. Timer2 counts C5 and C6. The timer clock period for each register setting is described in Figure 18.4 and Figure 18.5

Timer 1 When PCLK = 16MHz			Overflow Time (ms) T1OVF											
CCK	Frequency (KHz)	Period (us)	15	14	13	12	11	10	9	8	7	6	5	4
0	16000	0.0625	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016	0.008	0.004	0.002
1	8000	0.125	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016	0.008	0.004
2	4000	0.25	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016	0.008
3	2000	0.5	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016
4	1000	1	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032
5	500	2	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064
6	250	4	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128
7	125	8	524.288	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256

Figure 18.4 Timer1 Clock Period

Timer 2 (When PCLK = 16MHz)			Overflow Time (ms) T2OVF											
DCK	Frequency (KHz)	Period (us)	15	14	13	12	11	10	9	8	7	6	5	4
0	16000	0.0625	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016	0.008	0.004	0.002
1	8000	0.125	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016	0.008	0.004
2	4000	0.25	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016	0.008
3	2000	0.5	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032	0.016
4	1000	1	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064	0.032
5	500	2	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128	0.064
6	250	4	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256	0.128
7	125	8	524.288	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512	0.256
8	62.5	16	1048.576	524.288	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024	0.512
9	31.25	32	2097.152	1048.576	524.288	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024
10~15	31.25	32	2097.152	1048.576	524.288	262.144	131.072	65.536	32.768	16.384	8.192	4.096	2.048	1.024

Figure 18.5 Timer2 Clock Period

SECTION 3. CHARACTERISTICS

CHAPTER 1. FLASH Programming

1.1 FLASH API

1.1.1 FLASH WRITE

int32_t flash_write(uint32_t flash_addr, void *buf, uint32_t size)

This API writes to flash memory. The memory must be erased first to write new data. Flash access must be protected with IRQ disabled. It returns a non-zero on error, otherwise 0.

1.1.2 FLASH READ

int32_t flash_read(uint32_t flash_addr, uint8_t *buf, uint32_t size)

This API read flash memory.

1.1.3 FLASH ERASE

int32_t flash_erase(uint32_t flash_addr, uint8_t *buf, uint32_t size)

This API read flash memory. The whole sector(4KB) at the specified memory will be erased. Flash address should be aligned sector size. Flash access must be protected with IRQ disabled. It returns a non-zero on error, otherwise 0.

CHAPTER 2. Electrical Characteristics

2.1 DC Characteristics

2.1.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum rating

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +3.63	V	–
	IO_VDD	-0.3~+3.63	V	–
	RF_VDD	-0.3~+1.65	V	[1]RFA_VDD, [20]VDD_SW_10, [44]A_VDD, [47]RFP_VDD, [48]RFV_VDD
	VSS	-0.3~+0.3	V	–
Normal Pin	VI	-0.3~min(VBAT+0.3,3.63)	V	–
	VO	-0.3~min(VBAT+0.3,3.63)	V	
	IOH	5	mA	–
	ΣIOH	TBD	mA	–
	IOL	5	mA	–
	ΣIOL	TBD	mA	–
Xtal Pin	XO_OUT	-0.3~+1.65	V	
	XO_IN	-0.3~+1.65	V	
Storage Temperature	TSTG	-65 – +150	°C	–

Notes) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.1.2 ESD Characteristics

Table 2.2 ESD Characteristics

Parameter	Symbol	Min	Units
ESD HBM	-	2000	V
ESD MM	-	200	V
ESD CDM	-	750	V

2.1.3 Recommended Operating Conditions

Table 2.3 Recommended Operating Conditions (T_A = - 20 °C to + 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VBAT	2x1.5V Battery 1x3V Battery	1.9	3.0	3.6	V
Operating Temperature	T_{OPR}	-	-30	-	85	°C

Operating Frequency	F_{OPR}	-	-	32	-	MHz

2.1.4 DC/DC Converter Characteristics

Table 2.4 DC/DC Converter Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Buck Input voltage	PW1	-	1.9	3.0	3.6	V
Buck Output voltage	BUCK_OUT	-	-	1.2	-	V
Buck efficiency	-	Load current : 20 mA	70	82	88	%

2.1.5 PMU LDO Characteristics

Table 2.5 PMU LDO Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating input voltage	VBAT	I_{out}=10 mA	1.9	3.0	3.6	V
Output Voltage	V_{PMU_OUT}	I_{out}=10 mA	-	1.2	-	V
Power Supply voltage rejection ratio	-	Freq. = 10 kHz	-	-27	-	dB
External Capacitor	C_L	-	1	-	-	uF

2.1.6 Brown Out Detector (BOD) Characteristics

Table 2.6 Brown Out Detector Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V_{BODR}	-	1.6	1.8	2.0	V

2.1.7 32MHz Crystal Oscillator Characteristics

Table 2.7 32MHz Crystal Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Crystal Frequency	F_{X32M}	-	-	32	-	MHz
Crystal Tolerance	-	-	-40	-	40	ppm
ESR Equivalent series resistance	-	-	-	20	-	ohm
Load Capacitance	-	-	7	-	10	pF
Start-up time	-	-	-	200	-	us

2.1.8 32kHz Internal Oscillator Characteristics

Table 2.8 32kHz Internal Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Current	I_{OP}	-	-	150	250	nA
Output Frequency	F_{OUT}	-	29.4	32.768	36.1	KHz

Notes) 32kHz internal oscillator frequency is self-calibrated at BLE Active mode.

2.1.9 32.768kHz Crystal Oscillator Characteristics

Table 2.9 32.768 kHz Crystal Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Current	I_{DD}	CL=7pF	-	150	400	nA
Crystal Tolerance	-	-	-100	-	100	ppm
Output Frequency	f_{OUT}	-	-	32.768	-	KHz
External Load Capacitor	C_L	-	5	-	7	pF
Feedback Resistance	R_{FB}	-	13.2	23.8	53	MΩ

2.1.10 12-bit SAR-ADC Characteristics

Table 2.10 12-bit SAR-ADC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	VBAT	-	1.9	3.0	3.6	V
Resolution		-	-	-	12	BIT
Operating Current	I_{VBAT}	@f_{MCLK}=8MHz	-	100	-	uA
Analog Input Range	V_{in}	-	0	-	VBAT	V
Differential nonlinearity	DNL	-	-	±6	±12	LSB
Integral nonlinearity	INL	-	-	±10	±20	LSB
Input Clock Frequency	MCLK	-	-	-	8	MHz
Sampling Time	t_{SAMPLE}	@MCLK=8MHz	-	1.0 (8*MCLK)	-	us
Conversion Time	t_{CONV}	-	-	6.0 (48*MCLK)	-	us

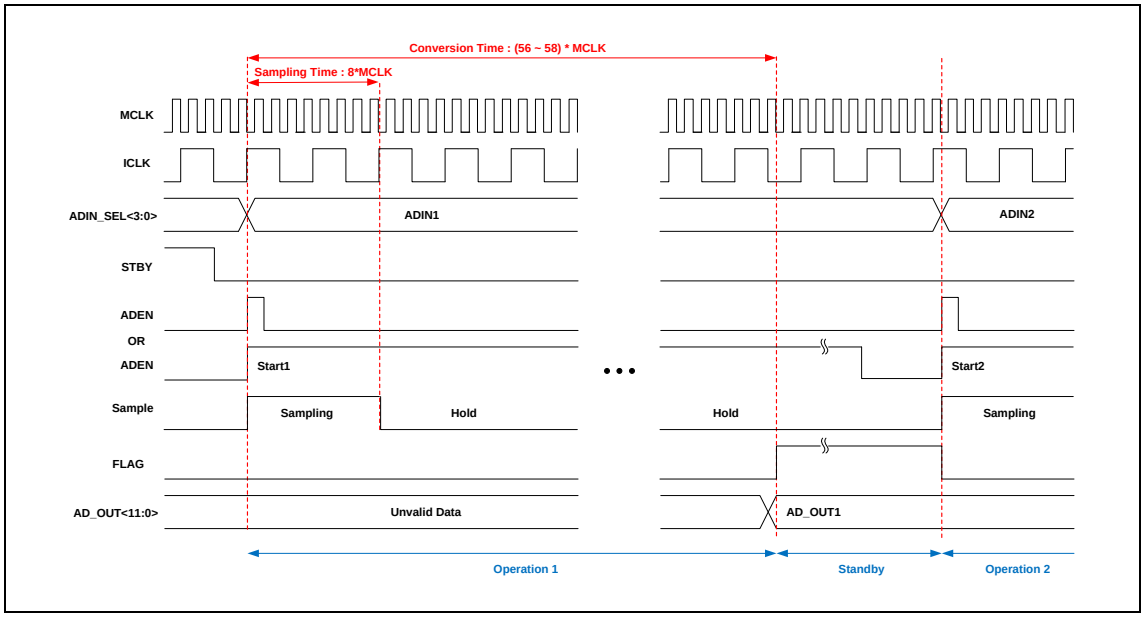


Figure 2.2 ADC timing diagram

2.1.11 Power-On Reset(POR) Characteristics

Table 2.11 Power-On Reset Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POR Detect Voltage	V_{POR}	EXT DC SIM	1.16	1.42	1.64	V
VBAT Ramping-up time 3.0V		0V 3.0V VBAT ramping-up time	-	-	0.5	ms

2.1.12 FLASH Memory Characteristics

Table 2.12 Flash Memory Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VVDDEXT	-	1.65	1.8	3.6	V
VCC Read Current	ICC1	F=33MHz, Use 4 I/O	-	3.9	6.5	mA
VCC Program Current	ICC2	-	-	5.8	10	mA
VCC Sector/Block Erase Current	ICC3	-	-	3.5	10	mA
VCC Chip Erase Current	ICC4	-	-	3.5	10	mA
Page Program Cycle Time	tPP	-	-	0.85	4	ms
Sector Erase Cycle Time	tSE	-	-	40	240	ms
Block(64KB) Erase Cycle Time	tBE	-	-	0.48	3	s
Chip Erase Cycle Time	tCE	-	-	3	9	S
Endurance			10,000			Write/Erase Cycle

2.1.13 General RF Characteristics

Table 2.13 General RF Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF Frequency Range	F_{SYN}	-	2400	-	2483.5	MHz
Channel Spacing	F_{CH}	-	-	2	-	MHz
On-air data rate	-	-	-	1	-	Mbps
Reference Frequency	F_{REF}	-	-	32	-	MHz
IDLE to TX settling time	$T_{IDLE-TX}$	Including calibrations and synthesizer lock	-	-	120	µs
IDLE to RX settling time	$T_{IDLE-RX}$	Including calibrations and synthesizer lock	-	-	120	µs

2.1.14 RF Transmitter Characteristics

Table 2.14 RF Transmitter Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Accuracy	-	BT TRM-LE/CA/06/C	-150	-	150	kHz
Maximum drift	-	BT Radio Frequency tolerance	–50	-	50	kHz
Maximum drift rate	-	BT Radio Frequency tolerance	-20	-	20	kHz/50μs
Initial frequency drift	-	-	-20	-	20	kHz
Modulation Deviation	Δf	-	185	250	-	kHz
Modulation Index	BT	-	0.45	0.5	0.55	
Output Power Range	P_{TX}		-20	0	+1	dBm
TX Power Variation vs. Frequency	$\Delta P_{TX-FREQ}$	Measured across any frequency band (2400–2483.5 MHz)	-	±1	±2	dB
In-band spurious emission	-	2MHz offset, 100kHz RBW	-	-	-26	dBm
	-	3MHz offset, 100kHz RBW	-	-	-36	dBm
Out-of-band spurious emission	-	<1.0GHz, FCC-15.247, RBW 100kHz	-	-	-55.5	dBm
	-	>1.0GHz, FCC-15.247, RBW 100kHz	-	-	-41.5	dBm
	-	2398MHz, RBW 1MHz (ETSI)	-	-	-30	dBm

2.1.15 RF Receiver Characteristics

Table 2.15 RF Receiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range	F_{TX}	World Wide (Not Supported)	2400	-	2483.5	MHz
RX Sensitivity (PER < 30.8%)	$P_{RX-1MHz}$	clean transmitter	-	-94	-86	dBm
RX Sensitivity (PER < 30.8%)	$P_{RX-1MHz}$	dirty transmitter	-	-91	-82	dBm
Maximum Receiving Power	P_{RX-MAX}	-	-	0	-	dBm
RX Channel Bandwidth	BW	Depends on the input data rate	-	1.0	-	MHz
RSSI Resolution	$RSSI_{RES}$	-50 ~ -85 dBm	-	1	-	dB
RSSI Accuracy	$RSSI_{ACC}$	-50 ~ -85 dBm	-4	-	4	dB
C/I and receiver selectivity performance	CO	Co-channel PER < 30.8%, wanted signal –67 dBm	-	12	21	dB
	C/I_1	±1 MHz offset, PER < 30.8%, wanted signal –67 dBm	-	-19	-12	
	C/I_2	±2 MHz offset, PER < 30.8%, wanted signal –67 dBm	-	-23	-20	
	C/I_3	±3 MHz offset, PER < 30.8%, wanted signal –67 dBm	-	-37	-30	
	C/I_{image}	Image Frequency	-	-15	-12	
Blockers (For Desired signal at -67dBm)	P_{BLOCK1}	Blockers from 20 to 1999 MHz	-33	-	-	dBm
	P_{BLOCK2}	Blockers from 2 to 2.399 GHz	-38	-	-	dBm
	P_{BLOCK3}	Blockers from 2.484 to 2.999 GHz	-38	-	-	dBm
	P_{BLOCK4}	Blockers from 3.0 to 12.75 GHz	-33	-	-	dBm
Intermodulation		Standard test	-47	-43	-	dBm
Receiver Spurious emission		30 MHz to 1 GHz, MBW 100kHz	-	-	-60	dBm
		1 GHz to 12,75 GHz, MBW 1MHz	-	-	-50	dBm

2.1.16 DC Characteristics

Table 2.16 DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage	VIL	-	0	-	0.2VDD	V
Input High Voltage	VIH	-	0.8VDD	-	VDD	V
Output Normal Voltage of GPIO	VOL	VBAT=3.0V, IOL=5mA	-	-	0.5	V
Output High Voltage of GPIO	VOH	VBAT=3.0V, IOH=-5mA	2.4	-	-	V
Input High Leakage Current	IIH	-	-	-	0.1	uA
Input Low Leakage Current	IIL	-	-	-	0.1	uA
Pull-Up Resistors	RPU	VBAT=3.0V, VIN = 0V	-	50	-	kohm
Power Supply Current	IDD1	NORMAL STATE : BLE Tx, 0dBm 3V DC/DC Buck SRAM execution	-	9.5	11.5	mA
	IDD2	NORMAL STATE : BLE Rx 3V DC/DC Buck SRAM execution	-	9.5	11.5	mA
	IDD3	BLE_IDLE	-	1.6	2.5	mA
	IDD4	MCU IDLE	-	1.25	2	mA
	IDS1	DEEP_SLEEP (48KB Retention on, 32KHz CLK on)	-	1300	-	nA
	IDS2	HIBERNATE (48KB Retention off, 32KHz CLK on)	-	900	-	nA
	IDS3	DORMANT (48KB Retention off, 32KHz CLK off)	-	700	-	nA

2.1.17 General Characteristics

Table 2.17 General Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Wake-up time	-	From Idle to CPU Active	-	1	-	us
	-	From Deep Sleep to CPU Active	-	4.5	5	ms

Note) Refer to Application Note