A31R713

General Purpose Cortex-M0+ Microcontroller
Flash 64KB, SRAM 8KB, ADC, LCD Driver

Datasheet Version 1.10

Features

- High performance Cortex-M0+ core
- 64KB code flash memory
- 8KB SRAM
- Watchdog Timer
- Eight general purpose timers
  - Periodic, one-shot, PWM, capture
- 12-bit ADC, 50ksps
  - 11-channel inputs
- External communication ports
  - 2xUSART(UART + SPI)
  - 1xI2C
  - 1xUART
- Clock monitoring function for system clock
- LCD driver for up to 4x38 segments
  - Internal/external resistor bias
  - Voltage booster with 16-step contrast control
- 16-bit CRC generator
  - CRC-CCITT
  - CRC-16
- SWD debug interface
- Supports USART (UART + SPI) ISP
- Three types of package options
  - LQFP80-1212
  - TQFP64-0707
  - LQFP48-0707
- Commercial grade (-40℃ to +85℃)

Applications

- LCD remote controller
- OLED remote controller
- Consumer electronics
- General purpose

Product Selection Table

Table 1. Device Summary

Part Number	Flash	SRAM	USART	UART	I2C	TIMER	ADC	COM	SEG	I/O	Package
A31R713ML	64KB	8KB	2	1	1	8	11 ch	4	38	73	80LQFP-1212
A31R713RT*	64KB	8KB	2	1	1	7	11 ch	4	31	61	64TQFP-0707
A31R713CL*	64KB	8KB	2	1	1	5	8 ch	4	23	45	48LQFP-0707

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.

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1 Description

The A31R713 is a microcontroller based on ARM Cortex-M0+ core with a flash memory of up to 64KB, and an SRAM of 8KB. Operation voltage of the device is 1.8V to 5.5V. It provides a highly flexible and cost effective solution for many embedded control applications.

The A31R713 has 16-bit timers, 32-bit timers, 12-bit ADC, CRC generator, UART, USART, I2C, LCD driver/controller, etc. The A31R713 also has a POR, LVR, LVI, and an internal RC oscillator. The A31R713 support sleep and deep sleep modes to reduce power consumption.

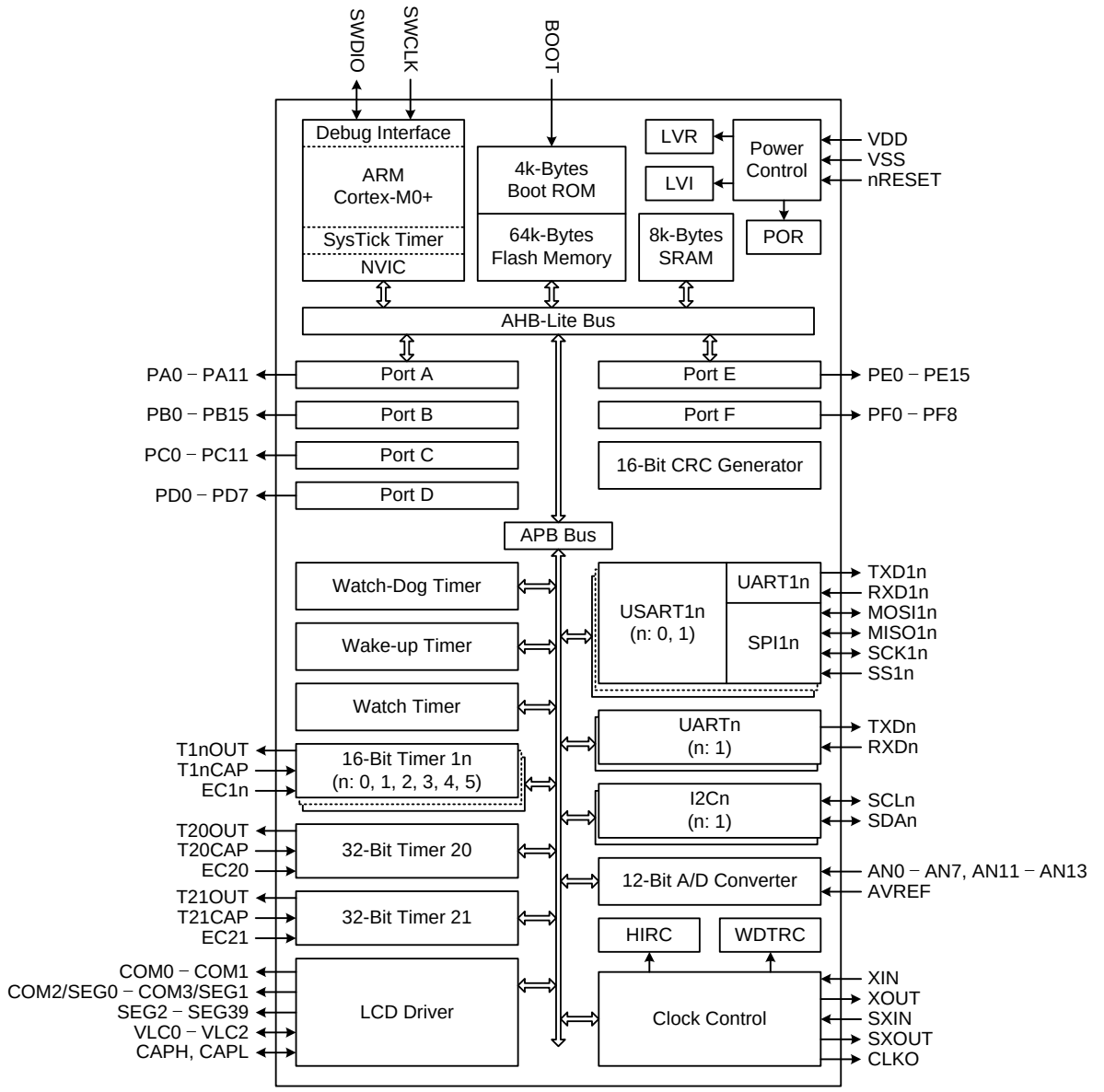
1.1 Device overview

Table 2. A31R713 features and peripheral counts

Device / Peripheral	A31R713
CPU	Cortex-M0+
Flash ROM (Kbytes)	64
SRAM (bytes)	8KB
I/O	73 programmable
Timers	Watchdog timer
	Eight general purpose timers — Periodic, one-shot, PWM, capture mode
LCD driver	• 38 segments and 4 commons • Duty selectable, resistor bias • Voltage booster with 16-step contrast control
ADC	11-channel input, 12-bit ADC with 50ksps
CRC generator	• 16-bit CRC generator, CRC-16, CRC-CCITT
External communication ports	• 2 USARTs (UART + SPI) • 1 I^2C • 1 UART
System fail-safe function	Clock monitoring
Debug interface	SWD debug interface
Packages	LQFP 80-1212 (0.5mm pitch)
	TQFP 64-0707 (0.4mm pitch)
	LQFP 48-0707 (0.5mm pitch)
Operating temperature	-40℃ to +85℃ (commercial grade)

1.2 Block diagram

Figure 1 shows a block diagram of A31R713.



NOTE: There are no T13OUT and T14OUT pins of 16-bit Timer 1n modules.

Figure 1. A31R713 Block Diagram

1.3 Functional description

The following section provides an overview of the features of the A31R713 microcontroller.

1.3.1 ARM Cortex-M0+

Cortex-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area-optimized, low-power processor.

On core system timer (SYSTICK) provides a simple 24-bit timer to use as a real time operating system (RTOS) or as a simple counter. The processor implements the ARMv6-M Thumb instruction set, including a number of 32-bit instructions that use Thumb-2 technology. Hardware single-cycle multiplication is available.

Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.

It also supports SWD debugging features.

1.3.2 Nested vector-interrupt controller (NVIC)

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC embedded in the Cortex-M0+ processor core is capable of low latency interrupts processing and efficient processing of late arriving interrupts.

All NVIC registers are only accessible using word transfers.

1.3.3 64KB internal code flash memory

A31R713 has built-in 64KB code flash memory. It supports self-programming feature, and supports ISP and JTAG programming in boot or debug mode.

1.3.4 8KB internal SRAM

On-chip 8KB SRAM is used as a working memory space and as a program code area temporarily.

1.3.5 Boot logic

A boot logic supports flash programming. The boot logic will be activated when the external boot pin was set to boot mode.

1.3.6 System Control Unit (SCU)

An SCU block manages internal power, clock, reset and operation mode. It also controls the analog blocks (Oscillator Block, VDC and LVR).

1.3.7 24-bit Watchdog timer (WDT)

A Watchdog timer monitors the system. It generates internal reset or interrupt to notice abnormal status of the system.

1.3.8 Multi-purpose 16-bit timer and 32-bit timer

Six-channel 16-bit and two-channel 32-bit general-purpose timers support the functions introduced below:

- Periodic timer mode
- Counter mode
- PWM mode(except T13/T14)
- Capture mode

1.3.9 USART (UART and SPI)

USART supports UART and SPI mode. The A31R713 has 2 channel USART modules.

Boot mode uses this USART block to download flash program.

1.3.10 Inter-Integrated Circuit interface (I2C)

A31R713 has one channel of I2C block and supports up to 1MHz I2C communication. Master and slave modes are available.

1.3.11 Universal Asynchronous Receiver/Transmitter (UART)

A31R713 has one channel of UART block. For accurate baud rate control, a fractional baud-rate generation feature is available.

1.3.12 General PORT I/Os (GPIO)

12-bit PA port, 16-bit PB port, 12-bit PC port, 8-bit PD port, 16-bit PE port, and 9-bit PF port are available and provide multiple functions.

- General I/O port
- External interrupt input port and on-chip input debounce filter
- Programmable pull-up, pull-down, and open-drain selection

1.3.13 12-bit Analog-to-Digital Converter (ADC)

An ADC can convert analog signal at a conversion rate of up to 50ksps. 11-channel analog MUX provides various combinations of data from external analog signals.

1.3.14 LCD driver/controller

A LCD driver supports an internal/external resistor bias and capacitor bias, voltage booster and 16-step contrast control and various duties.

1.3.15 16-bit Cyclic Redundancy Check (CRC) generator

A31R713 has two polynomials for the CRC generator: CRC-CCITT and CRC-16.

2 Pinouts and pin descriptions

In chapter 2, pinouts and pin descriptions of A31R713 are introduced.

2.1 Pinouts

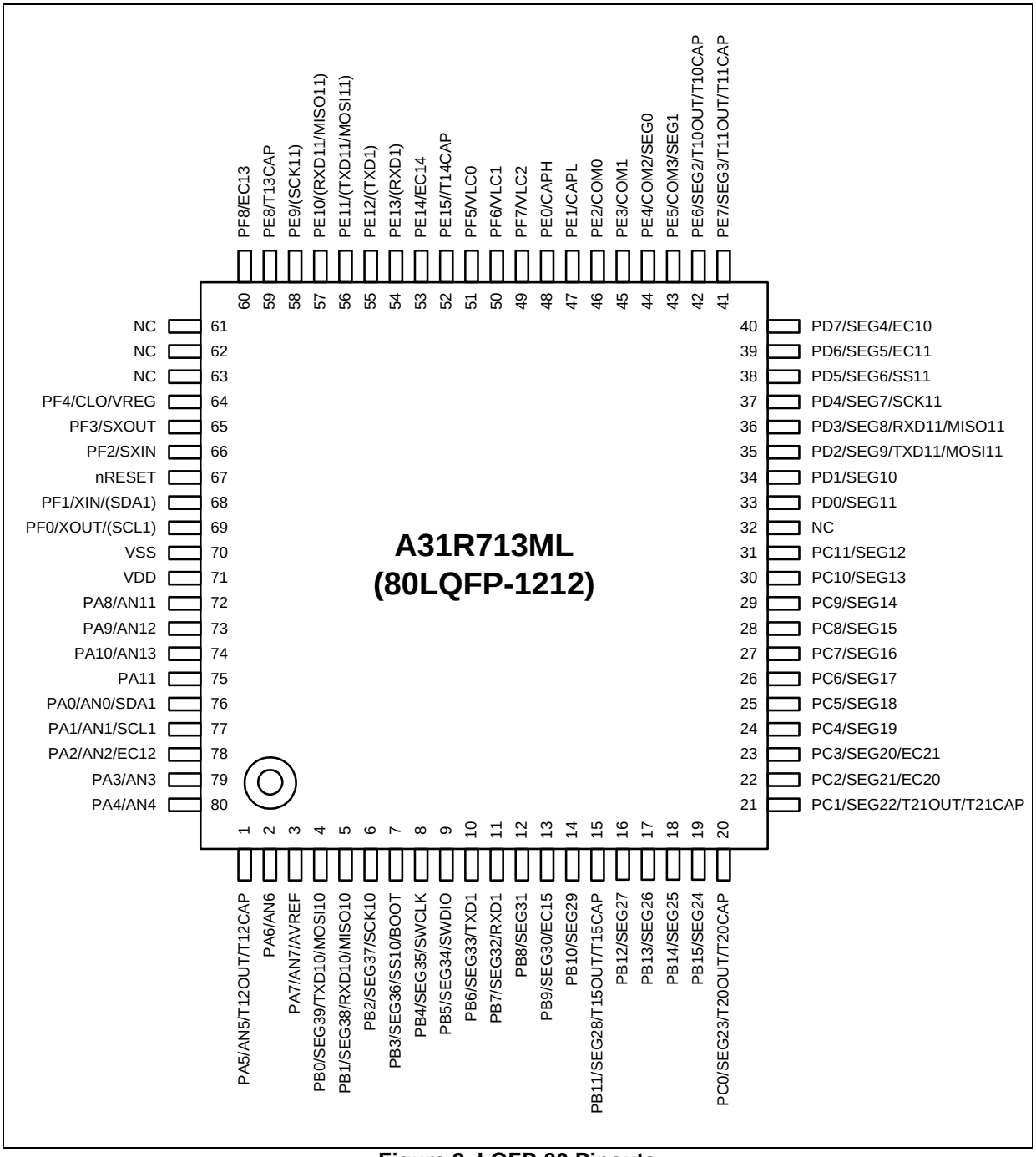
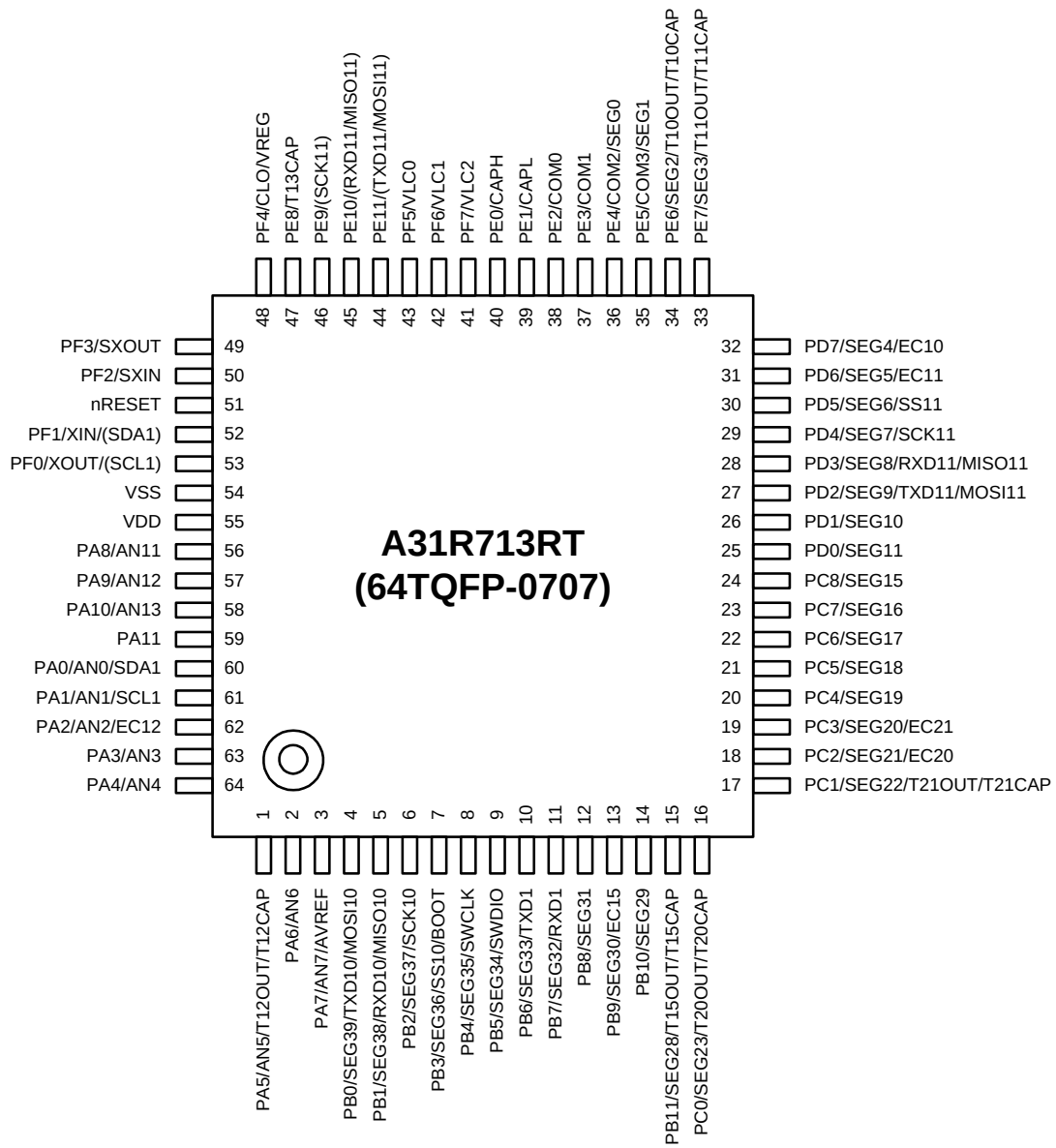
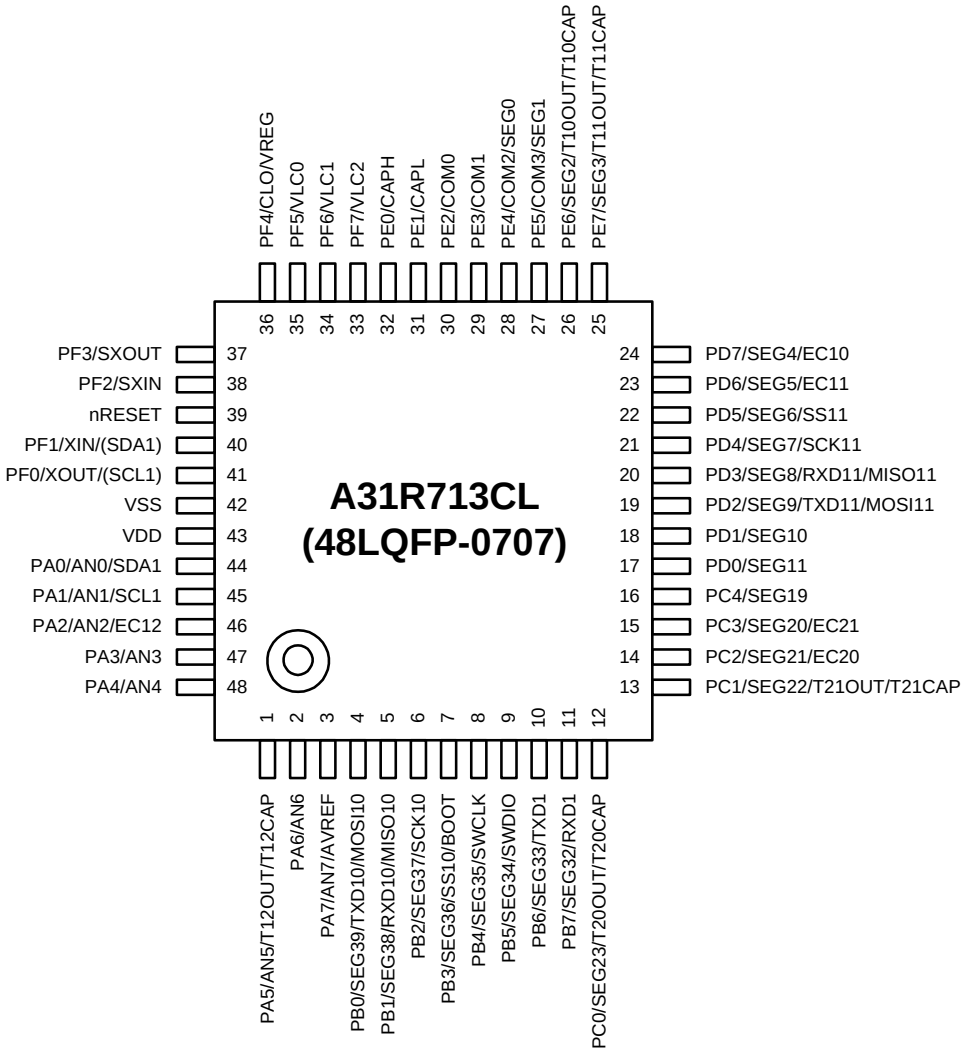


Figure 2. LQFP-80 Pinouts



NOTE: The PB12-PB15, PC9-PC11, PE12-PE15 and PF8 pins should be selected as a push-pull output or an input with pull-up or pull-down resistor by software control when the 64-pin package is used.

Figure 3. TQFP-64 Pinouts



NOTE: The PA8-PA11, PB8-PB15, PC5-PC11, PE8-PE15 and PF8 pins should be selected as a push-pull output or an input with pull-up or pull-down resistor by software control when the 48-pin package is used.

Figure 4. LQFP-48 Pinouts

2.2 Pin description

Table 3 shows pin configuration containing one pair of power/ground and other dedicated pins. Multi-function pins have up to five selections of functions including GPIO.

Table 3. Pin Description

Pin number			Pin name	Type	Description	Remark
LQFP-80	TQFP-64	LQFP-48				
1	1	1	PA5*	IOUDS	PORT A Bit 5 Input/Output	
			AN5	IA	A/D Converter Analog Input 5	
			T12OUT	O	Timer 12 Pulse Output	
			T12CAP	I	Timer 12 Capture Input	
2	2	2	PA6*	IOUDS	PORT A Bit 6 Input/Output	
			AN6	IA	A/D Converter Analog Input 6	
3	3	3	PA7*	IOUDS	PORT A Bit 7 Input/Output	
			AN7	IA	A/D Converter Analog Input 7	
			AVREF	IA	A/D Converter Reference Input	
4	4	4	PB0*	IOUDS	PORT B Bit 0 Input/Output	
			SEG39	O	LCD Segment Signal Output	
			TXD10	O	UART Data Output	
			MOSI10	I/O	SPI Master Output, Slave Input	
5	5	5	PB1*	IOUDS	PORT B Bit 1 Input/Output	
			SEG38	O	LCD Segment Signal Output	
			RXD10	I	UART Data Input	
			MISO10	I/O	SPI Master Input, Slave Output	
6	6	6	PB2*	IOUDS	PORT B Bit 2 Input/Output	
			SEG37	O	LCD Segment Signal Output	
			SCK10	I/O	SPI Clock Input/Output	
7	7	7	PB3	IOUDS	PORT B Bit 3 Input/Output	
			SEG36	O	LCD Segment Signal Output	
			SS10	I	SPI Slave Select Input	
			BOOT*	I	Boot Mode Selection Input	Pull-up
8	8	8	PB4	IOUDS	PORT B Bit 4 Input/Output	
			SEG35	O	LCD Segment Signal Output	
			SWCLK*	I	SWD Clock Input	Pull-down
9	9	9	PB5	IOUDS	PORT B Bit 5 Input/Output	
			SEG34	O	LCD Segment Signal Output	
			SWDIO*	I/O	SWD Data Input/Output	Pull-up
10	10	10	PB6*	IOUDS	PORT B Bit 6 Input/Output	
			SEG33	O	LCD Segment Signal Output	
			TXD1	O	UART Data Output	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
LQFP-80	TQFP-64	LQFP-48				
11	11	11	PB7*	IOUDS	PORT B Bit 7 Input/Output	
			SEG32	O	LCD Segment Signal Output	
			RXD1	I	UART Data Input	
12	12	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
			SEG31	O	LCD Segment Signal Output	
13	13	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
			SEG30	O	LCD Segment Signal Output	
			EC15	I	Timer 15 Event Count Input	
14	14	-	PB10*	IOUDS	PORT B Bit 10 Input/Output	
			SEG29	O	LCD Segment Signal Output	
15	15	-	PB11*	IOUDS	PORT B Bit 11 Input/Output	
			SEG28	O	LCD Segment Signal Output	
			T15OUT	O	Timer 15 Pulse Output	
			T15CAP	I	Timer 15 Capture Input	
16	-	-	PB12*	IOUDS	PORT B Bit 12 Input/Output	
			SEG27	O	LCD Segment Signal Output	
17	-	-	PB13*	IOUDS	PORT B Bit 13 Input/Output	
			SEG26	O	LCD Segment Signal Output	
18	-	-	PB14*	IOUDS	PORT B Bit 14 Input/Output	
			SEG25	O	LCD Segment Signal Output	
19	-	-	PB15*	IOUDS	PORT B Bit 15 Input/Output	
			SEG24	O	LCD Segment Signal Output	
20	16	12	PC0*	IOUDS	PORT C Bit 0 Input/Output	
			SEG23	O	LCD Segment Signal Output	
			T20OUT	O	Timer 20 Pulse Output	
			T20CAP	I	Timer 20 Capture Input	
21	17	13	PC1*	IOUDS	PORT C Bit 1 Input/Output	
			SEG22	O	LCD Segment Signal Output	
			T21OUT	O	Timer 21 Pulse Output	
			T21CAP	I	Timer 21 Capture Input	
22	18	14	PC2*	IOUDS	PORT C Bit 2 Input/Output	
			SEG21	O	LCD Segment Signal Output	
			EC20	I	Timer 20 Event Count Input	
23	19	15	PC3*	IOUDS	PORT C Bit 3 Input/Output	
			SEG20	O	LCD Segment Signal Output	
			EC21	I	Timer 21 Event Count Input	
24	20	16	PC4*	IOUDS	PORT C Bit 4 Input/Output	
			SEG19	O	LCD Segment Signal Output	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
LQFP-80	TQFP-64	LQFP-48				
25	21	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
			SEG18	O	LCD Segment Signal Output	
26	22	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
			SEG17	O	LCD Segment Signal Output	
27	23	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
			SEG16	O	LCD Segment Signal Output	
28	24	-	PC8*	IOUDS	PORT C Bit 8 Input/Output	
			SEG15	O	LCD Segment Signal Output	
29	-	-	PC9*	IOUDS	PORT C Bit 9 Input/Output	
			SEG14	O	LCD Segment Signal Output	
30	-	-	PC10*	IOUDS	PORT C Bit 10 Input/Output	
			SEG13	O	LCD Segment Signal Output	
31	-	-	PC11*	IOUDS	PORT C Bit 11 Input/Output	
			SEG12	O	LCD Segment Signal Output	
32			NC	-	-	
33	25	17	PD0*	IOUDS	PORT D Bit 0 Input/Output	
			SEG11	O	LCD Segment Signal Output	
34	26	18	PD1*	IOUDS	PORT D Bit 1 Input/Output	
			SEG10	O	LCD Segment Signal Output	
35	27	19	PD2*	IOUDS	PORT D Bit 2 Input/Output	
			SEG9	O	LCD Segment Signal Output	
			TXD11	O	UART Data Output	
			MOSI11	I/O	SPI Master Output, Slave Input	
36	28	20	PD3*	IOUDS	PORT D Bit 3 Input/Output	
			SEG8	O	LCD Segment Signal Output	
			RXD11	I	UART Data Input	
			MISO11	I/O	SPI Master Input, Slave Output	
37	29	21	PD4*	IOUDS	PORT D Bit 4 Input/Output	
			SEG7	O	LCD Segment Signal Output	
			SCK11	I/O	SPI Clock Input/Output	
38	30	22	PD5*	IOUDS	PORT D Bit 5 Input/Output	
			SEG6	O	LCD Segment Signal Output	
			SS11	I	SPI Slave Select Input	
39	31	23	PD6*	IOUDS	PORT D Bit 6 Input/Output	
			SEG5	O	LCD Segment Signal Output	
			EC11	I	Timer 11 Event Count Input	
40	32	24	PD7*	IOUDS	PORT D Bit 7 Input/Output	
			SEG4	O	LCD Segment Signal Output	
			EC10	I	Timer 10 Event Count Input	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
LQFP-80	TQFP-64	LQFP-48				
41	33	25	PE7*	IOUDS	PORT E Bit 7 Input/Output	
			SEG3	O	LCD Segment Signal Output	
			T11OUT	O	Timer 11 Pulse Output	
			T11CAP	I	Timer 11 Capture Input	
42	34	26	PE6*	IOUDS	PORT E Bit 6 Input/Output	
			SEG2	O	LCD Segment Signal Output	
			T10OUT	O	Timer 10 Pulse Output	
			T10CAP	I	Timer 10 Capture Input	
43	35	27	PE5*	IOUDS	PORT E Bit 5 Input/Output	
			COM3	O	LCD Common Signal Output	
			SEG1	O	LCD Segment Signal Output	
44	36	28	PE4*	IOUDS	PORT E Bit 4 Input/Output	
			COM2	O	LCD Common Signal Output	
			SEG0	O	LCD Segment Signal Output	
45	37	29	PE3*	IOUDS	PORT E Bit 3 Input/Output	
			COM1	O	LCD Common Signal Output	
46	38	30	PE2*	IOUDS	PORT E Bit 2 Input/Output	
			COM0	O	LCD Common Signal Output	
47	39	31	PE1*	IOUDS	PORT E Bit 1 Input/Output	
			CAPL	O	Capacitor terminal for voltage booster	
48	40	32	PE0*	IOUDS	PORT E Bit 0 Input/Output	
			CAPH	O	Capacitor terminal for voltage booster	
49	41	33	PF7*	IOUDS	PORT F Bit 7 Input/Output	
			VLC2	I/O	LCD bias voltage pin	
50	42	34	PF6*	IOUDS	PORT F Bit 6 Input/Output	
			VLC1	I/O	LCD bias voltage pin	
51	43	35	PF5*	IOUDS	PORT F Bit 5 Input/Output	
			VLC0	I/O	LCD bias voltage pin	
52	-	-	PE15*	IOUDS	PORT E Bit 15 Input/Output	
			T14CAP	I	Timer 14 Capture Input	
53	-	-	PE14*	IOUDS	PORT E Bit 14 Input/Output	
			EC14	I	Timer 14 Event Count Input	
54	-	-	PE13*	IOUDS	PORT E Bit 13 Input/Output	
			(RXD1)	I	UART Data Input	
55	-	-	PE12*	IOUDS	PORT E Bit 12 Input/Output	
			(TXD1)	O	UART Data Output	
56	44	-	PE11*	IOUDS	PORT E Bit 11 Input/Output	
			(TXD11)	O	UART Data Output	
			(MOSI11)	I/O	SPI master output, slave input	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
LQFP-80	TQFP-64	LQFP-48				
57	45	-	PE10*	IOUDS	PORT E Bit 10 Input/Output	
			(RXD11)	I	UART Data Input	
			(MISO11)	I/O	SPI master input, slave output	
58	46	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
			SCK11	I/O	SPI clock input/output	
59	47	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
			T13CAP	I	Timer 13 Capture Input	
60	-	-	PF8*	IOUDS	PORT F Bit 8 Input/Output	
			EC13	I	Timer 13 Event Count Input	
61	-	-	NC	-	-	
62	-	-	NC	-	-	
63	-	-	NC	-	-	
64	48	36	PF4*	IOUDS	PORT F Bit 4 Input/Output	
			CLKO	O	System Clock Output	
			VREG	O	Regulator voltage output for sub clock. 0.1uF capacitor needed	
65	49	37	PF3*	IOUDS	PORT F Bit 3 Input/Output	
			SXOUT	O	Sub Oscillator Output	
66	50	38	PF2*	IOUDS	PORT F Bit 2 Input/Output	
			SXIN	I	Sub Oscillator Input	
67	51	39	nRESET	Input	External Reset Input	Pull-up
68	52	40	PF1*	IOUDS	PORT F Bit 1 Input/Output	
			XIN	I	Main Oscillator Input	
			(SDA1)	I/O	I2C Data Input/Output	
69	53	41	PF0*	IOUDS	PORT F Bit 0 Input/Output	
			XOUT	O	Main Oscillator Output	
			(SCL1)	I/O	I2C Clock Input/Output	
70	54	42	VSS	P	Ground	
71	55	43	VDD	P	VDD	
72	56	-	PA8*	IOUDS	PORT A Bit 8 Input/Output	
			AN11	IA	A/D Converter Analog Input 11	
73	57	-	PA9*	IOUDS	PORT A Bit 9 Input/Output	
			AN12	IA	A/D Converter Analog Input 12	
74	58	-	PA10*	IOUDS	PORT A Bit 10 Input/Output	
			AN13	IA	A/D Converter Analog Input 13	
75	59	-	PA11*	IOUDS	PORT A Bit 11 Input/Output	
76	60	44	PA0*	IOUDS	PORT A Bit 0 Input/Output	
			AN0	IA	A/D Converter Analog Input 0	
			SDA1	I/O	I2C Data Input/Output	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
LQFP-80	TQFP-64	LQFP-48				
77	61	45	PA1*	IOUDS	PORT A Bit 1 Input/Output	
			AN1	IA	A/D Converter Analog Input 1	
			SCL1	I/O	I2C Clock Input/Output	
78	62	46	PA2*	IOUDS	PORT A Bit 2 Input/Output	
			AN2	IA	A/D Converter Analog Input 2	
			EC12	I	Timer 12 Event Count Input	
79	63	47	PA3*	IOUDS	PORT A Bit 3 Input/Output	
			AN3	IA	A/D Converter Analog Input 3	
80	64	48	PA4*	IOUDS	PORT A Bit 4 Input/Output	
			AN4	IA	A/D Converter Analog Input 4	

NOTES:

1. *Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. (*) Selected pin function after reset condition
3. Pin order may be changed with revision notice.

3 System and memory overview

Main system and memory of A31R713 consist of the followings:

- ARM® Cortex® -M0+ core
- Internal SRAM
- Internal Flash memory
- AHB (Advanced High Performance Bus) and APB (Advanced Peripheral Bus)

3.1 Cortex®–M0+ core

The Cortex-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

Please refer to the technical reference manual “ARM DDI 0484C” provided by ARM for detail information of Cortex-M0+.

3.2 Interrupt controller

The Cortex-M0+ process has embedded an interrupt controller named NVIC (Nested Vector Interrupt Controller). A31R713 has additional interrupt control block for controlling 28 interrupt sources generated by internal peripherals.

To use interrupts from internal peripherals, both the NVIC and the interrupt control block must be configured properly. This document describes only the peripheral interrupt controller. For more information about NVIC inside the Cortex-M0+ processor, please refer to the technical reference manual “ARM DDI 0484C” in ARM technical document site.

Table 4. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Exception
-13	0x0000_000C	Hard Fault Exception
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
-5	0x0000_002C	SVCall Exception
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Exception
-1	0x0000_003C	SysTick Exception
0	0x0000_0040	LVI Interrupt
1	0x0000_0044	WUT Interrupt
2	0x0000_0048	WDT Interrupt
3	0x0000_004C	EINT0 Interrupt
4	0x0000_0050	EINT1 Interrupt
5	0x0000_0054	EINT2 Interrupt
6	0x0000_0058	EINT3 Interrupt
7	0x0000_005C	TIMER10 Interrupt
8	0x0000_0060	TIMER11 Interrupt
9	0x0000_0064	TIMER12 Interrupt
10	0x0000_0068	Reserved
11	0x0000_006C	USART10 Interrupt
12	0x0000_0070	WT Interrupt
13	0x0000_0074	Reserved
14	0x0000_0078	I2C1 Interrupt
15	0x0000_007C	TIMER20 Interrupt
16	0x0000_0080	TIMER21 Interrupt
17	0x0000_0084	USART11 Interrupt
18	0x0000_0088	ADC Interrupt
19	0x0000_008C	Reserved
20	0x0000_0090	UART1 Interrupt

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
21	0x0000_0094	TIMER13 Interrupt
22	0x0000_0098	TIMER14 Interrupt
23	0x0000_009C	TIMER15 Interrupt
24	0x0000_00A0	Reserved
25	0x0000_00A4	
26	0x0000_00A8	
27	0x0000_00AC	
28	0x0000_00B0	
29	0x0000_00B4	
30	0x0000_00B8	
31	0x0000_00BC	

3.3 Boot mode

Boot mode pins

A31R713 has a Boot mode to program the internal flash memory. The Boot mode will be activated by setting a BOOT pin to “Low” level at reset timing (Normal operation mode is “High” level).

The Boot mode supports either UART boot or SPI boot. For the UART boot, TXD10/RXD10 ports are used. For the SPI boot, MOSI10/MISO10/SCK10/SS10 ports are used.

Table 5 introduces pins used in the Boot mode.

Table 5. Boot Mode Pin List

Block	Pin Name	Direction	Description
SYSTEM	nRESET	I	Reset Input signal
	BOOT/PB3	I	‘0’ to enter Boot mode
UART mode of USART10	RXD10/PB1	I	UART Boot Receive Data
	TXD10/PB0	O	UART Boot Transmit Data
SPI mode of USART10	SS10/PB3	I	SPI Boot Slave Selectable after Boot ROM
	SCK10/PB2	I	SPI Boot Clock Input
	MISO10/PB1	I	SPI Boot Data Input with function exchange
	MOSI10/PB0	O	SPI Boot Data Output with function exchange

Boot mode connection

A user can design target boards using any of Boot mode ports – UART or SPI mode of USART10. Examples of connection diagrams in the Boot mode are introduced in figures 5 and 6.

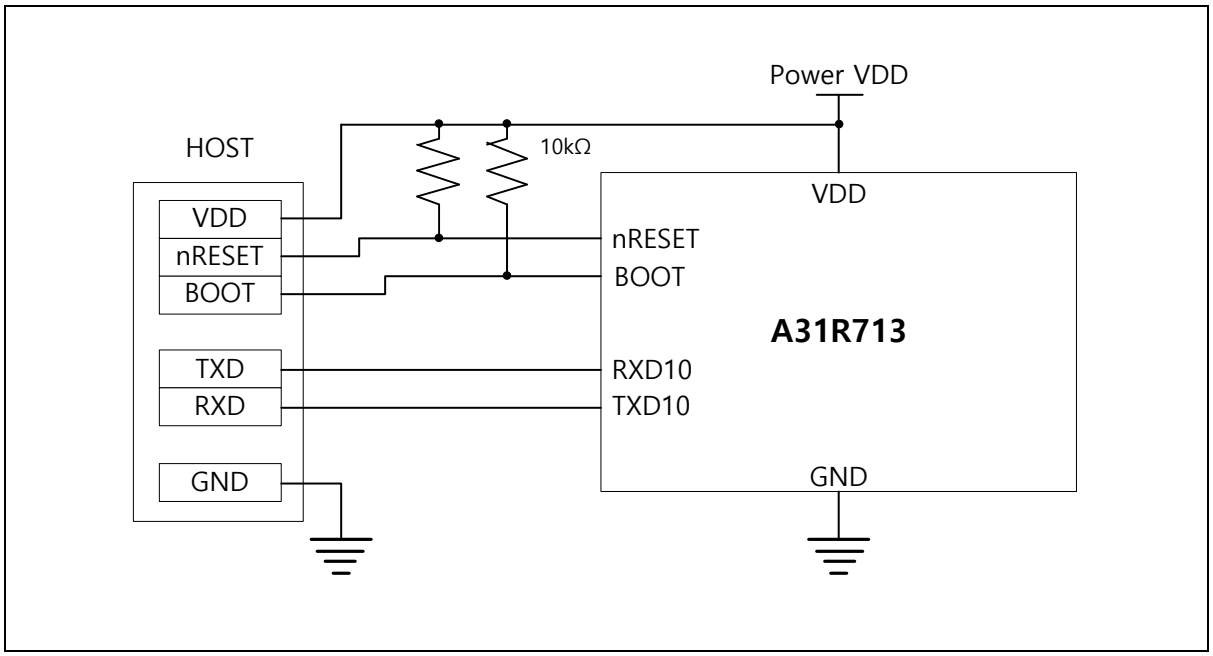


Figure 5. Connection Diagram of UART Boot

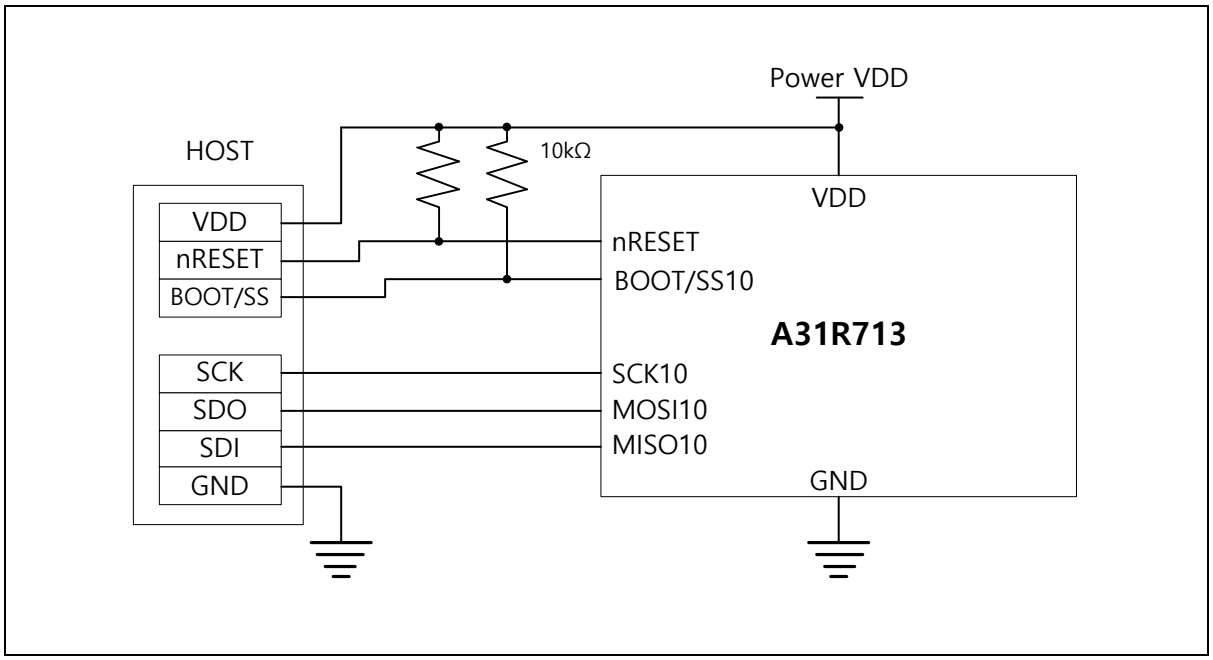


Figure 6. Connection Diagram of SPI Boot

3.4 SWD debug mode and E-PGM+ connection

Connections for SWD debugger interface or E-PGM+ is described in figure 7.

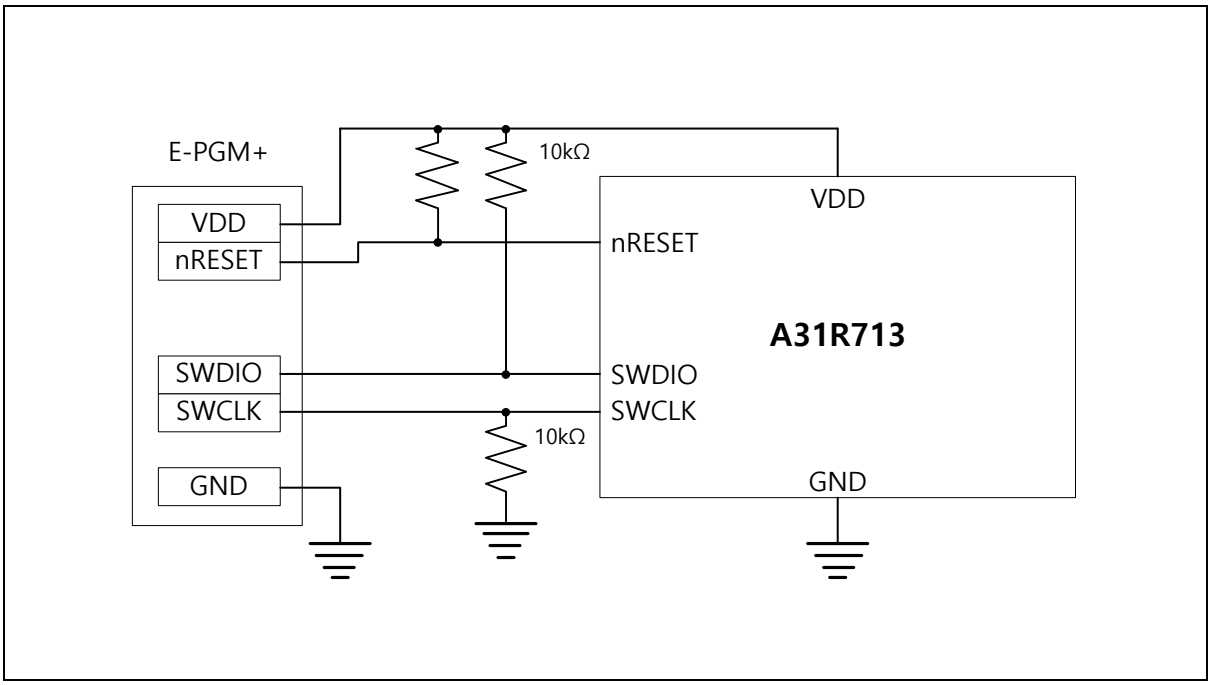
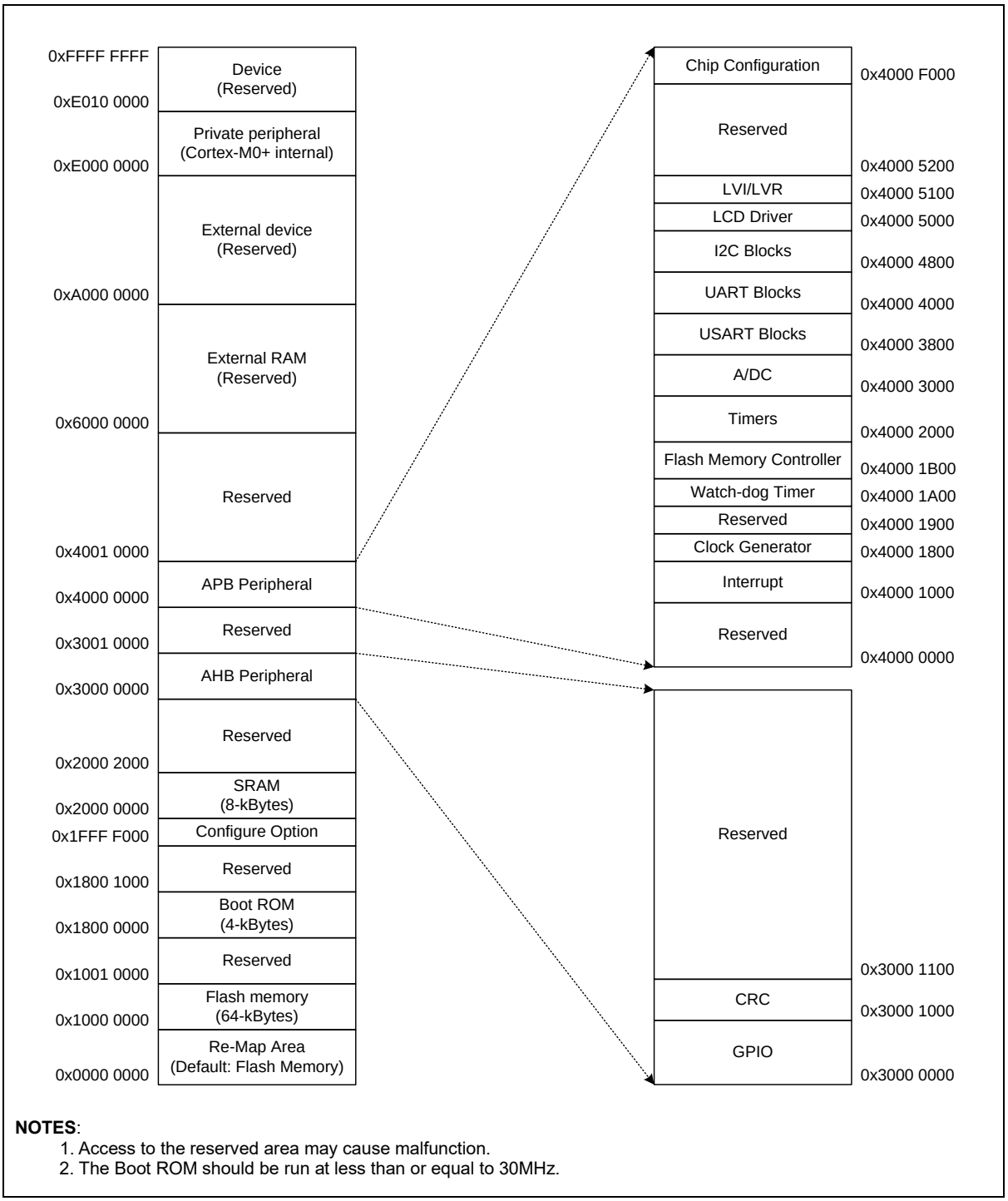


Figure 7. Connection between A31R713 and E-PGM+ using SWD Debugger Interface

3.5 Memory organization

3.5.1 Memory map

Figure 8 shows addressable memory space in memory map.



NOTES:
1. Access to the reserved area may cause malfunction.
2. The Boot ROM should be run at less than or equal to 30MHz.

Figure 8. Main Memory Map

3.5.2 Internal SRAM

A31R713 has a block of 0-wait on-chip SRAM. Its size is 8KB, and its base address is 0x2000_0000. The SRAM's memory area is mainly for data memory and stack memory. It is possible to locate code area in the SRAM memory for fast operation or for flash erase or program operation for self-program.

This device does not support memory remapping. So jump and return is required to process the code in SRAM memory area.

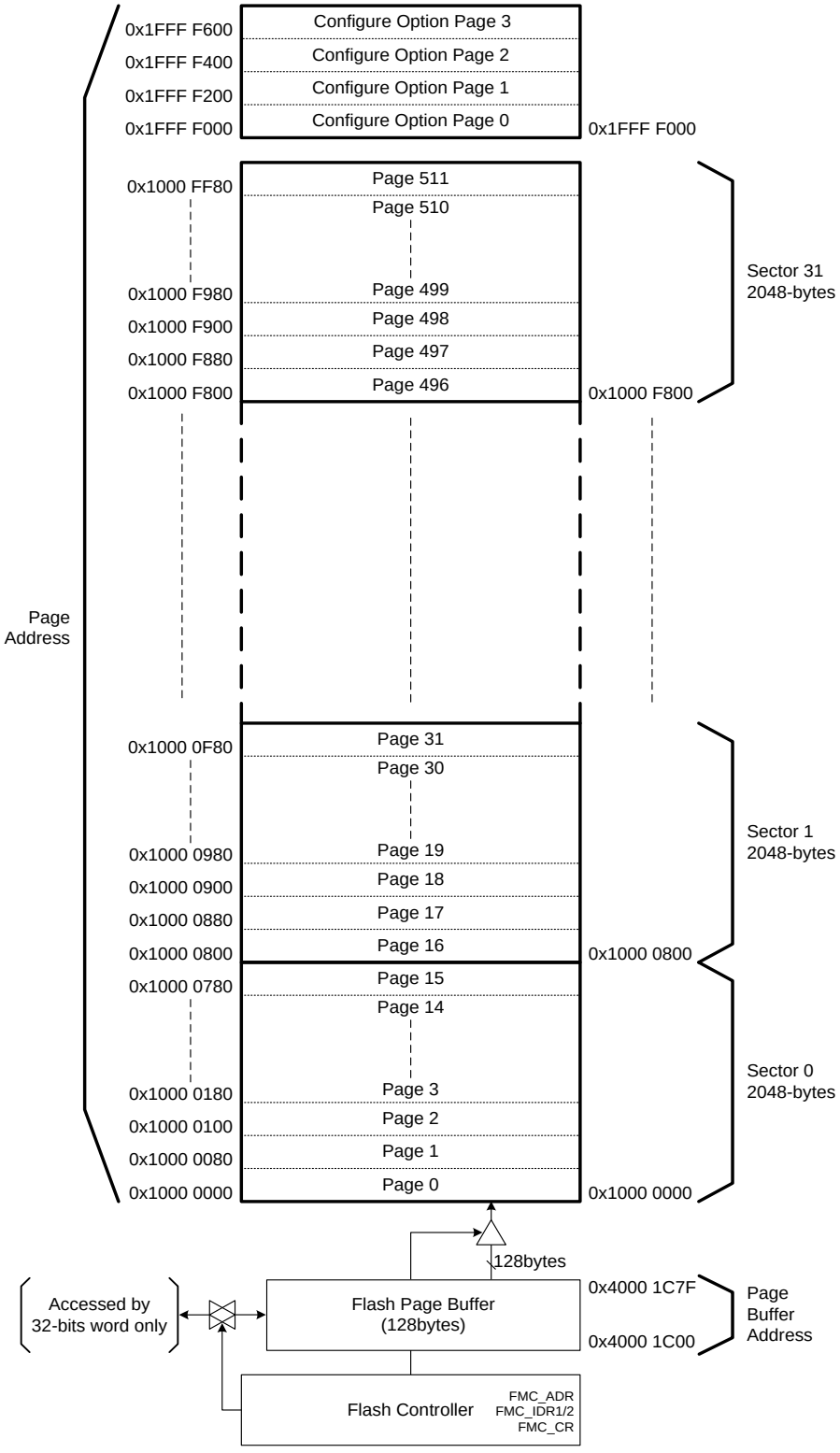
3.5.3 Flash memory

A31R713 has an internal flash memory featuring the followings:

- 64KB Flash code memory
- 32-bit read data bus width
- 128-byte page size
- Page erase and bulk erase available
- 128-byte unit program

Table 6. Internal Flash Memory Specification

Item	Description
Size	64KB
Start address	0x1000_0000
End address	0x1000_FFFF
Page size	128-byte
Total page count	512 pages
PGM unit	128-byte
Erase unit	128-byte or bulk



NOTES:

1. If any instruction other than 32-bit is used to write data to the buffer, wrong data will be written.
2. Each configure option page0/1/2/3 has 128bytes respectively.

Figure 9. Internal Flash Memory Block Diagram

3.5.4 Configure option area

Configuration option area of A31R713 is used for system related trimming values, user option, and user data. The configure option area consists of four pages in the flash memory, which can be erased and written by the flash memory controller. This area can be read by any instruction.

The four pages of the configuration option area are listed in the followings:

- Page 0: System related trimming values
- Page 1: User option for read protection, watchdog timer, and LVR voltage level configurations
- Page 2: User data 0 area
- Page 3: User data 1 area

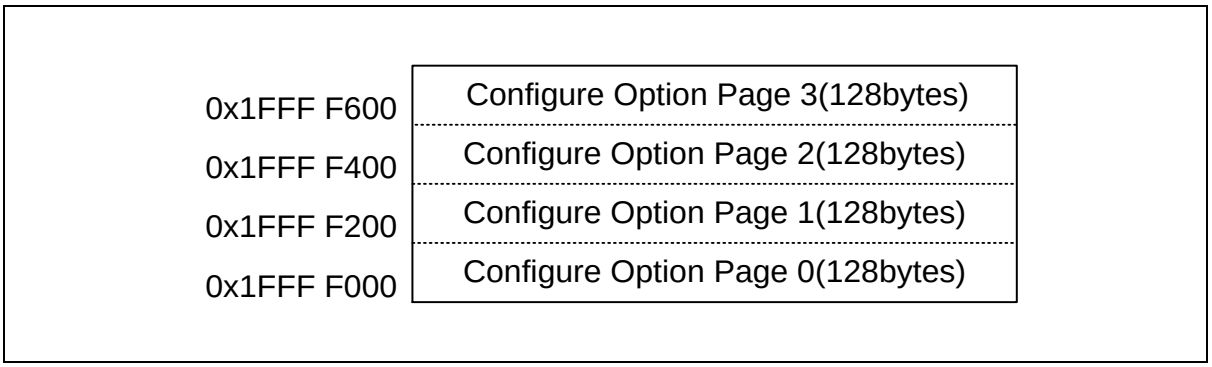


Figure 10. Configure Option Area Structure

Configuration option page

Base address of the configuration option area ranges from 0x1FFF_F000 to 0x1FFF_F600. The area map is shown in Table 7.

Table 7. Configuration Option Area Map

Page	NAME	ADDRESS	DESCRIPTION
0	-	0x1FFF_F000 to 0x1FFF_F07F	System Trimming Values
1	CONF_RPCNFIG	0x1FFF_F200	Configuration for Read Protection
	CONF_WDTCNFIG	0x1FFF_F20C	Configuration for Watch-Dog Timer
	CONF_LVRCNFIG	0x1FFF_F210	Configuration for Low Voltage Reset
	CONF_CNFIGWTP1	0x1FFF_F214	Erase/Write Protection for Configure Option Page 1/2/3
	CONF_FMWTP1	0x1FFF_F240	Erase/Write Protection for Flash Memory
2	**-**	0x1FFF_F400 to 0x1FFF_F47F	User Data Area 0
3	**-**	0x1FFF_F600 to 0x1FFF_F67F	User Data Area 1

4 SCU (System Control Unit)

A31R713 has a built-in intelligent power control block, which manages analog blocks and operating modes. Internal reset and clock signals are controlled by SCU block to maintain optimized system performance and power dissipation.

4.1 SCU block diagram

Figure 11 shows the SCU block diagram.

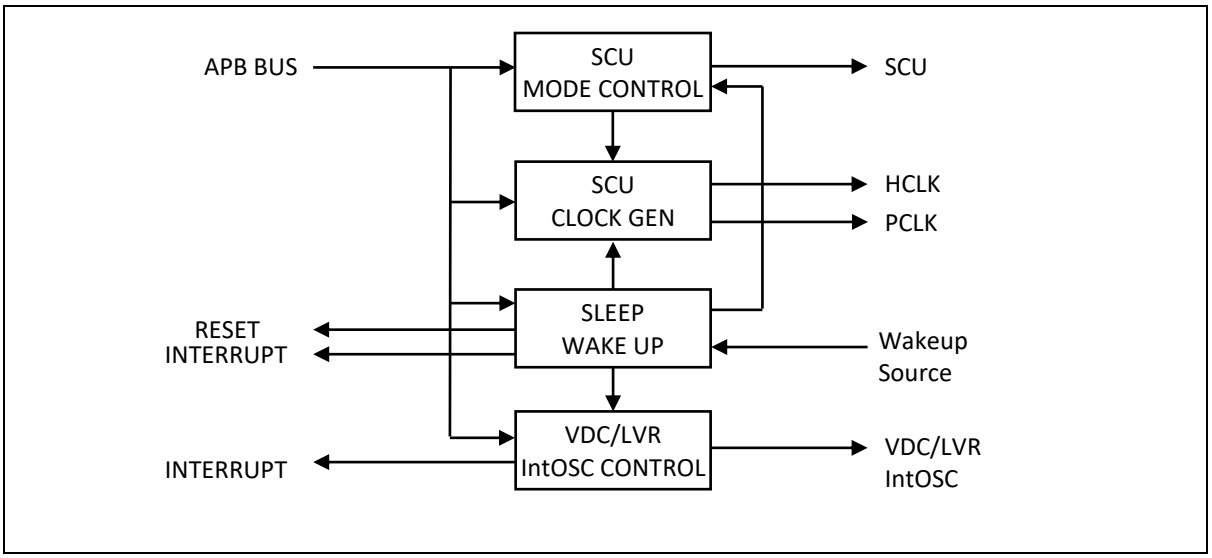


Figure 11. SCU Block Diagram

4.2 Clock system

A31R713 has two main operating clocks. One is HCLK, which supplies the clock to the CPU and AHB bus system. The other one is PCLK, which supplies the clock to the peripheral systems.

Users can control the clock system variation by software. Figure 12 shows the clock system of A31R713 and Table 8 shows the descriptions for clock sources.

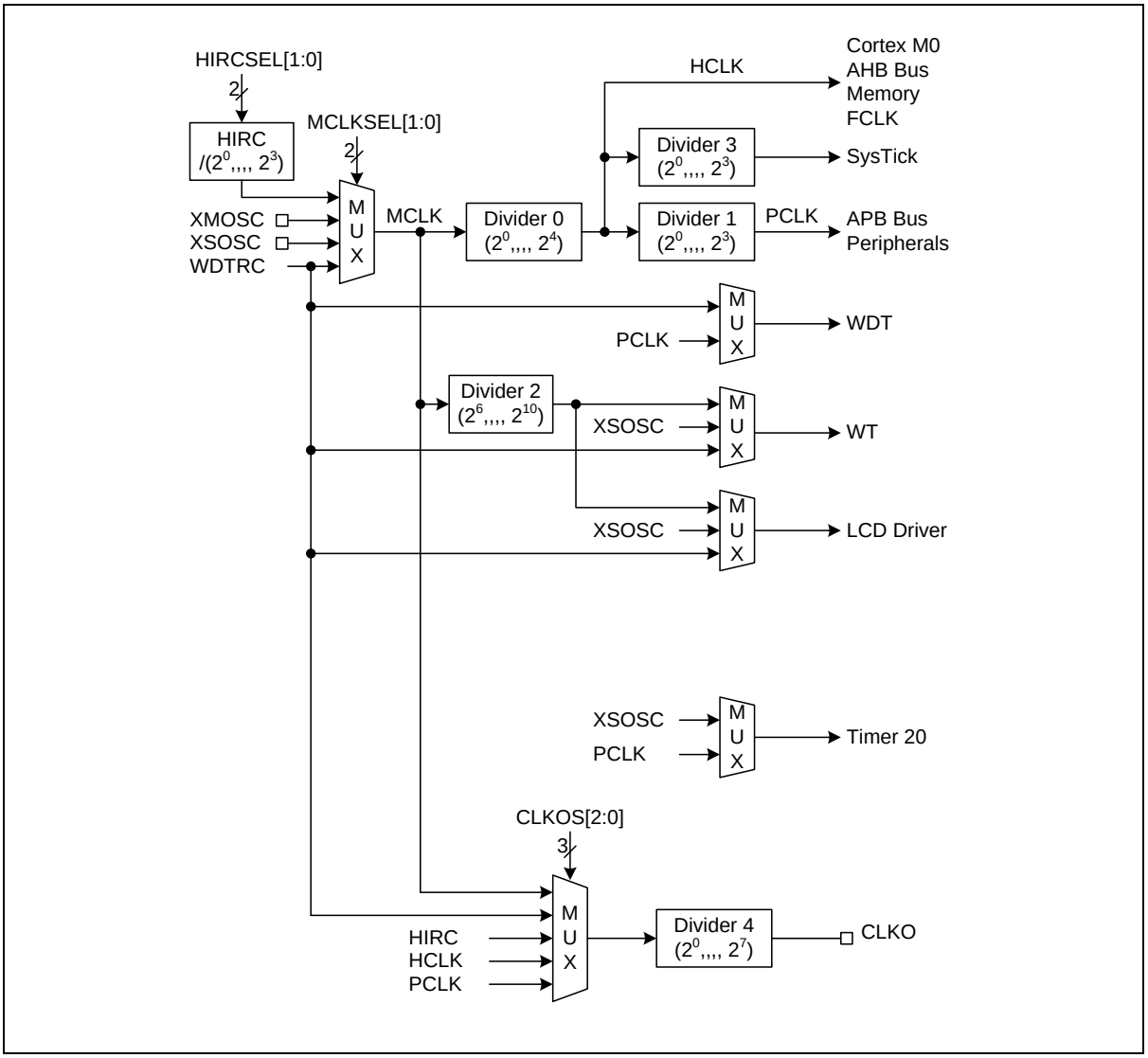


Figure 12. Clock Source Configuration

Each mux to switch clock source has a glitch-free circuit. So a clock can be switched without glitch risks. When you change the clock mux control, be sure both clock sources are alive. If either is not alive, clock change operation stops and system will shut down and not recover.

Table 8. Clock Sources

Clock name	Mnemonic	Frequency	Description
Main OSC	XMOSC	• X-TAL (2MHz to 16MHz) • External Clock (2MHz to 40MHz)	• External Main Crystal OSC • External Main Clock
Sub OSC	XSOSC	X-TAL (32.768kHz)	External Sub Crystal OSC
Internal RC OSC	HIRC	2.5MHz to 40MHz	High Frequency Internal RC OSC
WDT RC OSC	WDTRC	40kHz	Watchdog Timer RC OSC

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks, FCLK and HCLK. FCLK is a free running clock and is always running except during power down mode. HCLK can be stopped during sleep mode.

The HCLK clock operates the BUS system and memory systems. Max BUS operating clock speed is 40MHz. HCLK frequency should be limited to a frequency of 40MHz or lower.

4.2.2 Miscellaneous clock domain

Various clock sources are required for each functional block. The SCU provides clock source selectivity with dedicated pre-scaler for each functional block. The clock selection mux does not support glitch-free function, so the clock is unpredictable during clock selection. Figure 13 shows the configurations for miscellaneous clocks.

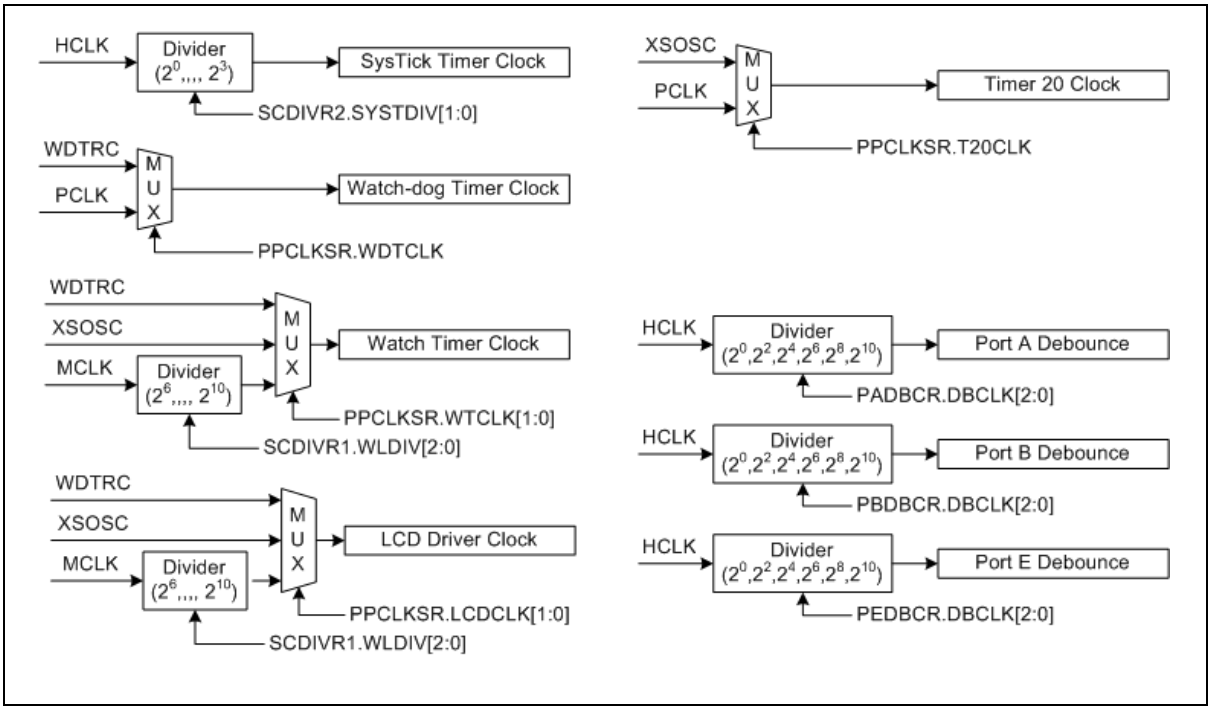


Figure 13. Miscellaneous Clock Configuration

4.2.3 PCLK clock domain

PCLK is the master clock for all the peripherals except for the CRC generator and ports. It can shut down during power down mode. Each peripheral clock is generated by SCU_PPCLKEN1 and SCU_PPCLKEN2 register set. Figure 12 illustrates the PCLK clock distributions. The peripherals are not accessible even by reading its registers until each PCLK clock of each block is enabled.

4.2.4 Clock configuration procedure

After power on the device, a default system clock is generated by HIRC (2.5MHz) clock. The HIRC is enabled by default during power up sequence. Other clock sources are enabled by user controls and configuration options with a system clock.

XMOSC and XSOSC clocks are enabled by XMOSCEN and XSOSCEN bits of SCU_CLKSRCR register respectively. Before enabling XMOSC and XSOSC blocks, the pin mux configuration should be set for XIN/XOUT and SXIN/SXOUT/VREG functions. PF0/PF1 and PF2/PF3/PF4 pins are shared by XMOSC's XIN/XOUT function and XSOSC's SXIN/SXOUT/VREG function – PF_MOD and PF_AFSR1 registers should be configured properly.

After enabling the XMOSC and XSOSC blocks, a user can check stability of crystal oscillation through a clock monitoring control register, SCU_CMONCR. It takes more than 1ms to ensure stable crystal oscillation before changing the system clock.

Figure 14 shows an example flow chart to configure the system clock to XMOSC and XSOSC clock.

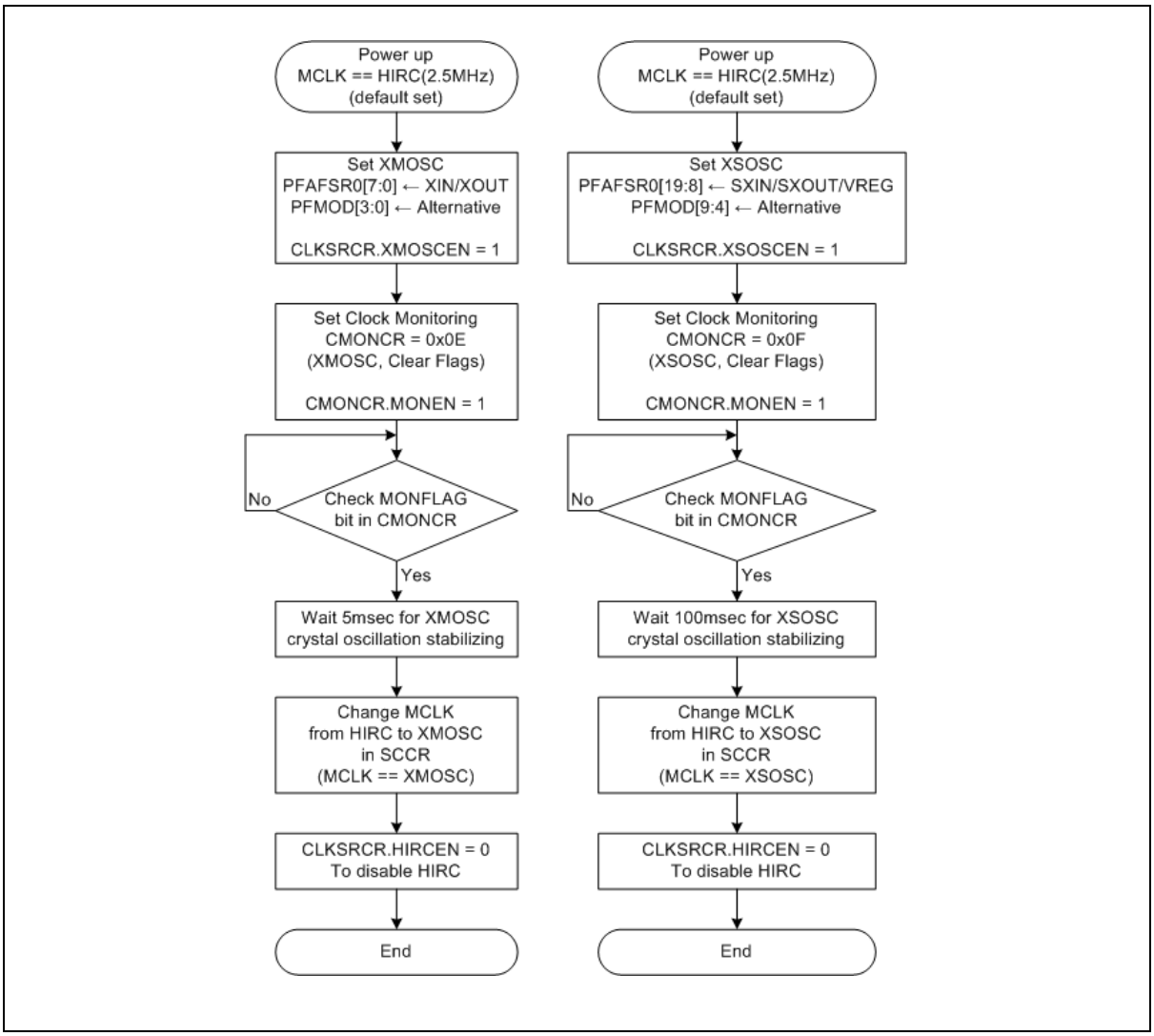


Figure 14. Clock Configuration Procedure

4.3 Reset

A31R713 has two system resets. One is the cold reset by POR, which is effective during power up or down sequence. The other is the warm reset, generated by several reset sources. The reset event makes the device to turn back to its initial state.

The cold reset has only one reset source, which is POR, while the warm reset has several reset sources as shown below:

- nRESET pin
- WDT reset
- LVR reset
- MON reset
- S/W reset
- CPU request reset

4.3.1 Cold reset

The cold reset is one of important feature of the A31R713 when it powers up. This characteristic will globally affect the system boot.

Internal VDC is enabled when VDD power is turned on. Internal VDD level slope follows the External VDD power slope. Internal POR trigger level is at 1.2V of the internal VDC voltage. At this time, boot operation begins.

Internal RC clock turns on and counts 4ms for internal VDC level to stabilize. At this time, external VDD voltage level should be bigger than initial LVR level (1.62V). After 4ms of counting, the CPU reset is released and operation begins.

Figure 15 shows waveform of power up sequence and internal reset.

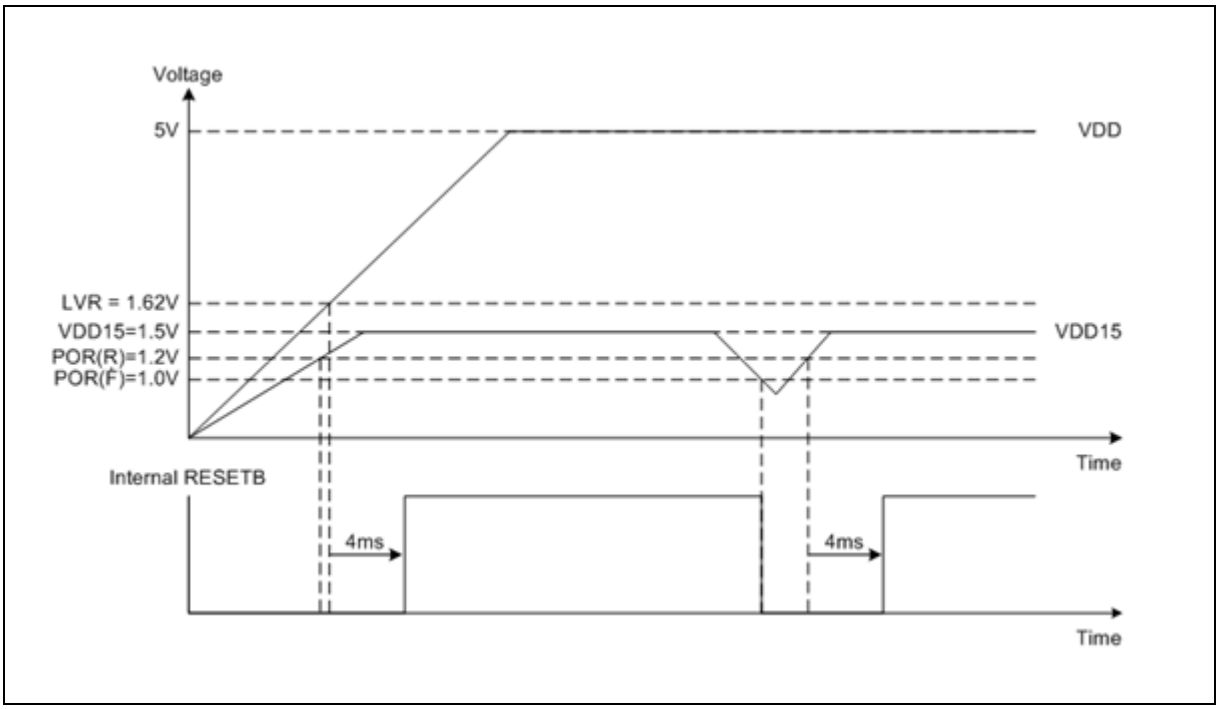


Figure 15. Power-up POR Sequence

A register SCU_RSTSSR shows the POR reset status. The last reset comes from the POR. SCU_RSTSSR.PORSTA is set to '1'. After power on, this bit is always '1' if the bit is not cleared by

S/W. If abnormal internal voltage drop is detected during normal operation, the system will be reset and this bit also will be set to ‘1’.

When the cold reset is applied, the entire device returns to its initial state.

4.3.2 Warm reset

The warm reset event has several reset sources and some parts of the device return to their initial states when the warm reset takes place.

The warm reset status appears in a register SCU_RSTSSR. A reset for each peripheral block is controlled by a register SCU_PPRST. The reset can be masked independently.

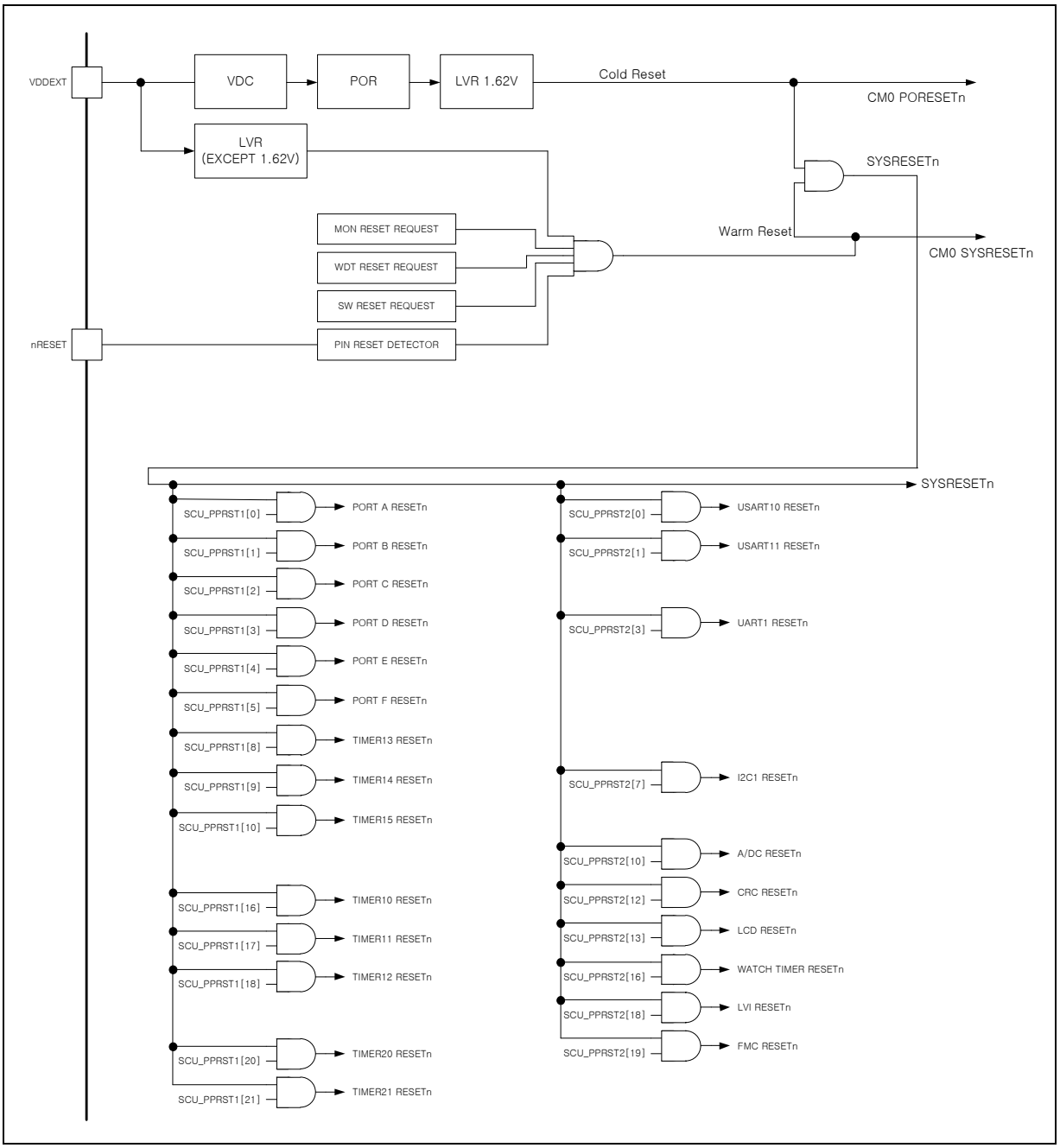


Figure 16. Reset Configuration

4.3.3 LVR reset

The LVR voltage level is set by a low voltage reset configuration register (CONF_LVRCNFIG) in the configuration option page 1.

LVR reset status appears in a register SCU_RSTSSR. The reset for LVR is controlled by a register SCU_LVRCR. The register is cleared to “0x00” on POR reset.

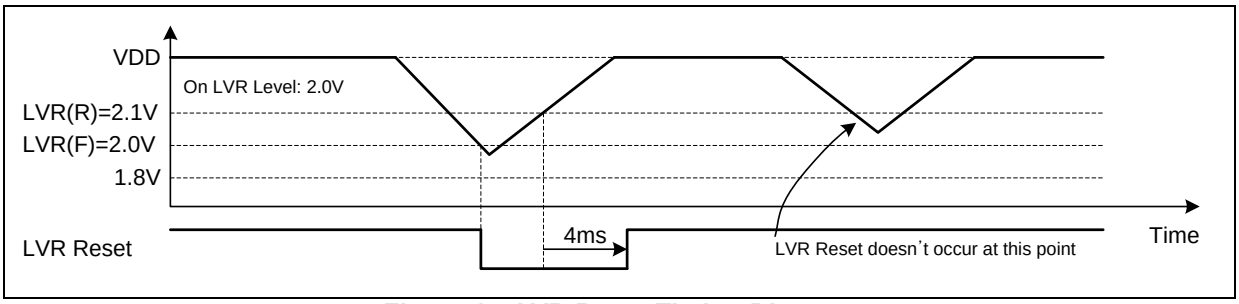


Figure 17. LVR Reset Timing Diagram

4.4 Operation mode

INIT mode is the initial state of the device when reset. At RUN mode, the chip runs at its max CPU performance with a high-speed clock system. At SLEEP and DEEP SLEEP mode, the chip runs at a low power consumption mode. The system saves power by halting the processor core and unused peripherals.

Figure 18 shows the operation mode transition diagram.

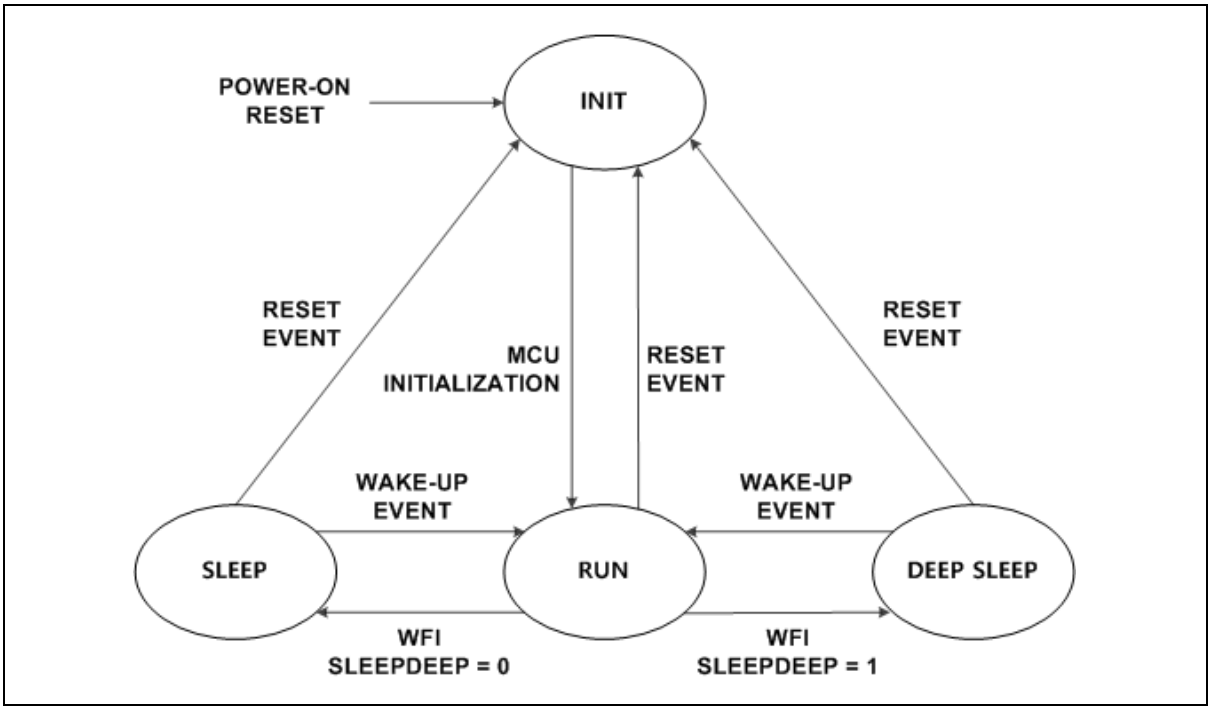


Figure 18. Operating Mode

4.4.1 Run mode

This mode is to operate CPU core and peripheral hardware with a high-speed clock. The device enters in the INIT state after reset, and then enters in the RUN mode.

4.4.2 Sleep mode

The device stops only CPU in this mode. Each peripheral function turns on by a function enable bit and a clock enable bit of the register SCU_PPCLKEN.

4.4.3 Deep sleep mode

The device stops not only CPU but also a selected system clock (MCLK) in this mode. Watch timer with sub clock and watchdog timer with WDTRC still operate in this mode.

Table 9. Functional table on current mode

IP	Main Run (IDD1)	Main Sleep (IDD2)	Sub Run (IDD3)	Sub Sleep (IDD4)	Deep Sleep (IDD5)
CPU	O	X	O	X	X
FLASH	O	X	O	X	X
SRAM	O	X	O	X	X
FMC	Optional	X	Optional	X	X
CRC	Optional	X	Optional	X	X
POR	O	O	O	O	O
LVR/LVI	Optional	Optional	Optional	Optional	Optional
GPIO	Optional	Optional	Optional	Optional	Optional
SCU	O	O	O	O	O
I2C	Optional	Optional	Optional	Optional	X
USART	Optional	Optional	Optional	Optional	Optional
UART	Optional	Optional	Optional	Optional	X
SysTick	Optional	Optional	Optional	Optional	X
T10 – T15	Optional	Optional	Optional	Optional	X
T20	Optional	Optional	Optional	Optional	Optional
T21	Optional	Optional	Optional	Optional	X
WDT	Optional	Optional	Optional	Optional	Optional
WUT	O	O	O	O	X
A/DC	Optional	Optional	X	X	X
LCD Driver	Optional	Optional	Optional	Optional	Optional
WT	Optional	Optional	Optional	Optional	Optional
HIRC	Optional	Optional	X	X	X
WDTRC	Optional	Optional	Optional	Optional	Optional
XMOSC	Optional	Optional	X	X	X
XSOSC	Optional	Optional	Optional	Optional	Optional

NOTES:
1. O: Enable, X: Disable, Optional: A function can be disabled/enabled by s/w.
2. It can be woken up from sleep and deep sleep modes by an interrupt source of the optional peripherals.

4.5 Pin description for SCU

Table 10. Pins and External Signals for SCU

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator for Main Clock
SXIN/SXOUT	OSC	External Crystal Oscillator for Sub Clock
VREG	O	Regulator voltage output for sub clock. 0.1uF capacitor needed
CLKO	O	Clock Output Monitoring Signal

5 PCU and GPIO

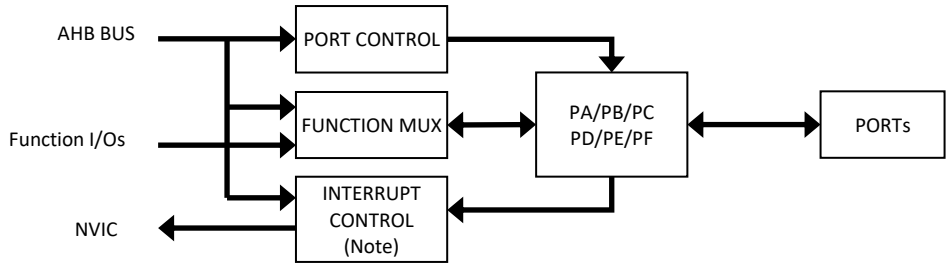
PCU (Port Control Unit) configures and controls external I/Os as shown below:

- It configures direction of an external signal of each pin.
- It sets Interrupt trigger mode for each pin.
- The PCU sets internal pull-up/down register control and open drain control.

Most pins, except for dedicated function pins, can be used as GPIO (General Purpose I/O) ports. GPIO block controls the GPIO as shown below:

- Output signal level (H/L) select
- External interrupt interface
- Pull-up/down enable or disable

5.1 PCU and GPIO block diagrams



NOTE: Refer to the Chapter 3.2 Interrupt controller.

Figure 19. PCU Block Diagram

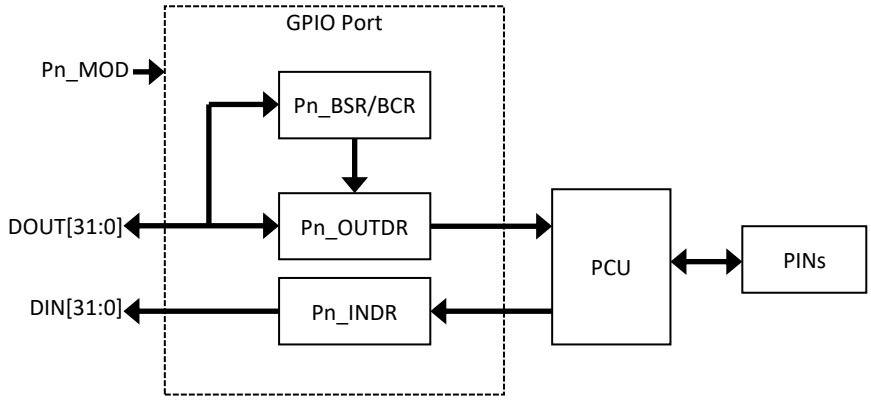
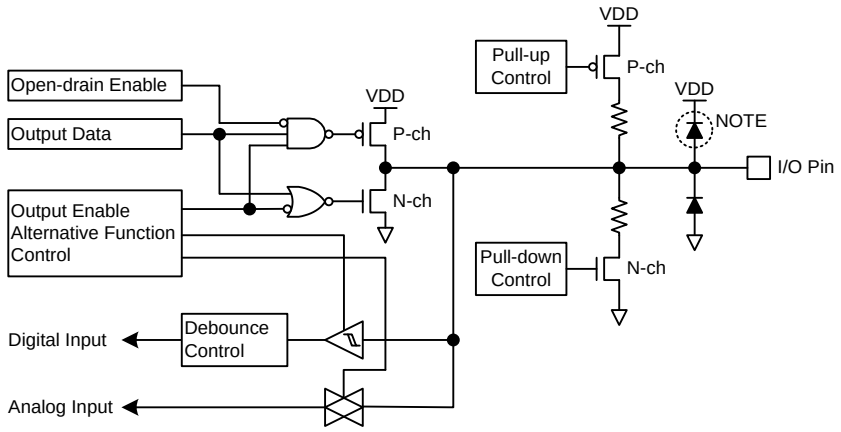


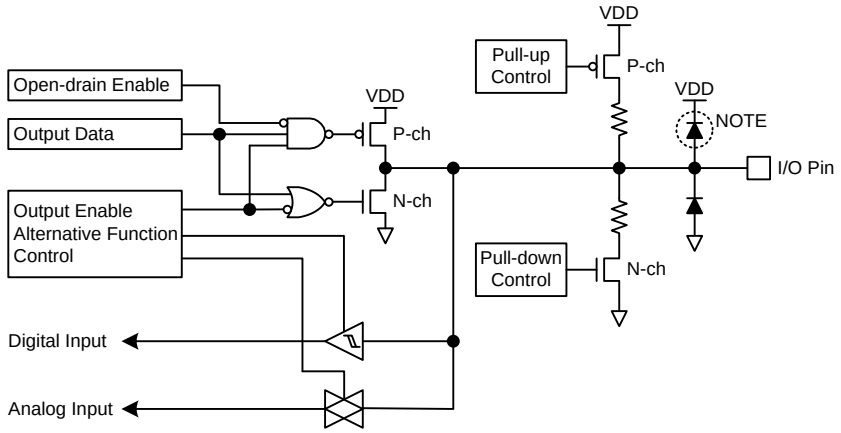
Figure 20. GPIO Block Diagram

5.2 I/O port block diagram



NOTE: The PB0-PB15, PC0-PC11, PD0-PD7, PE0-PE7, PF5-PF7 pins(COM,SEG,VLC,CAPH/L) do not have diode between VDD and PAD.

Figure 21. I/O Port Block Diagram (External Interrupt I/O pins)



NOTE: The PB0-PB15, PC0-PC11, PD0-PD7, PE0-PE7, PF5-PF7 pins(COM,SEG,VLC,CAPH/L) do not have diode between VDD and PAD.

Figure 22. I/O Port Block Diagram (General I/O pins)

5.3 Pin multiplexing

GPIO pins support alternative functions. Table 11 shows pin multiplexing information.

Table 11. GPIO Alternative Functions

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PA	0	–	SDA1	–	AN0	–
	1	–	SCL1	–	AN1	–
	2	–	EC12	–	AN2	–
	3	–	–	–	AN3	–
	4	–	–	–	AN4	–
	5	–	T12OUT	T12CAP	AN5	–
	6	–	–	–	AN6	–
	7	–	–	–	AN7	AVREF
	8	–	–	–	AN11	–
	9	–	–	–	AN12	–
	10	–	–	–	AN13	–
	11	–	–	–	–	–
PB	0	SEG39	TXD10	MOSI10	–	–
	1	SEG38	RXD10	MISO10	–	–
	2	SEG37	–	SCK10	–	–
	3	SEG36	BOOT	SS10	–	–
	4	SEG35	–	SWCLK	–	–
	5	SEG34	–	SWDIO	–	–
	6	SEG33	TXD1	–	–	–
	7	SEG32	RXD1	–	–	–
	8	SEG31	–	–	–	–
	9	SEG30	EC15	–	–	–
	10	SEG29	–	–	–	–
	11	SEG28	T15OUT	T15CAP	–	–
	12	SEG27	–	–	–	–
	13	SEG26	–	–	–	–
	14	SEG25	–	–	–	–
	15	SEG24	–	–	–	–

Table 11. GPIO Alternative Functions (continued)

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PC	0	SEG23	T20OUT	T20CAP	–	–
	1	SEG22	T21OUT	T21CAP	–	–
	2	SEG21	EC20	–	–	–
	3	SEG20	EC21	–	–	–
	4	SEG19	–	–	–	–
	5	SEG18	–	–	–	–
	6	SEG17	–	–	–	–
	7	SEG16	–	–	–	–
	8	SEG15	–	–	–	–
	9	SEG14	–	–	–	–
	10	SEG13	–	–	–	–
	11	SEG12	–	–	–	–
PD	0	SEG11	–	–	–	–
	1	SEG10	–	–	–	–
	2	SEG9	TXD11	MOSI11	–	–
	3	SEG8	RXD11	MISO11	–	–
	4	SEG7	–	SCK11	–	–
	5	SEG6	–	SS11	–	–
	6	SEG5	EC11	–	–	–
	7	SEG4	EC10	–	–	–
PE	0	CAPH	–	–	–	–
	1	CAPL	–	–	–	–
	2	COM0	–	–	–	–
	3	COM1	–	–	–	–
	4	COM2/SEG0	–	–	–	–
	5	COM3/SEG1	–	–	–	–
	6	SEG2	T10OUT	T10CAP	–	–
	7	SEG3	T11OUT	T11CAP	–	–
	8	–	–	–	–	T13CAP
	9	–	–	–	(SCK11)	–
	10	–	–	–	(RXD11)	(MISO11)
	11	–	–	–	(TXD11)	(MOSI11)
	12	–	–	–	(TXD1)	–
	13	–	–	–	(RXD1)	–
	14	–	–	–	EC14	–
	15	–	–	–	–	T14CAP

Table 11. GPIO Alternative Functions (continued)

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PF	0	XOUT	(SCL1)	–	–	–
	1	XIN	(SDA1)	–	–	–
	2	SXIN	–	–	–	–
	3	SXOUT	–	–	–	–
	4	CLKO	VREG	–	–	–
	5	VLC0	–	–	–	–
	6	VLC1	–	–	–	–
	7	VLC2	–	–	–	–
	8	–	EC13	–	–	–

NOTES:

1. An unused pin shouldn't be configured as an input floating.
2. After reset, the PB3 pin is configured as BOOT alternative function and the internal pull-up is activated.
3. After reset, the PB4 and PB5 pins are configured as SWCLK and SWDIO alternative functions, and the internal pull-down on SWCLK and the internal pull-up on SWDIO are activated.
4. The SWCLK and SWDIO pins shouldn't be changed as other alternative functions by software during the pins are connected with debugger host.
5. The PF4/VREG pin is configured as a function pin by software control.
6. The PF4/VREG pin should be configured as a VREG alternative function if a sub oscillator is used.
7. A USART11 should be used as a pin pair for MOSI11/MISO11 in SPI mode. In other words, there are two pairs for SPI interface, one of which is a pair of PD2/PD3 and the other is a pair of PE10/PE11.

6 WDT

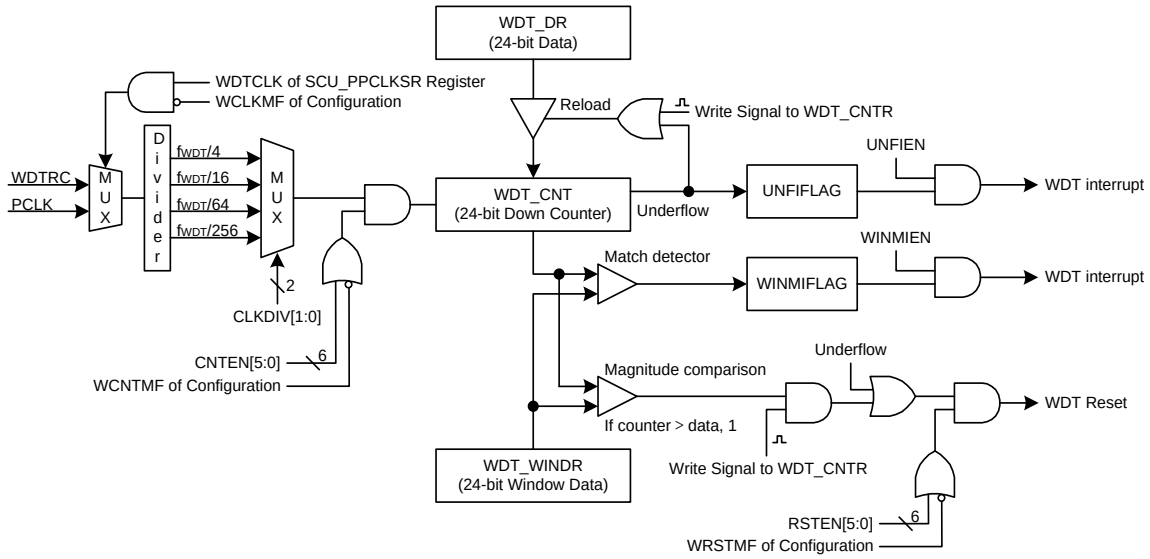
WDT (Watchdog Timer) rapidly detects CPU malfunctions such as endless loops caused by noise and recovers the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request.

When the WDT is not being used for malfunction detection, it can be used as a timer to generate interrupts at fixed intervals. When WDT_CNT value reaches WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of the WDT can be set by WDT_DR. If an underflow occurs, an internal reset may be generated. The WDT operates at 40kHz which is the embedded RC oscillator's clock.

The WDT operations are listed in the followings:

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Includes Counter Window function

6.1 WDT block diagram



NOTE: When a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register, after 1-clock delay, with the clock selected by the CLKDIV bits.

Figure 23. WDT Block Diagram

7 WT

WT (WATCH TIMER) has a function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register. To operate the watch timer, determine the input clock source, output interval and set WTEN as '1' in watch timer control register (WT_CR). It is able to operate simultaneously or individually. To stop the WT, clear the WTEN bit in the WT_CR register. Even when the CPU is in STOP mode, sub clock stays alive and the WT can continue operation. The WT_CR can control WT clear and set Interval value at writing, and can read 12-bit WT counter value at reading. The WT features the followings:

- 14-bit Divider
- 12-bit up-counter
- RTC function

7.1 WT block diagram

Figure 24 shows a block diagram of the WT block.

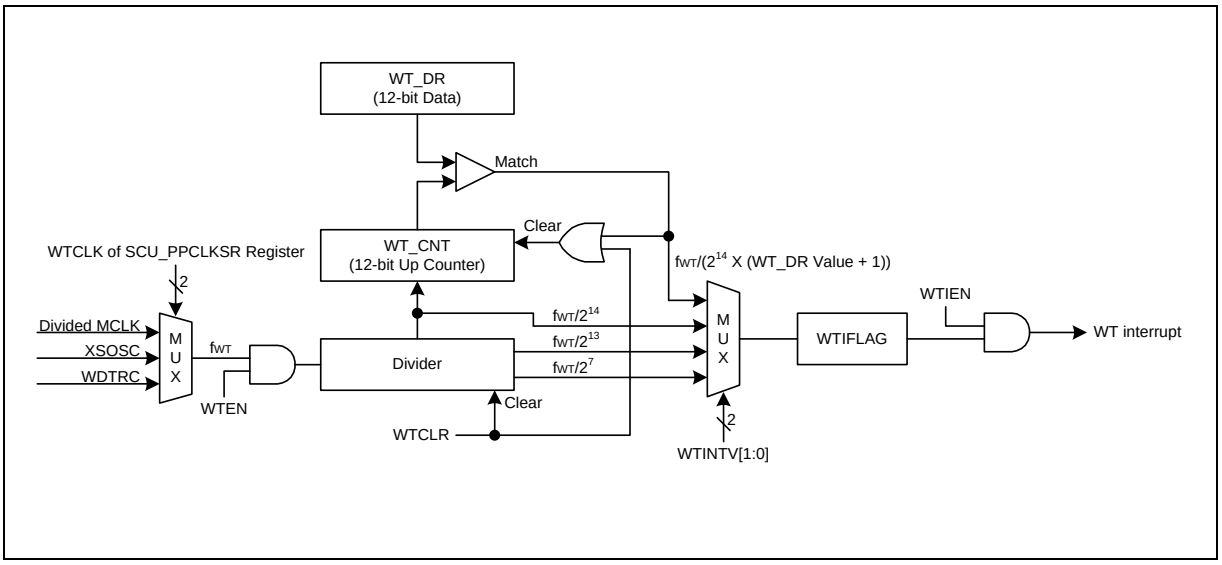


Figure 24. WT Block Diagram

8 Timer counter 10/11/12/13/14/15 and Timer counter 20/21

8.1 Timer counter 10/11/12/13/14/15

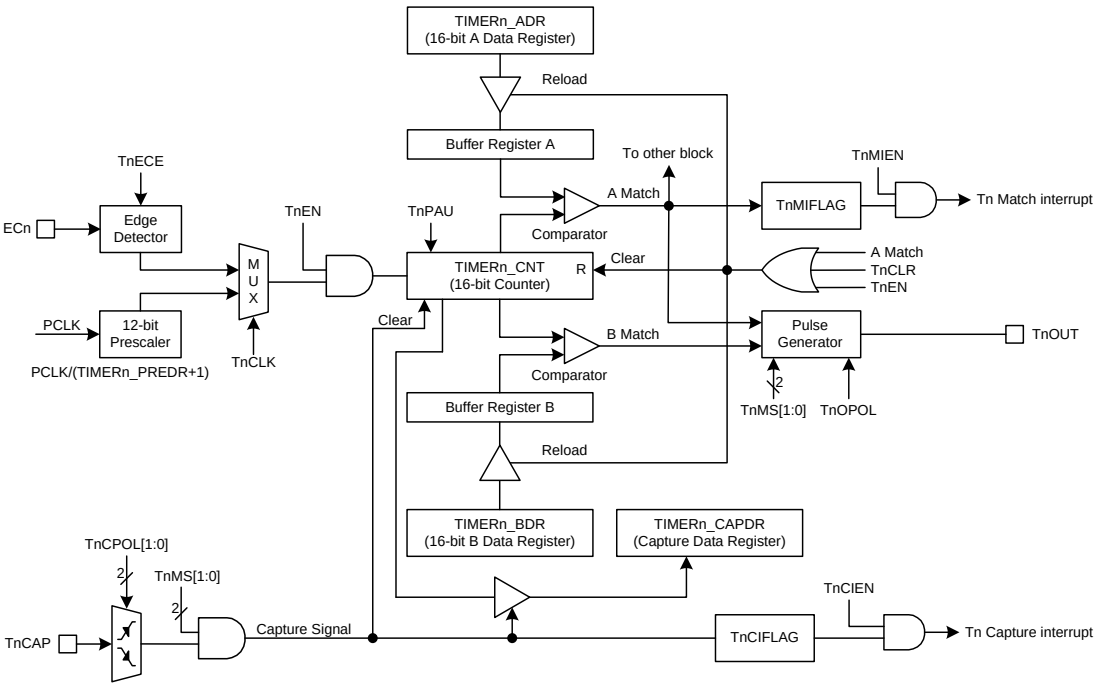
The timer block comprises 6 channels of 16-bit general purpose timers. Each has an independent 16-bit counter and a dedicated prescaler that feeds counting clock. They support periodic timer, PWM pulse, one-shot and capture mode.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source. The timer counter 10/11/12/13/14/15 features the followings:

- 16-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function

8.1.1 Timer counter 10/11/12/13/14/15 block diagram

Figure 25 shows the block diagram of a timer block unit.



NOTES:

1. TnEN bit is automatically cleared to logic “0b” after one pulse is generated at a PPG one-shot mode.
2. After the TnEN bit is set, counting of TIMERn_CNT may be delayed 2 clocks or more.
3. There are no T13OUT and T14OUT pins of 16-bit Timer 1n modules.

Figure 25. Timer Counter n Block Diagram (n = 10, 11, 12, 13, 14 and 15)

8.1.2 Pin description for timer counter 10/11/12/13/14/15

Table 12. Pins and External Signals for Timer Counter n (n = 10, 11, 12, 13, 14 and 15)

PIN NAME	TYPE	DESCRIPTION
ECn	I	External clock input
TnCAP	I	Capture input
TnOUT	O	PWM/one-shot output (Except T13OUT and T14OUT)

8.2 Timer counter 20

A timer block comprises a single channel 32-bit general purpose timer. This timer has an independent 32-bit counter and a dedicated prescaler that feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

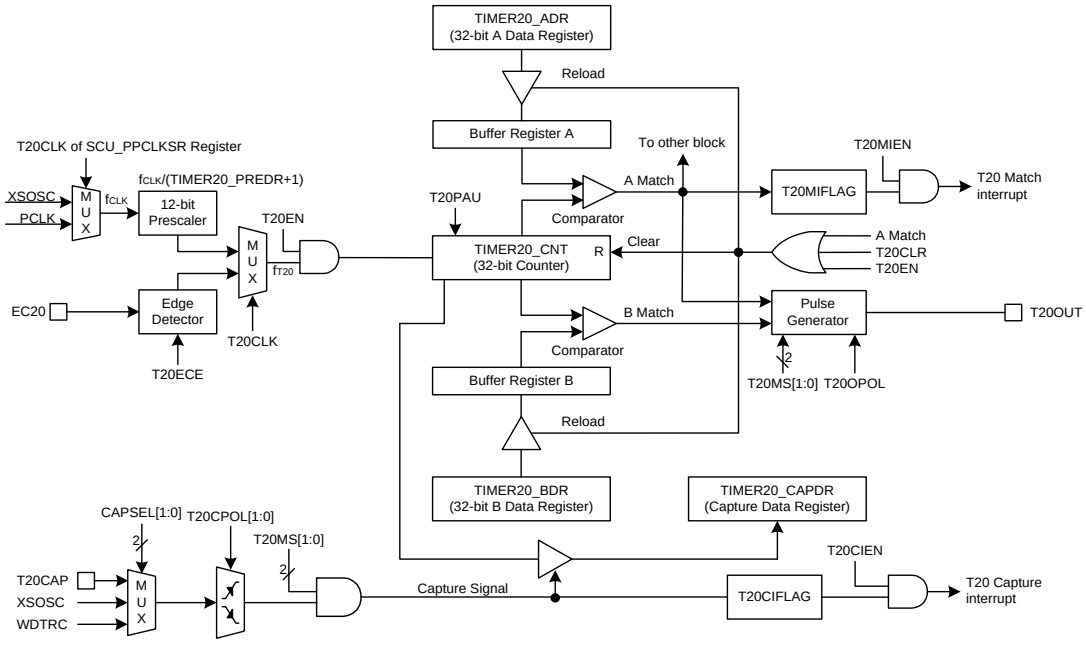
One more optional free-run timer is provided. Main purpose of this timer is a periodical tick timer or a wake-up source. The Timer counter 20 features the followings:

- 32-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode

Synchronous start and clear function

8.2.1 Timer counter 20 block diagram

Figure 26 shows the block diagram of a timer block unit.



NOTES:

1. T20EN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.
2. After T20EN bit is set, counting of TIMER20_CNT may be delayed by 2 clocks or more.

Figure 26. Timer Counter 20 Block Diagram

8.2.2 Pin description for Timer counter 20

Table 13. Pins and External Signals for Timer Counter 20

PIN NAME	TYPE	DESCRIPTION
EC20	I	External clock input
T20CAP	I	Capture input
T20OUT	O	PWM/one-shot output

8.3 Timer counter 21

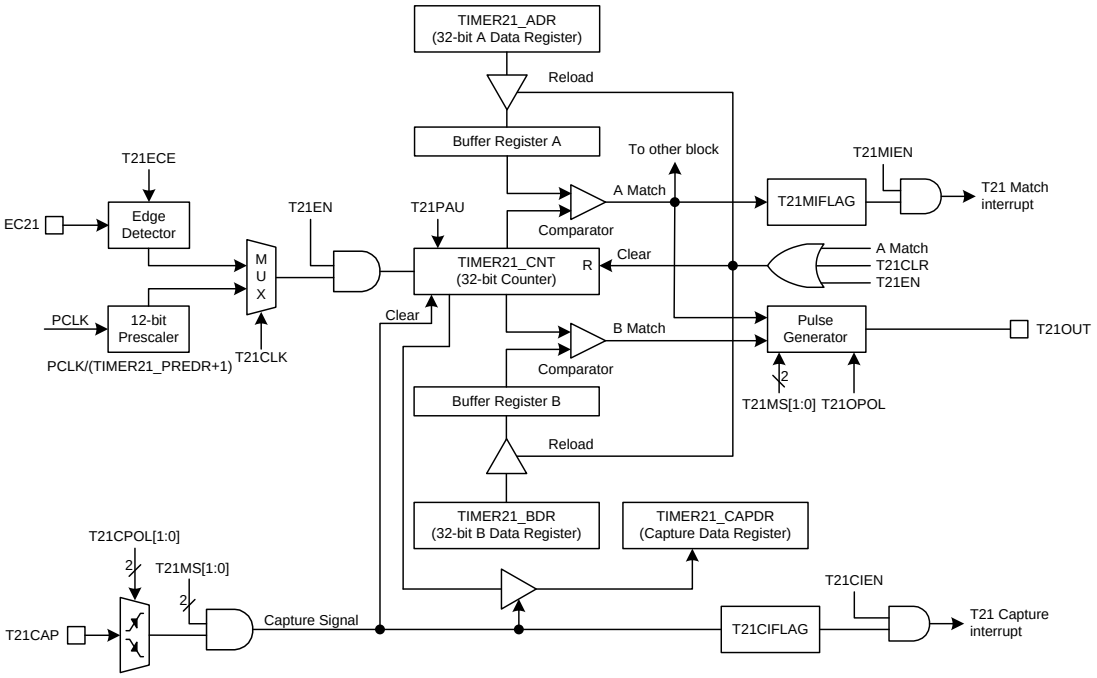
A timer block comprises a single channel 32-bit general purpose timer. This timer has an independent 32-bit counter and a dedicated prescaler that feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

One more optional free-run timer is provided. Main purpose of this timer is a periodical tick timer or a wake-up source. The Timer counter 21 features the followings:

- 32-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function

8.3.1 Timer counter 21 block diagram

Figure 27 shows the block diagram of a timer block unit.



NOTES:

1. T21EN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.
2. After T21EN bit is set, counting of TIMER21_CNT may be delayed by 2 clocks or more.

Figure 27. Timer Counter 21 Block Diagram

8.3.2 Pin description for Timer counter 21

Table 14. Pins and External Signals for Timer Counter 21

PIN NAME	TYPE	DESCRIPTION
EC21	I	External clock input
T21CAP	I	Capture input
T21OUT	O	PWM/one-shot output

9 12-bit A/D Converter

ADC (Analog-to-Digital Converter) of A31R713 allows conversion of an analog input signal to a corresponding 12-bit digital value. Its A/D module has eleven analog inputs as shown in Figure 28. Output of the multiplexer is the input into the converter, which generates the result through successive approximation.

The A/D module has three registers such as a control register (ADC_CR), a data register (ADC_DR), and a prescaler data register (ADC_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC_DR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC_DR, A/D conversion status bit ADCIFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, ADCIFLAG bit is read as '0'. Main features of the ADC are listed in the followings:

- 11-channel of analog inputs
- S/W (ADST), Timer trigger (T10/11/12 A match) support
- Conversion time: 58 clocks
- 6-bit Prescaler

9.1 12-bit ADC block diagram

Figure 28 shows a block diagram of an ADC block.

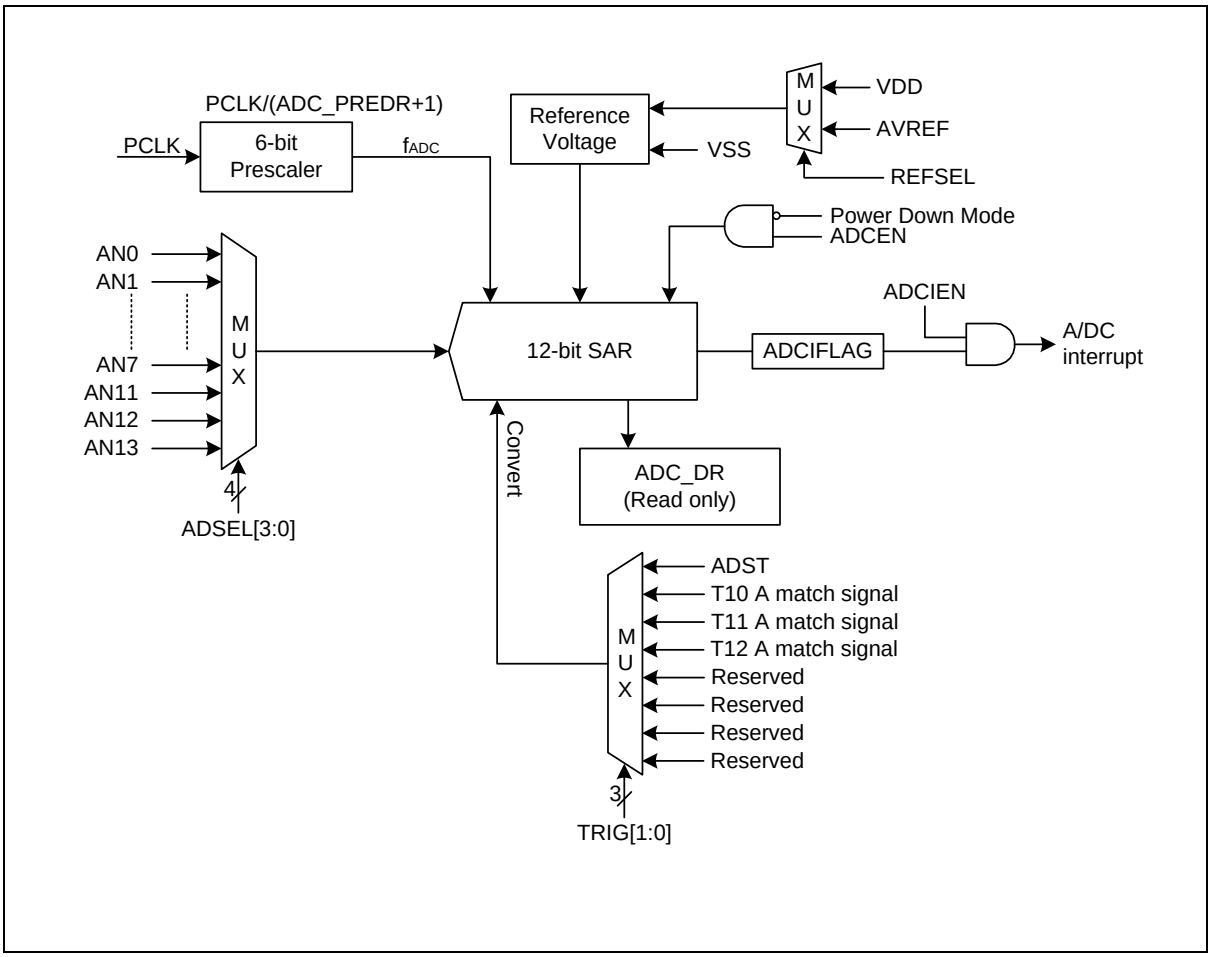


Figure 28. 12-bit ADC Block Diagram

9.2 Pin description for 12-bit ADC

Table 15. Pins and External Signals for 12-bit ADC

PIN NAME	TYPE	DESCRIPTION
VDD	P	Analog/Digital Power
VSS	P	Analog/Digital GND
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13

NOTE: Where A=Analog, P= Power

10 USART 10/11 and UART 1

10.1 USART 10/11

USART (Universal Synchronous and Asynchronous serial Receiver and Transmitter) is a highly flexible serial communication device. The USART of A31R713 features the followings:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation, and Parity Check Supported by Hardware.
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode

10.1.1 USART 10/11 block diagram

Figure 29 shows a block diagram of the UART block.

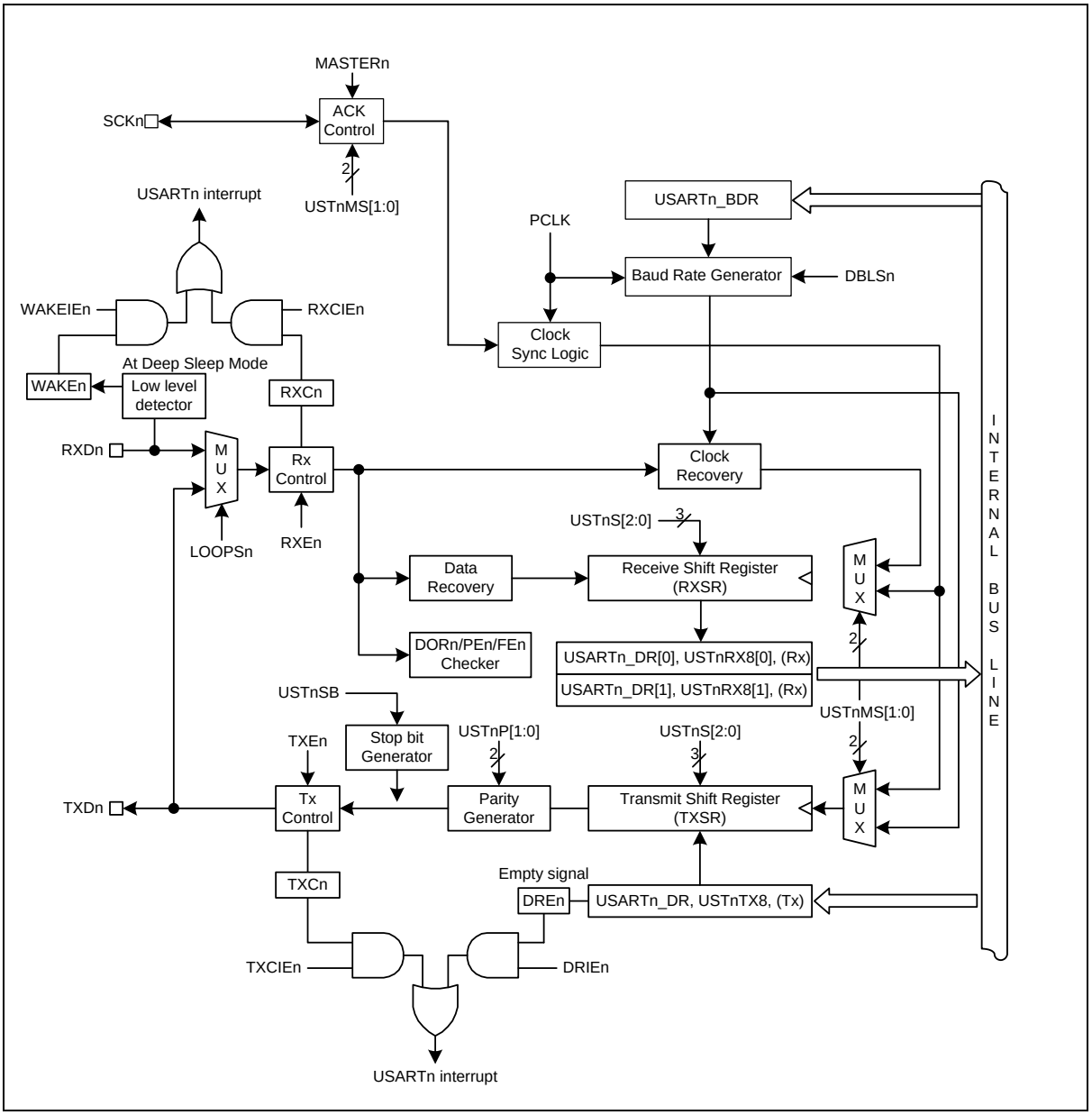
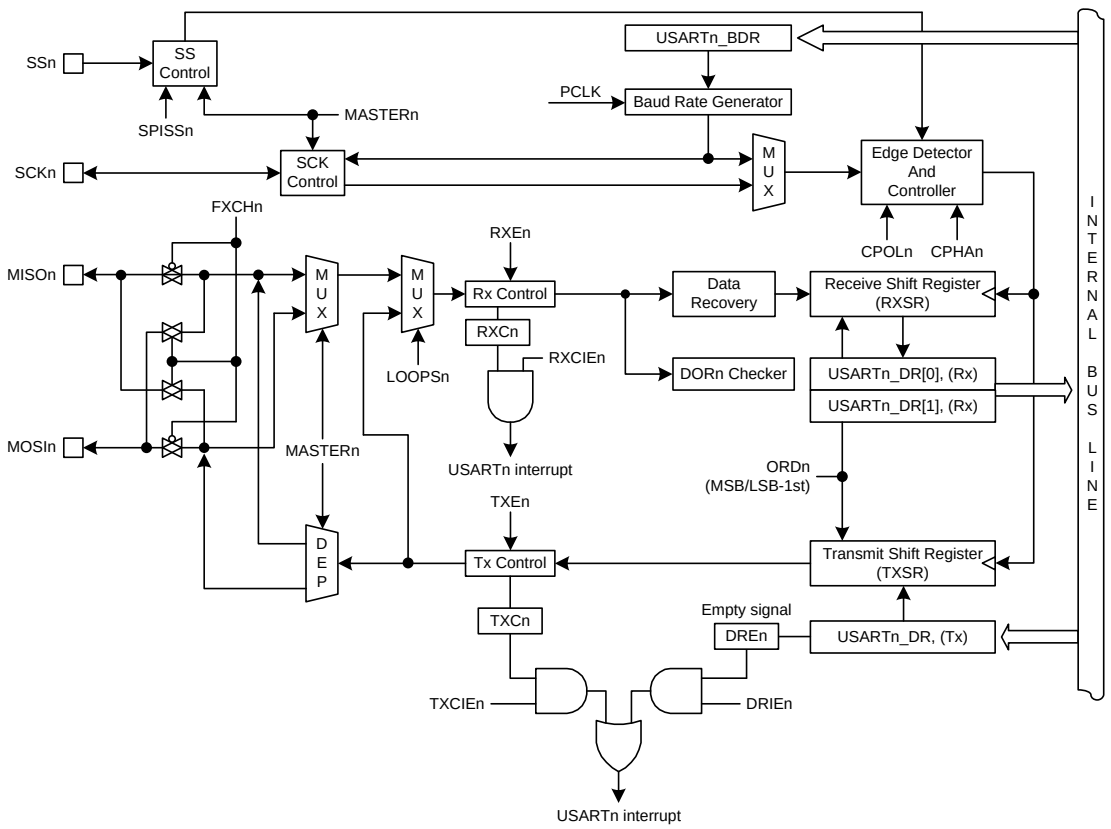


Figure 29. UART n Block Diagram of USART (n = 10 and 11)

Figure 30 shows a block diagram of the SPI block.



NOTES:

1. After the transmitting, the next transmission should be started after one clock of the SPI clock.
2. A USART11 should be used as a pin pair for MOSI11/MISO11 in SPI mode. In other words, there are two pairs for SPI interface, one of which is a pair of PD2/PD3 and the other is a pair of PE10/PE11.
3. In SPI mode, both MOSI1n and MISO1n should be configured as alternative function pins.

Figure 30. SPIn Block Diagram of USART (n = 10 and 11)

10.1.2 Pin description for USART 10/11

Table 16. Pins and External Signals for USART 10/11

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

10.2 UART 1

There are built-in 1-channel of UART module (Universal Asynchronous Receiver/Transmitter) in A31R713. UART operation status including error status can be read from a status register.

A prescaler, which generates proper baud rate, exists for each UART channel. The prescaler can divide the UART clock source, PCLK, from 3 to 65535. Then, baud rate is generated using a 1:16 clock and an 8-bit precision clock tuning function.

The UART 1 of A31R713 features the followings:

- Compatible with 16450
- Configurable standard asynchronous control bit (start, stop, and parity)
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

10.2.1 UART 1 block diagram

Figure 31 shows a block diagram of the UART block.

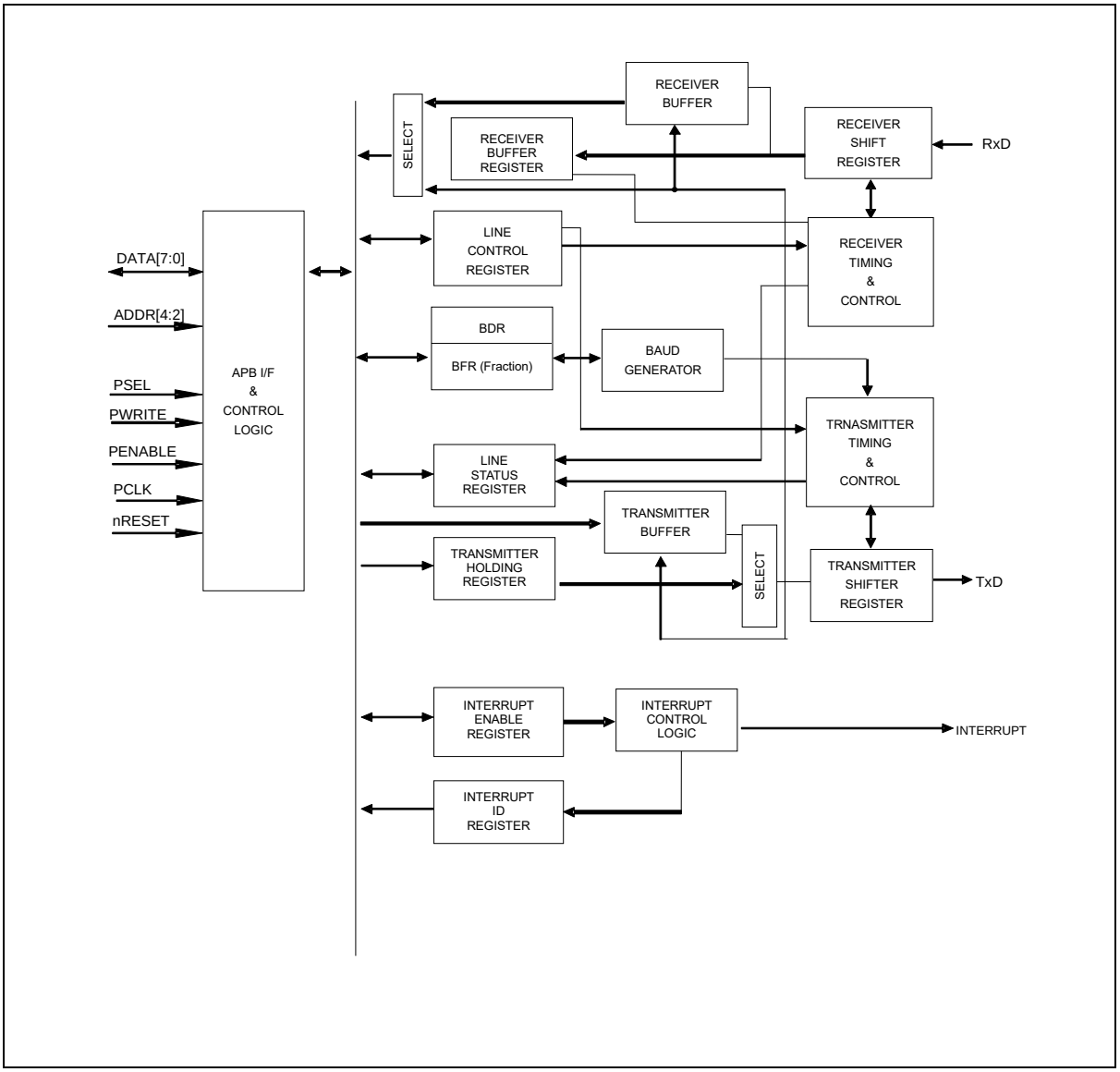


Figure 31. UART 1 Block Diagram

10.2.2 Pin description for UART 1

Table 17. Pins and External Signals for UART 1

PIN NAME	TYPE	DESCRIPTION
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

11 I2C 1 interface

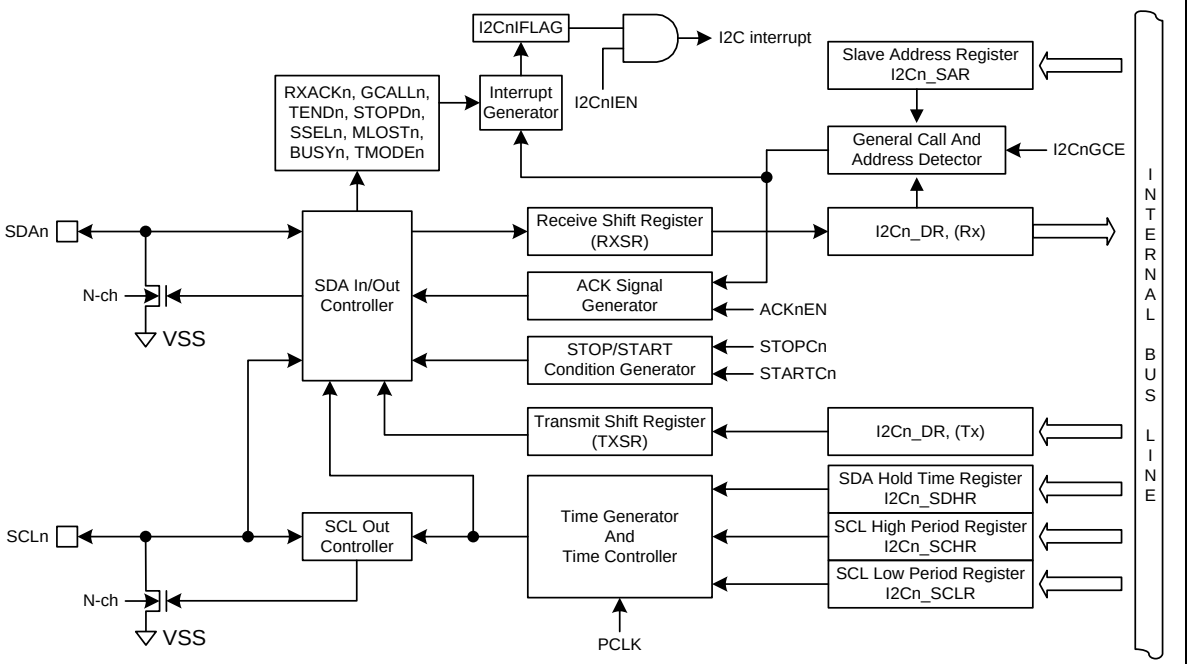
I2C is one of industrial standard serial communication protocols, which uses 2 bus lines, Serial Data Line (SDAn) and a Serial Clock Line (SCLn), to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs a pull-up resistor (n = 1).

The I2C 1 of A31R713 features the followings:

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer read speed
- 7-bit address
- Support two slave addresses
- Both master and slave operation
- Bus busy detection

11.1 I2C 1 block diagram

Figure 32 shows a block diagram of the I2C block.



NOTE: When the corresponding port of I2C is a sub-function for SCLn/SDAn pin, the SCLn/SDAn pins are automatically set as N-channel open-drain outputs and the input latch is read when reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 32. I2C Block Diagram (n = 1)

11.1.1 Pin description for I2C 1

Table 18. Pins and External Signals for I2C (n = 1)

PIN NAME	TYPE	DESCRIPTION
SCLn	I/O	I2C channel n Serial clock bus line (open-drain)
SDAn	I/O	I2C channel n Serial data bus line (open-drain)

12 LCD driver

LCD driver of A31R713 includes an LCD control register (LCD_CR) and an LCD contrast control register (LCD_CCR). LCLK[1:0] of the LCD_CR determines frequency of COM signal scanning each segment output. A RESET clears the LCD_CR, and sets the LCD_CCR to logic '0'.

LCD display can continue its operation even during Sleep mode and Deep sleep mode if it uses a selected clock for LCD driver.

A clock and duty of the LCD driver is initialized by hardware whenever a value is written to the control register. So, it is recommended not to rewrite the LCD_CR frequently.

12.1 LCD driver block diagram

Figure 33 shows a block diagram of the LCD driver block.

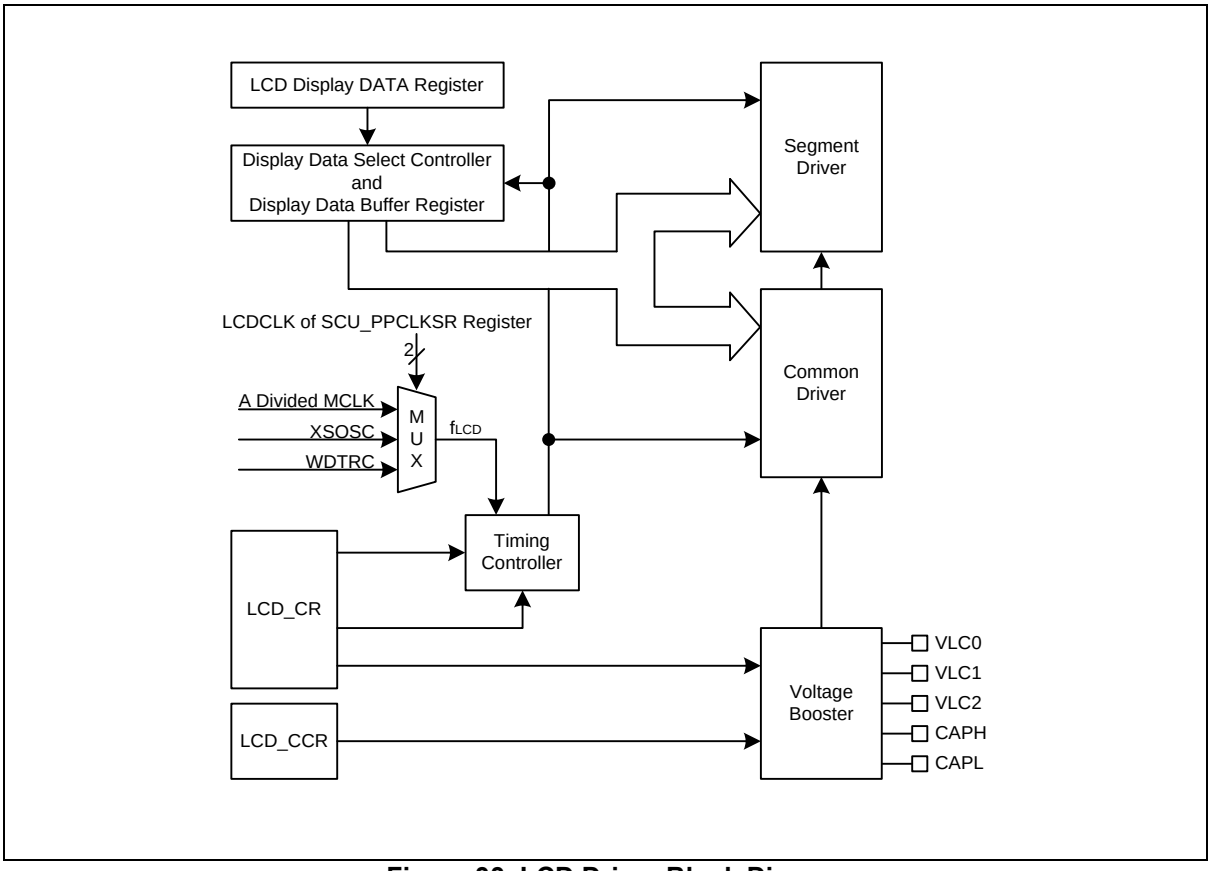


Figure 33. LCD Driver Block Diagram

12.2 Pin description for LCD driver

Table 19. Pins and External Signals for LCD Driver

PIN NAME	TYPE	DESCRIPTION
COM0 to COM3	O	LCD common signal outputs
SEG0 to SEG39	O	LCD segment signal outputs
VLC0/1/2	I/O	LCD bias voltage input/output
CAPH/CAPL	O	Capacitor terminal for voltage booster

13 CRC and checksum

A CRC (cyclic redundancy check) generator is used to obtain 16-bit CRC code of Flash ROM and any data stream.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of functional safety standards, they offer means of verifying Flash memory's integrity.

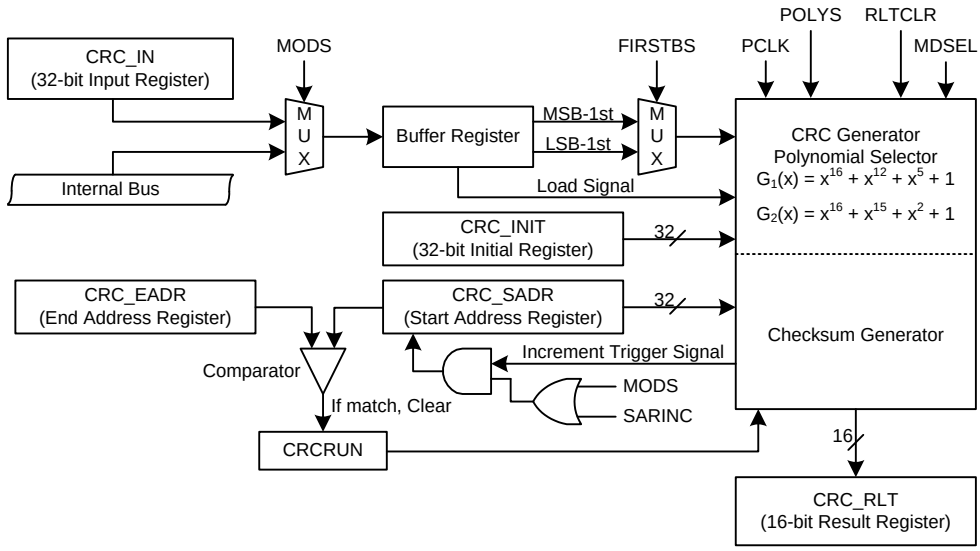
The CRC generator helps computing the signature of the software during runtime, comparing with a reference signature.

A CRC generator of A31R713 has following features:

- Auto CRC and User CRC Mode
- Supports CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
- Supports CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC and Checksum mode
- CRC/Checksum Start Address Auto Increment (User mode only)

13.1 CRC and checksum block diagram

Figure 34 shows a block diagram of the CRC and checksum interface block.



NOTES:

1. The operation is finished after calculating from the CRC_SADR to the CRC_EADR on auto mode or SARINC=1.
2. The CRC_SADR and CRC_EADR are the same value after completion.
3. The end address (CRC_EADR) must be greater than the start address (CRC_SADR) by at least 4.
4. The CRC_SADR/CRC_EADR on the “Auto mode” should have any value in flash memory area (0x10000000 to 0x1000FFFF).
5. The CPU will be held at “Auto Mode” if the CPU is in the flash memory and the global interrupt should be disabled by software.
6. The HCLK frequency should be less than or equal to 20MHz in “Auto mode” by CRC_CR.MODS bit.
7. On auto mode run, the CRC_CR register cannot be written and the CRC_RLT register cannot be read.

Figure 34. CRC and Checksum Block Diagram

14 Electrical characteristics

Unless otherwise specified, test conditions for DC characteristics are as shown in the followings:

- T_A = - 40 °C to +85°C
- VDD = 1.8 to 5.5V

NOTE: Refer to Figure 52. A31R713 Numbering Nomenclature for device part number by Commercial grade.

14.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions, which should not be exceeded under the worst possible conditions.

Table 20. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	VDD	-0.3 to +6.5	V	–
Normal pin	V_I	-0.3 to VDD +0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD +0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-60	mA	Maximum current (ΣI_{OH})
	I_{OL}	20	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	80	mA	Maximum current (ΣI_{OL})
Total power dissipation	P_T	300	mW	–
Storage temperature	T_{STG}	-65 to +150	°C	–

14.2 Recommended operating conditions

Table 21. Recommended Operating Conditions

Parameter	Symbol	Conditions			Min	Max	Units
Operating voltage	VDD	fx = 32 to 38kHz	Sub Clock		1.8	5.5	V
		fx = 2.0 to 4.2MHz	Main Clock	Ceramic	2.2	5.5	
		fx = 2.0 to 16MHz		Crystal	2.7	5.5	
		fx = 2.0 to 40MHz	External Clock		3.0	5.5	
		fx = 40kHz	Internal RC		1.8	5.5	
		fx = 2.5 to 40MHz			1.8	5.5	
Operating temperature	T_{OPR}	VDD = 1.8 to 5.5V (Commercial grade)			-40	85	°C

14.3 ADC characteristics

Table 22. ADC Characteristics

(VDD = 2.2V to 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral non-linearity	INL	AVREF=2.7V – 5.5V, T_A = 25 °C		–	–	±5	LSB
Differential non-linearity	DNL			–	–	±1	
Zero offset error	ZOE			–	–	±5	
Full scale error	FSE			–	–	±5	
Conversion time	t_{CONV}	AVREF=4.0V – 5.5V		20	–	–	µs
		AVREF=3.0V – 5.5V		30	–	–	
		AVREF=2.7V – 5.5V		60	–	–	
Analog input voltage	V_{AN}	–		VSS	–	AVREF	V
Analog reference voltage	AVREF	–		2.2	–	VDD	V
ADC input leakage current	I_{AN}	AVREF=5.0V		–	–	2	µA
ADC current	I_{ADC}	Enable	VDD=5.0V	–	1	2	mA
		Disable		–	–	0.1	µA

NOTES:

1. Zero offset error is a difference between 0x000 and the converted output for zero input voltage (VSS).
2. Full scale error is a difference between 0xFFF and the converted output for top input voltage (VDD).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V.
   (It is recommended that the clock of ADC is 0.5MHz under 2.7V)

14.4 Power-on reset characteristics

Table 23. Power-on Reset Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset release level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.2	–	V
VDD voltage rising time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	0.1	–	μA

14.5 Low voltage reset characteristics

Table 24. Low Voltage Reset Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection level	V_{LVR}	• 1.62V level: Rising edge voltage, • Other levels: Falling edge voltage		–	1.62	1.77	V
				1.85	2.00	2.15	
				1.98	2.13	2.28	
				2.13	2.28	2.43	
				2.31	2.46	2.61	
				2.47	2.67	2.87	
				2.84	3.04	3.24	
				3.00	3.20	3.40	
				3.35	3.55	3.75	
				3.45	3.75	4.05	
				3.69	3.99	4.29	
				3.95	4.25	4.55	
				4.25	4.55	4.85	
Hysteresis	$\triangle V$	–		–	100	200	mV
Minimum pulse width	t_{LW}	–		100	–	–	µs
LVR current	I_{LVR}	Enable, All mode	VDD = 5V	–	10.0	20.0	µA
		Disable		–	–	0.1	

14.6 Low voltage indicator characteristics

Table 25. Low Voltage Indicator Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection level	V_{LVI}	Falling edge voltage		1.85	2.00	2.15	V
				1.98	2.13	2.28	
				2.13	2.28	2.43	
				2.31	2.46	2.61	
				2.47	2.67	2.87	
				2.84	3.04	3.24	
				3.00	3.20	3.40	
				3.35	3.55	3.75	
				3.45	3.75	4.05	
				3.69	3.99	4.29	
				3.95	4.25	4.55	
				4.25	4.55	4.85	
Hysteresis	△V	–		–	–	200	mV
Minimum pulse width	t_{LW}	–		100	–	–	µs
LVI current	I_{LVI}	Enable, All mode	VDD = 5V	–	10.0	20.0	µA
		Disable		–	–	0.1	

14.7 High frequency internal RC oscillator characteristics

Table 26. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HIRC}	VDD = 1.8V to 5.5V	–	40	–	MHz
Accuracy	–	T_A = -10 °C to + 55 °C	–	–	±2.0	%
		T_A = -20 °C to +85 °C	–	–	±3.0	
		T_A = -40 °C to +85 °C	–	–	±4.0	
		T_A = -10 °C to + 55 °C User trim by S/W	–	–	±1.0	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	100	µs
IRC current	I_{HIRC}	Enable	–	500	–	µA
		Disable	–	–	0.1	µA

14.8 Internal watchdog timer RC oscillator characteristics

Table 27. Internal Watchdog Timer RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	34	40	46	kHz
Stabilization time	t_{WDTS}	–	–	–	1	ms
WDTRC current	I_{WDTRC}	Enable	–	3	6	µA
		Disable	–	–	0.1	

14.9 LCD voltage characteristics

Table 28. LCD Voltage Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD voltage(NOTE)	VLC2	Voltage booster enabled, 1/2 bias		Typx0.93	1.0+(nx0.05)	Typx1.07	V
		LCD booster enabled, 1/3 bias	VLCD[3:0]=0x00	Typx0.93	0.75	Typx1.07	V
			VLCD[3:0]=0x01		0.79		
			VLCD[3:0]=0x02		0.83		
			VLCD[3:0]=0x03		0.86		
			VLCD[3:0]=0x04		0.90		
			VLCD[3:0]=0x05		0.94		
			VLCD[3:0]=0x06		0.98		
			VLCD[3:0]=0x07		1.01		
			VLCD[3:0]=0x08		1.05		
			VLCD[3:0]=0x09		1.09		
			VLCD[3:0]=0x0A		1.13		
			VLCD[3:0]=0x0B		1.17		
			VLCD[3:0]=0x0C		1.20		
			VLCD[3:0]=0x0D		1.24		
			VLCD[3:0]=0x0E		1.28		
			VLCD[3:0]=0x0F		1.32		
LCD mid bias voltage	VLC0/1	Voltage booster enabled, 1/2 bias, No panel load, VDD=3V		Typx0.9	2xVLC2	Typx1.1	V
	VLC0	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V		Typx0.9	3xVLC2	Typx1.1	
	VLC1			Typx0.9	2xVLC2	Typx1.1	
	VLC1	Voltage booster disabled, 1/3 bias, LCD dividing resistor VDD=2.7V to 5.5V LCD clock = 0Hz, VLC0=VDD		Typ-0.2	2/3xVDD	Typ+0.2	
	VLC2			Typ-0.2	1/3xVDD	Typ+0.2	
LCD driver output impedance	R_{LO}	VLCD=3V, ILOAD=±10uA		–	5	10	kΩ
LCD bias dividing resistor	RLCD1	Internal resistor mode, TA = 25°C		20	30	40	kΩ
	RLCD2			40	60	80	
	RLCD3			80	120	160	
LCD Block Current	I_{LCD}	Voltage booster mode VDD=3V, VLCD=3.15V, 1/3 bias		–	3	6	µA

NOTE: Where n is the value of LCD_CCR. VLCD[3:0] bits(n = 0 to 10).

14.10 DC electrical characteristics

Table 29. DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	V_{IH}	All input pins, nRESET		0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, nRESET		–	–	0.2VDD	V
Input hysteresis	△V	All input pins, nRESET, VDD=3V		100	200	–	mV
Output High Voltage	V_{OH}	VDD=4.5V, I_{OH} = – 2mA, All output pins		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD=4.5V, I_{OL} = 8mA, All output pins		–	–	1.0	V
Input high leakage current	I_{IH}	All Input ports		–	–	1	µA
Input low leakage current	I_{IL}	All Input ports		– 1	–	–	µA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, All Input ports	VDD=5V	25	50	100	kΩ
			VDD=3V	50	100	200	
		V_I=0V, T_A=25°C, RESETB	VDD=5V	150	250	400	
			VDD=3V	300	500	700	
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, All Input ports	VDD=5V	13	25	50	kΩ
			VDD=3V	25	50	100	
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=5V		600	1,200	2,000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS, T_A=25°C, VDD=5V		2.5	5	10	MΩ

14.11 Supply current characteristics

Table 30. Supply Current Characteristics

Parameter	Symbol	Conditions		Typ	Max	Units
Supply current	IDD1 (run)	f_{HIRC} = 40MHz	VDD=5V±10%	6.5	13.0	mA
		f_{HIRC} = 20MHz	VDD=5V±10%	4.0	8.0	
		f_{XIN} = 16MHz	VDD=5V±10%	5.0	10.0	
			VDD=3V±10%	3.5	7.0	
	I_{DD2} (sleep)	f_{HIRC} = 40MHz	VDD=5V±10%	4.0	8.0	mA
		f_{HIRC} = 20MHz	VDD=5V±10%	2.5	5.0	
		f_{XIN} = 16MHz	VDD=5V±10%	3.2	6.4	
			VDD=3V±10%	2.0	4.0	
	I_{DD3}	f_{SUB} = 32.768kHz or f_{WDTRC} = 40kHz, VDD=3V±10%, TA=25°C	Sub run	90	180	uA
	I_{DD4}		Sub sleep	7.5	15.0	
	I_{DD5}	Deep sleep, VDD=5V±10%, TA=25°C		0.5	3.0	

NOTES:

1. fXIN is an external main oscillator, fSUB is an external sub oscillator, fHIRC is a high frequency internal RC oscillator, and fx is the selected system clock.
2. All supply current items don't include the current of an internal watch-dog timer RC (WDTRC) oscillator and peripheral blocks.
3. All supply current items include the current of the power-on reset (POR) block.

14.12 AC characteristics

Table 31. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 5 V	10	–	–	μs
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 5 V	100	–	–	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	VDD = 5 V All external counter input	100	–	–	
External counter transition time	t_{REC}, t_{FEC}	ECn, VDD = 5 V All external counter input	–	–	50	
I/O frequency	f_{IO1}	VDD = 3.0V, C_L = 30pF, All except f_{IO2}	–	–	3	MHz
	f_{IO2}	VDD = 2.7V, C_L = 30pF, SPI pins	–	–	4	

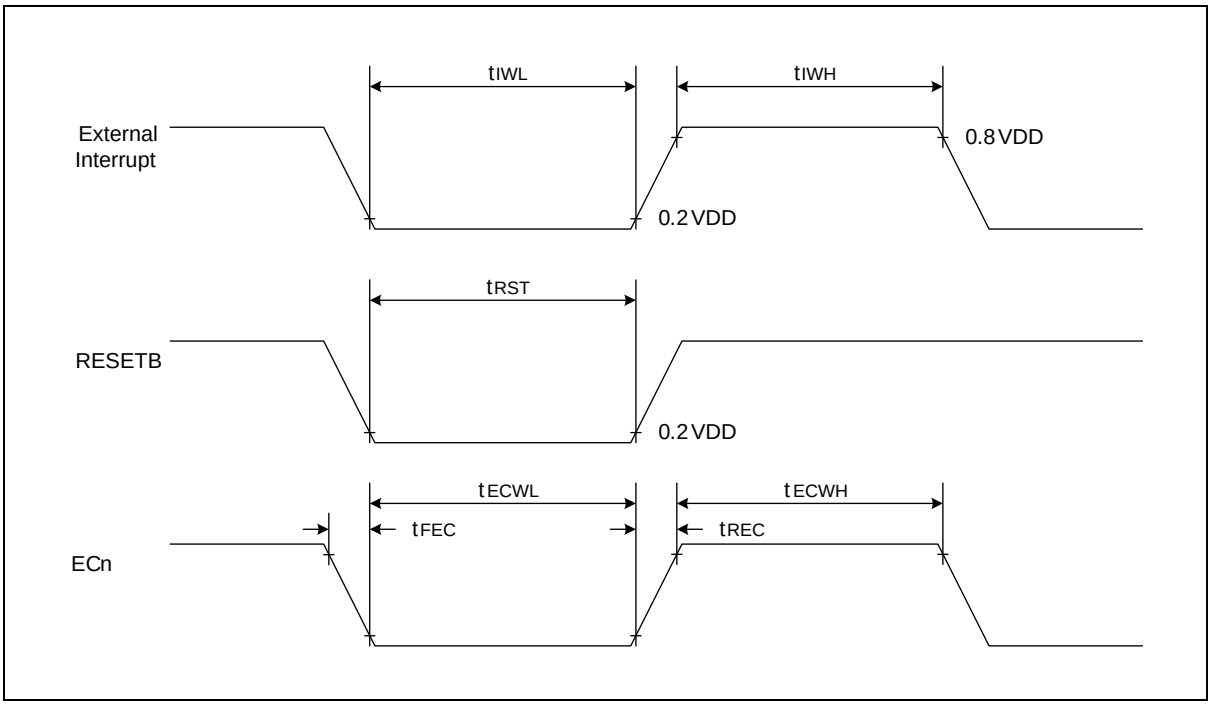


Figure 35. AC Timing

14.13 SPI characteristics

Table 32. SPI Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
SPI clock frequency	f_{SCK}	Pins: PE[11:9]	VDD ≥ 2.7V	–	–	4	MHz
			VDD ≥ 1.8V	–	–	2	
		Pins: PD[4:2], PB[2:0] LCD Cap Bias Off	VDD ≥ 2.7V	–	–	4	
			VDD ≥ 1.8V	–	–	2	
		Pins: PD[4:2], PB[2:0] LCD Cap Bias On	VDD ≥ 2.7V	–	–	3	
			VDD ≥ 1.8V	–	–	0.5	
Input/output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal/External SCK source		0.8*Typ	t_{SCK}/2	1.2*Typ	ns
First output clock delay time	t_{FOD}	Internal/External SCK source, CPHA = 0		0.4*t_{SCK}	–	–	
Output clock delay time	t_{DS}	–		–	–	18	
Input setup time	t_{DIS}			13	–	–	
Input hold time	t_{DIH}			15	–	–	

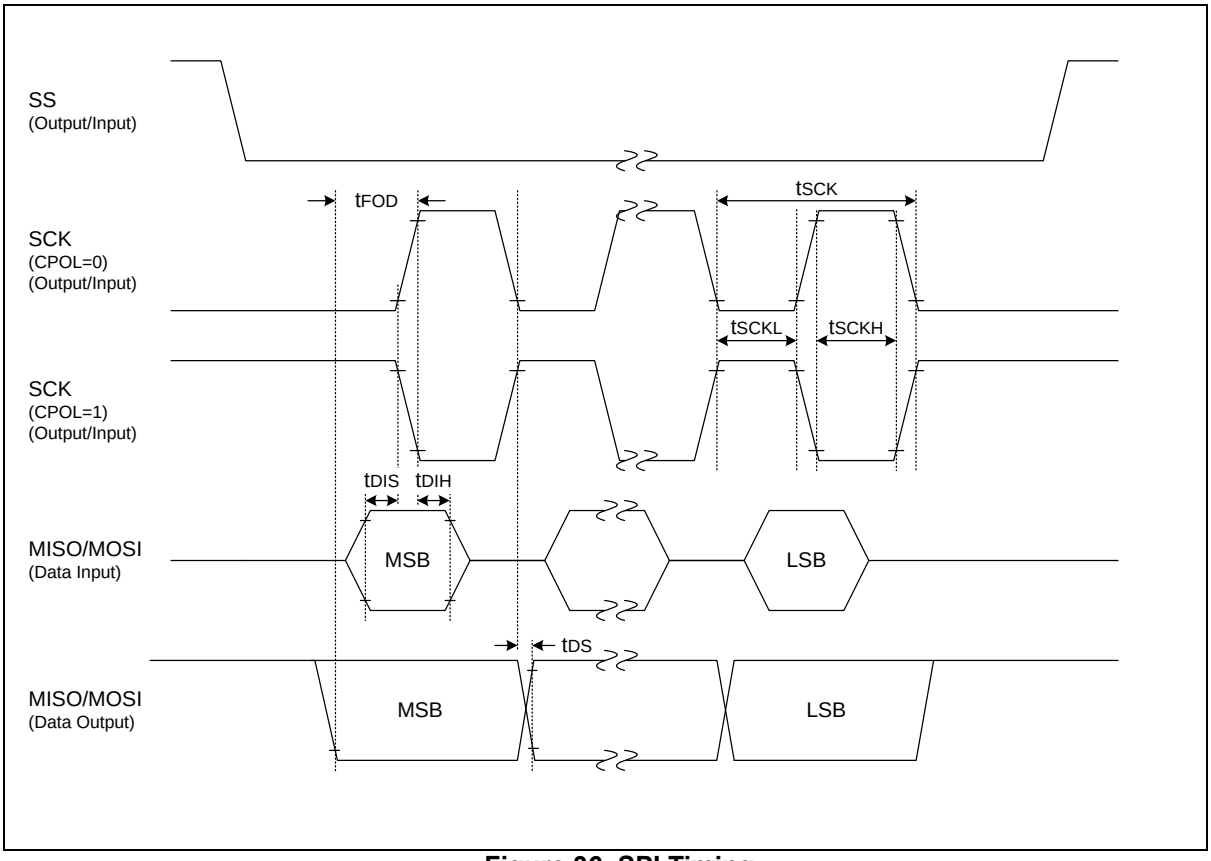


Figure 36. SPI Timing

14.14 I2C characteristics

Table 33. I2C Characteristics

Parameter	Symbol	Standard		Fast		Fast Plus		Units
		Min	Max	Min	Max	Min	Max	
I2C operating voltage	–	VDD ≥ 1.8V		VDD ≥ 2.0V		VDD ≥ 2.7V		–
Clock frequency	t_{SCL}	0	100	0	400	0	1000	kHz
Clock high pulse width	t_{SCLH}	4.0	–	0.6	–	0.26	–	µs
Clock low pulse width	t_{SCLL}	4.7	–	1.3	–	0.5	–	
Bus free time	t_{BF}	4.7	–	1.3	–	0.5	–	
Start condition setup time	t_{STSU}	4.7	–	0.6	–	0.26	–	
Start condition hold time	t_{STHD}	4.0	–	0.6	–	0.26	–	
Stop condition setup time	t_{SPSU}	4.0	–	0.6	–	0.26	–	
Stop condition hold time	t_{SPHD}	4.0	–	0.6	–	0.26	–	
Output Valid from Clock	t_{VD}	0	–	0	–	0	–	
Data input hold time	t_{DIH}	0	–	0	1.0	0	0.45	
Data input setup time	t_{DIS}	250	–	100	–	50	–	ns

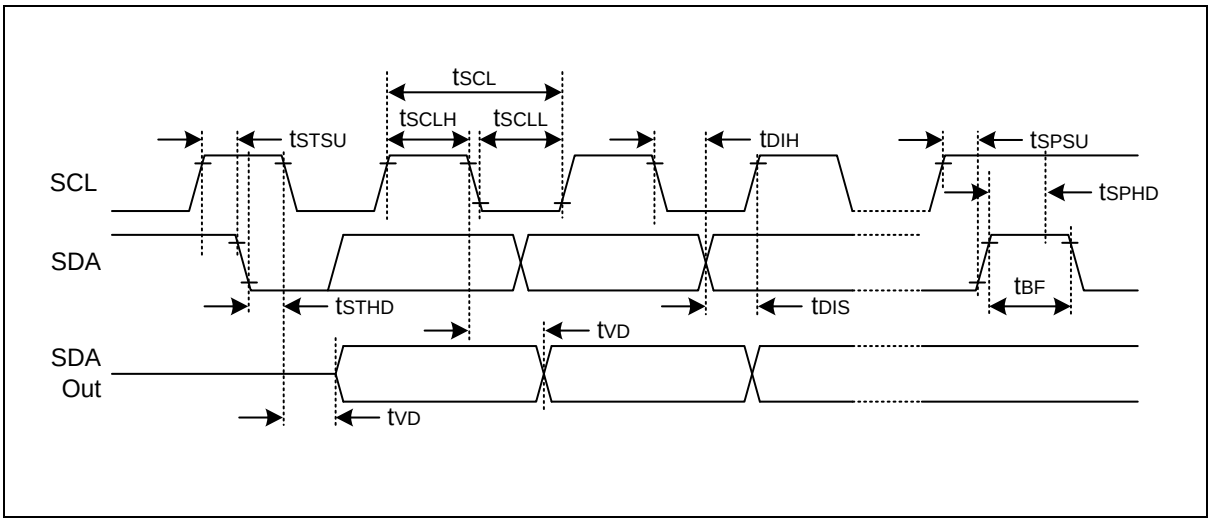


Figure 37. I2C Timing

14.15 UART timing characteristics

Table 34. UART Timing Characteristics (PCLK=11.1MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1,250	tCPU x 16	1,650	ns
Output data setup to clock rising edge	t_{S1}	590	tCPU x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	tCPU – 50	tCPU	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	tCPU x 8	970	

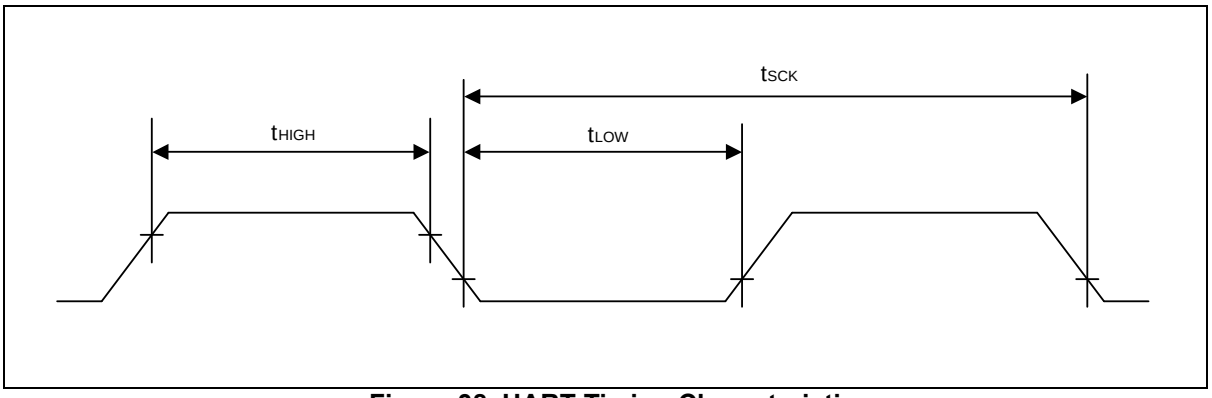


Figure 38. UART Timing Characteristics

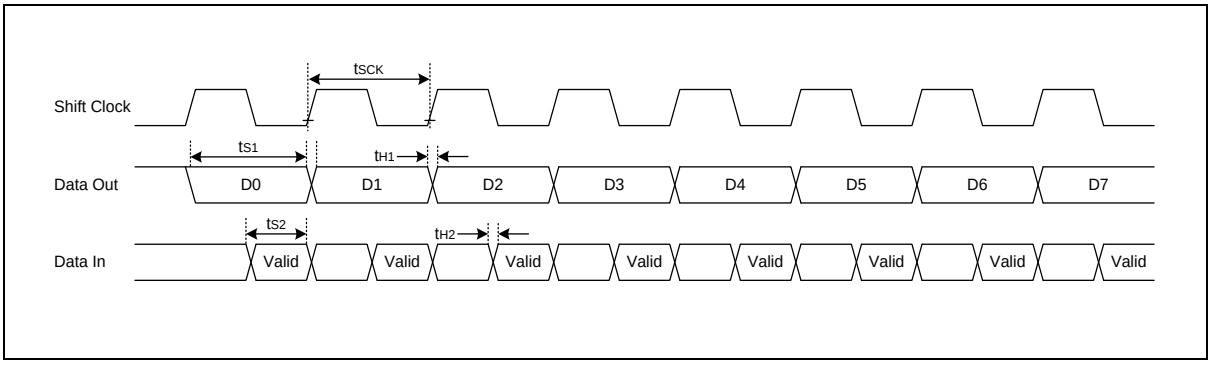


Figure 39. Timing Waveform of UART Module

14.16 Data retention voltage in Stop mode

Table 35. Data Retention Voltage in Stop Mode

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	• V_{DDDR} = 1.8V (T_A=25°C) • Deep sleep mode	–	–	1	µA

14.17 Internal flash characteristics

Table 36. Internal Flash Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Page write time	t_{FSW}	–		–	3.0	3.5	ms
Page erase time	t_{FSE}	–		–	3.0	3.5	
Chip erase time	t_{FCE}	–		–	3.0	3.5	
Flash program voltage	V_{PGM}	On erase/write		2.0	–	5.5	V
System clock frequency	f_{HCLK}	–		2.0	–	–	MHz
Endurance of Write/Erase	NF_{WE}	• Page 0 to 511 • Configure Option Page 1	T_A=25 °C, Page unit	10,000	–	–	Cycles
		Configure Option Page 2/3		100,000			
Retention time	t_{RT}			10	–	–	Years

14.18 Input/output capacitance

Table 37. Input/Output Capacitance

(VDD = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input capacitance	C_{IN}	• f=1MHz • Unmeasured pins are connected VSS	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

14.19 Main oscillator characteristics

Table 38. Main Oscillator Characteristics

(VDD = 2.2V to 5.5V)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	2.7 V to 5.5 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	2.2 V to 5.5 V	2.0	–	4.2	
		2.7 V to 5.5 V	2.0	–	16.0	
External Clock	XIN input frequency	3.0 V to 5.5 V	2.0	–	40.0	MHz
	External Clock Duty Ratio	–	–	50	–	%

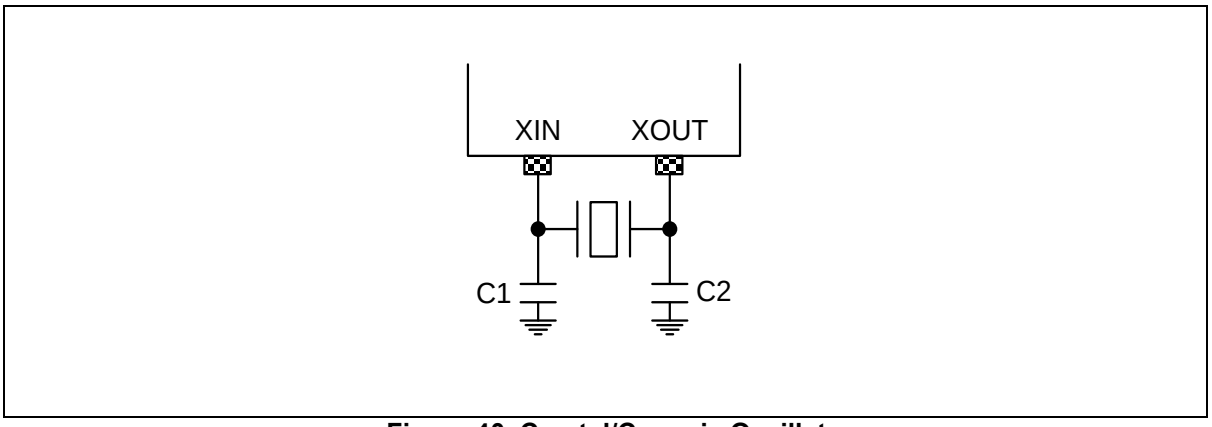


Figure 40. Crystal/Ceramic Oscillator

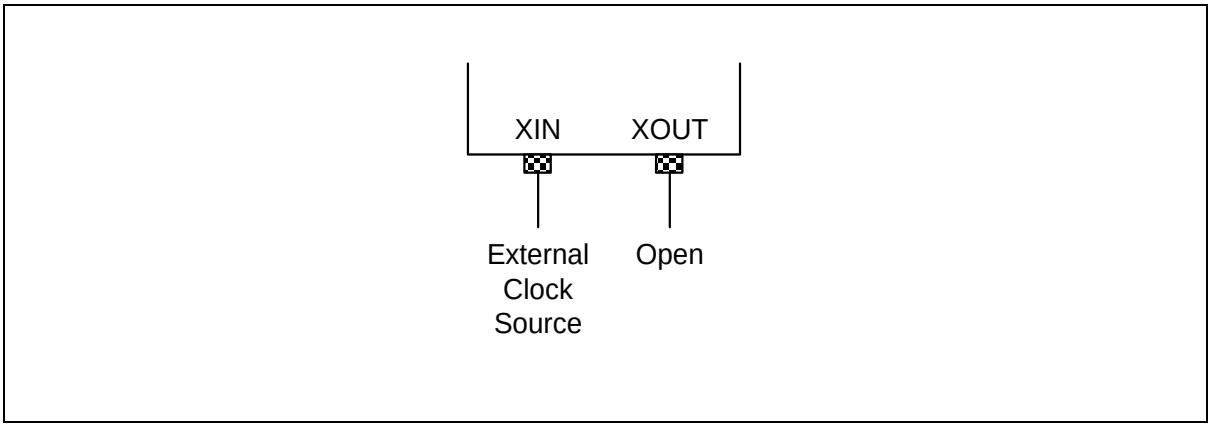


Figure 41. External Clock

14.20 Sub-oscillator characteristics

Table 39. Sub-oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	–	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	38	

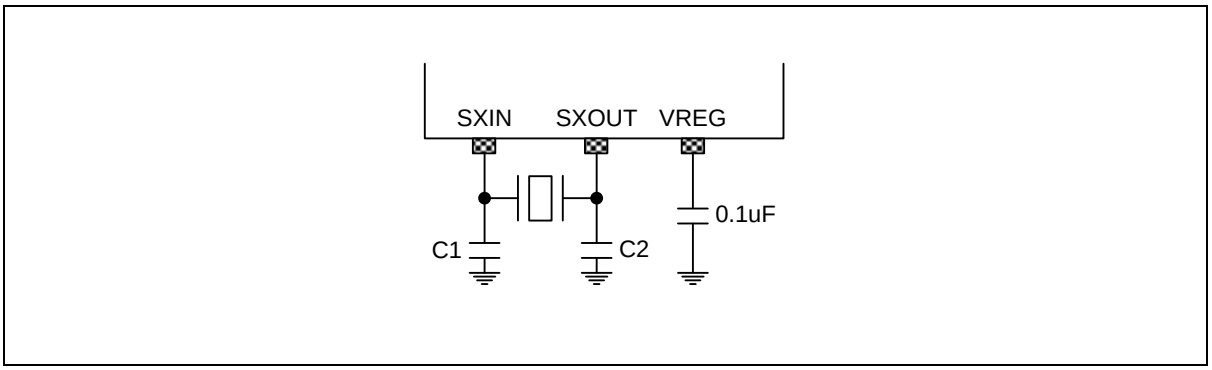


Figure 42. Crystal Oscillator

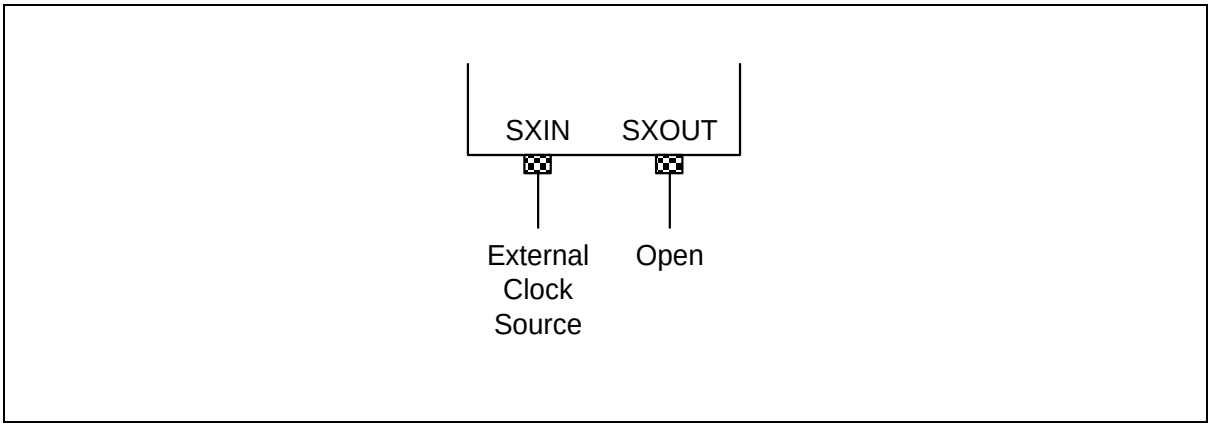


Figure 43. External Clock

14.21 Main oscillation stabilization time

Table 40. Main Oscillation Stabilization Time

Oscillator	Conditions		Min	Typ	Max	Unit
Crystal	• f_{XIN} ≥ 2MHz	VDD = 2.7V to 5.5V	–	–	60	ms
Ceramic	• Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	VDD = 2.2V to 5.5V	–	–	10	
External clock	• f_{XIN} = 2.0 to 40MHz • XIN input high and low width (t_{XL}, t_{XH})		12.5	–	250	ns

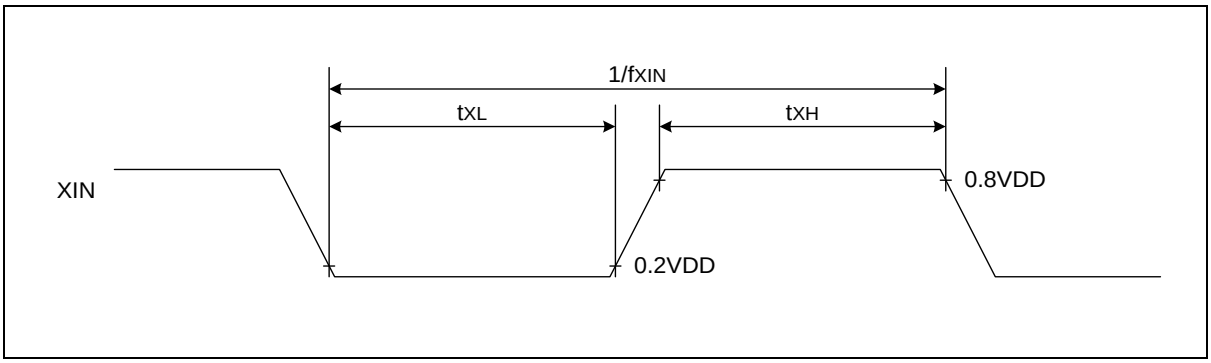


Figure 44. Clock Timing Measurement at XIN

14.22 Sub-oscillation stabilization time

Table 41. Sub-oscillation Stabilization Time

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD=3V, T_A=25 ˚C	–	0.7	1.5	
External clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	µs

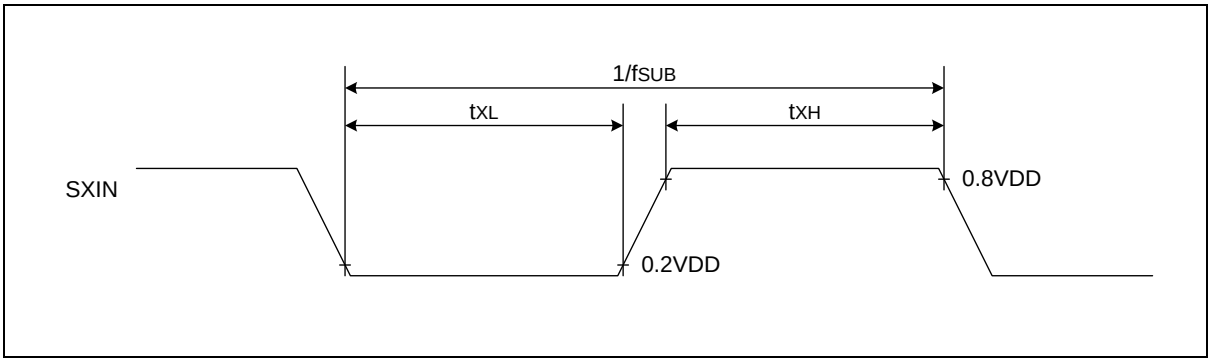


Figure 45. Clock Timing Measurement at SXIN

14.23 Operating voltage range

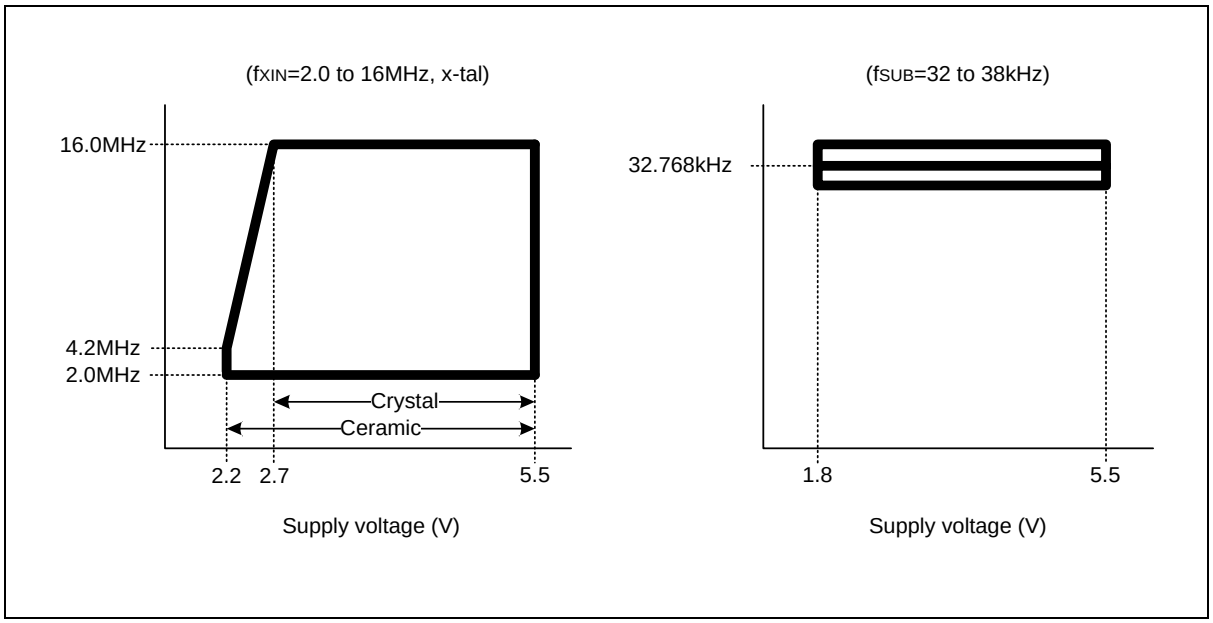


Figure 46. Operating Voltage Range

14.24 Recommended circuit and layout

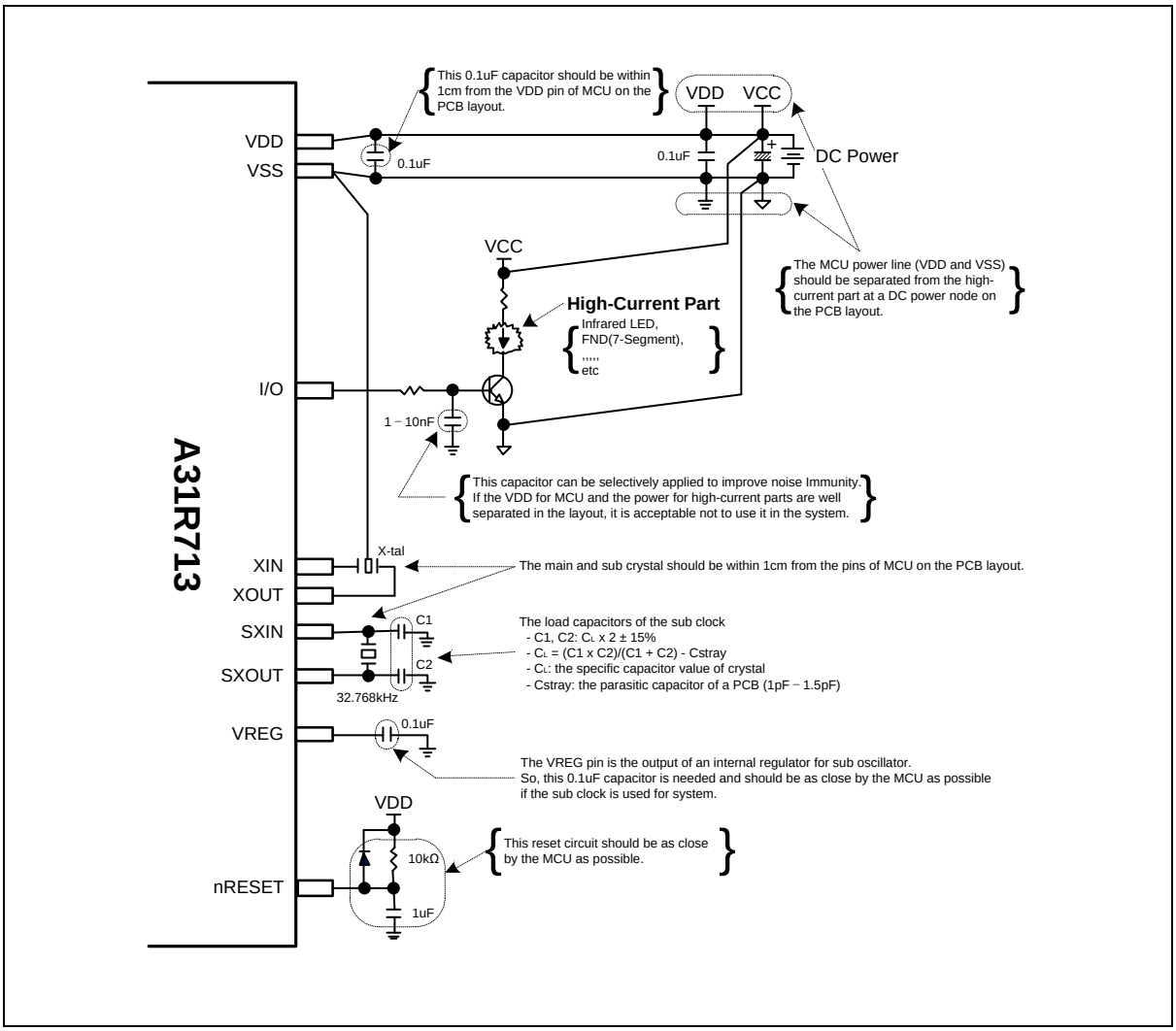
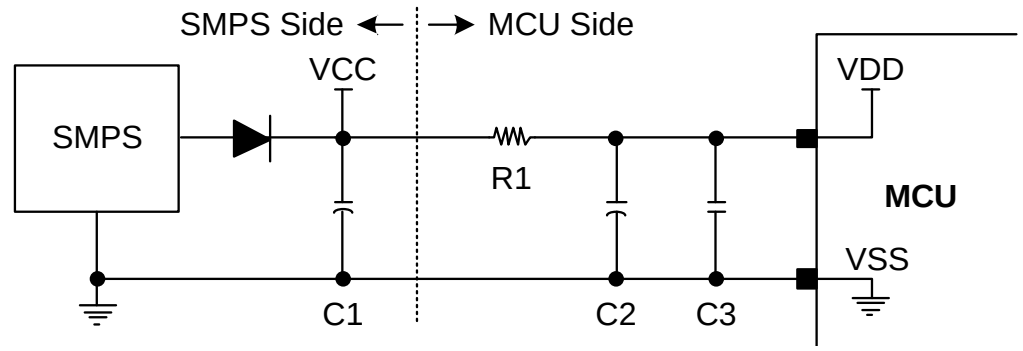


Figure 47. Recommended Circuit and Layout



NOTES:

1. Capacitor C1 is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470uF/25V more
2. Resistor R1 and capacitor C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10Ω - 20Ω
   - Recommended C2: 47uF/25V more
   - The R1 and C2 should be as close by the C3 as possible.
3. Capacitor C3 is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2uF more.
   - C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of MCU.

Figure 48. Recommended Circuit and Layout with SMPS Power

15 Package information

15.1 80 LQFP package information

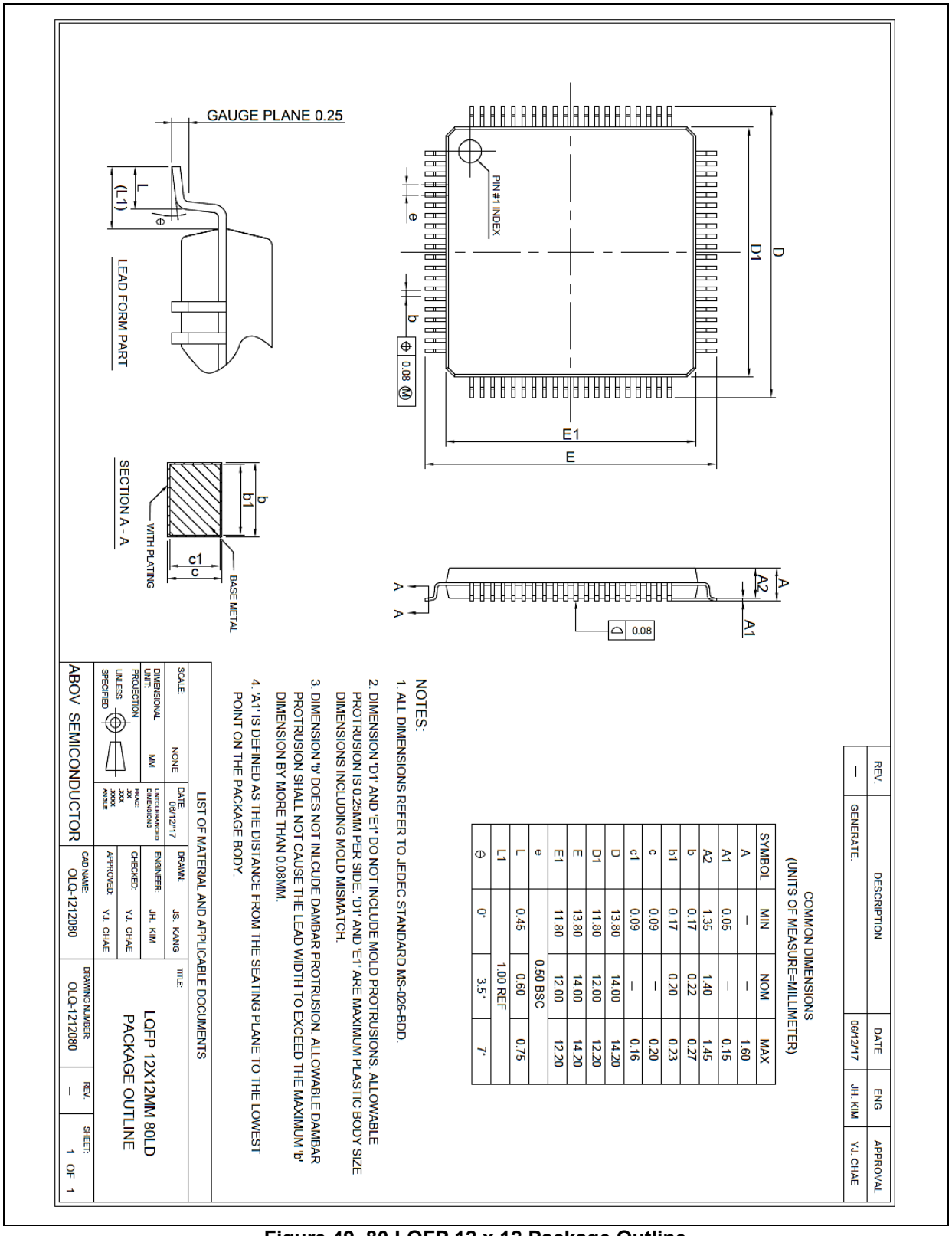


Figure 49. 80 LQFP 12 x 12 Package Outline

15.2 64 TQFP package information

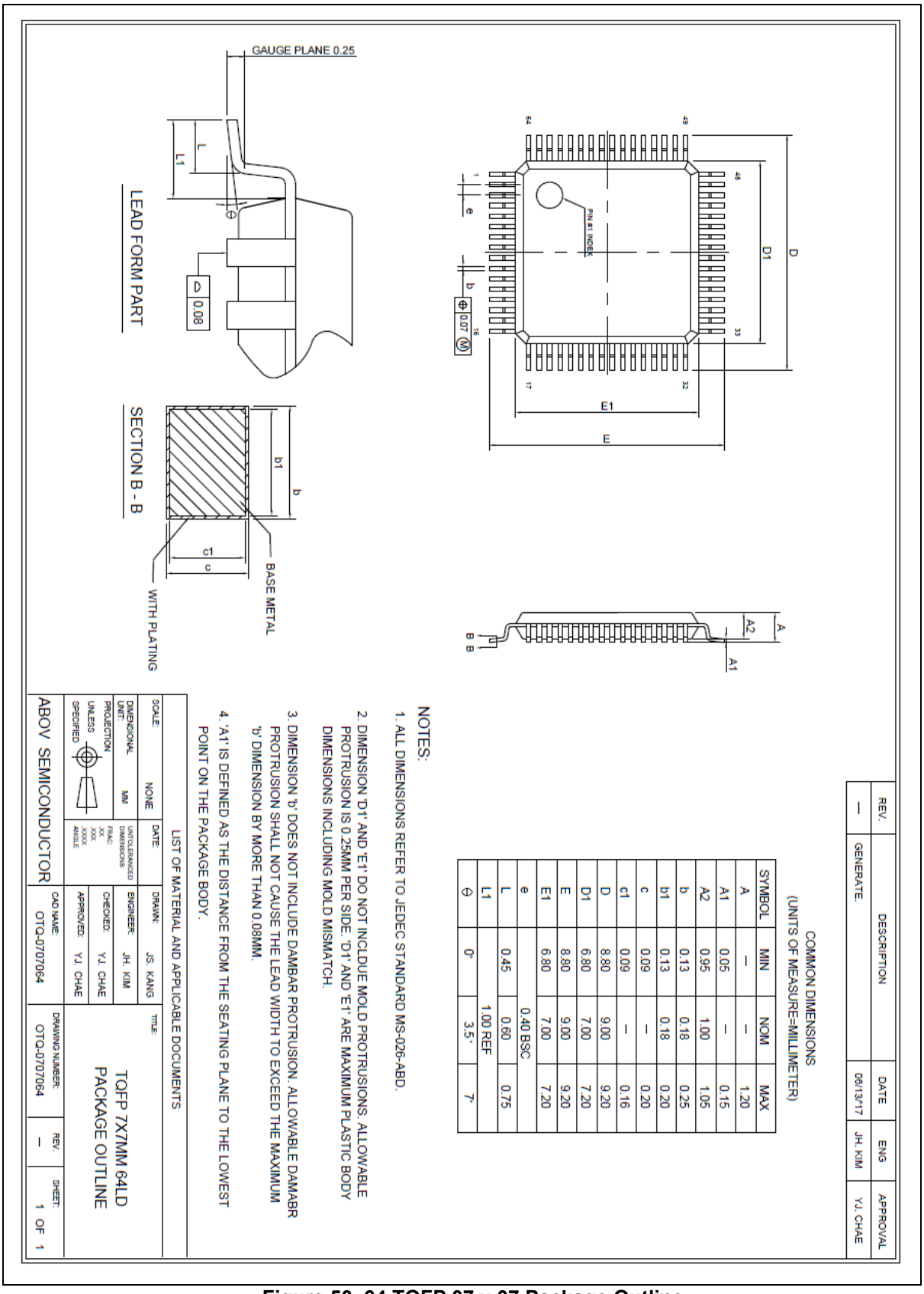


Figure 50. 64 TQFP 07 x 07 Package Outline

15.3 48 LQFP package information

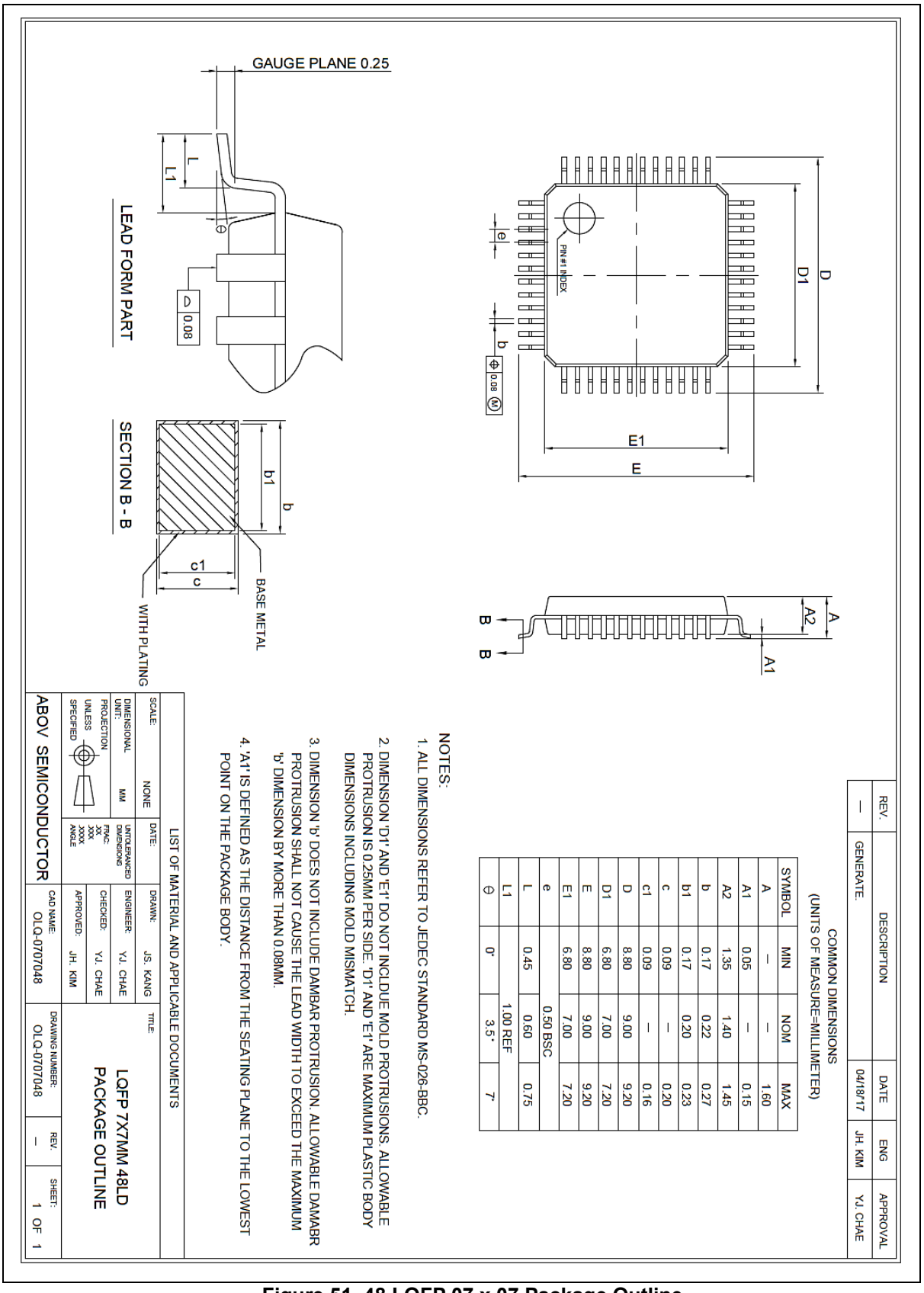


Figure 51. 48 LQFP 07 x 07 Package Outline

16 Ordering information

Table 42. A31R713 Ordering Information

Part Number	Flash	SRAM	USART	UART	I2C	TIMER	ADC	COM	SEG	I/O	Package
A31R713ML	64KB	8KB	2	1	1	8	11 ch	4	38	73	80LQFP-1212
A31R713RT*	64KB	8KB	2	1	1	7	11 ch	4	31	61	64TQFP-0707
A31R713CL*	64KB	8KB	2	1	1	5	8 ch	4	23	45	48LQFP-0707

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.

A31R71 3 M L N (T)

A31R71 family name

Code memory size

3	64Kbytes

Pin count

M	80 pins
R	64 pins
C	48 pins

Package type

L	LQFP1 (0.5mm pin pitch)
M	LQFP2 (0.65mm pin pitch)
T	TQFP

Temperature

None	-40 to +85℃ (commercial grade)
2	-40 to +105℃ (industrial grade, A31R713 is not supported)

Product information

N	Internal management code

Packing

(T)	Tape & reel
(W)	Wafer
(C)	Chip carrier

NOTE: For more information on any aspect of this device, please contact your nearest distributor or ABOV sales offices.

Figure 52. A31R713 Numbering Nomenclature

Revision history

Date	Version	Description
Feb.4, 2020	1.00	1st creation
Nov.30, 2020	1.01	Add a note about disabling “clock monitoring function”, “Chapter 5.6.19 SCU_CMONCR", clock monitoring control register in the user’s manual. Add notes about TXEn bit and RXEn bit, "Chapter 13.3.1 USARTn_CR1" USARTn control register 1 in the user’s manual.
Aug.11, 2021	1.02	Modify package dimension for fix typos, “Chapter 15 Package information”.
Oct.26, 2022	1.10	Change the document format.

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