32-bit Cortex-M3 based General Purpose Microcontroller

FlashROM 384 · 256 · 128KB / DataFlashROM 32KB / SRAM 24KB

A33G52x

Datasheet

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2020.09.18

Histoy of changes

Date	Person	Version	Changes
2017/12/07	S.H.Kim	Ver1.0	Published standard version
2017/12/23	S.H.Kim	Ver1.0	Modified the description of PMU_PER, PMU_PCCR registers Changed block diagram of PMU
2018/01/04	S.H.Kim	Ver1.0.1	Modified descriptions of Table 1.2 Replaced TRACEDIV with Reserved FMC_AR description and register
2018/01/18	S.H.Kim	Ver1.0.2	Modified block diagrams of PMU, Timer, I2C, SPI, UART, ADC, etc. Added Nomenclature of A33G52x (Figure 1.2) Modified the description of PMU_CMR, PMU_MCMR
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2020/09/18	S.H.Kim	Ver1.0.18	Added Maximum Operating Junction Temperature (T_J) Specification

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CHAPTER 1. Overview

1.1 Overview

A33G52x processor is designed for the main controller of various household appliances.In particular, accordance with the tendency that the microcontroller is becoming more complicated and high performance in consumer electronics, ARM's high-speed 32-bit Cortex-M3 Core is used. In addition, for handling more features, this microcontroller has a variety of peripheral devices and large amounts of flash memory.

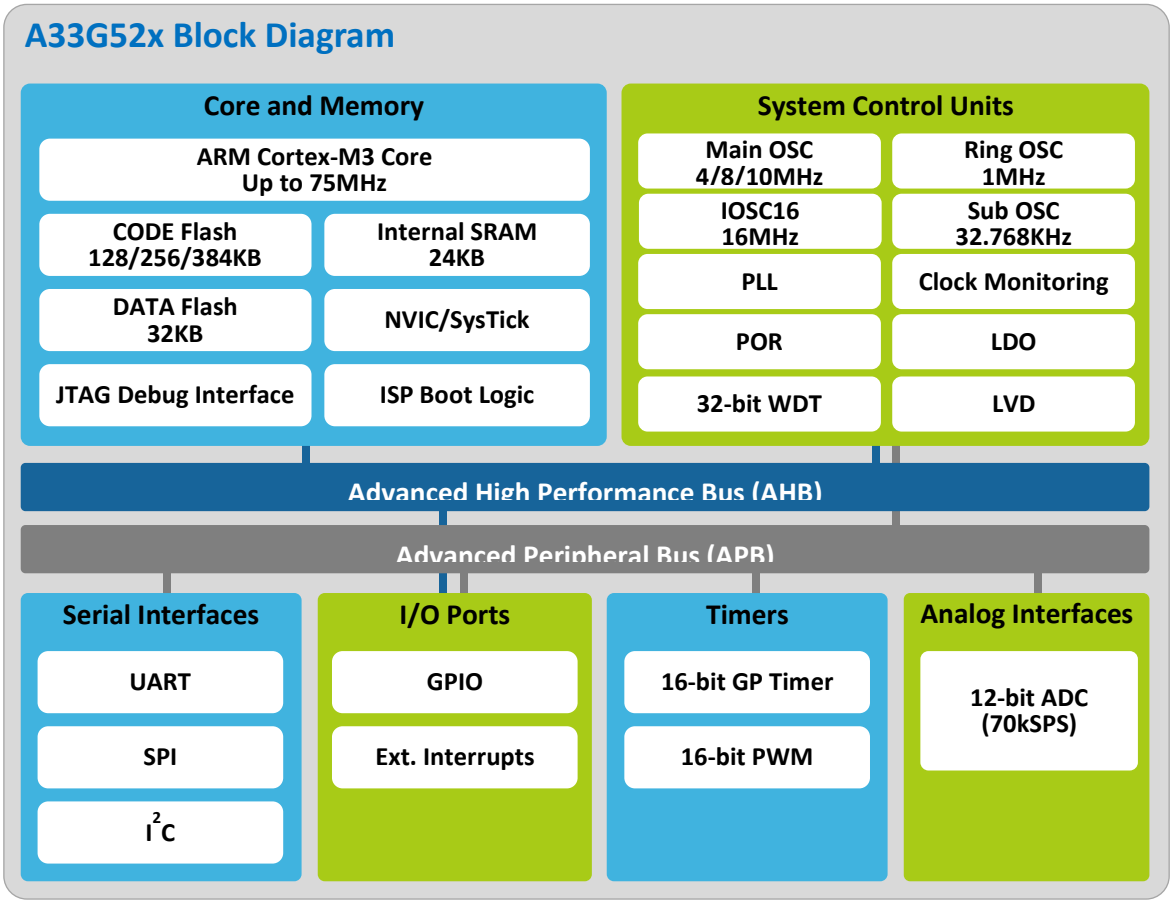


Figure 1.1. Block diagram of A33G52x Series MCUs

1.2 Ordering Information

Table 1.1. Ordering Information

Product Name	CODE Flash [KB]	DATA Flash [KB]	SRAM [KB]	UART [ch]	SPI [ch]	I2C [ch]	PWM [ch]	12-bit ADC [ch]	I/O Ports [ch]	Package
A33G527VQ	384	32	24	4	2	2	8	16	90	100 MQFP
A33G527VL	384	32	24	4	2	2	8	16	90	100 LQFP14
A33G527RL	384	32	24	4	2	2	8	10	60	64 LQFP12
A33G526VQ	256	32	24	4	2	2	8	16	90	100 MQFP
A33G526VL	256	32	24	4	2	2	8	16	90	100 LQFP14
A33G526MM	256	32	24	4	2	2	8	15	71	80 LQFP14
A33G526ML	256	32	24	4	2	2	8	15	71	80 LQFP12
A33G526RL	256	32	24	4	2	2	8	10	60	64 LQFP12
A33G526RM	256	32	24	4	2	2	8	10	60	64 LQFP10
A33G524MM	128	32	24	4	2	2	8	15	71	80 LQFP14
A33G524ML	128	32	24	4	2	2	8	15	71	80 LQFP12
A33G524RL	128	32	24	4	2	2	8	10	60	64 LQFP12
A33G524RM	128	32	24	4	2	2	8	10	60	64 LQFP10

1.3 Main Features

A33G52x has a Cortex-M3 32-bit embedded core, and has a variety of peripherals. A brief description of each part is as follows:

Table 1.2. Outline of Specifications

Category	Module	Description
Core	CPU	○ Max. Speed : 75 MHz ○ 32-bit ARM Cortex-M3 CPU ○ CPU Register Set General Purpose Register : 32-bit Thumb-2 Instruction Main Stack Pointer (MSP) & Process Stack Pointer (PSP) : R13 Link Register (LR) : R14 Program Counter (PC) : R15 ○ Data Alignment: Little endian ○ Harvard Architecture ○ AHB/APB
	Interrupt	○ NVIC (Nested-Vectored Interrupt Controller) ○ 64 Peripheral Interrupts ○ 3-bit width of Group Priority: 8-step priority.
Memory	Code Flash	○ Capacity : 384KB (A33G527) 256KB (A33G526) 128KB (A33G524) ○ Built-in high capacity code flash memory ○ Max. 25 MHz Flash Access Timing ○ 1Byte unit PROGRAM ○ 512Bytes or 1KB Sector ERASE ○ Self-PROGRAM 1-word (4 Bytes) PROGRAM Supports to update data in some Code Flash memory region during execution of user program in Code area. ○ CRC16 generation and verification of data in code flash. ○ Endurance : 10,000 cycles ○ Lifetime : 10 years
	Data Flash	○ Capacity: 32KB ○ Max. 25 MHz Flash Access Timing ○ 1Byte unit PROGRAM, ○ 1KB unit Sector ERASE ○ CRC16 generation and verification of data in data flash. ○ Endurance : 100,000 cycles ○ Lifetime : 10 years

	Boot Rom	○ Enter the boot mode of the processor according to the external BOOT pin input ○ SPI and UART Interfaces in BOOT mode ○ In System Programming User data can be programmed in the internal flash memory on the application board in BOOT mode.
	SRAM	○ Capacity: 24KB ○ Available as a program region ○ Suitable high-speed operation for time-critical code execution. ○ The SRAM area is partially remapped to the interrupt vector area.
PMU (Power Management Unit)	Operation Modes	○ Run Mode (Run) ○ Sleep Mode (Idle) ○ Deep-Sleep Mode (Power Down)
	Clock	○ 1MHz Internal Ring Oscillator (RINGOSC) ○ 16MHz Internal Oscillator (IOSC16) ○ 4~10MHz External Main Oscillator (MXOSC) ○ 32.768kHz External Auxiliary Oscillator (SXOSC) ○ PLL Frequency synthesizer (PLL) High frequency operation (Max. 75MHz Output Frequency) 1MHz-unit fine-tuning of output frequency. ○ Main system clock monitoring. ○ External oscillation clock monitoring and non-oscillation error handling function. ○ Frequency dividing function for main system clock (HCLK) and peripheral device module clock (PCLK).
	Reset	Reset events are occurred by below reset sources : ○ Main Clock Fail ○ External nRESET Pin ○ Core reset ○ Software Reset ○ POR (Power-On Reset) ○ LVD (Low Voltage-Monitoring) Reset ○ External main oscillation error
	LDO (Low Drop Out)	○ Integrated LDO (Low Drop Out) for low-power operation
	POR (Power On Reset)	○ Internal core voltage monitoring and reset signal generation
	LVD (Low Voltage Detector)	○ 8-step voltage detection level ○ LVD (Low Voltage Detector) reset ○ LVD Interrupt ○ Wake-up by LVD function after sleep or deep-sleep mode.

	Low-Power Consumption	○ Low-power operation mode Sleep mode (Idle) Deep Sleep Mode (Power Down)
	Wake-up Event	Wake-up events are occurred by below wake-up sources : ○ GPIOA~GPIOF ○ FRT ○ Failure of external main oscillation ○ WDT ○ LVD ○ Rapid wake-up operation with internal oscillator and external clock source
GPIO	PCU GPIO	○ General purpose I/O Ports ○ 100-pin LQFP/MQFP I/O pins: 90 ○ 80-pin MQFP I/O pins: 71 ○ 64-pin LQFP I/O pins: 60 ○ Configuration of pin mode Push-Pull Output Open-Drain Logic Input Analog Input ○ Setting pin function using MUX ○ High/Low Level detection and Interrupt ○ Rising/Falling edge detection and interrupt ○ Setting Pull-up/Pull-down/Debounce ○ Large-current Port (Port D) ○ Separate bit set/reset function ○ Wake-up event by external asynchronous input

Timer	16-bit Timer	○ 16-bit general purpose up-count timer ○ 10 channels TnC: Timer input 10-ch TnO: Timer output 10-ch ○ Timer operation modes Periodic timer mode Counter mode PWM mode Capture mode ○ Interrupt Events Timer/Counter match interrupt Timer overflow interrupt ○ Timer Input clock MXOSC/IOSC16/SXOSC/RINGOSC Timer input by external TnC pin in capture mode ○ Output timer clock signal by external TnO pin ○ 10-bit prescaler
	WDT	○ 32-bit down-count timer ○ Reset event and peridic Interrupt ○ MXOSC/IOSC16/SXOSX/RINGOSC clock source selection ○ 8-step prescaler
	FRT	○ 32-bit Free-run Timer system internal's time calculation 32-bit up-count timer ○ Periodic interrupt mode Occurred timer interrupt according to the time interval set by the user. Integrated comparator for match interrupt ○ Overflow interrupt ○ 8-step prescaler
PWM (Pulse-Width Modulation)	PWM	○ PWM generator with 8 channels ○ PWM signal with 16-bit independent counter ○ consists of 1-unit per 4 channels. ○ 8-bit prescaler per 1 unit ○ Configuration of duty and period of PWM output signal ○ 1/2, 1/4, 1/8, 1/16 clock divider ○ 16-bit period and count value set ○ built-in channels that outputs inverted PWM signal

Serial Interfaces	I2C	○ Standard I2C communication specification ○ 2 channels ○ Supports master/slave per channel ○ 7-bit slave address ○ Byte-by-byte data communication by interrupt and polling type ○ I2C Max. transfer rate: 400kbps ○ Configuring I2C clock and data signal latency
	SPI	○ 2 channels synchronous serial communication port ○ Double buffer structure for high-speed transmission ○ Master / slave selection function of communication channel ○ Setting function for transmission data Number of bits (8/9/16/17 bit variable) SPI clock speed LSB-first or MSB first transmission ○ Supports SPI0 channel when entering BOOT mode.
	UART	○ 16550/16450 compatible asynchronous serial communication port ○ 4 channels 16550- compliant device with 2-channel FIFO 16450-compliant device with two-channel double buffer ○ Built-in fractional point divider to improve baud rate accuracy. ○ Supports UART0 channel when entering BOOT mode. ○ Single/Multi-Sampling of receiving data
12-bit A/D converter	ADC	○ 12-bit resolution ○ Single SAR A/D converter ○ Built-in Analog MUX for multiple input ○ Input voltage for ADC conversion GNDV ~ AVDDV ○ 70kSPS A/D conversion time Max. 15us/channel (AVDD=5.0V, A/D conversion clock=4MHz) ○ Interrupt of end of A/D conversion ○ Trigger source of A/D conversion: Timer 7-channels ○ A/D conversion by internal START bit or external trigger source ○ Channels 100-pin LQFP/MQFP : 16-ch x 1-unit 80/64-pin LQFP : 10-ch x 1-unit
Debug	Debug Interfaces	○ 100-pin MQFP/LQFP Trace / JTAG / SWD ○ 80-pin LQFP JTAG / SWD ○ 64-pin LQFP JTAG / SWD

1.4 Block Diagram

A33G52x is shown as below consists of a variety of peripheral devices.

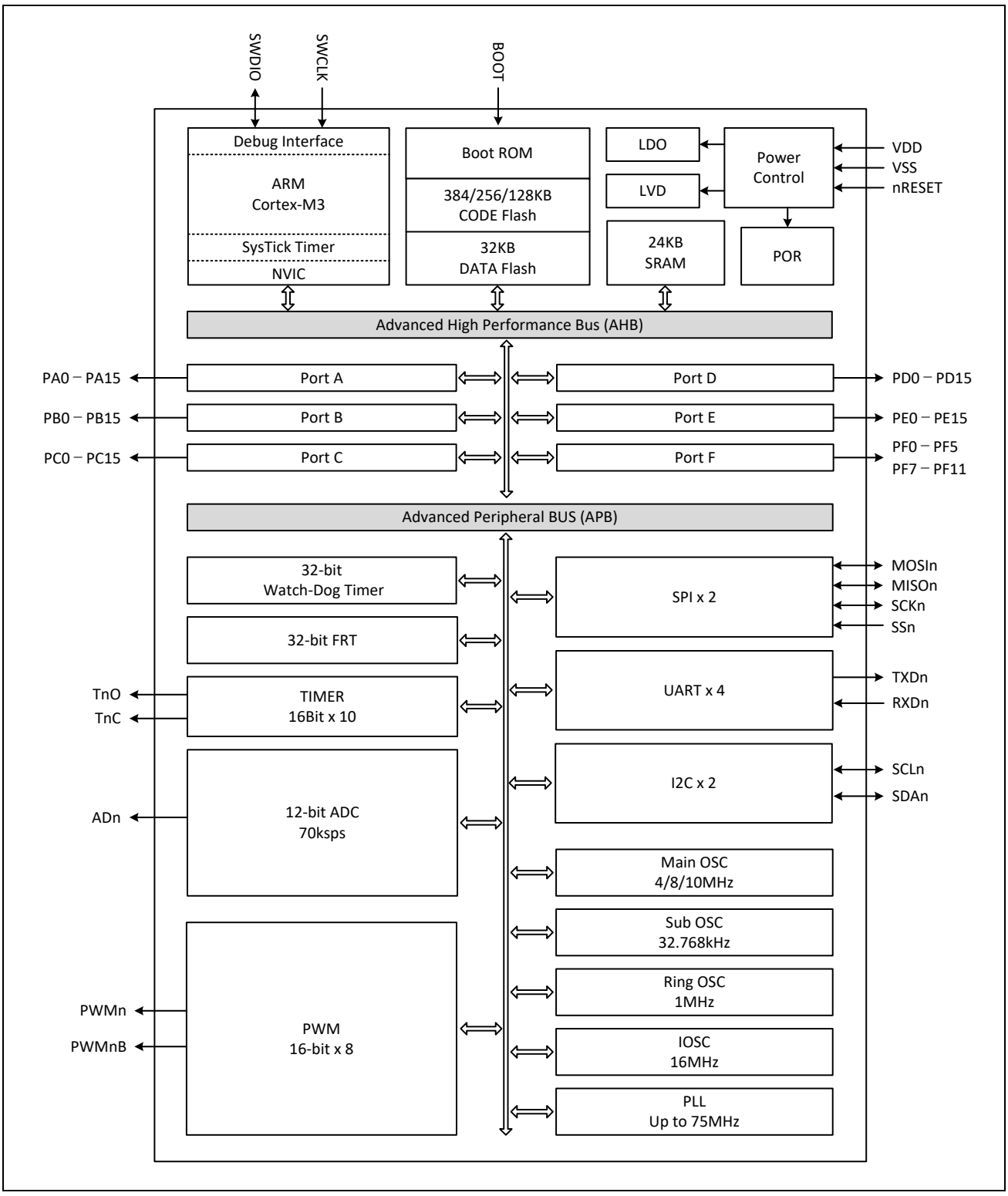


Figure 1.2. Internal block diagram of A33G52x MCUs

1.5 Pin Layout of Packages

1.5.1 A33G527VQ / A33G526VQ (100MQFP)

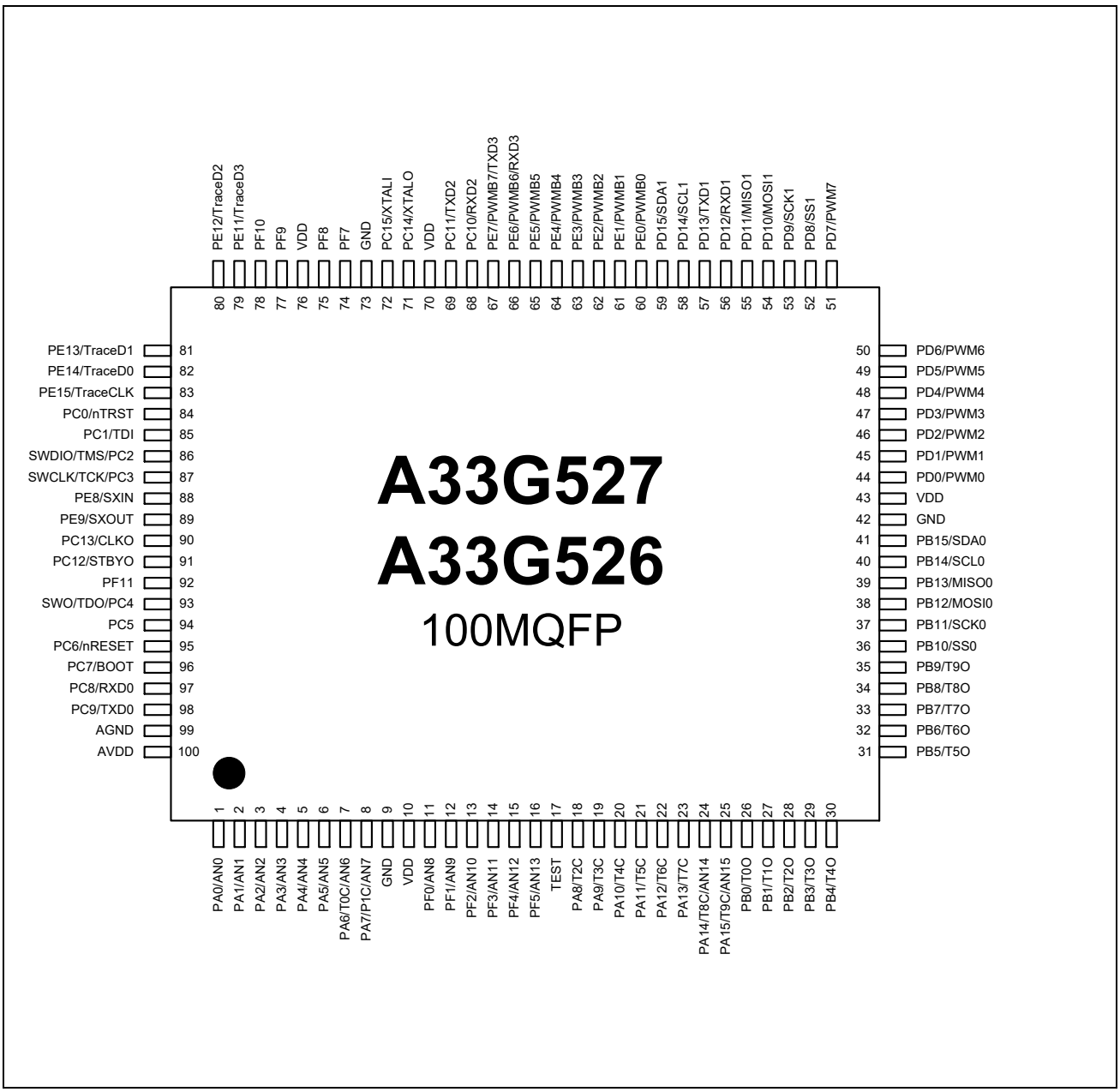


Figure 1.3. Pin layout of . A33G527VQ / A33G526VQ (100MQFP)

1.5.2 A33G527VL / A33G526VL (100LQFP14)

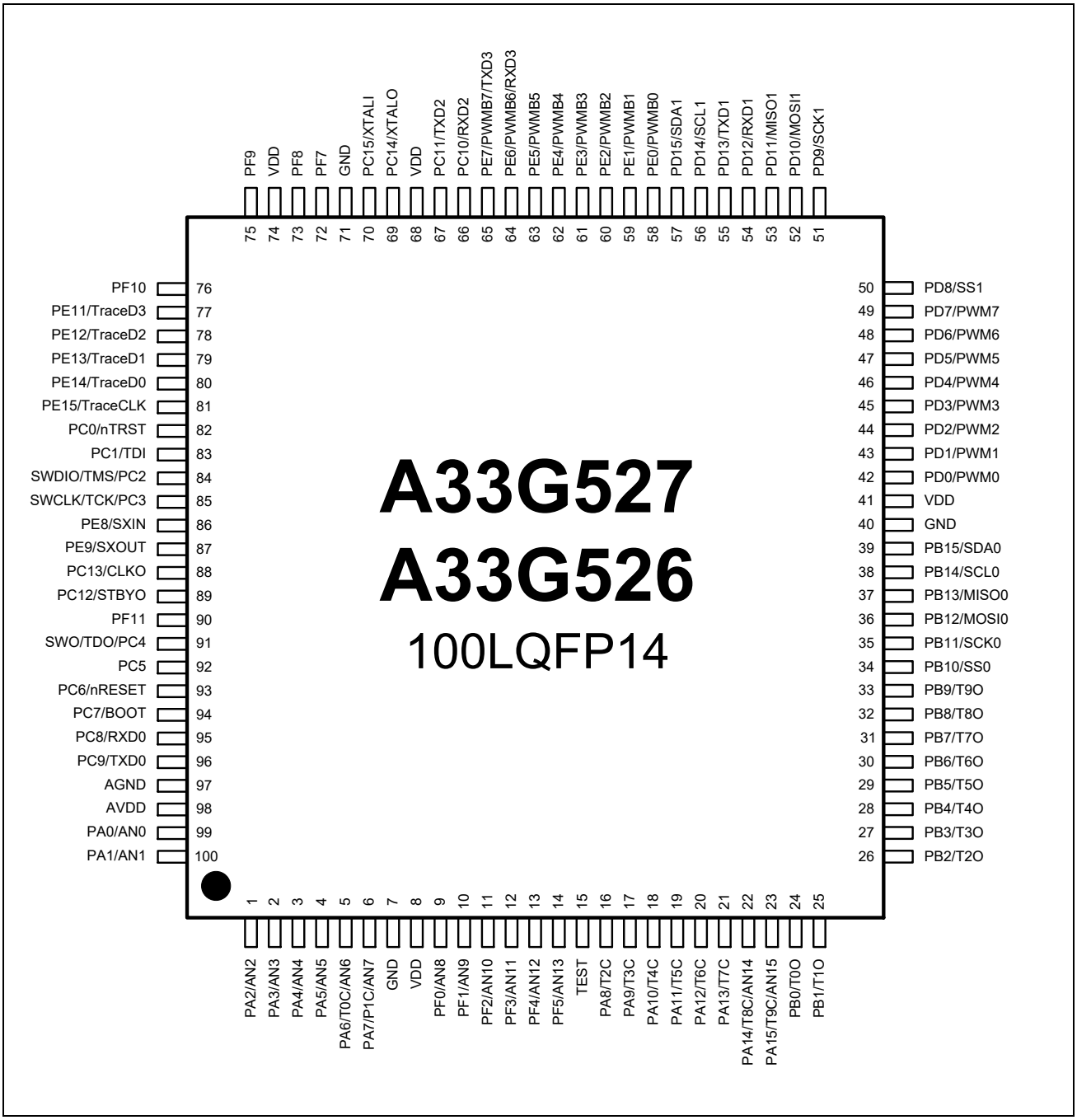


Figure 1.4. Pin layout of . A33G527VL / A33G526VL (100LQFP14)

1.5.3 A33G526MM / A33G524MM (80LQFP14)

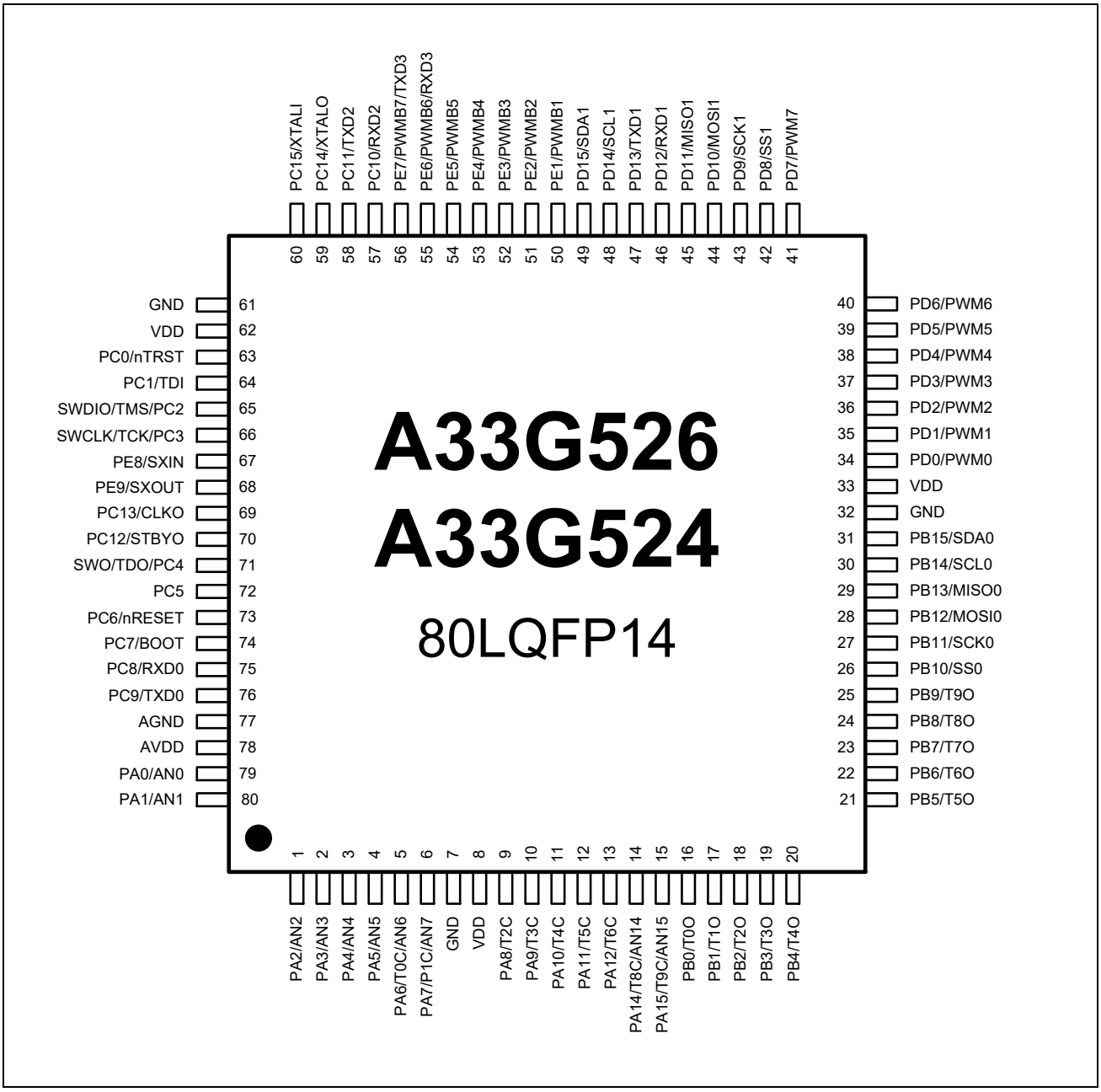


Figure 1.5. Pin layout of . A33G526MM / A33G524MM (80LQFP14)

1.5.4 A33G526ML / A33G524ML (80LQFP12)

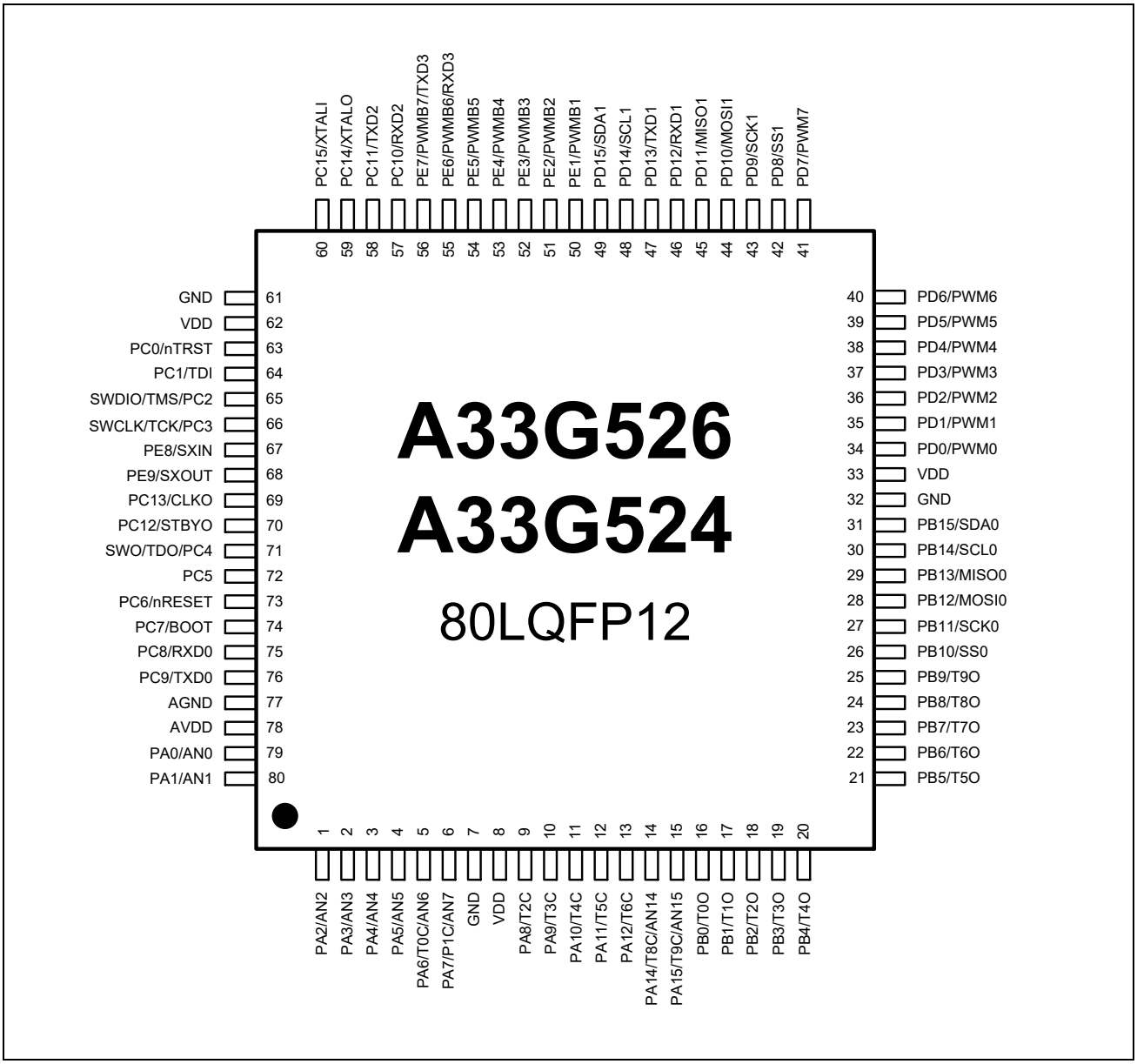


Figure 1.6. Pin layout of . A33G526ML / A33G524ML (80LQFP12)

1.5.5 A33G527RL / A33G526RL / A33G524RL (64LQFP12)

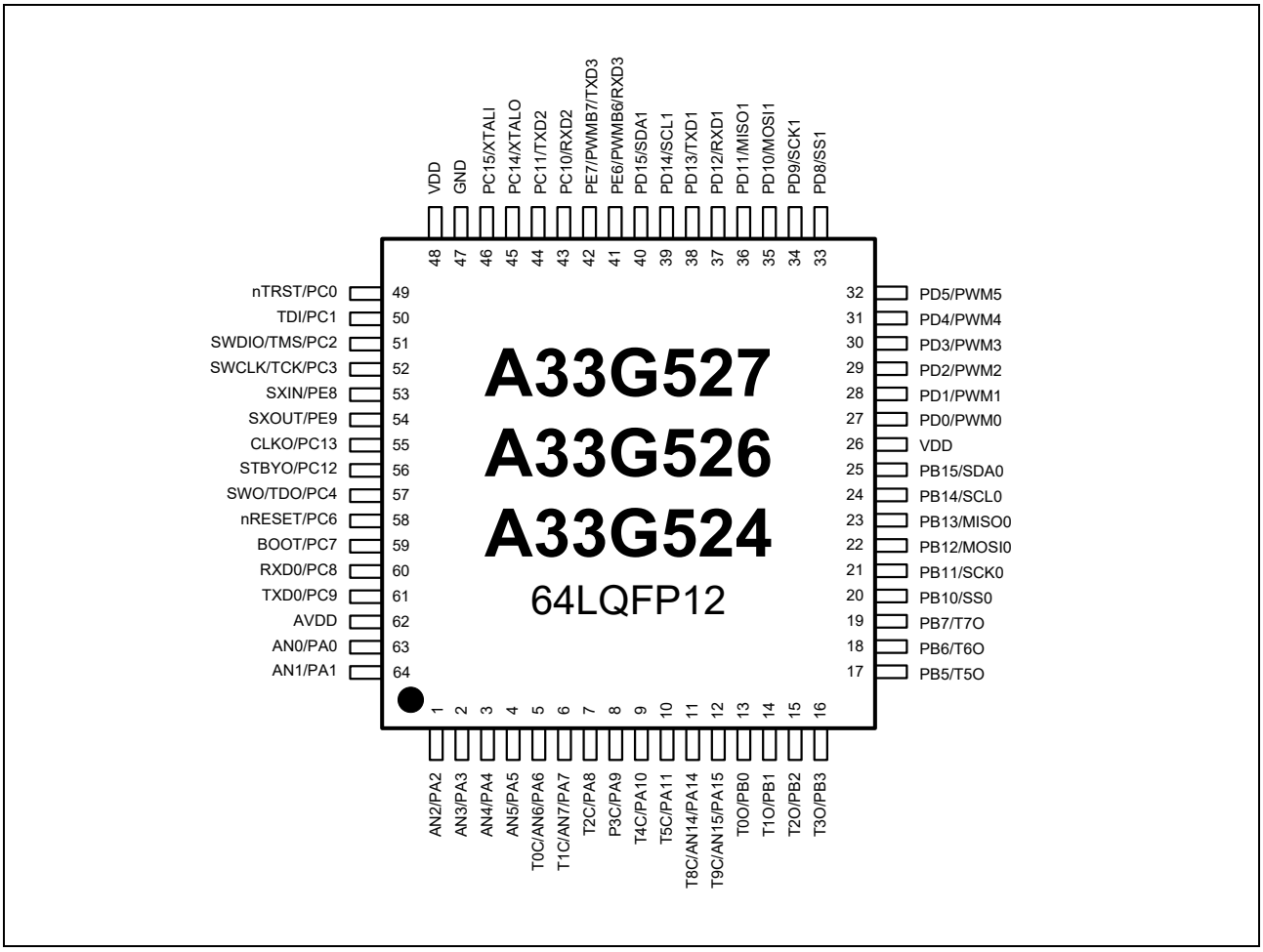


Figure 1.7. Pin layout of . . A33G527RL / A33G526RL / A33G524RL (64LQFP12)

1.5.6 A33G526RM / A33G524RM (64LQFP10)

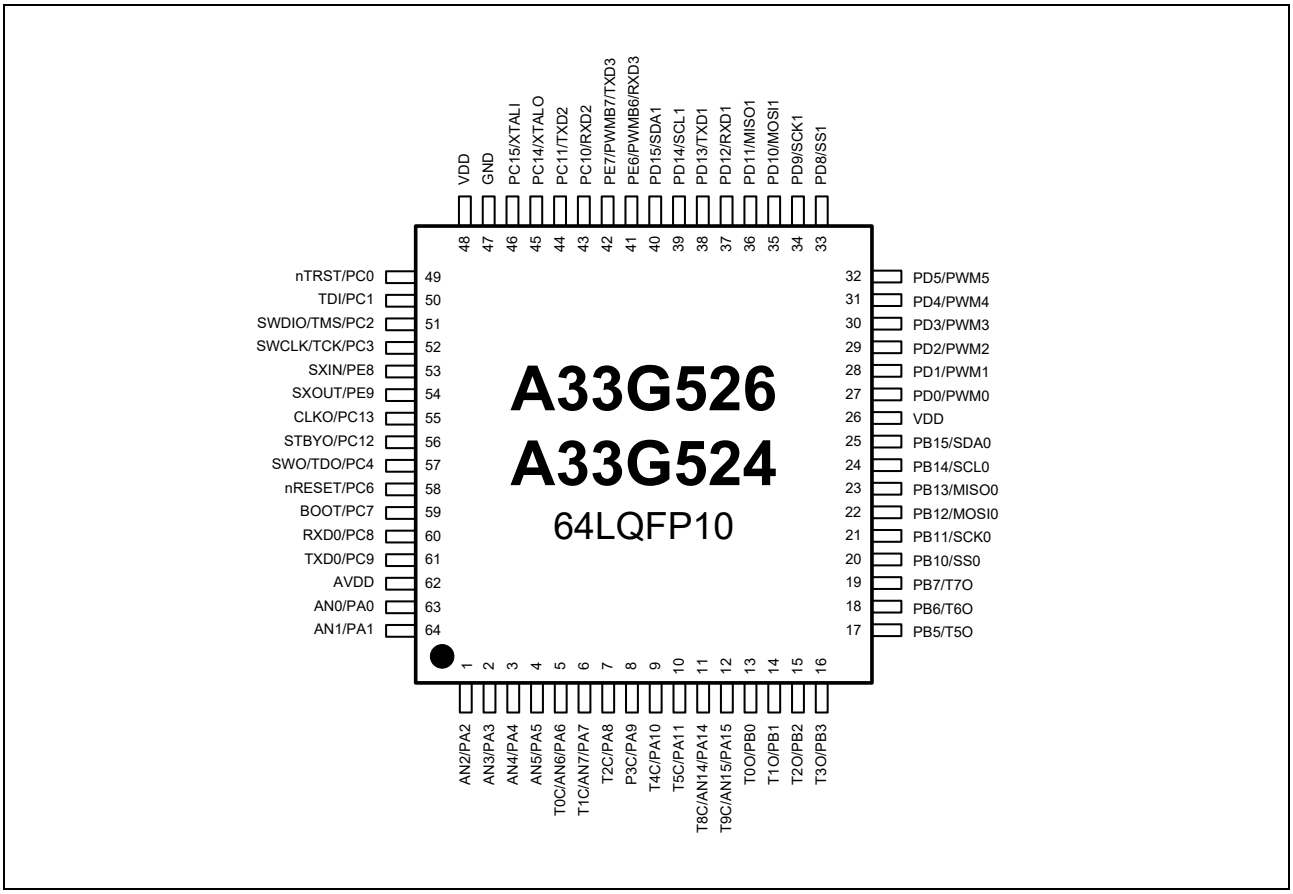


Figure 1.8. Pin layout of . A33G526RM / A33G524RM (60LQFP10)

1.6 Pin Configuration

Depending on the package type of each A33G52x microcontroller, there are some differences in the number of pins and configurations.
The pin configuration of A33G52x MCUs is as follows.

Table 1.3 Pin Configuration

Pin Number				Name	Type	Description	Remark
100LQFP14	100MQFP	80LQFP14 80LQFP12	64LQFP12 64LQFP10				
99	1	79	63	PA0*	IOUS	GPIO A bit	
				AN0	IA	ADC input 0	
100	2	80	64	PA1*	IOUS	GPIO A bit 1	
				AN1	IA	ADC input 1	
1	3	1	1	PA2*	IOUS	GPIO A bit 2 input/output	
				AN2	IA	ADC INPUT 2	
2	4	2	2	PA3*	IOUS	GPIO A bit 3 input/output	
				AN3	IA	ADC INPUT 3	
3	5	3	3	PA4*	IOUS	GPIO A bit 4 input/output	
				AN4	IA	ADC INPUT 4	
4	6	4	4	PA5*	IOUS	GPIO A bit 5 input/output	
				AN5	IA	ADC INPUT 5	
5	7	5	5	PA6*	IOUS	GPIO A bit 6 input/output	
				T0C	IPUS	Timer 0 Clock/Capture input	
				AN6	IA	ADC INPUT 6	
6	8	6	6	PA7*	IOUS	GPIO A bit 7 input/output	
				T1C	IUS	Timer 1 Clock/Capture input	
				AN7	IA	ADC INPUT 7	
7	9	7	-	GND	P	GND	
8	10	8	-	VDD	P	VDD (3.0~ 5.5V)	
9	11	-	-	PF0*	IOUS	GPIO F bit 0 input/output	
				AN8	IA	ADC INPUT 8	
10	12	-	-	PF1*	IOUS	GPIO F bit 1 input/output	
				AN9	IA	ADC INPUT 9	
11	13	-	-	PF2*	IOUS	GPIO F bit 2 input/output	
				AN10	IA	ADC INPUT 10	
12	14	-	-	PF3*	IOUS	GPIO F bit 3 input/output	
				AN11	IA	ADC INPUT 11	
13	15	-	-	PF4*	IOUS	GPIO F bit 4 input/output	
				AN12	IA	ADC INPUT 12	
14	16	-	-	PF5*	IOUS	GPIO F bit 5 input/output	
				AN13	IA	ADC INPUT 13	
15	17	-	-	TEST	IDS	Test mode input (default Pull-down)	
16	18	9	7	PA8*	IOUS	GPIO A bit 8 input/output	
				T2C	IUS	Timer 2 Clock/Capture input	
17	19	10	8	PA9*	IOUS	GPIO A bit 9 input/output	
				T3C	IUS	Timer 3 Clock/Capture input	
18	20	11	9	PA10*	IOUS	GPIO A bit 10 input/output	
				T4C	IUS	Timer 4 Clock/Capture input	
19	21	12	10	PA11*	IOUS	GPIO A bit 11 input/output	
				T5C	IUS	Timer 5 Clock/Capture input	
20	22	13	-	PA12*	IOUS	GPIO A bit 12 input/output	
				T6C	IUS	Timer 6 Clock/Capture input	
21	23	-	-	PA13*	IOUS	GPIO A bit 13 input/output	
				T7C	IUS	Timer 7 Clock/Capture input	
22	24	14	11	PA14*	IOUS	GPIO A bit 14 input/output	
				T8C	IUS	Timer 8 Clock/Capture input	
				AN14	IA	ADC INPUT 14	

23	25	15	12	PA15*	IOUS	GPIO A bit 15 input/output	
				T9C	IUS	Timer 9 Clock/Capture input	
				AN15	IA	ADC INPUT 15	
24	26	16	13	PB0*	IOUS	GPIO B bit 0 input/output	
				T0O	OUS	Timer 0 Output	
25	27	17	14	PB1*	IOUS	GPIO B bit 1 input/output	
				T1O	OUS	Timer 1 Output	
26	28	18	15	PB2*	IOUS	GPIO B bit 2 input/output	
				T2O	OUS	Timer 2 Output	
27	29	19	16	PB3*	IOUS	GPIO B bit 3 input/output	
				T3O	OUS	Timer 3 Output	
28	30	20	-	PB4*	IOUS	GPIO B bit 4 input/output	
				T4O	OUS	Timer 4 Output	
29	31	21	17	PB5*	IOUS	GPIO B bit 5 input/output	
				T5O	OUS	Timer 5 Output	
30	32	22	18	PB6*	IOUS	GPIO B bit 6 input/output	
				T6O	OUS	Timer 6 Output	
31	33	23	19	PB7*	IOUS	GPIO B bit 7 input/output	
				T7O	OUS	Timer 7 Output	
32	34	24	-	PB8*	IOUS	GPIO B bit 8 input/output	
				T8O	OUS	Timer 8 Output	
33	35	25	-	PB9*	IOUS	GPIO B bit 9 input/output	
				T9O	OUS	Timer 9 Output	
34	36	26	20	PB10*	IOUS	GPIO B bit 10 input/output	
				SS0	IOUS	SPI Channel 0 Select Signal input/output	
35	37	27	21	PB11*	IOUS	GPIO B bit 11 input/output	
				SCK0	IOUS	SPI Channel 0 Clock Signal input/output	
36	38	28	22	PB12*	IOUS	GPIO B bit 12 input/output	
				MOSI0	IOUS	SPI Channel 0 Master Out/Slave In Signal	
37	39	29	23	PB13*	IOUS	GPIO B bit 13 input/output	
				MISO0	IOUS	SPI Channel 0 Master In/Slave Out Signal	
38	40	30	24	PB14*	IOUS	GPIO B bit 14 input/output	
				SCL0	OUS	I2C Channel 0 SCL Signal	
39	41	31	25	PB15*	IOUS	GPIO B bit 15 input/output	
				SDA0	OUS	I2C Channel 0 SDA Signal	
40	42	32	-	GND	P	GND	
41	43	33	26	VDD	P	VDD (3.0 ~ 5.5V)	
42	44	34	27	PD0*	IOUC	GPIO D bit 0 input/output	
				PWM0	OUC	PWM Channel 0 Output	
43	45	35	28	PD1*	IOUC	GPIO D bit 1 input/output	
				PWM1	OUC	PWM Channel 1 Output	
44	46	36	29	PD2*	IOUC	GPIO D bit 2 input/output	
				PWM2	OUC	PWM Channel 2 Output	
45	47	37	30	PD3*	IOUC	GPIO D bit 3 input/output	
				PWM3	OUC	PWM Channel 3 Output	
46	48	38	31	PD4*	IOUC	GPIO D bit 4 input/output	
				PWM4	OUC	PWM Channel 4 Output	
47	49	39	32	PD5*	IOUC	GPIO D bit 5 input/output	
				PWM5	OUC	PWM Channel 5 Output	
48	50	40	-	PD6*	IOUC	GPIO D bit 6 input/output	
				PWM6	OUC	PWM Channel 6 Output	
49	51	41	-	PD7*	IOUC	GPIO D bit 7 input/output	
				PWM7	OUC	PWM Channel 7 Output	
50	52	42	33	PD8*	IOUC	GPIO D bit 8 input/output	
				SS1	IOUC	SPI Channel 0 Select Signal	

						input/output	
51	53	43	34	PD9*	IOUC	GPIO D bit 9 input/output	
				SCK1	IOUC	SPIO Channel Clock Signal input/output	
52	54	44	35	PD10*	IOUC	GPIO D bit 10 input/output	
				MOSI1	IOUC	SPI Channel 1 Master Out/Slave In Signal	
53	55	45	36	PD11*	IOUC	GPIO D bit 11 input/output	
				MISO1	IOUC	SPI Channel 1 Master In/Slave Out Signal	
54	56	46	37	PD12*	IOUC	GPIO D bit 12 input/output	
				RXD1	IUC	UART Channel 1 Receive Data input	
55	57	47	38	PD13*	IOUC	GPIO D bit 13 input/output	
				39TXD1	OUC	UART Channel 1 Transmit Data Output	
56	58	48	39	PD14*	IOUC	GPIO D bit 14 input/output	
				SCL1	OUC	I2C Channel 1 SCL Signal	
57	59	49	40	PD15*	IOUC	GPIO D bit 15 input/output	
				SDA1	OUC	I2C Channel 1 SDA Signal	
58	60	-	-	PE0*	IOUS	GPIO E bit 0 input/output	
				PWMB0	OUS	PWM Channel 0 inversion Output	
59	61	50	-	PE1*	IOUS	GPIO E bit 1 input/output	
				PWMB1	OUS	PWM Channel 1 inversion Output	
60	62	51	-	PE2*	IOUS	GPIO E bit 2 input/output	
				PWMB2	OUS	PWM Channel 2 inversion Output	
61	63	52	-	PE3*	IOUS	GPIO E bit 3 input/output	
				PWMB3	OUS	PWM Channel 3 inversion Output	
62	64	53	-	PE4*	IOUS	GPIO E bit 4 input/output	
				PWMB4	OUS	PWM Channel 4 inversion Output	
63	65	54	-	PE5*	IOUS	GPIO E bit 5 input/output	
				PWMB5	OUS	PWM Channel 5 inversion Output	
64	66	55	41	PE6*	IOUS	GPIO E bit 6 input/output	
				PWMB6	OUS	PWM Channel 6 inversion Output	
				RXD3	IUS	UART Channel 3 Receive Data input	
65	67	56	42	PE7*	IOUS	GPIO E bit 7 input/output	
				PWMB7	OUS	PWM Channel 7 inversion Output	
				TXD3	OUS	UART Channel 3 Transmit Data Output	
66	68	57	43	PC10*	IOUS	GPIO C bit 10 input/output	
				RXD2	IUS	UART Channel 2 Receive Data input	
67	69	58	44	PC11*	IOUS	GPIO C bit 11 input/output	
				TXD2	OUS	UART Channel 2 Transmit Data Output	
68	70	-	-	VDD	P	VDD (3.0 ~ 5.5V)	
69	71	59	45	PC14*	IOUS	GPIO C bit 14 input/output	
				XTALO	IA	Main Crystal Oscillator Output (4/8/10MHz)	
70	72	60	46	PC15*	IOUS	GPIO C bit 15 input/output	
				XTALI	IA	Main Crystal Oscillator input (4/8/10MHz)	
71	73	61	47	GND	P	GND	
72	74	-	-	PF7	IOUS	GPIO F bit 7 input/output	
73	75	-	-	PF8	IOUS	GPIO F bit 8 input/output	
74	76	62	48	VDD	P	VDD (3.0 ~ 5.5V)	
75	77	-	-	PF9	IOUS	GPIO F bit 9 input/output	
76	78	-	-	PF10	IOUS	GPIO F bit 10 input/output	
77	79	-	-	PE11*	IOUS	GPIO E bit 11 input/output	
				TraceD3	IOUS	ETM Trace Data 3	
78	80	-	-	PE12*	IOUS	GPIO E bit 12 input/output	

				TraceD2	IOUS	ETM Trace Data 2	
79	81	-	-	PE13*	IOUS	GPIO E bit 13 input/output	
				TraceD1	IOUS	ETM Trace Data 1	
80	82	-	-	PE14*	IOUS	GPIO E bit 14 input/output	
				TraceD0	IOUS	ETM Trace Data 0	
81	83	-	-	PE15*	IOUS	GPIO E bit 15 input/output	
				TraceCLK	IOUS	ETM Trace Clock	
82	84	63	49	PC0	IOUS	GPIO C bit 0 input/output	
				nTRST*	IUS	JTAG nTRST Signal input	
83	85	64	50	PC1	IOUS	GPIO C bit 1 input/output	
				TDI*	IUS	JTAG TDI Signal input	
84	86	65	51	PC2	IOUS	GPIO C bit 2 input/output	
				TMS*	IUS	JTAG TMS Signal input	
				SWDIO	IOUS	SWD data input/output	
85	87	66	52	PC3	IOUS	GPIO C bit 3 input/output	
				TCK*	IUS	JTAG TCK Signal input	
				SWCLK	IUS	SWD Clock signal	
86	88	67	53	PE8*	IOUS	GPIO E bit 8 input/output	
				SXIN	IA	Sub Crystal Oscillator Signal input (32.768kHz)	
87	89	68	54	PE9*	IOUS	GPIO E bit 9 input/output	
				SXOUT	IA	Sub Crystal Oscillator Signal Output (32.768kHz)	
88	90	69	55	PC13*	IOUS	GPIO C bit 13 input/output	
				CLKO	OUS	External Clock Output	
89	91	70	56	PC12*	IOUS	GPIO C bit 12 input/output	
				STBYO	OUS	Stand-by(Power-down) Indication Output Signal	
90	92	-	-	PF11	IOUS	GPIO F bit 11 input/output	
91	93	71	57	PC4	IOUS	GPIO C bit 4 input/output	
				TDO*	OUS	JTAG TDO Signal Output	
				SWO	OUS	SWD Output	
92	94	72	-	PC5	IOUS	GPIO C bit 5 input/output	
93	95	73	58	PC6	IOUS	GPIO C bit 6 input/output	
				nRESET*	IUS	Reset input	
94	96	74	59	PC7	IOUS	GPIO C bit 7 input/output	
				BOOT*	IUS	Boot Signal input (input mode when reset)	
95	97	75	60	PC8	IOUS	GPIO C bit 8 input/output	
				RXD0*	IUS	UART Channel 0 Receive Data input (UART Boot Channel)	
96	98	76	61	PC9	IOUS	GPIO C bit 9 input/output	
				TXD0*	OUS	UART Channel 0 Transmit Data Output (UART Boot Channel)	
97	99	77	-	AGND	P	ADC/Analog GND	
98	100	78	62	AVDD	P	ADC/Analog VDD	

*Legend: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type
A=Analog, P=Power

(*) Initial setting in reset state In reset state, all pins except for certain pin will be Hi-Z state.

1.7 A33G52x Memory Map

1.7.1 Overall Memory Map

The memory configuration of A33G52x MCUs are as follows. The code flash area is assigned differently depending on the device name.

- A33G527 (384KB)
- A33G526 (256KB)
- A33G524 (128KB)

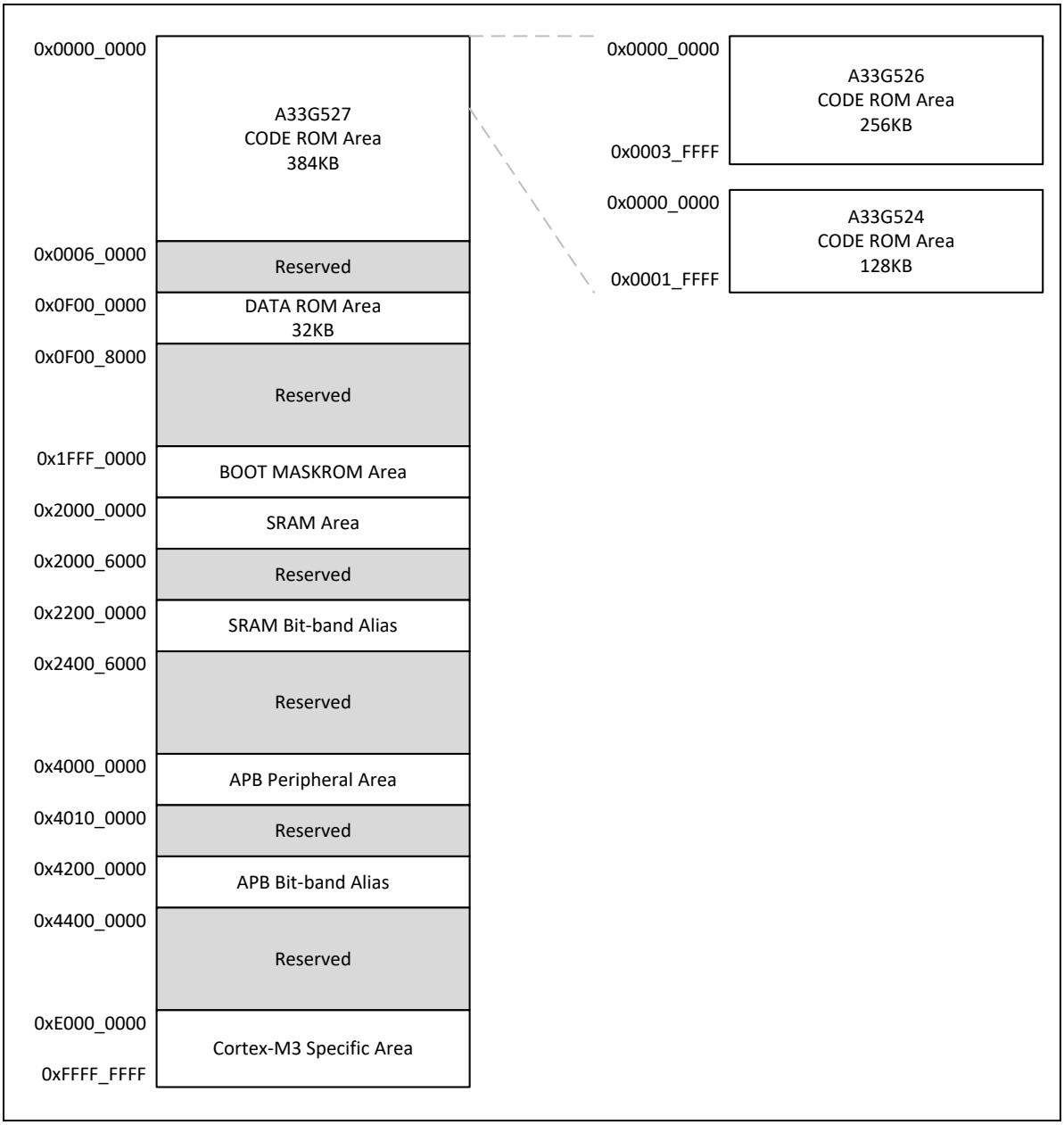


Figure 1.9. Overall Memory Map

1.7.2 Memory Map of Cortex-M3

The A33G52x has a fixed memory area for Cortex-M3 from 0xE000_0000 to 0xFFFF_FFFF, and the sections are divided according to the interfaces to the internal and private peripheral buses (PPB) supported by this CPU.

- Interfaces accessible to internal-only peripheral buses
  - Instrumentation Trace Macrocell (ITM)
  - Data Watchpoint and Trace (DWT)
  - Flashpatch and Breakpoint (FPB)
  - System Control Space (SCS) : Memory Protection Unit (MPU) + Nested Vectored Interrupt Controller (NVIC).
- Interfaces accessible to external dedicated peripheral buses
  - Trace Point Interface Unit (TPIU)
  - Embedded Trace Macrocell (ETM)
  - ROM table.
  - Implementation-specific areas of the PPB memory map.

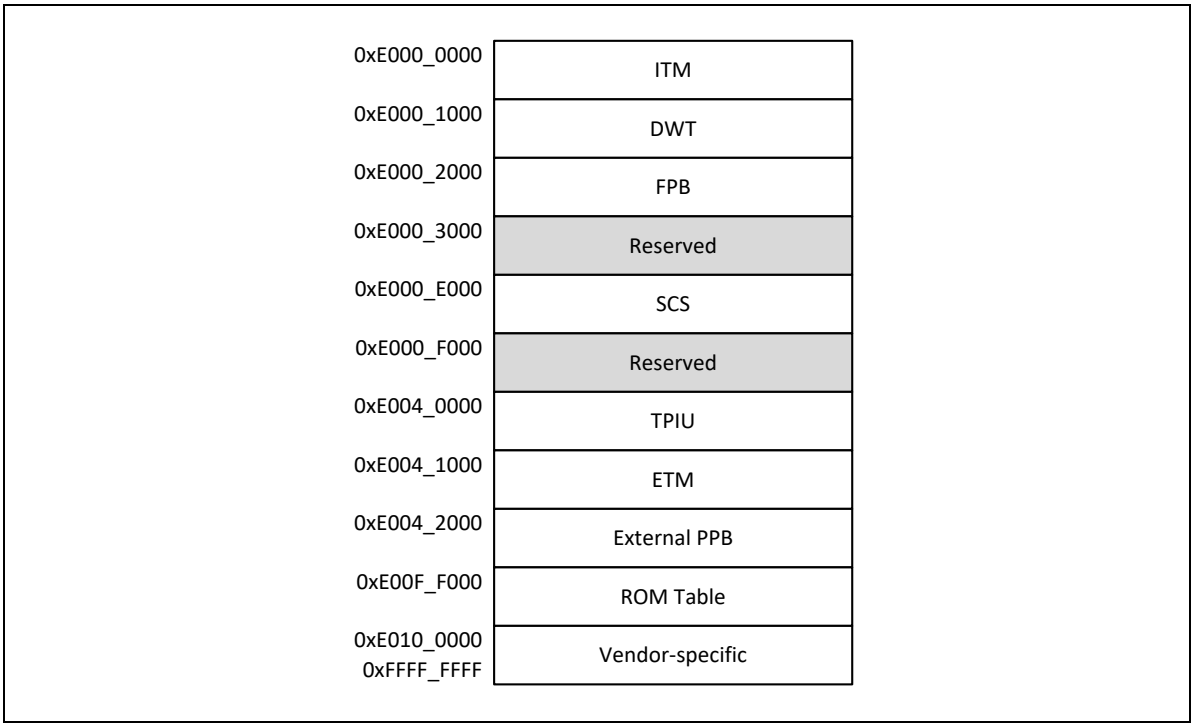


Figure 1.10. Cortex-M3 dedicated Memory Map

1.7.3 Memory map of internal peripehrals

The APB Peripheral Area, which is the total memory map of the A33G52x, is assigned to each peripheral area of the MCU. In this area, special function registers (SFRs) are provided for controlling peripheral devices. For information on the SFR for each peripheral device, refer to the register map in the A33G52x user's manual.

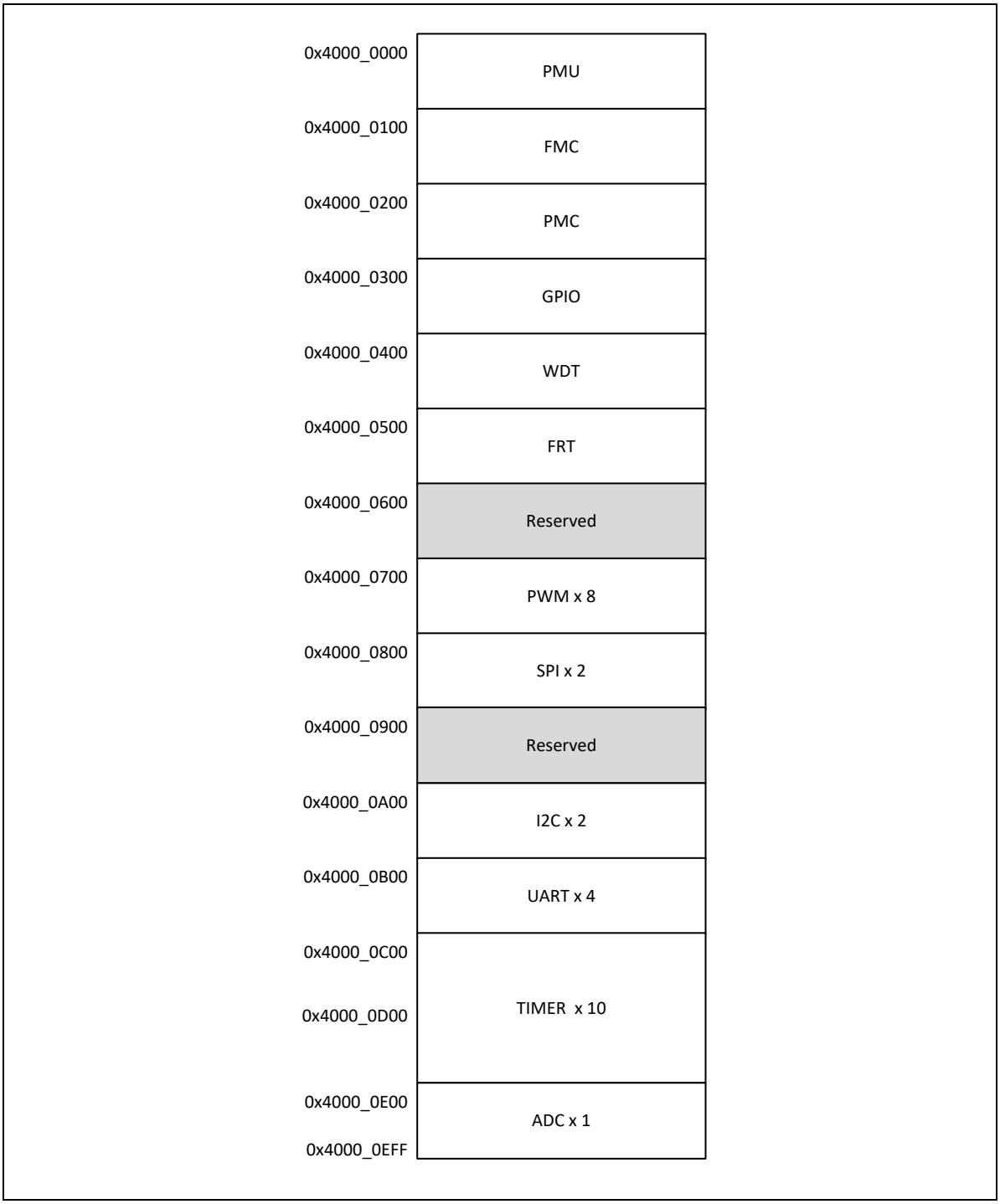


Figure 1.11. Memory Map of Internal Peripherals

CHAPTER 2. CORE

2.1 Cortex-M3

The A33G52x series is based on the Cortex-M3 CPU core, ARM's high-performance 32-bit MCU core. The Cortex-M3 is a processor designed for the harvard architecture and supporting the Thumb-2 instruction set.
For more information, please refer to the ARM document number “DDI337”

2.2 Interrupt Controller

A33G52x has the Cortex-M3's NVIC (Nested-Vectored Interrupt Controller). NVIC is designed to handle interrupts simultaneously in the CPU more effectively. The NVIC built into the Cortex-M3 makes interrupt processing faster and more efficient.

IRQ interrupts are disabled when the A33G52x system is initialized. To use the various interrupts supported by the A33G52x, you must enable the IRQ interrupt. Even if the peripheral's interrupt function is enabled, peripheral interrupts will NOT occur if the IRQ interrupt is NOT enabled.

The interrupt vector map of A33G52x is defined as follows:

Table 2.1. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MPU Fault Handler
-11	0x0000_0014	BUS Fault Handler
-10	0x0000_0018	Usage Fault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVDFAIL
1	0x0000_0044	MXOSCFAIL
2	0x0000_0048	Reserved
3	0x0000_004C	WDT
4	0x0000_0050	FRT
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	TIMER4
10	0x0000_0068	TIMER5
11	0x0000_006C	TIMER6
12	0x0000_0070	TIMER7
13	0x0000_0074	TIMER8
14	0x0000_0078	TIMER9
15	0x0000_007C	MCKFAIL
16	0x0000_0080	GPIOA
17	0x0000_0084	GPIOB
18	0x0000_0088	GPIOC
19	0x0000_008C	GPIOD
20	0x0000_0090	GPIOE
21	0x0000_0094	GPIOF
22	0x0000_0098	Reserved
23	0x0000_009C	
24	0x0000_00A0	PWM0
25	0x0000_00A4	PWM1
26	0x0000_00A8	PWM2
27	0x0000_00AC	PWM3
28	0x0000_00B0	PWM4
29	0x0000_00B4	PWM5

30	0x0000_00B8	PWM6
31	0x0000_00BC	PWM7
32	0x0000_00C0	SPI0
33	0x0000_00C4	SPI1
34	0x0000_00C8	Reserved
35	0x0000_00CC	
36	0x0000_00D0	I2C0
37	0x0000_00D4	I2C1
38	0x0000_00D8	UART0
39	0x0000_00DC	UART1
40	0x0000_00E0	UART2
41	0x0000_00E4	UART3
42	0x0000_00E8	Reserved
43	0x0000_00EC	ADC
44	0x0000_00F0	Reserved
45	0x0000_00F4	
46	0x0000_00F8	
47	0x0000_00FC	
48	0x0000_0100	
49	0x0000_0104	
50	0x0000_0108	
51	0x0000_010C	
52	0x0000_0110	
53	0x0000_0114	
54	0x0000_0118	
55	0x0000_011C	
56	0x0000_0120	
57	0x0000_0124	
58	0x0000_0128	
59	0x0000_012C	
60	0x0000_0130	
61	0x0000_0134	
62	0x0000_0138	
63	0x0000_013C	

CHAPTER 3. PMU (Power Management Unit)

Table 3.1. Operation Summary

Item	Pin Name	Remark
Clock usage	Main XTAL, Sub XTAL RingOSC, IOSC16 HCLK, PCLK	Clock settings
Reset Source	External Reset Soft-Reset LVD (Low Voltage Detector) Clock Fail	 PMU_CFGR LVD_CON PMU_CMR
Reset Generation	External Reset Soft-Reset LVD Clock Fail	 PMU_CFGR LVD_CON PMU_CMR
Interrupt Generation	LVD(0) MXOSCFAIL(1)	LVD_CON PMU_CMR
Interrupt Clear Method	Writing '1' to the interrupt bit	PMU_CMR, LVD_CON

3.1 Overview

PMU (Power Managament Unit), the power management module of A33G52x MCU, can control and monitor the source clock of the chip, and set system operation speed. In addition, the power consumption of the application can be controlled by controlling the operation mode of the MCU. There is also a function to prevent malfunction of user application by setting reset.
It also provides the function to enable the peripherals' clocks and devices in the Power Managament Unit (PMU) block to enable control of each peripheral device in the MCU.

Features of PMU (Power Managament Unit)

- MCU operating mode for low power consumption
  - Run mode (Run)
  - Sleep mode (Idle)
  - Deep-sleep mode (Power Down)
- Input clock sources for MCU operation
  - 1MHz internal ring oscillator (RINGOSC)
  - 16MHz internal oscillator (IOSC16)
  - 4/8/10MHz external main oscillator (MXOSC)
  - 32.768kHz external auxiliary oscillator (SXOSC)
- PLL frequency output
  - High-speed clock driving up to 75MHz frequency output
  - Fine adjustment in 1MHz unit
- Clock monitoring and non-oscillation error check
  - Main clock and external main oscillator clock monitoring
  - No-oscillation error handling function
- Reset source and wake-up event
- Others
  - LDO (Low Drop Out)
  - POR (Power On Reset)
  - LVD (Low Level Detector)

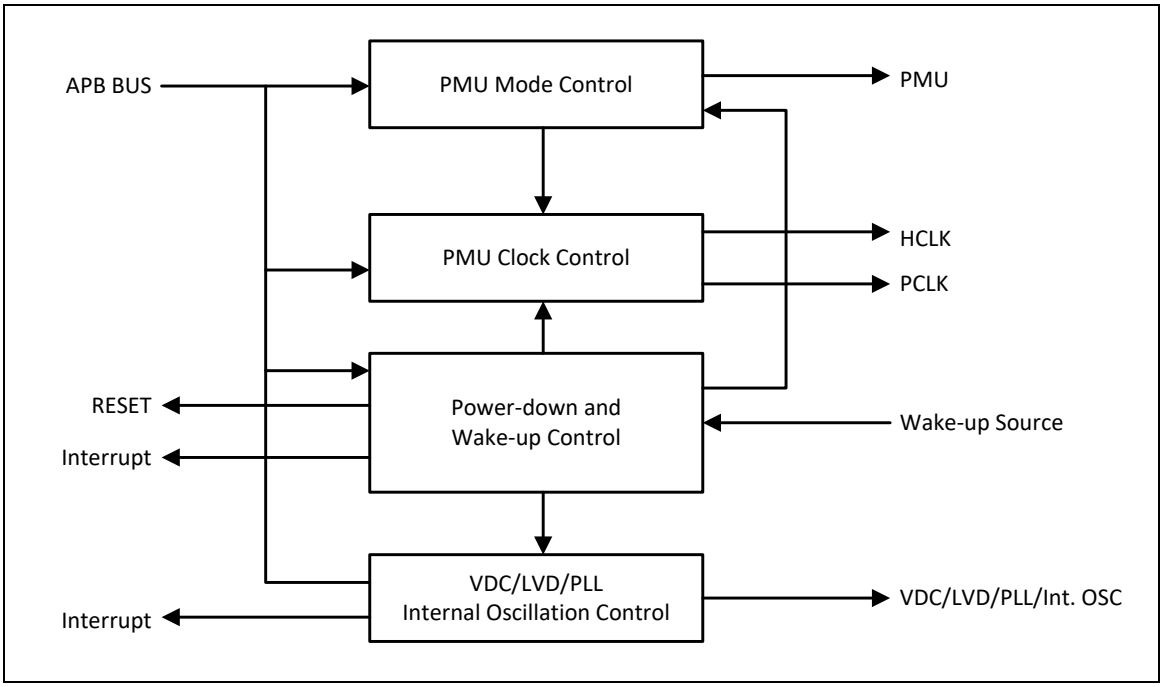


Figure 3.1. Block diagram of PMU

3.2 Pin configuration and clock sources

3.2.1 Pin Configurations

The Power Management Unit (PMU) of the A33G52x has input / output pins that can be set.
The input signals that can be set in the PMU include reset input (nRESET), main oscillator input (XTALI / XTALO), and auxiliary oscillator input (SXIN / SXOUT).
The output signals that can be set by the PMU include the STBYO pin indicating the power down state and the CLKO pin for dividing the internal PLL or main clock.

Table 3.2. Power Management Unit (PMU) and PLL related pins.

Pin	I/O	Description
nRESET	I	Initialize entire chip by the external reset input pin. This pin is Schmitt-Trigger type input.
XTALI/XTALO	OSC	Main crystal oscillator pin
SXIN/SXOUT	OSC	32kHz crystal sub-oscillatorp pin
STBYO	O	A indicator pin of Stand-by mode
CLKO	O	Clock output pin of internal PLL

3.2.2 Clock Sources

A ring oscillator (RINGOSC) of about 1MHz and a 16MHz RC oscillator (IOSC16) are built in the A33G52x MCUs. The external main crystal (MXOSC) oscillation can be used as a clock input, and the clock can be used to 75MHz using the internal PLL. In addition, the external clock 32768kHz crystal (SXOSC) oscillation as an auxiliary clock, more time-critical periodic time calculation is possible.
The A33G52x supports clock sources as shown below.

Table 3.3. The Clock Sources

Clock Source	Frequency	Description
RINGOSC	1MHz (±50%)	Clock monitoring for internal system Used for WDT, Clock monitoring (Large variations in temperature and voltage)
IOSC16	16MHz (±3%)	Intenal main clock (This clock can be used instead of XTAL)
MXOSC (MainOSC)	X-TAL(4MHz~10MHz)	External Main clock
SXOSC (SubOSC)	SX-TAL(32.768kHz)	External auxiliary clock (for real time clock)
PLL	8MHz ~ 75MHz	multiplier and divider of PLL clock High frequency output XTAL or IOSC16 input as clock source

3.3 Block Diagram

3.3.1 PMU Clock

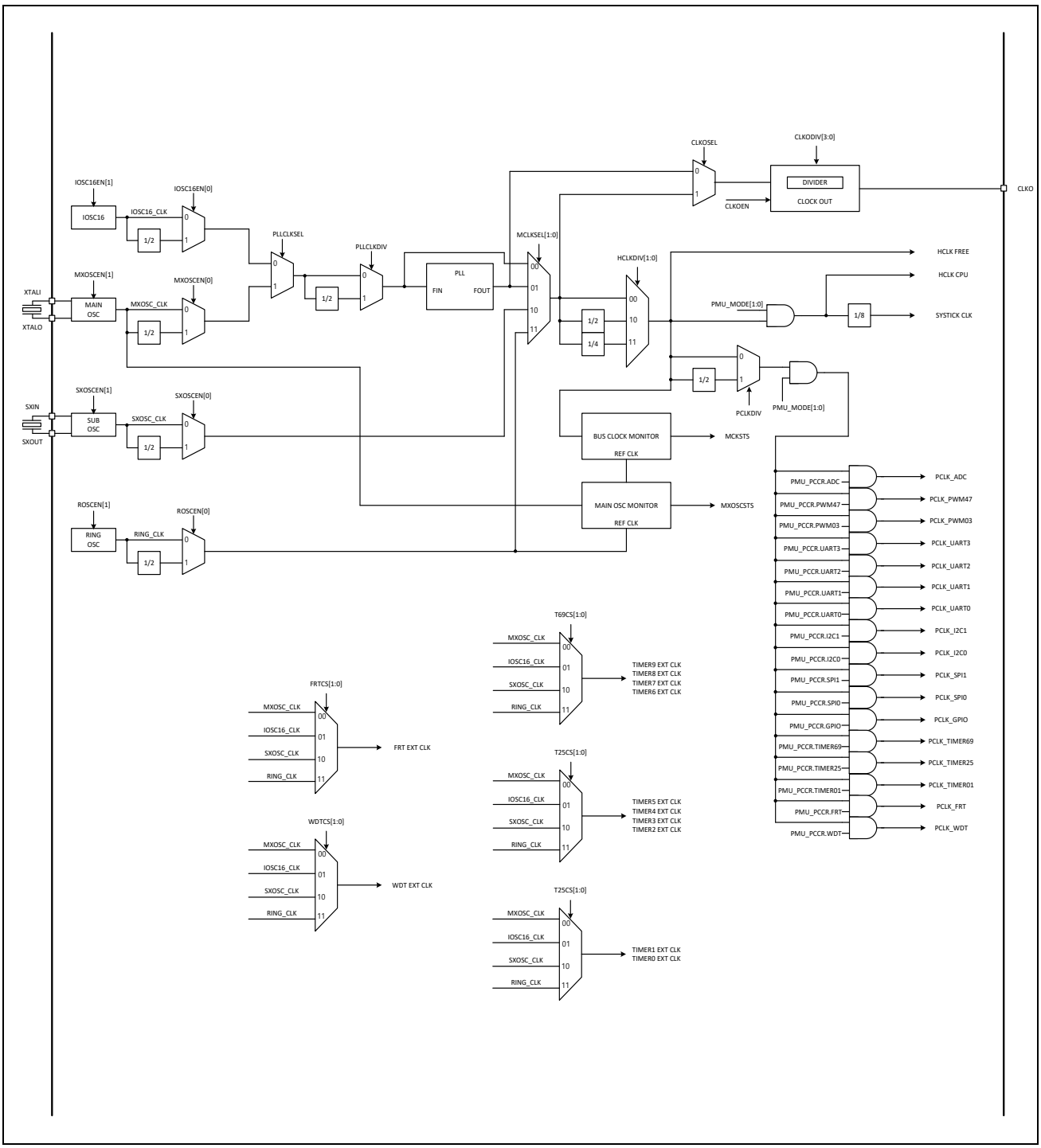


Figure 3.2. Block diagram of A33G52x PMU Clock

3.3.2 PMU Reset

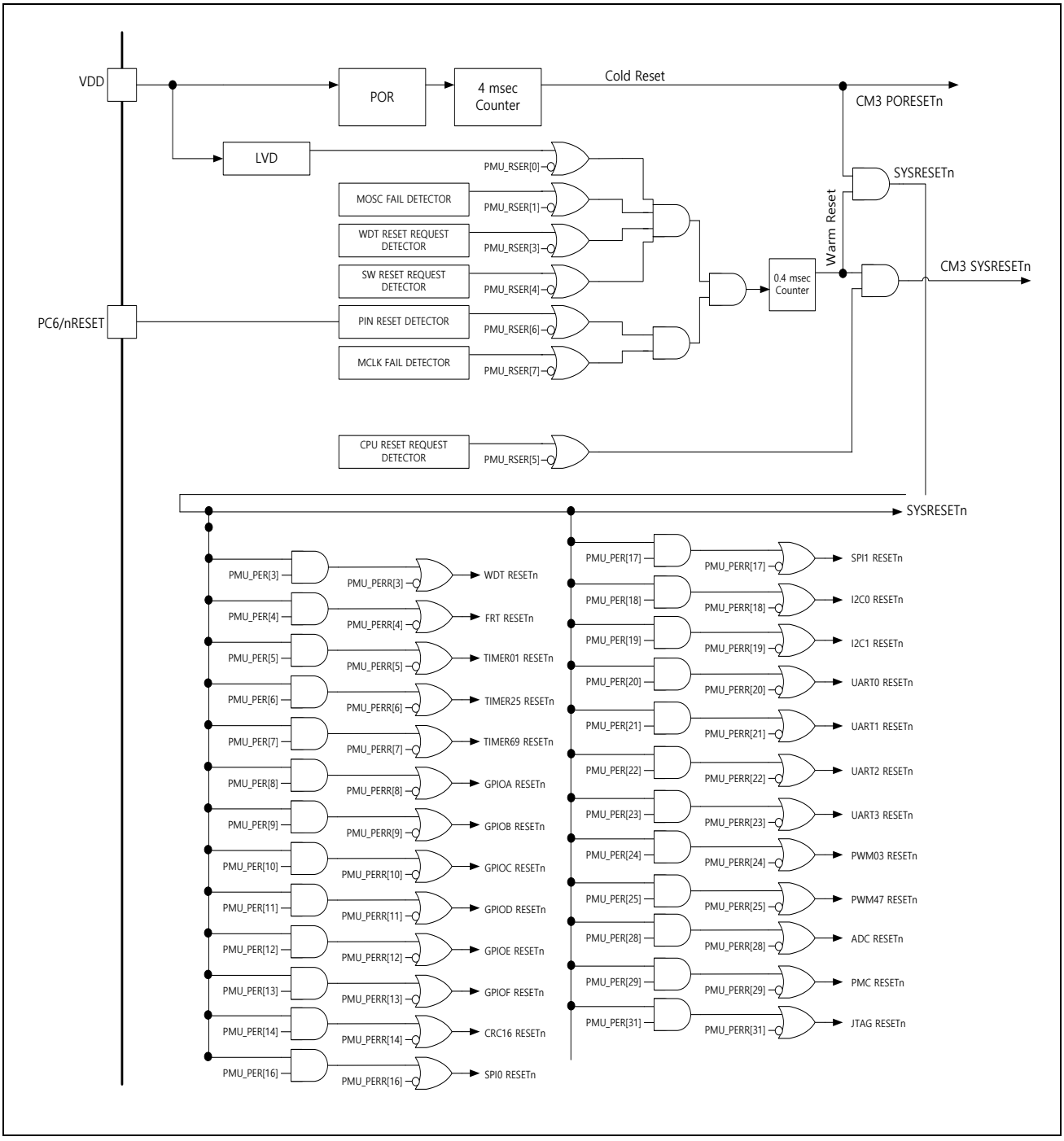


Figure 3.3. Block diagram of A33G52x PMU Reset

3.4 Functional Description

3.4.1 Operating Modes for Low-Power Consumption

The A33G52x series has various power-saving options and operating modes that help its applications to reduce power consumption. When designing an embedded system with an A33G52x microcontroller unit (MCU), it is important to fully understand the device details of the intended system to optimize the use of the MCU's peripherals and operating modes for minimal power consumption.

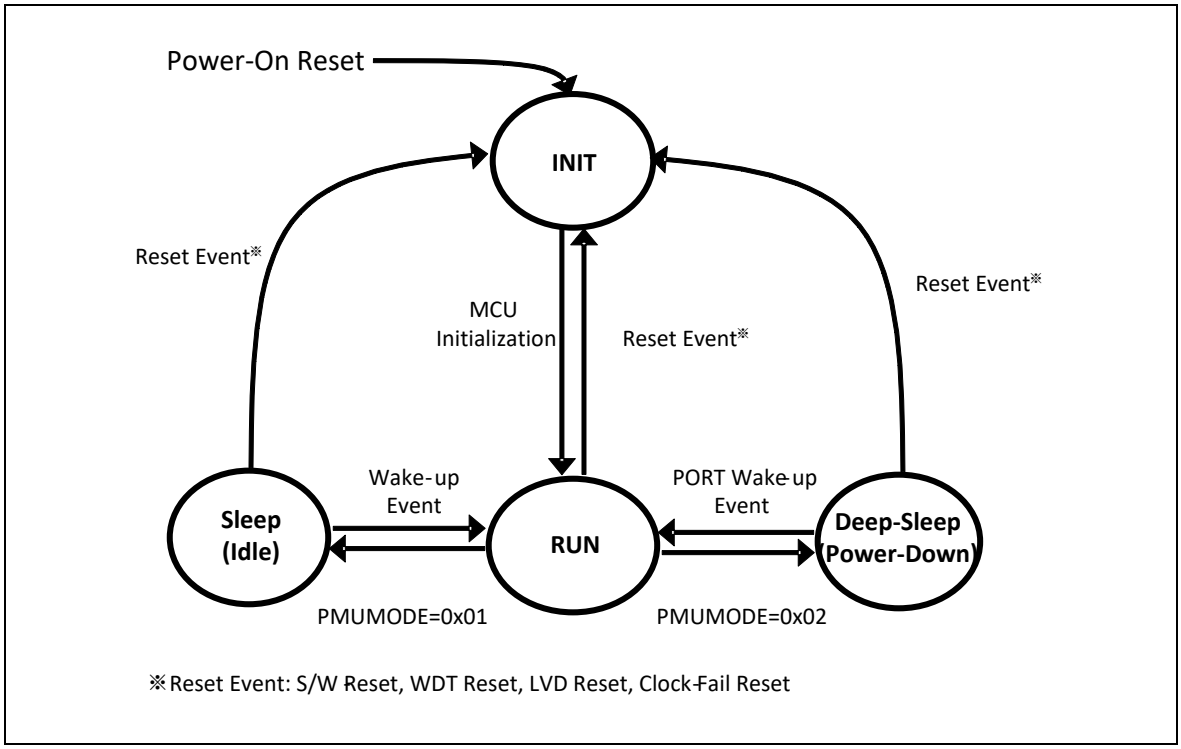


Figure 3.4. Operating modes of A33G52x

Run Mode

This mode is the normal operating mode of A33G52x MCUs. Once activated by an external power supply, the power-on reset (POR) holds the MCU chip in a reset state until it stabilizes. Upon its stabilization, the MCU initializes all clock sources and registers in initialization mode and then enters run mode. In run mode, all clock sources, buses, and peripherals can be enabled, and the current consumption will vary with their operating frequencies.

Sleep (Idle) Mode

When in run mode, writing 0x01 to the PMUMODE of the PMU_MR register triggers the MCU to enter sleep mode, in which the clock input to the CPU becomes disabled.

By using the wake-up source enable register (PMU_WSER), designers can set the wake-up sources of various peripherals, including GPIOA through GPIOF (5–10), FRT (4), WDT (3), main oscillator error (2), and LVD (0). When a wake-up event occurs based on the settings, the MCU will return to run mode.

In addition, the clock for each peripheral device can be individually enabled or disabled to supply power to only the minimum number of peripherals, thereby reducing power consumption.

Deep-Sleep (Power-Down) Mode

An A33G52x MCU operating in run mode can be switched to deep-sleep (power-down) mode by writing 0x00 to the main clock select (MCLKSEL) of the power management unit's (PMU's) bus clock control register (PMU_BCCR), which will set the ring oscillator as the main clock source, and then writing 0x02 to the PMUMODE of the PMU mode register (PMU_MR). In deep-sleep mode, the PLL and its clock source, the internal oscillator, are disabled, along with the system clock (HCLK) and peripheral clock (PCLK). This system stop allows for operation with minimal power consumption.

From among the various wake-up sources for peripherals provided by the wake-up source enable register (PMU_WSER), only those for the external GPIOA through GPIOF (5–10) can render wake-up events (levels) in deep-sleep mode.

By default, this mode automatically powers off the main oscillator (MXOSC) and sub-oscillator (SXOSC). As such, the peripherals fed with a clock signal from the main or sub-oscillator will stop operating in deep-sleep mode. To keep those peripherals running in this mode, the MCU can be configured in either of the following ways:
1) Set the ring oscillator as the clock source to feed the peripherals that need to continue running in deep-sleep mode.
2) To continue using the main or sub-oscillator in deep-sleep mode, set the ECLKMD bit of the PMU mode register (PMU_MR) to "1." This will prevent the main and sub-oscillators from automatically being powered off. Next, configure the PMU clock control register (PMU_CCR) manually to disable the clock sources that are NOT in use in deep-sleep mode. However, this method requires special care to ensure effective power saving in deep-sleep mode.

Table 3.4. Operability of the clock sources, buses, and modules in each operating mode

Functions \ MCU modes		Run mode	Sleep mode	Deep sleep mode
Clock sources	IOSC16	O	O	X
	RING	O	O	X
	MXOSC	O	O	△
	SXOSC	O	O	△
	PLL	O	O	X
Buses	AHB	O	O	X
	APB	O	O	X
Modules	CORE	O	X	X
	PMU	O	O	X
	FLASH	O	O	X
	WDT	O	O	X
	FRT	O	O	X
	TIMER	O	O	X
	PWM	O	O	X
	GPIO (PCU)	O	O	X*
	ADC	O	O	X
	UART	O	O	X
	I2C	O	O	X
	SPI	O	O	X

O: Operable
X: Not operable
△: Operability depends on the settings of PMU_MR<ECLKMD>.
*: If the GPIO's wake-up source is set in the PMU_WSER resister, its level event is available.

3.4.2 PLL Output Frequency Setting

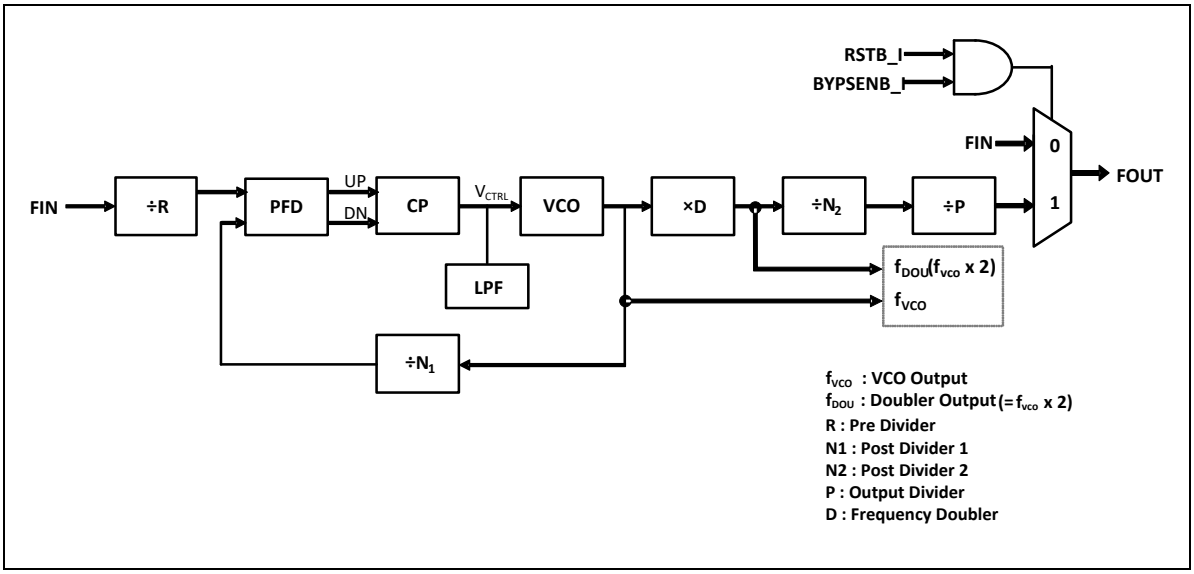


Figure 3.5. Block diagram of A33G52x PLL

[Calculating the PLL output frequency value]

The PLL of the A33G52x can accurately set the output frequency, F_{OUT}, in 1MHz increments. To control the PLL, first write 0x80750000 in the PMU_PLLCON register and calculate the parameter value for the PLL output frequency according to the following formula and write to each corresponding bit. The formula for the F_{IN} input to the F_{VCO} input of the PLL is as follows, and the input range of the F_{IN} frequency is between 1MHz and 3MHz. However, it is recommended to set the input frequency (FIN) to 2MHz as much as possible.

$$\mathrm{FIN} = \frac{\mathrm{PLLINCLK}}{(\mathrm{R}+1)}, \qquad 1\mathrm{MHz} \le \mathrm{FIN} \le 3\mathrm{MHz}\ (\mathrm{Recommanded\ FIN} = 2\mathrm{MHz})$$

At this time, the range of F_{VCO} output frequency should be set to 200MHz or less, and the calculation formula is as follows.

$$\mathrm{VCO} = \mathrm{FIN} \times (\mathrm{N}_1 + 1), \quad 50\mathrm{MHz} \le \mathrm{VCO} \le 200\mathrm{MHz}\ if\ \mathrm{D} = 0$$

PMU_PLLCON also supports a doubler function that can double the VCO output through the bit setting of VCOMODE. When using this doubler, the output of the VCOx2 must be set between minimum 100 MHz and maximum 250 MHz.

$$\mathrm{VCOx2} = \mathrm{VCO} \times (\mathrm{D}+1), \qquad 100\mathrm{MHz} \le \mathrm{VCOx2} \le 250\mathrm{MHz}\ if\ \mathrm{D} = 1$$

As a result, the final frequency of PLL, FOUT, can be obtained from the formula below using the formula above.

$$\mathrm{FOUT} = \frac{\mathrm{PLLINCLK} \times (\mathrm{N}_1+1)}{(\mathrm{R}+1) \times (\mathrm{N}_2+1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1) = \frac{\mathrm{FIN} \times (\mathrm{N}_1+1)}{(\mathrm{N}_2+1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1)$$

3.4.3 Cold-Reset and Wram-Reset

The A33G52x offers a variety of reset functions to protect the entire system from malfunctions in a service routine or core and to ensure the operation of the MCUs that the user can trust. Since the reset timing of the A33G52x is based on the ring oscillator (RINGOSC), it is necessary to consider the error (± 50%) of RINGOSC when applying the reset function to the user application.
The A33G52x supports two types of reset: Cold-Reset, which causes the system to be powered off and then on to initialize the system, and Warm-Reset, which initializes the system without any system power fluctuations. After the reset occurs, the user code is executed when the system boots normally.

In the case of the former, when the system power is on, a power on reset (POR) reset occurs when the power reaches 1.2V, and a LVD reset occurs when the voltage value set by LVD reset is detected. After performing a cold-reset, a warm-reset occurs and the system is initialized and the boot ROM and main code are executed.
The figure below shows the A33G52x cold reset timing diagram.

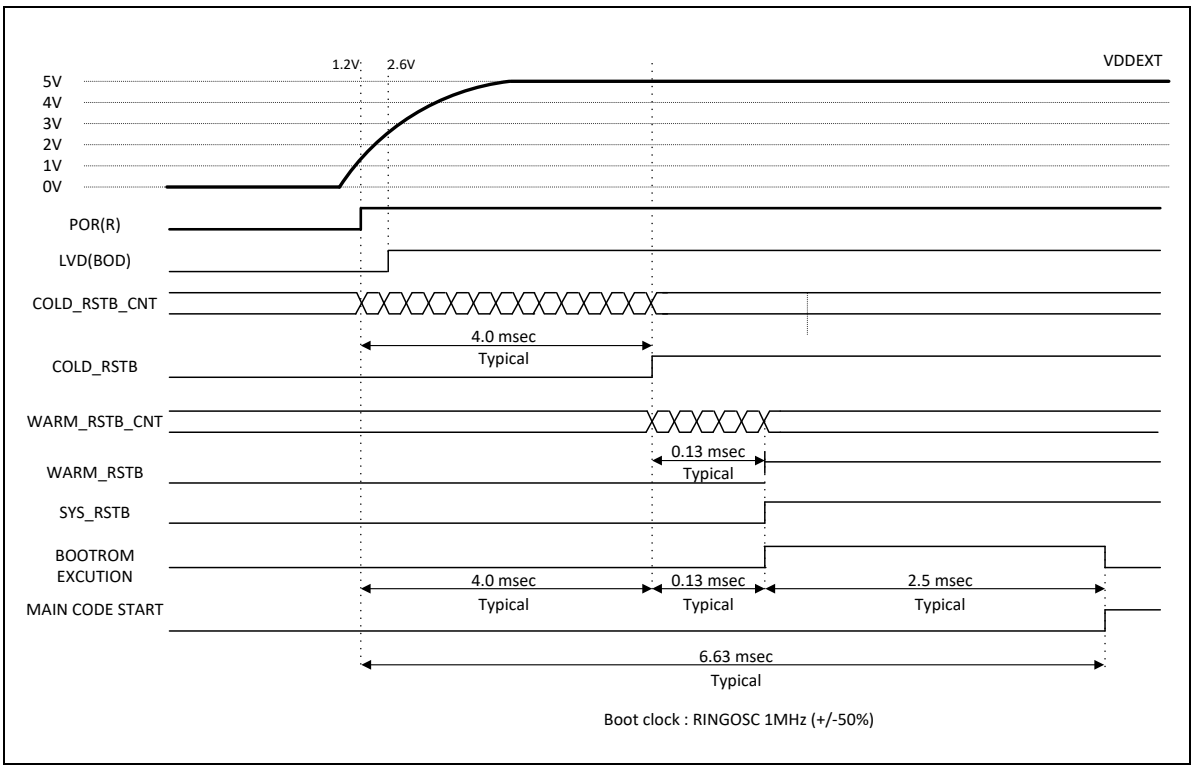


Figure 3.6. Cold Reset timing of A33G52x

In the latter case, it is also called a soft reset. While the system is operating at VVDD voltage, the mcu can occur reset itself by running a specific routine or by configuring a reset source. When this warm reset is happend, the system executes the boot ROM and main code.
A reset event can be performed for each module by setting the reset source provided by PMU_RSER (PMU reset source enable register) of A33G52x. The figure below shows the timing of the warm-reset.

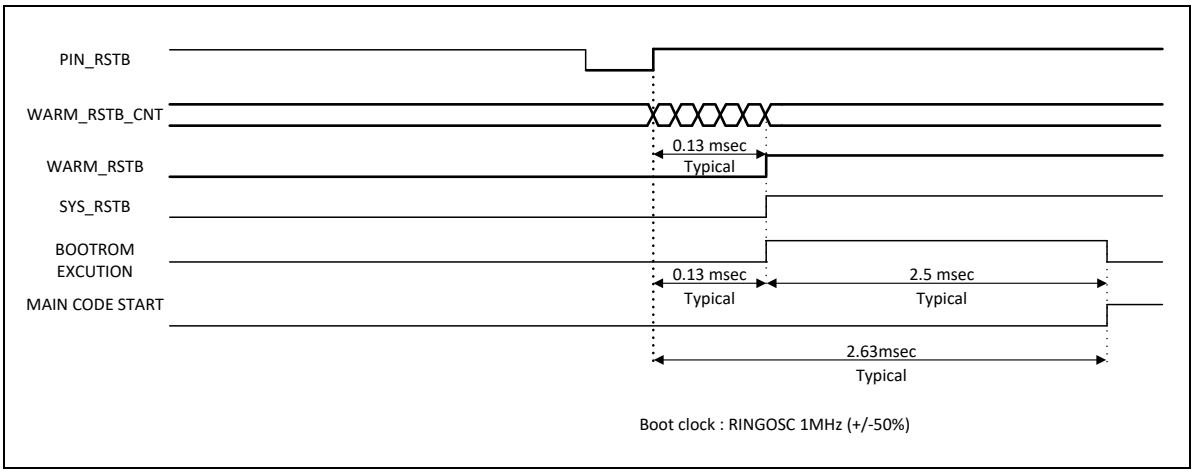


Figure 3.7. Warm Reset timing of A33G52x

3.4.4 Clock Monitoring

Using the clock monitoring function of A33G52x causes a reset or an interrupt when the oscillator stops oscillation or occurs erroneously oscillation due to external noise or the like.
However, when this interrupt occurs, the core clock must NOT be the main oscillator. This function uses the internal ring oscillator for monitoring and clock switching. To enable this function, it is necessary to set the internal ring oscillator to always operate.
Procedures for main oscillator oscillation and monitoring function are shown below.

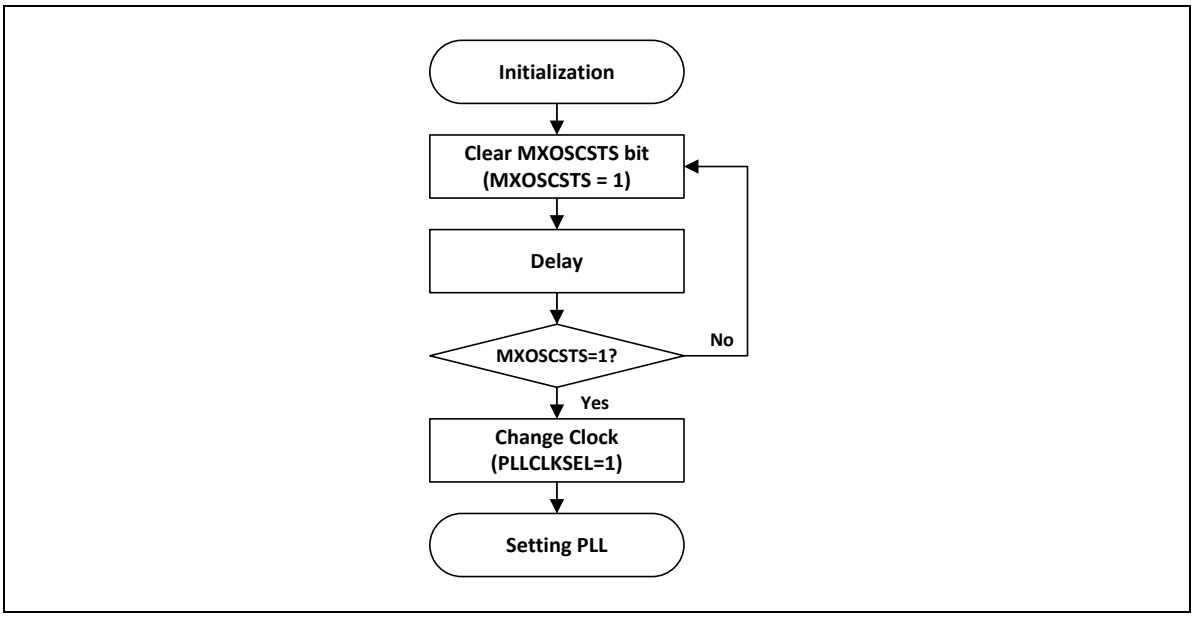


Figure 3.8. The main oscillator operating procedures

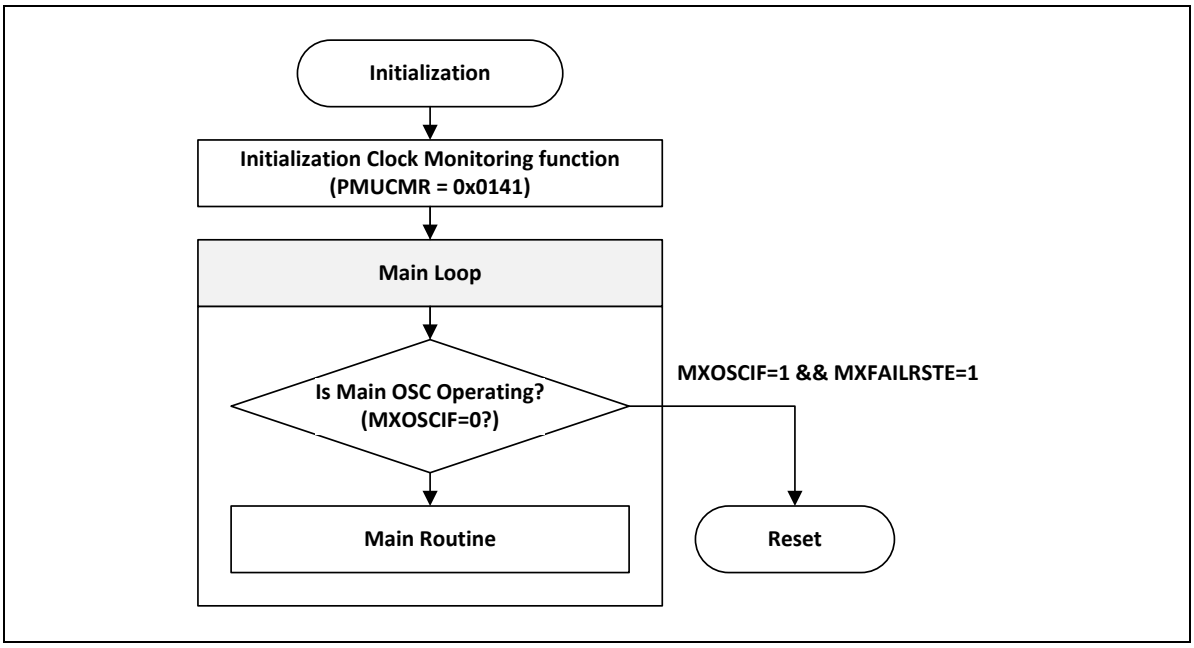


Figure 3.9. Functional flow chart of clock monitoring

CHAPTER 4. PMC (Port Map Controller)

Table 4.1. Operation Summary

Item	Pin Name	Remark
Clock usage	PCLK	Debounce settings
Reset Source	PMU_PER settings	
Reset Generation	None	
Interrupt Generation	Depend on the conditions of port interrupts (GPIOA(16)~GPIOF(21))	Pn_ICR
Interrupt Clear Method	Writing '1' to the interrupt bit	Pn_ISR

4.1 Overview

The PMC (Port Map Controller) controls the pins of the A33G52x MCU. By setting the PMC block register according to the purpose of the user application, you can set functions such as pin function setting, use I / O function, pull-up / pull-down, and debounce.

Features of PMC (Port Map Controller)

- MUX registers for setting the purpose of each pin.
- Direction(Input/Output) setting of each pin
  - Push-pull output
  - Open-drain output
  - Logic input
  - Analog input
- Pull-up/Pull-down resistor setting of each pin
- Interrupt settings for each input pin
  - Level interrupt
  - Rising-edge interrupt
  - Falling-edge interrupt
  - Supports up to 6 GPIO interrupts : GPIOA(16)~GPIOF(21)
- Debounce setting of each pin

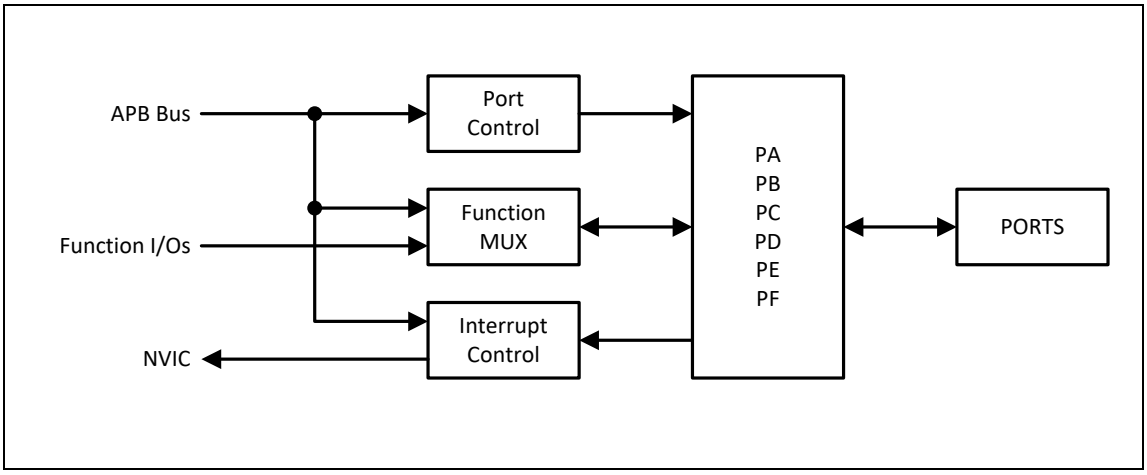


Figure 4.1. Block Diatram of PMC (Port Map Controller)

4.2 Block Diagram

4.2.1 PA Port

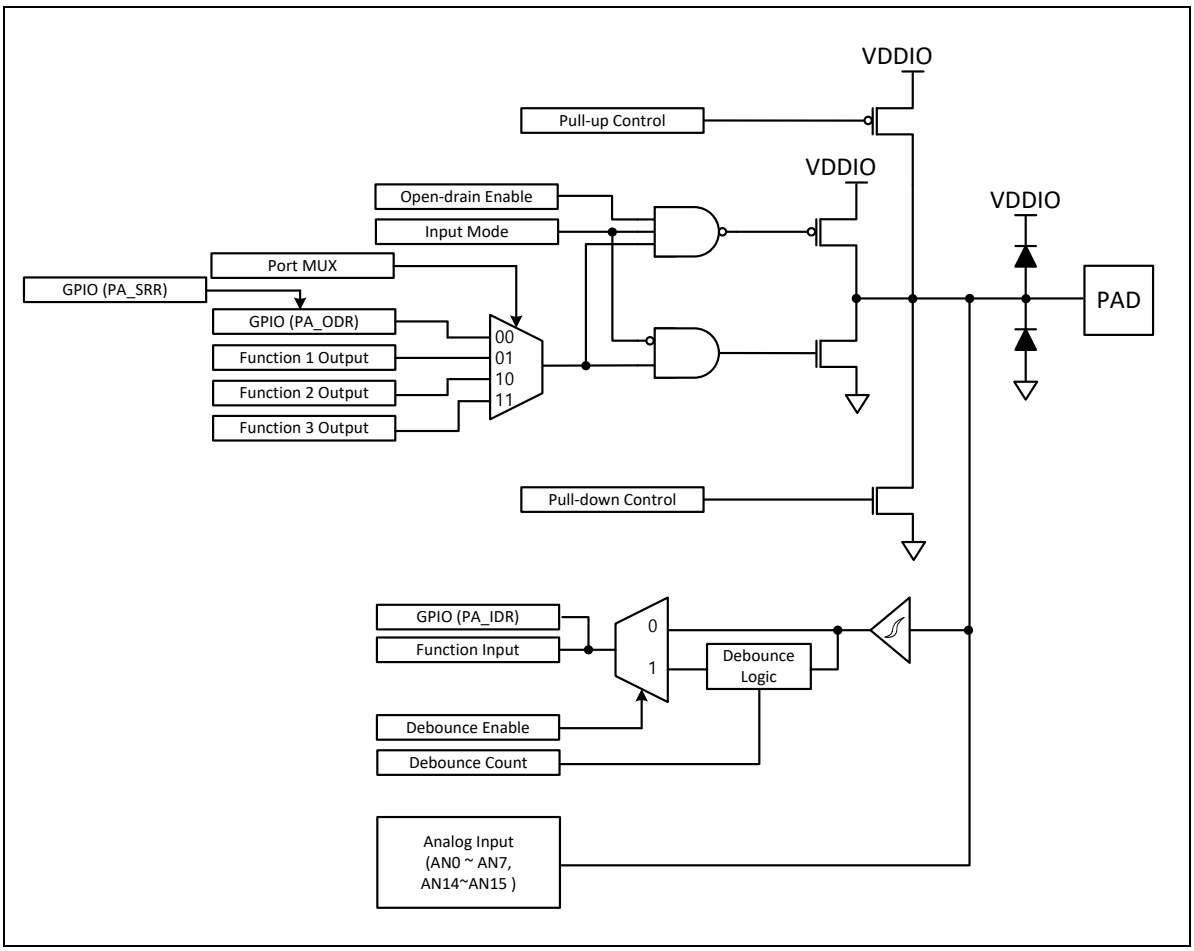


Figure 4.2. Block diagram of PA port

4.2.2 PB Port

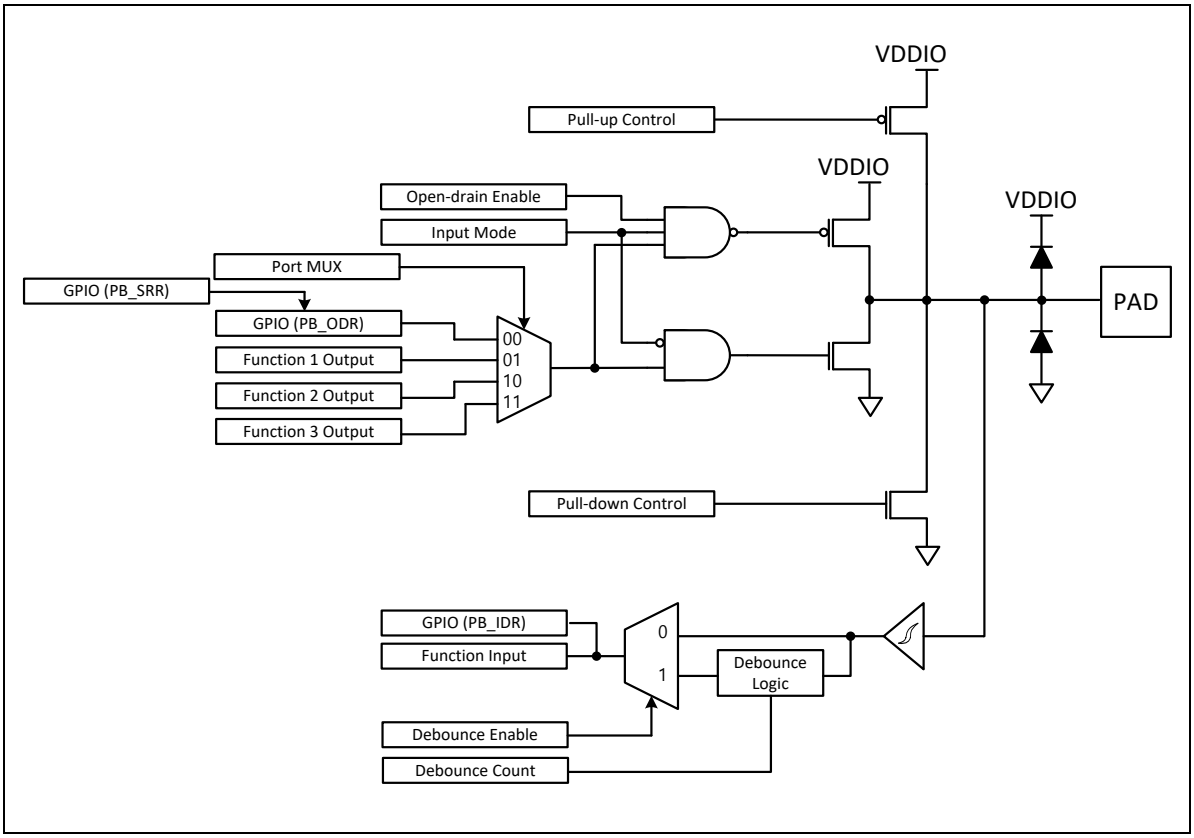


Figure 4.3. Block diagram of PB port

4.2.3 PC Port

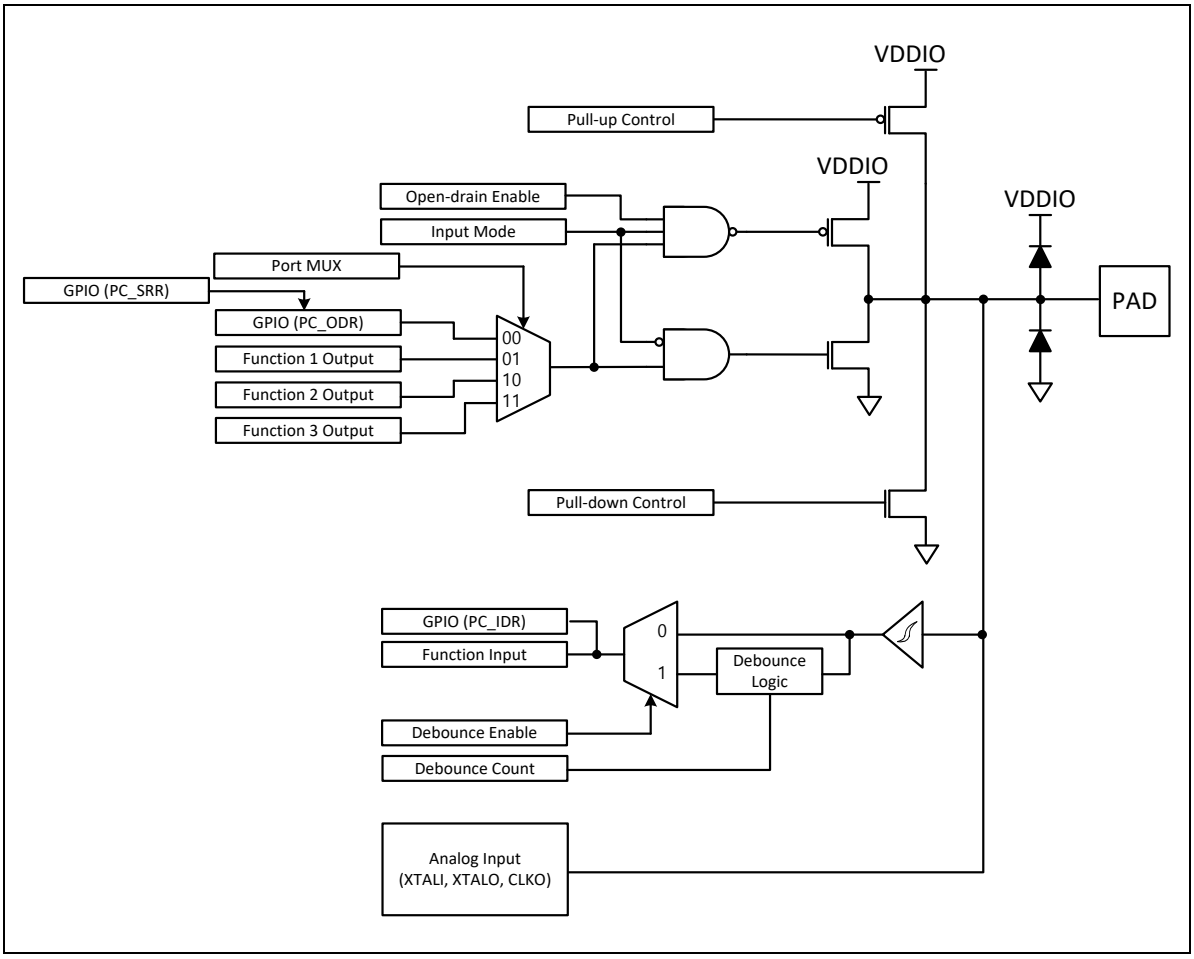


Figure 4.4. Block diagram of PC port

4.2.4 PD Port

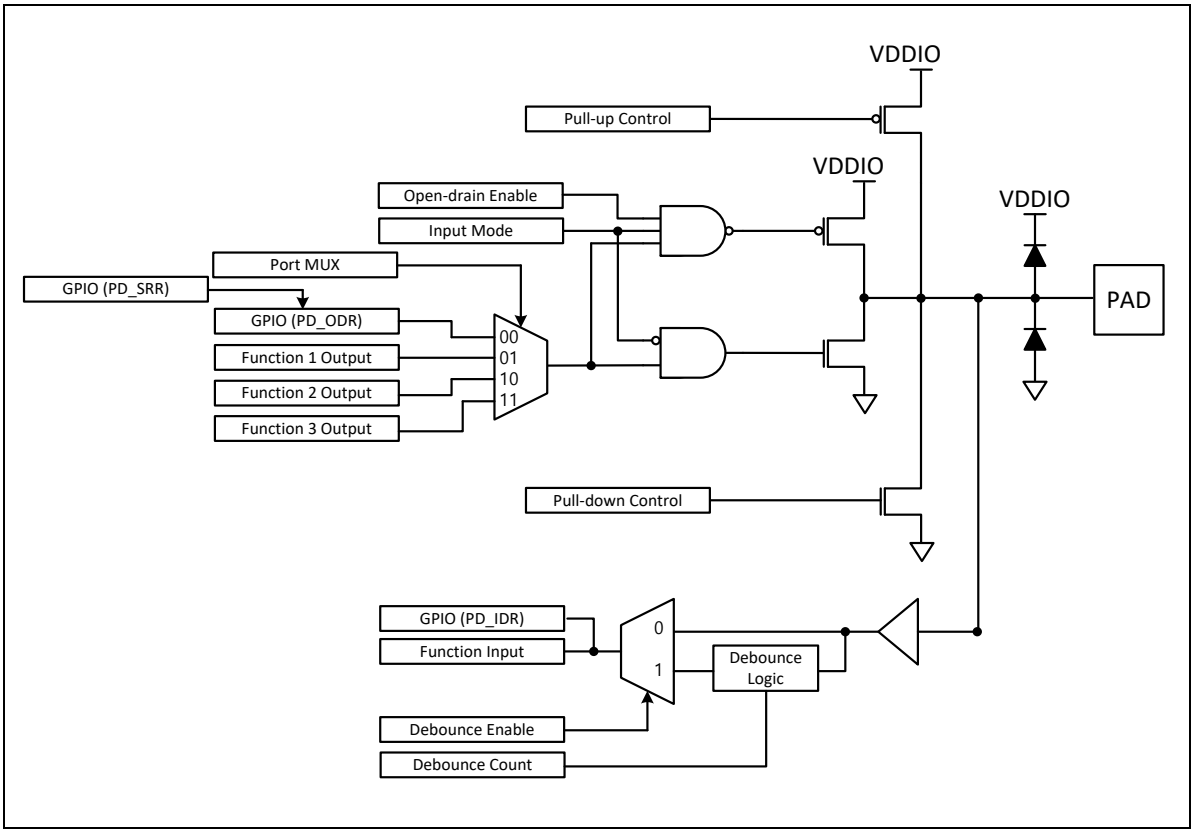


Figure 4.5. Block diagram of PD port

4.2.5 PE Port

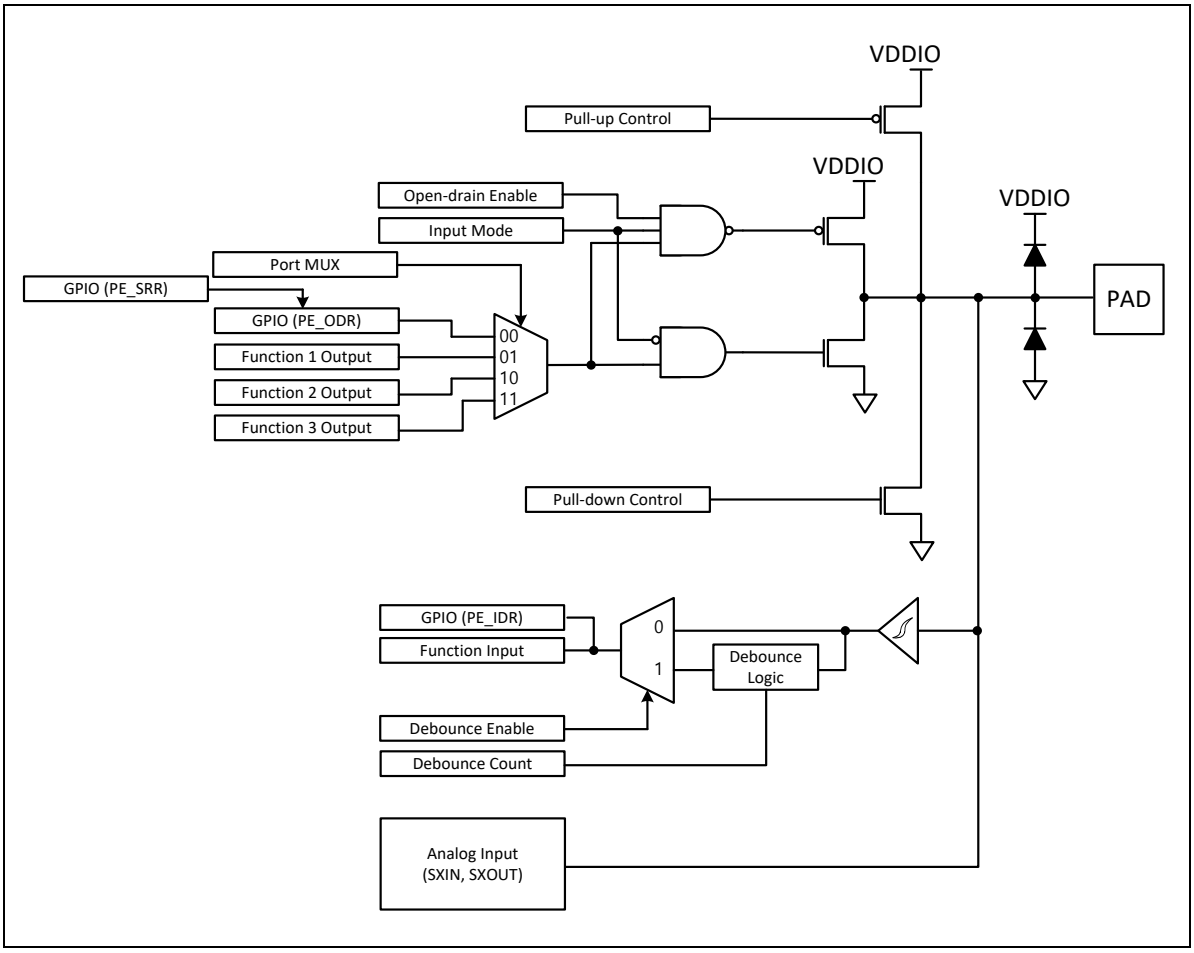


Figure 4.6. Block diagram of PE port

4.2.6 PF Port

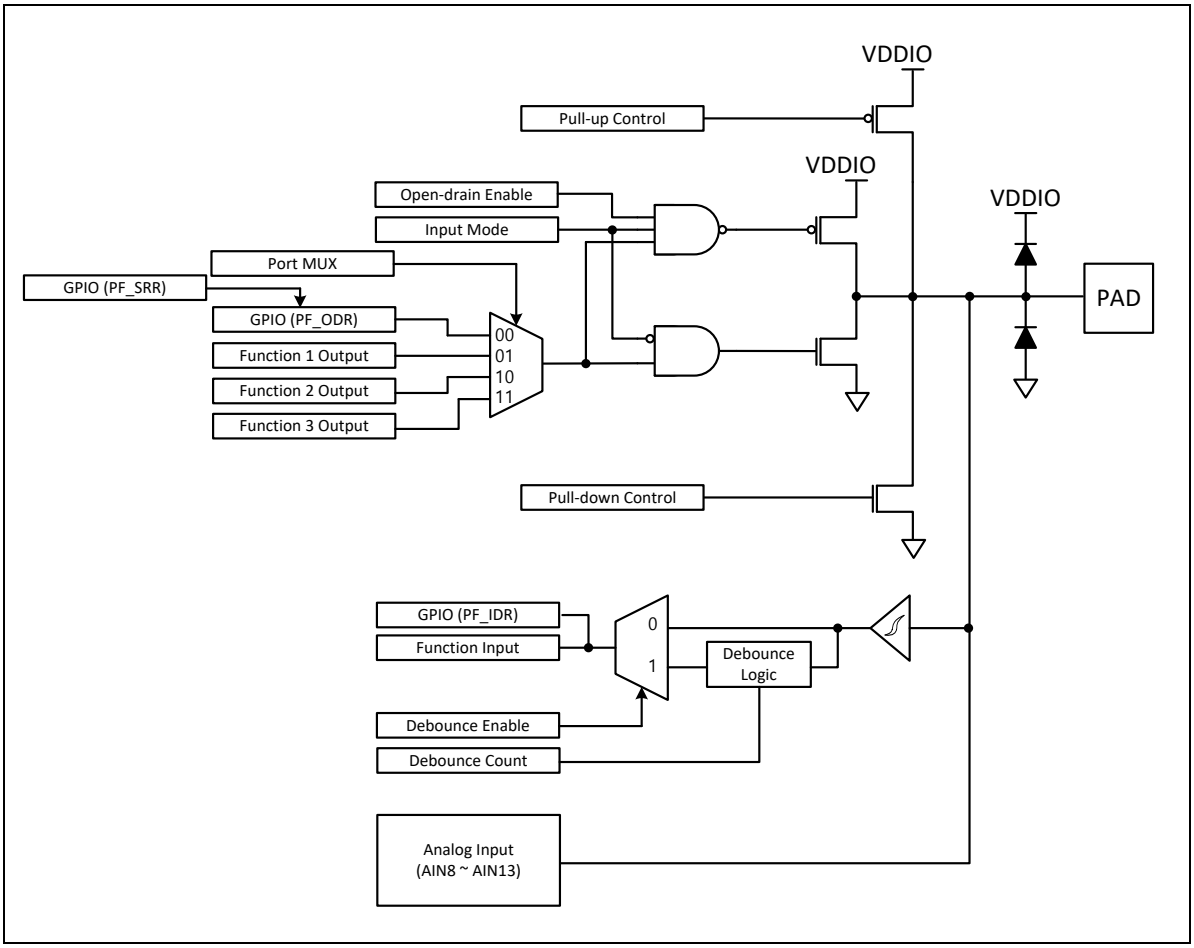


Figure 4.7. Block diagram of PF port

4.3 Pin Configuration

Every pin of A33G52x is a multi-function pin. The function selection for each port is shown as follows.

Table 4.2. Function selection of the external pins

Port	Pin	Function			
		00			00(default)
PA	0	**PA0**			AN0
	1	**PA1**			AN1
	2	**PA2**			AN2
	3	**PA3**			AN3
	4	**PA4**			AN4
	5	**PA5**			AN5
	6	**PA6**	T0C		AN6
	7	**PA7**	T1C		AN7
	8	**PA8**	T2C		
	9	**PA9**	T3C		
	10	**PA10**	T4C		
	11	**PA11**	T5C		
	12	**PA12**	T6C		
	13	**PA13**	T7C		
	14	**PA14**	T8C		AN14
	15	**PA15**	T9C		AN15
PB	0	**PB0**	T0O		
	1	**PB1**	T1O		
	2	**PB2**	T2O		
	3	**PB3**	T3O		
	4	**PB4**	T4O		
	5	**PB5**	T5O		
	6	**PB6**	T6O		
	7	**PB7**	T7O		
	8	**PB8**	T8O		
	9	**PB9**	T9O		
	10	**PB10**	SS0		
	11	**PB11**	SCK0		
	12	**PB12**	MOSI0		
	13	**PB13**	MISO0		
	14	**PB14**	SCL0		
	15	**PB15**	SDA0		

Table 4.3. Function selection of the external pins (continued-1)

포트	핀	기능			
		00	01	10	11
PC	0	PC0	**nTRST***		
	1	PC1	**TDI***		
	2	PC2	***TMS (SWDIO)**		
	3	PC3	***TCK (SWCLK)**		
	4	PC4	***TDO (SWO)**		
	5	**PC5**			
	6	PC6	**nRESET***		
	7	**PC7/BOOT**			
	8	**PC8**	RXD0		
	9	**PC9**	TXD0		
	10	**PC10**	RXD2		
	11	**PC11**	TXD2		
	12	**PC12**	STBYO		
	13	**PC13**	CLKO		
	14	**PC14**	XTALO		
	15	**PC15**	XTALI	CLKIN	
PD	0	**PD0**	PWMA0		
	1	**PD1**	PWMA1		
	2	**PD2**	PWMA2		
	3	**PD3**	PWMA3		
	4	**PD4**	PWMA4		
	5	**PD5**	PWMA5		
	6	**PD6**	PWMA6		
	7	**PD7**	PWMA7		
	8	**PD8**	SS1		
	9	**PD9**	SCK1		
	10	**PD10**	MOSI1		
	11	**PD11**	MISO1		
	12	**PD12**	RXD1		
	13	**PD13**	TXD1		
	14	**PD14**	SCL1		
	15	**PD15**	SDA1		

Table 4.4. Function selection of the external pins (continued-2)

포트	핀	기능			
		00	01	10	11
PE	0	**PE0**	PWM0B		
	1	**PE1**	PWM1B		
	2	**PE2**	PWM2B		
	3	**PE3**	PWM3B		
	4	**PE4**	PWM4B		
	5	**PE5**	PWM5B		
	6	**PE6**	PWM6B	RXD3	
	7	**PE7**	PWM7B	TXD3	
	8	**PE8**	SXIN		
	9	**PE9**	SXOUT		
	11	**PE11**	TraceD3		
	12	**PE12**	TraceD2		
	13	**PE13**	TraceD1		
	14	**PE14**	TraceD0		
	15	**PE15**	TraceCLK		
PF	0	**PF0**			AN8
	1	**PF1**			AN9
	2	**PF2**			AN10
	3	**PF3**			AN11
	4	**PF4**			AN12
	5	**PF5**			AN13
	7	**PF7**			
	8	**PF8**			
	9	**PF9**			
	10	**PF10**			
	11	**PF11**			

4.4 Functional Description

4.4.1 Port Function

All pins except a IO function pins of A33G52x can be used as GPIO. To use GPIO, first set the pin MUX register of the corresponding port to GPIO.
When the I/O port is set as the input function by the pin control register, the output function of the I/O port is disabled.
Depending on the function selection of the Pn_MR register and the direction selection of the Pn_PCR register,
The port function can be used differently. The input data register captures the current data or debounced input data to the I/O pins per GPIO clock cycle.

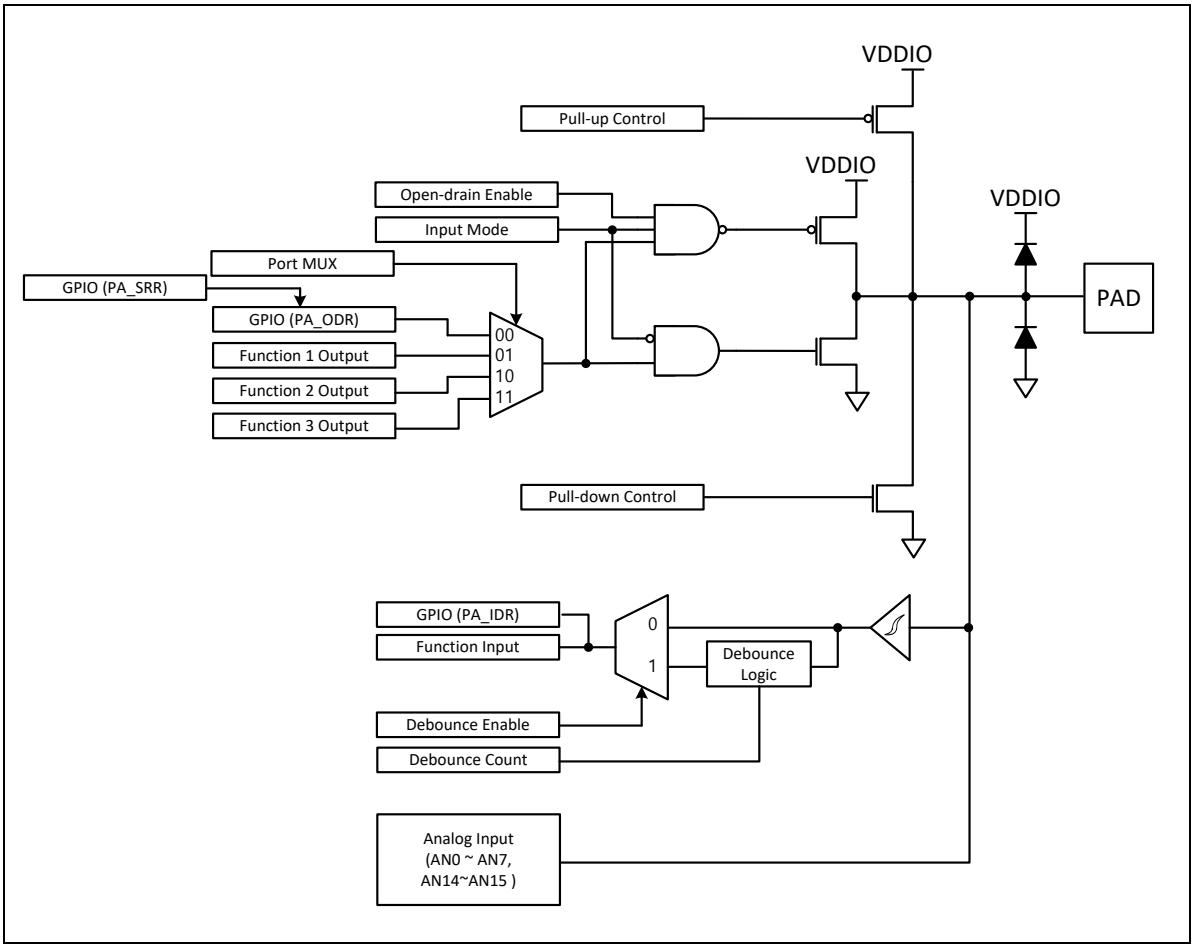


Figure 4.8. Block diagram of PA port (Example)

4.4.2 Debounce of Input Port

The input debounce function is supported on each port of the A33G52x. The debounce function is used to filter the interference noise of the input port to filter out the normal signal.
You can set the Pn_DPR register to adjust the filtering level of each 16-pin port and enable / disable for each pin.
The filtering level uses a clock that divides the PCLK clock by a 16-bit counter and can set this value.
The simplified block configuration is shown below.

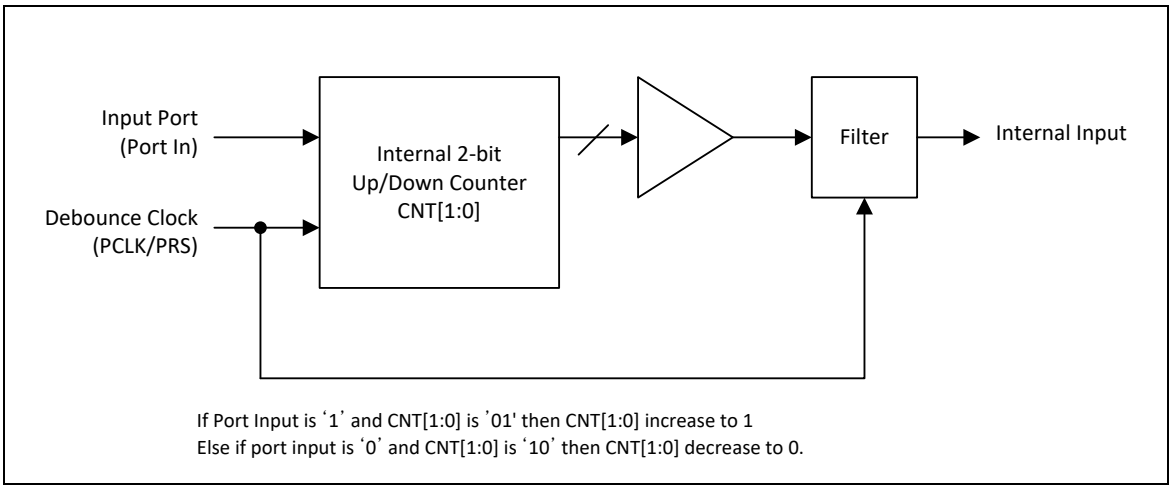


Figure 4.9. Simplified block diagram of a debounce port

When the debounce logic of the logic input is activated, the debounce function operates on the basis of the clock determined by DPR <4: 0> of Pn_DPR.
Debounce will change the input recognition value if the changed input is maintained for a maximum of 3 clocks continuously.
If the internal counter is '01', the input is set to '1'. If the internal counter is '10', it is set to '0'.
Otherwise, it retains its previous value without change.

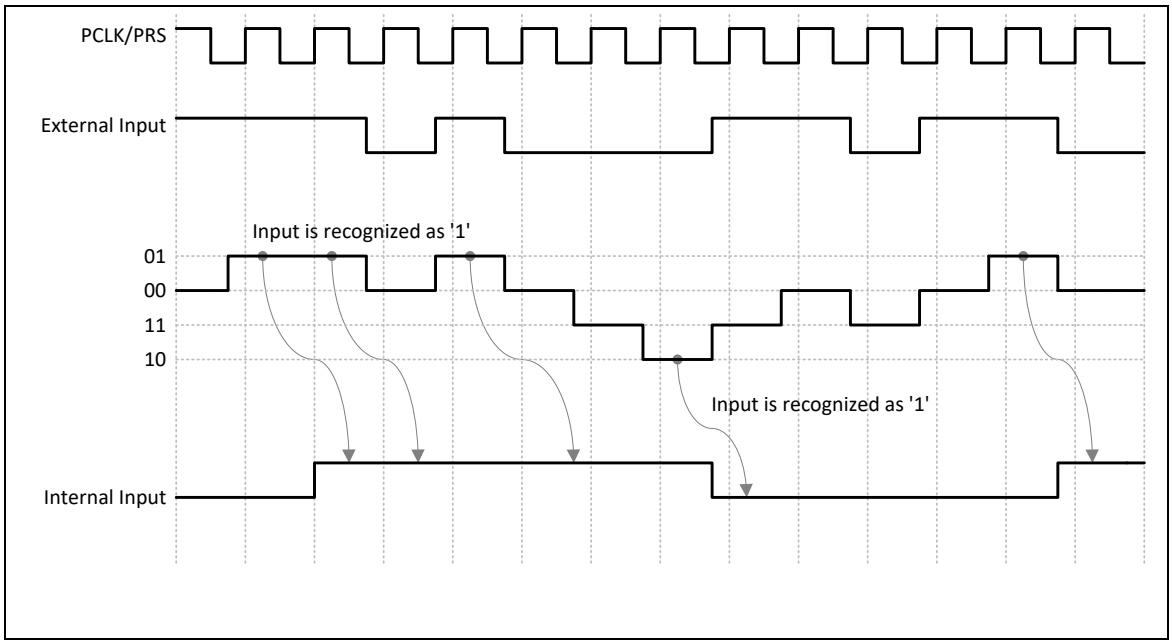


Figure 4.10. The timing of debounce function

4.4.3 GPIO Interrupt

There are six interrupt sources in the GPIO block of the A33G52x, and each port can be an interrupt source. To use an interrupt on any port of the GPIO, set the Pn_IER register to one of two ways to use the interrupt level or edge interrupt. You can set the level or rising edge, falling edge, and rising / falling edge in this next Pn_ICR register. If an interrupt is generated in this way, the interrupt flag bit of the corresponding port can be checked in the interrupt Pn_ISR register. To clear this bit value, write '1' to the correspondng bit of Pn_ISR.

Table 4.5. The pin configuration for each port

Port	Pins	Pin Name	Remark
PA	16	PA0 - PA15	Output or Schmitt-trigger input
PB	16	PB0 - PB15	Output or Schmitt-trigger input
PC	16	PC0 - PC15	Output or Schmitt-trigger input
PD	16	PD0 - PC15	Strong output or CMOS input
PE	15	PE0 - PE9, PE11 - PE15	Output or Schmitt-trigger input
PF	6	PF0 - PF5	Output or Schmitt-trigger input

CHAPTER 5. GPIO (General Purpose I/O)

Table 5.1. Operation Summary

Item	Pin Name	Remark
Clock usage	PCLK	
Reset Source	Set by PMU_PER	
Reset Generation	None	
Interrupt Generation	None	Included in PMC
Interrupt Clear Method	None	

5.1 Overview

The A33G52x can be used for application purposes by setting all pins to GPIO (General Purpose Input Output) except the VDD and GND pins. Each port consists of 16 bits. When the GPIO pin is set to output mode, the signal can be output by setting the value of each bit to 'H' or 'L'. When the GPIO pin is set to logic input, the signal input status can be checked by the corresponding bit value of each pin.

Features of GPIO (General Purpose Input Output)

- Output value (High/Low) selection function of each pin
- Function to check logic input status of each pin
- General Purpose GPIO Usage
- Pin function selection by PMC register

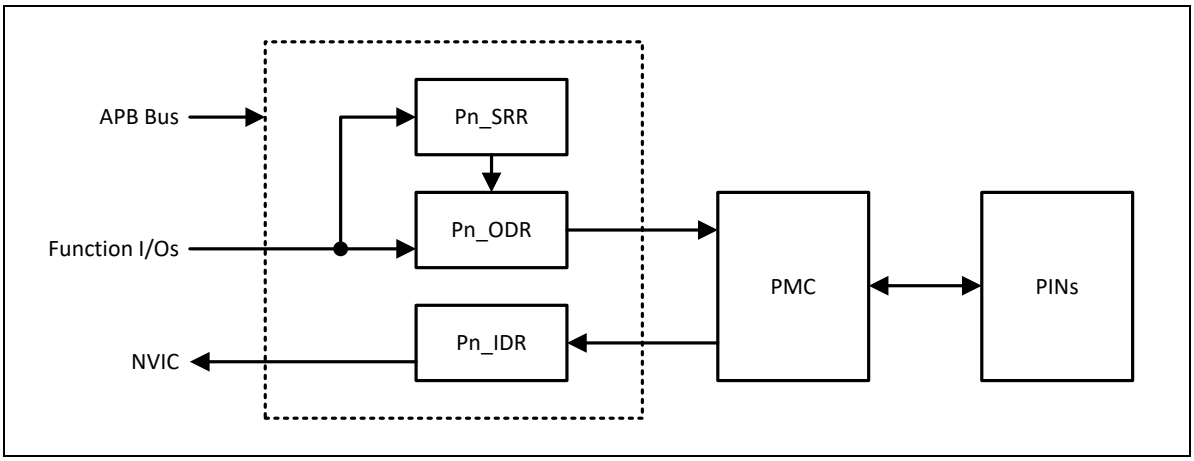


Figure 5.1. Block diagram of GPIO

5.2 Block Diagram

5.2.1 PA Port

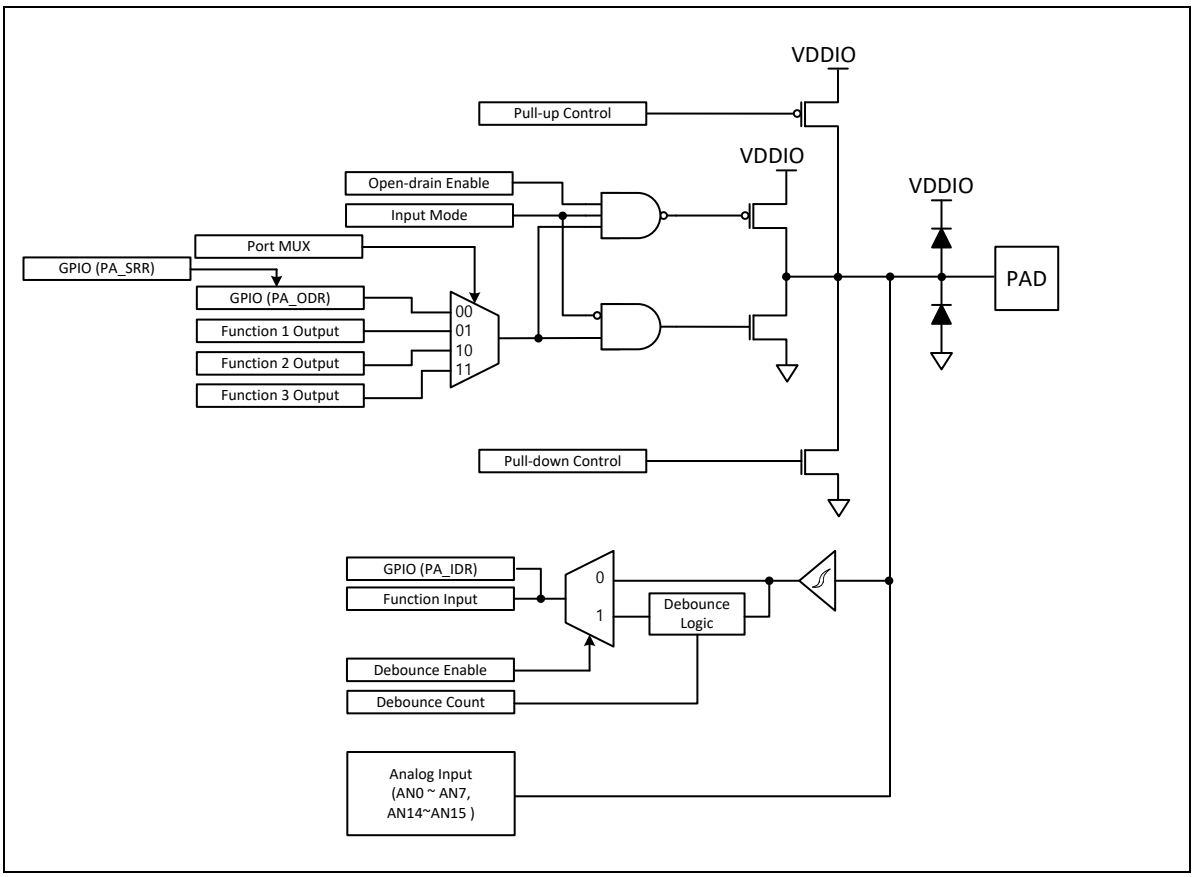


Figure 5.2. Block diagram of PA port

5.2.2 PB Port

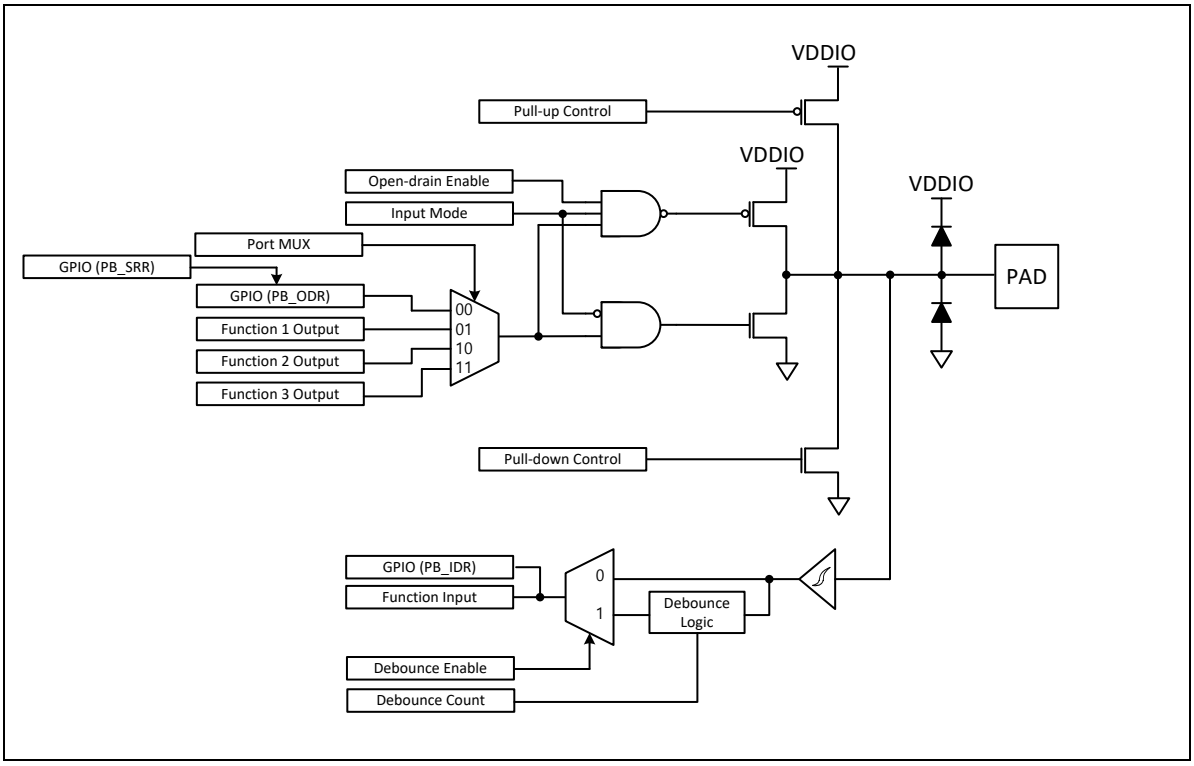


Figure 5.3.Block diagram of PB port

5.2.3 PC Port

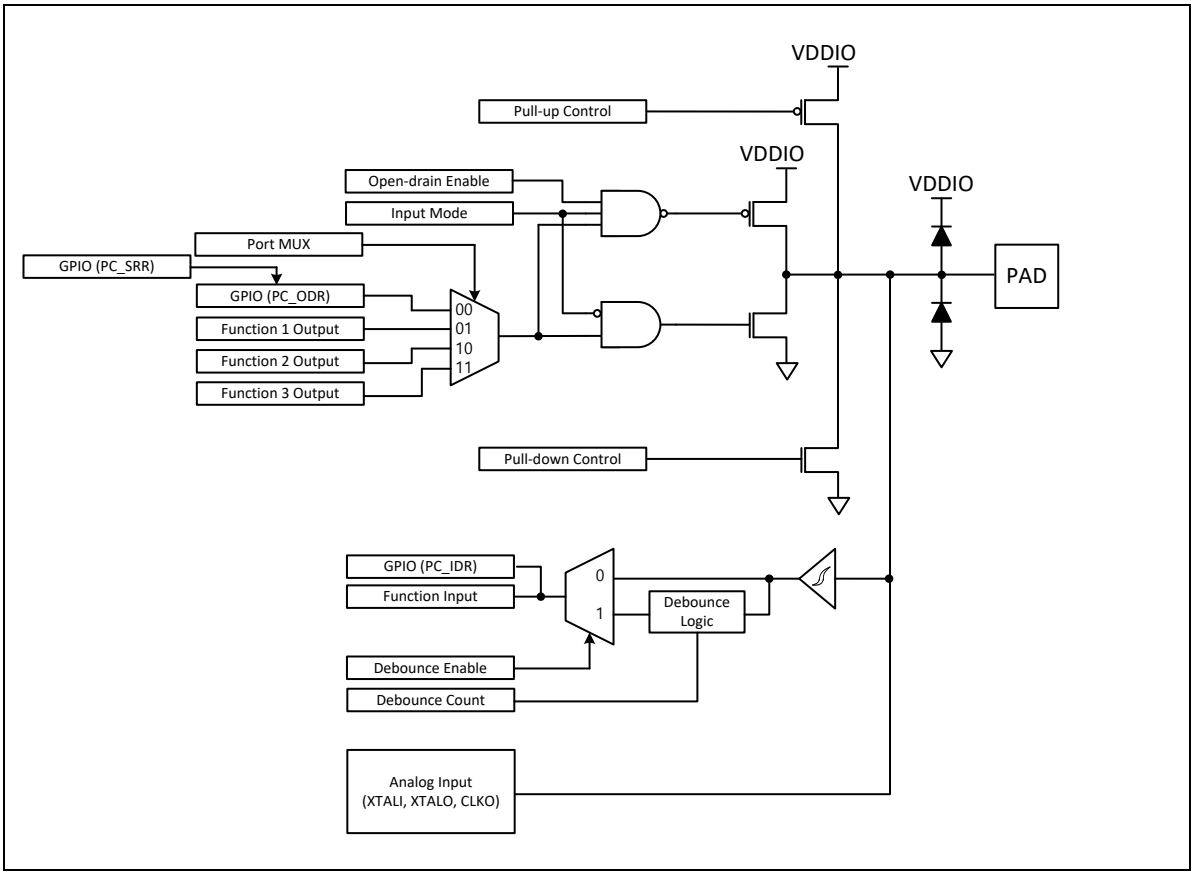


Figure 5.4. PC Block diagram of PC port

5.2.4 PD Port

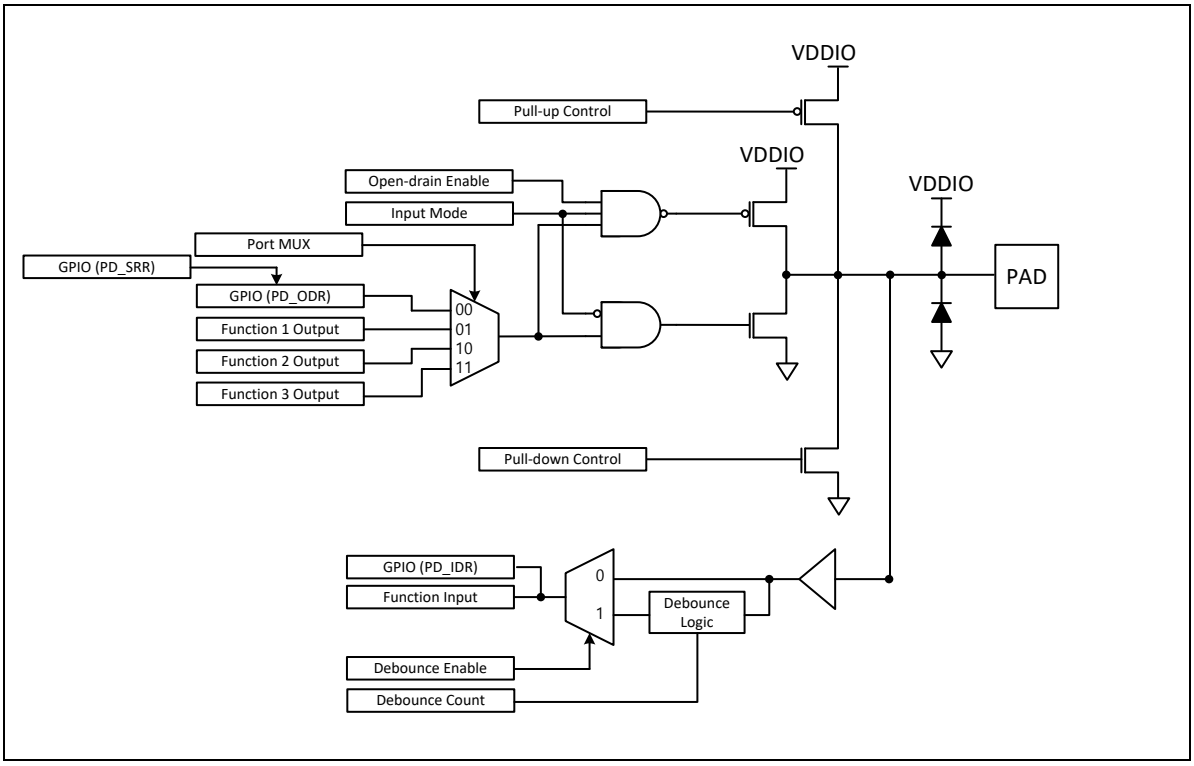


Figure 5.5. Block diagram of PD port

5.2.5 PE Port

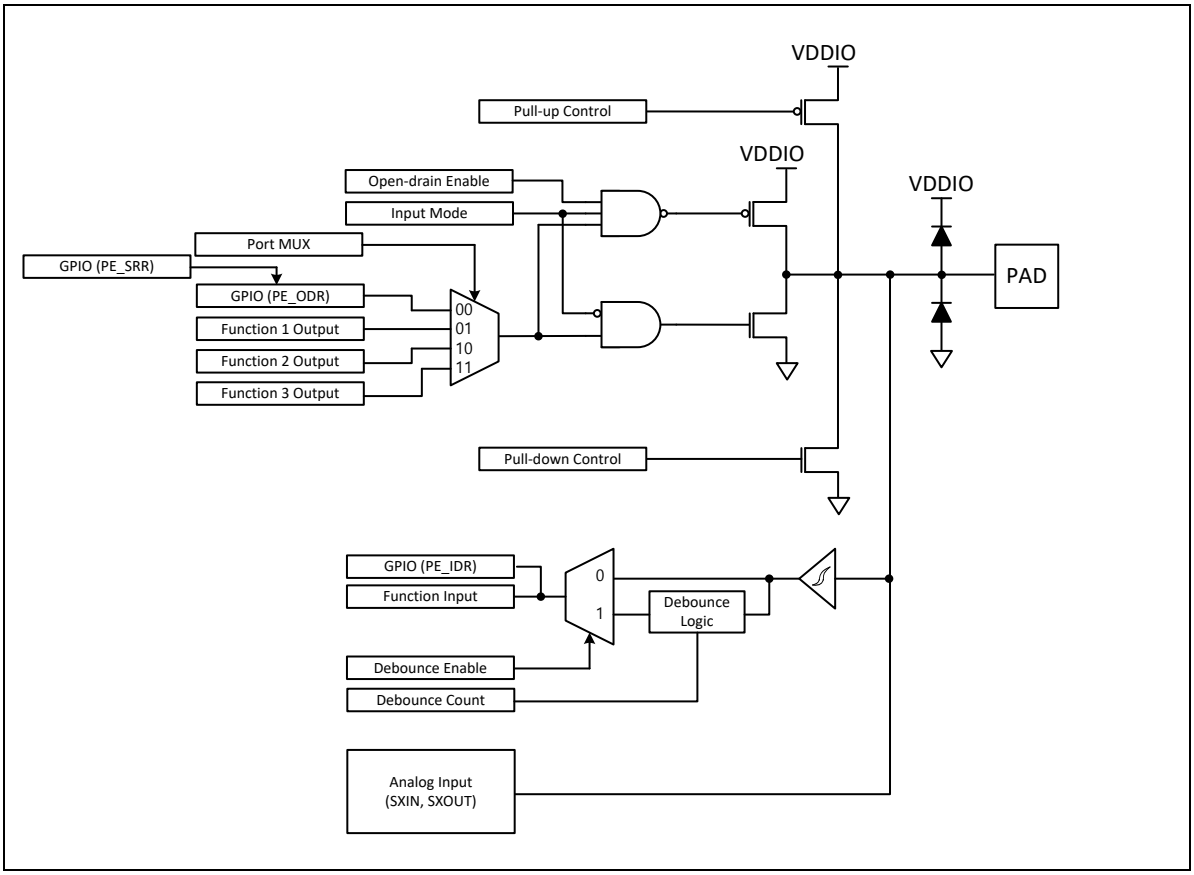


Figure 5.6. Block diagram of PE port

5.2.6 PF Port

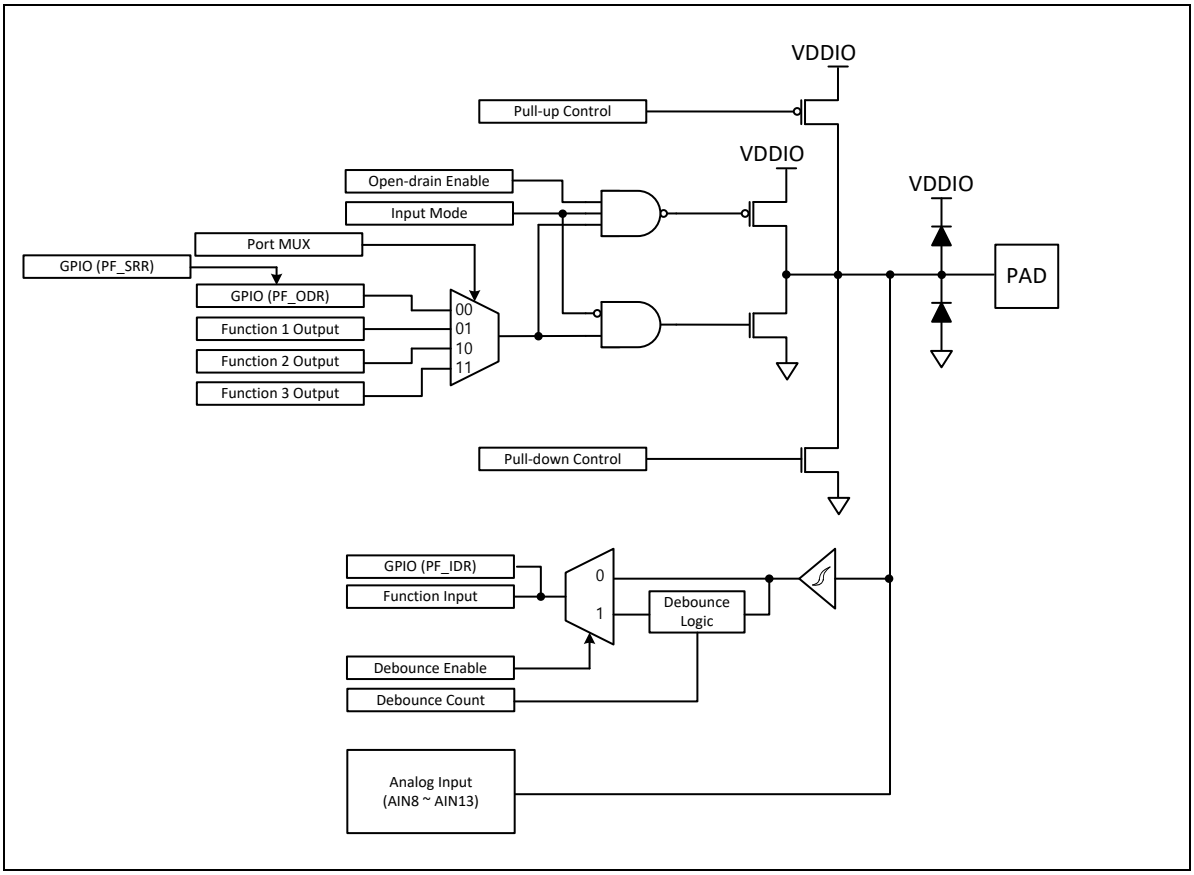


Figure 5.7. Block diagram of PF port

5.3 Pin Configuration

Most of the I/O pins of the A33G52x are multifunctional pins that perform more than two functions per pin. GPIO (General Purpose Input Output) output or input can be used after setting the pin function and direction of GPIO in PMC (Port Map Controller) block.

Table 5.2. The pin configuration for each port

Port	Pins	Pin Name	Remark
PA	16	PA0 - PA15	Output or Schmitt-trigger input
PB	16	PB0 - PB15	Output or Schmitt-trigger input
PC	16	PC0 - PC15	Output or Schmitt-trigger input
PD	16	PD0 - PC15	Strong output or CMOS input
PE	15	PE0 - PE9, PE11 - PE15	Output or Schmitt-trigger input
PF	6	PF0 - PF5, PF7 – PF11	Output or Schmitt-trigger input

5.4 Functional Description

All pins other than A33G52x function pins can be set to GPIO (General Purpose Input Output). To use GPIO, first set the pin MUX register on the port map controller (PMC) of that port to GPIO.

5.4.1 GPIO Interrupt

The GPIO block has six interrupt sources, and each port can be an interrupt source. To use each port of the GPIO as an interrupt source, set the edge or level and the polarity according to the interrupt generation method, and then set the interrupt enable register. Interrupts can be set for each pin by level or edge method. When an interrupt occurs, the corresponding bit of the port status register (PnISR) can be set to '1' to clear the interrupt flag.

Table 5.3 The Interrupt Pins of the GPIO block

Interrupt Source	Corresponding Pin
PA	Port A[15:0]
PB	Port B[15:0]
PC	Port C[15:0]
PD	Port D[15:0]
PE	Port E[15:0]
PF	Port F[11:0]

CHAPTER 6. 32-bit WDT

Table 6.1. Operation Summary

Item	Pin Name	Remark
Clock usage	RingOSC, IOSC16, PCLK, Main XTAL, Sub XTAL	Select by PMU_PCSR Built-in Prescler
Reset Source	Set by PMU_PER	
Reset Generation	When WDT counter value reaches ‘0’	Set by WDT_CON
Interrupt Generation	When WDT counter value reaches ‘0’ (WDT(3))	Set by WDT_CON
Interrupt Clear Method	Writng non-’0’ value to the WDT_CVR	WDT_CVR

6.1 Overview

WDT (Watschdog Timer) monitors the operation of the MCU and is typically used to detect the occurrence of software errors. When MCU is out of control due to a malfunction, the watchdog timer generates reset to exit from the out of control. A33G52x Watchdog Timer consists of a 32-bit down counter. If the watchdog timer was selected as a reset source, when current downcount value register counts down to '0', the MCU restarts. If the MCU monitoring function is not used, the WDT can be used as a periodic timer with interrupt.

Features of WDT (Watchdog Timer)

- 32-bit down-counting timer
- Reset by underflow of the WDT
- Interrupt with periodic timer or underflow
- Selectable input clock of the WDT
  - PCLK
  - Selected clock source in PMU_PCSR<WDTCS[1:0]> : Main XTAL, IOSC16, SXOSC, RINGOSC
- Support 8-Step prescaler for the WDT input clock
- Selectable operation mode of the WDT in debug-mode

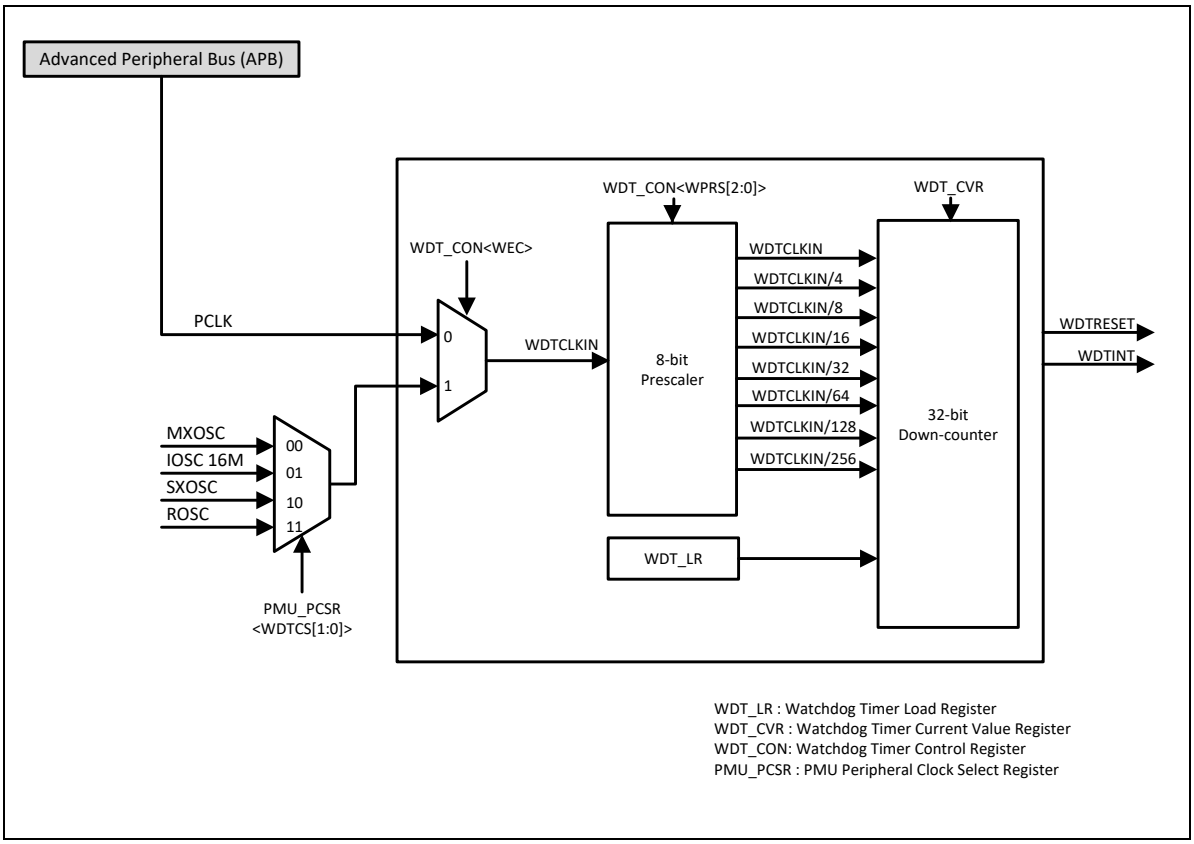


Figure 6.1. Block diagram

6.2 Operation Description

6.2.1 Control Downcounter of Watchdog Timer

If WDT(Watchdog Timer) is activated, WEN in WDT_CON register is set to ‘1’ and 32bits Downcounting with WDT_CVR register starts. In this case, WDT_CVR register must be set to prevent immediate reset or interrupt occurrence.
To chang the value of WDT_CVR, non-zero value should be written in WDT_LR when WEN is ‘1’, and the value of counter is reset if the value of counter is reloaded using WDT_LR register during operation of downcounter. However, the operating downcounter value must be greater than ‘0’.

6.2.2 Watchdog Timer Reset Mode

To reset WDT(Watchdog Timer), WRE of WDT_CON register and WDTRSTE(Bit 3) must be set to ‘1’. The reset by WDT(Watchdog Timer) to detect software errors occurs in transition state of downcounter from ‘1’ to ‘0’

6.2.3 Watchdog Timer Interrupt Mode

Watchdog Timer (WDT) interrupts can be used when certain safety tasks or data logging needs to be performed before the actual reset is generated.
Watchdog Timer interrupts is activated when WIE bit of WDT_CON register is set to ‘1’.
Interrupt ist generated when value of WDT_CVR register becomes ‘0’ (in trasition sate from ‘1’ to ‘0’), and WOF bit of WDT_CON register is set to ‘1’. To clear the WOF bit, non-zero value should be written in WDT_CVR with WDT_LR.

6.2.4 Using Watchdog Timer in Debug Mode

If the WDH bit of WDT CON register is set to ‘1’, watchdog timer counter in debug state can be stopped.
It can be checked that the downcounting of WDT(Watchdog Timer) is stopped when the debugging is paused after debugging run in debug mode, and it can be checked that the value of down counter decreases by 1 after debugging re-run.
Conversely, if the WDH bit is clear to '0', the Watchdog Timer counter continues to operate in the debug mode without stopping. When debugging is paused after debugging run, the value of the downcounter seems to be stopped, but it can be checked that the value is decreased after debugging re-run because of in operation of the downcounter.

CHAPTER 7. 32-bit FRT (32-bit Free-run Timer)

Table 7.1. Operation Summary

Item	Pin Name	Remark
Clock usage	RINGOSC, IOSC16, MXOSC, SXOSC PCLK	Set by PMU_PCSR or FRT_CON Built-in prescaler
Reset Source	Set by PMU_PER	
Reset Generation	None	
Interrupt Generation	When FNT_CNT=FRT_PRD, (FRT(4))	Interval mode
Interrupt Clear Method	Writing '0' to the FMF and FOF bit	FRT_CON

7.1 Overview

The A33G52x has a built-in 32-bit up-count timer for FRT (Free-run Timer). This FRT (Free-run Timer) can perform overflow interrupts or match interrupts according to the setting period of user application.

Features of FRT (Free-run Timer)

- 32-bit up-count timer
  - Periodic timer mode accoding to setting period
  - Free-run timer mode
- FRT (Free-run Timer) interrupts
  - Overflow interrupt
  - Match interrupt
- FRT (Free-run Timer) intput clocks
  - PCLK
  - Selected clock source by PMU_PCSR<FRTCS[3:2]> : Main XTAL, IOSC16, SXOSC, RINGOSC
- 8-steps FRT prescaler support for FRT (Free-run Timer) input clock

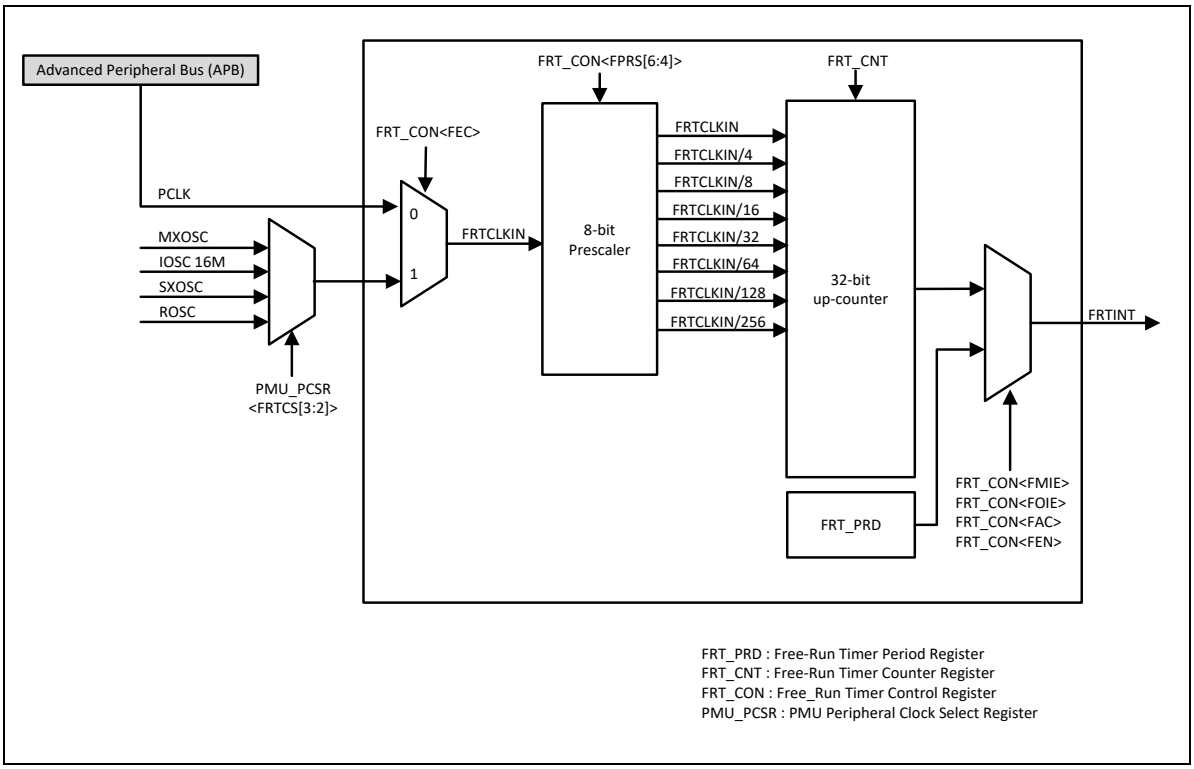


Figure 7.1. Block diagram of FRT (Free-run Timer)

7.2 Functional Description

The operation mode of A33G52x FRT (Free-run Timer) is determined by FRT_CON<FAC> bit value.
When FRT_CON<FAC> value is set to '0', FRT (Free-run Timer) runs in free-runs mode and when FRT_CON<FAC> value is set to '1', FRT (Free-run Timer) runs in periodic mode.
When FRT runs in free-run timer mode, FRT_CON<FOIE> bit determines whether overflow interrupt occurs. When FRT runs in periodic timer, FRT_CON<FMIE>bit determines whether match interrupt occurs.

7.2.1 Free-run Mode

When FRT (Free-run Timer) operates free-run mode, FRT_CNT value increases from 0 to 0xFFFF_FFFF regardless of FRT_PRD value. If FRT_CNT value reaches to 0xFFFF_FFFF, the next value is set to 0. In this case, FRT_CON<FOIE> bit was set to '1', an overflow interrupt occurs when FRT_CNT value changes from 0xFFFF_FFFF to 0.

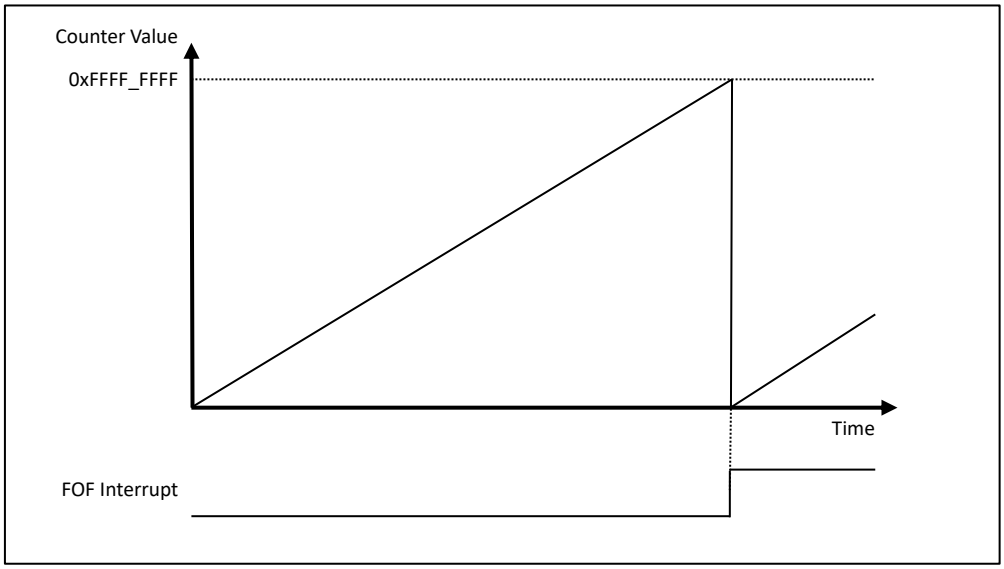


Figure 7.2. A Operating Timing in Free-run mode

7.2.2 Periodic timer mode

When the FRT (Free-Run Timer) is executed in the periodic timer mode, the FRT_CNT value is initialized to 0 and counted up again when the FRT_CNT value becomes equal to the FRT_PRD value. At this moment, If the FRT_CON<FMIE> bit was set to '1', a match interrupt occurs.

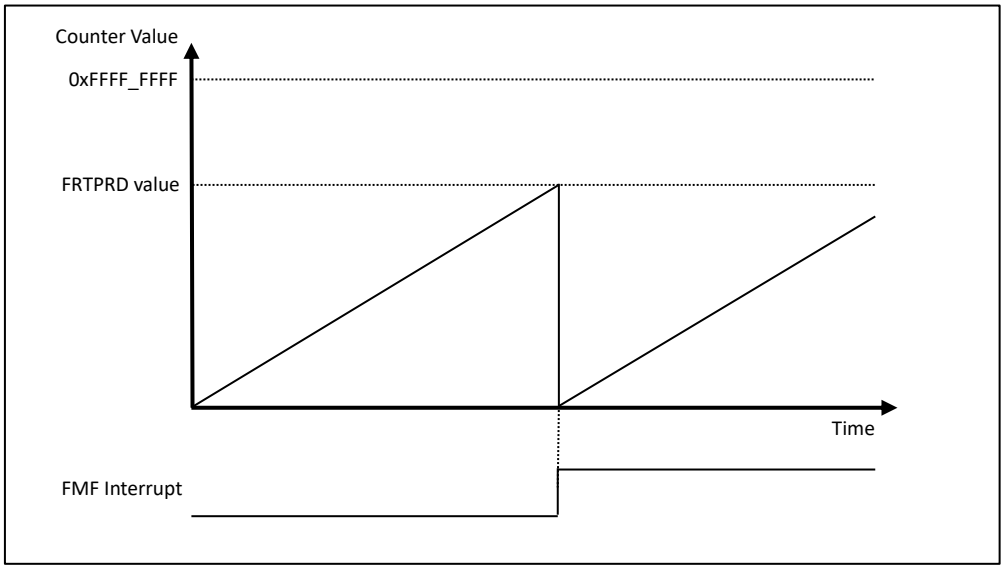


Figure 7.3. A Operating Example in Periodic mode-1

If the FRT_CNT value is set to a value larger than FRT_PRD, FRT_CNT initializes 0xFFFF_FFFF, and the next operation is the same as the periodic timer mode. In this case, Although FRT_CON<FOIE> bit was set to 1, match interrupt does not occur when FRT_CNT value changes from 0xFFFF_FFFF to 0. In this case, if the FRT_CNT value changes from 0xFFFF_FFFF to 0, even though the FRT_CON <FOIE> bit is set to 1, no match interrupt occurs.

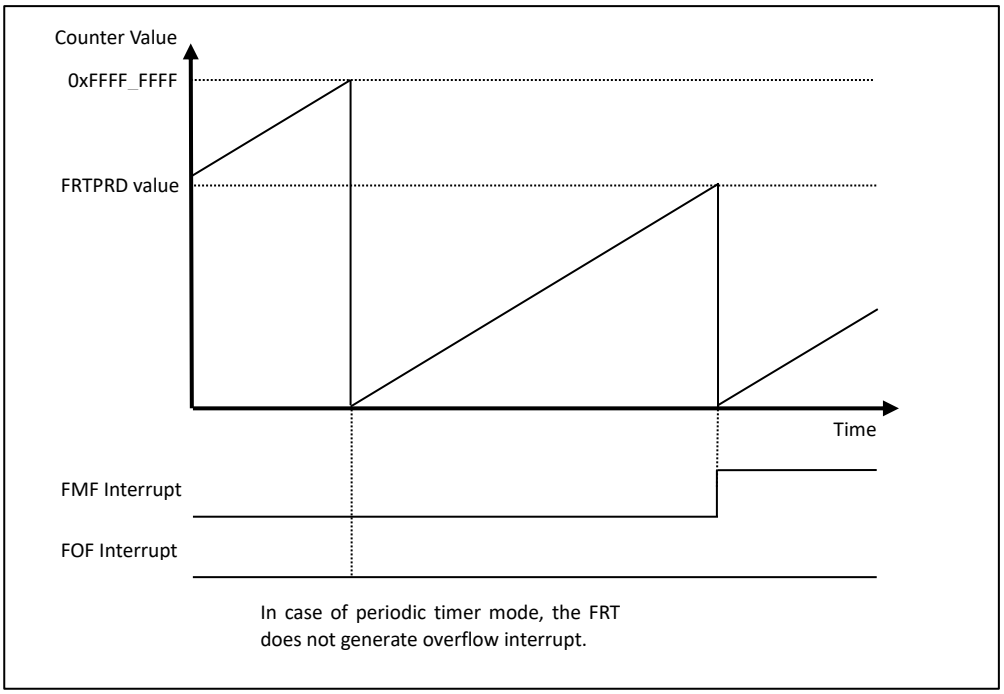


Figure 7.4. A operating example in periodic mode-2

7.2.3 Timing Calculation of FRT (Free-run Timer)

FRT interval timer mode, the timer is assumed to calculate the timing. Clock source PCLK 16MHz, FRTPRD value is 0x4000 (16384), FPRS = 000 is assumed.

1-clock period : 1/16MHz = 0.0625 µsec
Interrupt interval : 0.0625 µsec x 16384 = 1.024 msec

The table below shows the interval of interrupt depending on the FPRS values.

Table 7.2. Interrupt intervals according to the FPRS value(PCLK=16MHz, FRTPRD=0x4000)

FRT_CON<FPRS[6:4]>	Clock Source	Interval of Interrupt
000	FRTCLKIN	1.024 msec
001	FRTCLKIN/4	4.096 msec
010	FRTCLKIN/8	8.192 msec
011	FRTCLKIN/16	16.384 msec
100	FRTCLKIN/32	32.768 msec
101	FRTCLKIN/64	65.536 msec
110	FRTCLKIN/128	131.072 msec
111	FRTCLKIN/256	262.144 msec

CHAPTER 8. 16-bit TIMER

Table 8.1. Operation Summary

Item	Pin Name	Remark
Clock usage	RINGOSC, IOSC16, MXOSC, SXOSC PCLK, TnC	Set by PMU_PCSR Set by TIMERn_CON Built-in prescaler
Reset Source	Set by PMU_PER	
Reset Generation	None	
Interrupt Generation	Timer mode: Match/Clear/Overflow Capture mode : Capture Input (TIMER0(5) ~ TIMER9(14))	Set by TIMERn_CON
Interrupt Clear Method	Writing '1' to the interrupt bit	TIMERn_CON

8.1 Overview

The A3352x MCU has a 16-bit timer with 10 channels. The clock source of 16-bit timer can be inputted by peripheral system clock (PCLK) or by external clock source. And it has a built-in 10-bit prescaler that can generate various timer clocks. . This 16-bit timer supports four types of operating modes: periodic timer mode, PWM mode, one shot mode, and capture mode. If the 16-bit timer operates in the periodic mode, a certain periodic interrupt set by the user may occur. When the 16-bit timer operates in PWM mode, the PWM signal can be output by adjusting the period and duty. In one-shot mode and PWM mode, one PWM signal is output. One shot and PWM mode is a mode that can output one PWM waveform. Capture mode can able to measure the time of signal accoding to condition of external input signalWhen using the capture mode, the time interval of the signal can be measured according to the set condition of the external input signal. You can also export output to the outside to control other devices.

Main features of 16-bit TIMER

- 16-bit upcount timer
- 4 types of operating modes
  - Periodic timer mode
  - One-shot timer mode
  - PWM mode
  - Capture mode
- Timer Interrupts
  - Match interrupt [1:0] / Overflow interrupt
- Timer Input clocks
  - 4-steps (1/2, 1/4, 1/8, 1/16) Prescaler of PCLK
  - Clock source selected by PMU_PCSR : Main XTAL, IOSC16, SXOSC, RINGOSC
  - Timer clock source through the input of TnC port
- 10-bit prescaler for timer input clock division

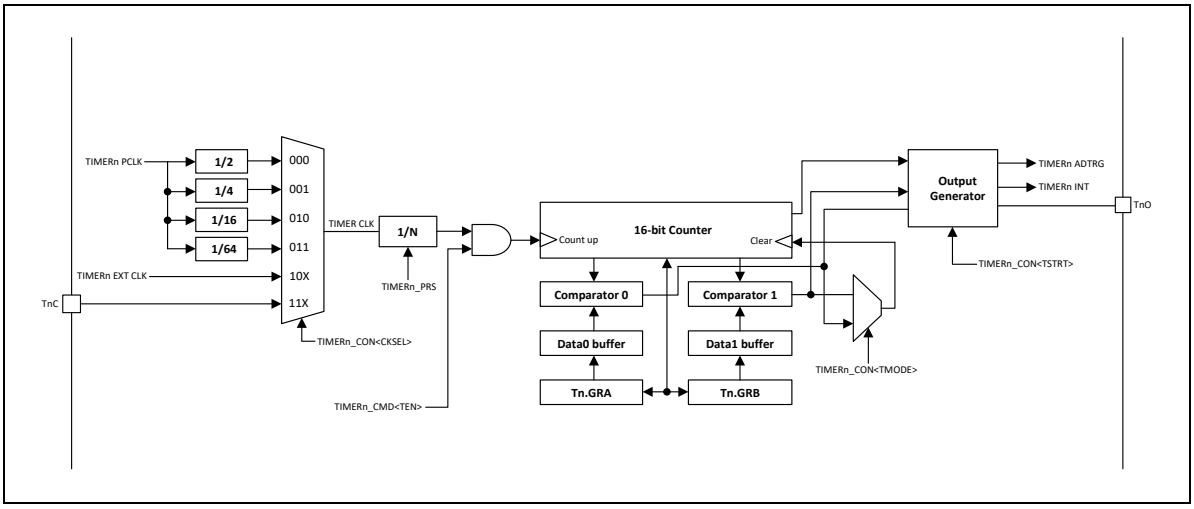


Figure 8.1. Block diagram of 16-bit Timer

8.2 Pin Configuration

Table 8.2. The external pin of 16-bit timer

Pin Name	Type	Description	Support by package		
			A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G526MM A33G526ML A33G524MM A33G524ML	A33G527VQ A33G527VL A33G526VQ A33G526VQ
T0C	I	Timer0 capture input signal / external clock input	O	O	O
T1C	I	Timer1 capture input signal / external clock input	O	O	O
T2C	I	Timer2 capture input signal / external clock input	O	O	O
T3C	I	Timer3 capture input signal / external clock input	O	O	O
T4C	I	Timer4 capture input signal / external clock input	O	O	O
T5C	I	Timer5 capture input signal / external clock input	O	O	O
T6C	I	Timer6 capture input signal / external clock input	O	O	O
T7C	I	Timer7 capture input signal / external clock input	-	-	O
T8C	I	Timer8 capture input signal / external clock input	O	O	O
T9C	I	Timer9 capture input signal / external clock input	O	O	O
T0O	O	Timer0 Timer/PWM/One-shot Output	O	O	O
T1O	O	Timer1 Timer/PWM/One-shot Output	O	O	O
T2O	O	Timer2 Timer/PWM/One-shot Output	O	O	O
T3O	O	Timer3 Timer/PWM/One-shot Output	O	O	O
T4O	O	Timer4 Timer/PWM/One-shot Output	O	O	O
T5O	O	Timer5 Timer/PWM/One-shot Output	O	O	O
T6O	O	Timer6 Timer/PWM/One-shot Output	O	O	O
T7O	O	Timer7 Timer/PWM/One-shot Output	O	O	O
T8O	O	Timer8 Timer/PWM/One-shot Output	-	O	O
T9O	O	Timer9 Timer/PWM/One-shot Output	-	O	O

8.3 Functional Description

8.3.1 The default behavior of 16-bit timer

TMCLK in Figure 8.2 is the reference clock for timer operation. This clock can be run counting clock by dividing prescalervalue of timer This clock can be operated by counting the value set in the prescaler register. The figure below shows the start and end points of the counter in the timer's periodic mode.

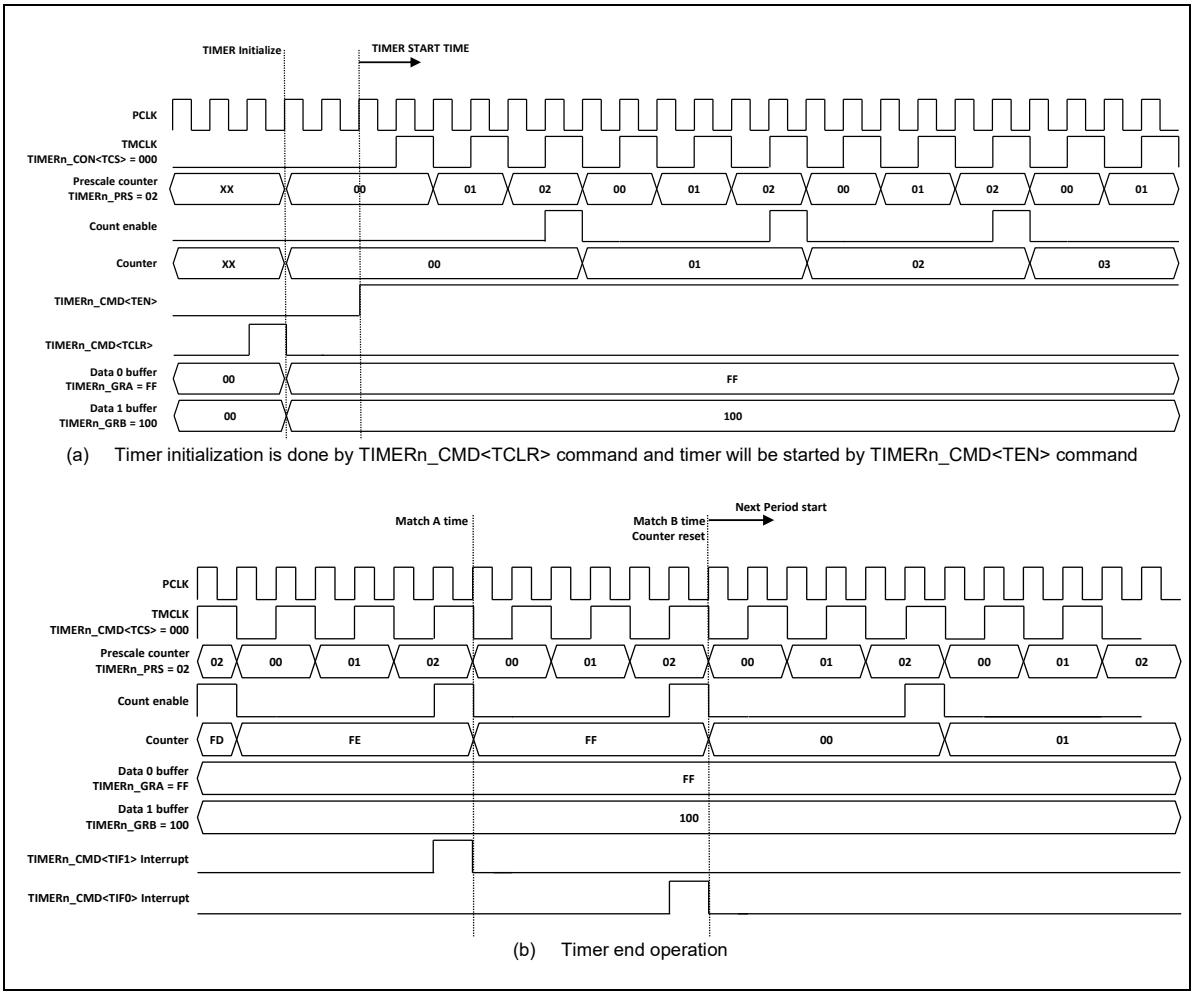


Figure 8.2 Timer base start and match actions

The timer count period can be obtained by the following formula:
Period = TMCLK Period * TIMERn_GRA Value
Match A Interrupt Timing = TMCLK Period * TIMERn_GRA Value

It is recommended to write the value first in the TCLR of TIMERn_CMD before changing the TEN bit value of TIMERn_CMD when changing timer setting or restarting with new setting value.

8.3.2 Periodic mode of 16-bit timer

Figure8.3 is shown the timing of 16-bit timer's periodic mode. The TIMERn_GRA value defines the period of the timer, but the TIMERn_GRB value does not affect the period of the timer.

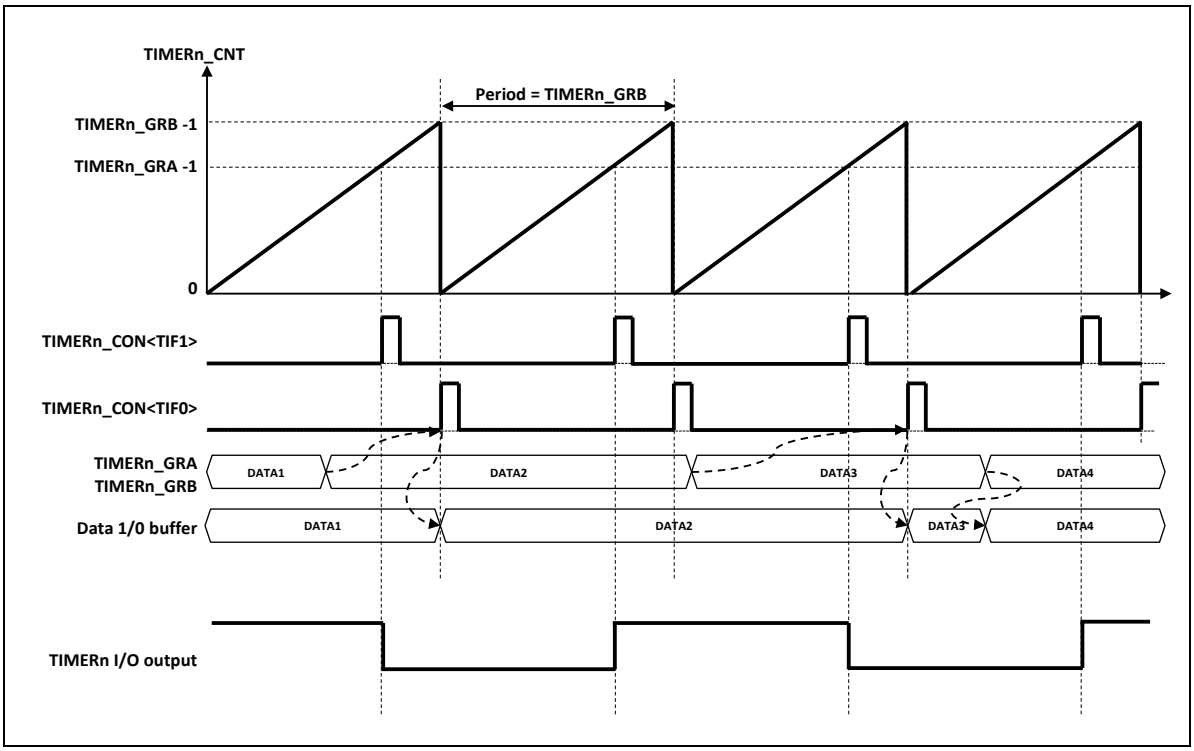


Figure 8.3 The periodic mode operation of 16-bit timer

The timer count period in periodic mode can be obtained by the following formula:

Period = TMCLK Period * TIMERn_.GRA Value
Match A Interrupt Timing = TMCLK Period * TIMERn_GRA Value

If TIMERn_GRA value is '0', it means that the timer period is '0'. In this case, the TIMERn_CMD <TEN> bit is set to '1' to execute the timer, but the timer does not work.
When a load condition occurs, the TIMERn_GRA and TIMERn_GRB values are loaded into the internal comparison data 0 buffer. In periodic mode, the TCLR behavior of the TIMERn_CMD register is loaded into the data buffer and the next GRA match event is loaded into the data buffer.

8.3.3 One-shot mode of 16-bit timer

Figure8.4 is shown the timing of 16-bit timer's one-shot mode.
The TIMER_nGRB value determines the one-shot period, and the other comparison point is provided by TIMERn_GRA.

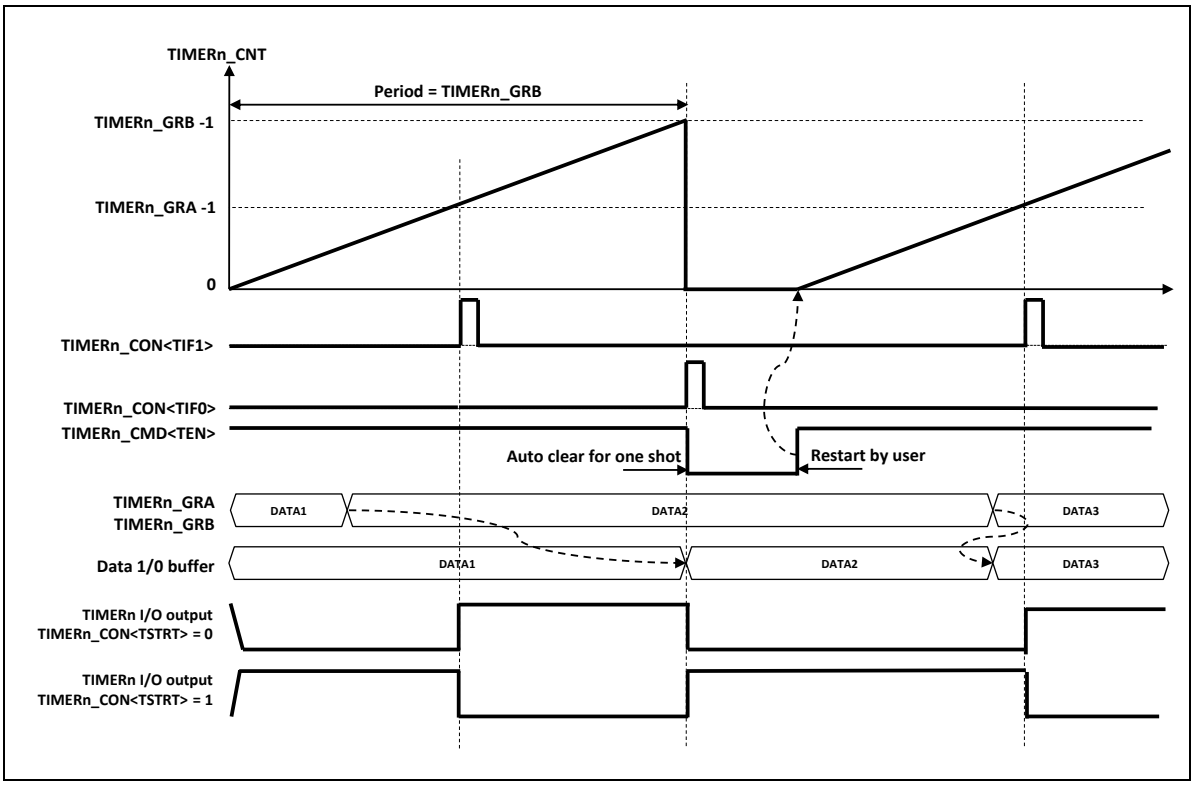


Figure 8.4 The one-shot mode operation of 16-bit timer

The timer count period in one-shot mode can be obtained by the following formula:

Period = TMCLK Period * TIMERn_GRB Value
Match A Interrupt Timing = TMCLK Period * TIMERn_GRA Value

If TIMERn_GRB value is '0', it means that the timer period is '0'. In this case, the TIMERn_CMD <TEN> bit is set to '1' to execute the timer, but the one-shot timer does not work.
When a load condition occurs, the TIMERn_GRA and TIMERn_GRB values are loaded into the internal compare data 0 buffer and data 1 buffer. In one-shot mode, the TCLR write behavior of the TIMERn_CMD register is loaded into the data buffer and the next GRB match event is loaded into the data buffer.
The signal output from the TnO pin is the same as in PWM mode. The TIMERn_GRB value defines the period of the output pulse and the TIMERn_GRA value defines the duty of the one-shot pulse.

8.3.4 PWM mode of 16-bit timer

Figure8.5 is shown the timing of 16-bit timer's PWM mode. The TIMERn_GRB value determines the PWM pulse period and the TIMERn_GRA value, which is a comparison point, determines the PWM pulse duty.

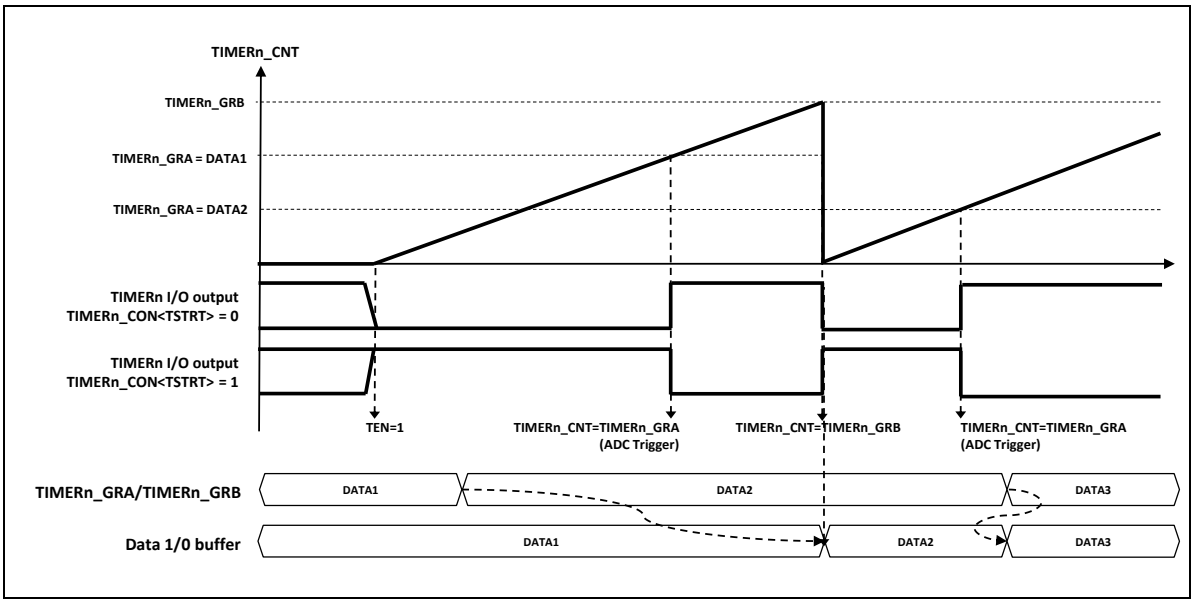


Figure 8.5 The PWM mode operation of 16-bit timer

The timer count period in PWM mode can be obtained by the following formula:

Period = TMCLK Period * TIMERn_GRB Value
Match A Interrupt Timing = TMCLK Period * TIMERn_GRA Value

If TIMERn_GRB value is '0', it means that the timer period is '0'. In this case, the TIMERn_CMD <TEN> bit is set to '1' to execute the timer, but the PWM timer does not work.
When a load condition occurs, the TIMERn_GRA and TIMERn_GRB values are loaded into the internal compare data 0 buffer and data 1 buffer. In one-shot mode, the TCLR write behavior of the TIMERn_CMD register is loaded into the data buffer and the next GRB match event is loaded into the data buffer.
The signal output from the TnO pin is PWM. The TIMERn_GRB value defines the period of the output pulse and the TIMERn_GRA value defines the duty of the one-shot pulse. The level of the voltage to be output when this PWM starts operation can be controlled by the value of the TSTRT bit in the TIMERn_CON register.
The ADC trigger generator is enabled with Match interrupt time.

8.3.5 Capture mode of 16-bit timer

Figure8.6 is shown the timing of 16-bit timer's capture mode.
TnC is used for pulse acquisition of the input signal. Counter values can be captured according to the capture conditions such as rising or falling edges.

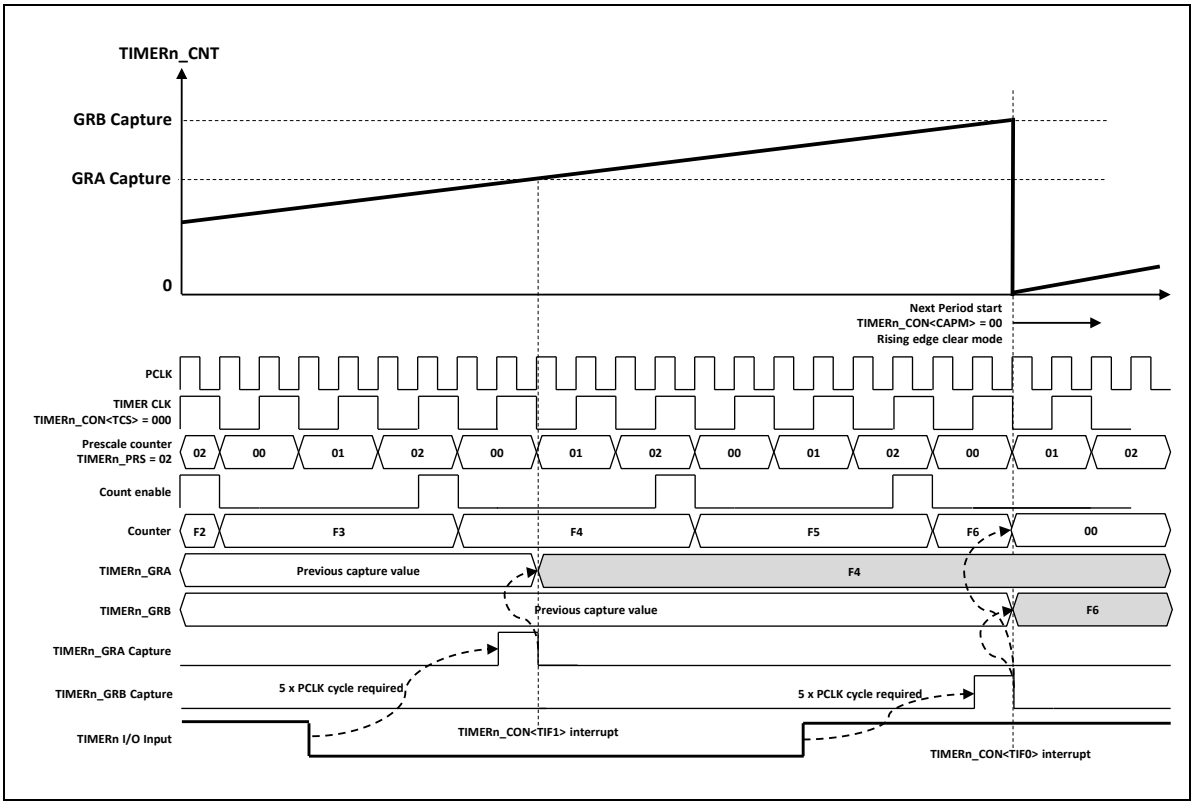


Figure 8.6 The capture mode operation of 16-bit timer

Timer capture internally requires a minimum of 5 PCLK clock cycles, and the actual capture point is the rising or falling edge of the TnC input signal after 5 clock cycles. The internal counter value can be cleared by the rising edge or falling edge with the CAPM bit in the TIMERn_CON register.

8.3.6 ADC Trigger mode of 16-bit timer

A33G52x's 16-bit timer can generate the ADC start trigger signal and can be the trigger source for a ADC block. The ADC trigger source control of timer can be set in ADC control register (ADC_CON)
Figure8.6 is shown the timing of 16-bit timer's ADC trigger mode. To use a timer as the ADC trigger source, the ADC conversion rate must be less than the timer period. Otherwise, an overrun situation will occur. The ADC ACK is not needed because the trigger signal is automatically cleared after 3 PCLK clock pulses.

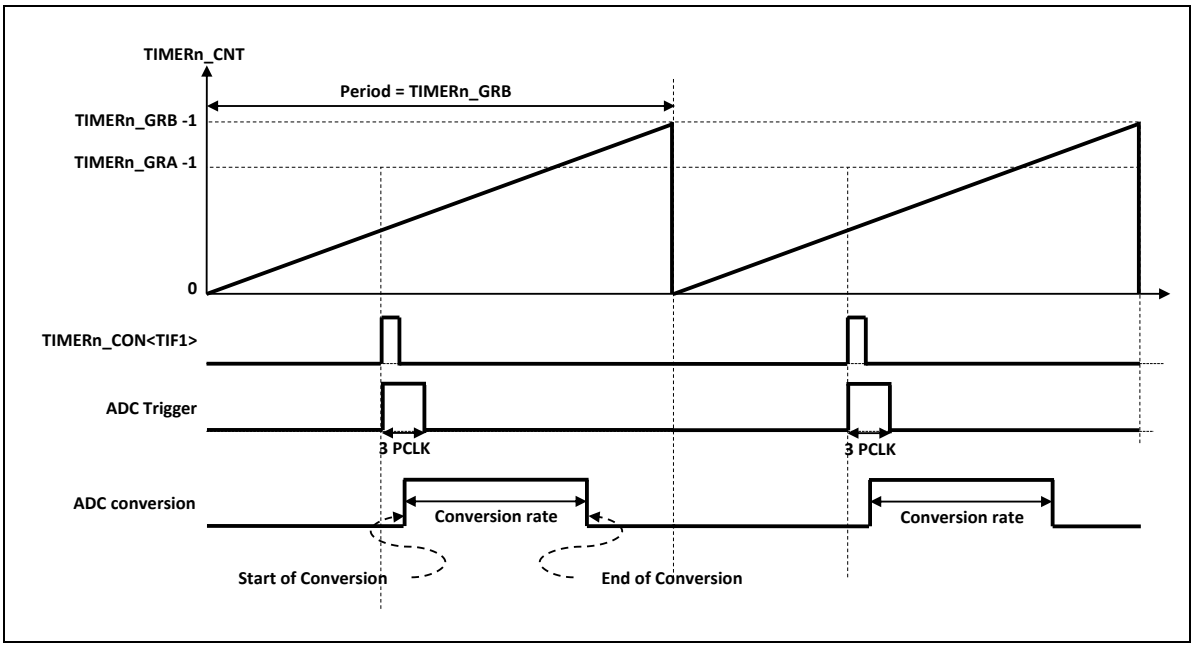


Figure 8.7 Block Diagram for ADC Trigger Timing of 16-bit timer

CHAPTER 9. PWM Generator

Table 9.1. Operation Summary

Item	Pin Name	Remark
Clock usage	PCLK	Built-in prescaler
Reset Source	Set by PMUPER	
Reset Generation	When PWM counter is cleared to '0'	Set by PWMn_CTRL
Interrupt Generation	When PWM counter is cleared to '0' (PWM0(24) ~ PMW7(31))	Set by PWMn_CTRL
Interrupt Clear Method	When writing non-'0' value ot PRF	PWMn_CTRL

9.1 Overview

The A33G52x has eight built-in PWM (Pulse-Width Modulation) generators that can output PWM (Pulse-Width Modulation) waveforms. This PWM (Pulse-Width Modulation) generator has a 16-bit resolution, four channels form a 1-unit, and each unit has a built-in prescaler. 이 PWM (Pulse-Width Modulation) It can be used as square waveform signal required for user application such as LED, motor, inverter, etc. through PWM related register setting.

Main features of PWM (Pulse-Width Modulation)

- PWM (Pulse-Width Modulation) output with 16-bit resolution
- PWM output 8 channels
- PWM invert signal output channels
  - 100-pin (PWM0~PWM7)
  - 80pin (PWM1~PWM7)
- PWM duty setting function by setting counter and period register.
- PWM input clocks
  - PCLK
  - 4 steps (1/2, 1/4, 1/8, 1/16) prescaler
- Integrated 1-unit 8-bit prescaler for PWM input clock division
- In multichannel PWM operation, timing synchronization based on the PWM signal with the shortest cycle

9.2 Block Diagram

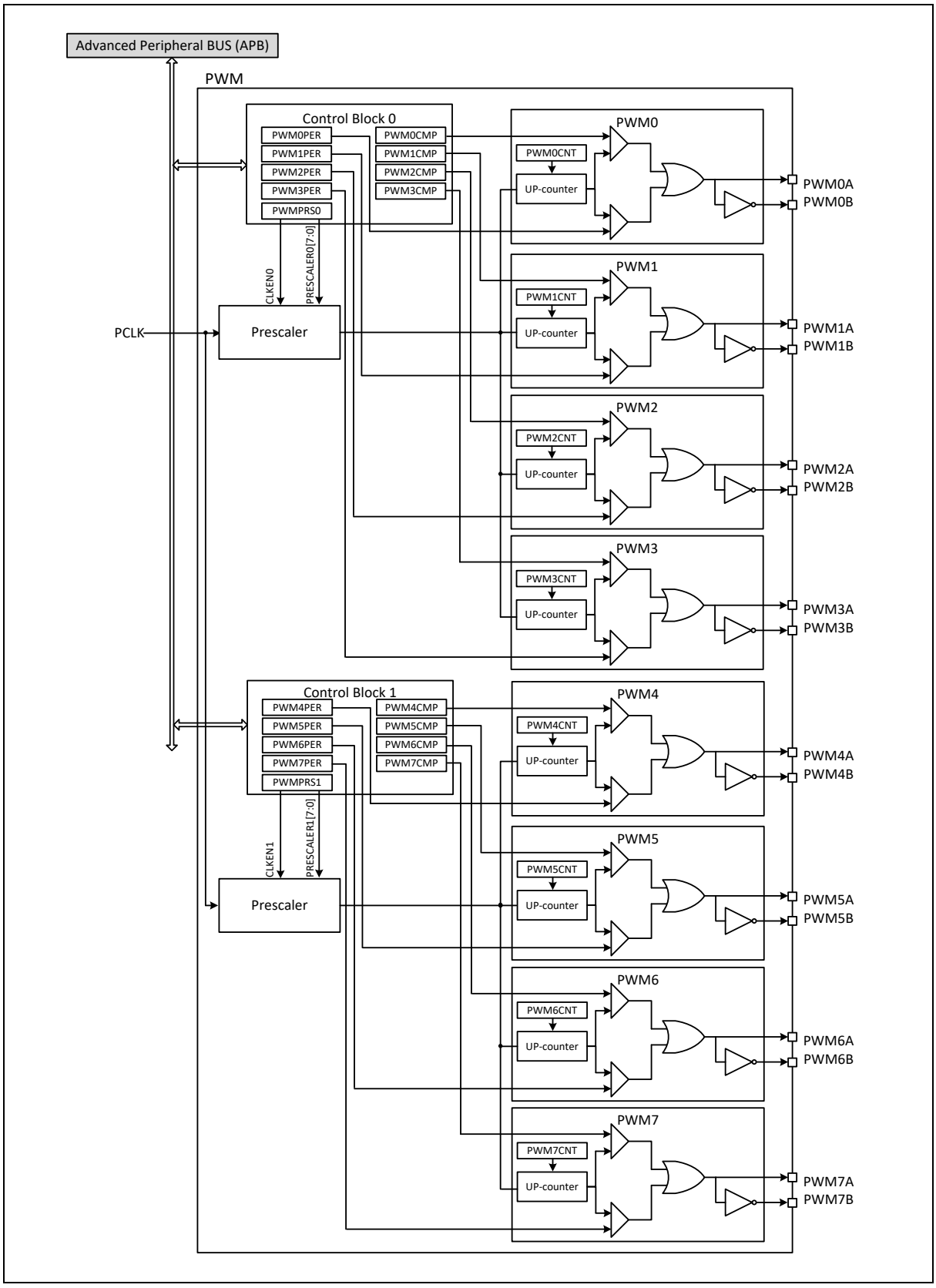


Figure 9.1. The block diagram of PWM

9.3 Pin configuration

PWM (Pulse-Width Modulation) pin configuration of A33G52x series is as follows. The 80-pin and 100-pin products are each provided with an inverted output signal mode for PWM0-7.

Table 9.2. The external pins of PWM

Pin Name	Type	Description	Support by package		
			A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G526MM A33G526ML A33G524MM A33G524ML	A33G527VQ A33G527VL A33G526VQ A33G526VQ
PWM0A	O	Output of PWM0	O	O	O
PWM0B	O	Reverse output of PWM0	-	-	O
PWM1A	O	Output of PWM1	O	O	O
PWM1B	O	Reverse output of PWM1	-	O	O
PWM2A	O	Output of PWM2	O	O	O
PWM2B	O	Reverse output of PWM2	-	O	O
PWM3A	O	Output of PWM3	O	O	O
PWM3B	O	Reverse output of PWM3	-	O	O
PWM4A	O	Output of PWM4	O	O	O
PWM4B	O	Reverse output of PWM4	-	O	O
PWM5A	O	Output of PWM5	O	O	O
PWM5B	O	Reverse output of PWM5	-	O	O
PWM6A	O	Output of PWM6	-	O	O
PWM6B	O	Reverse output of PWM6	O	O	O
PWM7A	O	Output of PWM7	-	O	O
PWM7B	O	Reverse output of PWM7	O	O	O

9.4 Functional Description

9.4.1 Setting the input clock of PWM (Pulse-Width Modulation) Generator

The source clock for PWM (Pulse-Width Modulation) is determined by the system peripheral clock and the prescaler in the PWM_PRSn register or the prescaler in the PWMn_CTRL register. PWM (Pulse-Width Modulation) source clock can be obtained by the formula below.

$$\mathbf{PWMCLKn} = \frac{\boldsymbol{PCLK}}{\boldsymbol{PRESCALER}\mathbf{n} + \mathbf{1}}$$

The first way to get the PWM source clock is to obtain the PWM input clock PWMCLKn by activating PWMCLKn with the PWMPRSn [15] bits in the PWM_PRSn register and setting the PRESCALERn [7: 0] value to the system peripheral input clock. PWMCLK0 is the clock applied to PWM0-3 group, and PWMCLK1 is the clock applied to PWM4-7 group.
PWMCLKn applied to each PWMn can be set to the input clock of each PWM (Pulse-Width Modulation) channel by dividing 2, 4, 8, or 16 by the value set in CKSEL [7: 5] through the clock divider.

9.4.2 Setting the period and PWM output signal

Each PWMn channel has a PWMn_PER register for setting the PWM frequency.
PWM period can be obtained by below fomula with 16-bit width value.
The PWM (Pulse-Width Modulation) period can be obtained by applying the following formula with 16-bit PWMn_PER value and the PWM input clock.

$$\textbf{PWM Period} = \frac{\boldsymbol{PWMCLK}}{\boldsymbol{PERIOD} + \mathbf{1}}$$

Each PWMn channel can set PWM duty as well as period. PWM duty can be set to a value in the range of 0 ~ PERIOD in PWMn_CMP[15:0].
The default output of PWMnA is 'L', and the PWMnA output changes to 'H' when the PWMn_CNT register value reaches the PWMn_CMP value.
You can also invert the starting output level of PWMnA by entering a value in the INVA bit in the PWMn_CTRL register. If you enter 0 as the default value, the start output value will be Low. If you input 1, High will be output. PWMnB is output when the PWMnA waveform is inverted.

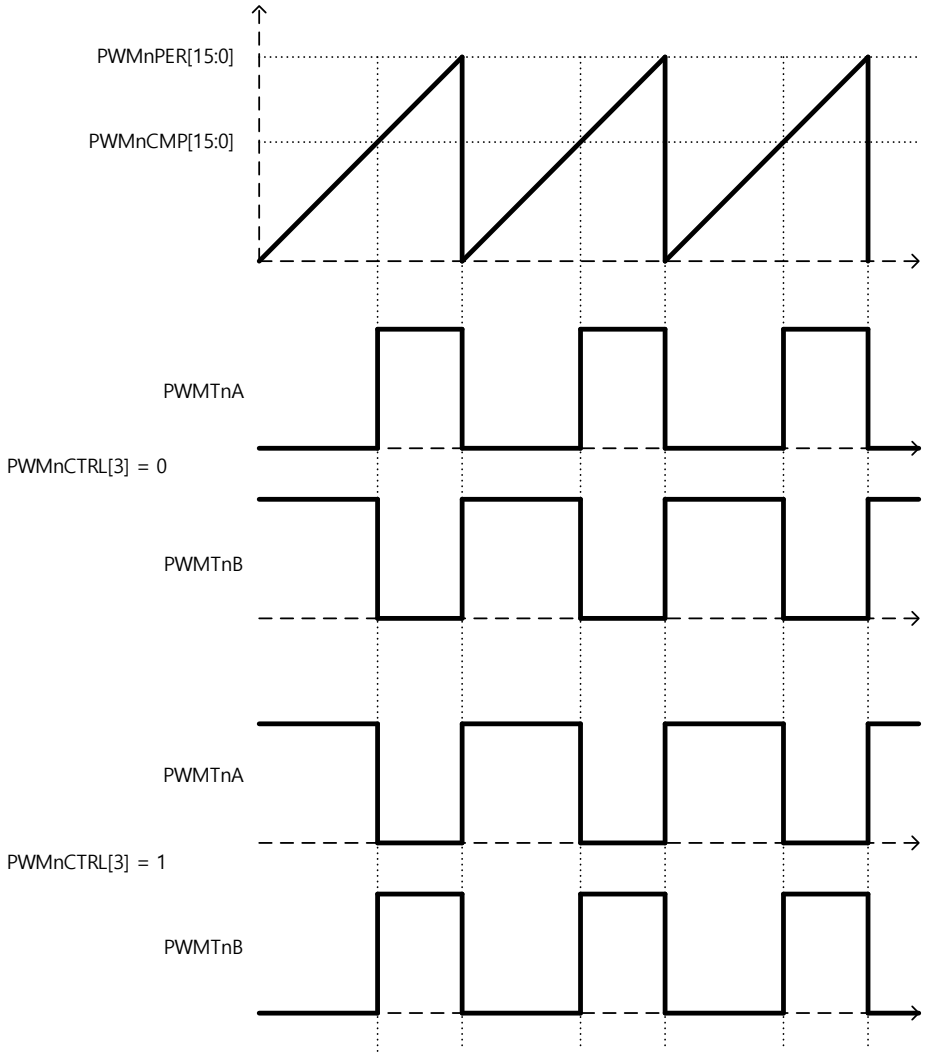


Figure 9.2. The block diagram of PWM output timing

After each of the above functions are set, if 1 is input to the STRT bit in the PWMn_CTRL register, PWM is output. If 0 is input, PWM output is stopped.

9.4.3 PWM (Pulse-Width Modulation) Interrupts

Each of PWMn channels can be configured periodic interrupt. If the PRIE bit in the PWMn_CTRL register is set to '1', the PWM periodic interrupt is enabled. If the PRIE bit in the PWMn_CTRL register is set to '0', the periodic interrupt is disabled. Interrupt vector is supported for each channel. If an interrupt occurs in each PWMn channel, it is possible to check whether an interrupt is generated by reading the PRF bit in the PWMn_CTRL register. If a periodic interrupt occurs, the PRF bit must be cleared by writing 1 to it.

9.4.4 Synchronization of PWM channels

The PWM (Pulse-Width Modulation) block has a function to set synchronization between channels. if the synchronization function is enabled through the control registers of each channel in the PWM0-3 group synchronizes the counting of the active PWM channels. The timing of the synchronized PWM channels is set based on the peirod of the shortest PWM channel. Similarly, PWM4-7 groups operate in the same way as PWM0-3 groups. However, the synchronization function of PWM0-3 group and PWM4-7 group is independent and does not affect the operation between PWM0-3 and PWM4 ~ 7 groups.

CHAPTER 10. I²C Interface

Table 10.1. Operation Summary

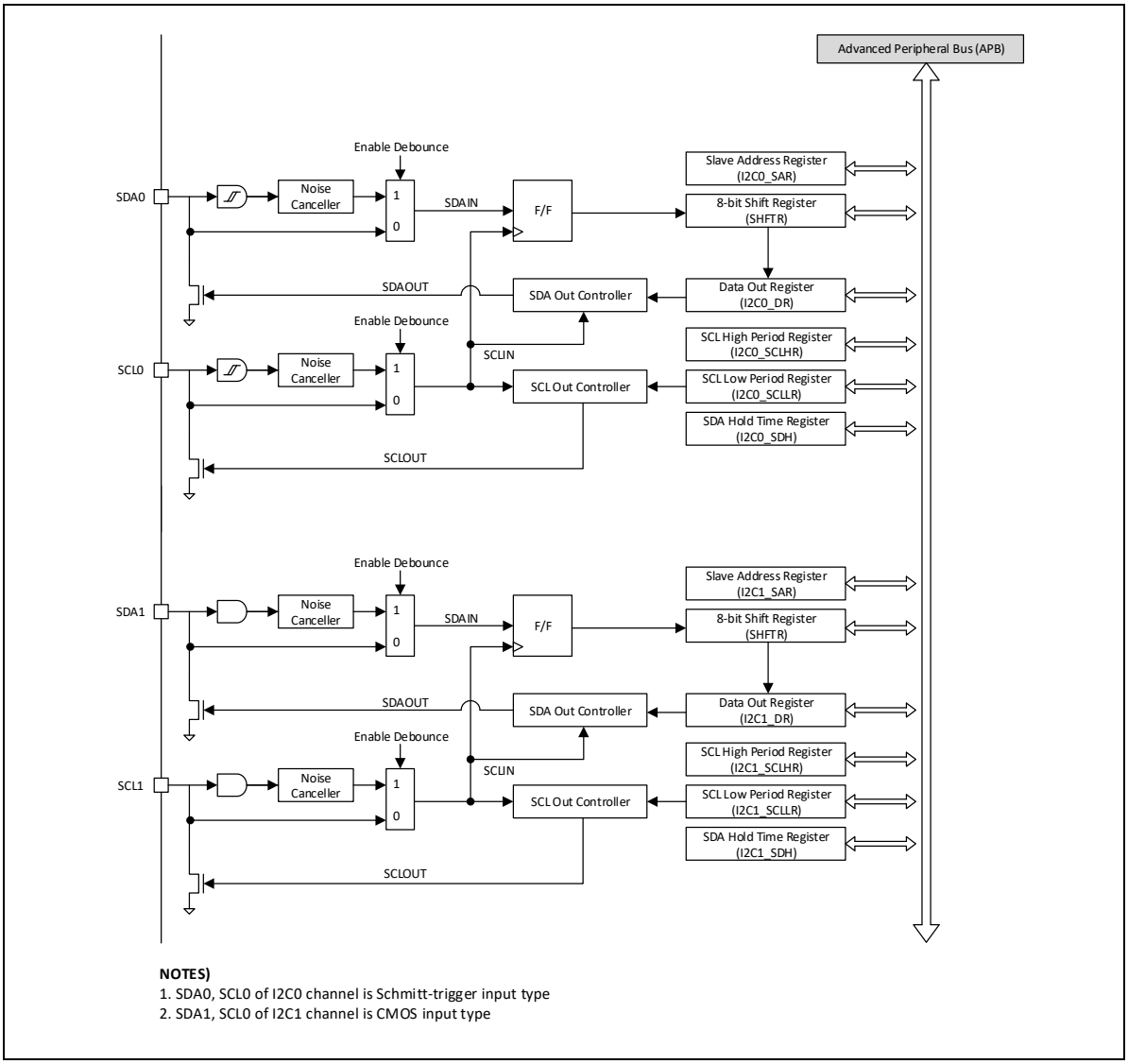
Item	Pin Name	Remark
Clock usage	PCLK	Transper rate
Reset Source	Set by PMU_PER Software reset function	 I2Cn_CR
Reset Generation	None	
Interrupt Generation	GCALL, End of transmit, End of receive ACK/STOP reception, SLAVE selected (I2C0(36), I2C1(37))	I2Cn_SR
Interrupt Clear Method	Write 0xFF to the I2Cn_SR	I2Cn_SR

10.1 Overview

The I2C interface on the A33G52x meets the standard I2C (Inter Integrated Circuit) communication interface and is used for serial communication with internal and external devices of the same serial bus format. It supports both master and slave mode with 2 channels and can send or receive data per byte-based interrupt or polling method. I2C (Inter Integrated Circuit) blocks are used to communicate with various peripherals with the same bus format. A33G52x To use the I2C (Inter Integrated Circuit) function, it is recommended to set SCL and SDA as open drain and then connect the external pull-up resistor and use it as 'HIGH' state.

Main features of I2C (Inter Integrated Circuit) Interrface

- Standard I2C (Inter Integrated Circuit) interface communication
  - 2 channels support
- Master and slave operation mode setting
- Single master – multi-slave operation support
  - 1: 1 and N: N (up to 1008) slave device support
- The setting function of i2c transmission rate
  - Up to 400kHz communication speed setting support
- I2C (Inter Integrated Circuit) interrupt
- 7-bit slave addressing
- Delay setting for SCL High or Low waveforms
- time setting function for SDA previous value data



NOTES)
1. SDA0, SCL0 of I2C0 channel is Schmitt-trigger input type
2. SDA1, SCL0 of I2C1 channel is CMOS input type

Figure 10.1. The block diagram of I2C Interface

10.2 Pin Configuration

The I2C (Inter Integrated Circuit) has two signals: SCL and SDA. For communication, these signals must be set to the internal or external pull-up state of the open-drain. However, if only internal pull-up is connected without external pull-up, the communication speed may be limited due to high resistance value.

Table 10.2. The List of I²C Pins

Pin Name	Type	Description	Support by package		
			A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G526MM A33G526ML A33G524MM A33G524ML	A33G527VQ A33G527VL A33G526VQ A33G526VQ
SCL0	I/O	Serial Clock Signal (open-drain)	O	O	O
SDA0	I/O	Serial Data Signal (open-drain)	O	O	O
SCL1	I/O	Serial Clock Signal (open-drain)	O	O	O
SDA1	I/O	Serial Data Signal (open-drain)	O	O	O

Notes)

1. SDA0, SCL0 Schmitt-trigger input type
2. SDA1, SCLK1 CMOS input Type

10.3 Functional Description : I2C Protocol

10.3.1 I²C (Inter Integrated Circuit) Bit Transfer

The data on the SDA line must be stable during HIGH period of the clock, SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

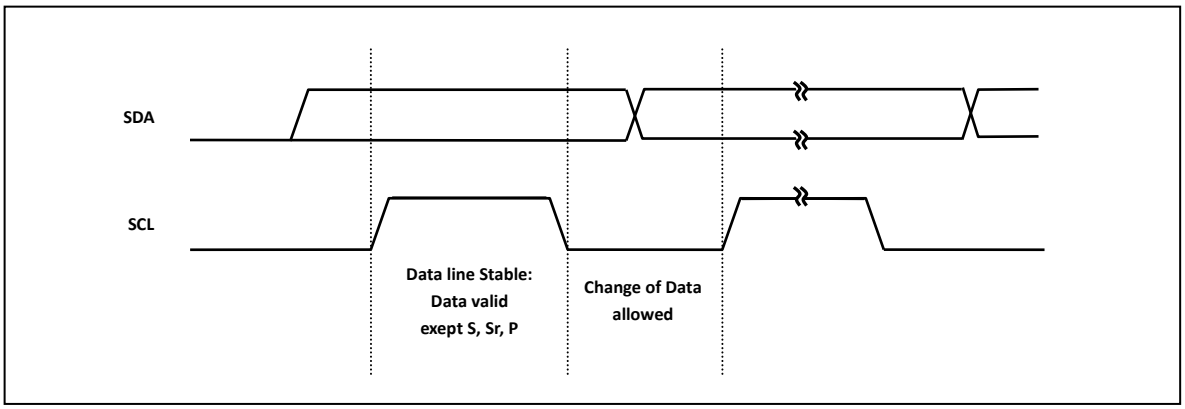


Figure 10.2. Bit Transfer on the I2C Interface Bus

10.3.2 START / Repeated START / STOP

One master device can send a START (S) signal to another device to communicate. When communication is complete, the master sends a STOP (P) signal to release the bus in use and make it available to other devices.

The conditions for determining START (S) and STOP (P) in I2C communication are as follows.
START (S) condition is that SDA line signal changes from 'H' to 'L' during SCL level is 'H'.
STOP (P) condition is that SDA line signal changes from 'L' to 'H' during SCL level is 'H'.

The START(S) and STOP(P) condition can be generated by the master at any time. After START (S) signal, the staus of the bus is busy. When the master sends a START (S) signal, the bus goes into the BUSY state. When the STOP signal is transmitted by the master, the bus is released. Then the state between START (S) and STOP (P) becomes BUSY.
For example, when the bus is between START and STOP, the bus remains in the BUSY state. If the condition is repeated START (Sr) instead of STOP, the state of the bus will be BUSY. START (S) and repeat START (Sr) are functionally the same.
START and STOP conditions are always generated by the master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

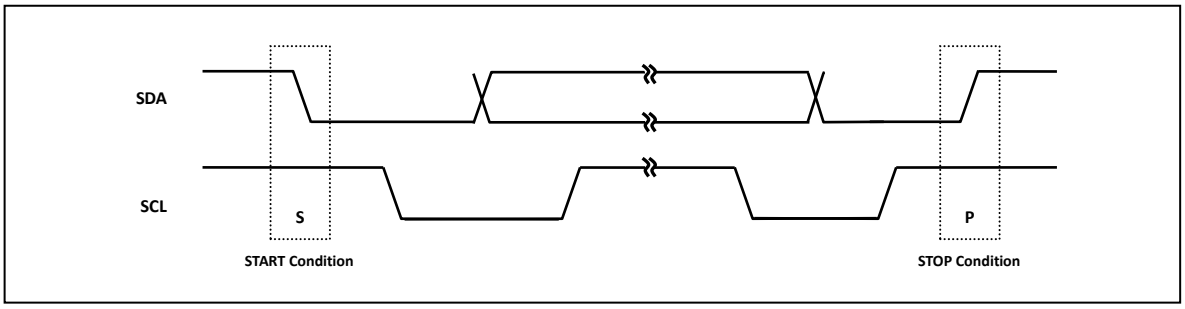


Figure 10.3. START and STOP Condition

10.3.3 Data Transfer

All data sent to the SDA line is configured in 8-bit units, and the number of bytes transferred is unlimited. SDA line transmits ACK bits after every data transmission. The data is transferred with the most significant bit (MSB) first If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

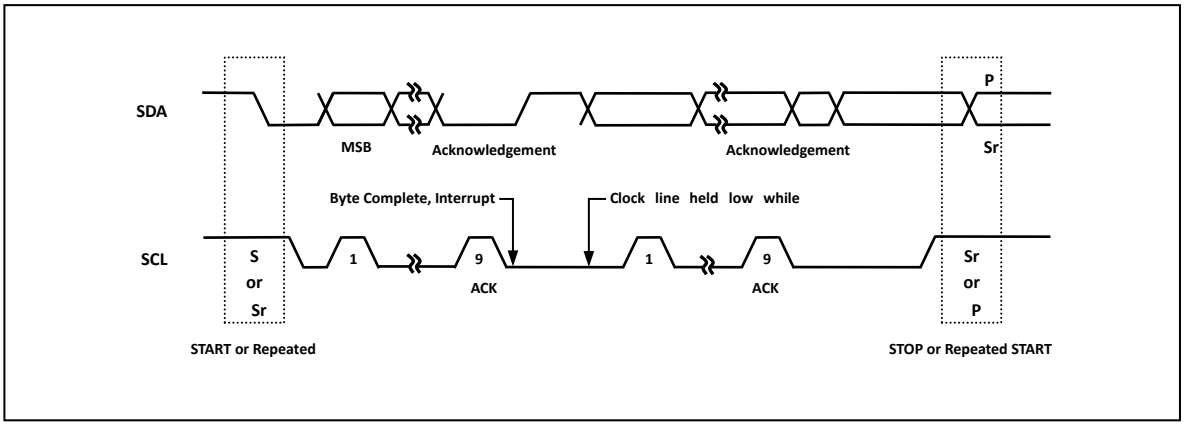


Figure 10.4. Data Transfer on the I²C bus

10.3.4 Acknowledge (ACK)

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

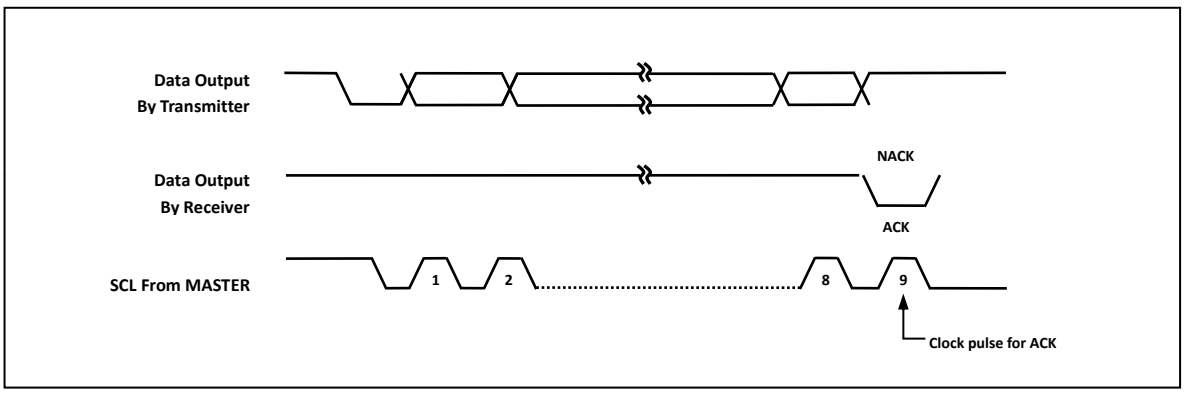


Figure 10.5. Acknowledge on the I²C Bus

10.3.5 Synchronization / Arbitration

Clock synchronization is performed using the wired-AND connection of I2C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and it will hold the SCL line in that state until the clock HIGH state is reached. However the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. In this way, a synchronized SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.
A master may start a transfer only if the bus is free. Two or more masters may generate a START condition. Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output state because the level on the bus doesn't correspond to its own level. Arbitration continues for many bits until a winning master gets the ownership of I2C bus. Its first stage is comparison of the address bits.

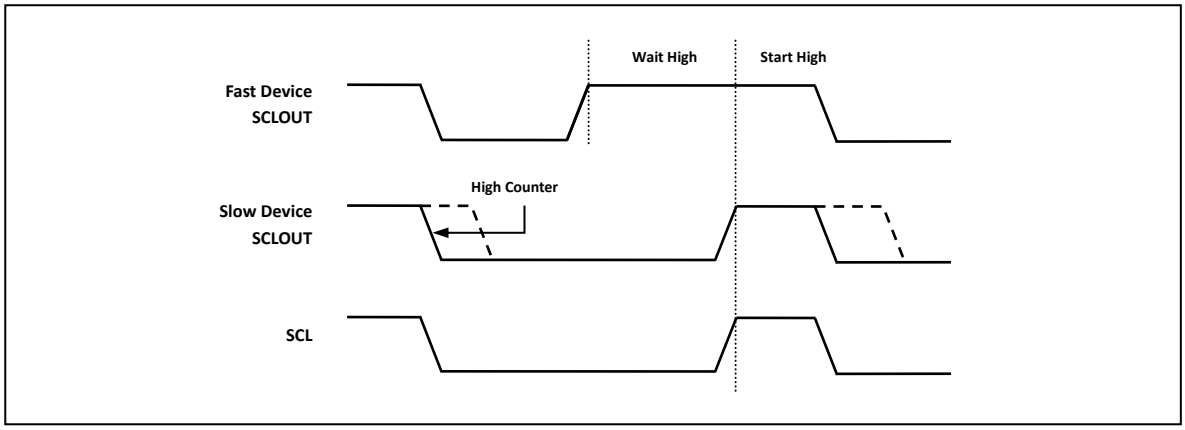


Figure 10.6. I²C clock synchronization during arbitration procedure

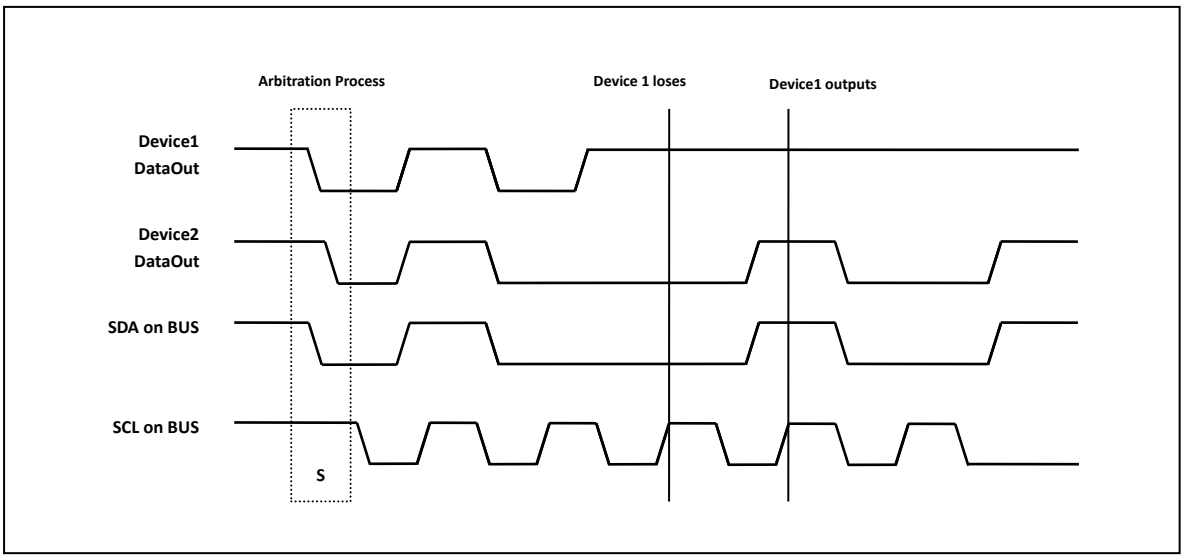


Figure 10.7. Arbitration precedure of two I²C masters

10.3.6 Debounce function for I2C

I2C is one of the standard serial communication protocols, which is widely used in industry. The I2C uses 2 bus lines such as Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data.
I2C features the followings (n = 0 and 1):

Table 10.3. The List of the I2C Channel

Channel	Pin Name		Description
I2C0	PB14	SCL0	Output or Schmitt-trigger input
	PB15	SDA0	Output or Schmitt-trigger input
I2C1	PD14	SCL1	Output or CMOS input
	PD15	SDA1	Output or CMOS input

For the input pins of SCL1, SDA1 CMOS type, it is recommended to debounce. The debounce settings of I2C1 channel is introduced in figure 10.8.
Each of SCD1 pin and SCA1 pin can use the debounce to prevent reset malfunction which is due to noise. This is configured in registers PD_DER (0x4000_026C) and the PD_DPR (0x4000_027C), and must be applied to the pin ports of SCL1 and SDA1. First, a user needs to set the debounce clock (prescaler) and enable the debounce filter by configuring the PD_DPR. When the filter is enabled, input signals in less than 4 clocks is considered as noise and ignored.

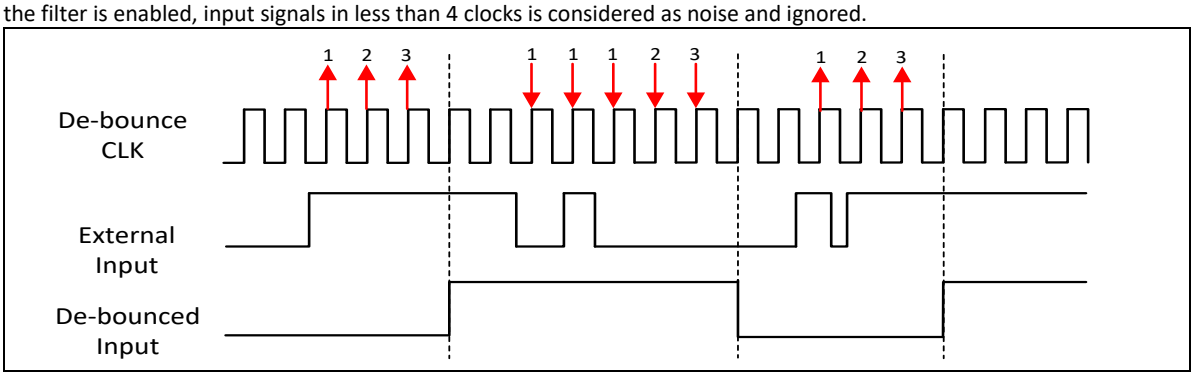


Figure 10.8. I²C clock synchronization during arbitration procedure

Assuming that input time of the PD_DPR is 16us and PCLK = 20MHz, the debounce filtering time is calculated as shown below (f = debounce clock frequency, T = debounce clock period).

$4 \times T \geq 16\text{us}$

$T \geq 4us$

$\frac{1}{f} \geq 4us$

$\text{f} = \frac{PCLK}{2^x} \leq \frac{1}{4us} = \frac{1}{4}us$

$2^x \geq \frac{PCLK}{\frac{1}{4}MHz} = \frac{20MHz}{\frac{1}{4}MHz} = 80$

$\text{x} \geq 7$

For Example,

$f = \frac{PCLK}{2^7} = \frac{20MHz}{2^7} = \frac{20}{128}us$

$T = \frac{128}{20}us$

$Filtering\ time = 4T = 4 \times \frac{128}{20}us = 25.6$

After the calculation, the result is '7'. Add the value to the PD_DPR to get 25.6us as the filtering time. For detailed information and relationship between the PD_DPR, PCLK, and debounce clock, please refer to spec. 4.5.15.
Example code shown below can be added during initialization process to complete software debounce processing for a PD pin.

```
PD_DPR <DPR>   = "7"
PD_DER <P14>   = "1"
```

CHAPTER 11. UART (Universal Asynchronous Receiver / Transmitter)

Table 11.1. Operation Summary

Item	Description	Remark
Clock usage	PCLK	Transfer rate
Reset Source	Set by PMU_PER	
Reset Generation	None	
Interrupt Generation	Rx data, Tx data Line status Error (UART0(38),UART1(39),UART2(40),UART3(50))	UARTn_IER, UARTn_IIR
Interrupt Clear Method	Line status interrupt: read UARTn_LSR Rx interrupt: read UARTn_RBR Tx interrupt: read UARTn_IIR or write to UARTn_THR	UARTn_IIR, UARTn_LSR, UARTn_RBR, UARTn_THR

11.1 Overveiw

The A33G52x has 4 channels of UART (Universal Asynchronous Receiver / Transmitter) compatible with 16C550/16C450. Among these, UART0 and UART1 channels are 16550 with FIFO type, and UART2 and UART3 channels are 16450 with double buffer type. All UART channels operate in the same data mode (no FIFO mode) as 16450 when they are initialized. After initialization, FIFO mode setting is possible only for UART0 and UART1. In the FIFO mode, up to 16 bytes of data can be stored in the transmit/receive FIFO.
The built-in UART (Universal Asynchronous Receiver / Transmitter) can read out the data of the set configuration and the received data or the current UART status. UART status information can be checked not only for the type and conditions of transmission and reception by UART (Universal Asynchronous Receiver / Transmitter) but also for errors (parity, overrun, framing, break interrupt) that occur when data is received.
Each Universal Asynchronous Receiver / Transmitter (UART) has a programmable baud rate generator to divide the prescaled clock into values from 1 to 65535. This divided clock is again divided into 16 clocks to create a clock that drives the UART's internal transmit / receive blocks.
Communication with the UART can also be controlled by an interrupt using a user-programmable interrupt function. However, the general purpose 16450/16550 has a modem control signal and associated registers, but not the A33G52x.

Main features of UART (Universal Asynchronous Receiver / Transmitter)

- 16550/16450 compatible asynchronous serial communication port 4 channels
  - 16550 compatible device with FIFO type 2 channels: UART0, UART1
  - 16450 compatible devices in double buffer type 2 channels: UART2, UART3
- Serial interface settings
  - 5-bit, 6-bit, 7-bit or 8-bit data
  - Even, odd, or no-parity bit generation and detection
  - bit, 1.5-bit or 2-stop bit generation and detection
- Add/Remove standard asynchronous communication bits (start, stop, and parity)
- Independently configurable transmit, receive, line status, interrupt
- 16-bit Programmable baud-rate generator
- Built-in decimal point divider to improve baud rate accuracy.
- Single and multi sampling function for received data
- Support boot program using UART0 channel when entering boot mode
- Status check function through UART interrupt ID register and line status register.
  - Stop bit error detection
  - Display information about current line status
  - Line break generation and detection
  - Receive error diagnosis function
- Loop-back control
- Priority-based interrupt system

11.2 Block Diagram

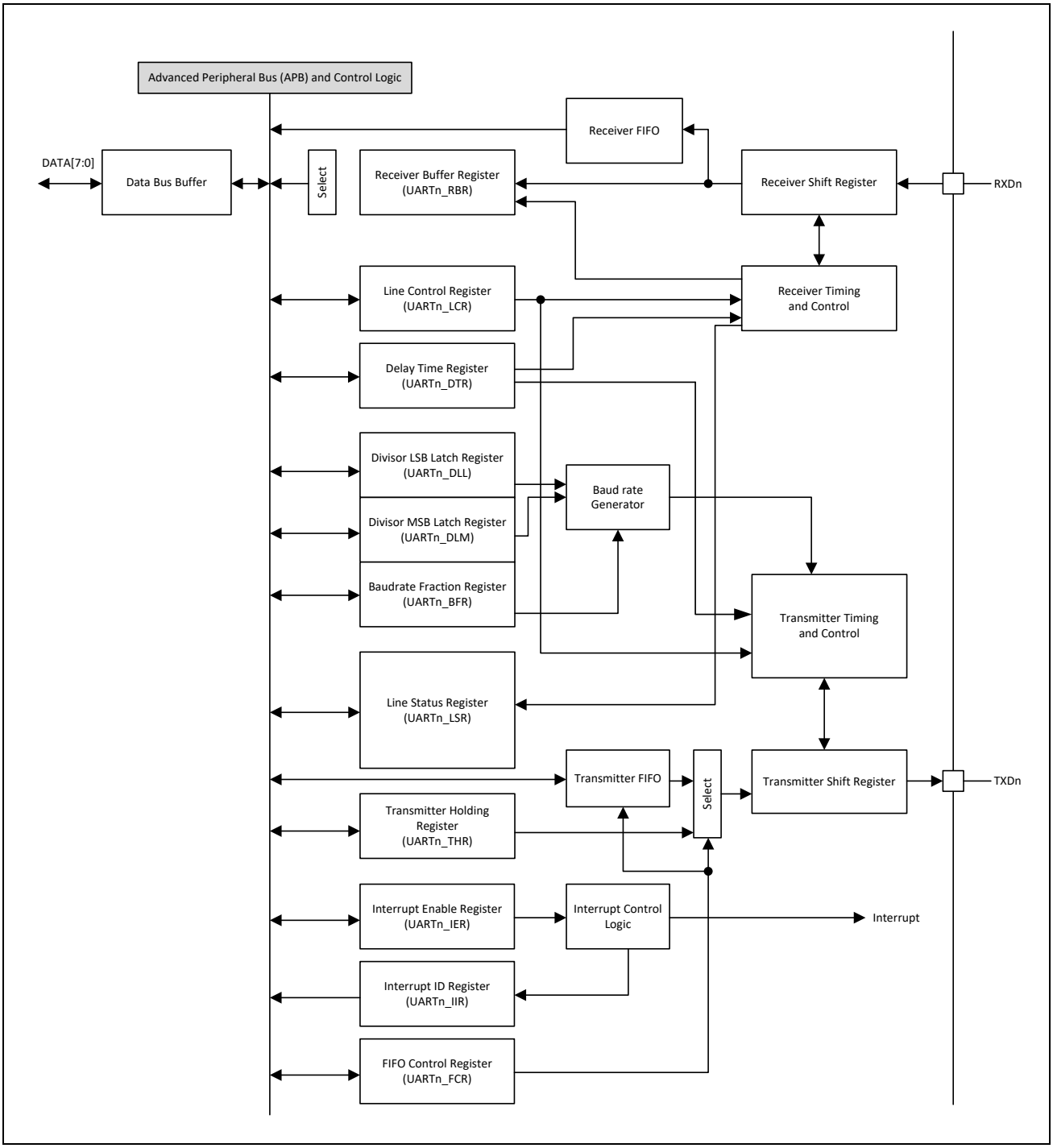


Figure 11.1. The block diagram of UART

11.3 Pin Configuration

Table 11.2. The List of UART Pins

Pin Name	Type	Description	Support by package		
			A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G526MM A33G526ML A33G524MM A33G524ML	A33G527VQ A33G527VL A33G526VQ A33G526VQ
TXD0	O	Serial output of UART0	O	O	O
RXD0	I	Serial input of UART0	O	O	O
TXD1	O	Serial output of UART1	O	O	O
RXD1	I	Serial input of UART1	O	O	O
TXD2	O	Serial output of UART2	O	O	O
RXD2	I	Serial input of UART2	O	O	O
TXD3	O	Serial output of UART3	O	O	O
RXD3	I	Serial input of UART3	O	O	O

11.4 Functional Description

The A33G52x has a built-in UART that supports single-sampling and multisampling modes when the start bit or data bit is detected by the UARTn_DTR <SMS> and UARTn_DTR <DMS> bits. The user can select the sampling method according to the operating environment. This sampling method supports noise-resistant UART communication environment.
In addition, in order to reduce the interference error caused by noise introduced into the received data of the UART, it is necessary to activate the Debounce function of the PMC (Port Map Control).

11.4.1 Receiver Single Sampling

On detecting a falling edge of input signal, UART recognizes the falling edge as a START bit signal. From this edge, every bits of a character transmission are sampled by 16-multiple clock signal.
If the SMS or DMS bit is '0' of UARTnDTR reigster, UART receiver will determine the bit value by the signal value on the seventh clock edge from a bit window.

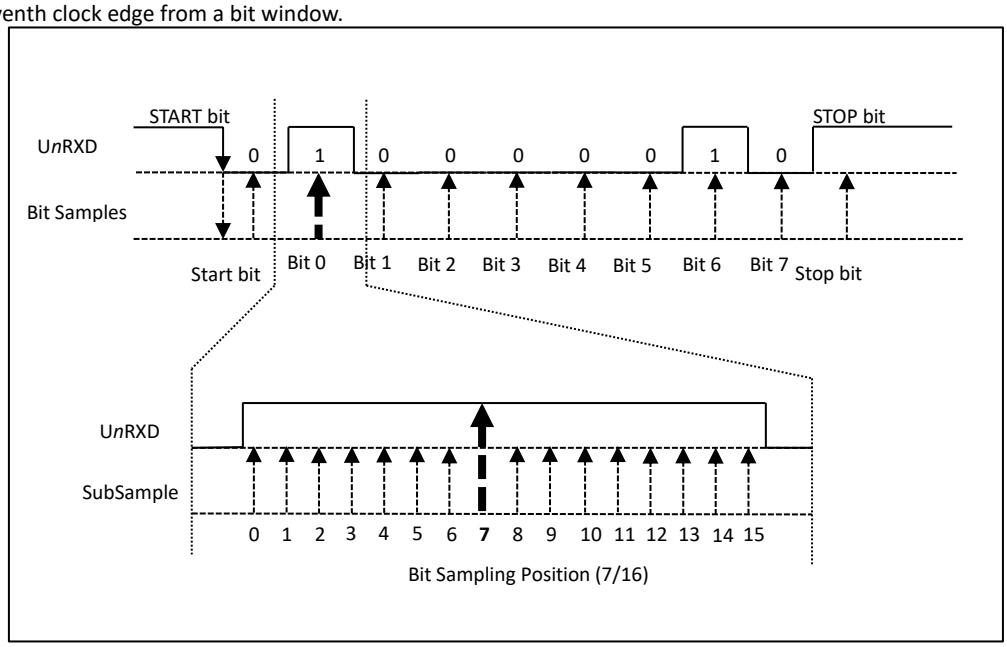


Figure 11.2. Sampling Method in 8-bit data receiving

11.4.2 Multi Sampling

If the SMS or DTS is '1', most occurrence value of signals on 7th, 8th, 9th clocks will be the bit value.

Noise error

Over-sampling techniques are used (except in synchronous mode) for data recovery by discriminating between valid incoming data and noise.

Figure 283. Data sampling for noise detection

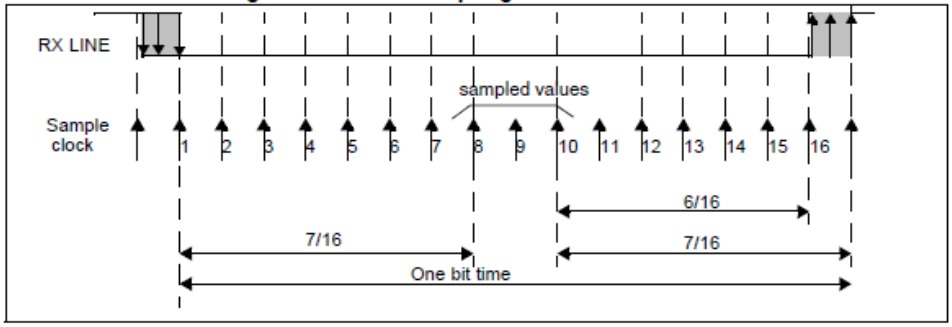


Figure 11.3. The multi-sampling timimng of start bit and Rx data bit

11.4.3 Transmit data format

The transmitter has a data transmission function. The start bit, the data bit, the optional parity bit, and the stop bit are shifted continuously, and the least significant bit is moved first.
The number of data bits is selected in the DLEN [1: 0] field of the UARTn_LCR register.
The parity bit is set according to the PARITY and PEN bits filed in the UARTn_LCR register. For example, if the parity type is even, then the parity bit is determined by the bit sum of all the data bits. For odd parity, the parity bit is the opposite sum for all data bits. The number of stop bits is selected within the fileized STOPBIT in the UARTn_LCR register.
An example of the transmit data format is shown below.

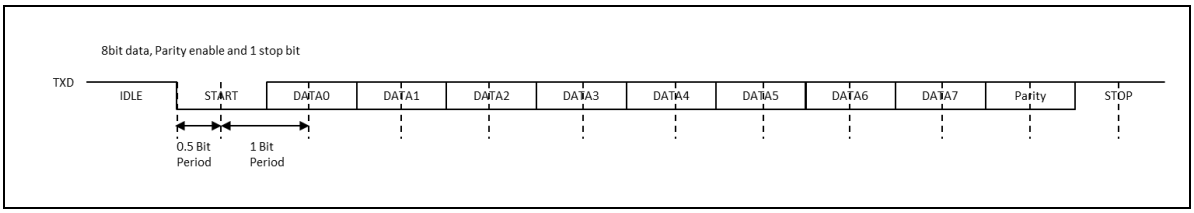


Figure 11.4. The example of transmit data format

11.4.4 Transmit Interrupt

The transfer operation produces some kind of interrupt flag. When the transmitter holding the register is empty, the THRE interrupt flag is set. When the transmitter shifter register is empty, the TXE interrupt flag is set. The user can choose which interrupt timing is best for the application.

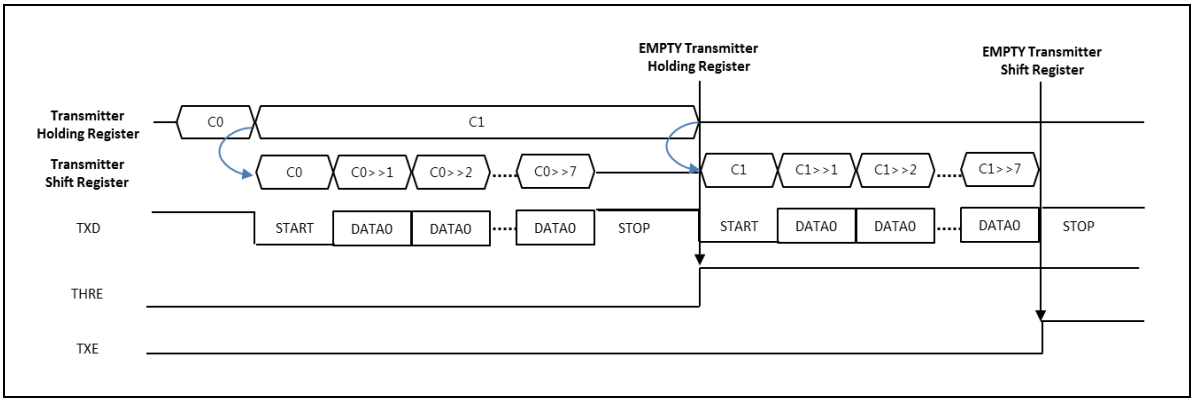


Figure 11.5. The diagram of transmit interrupt timing

11.4.5 Start Bit Detection

In the UART receiver block, there are two types of determination strategy of START bit.. One is by single-clock sampling and the other is by multi-clock sampling.
The single-clock sampling feature is the general sampling method, this feature acquire start bit value in the center of the bit period.
The multi-clock sampling feature has noise-rejection function for accurate communication against line noise. The timing diagrams of the single sampling and multi sampling features are shown as followings.

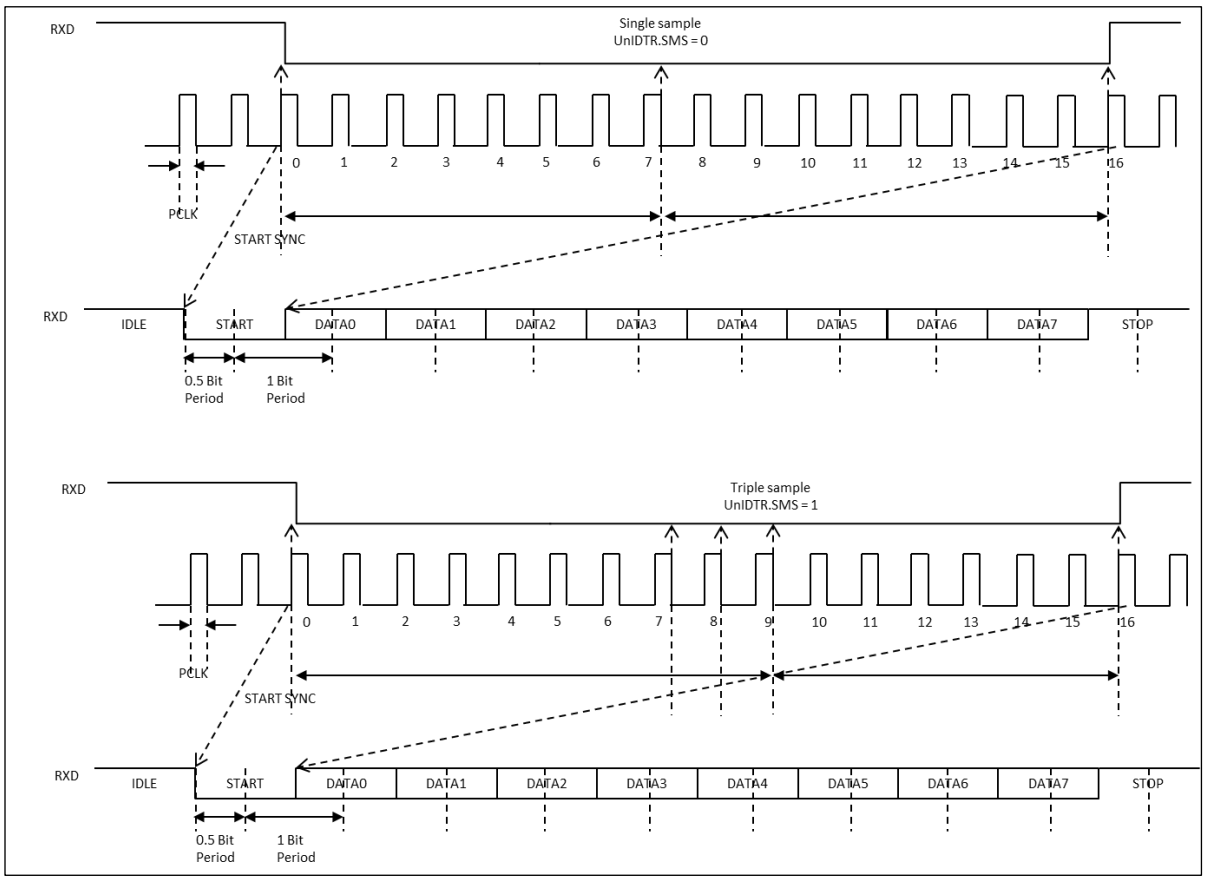


Figure 11.6. The timing diagram of the start bit detection in single sampling mode and multi sampling mode.

11.4.6 Data Sampling Strategy

In the receiver block, there are synchronous logics inside to prevent abnormal noise on the RxD input signal line. The start bit and data bit sampling type can be configured to any mode of single sampling or multi sampling. The start bit detection strategy can be selected by the SMS bit on UARTn_DTR register, the data bit detection strategy can be selected by the DMS bit on UARTn_DTR register.

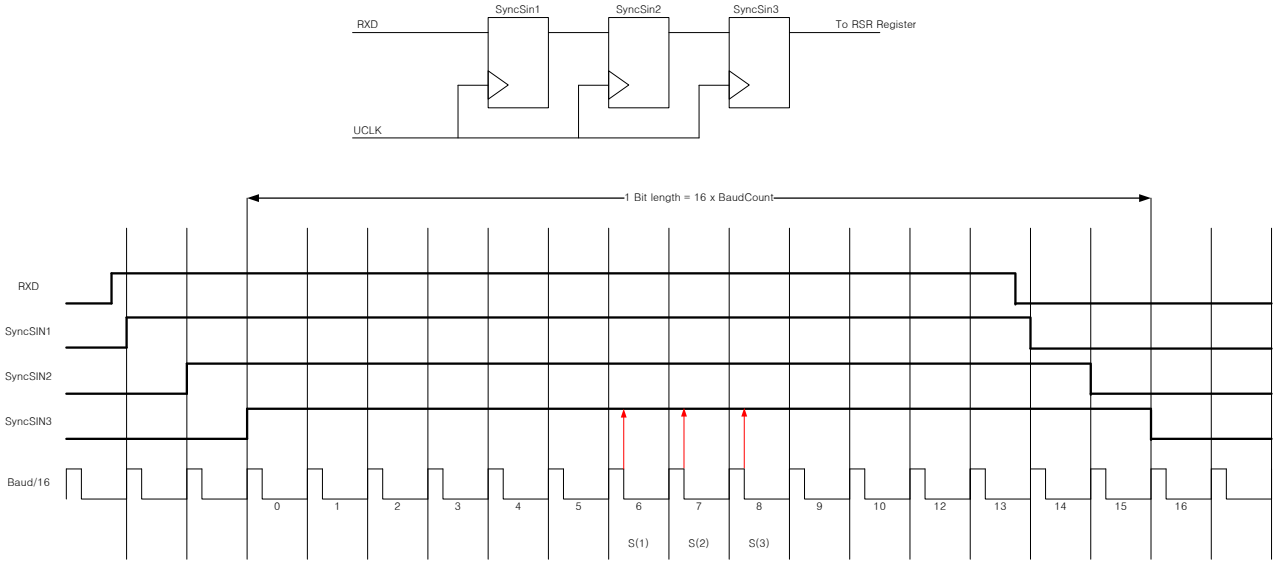


Figure 11.7. The timing diagram of data smapling

The figure 11.7 shows the timing diagram of a data sampling.
If the DMS bit was selected, the multi-sampling feature is activated and a bit value is to be determined by most occurrence value of the time of S(1), S(2), S(3) from the 8th clock in a bit period.
If the DMS bit was not selected, the single-sampling feature is activated and a bit value is tobe determined only by the value at S(2) timing. The DMS bit does not affect start bit strategy, the SMS has same feature with DMS, it only affect start bit detection.

11.4.7 Inter-frame Delay Transmittion

According to configuration of the inter-frame delay, the transmitter will insert idle timing between a successive character transmission. The period of idle between inter-frame transmission will be configured by the WAITVAL field on DTR register. If the WAITVAL field of UARTn_DTR was '0', there is no time delay on the transmission. On the contrary if this field was selected as '1', the line status of inter-frame transmission of every characters is set to be 'H' state during the configured timing.

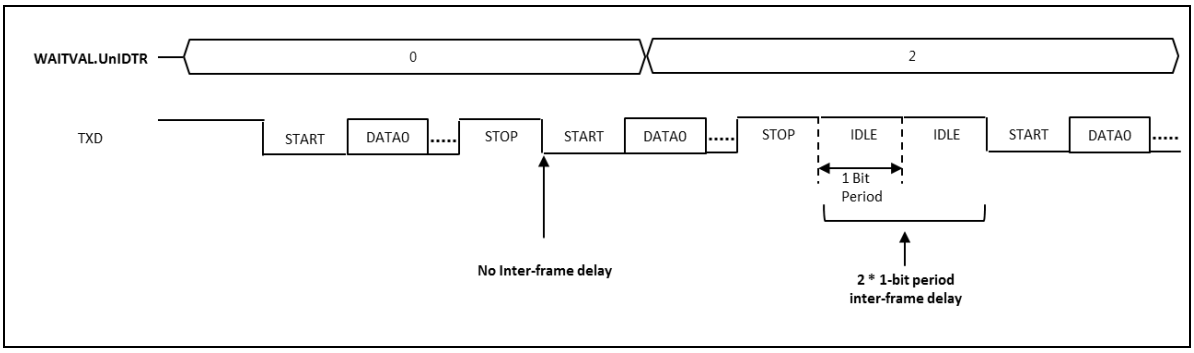


Figure 11.8. The timing diagram of inter-frame delay transmission

11.4.8 The Baud-rate Setting

Each channel of the UART has a programmable baud rate generator that can receive the PCLK clock and divide it by a divide value from 2 to 65535. (If dividing value is '1', it is the highest baud rate.). The output clock frequency of the baud rate generate is 16 x Baud rate. In order for UART communication to work properly, the UARTn_DLL and UARTn_DLM registers value must be written to appropriate values before UART operation.

The baud rate calculation formula is as follows:

$$\text{BDR (UARTn\_DLM: UARTn\_DLL)} = \frac{PCLK/2}{16 * baud\ rate}$$

Table 11.3. Divisor value for each baud rate (PCLK=37.5MHz)

PCLK=37.5 MHz (HCLK/2)		
Baud Rate	**Decimal Divisor Value**	**Error Rate (%)**
1200	976	0.06%
2400	488	0.06%
4800	244	0.06%
9600	122	0.06%
19200	61	0.06%
38400	30	1.70%
57600	20	1.70%
115200	10	1.70%

Table 11.4. Divisor value for each baud rate (PCLK=8MHz)

PCLK=8 MHz (HCLK/2)		
Baud Rate	**Decimal Divisor Value**	**Error Rate (%)**
1200	208	0.16%
2400	104	0.16%
4800	52	0.16%
9600	26	0.16%
19200	13	0.16%
38400	X	X
57600	X	X
115200	X	X

Table 11.7 shows the baud rate generator baud rate and transmit/receive error rate at each baud rate for PCLK = 37.5 MHz, and the error rate is minimized at baud rates below 19200 bps. The frequency of the input clock affects the accuracy of the baud rate. It is not recommended to use '0' as the division value.

CHAPTER 12. SPI (Serial Peripheral Interface)

Table 12.1. Operation Summary

Item	Description	Remark
Clock usage	PCLK	Transper rate
Reset Source	Set by PMU_PER	
Reset Generation	None	
Interrupt Generation	Tx Buffer Empty Rx Data Ready (SPI0(32), SPI1(33))	SPIn_SR
Interrupt Clear Method	Tx Buffer Empty: Write to SPn_TDR Rx Data Ready: Read from SPn_RDR	SPIn_TDR, SPIn_RDR

12.1 Overview

The A33G52x has two built-in Serial Peripheral Interface (SPI) channels. Serial Peripheral Interface (SPI) is serial communication synchronized by clock. It can support communication with multiple slaves in one master, and communication is done by selecting slave using SS line.
The A33G52x has two built-in Serial Peripheral Interface (SPI) channels. Serial Peripheral Interface (SPI) is serial communication synchronized by clock. It can support communication with multiple slaves in one master, and communication is done by selecting slave using SS line.
Serial Peripheral Interface (SPI) is a 3-wire or 4-wire synchronous transmission using four signal line like SS (Slave Select), SCK (SPI Clock), MOSI (Master-Out, Slave-Input), MISO (Master-Input, Slave-Output) and enables full-duplex communication. You can change the speed of the sending and receiving input clock. In addition, the transmit and receive buffers are configured in duplicate, allowing data to be read or written during transmission and reception.

Main Features of SPI (Serial Peripheral Interface)

- Master and Slave mode operation
- Full-duplex, 4-wired, 3-wired synchronous transmission
  - SS : Slave Select
  - SCLK : Serial Clock
  - MOSI : Maste- Output, Slave-Input
  - MISO : Master-Input, Slave-Output
- The control of SPI Clock Speed (SCK) and polarity
- Separated transmit and receive data register with 8,9,16,17-bit length
  - Selectable 8 bit, 9 bit, 16 bit, 17 bit SPI data size
- the transmission status check function
- Interrupt setting function by SS signal
- Loopback mode for internal verification
- Support boot program function using SPI0 channel when entering boot mode

12.2 Block Diagram

Below is a block diagram of the SPI (Serial Peripheral Interface).

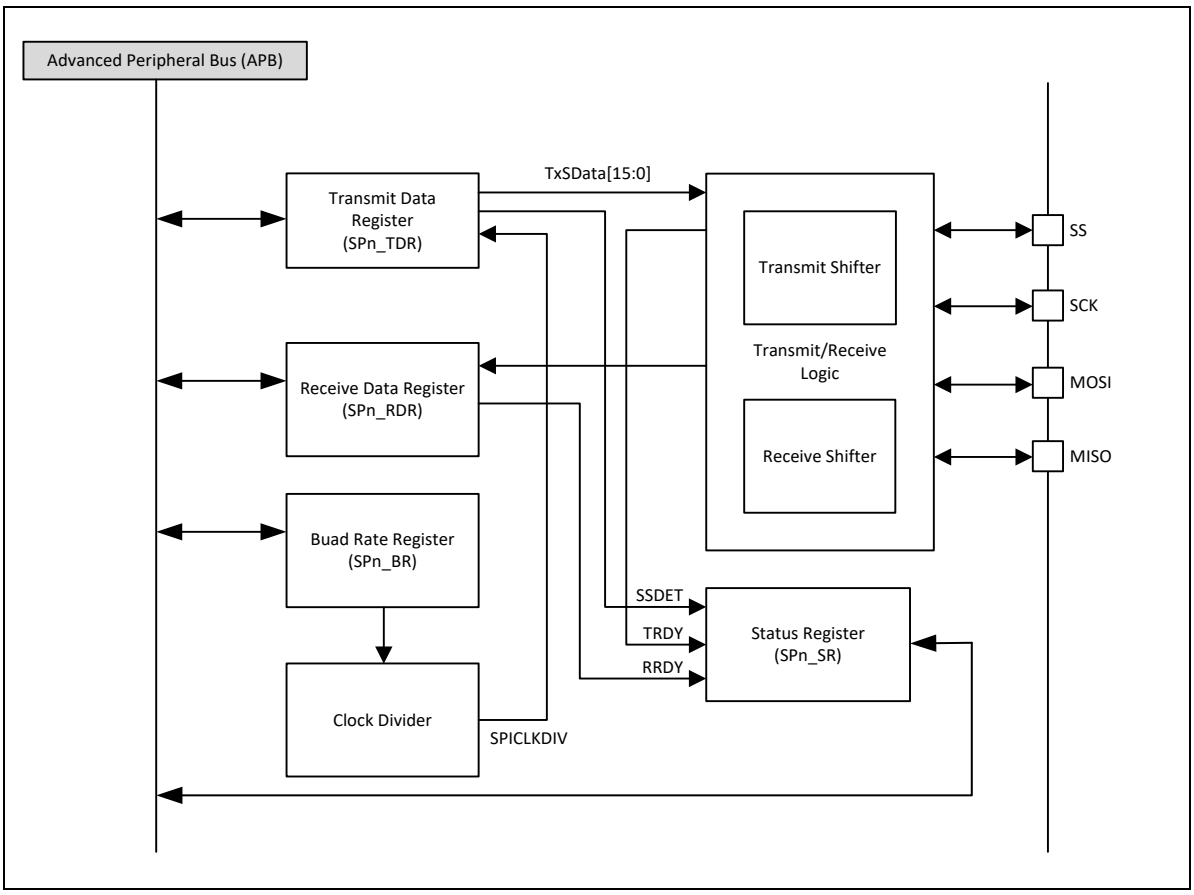


Figure 12.1. The block diagram of SPI

12.3 Pin Configuration

Table 12.2. The External Pins of SPIs

Pin Name	Type	Description	Support by package		
			A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G526MM A33G526ML A33G524MM A33G524ML	A33G527VQ A33G527VL A33G526VQ A33G526VQ
SS0	I/O	Slave Select signal of SPI0	O	O	O
SCK0	I/O	Serial Clock signal of SPI0	O	O	O
MOSI0	I/O	MOSI (Master-Out Slave-In) Data signal of SPI0	O	O	O
MISO0	I/O	MISO (Master-In Slave-Out) Data signal of SPI0	O	O	O
SS1	I/O	Slave Select signal of SPI1	O	O	O
SCK1	I/O	Serial Clock signal of SPI1	O	O	O
MOSI1	I/O	MOSI (Master-Out Slave-In) Data signal of SPI1	O	O	O
MISO1	I/O	MISO (Master-In Slave-Out) Data signal of SPI1	O	O	O

12.4 Functional Description

12.4.1 SPI Bus Timing

The sender and receiver of the Serial Peripheral Interface (SPI) share the same clock but are independent of each other. Full duplex transmission and reception is therefore possible. The transmitting and receiving ends have a double buffer structure, so that during the reception of the subsequent data, the RDR data received before is read or the subsequent data is written to the TDR while the data is being transmitted, so that a back-to-back transfer is possible.

The operation timing according to the CPHA bit and CPOL bit of the SPI (Serial Peripheral Interface) control register SPIn_CR is as follows.

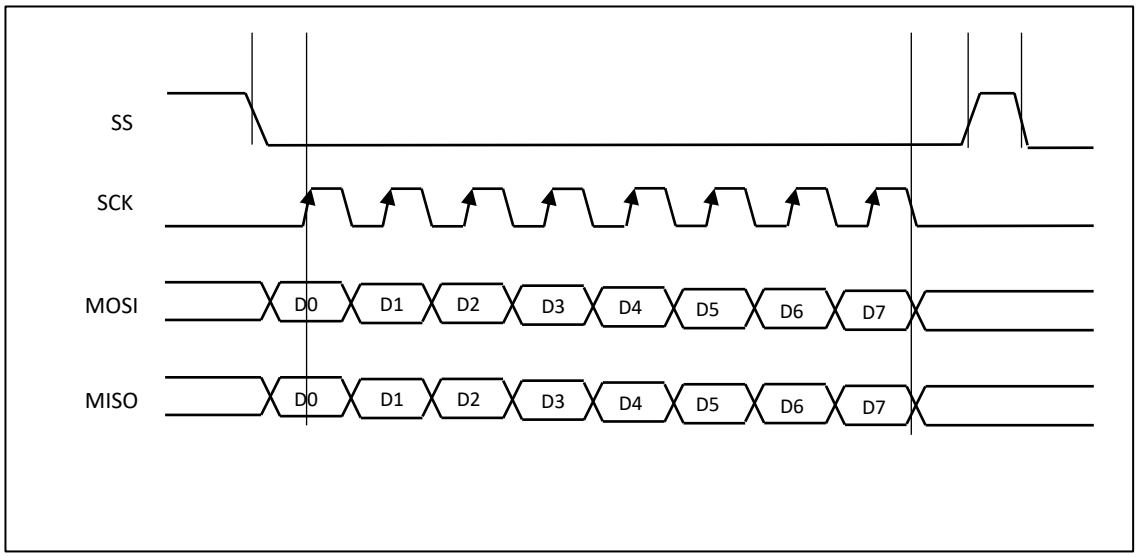


Figure 12.2. SPI Timing diagram of SPI (CPHA=0, CPOL=0, MSBF=0)

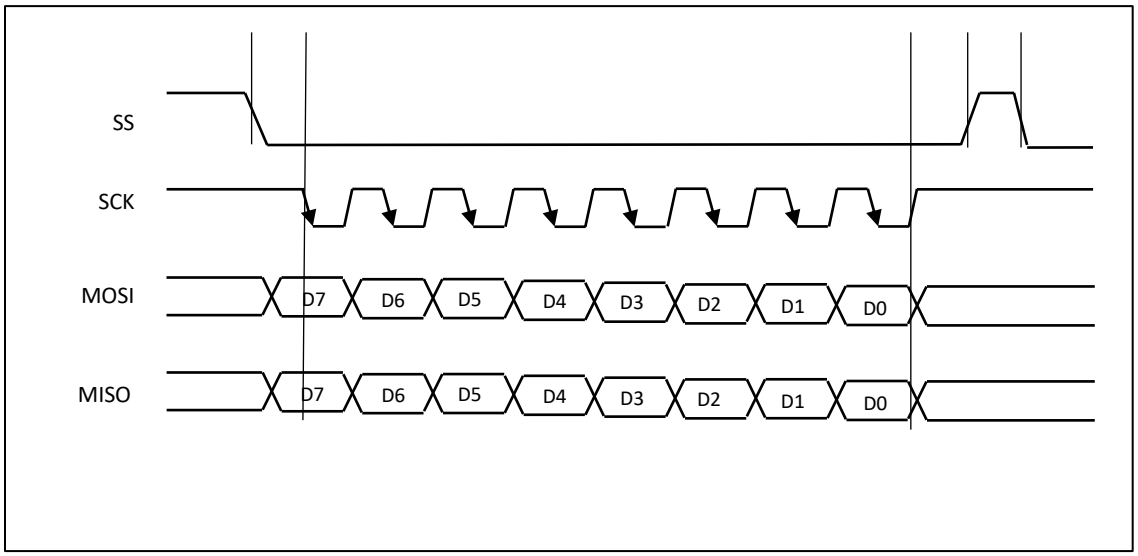


Figure 12.3. Timing diagram of SPI (CPHA=0, CPOL=1, MSBF=1)

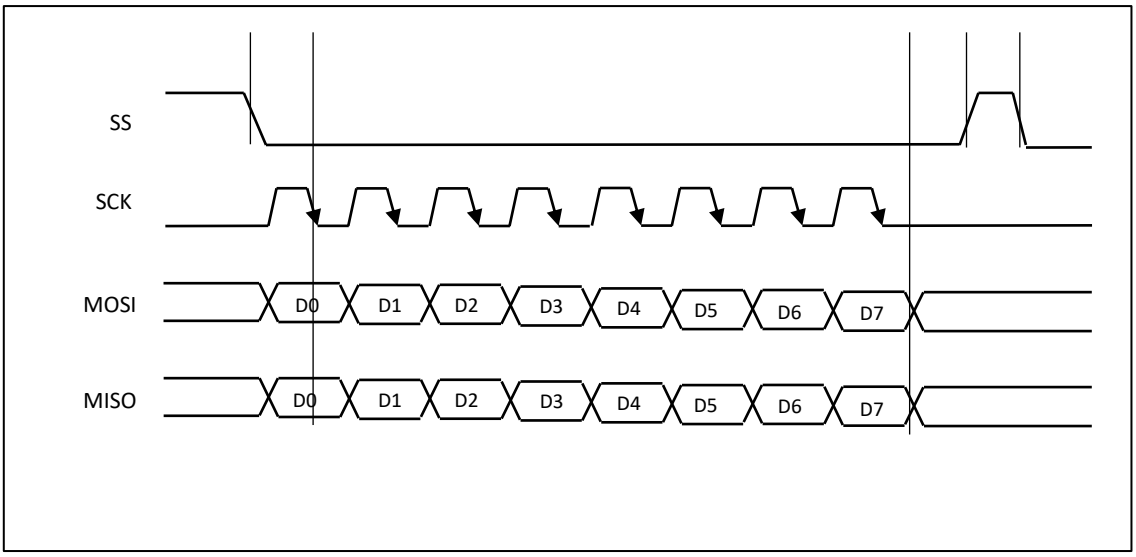


Figure 12.4. Timing diagram of SPI (CPHA=1, CPOL=0, MSBF=0)

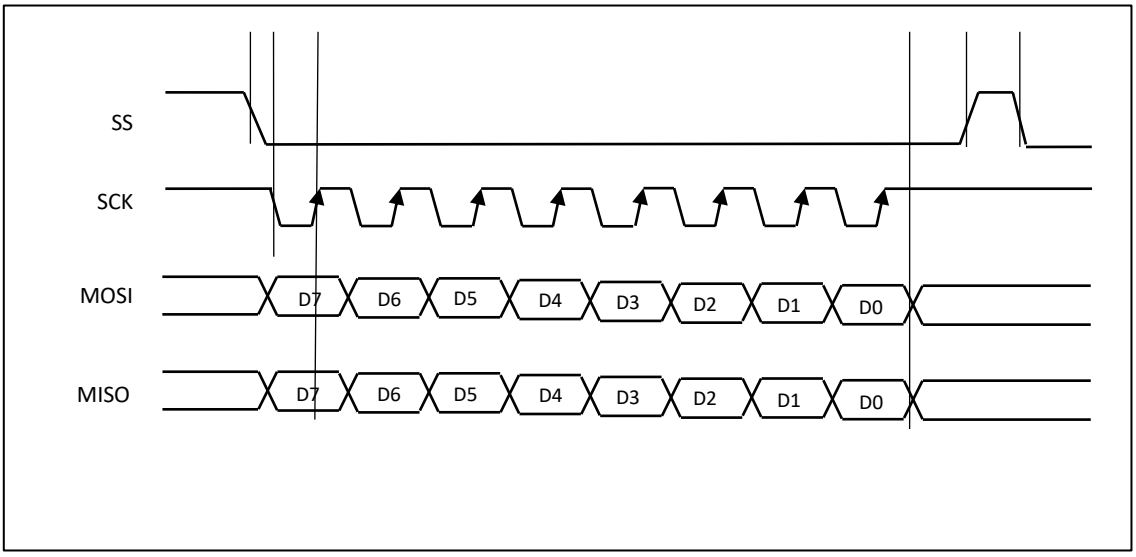


Figure 12.5. Timing diagram of SPI (CPHA=1, CPOL=1, MSBF=1)

CHAPTER 13. 12-bit ADC

Table 13.1. Operation Summary

Item	Description	Remark
Clock usage	PCLK Timer 0~7	Conversion speed Start-of-Conversion
Reset Source	Set by PMU_PER Set by ADCEN/ADSTBY	 ADC_MR
Reset Generation	None	
Interrupt Generation	End-of-Conversion (ADC(43))	ADC_MR
Interrupt Clear Method	Write '1' to ADIF	ADC_CR

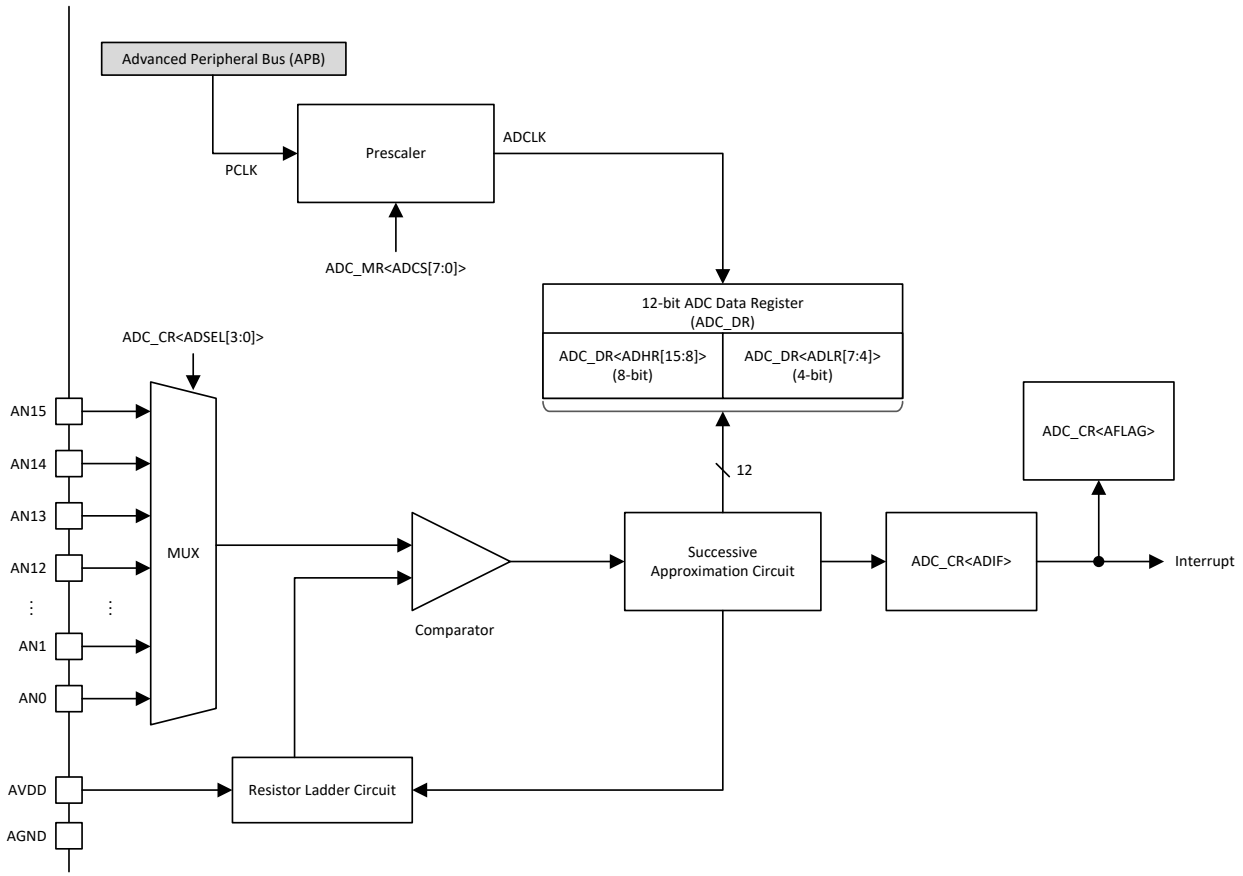
13.1 Overview

The A33G52x has a built-in 12-bit SAR type analog-to-digital converter (ADC) 1-unit and samples the analog signal as a digital signal at 70ksps speed. The ADC (Analog to Digital Converter) built in the A33G52x is designed to receive up to 16 channels in time-divisional manner.
When converting an analog signal to a digital signal, convert the analog value input to the ADC (Analog to Digital Converter) channel to a 12-bit resolution digital value using the signal applied to the AVDD pin (analog voltage supply pin) as the reference voltage . In other words, the input reference voltage of the ADC can be set by varying the voltage of the AVDD pin, and the analog voltage ranging from GND to AVDD can be input and output as a digital signal.

Main Features of 12-bit ADC (Analog Digital Converter)

- 12-bit resolution
- Up to 16 multiplexed input channels
  - 100-pin : 16 channels
  - 80-pin : 16 channels
  - 64-pin : 10 channels
- AVDD pin can be used to set the ADC input reference voltage
- Analog input voltage range: GND to AVDD
- Conversion Time: 15us per channel (at 4MHz ADC clock)
- A / D conversion end interrupt flag support
- External ADC start trigger signal input selection
  - A/D conversion trigger source through timer match function

13.2 Block Diagram



Note 1) The number of ADC input ports depends on the package type. Read the pin configuration of the ADC (CH13.3)

Note 2) The AGND port is not supported in the 64-pin package type and is connected to GND inside the chip. (Figure 16.14)

Figure 13.1. ADC block diagram

13.3 Pin Configuration

Following table shows the list of A/D converter input pins. AVDD and AVSS are the power pins to A/D converter, and AVDD is the reference voltage of A/D converter.

Table 13.2. The pin list of A/D converter

Pin Name	I/O	Description	Support by package		
			A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM	A33G527RL A33G526RL A33G526RM A33G524RL A33G524RM
AVDD*	Power	Analog Power Input	O	O	O
AGND**	Power	Analog GND	Connected to GND	O	O
AN0	Input	Analog Input Channel 0	O	O	O
AN1	Input	Analog Input Channel 1	O	O	O
AN2	Input	Analog Input Channel 2	O	O	O
AN3	Input	Analog Input Channel 3	O	O	O
AN4	Input	Analog Input Channel 4	O	O	O
AN5	Input	Analog Input Channel 5	O	O	O
AN6	Input	Analog Input Channel 6	O	O	O
AN7	Input	Analog Input Channel 7	O	O	O
AN8	Input	Analog Input Channel 8	-	O	O
AN9	Input	Analog Input Channel 9	-	O	O
AN10	Input	Analog Input Channel 10	-	O	O
AN11	Input	Analog Input Channel 11	-	O	O
AN12	Input	Analog Input Channel 12	-	O	O
AN13	Input	Analog Input Channel 13	-	-	O
AN14	Input	Analog Input Channel 14	O	O	O
AN15	Input	Analog Input Channel 15	O	O	O

Note) * Analog VDD volatage is equal to or lower than VDD voltage.
**AVDD, AGND power configuration: See 16.3.8.

13.4 Functional Description

13.4.1 A/D Conversion Timing

The 12-bit ADC built into the A33G52x operates at the following timings.

After start-of-A/D conversion, 10 clocks for stabilization, MSB → LSB conversion, and 1 bit conversion takes 4 clocks. Therefore, the total conversion time is 10 clock + (12-bit data * 4 clock) = total 58 clocks.

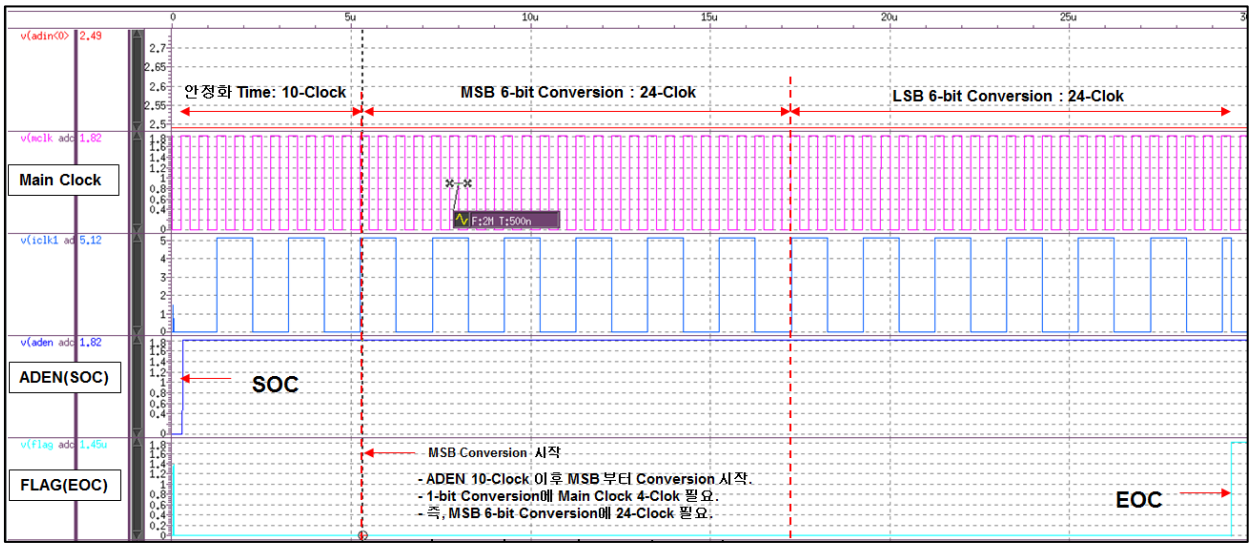


Figure 13.2. A/D conversion timing

13.4.2 ADC Operating Conditions

The ADC of the A33G52x MCU should be used by setting the A/D conversion time according to the reference input voltage AVDD. The following table specifies the ADC operating conditions.

Table 13.3 Operating condition of A/D conversion

AVDD Voltage (V)	ADC Clock (MHz)	A/D Conversion Time (µs)
2.4	0.25	240
2.7	1.00	60
3.0	2.00	30
4.0	3.00	20
5.0	4.00	15

13.4.3 The Resolution of 12-bit ADC

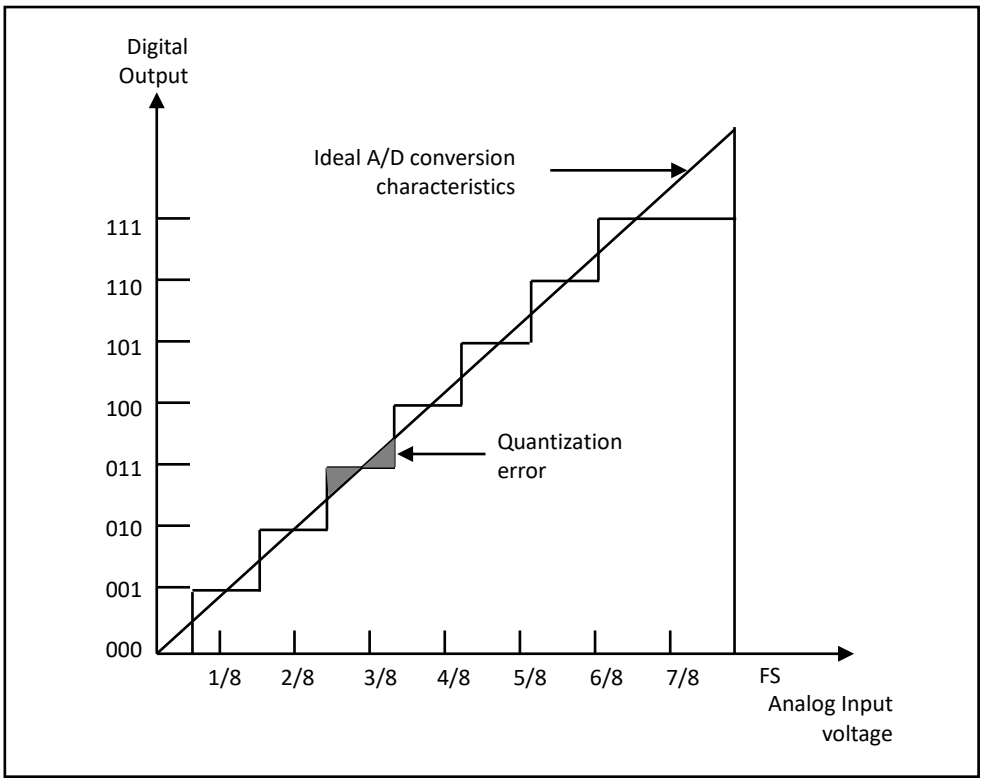


Figure 13.3. The definition of A/D conversion resolution (1)

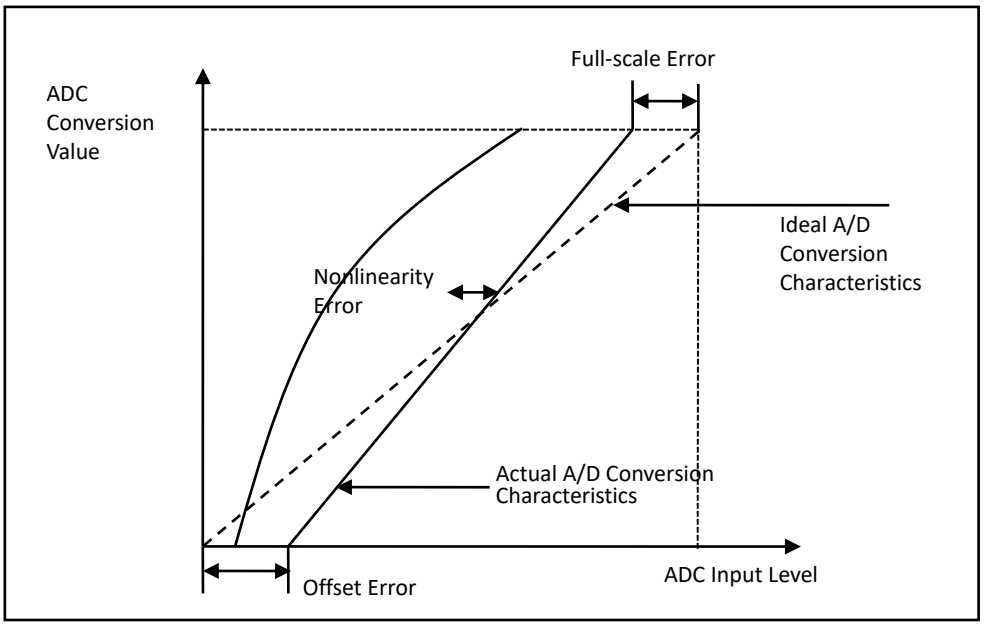


Figure 13.4. The definition of A/D conversion resolution (2)

13.5 Notice

The user should be observe the following notice to ensure that the correct operation of A/D converter.

1. Analog input voltage range : During A/D conversion, voltage level of analog input pin have to be in Vss ≤ ANn ≤ AVDD

2. Analog, Digital voltage:
   Even if ADC is not being used, VDD and GND must not be unconnected.

3. AVREF conversion range : Reference voltage, AVREF is fixed as AVDD.

4. Note for board design : Separates digital circuit from analog circuit in board layout.
   Especially, it needs to avoid the layout that digital signal line crosses analog signal line or goes closely around analog signal line; otherwise, it can cause an incorrect operation of analog circuit and it can affect to the accuracy of A/D conversion.

5. Note about noise : In order to protect circuit from surge voltage or abnormal voltage in AVREF or analog input pins, make a protection circuit between AVDD and AGND like figure 14.5. Bypass condensers connected to AVDD and AVREF and filter condenser connected to analog input pin should be connected to AGND.

6. Influence to absolute accuracy : Attaching external condenser can cause a coupling or a ground connection, and then if there is a noise on ground connection line, it can decrease an absolute accuracy. This condenser should be connected to stable ground like the AGND.
   If filter circuit is used, take into consideration on inference with digital signal at the same board, and check whether the circuit operates like an antenna.

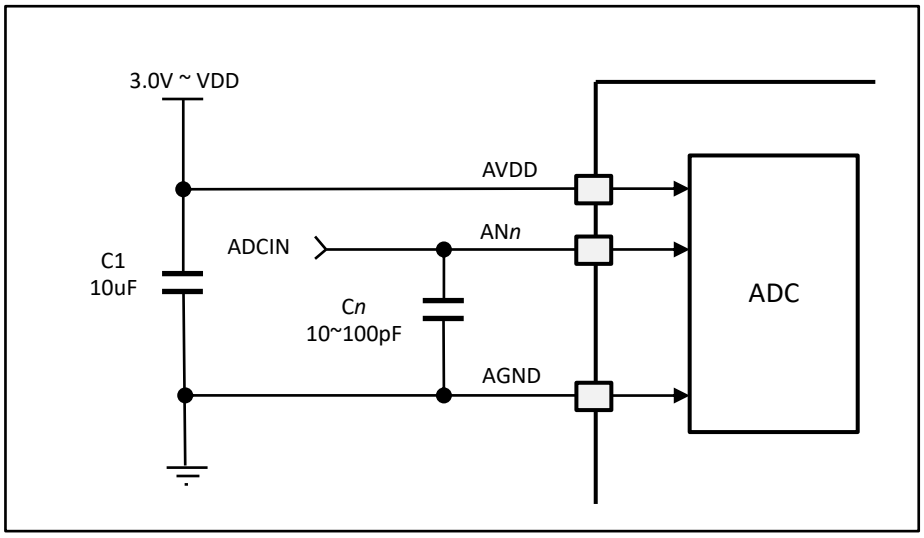


Figure 13.5. A example of ADC circuit

CHAPTER 14. FMC (Flash Memory Controller)

Table 14.1. Operation Summary

Item	Description	Remark
Clock usage	HCLK	Access speed
Reset Source	None	
Reset Generation	None	
Interrupt Generation	None	
Interrupt Clear Method	None	

14.1 Overview

The A33G52x MCU contains a non-volatile memory, code flash and data flash, which are electrically able to erase, program, each with a 1KB sector size. A33G52x series offers a high-capacity code flash, you can use the flash area according to the purpose of user application.
Code and data flash memory of A33G52x also supports CRC16 (Cyclic Redundancy Check 16) function, which enables error detection on data written to flash memory.
When the Extended mode is activated by setting the EX bit value in the FMC_TEST register, functions such as Self-Program, Self-Erase, 512-byte Page Erase, and Boot Block Protection are also available.
In addition, it supports limitations on read/program/erase for specific areas of memory, providing security features such as flash memory protection, external access protection, and security.

Main Features of FMC (Flash Memory Controller)

- Code Flash Capacity : Built-in high capacity code flash memory
  - A33G527 (384KB, 384 Sectors)
  - A33G526 (256KB, 256 Sectors)
  - A33G524 (128KB 128 Sectors)
- Data Flash Capacity : 32KB (32 Sectors)
- Up to 25 MHz Flash Access Timing
- Program size unit
  - Code Flash : 1-word (4 Bytes)
  - Data Flash : 1-byte
- 512 Bytes or 1KB sector ERASE
- Flash Self-PROGRAM of code flash memory
  - Supports to update data in some code flash memory region during execution of user program in code flash area.
- CRC16 generation and verification for error detection
- The restrict a specific area of flash memory for protection and security.
- Endurance
  - Code Flash 10,000 cycles
  - Data Flash 100,000 cycles
- Lifetime : 10 yesrs

14.2 Block Diagram

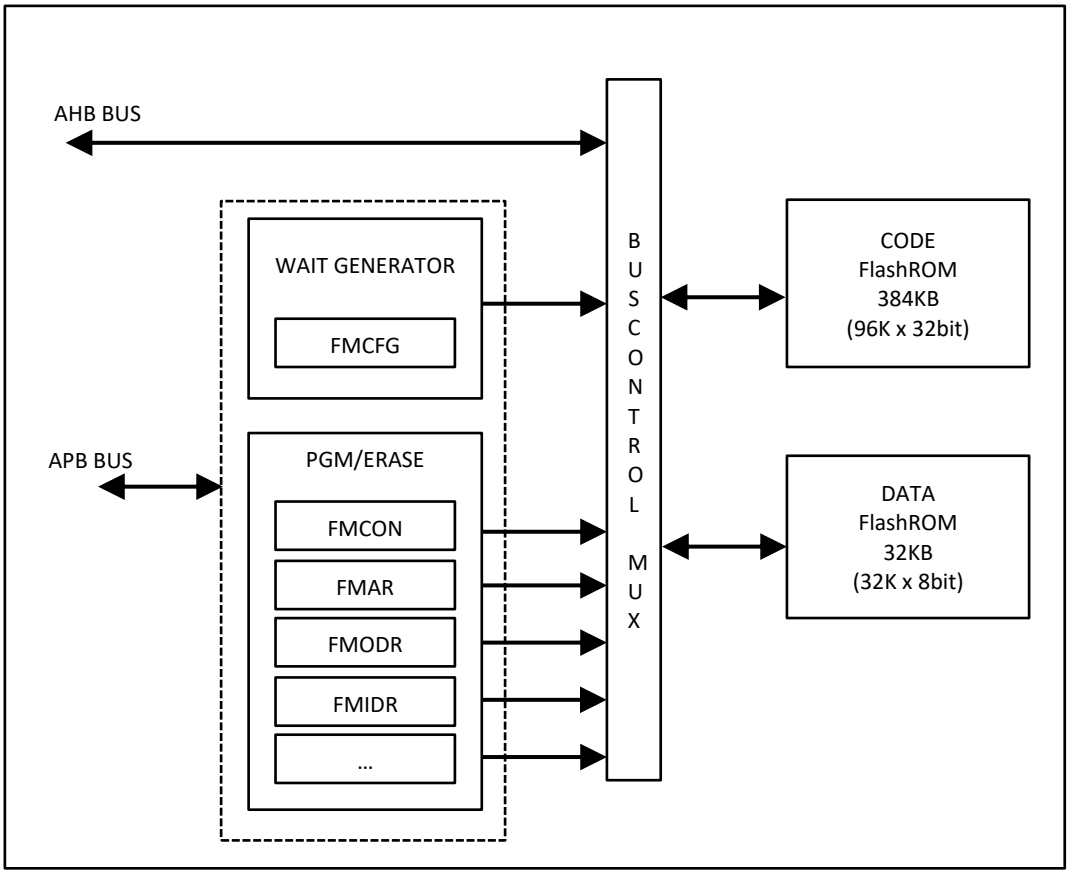
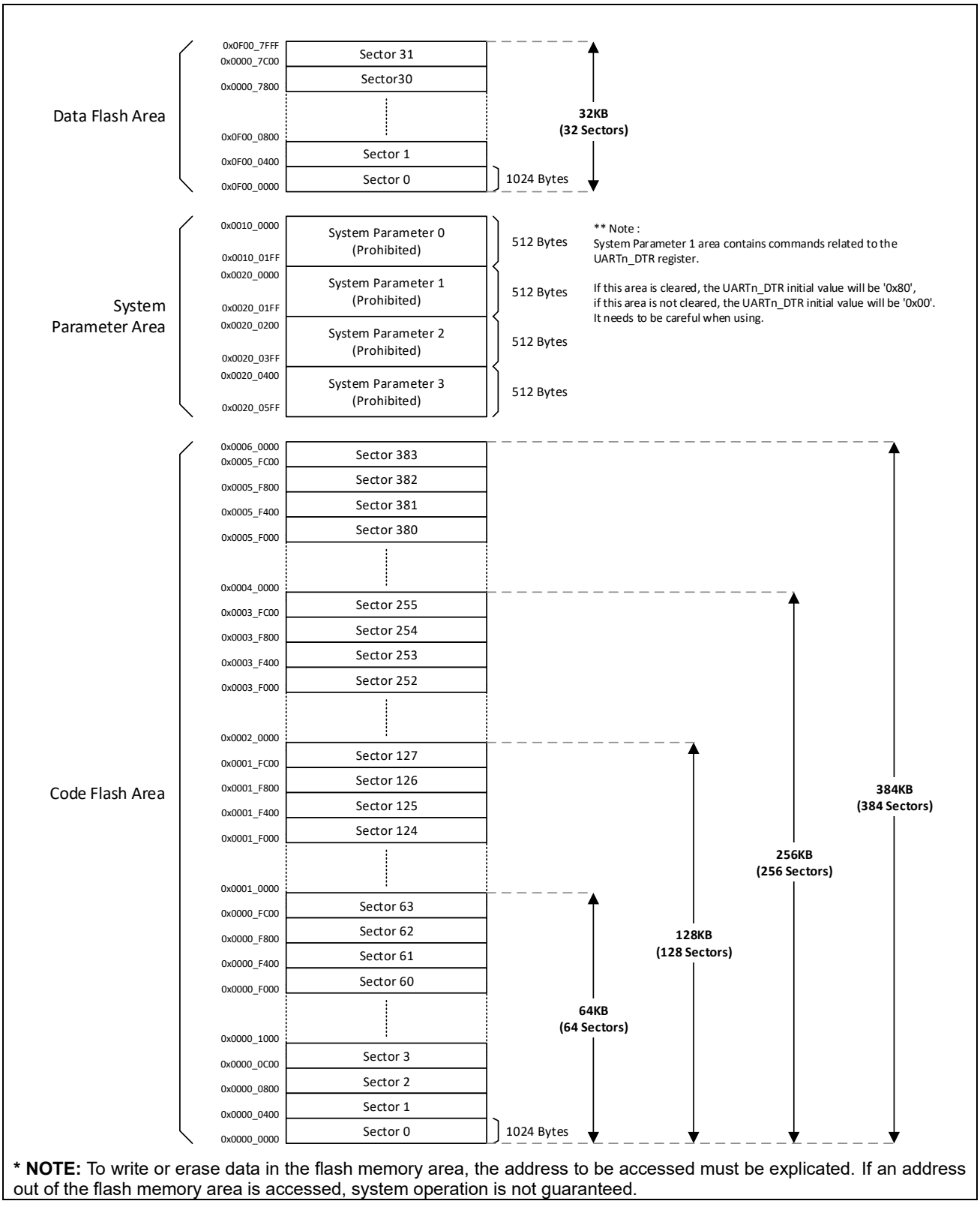


Figure 14.1. The block diagram of FMC (Flash memory controller)

14.2.1 Flash Memory Map

The flash memory map of the A33G52x is shown below.



*** NOTE:** To write or erase data in the flash memory area, the address to be accessed must be explicated. If an address out of the flash memory area is accessed, system operation is not guaranteed.

Figure 14.2. A33G52x Flash Memory Map

14.2.2 Configuring Code Flash Memory Sectors

Code flash memory on the A33G52x is a sector configuration of 1KB units. Addresses for each sector are shown in the table below.

Table 14.2. Sector list of code flash memory

Sector No.	Sector Size	Address	Sector No.	Sector Size	Address	Sector No.	Sector Size	Address	Sector No.	Sector Size	Address
0	1KB	0x0000_0000	96	1KB	0x0001_8000	192	1KB	0x0003_0000	288	1KB	0x0004_8000
1	1KB	0x0000_0400	97	1KB	0x0001_8400	193	1KB	0x0003_0400	289	1KB	0x0004_8400
2	1KB	0x0000_0800	98	1KB	0x0001_8800	194	1KB	0x0003_0800	290	1KB	0x0004_8800
3	1KB	0x0000_0C00	99	1KB	0x0001_8C00	195	1KB	0x0003_0C00	291	1KB	0x0004_8C00
4	1KB	0x0000_1000	100	1KB	0x0001_9000	196	1KB	0x0003_1000	292	1KB	0x0004_9000
5	1KB	0x0000_1400	101	1KB	0x0001_9400	197	1KB	0x0003_1400	293	1KB	0x0004_9400
6	1KB	0x0000_1800	102	1KB	0x0001_9800	198	1KB	0x0003_1800	294	1KB	0x0004_9800
7	1KB	0x0000_1C00	103	1KB	0x0001_9C00	199	1KB	0x0003_1C00	295	1KB	0x0004_9C00
8	1KB	0x0000_2000	104	1KB	0x0001_A000	200	1KB	0x0003_2000	296	1KB	0x0004_A000
9	1KB	0x0000_2400	105	1KB	0x0001_A400	201	1KB	0x0003_2400	297	1KB	0x0004_A400
10	1KB	0x0000_2800	106	1KB	0x0001_A800	202	1KB	0x0003_2800	298	1KB	0x0004_A800
11	1KB	0x0000_2C00	107	1KB	0x0001_AC00	203	1KB	0x0003_2C00	299	1KB	0x0004_AC00
12	1KB	0x0000_3000	108	1KB	0x0001_B000	204	1KB	0x0003_3000	300	1KB	0x0004_B000
13	1KB	0x0000_3400	109	1KB	0x0001_B400	205	1KB	0x0003_3400	301	1KB	0x0004_B400
14	1KB	0x0000_3800	110	1KB	0x0001_B800	206	1KB	0x0003_3800	302	1KB	0x0004_B800
15	1KB	0x0000_3C00	111	1KB	0x0001_BC00	207	1KB	0x0003_3C00	303	1KB	0x0004_BC00
16	1KB	0x0000_4000	112	1KB	0x0001_C000	208	1KB	0x0003_4000	304	1KB	0x0004_C000
17	1KB	0x0000_4400	113	1KB	0x0001_C400	209	1KB	0x0003_4400	305	1KB	0x0004_C400
18	1KB	0x0000_4800	114	1KB	0x0001_C800	210	1KB	0x0003_4800	306	1KB	0x0004_C800
19	1KB	0x0000_4C00	115	1KB	0x0001_CC00	211	1KB	0x0003_4C00	307	1KB	0x0004_CC00
20	1KB	0x0000_5000	116	1KB	0x0001_D000	212	1KB	0x0003_5000	308	1KB	0x0004_D000
21	1KB	0x0000_5400	117	1KB	0x0001_D400	213	1KB	0x0003_5400	309	1KB	0x0004_D400
22	1KB	0x0000_5800	118	1KB	0x0001_D800	214	1KB	0x0003_5800	310	1KB	0x0004_D800
23	1KB	0x0000_5C00	119	1KB	0x0001_DC00	215	1KB	0x0003_5C00	311	1KB	0x0004_DC00
24	1KB	0x0000_6000	120	1KB	0x0001_E000	216	1KB	0x0003_6000	312	1KB	0x0004_E000
25	1KB	0x0000_6400	121	1KB	0x0001_E400	217	1KB	0x0003_6400	313	1KB	0x0004_E400
26	1KB	0x0000_6800	122	1KB	0x0001_E800	218	1KB	0x0003_6800	314	1KB	0x0004_E800
27	1KB	0x0000_6C00	123	1KB	0x0001_EC00	219	1KB	0x0003_6C00	315	1KB	0x0004_EC00
28	1KB	0x0000_7000	124	1KB	0x0001_F000	220	1KB	0x0003_7000	316	1KB	0x0004_F000
29	1KB	0x0000_7400	125	1KB	0x0001_F400	221	1KB	0x0003_7400	317	1KB	0x0004_F400
30	1KB	0x0000_7800	126	1KB	0x0001_F800	222	1KB	0x0003_7800	318	1KB	0x0004_F800
31	1KB	0x0000_7C00	127	1KB	0x0001_FC00	223	1KB	0x0003_7C00	319	1KB	0x0004_FC00
32	1KB	0x0000_8000	128	1KB	0x0002_0000	224	1KB	0x0003_8000	320	1KB	0x0005_0000
33	1KB	0x0000_8400	129	1KB	0x0002_0400	225	1KB	0x0003_8400	321	1KB	0x0005_0400
34	1KB	0x0000_8800	130	1KB	0x0002_0800	226	1KB	0x0003_8800	322	1KB	0x0005_0800
35	1KB	0x0000_8C00	131	1KB	0x0002_0C00	227	1KB	0x0003_8C00	323	1KB	0x0005_0C00
36	1KB	0x0000_9000	132	1KB	0x0002_1000	228	1KB	0x0003_9000	324	1KB	0x0005_1000
37	1KB	0x0000_9400	133	1KB	0x0002_1400	229	1KB	0x0003_9400	325	1KB	0x0005_1400
38	1KB	0x0000_9800	134	1KB	0x0002_1800	230	1KB	0x0003_9800	326	1KB	0x0005_1800
39	1KB	0x0000_9C00	135	1KB	0x0002_1C00	231	1KB	0x0003_9C00	327	1KB	0x0005_1C00
40	1KB	0x0000_A000	136	1KB	0x0002_2000	232	1KB	0x0003_A000	328	1KB	0x0005_2000
41	1KB	0x0000_A400	137	1KB	0x0002_2400	233	1KB	0x0003_A400	329	1KB	0x0005_2400
42	1KB	0x0000_A800	138	1KB	0x0002_2800	234	1KB	0x0003_A800	330	1KB	0x0005_2800
43	1KB	0x0000_AC00	139	1KB	0x0002_2C00	235	1KB	0x0003_AC00	331	1KB	0x0005_2C00
44	1KB	0x0000_B000	140	1KB	0x0002_3000	236	1KB	0x0003_B000	332	1KB	0x0005_3000
45	1KB	0x0000_B400	141	1KB	0x0002_3400	237	1KB	0x0003_B400	333	1KB	0x0005_3400
46	1KB	0x0000_B800	142	1KB	0x0002_3800	238	1KB	0x0003_B800	334	1KB	0x0005_3800
47	1KB	0x0000_BC00	143	1KB	0x0002_3C00	239	1KB	0x0003_BC00	335	1KB	0x0005_3C00
48	1KB	0x0000_C000	144	1KB	0x0002_4000	240	1KB	0x0003_C000	336	1KB	0x0005_4000
49	1KB	0x0000_C400	145	1KB	0x0002_4400	241	1KB	0x0003_C400	337	1KB	0x0005_4400
50	1KB	0x0000_C800	146	1KB	0x0002_4800	242	1KB	0x0003_C800	338	1KB	0x0005_4800
51	1KB	0x0000_CC00	147	1KB	0x0002_4C00	243	1KB	0x0003_CC00	339	1KB	0x0005_4C00
52	1KB	0x0000_D000	148	1KB	0x0002_5000	244	1KB	0x0003_D000	340	1KB	0x0005_5000
53	1KB	0x0000_D400	149	1KB	0x0002_5400	245	1KB	0x0003_D400	341	1KB	0x0005_5400
54	1KB	0x0000_D800	150	1KB	0x0002_5800	246	1KB	0x0003_D800	342	1KB	0x0005_5800
55	1KB	0x0000_DC00	151	1KB	0x0002_5C00	247	1KB	0x0003_DC00	343	1KB	0x0005_5C00
56	1KB	0x0000_E000	152	1KB	0x0002_6000	248	1KB	0x0003_E000	344	1KB	0x0005_6000
57	1KB	0x0000_E400	153	1KB	0x0002_6400	249	1KB	0x0003_E400	345	1KB	0x0005_6400
58	1KB	0x0000_E800	154	1KB	0x0002_6800	250	1KB	0x0003_E800	346	1KB	0x0005_6800
59	1KB	0x0000_EC00	155	1KB	0x0002_6C00	251	1KB	0x0003_EC00	347	1KB	0x0005_6C00
60	1KB	0x0000_F000	156	1KB	0x0002_7000	252	1KB	0x0003_F000	348	1KB	0x0005_7000
61	1KB	0x0000_F400	157	1KB	0x0002_7400	253	1KB	0x0003_F400	349	1KB	0x0005_7400
62	1KB	0x0000_F800	158	1KB	0x0002_7800	254	1KB	0x0003_F800	350	1KB	0x0005_7800

63	1KB	0x0000_FC00	159	1KB	0x0002_7C00	255	1KB	0x0003_FC00	351	1KB	0x0005_7C00
64	1KB	0x0001_0000	160	1KB	0x0002_8000	256	1KB	0x0004_0000	352	1KB	0x0005_8000
65	1KB	0x0001_0400	161	1KB	0x0002_8400	257	1KB	0x0004_0400	353	1KB	0x0005_8400
66	1KB	0x0001_0800	162	1KB	0x0002_8800	258	1KB	0x0004_0800	354	1KB	0x0005_8800
67	1KB	0x0001_0C00	163	1KB	0x0002_8C00	259	1KB	0x0004_0C00	355	1KB	0x0005_8C00
68	1KB	0x0001_1000	164	1KB	0x0002_9000	260	1KB	0x0004_1000	356	1KB	0x0005_9000
69	1KB	0x0001_1400	165	1KB	0x0002_9400	261	1KB	0x0004_1400	357	1KB	0x0005_9400
70	1KB	0x0001_1800	166	1KB	0x0002_9800	262	1KB	0x0004_1800	358	1KB	0x0005_9800
71	1KB	0x0001_1C00	167	1KB	0x0002_9C00	263	1KB	0x0004_1C00	359	1KB	0x0005_9C00
72	1KB	0x0001_2000	168	1KB	0x0002_A000	264	1KB	0x0004_2000	360	1KB	0x0005_A000
73	1KB	0x0001_2400	169	1KB	0x0002_A400	265	1KB	0x0004_2400	361	1KB	0x0005_A400
74	1KB	0x0001_2800	170	1KB	0x0002_A800	266	1KB	0x0004_2800	362	1KB	0x0005_A800
75	1KB	0x0001_2C00	171	1KB	0x0002_AC00	267	1KB	0x0004_2C00	363	1KB	0x0005_AC00
76	1KB	0x0001_3000	172	1KB	0x0002_B000	268	1KB	0x0004_3000	364	1KB	0x0005_B000
77	1KB	0x0001_3400	173	1KB	0x0002_B400	269	1KB	0x0004_3400	365	1KB	0x0005_B400
78	1KB	0x0001_3800	174	1KB	0x0002_B800	270	1KB	0x0004_3800	366	1KB	0x0005_B800
79	1KB	0x0001_3C00	175	1KB	0x0002_BC00	271	1KB	0x0004_3C00	367	1KB	0x0005_BC00
80	1KB	0x0001_4000	176	1KB	0x0002_C000	272	1KB	0x0004_4000	368	1KB	0x0005_C000
81	1KB	0x0001_4400	177	1KB	0x0002_C400	273	1KB	0x0004_4400	369	1KB	0x0005_C400
82	1KB	0x0001_4800	178	1KB	0x0002_C800	274	1KB	0x0004_4800	370	1KB	0x0005_C800
83	1KB	0x0001_4C00	179	1KB	0x0002_CC00	275	1KB	0x0004_4C00	371	1KB	0x0005_CC00
84	1KB	0x0001_5000	180	1KB	0x0002_D000	276	1KB	0x0004_5000	372	1KB	0x0005_D000
85	1KB	0x0001_5400	181	1KB	0x0002_D400	277	1KB	0x0004_5400	373	1KB	0x0005_D400
86	1KB	0x0001_5800	182	1KB	0x0002_D800	278	1KB	0x0004_5800	374	1KB	0x0005_D800
87	1KB	0x0001_5C00	183	1KB	0x0002_DC00	279	1KB	0x0004_5C00	375	1KB	0x0005_DC00
88	1KB	0x0001_6000	184	1KB	0x0002_E000	280	1KB	0x0004_6000	376	1KB	0x0005_E000
89	1KB	0x0001_6400	185	1KB	0x0002_E400	281	1KB	0x0004_6400	377	1KB	0x0005_E400
90	1KB	0x0001_6800	186	1KB	0x0002_E800	282	1KB	0x0004_6800	378	1KB	0x0005_E800
91	1KB	0x0001_6C00	187	1KB	0x0002_EC00	283	1KB	0x0004_6C00	379	1KB	0x0005_EC00
92	1KB	0x0001_7000	188	1KB	0x0002_F000	284	1KB	0x0004_7000	380	1KB	0x0005_F000
93	1KB	0x0001_7400	189	1KB	0x0002_F400	285	1KB	0x0004_7400	381	1KB	0x0005_F400
94	1KB	0x0001_7800	190	1KB	0x0002_F800	286	1KB	0x0004_7800	382	1KB	0x0005_F800
95	1KB	0x0001_7C00	191	1KB	0x0002_FC00	287	1KB	0x0004_7C00	383	1KB	0x0005_FC00

14.2.3 Configuring Data Flash Memory Sectors

Data flash memory on the A33G52x is a sector configuration of 1KB units. Addresses for each sector are shown in the table below.

Table 14.3. Sector list of data flash memory

Sector No.	Sector Size	Address	Sector No.	Sector Size	Address
0	1KB	0x0F00_0000	16	1KB	0x0F00_4000
1	1KB	0x0F00_0400	17	1KB	0x0F00_4400
2	1KB	0x0F00_0800	18	1KB	0x0F00_4800
3	1KB	0x0F00_0C00	19	1KB	0x0F00_4C00
4	1KB	0x0F00_1000	20	1KB	0x0F00_5000
5	1KB	0x0F00_1400	21	1KB	0x0F00_5400
6	1KB	0x0F00_1800	22	1KB	0x0F00_5800
7	1KB	0x0F00_1C00	23	1KB	0x0F00_5C00
8	1KB	0x0F00_2000	24	1KB	0x0F00_6000
9	1KB	0x0F00_2400	25	1KB	0x0F00_6400
10	1KB	0x0F00_2800	26	1KB	0x0F00_6800
11	1KB	0x0F00_2C00	27	1KB	0x0F00_6C00
12	1KB	0x0F00_3000	28	1KB	0x0F00_7000
13	1KB	0x0F00_3400	29	1KB	0x0F00_7400
14	1KB	0x0F00_3800	30	1KB	0x0F00_7800
15	1KB	0x0F00_3C00	31	1KB	0x0F00_7C00

CHAPTER 15. Internal SRAM

Table 15.1. Operation Summary

Item	Description	Remark
Clock usage	HCLK	Access speed
Reset Source	None	
Reset Generation	None	
Interrupt Generation	None	
Interrupt Clear Method	None	

15.1 Overview

The A33G52x has a built-in 24-kbyte SRAM capable of data and code area.

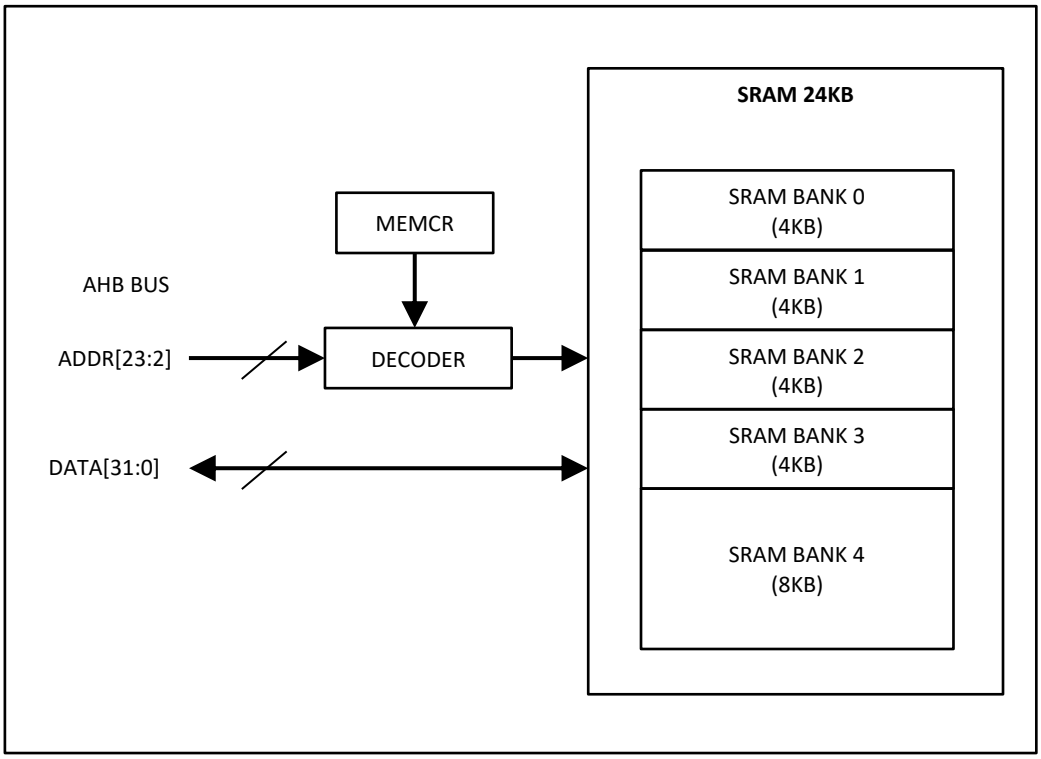


Figure 15.1. SRAM Block Diagram

15.1.1 Bank Configuration of SRAM

The SRAM consists of several blocks as below.

0x2000_0000 0x2000_0FFF	SRAM Block 0	remapped at 0x0000_0000 (Area 0)
0x2000_1000 0x2000_1FFF	SRAM Block 1	remapped at 0x0000_1000 (Area 1)
0x2000_2000 0x2000_2FFF	SRAM Block 2	remapped at 0x0000_2000 (Area 2)
0x2000_3000 0x2000_3FFF	SRAM Block 3	remapped at 0x0000_3000 (Area 3)
0x2000_4000 0x2000_5FFF	SRAM Block 4	Fixed Block

Figure 15.2. Configuration of the Banks of SRAM

CHAPTER 16. Electrical Characteristics

16.1 DC Characteristics

16.1.1 Absolute Maximum Ratings

The maximum rating of A33G527 is shown as follows

Table 16.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Digital Power Supply	VDD	-0.3 ~ +6.5	V
Analog Power Supply	AVDD	-0.3 ~ +5.5	V
Input Voltage	VI	VSS-0.3 ~ VDD+0.3	V
Output Voltage	VO	VSS-0.3 ~ VDD+0.3	V
Output Current	IOH	10	mA
	∑IOH	80	
	IOL	20	
	∑IOL	160	
Input Main Clock Range	fXIN	8	MHz
Operating Frequency	fPLLOUT	75	MHz
Total Power Dissipation	PT	600	mW
Storage Temperature	T_{STG}	-45 ~ +125	℃
Maximum Operating Junction Temperature	T_J	105	℃

Table 16.2. The Recommandation for Operating

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital Power Supply	VDD	4 ~ 75MHz	3.0	5.0	5.5	V
Analog Power Supply	AVDD		3.0	-	VDD	V
Operating Temperature	T_{OPR}	VDD=3.0~5.5V	-40	-	85	℃
Operating Frequency	FREQ	fXIN	-	4	8	MHz
		Internal OSC		16		
		PLL	4	-	75	
Supply Rise Rate	t_{rVDD}		-	-	0.05	V/us
Supply Fall Rate	t_{fVDD}		-	-	0.1	

16.1.2 I/O Ports DC Characteristics

The DC Characteristics of A33G52x I/O ports is shown as follows

Table 16.3. I/O Ports DC Characteristics(1) (VDD = +5V, VSS=0V, Temperature=25℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Input Low Voltage	V_{IL}	Port A,B,C,E,F	-0.3	-	1	V
		Port D	-0.3	-	1	V
Input High Voltage	V_{IH}	Port A,B,C,E,F	4	-	5.3	V
		Port D	2.7	-	5.3	V
Hysteresis Voltage(1)	V_H		-	1.0	-	V
Output Low Voltage (Port A,B,C,E,F)	V_{OL}	I_{OL}=3mA	0	-	1	V
Output Low Voltage (Port D)		I_{OL}=18mA	0	-	1	V
Output High Voltage (Port A,B,C,E,F)	V_{OH}	I_{OH}=-1.2mA	4	-	5	V
Output High Voltage (Port D)		I_{OH}=-8mA	4	-	5	V
Output Low Current	I_{OL}	V_{OL}=1V (Port A,B,C,E,F)	+3	-	-	mA
		V_{OL}=1V (Port D)	+18	-	-	mA
Output High Current	I_{OH}	V_{OH}=4V (Port A,B,C,E,F)	-	-	-1.2	mA
		V_{OH}=4V (Port D)	-	-	-8	mA
Input Low Leakage Current	I_{IL}		-4	-	-	uA
Input High Leakage Current	I_{IH}		-	-	+4	uA
Pull-up Resistor	R_{PU}		10	-	60	kΩ
Pull-down Resistor	R_{PD}		40		70	kΩ

(1) Hysteresis voltage between schmitt trigger switching levels. Based on characterization, NOT tested in production

Table 16.4 I/O Ports DC Characteristics(2) (VDD = +3.3V, VSS=0V, Temperature=25℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Input Low Voltage	V_{IL}	Port A,B,C,E,F	-0.3	-	0.6	V
		Port D	-0.3	-	0.6	V
Input High Voltage	V_{IH}	Port A,B,C,E,F	2.7	-	3.6	V
		Port D	2.2	-	3.6	V
Hysteresis Voltage(1)	V_H	Port A,B,C,E,F	-	1.0	-	V
Output Low Voltage (Port A,B,C,E,F)	V_{OL}	I_{OL}=2mA	0	-	0.66	V
Output Low Voltage (Port D)		I_{OL}=10mA	0	-	0.66	V
Output High Voltage (Port A,B,C,E,F)	V_{OH}	I_{OH}=0.8mA	2.64	-	3.3	V
Output High Voltage (Port D)		I_{OH}=6mA	2.64	-	3.3	V
Output Low Current	I_{OL}	V_{OL}=0.6V (Port A,B,C,E,F)	+2	-	-	mA
		V_{OL}=0.6V (Port D)	+10	-	-	mA
Output High Current	I_{OH}	V_{OH}=2.7V (Port A,B,C,E,F)	-	-	-0.8	mA
		V_{OH}=2.7V (Port D)	-	-	-6	mA
Input Low Leakage Current	I_{IL}		-4	-	-	uA
Input High Leakage Current	I_{IH}		-	-	4	uA
Pull-up Resistor	R_{PU}		10	-	100	kΩ
Pull-down Resistor	R_{PD}		40		70	kΩ

(1) Hysteresis voltage between schmitt trigger switching levels. Based on characterization, NOT tested in production.

16.1.3 POR (Power On Reset) Operating Characteristics

The characteristics of the Power-on-Reset is shown as follows

Table 16.5 The POR Operating Characteristics (Temperature range : -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Operating Current	IDD	Typ. <6uA If always on	-	60	-	nA
POR Set Level	VIH	VDD rising (slow)	1.05	1.20	1.35	V
POR Reset Level	VIL	VDD falling (slow)	1.00	1.10	1.20	V

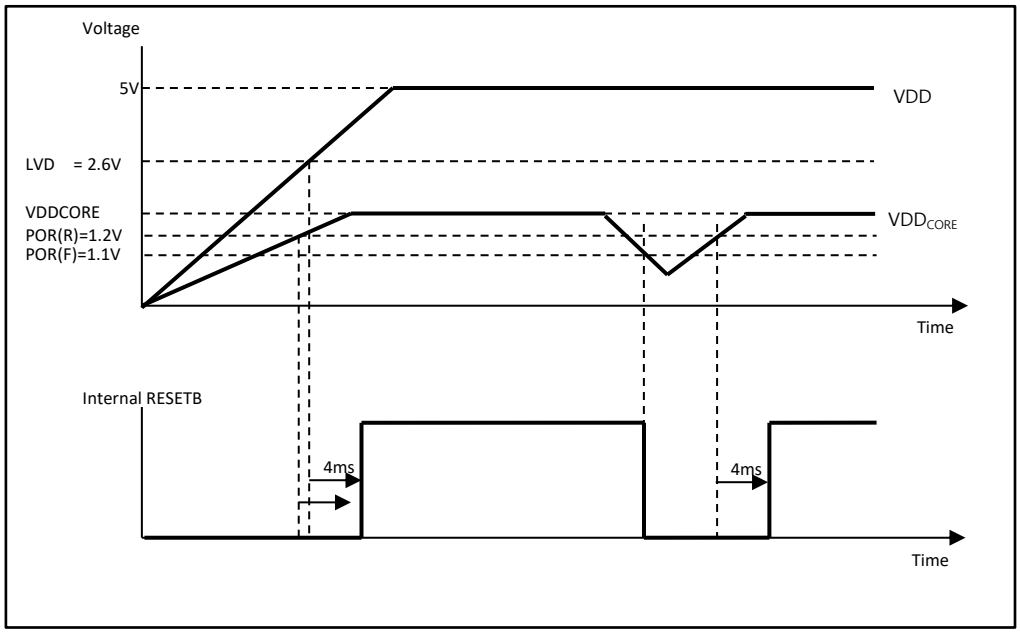


Figure 16.1. The Reset Timing

16.1.4 LVD (Low Voltage Detector) Operating Characteristics

The Characteristics of the LVD is shown as follows

Table 16.6 The LVD (Low Voltage Detector) Operating Characteristics (Temperature range : -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Operating Current	IDD	-	-	-	50	uA
Stop Current	I_{STOP}	-	-	-	-	uA
LVD LEVEL	V_{DET}	2.60V 2.80V 3.00V 3.30V 3.75V 4.00V 4.25V 4.50V	-10	-	+10	%
Hysteresis	V_H	2us delay		100		mV

Once the VDD level has fallen below the LVD level, it does not guarantee the operation before the stabilization time about 200us after rising over the LVD voltage.
The operating timing of LVD is shown as below.

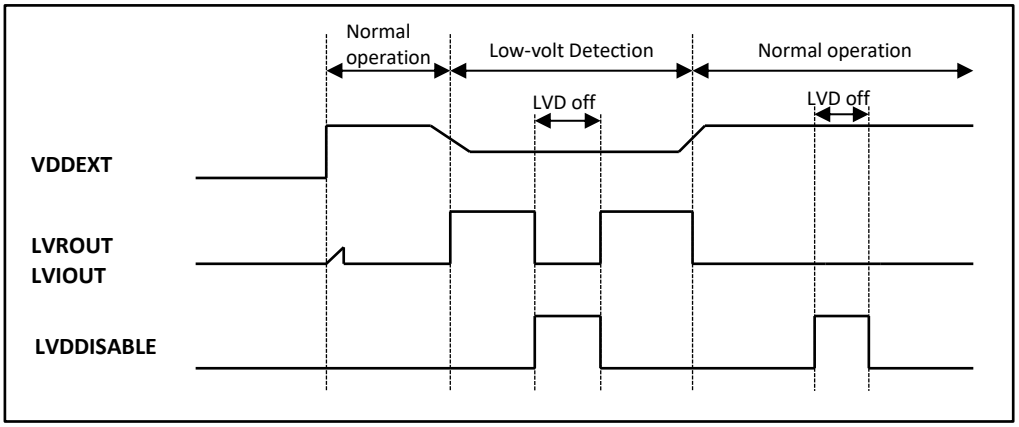


Figure 16.2. The Reset Timing

16.1.5 DC Characteristics of Internal Oscillator (IOSC16, RINGOSC)

The DC characteristics of internal 16MHz RC-Oscillator and RING-Oscillator are shown as follows.

Table 16.7 DC Characteristics of Internal Oscillator (Temperature=-0 ~ +40℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	160	250	uA	
Output frequency	15.76	16	16.24	MHz	±1.5%
Output frequency duty	40	-	60	%	

Table 16.8 DC Characteristics of Internal Oscillator (Temperature=-20 ~ +70℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	160	250	uA	
Output frequency	15.52	16	16.48	MHz	±3%
Output frequency duty	40	-	60	%	

Table 16.9 DC Characteristics of Internal Oscillator (Temperature=-40 ~ +85℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	160	250	uA	
Output frequency	15.36	16	16.64	MHz	±4%
Output frequency duty	40	-	60	%	

Table 16.10 DC Characteristicss of Internal Ring Oscillator (Temperature=-40 ~ +85℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	4	8	uA	
Output frequency	0.5	1.0	1.5	MHz	±50%

16.1.6 DC Characteristics of Main and Sub Crystal Oscillator

The operating characteristics of the main oscillator and sub oscillator built into the A33G52x are shown in the table below. To enhance noise immunity, the A33G52x adopts a full-swing scheme.

Table 16.11 Characteristics of Main Crystal Oscillator (Temperature=-40 ~ +85℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	500*	1000	uA	@8MHz/5V
Operating Frequency	4	8	10	MHz	
Output Voltage (V_{XOUT})	0.8 VDD		-	V	
Output Currrent (I_{XOUT})	3**			mA	
Load Capacitance		18/22	35	pF	

[*] The swing scheme changed from Half-Swing to Full-Swing, the IDD current was adjusted.
[**] Output Current(I_{XOUT}) indicates the current driving capacity of the transistor that constitutes the oscillation part.

Table 16.12 Built-in sub oscillator operating characteristics (temperature = -40 to + 85 ℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	4	7	uA	
Operating Frequency	-	32.768	-	kHz	
Output Voltage	-	1.5	-	V	
Load Capacitance	5	15	25	pF	

16.1.7 DC Characteristics of Internal PLL

The operating characteristics of the PLL built in the A33G52x are shown in the table below.

Table 16.13 The Characteristics of Internal PLL (Temperature=-40 ~ +85℃)

Item	Min	Typ	Max	Unit	Remark
IDD	-	1.3	-	mA	75MHz
Output Frequency	8	75	90	MHz	
Duty	40	-	60	%	
P-P Jitter	-	-	500	ps	@Lock state
VCO Frequency (Extended mode)	50	-	200	MHz	
VCOx2[1)] Frequency(Extended mode)	100		250	MHz	
Input Frequecy	4	-	8	MHz	
Lock Time	-	-	10	ms	

1) VCOx2 means that VCOMODE bit of PMU_PLLCON register is set to '1' then VCO Doubler Mode is enabled.

16.1.8 Current Consumption for Each Mode

The current consumption for each operation mode is shown as follows.

Table 16.14 Current Consumption for Each Mode (Room Temperature)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Normal Operation (Run Mode)	IDD_{NORMAL}	ROSC=RUN IOSC16=RUN MXOSC=RUN SUBOSC=RUN	-	30	-	mA
Sleep Mode (Idle Mode)	IDD_{SLEEP}	ROSC=RUN IOSC16=STOP MXOSC=STOP SUBOSC=STOP	-	500	-	uA
Deep-Sleep Mode (PowerDown Mode)	IDD_{STOP}	ROSC=STOP IOSC16=STOP MXOSC=STOP SUBOSC=STOP	-	100	-	uA

16.1.9 Specifications of Internal Flash Memory

The specifications of built-in flash memories are shown as follows.

Table 16.15 Specification of the Code Flash Memory

Parameter	Min	Typ.	Max	Unit
Operating Temperature	-40	-	+85	℃
Total code memory size*	-	-	384	KB
Unit sector size	1024	-	-	byte
BUS width	-	-	32	bit
Erase/program Endurance	10,000	-	-	cycle
Data retention	10	-	-	year

Note *) A33G527 : 384KB, A33G526 : 256KB, A33G524: 128KB

Table 16.16 Characteristics of the Code Flash Memory

Parameter	Symbol	Min	Typ.	Max	Unit
Standby current	I_{SB}	-	-	10	uA
Active read current (f=25MHz)	I_{CC1}	-	-	10	mA
Write current	I_{CC2}	-	-	7	mA
Erase current	I_{CC3}	-	-	7	mA
Read access time	tAC	40	-	-	ns
Read cycle time	tAAD	40	-	-	ns
Program time	tPROG	21	30	39	us
Sector erase time	tSER	2.8	4	5.2	ms
Macro erase time	tMER	5.6	8	10.4	ms

Table 16.17 Specification of the Data Flash Memory

Parameter	Min	Typ.	Max	Unit
Operating Temperature	-40	-	+85	℃
Total data memory size	-	-	32	KB
Unit sector size	1024	-	-	byte
BUS width	-	-	8	bit
Erase/program endurance	100,000	-	-	cycle
Data retention	10	-	-	year

Table 16.18 Characteristics of the Data Flash Memory

Parameter	Symbol	Min	Typ.	Max	Unit
Standby current	I_{SB}	-	1	10	uA
Active read current (f=20MHz)	I_{CC1}	-	-	3	mA
Write current	I_{CC2}	-	5	7	mA
Erase current	I_{CC3}	-	5	7	mA
Read access time	tAC	40	-	-	ns
Read cycle time	tAAD	40	-	-	ns
Program time	tPROG	21	30	39	us
Sector erase time	tSER	2.8	4	5.2	ms
Macro erase time	tMER	5.6	8	10.4	ms

16.1.10 A/D Converter Operating Characteristics

The electrical characteristics of A/D converter of A33G52x are as follows

Table 16.19 The Electrical Characteristics of A/D converter (Temperature=-20 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AVDD		3.0	5	5.5	V
Resolution				12		Bit
Operating Current	IDDA	VDD=5.0V		1	2	mA
Analog Input Range	VAN		VSS		AVDD	V
Conversion Rate	fCON	5.0V<AVDD <5.5V		60*MCLK	66.6	kSPS
Operating Frequency	MCLK				4	MHz
DC Accuracy	INL	AVDD=5.0V, T_A = 25 °C		±8		LSB
	DNL			±2		LSB
Zero Offset Error*	ZOE			2		LSB
Full Scale Error**	FSE			2		LSB

Notes)

* Zero Offset Error is the difference between the zero input voltage (VSS) converted to a digital value and 0x000.

** full Scale Error is the difference between the top input voltage (VDD) converted to a digital value and 0xFFF.

16.2 AC Characteristics

16.2.1 AC Characteristics of the Internal Flash Memory

Table 16.20 AC Characteristics of the Internal Flash Memory (Room Temperature)

Parameter	Symbol	Min	Typ.	Max	Unit
Address setup time	tAS	2		-	ns
Address hold time	tAH	2		-	ns
Setup time of write and erase	tS	5		-	ns
Hold time of write and erase	tH	2		-	ns
Data setup time	tDS	2		-	ns
Data hold time	tDH	2		-	ns
Read access time	tAC	-		40	ns
AE pulse width	tAE	10		-	ns
AE to AE delay during read (Read cycle time)	tAAD	40		-	ns
AE low pulse width	tAEL	10			ns
Program time	tPROG	-		20	us
Sector erase time	tSER	-		2	ms
Macro erase time	tMER	-		10	ms
NVSTR to AE delay	tNVSTR	10		-	ns
CS setup time to AE rising edge	tCS	5		-	ns
TBIT rises after NVSTR	tTR	-		100	ns
TBIT falls after NVSTR for write	tTF	21	30	39	us
TBIT falls after NVSTR for sector erase	tTF	2.8	4	5.2	ms
TBIT falls after NVSTR for macro erase	tTF	5.6	8	10.4	ms

16.2.2 I2C Characteristics

The following table and figure show the timing codition of SDA and SCL bus lines for I2C bus devices.

Table 16.21 Timing Characteristics of the I2C

Parameter	Symbol	STANDARD MODE		FAST MODE		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time after (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	us
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	us
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	us
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	us
Data setup time	$t_{SU;DAT}$	100	-	100	-	ns
Clock/data fall time	t_F	0	300	0	300	ns
Clock/data rise time	t_R	0	1000	0	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	us
Bus free time between a STOP and START condtion	t_{BUF}	4.7	-	1.3	-	us

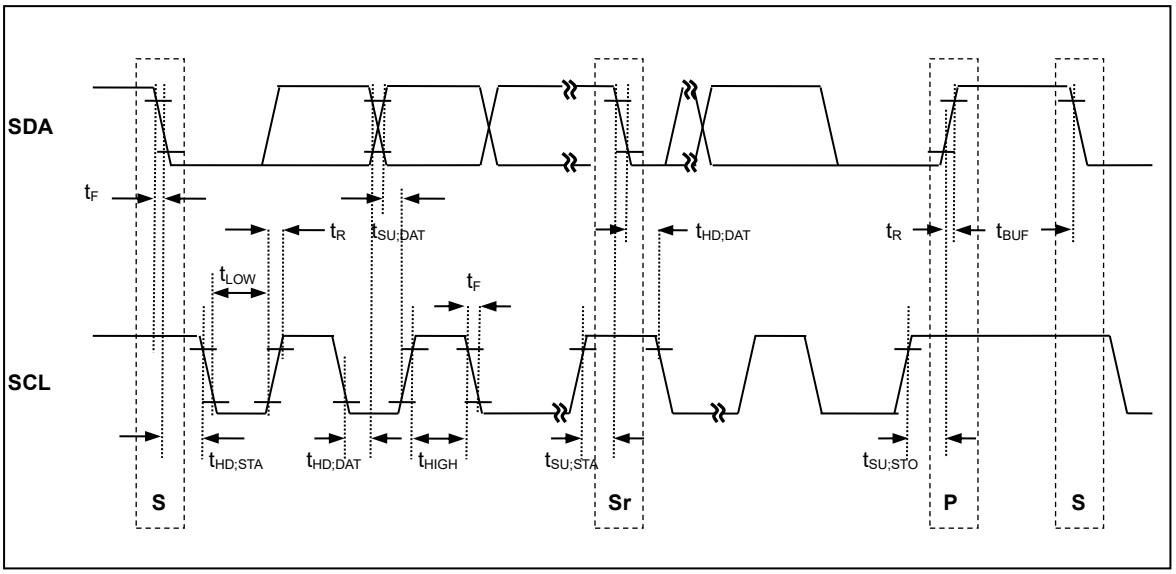


Figure 16.3. The timing of I2C interface bus

16.3 Characteristics of Analog Block

16.3.1 Power-On-Reset

A33G52x has a built-in Power-On Reset (POR) that monitors the internal voltage of VDD-Core and generates a reset signal for the MCU's cold start.

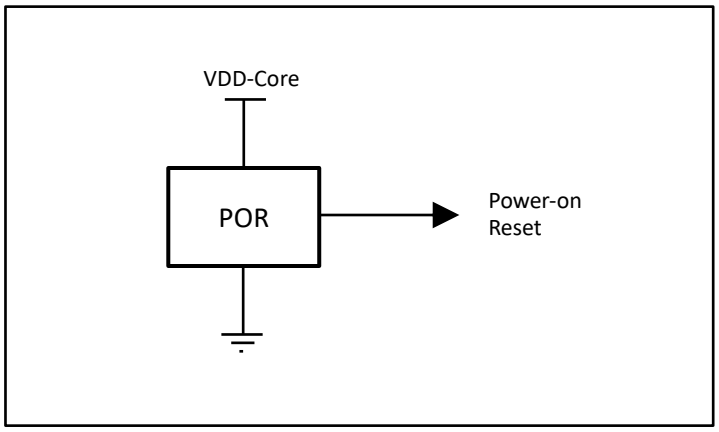


Figure 16.4. POR Block diagram

16.3.2 VDC (Voltage-Down Converter)

Built-in VDC generates the power regulated from external power for internal logics and analog block.

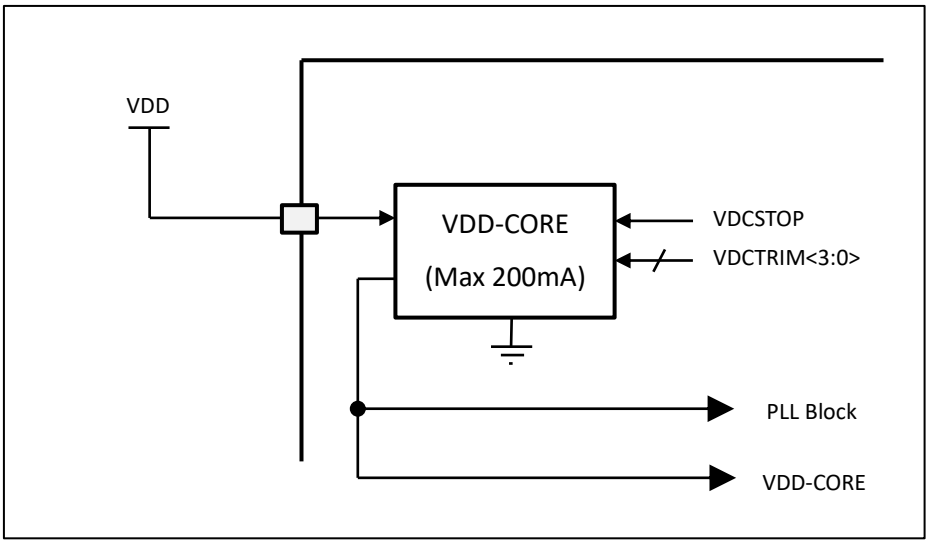


Figure 16.5. VDC Block diagram

16.3.3 LVD (Low Voltage Detector)

A33G52x has two built-in LVDs. Each LVD generate interrupt or reset depend on their settings. LVDs are monitoring external +5V power.
The configuration of LDCs is shown as follows.

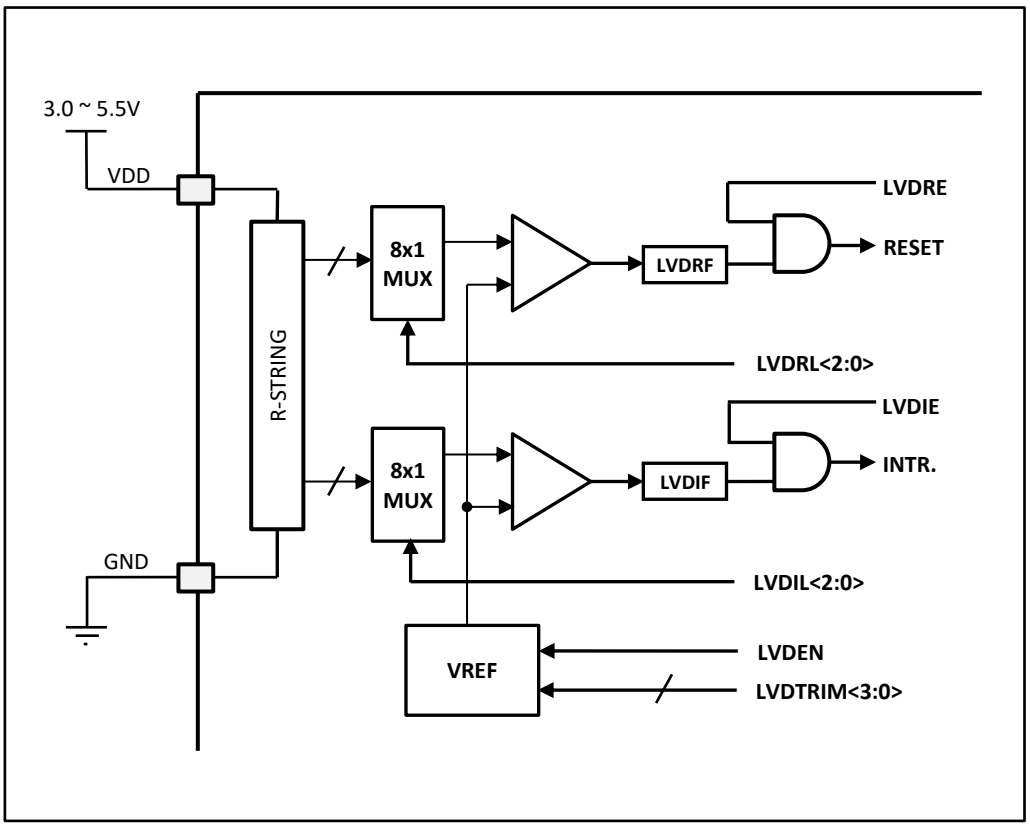


Figure 16.6. The Internal Configuration of LVDs

16.3.4 Internal Ring Oscillator (RingOSC/ROSC)

A33G52x has a simple ring oscillator to monitor system and supply to other peripherals. The Ring oscillator generates the frequency of 1MHz. It used for such as POR-Reset, WDT and clock monitoring. And for more smaller power consumption in the sleep mode, it used as the system operating clock. But ring oscillator is not desirable to be used in where need precise frequency due to the characteristics that ring oscillator is easily affected by the power and temperature.
The block diagram of the ring oscillator is shown as follows.

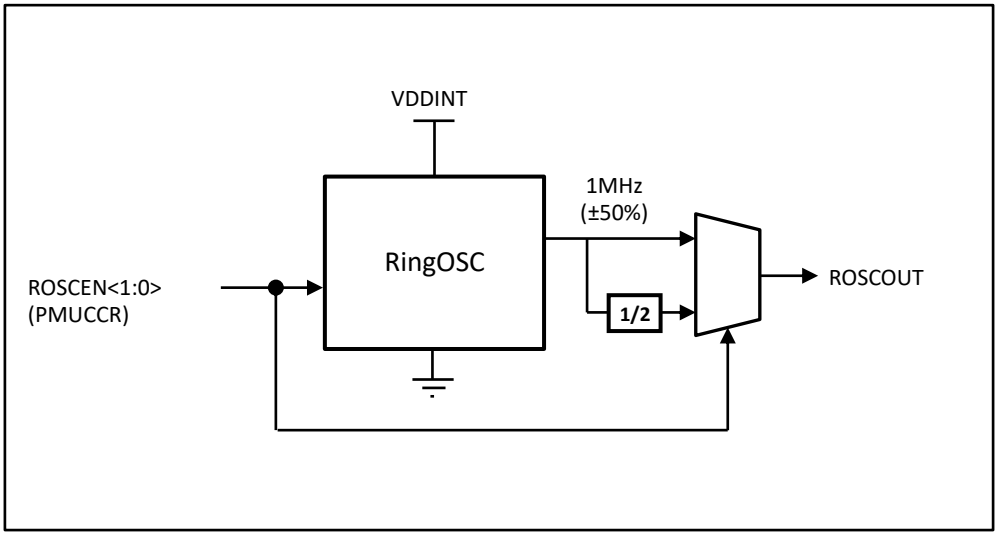


Figure 16.7. The Internal Configuration of RingOSC

16.3.5 Internal 16MHz Oscillator (IOSC16)

A33G52x has built-in 16MHz oscillator so that it can operate without any external clock.
The configuration of internal 16MHz oscillator is shown as follows

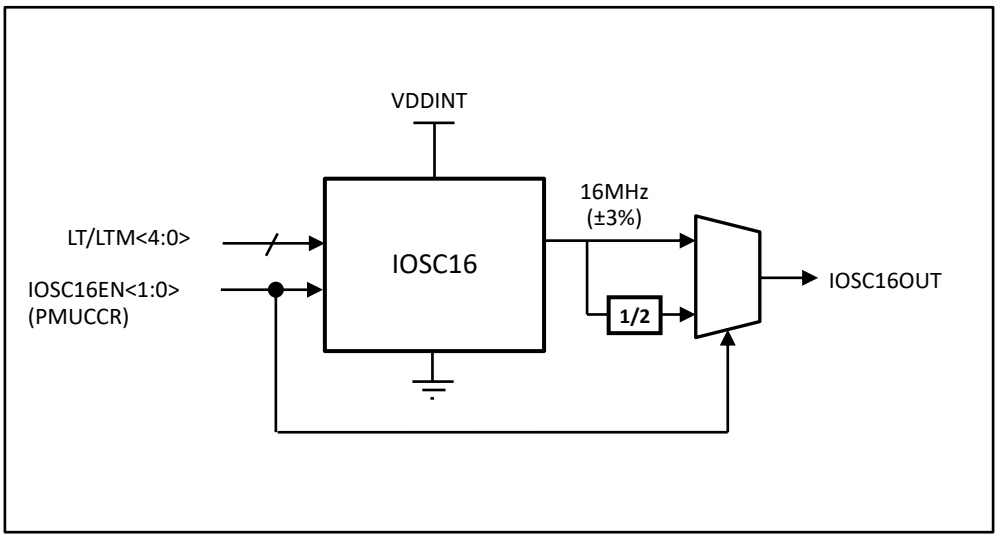


Figure 16.8. The Internal Configuration of IOSC16

16.3.6 PLL (Phase-Locked-Loop)

The built-in PLL can multiply internal or external clock to Max 75MHz. The PLL frequency synthesizer can be used to set the PLL output frequency up to 75MHz in 1MHz increments. The VDD-CORE power required for the PLL is supplied from inside the MCU.

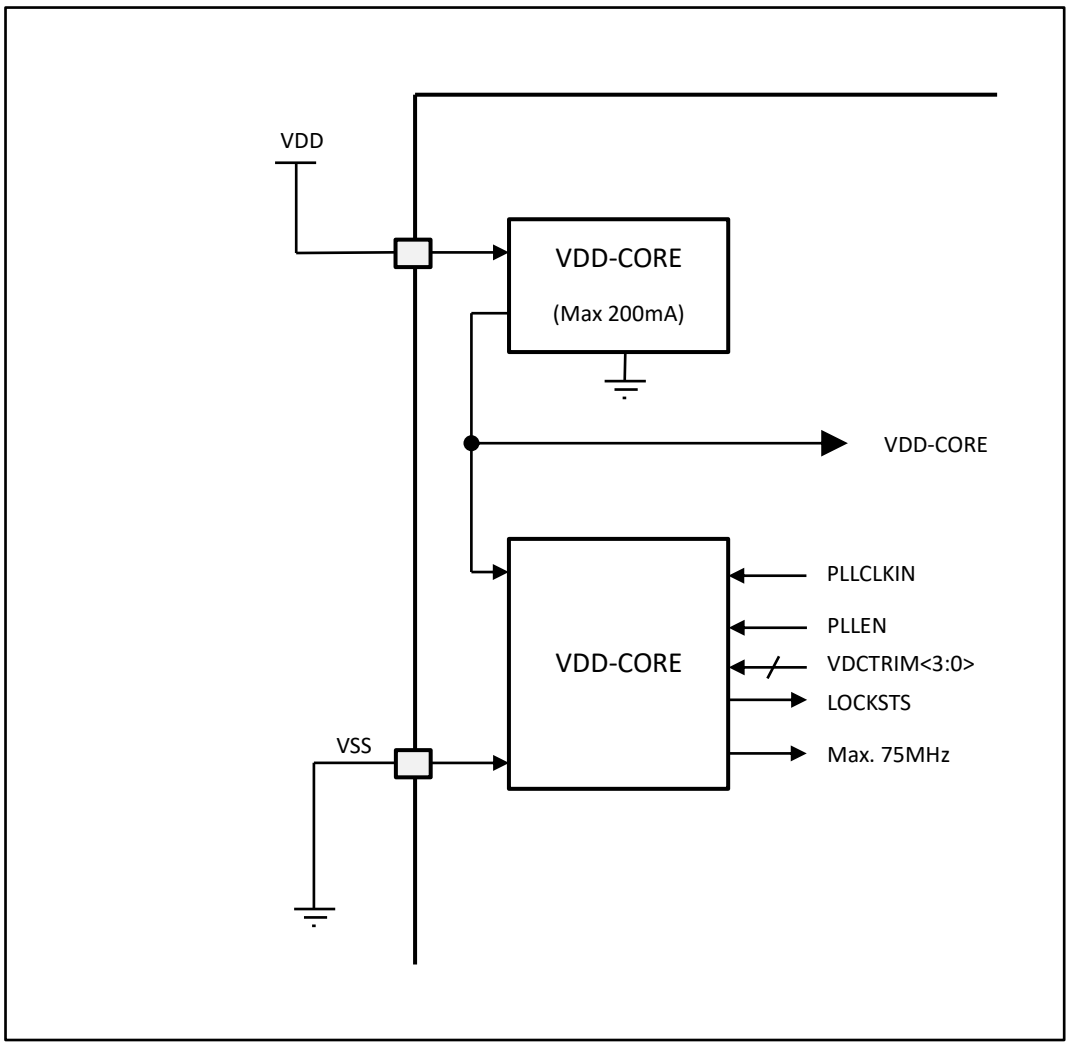


Figure 16.9. The Configuration of PLL

16.3.7 External Main and Sub Oscillator

A33G52x has a 4~10MHz main oscillator and a 32.768kHz suboscillator, which are crystal oscillators and designed for more immunity performance to electrical noises.
The configuration of the main and sub oscillator is shown as follows.

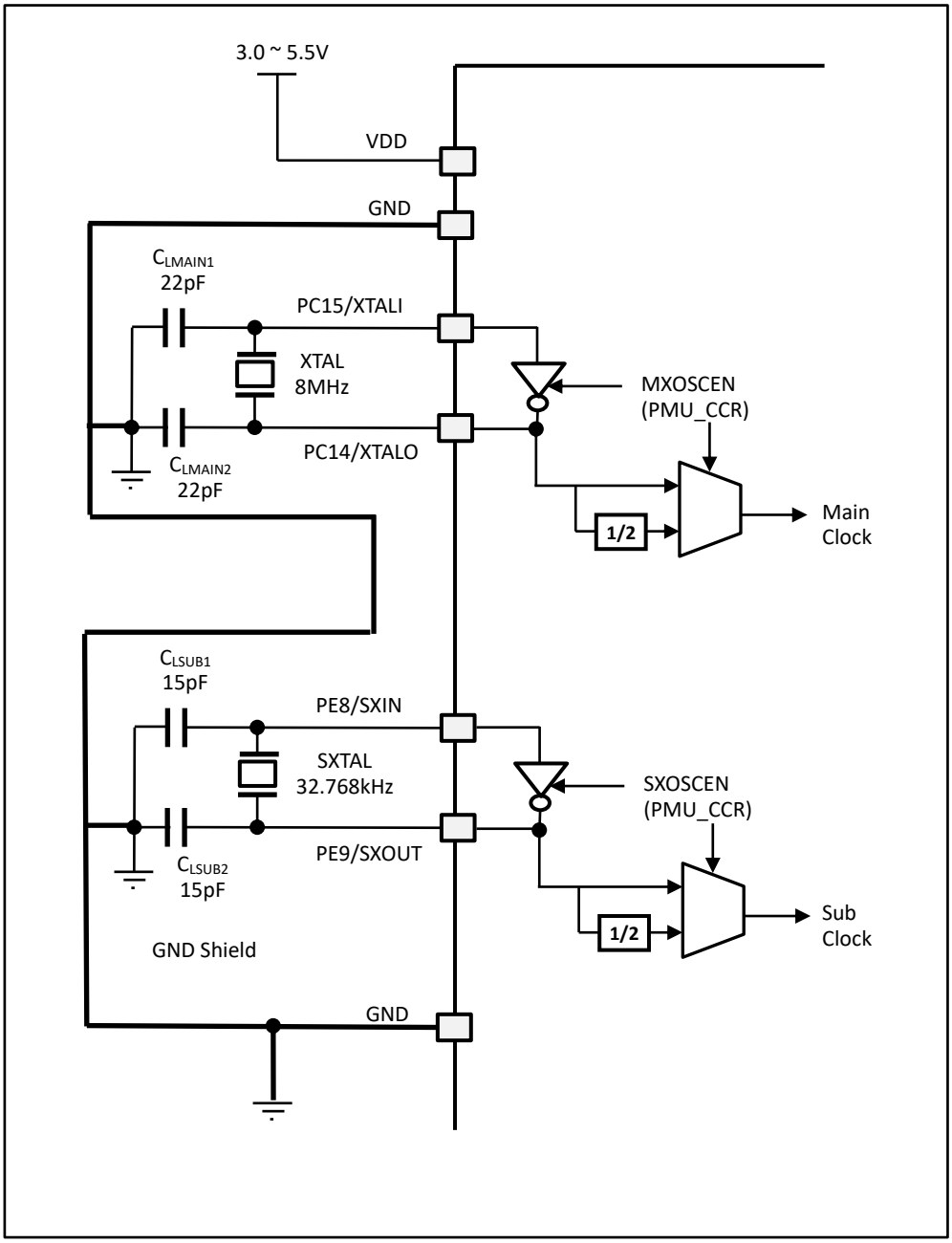


Figure 16.10. The Configuration of Main and Sub Oscillator

16.3.8 Power Configuration

The power configuration of A33G52x is shown as follows.

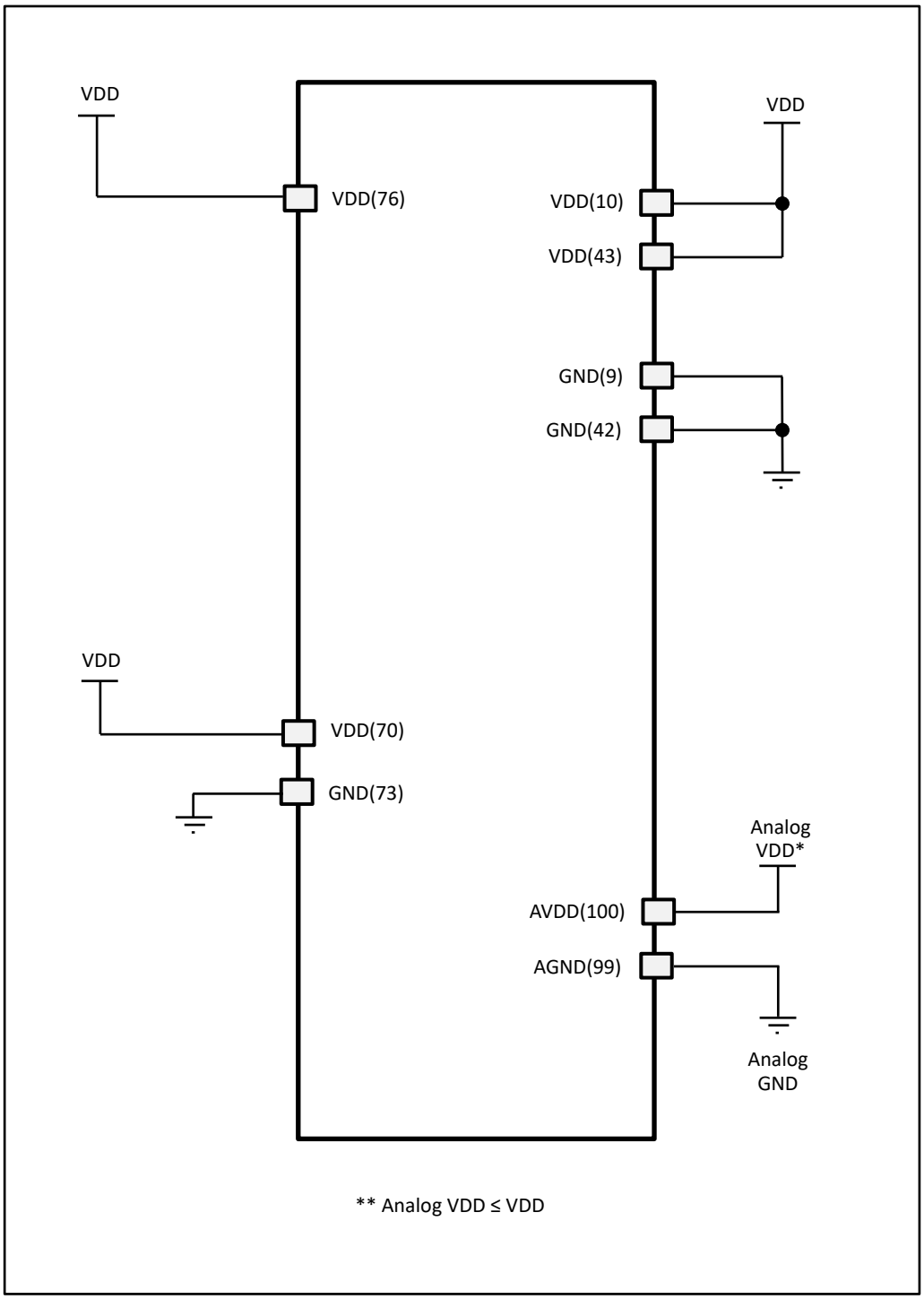


Figure 16.11. The Power Configuration of A33G52x (100MQFP)

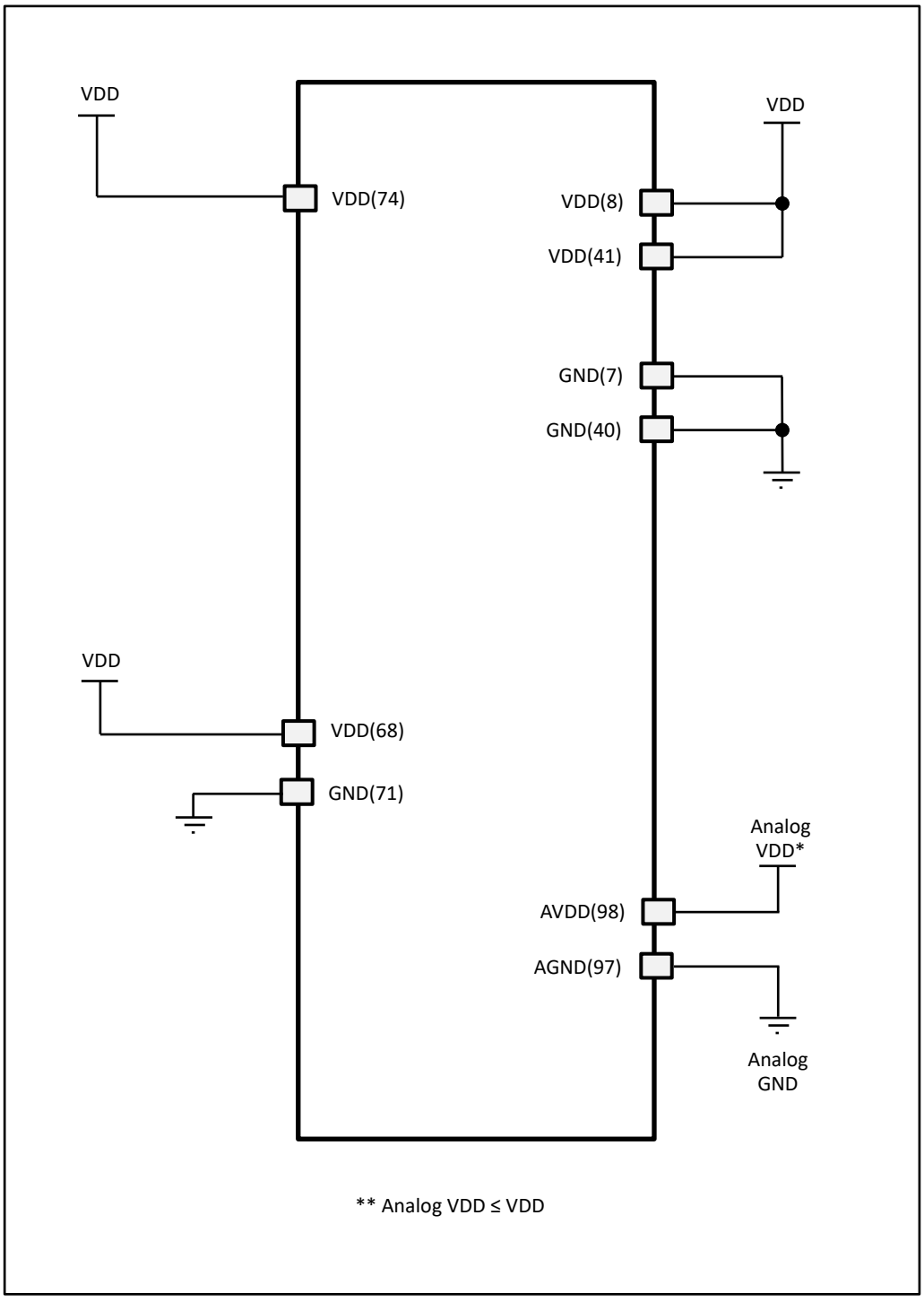


Figure 16.12. The Power Configuration of A33G52x (100LQFP14)

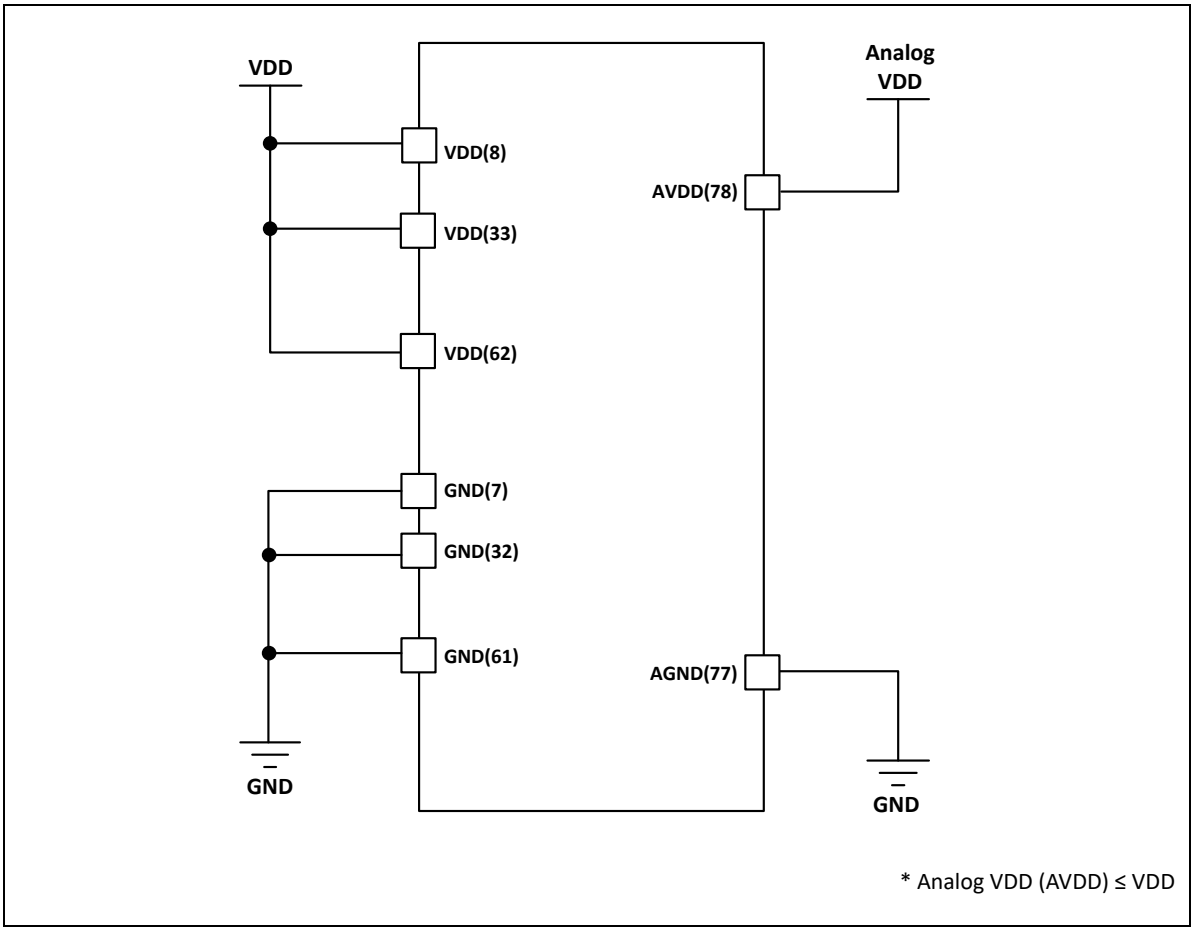


Figure 16.13. The Power Configuration of (80LQFP14/80LQFP12)

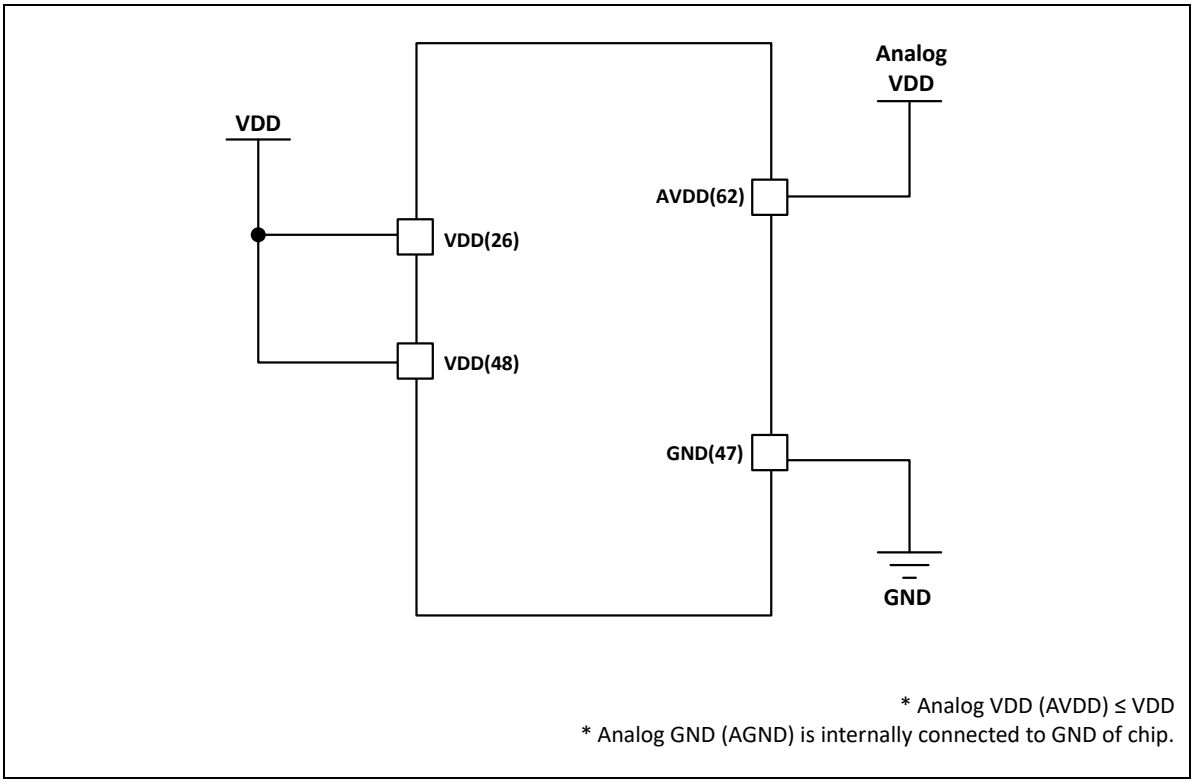


Figure 16.14. The Power Configuration of (64LQFP12/64LQFP10)

CHAPTER 17. Packages

17.1 Package Demension of 100MQFP

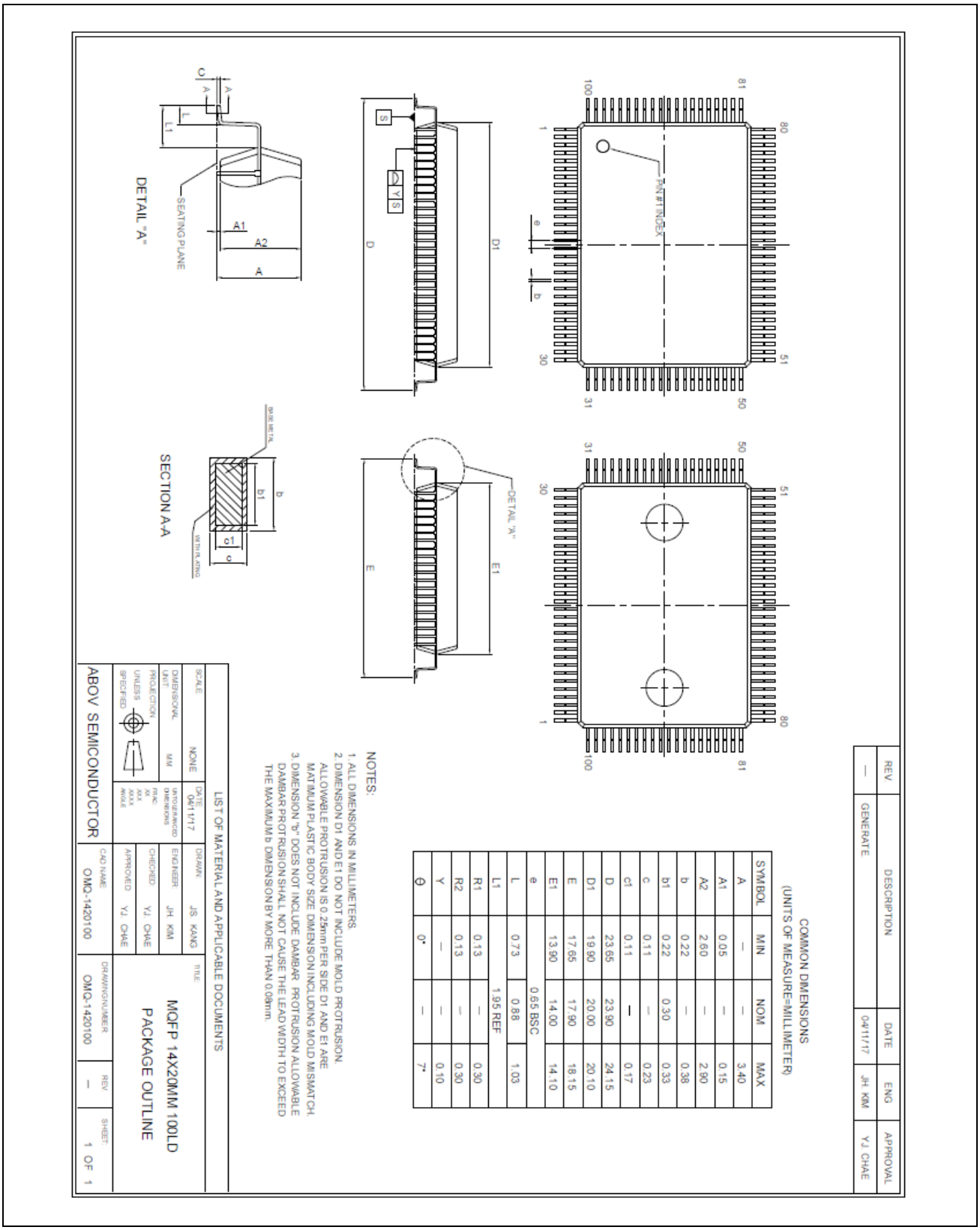


Figure 17.1. Package Dimension (100MQFP)

17.2 Package Demension of 100LQFP14

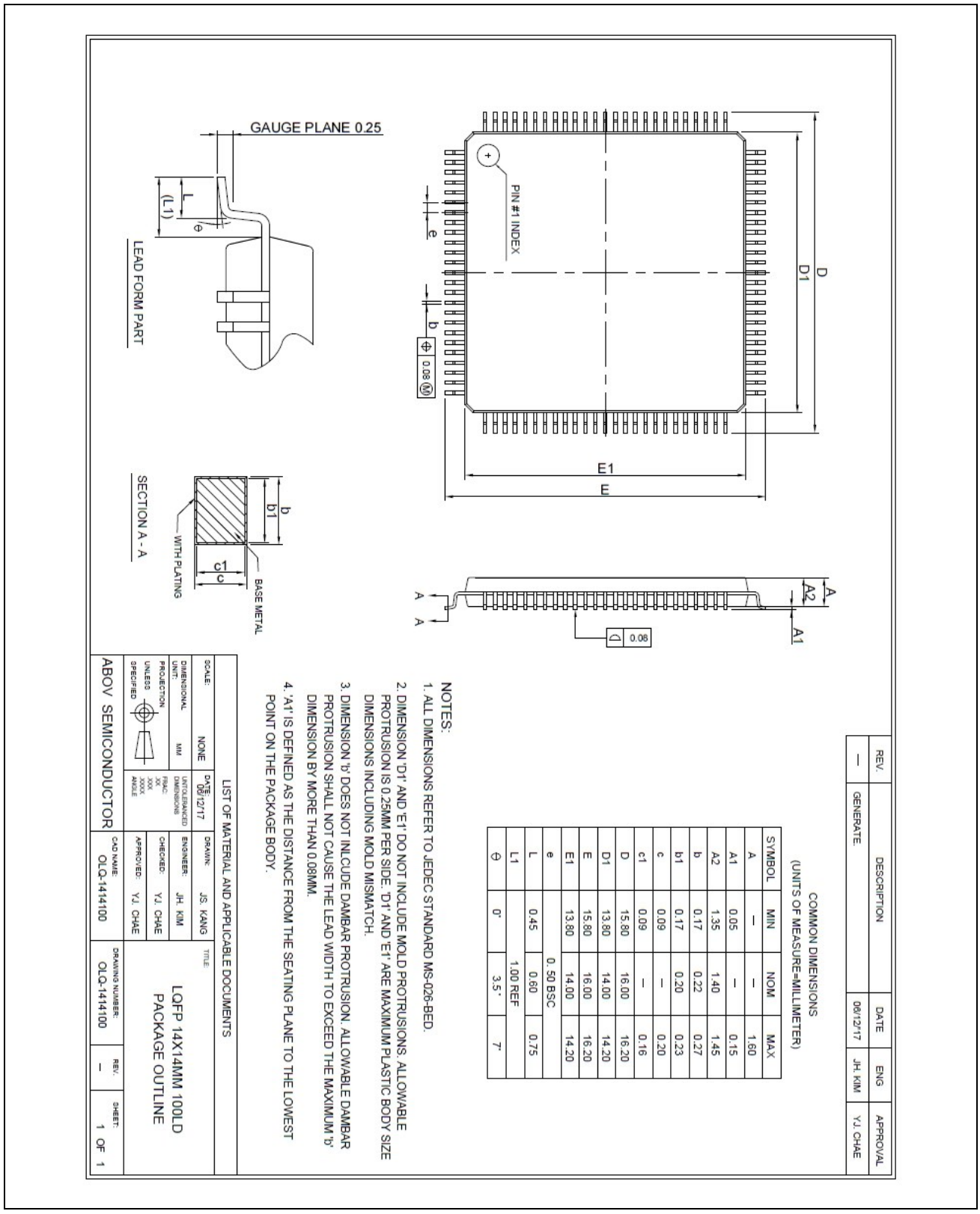


Figure 17.2. Package Dimension (100LQFP)

17.3 Package Demension of 80LQFP14

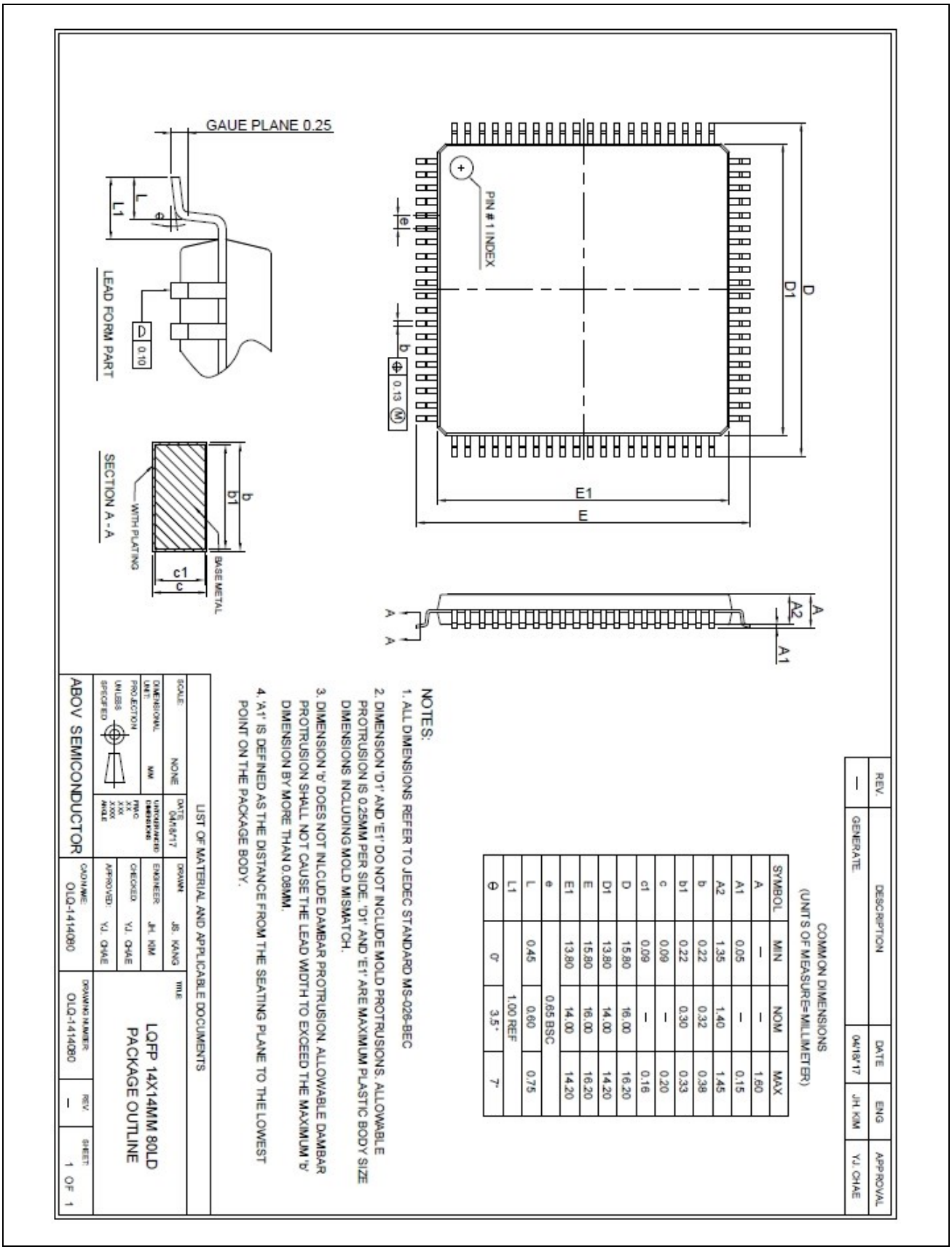


Figure 17.3. Package Dimension (80LQFP14)

17.4 Package Demension of 80LQFP12

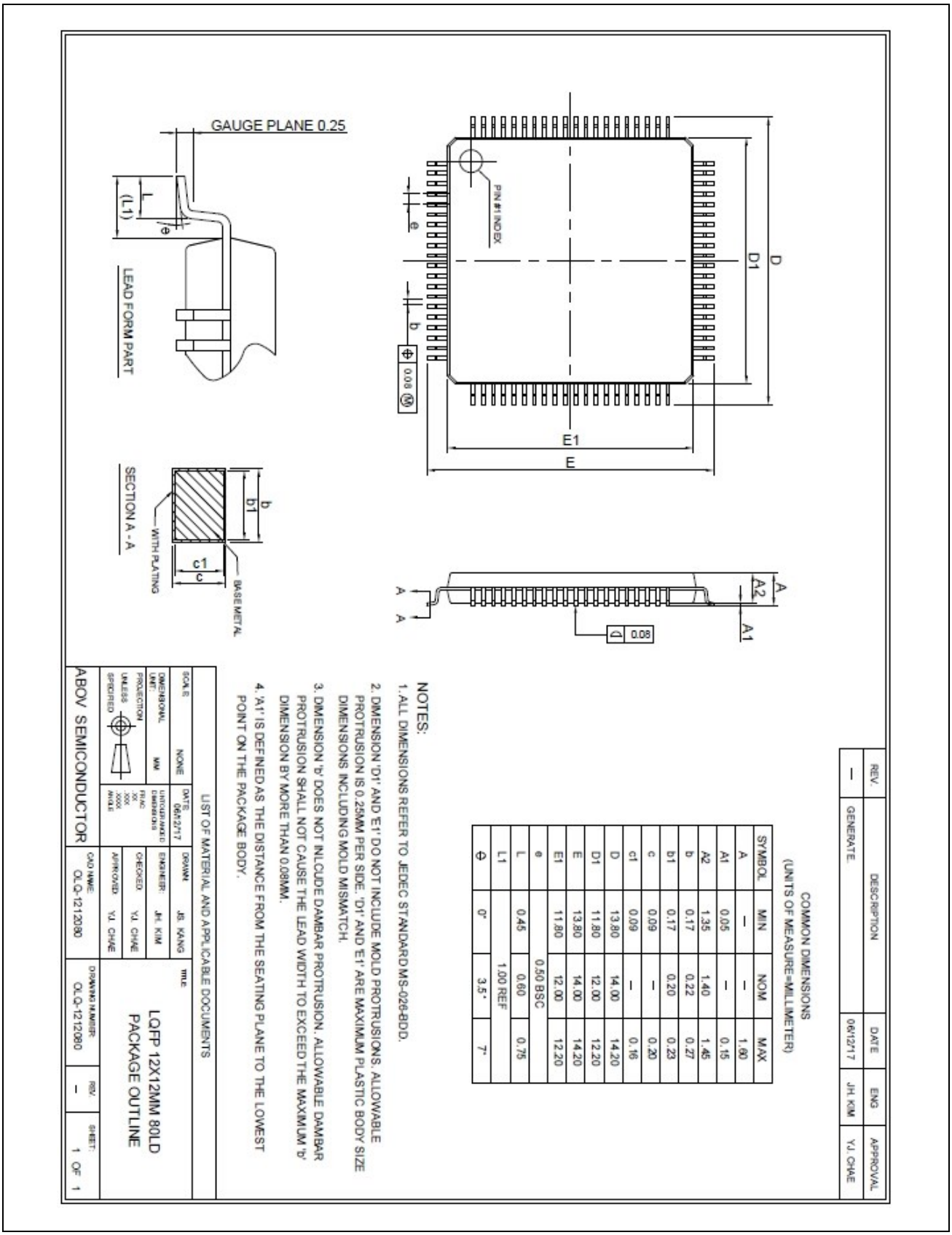


Figure 17.4. Package Dimension (80LQFP12)

17.5 Package Demension of 64LQFP12

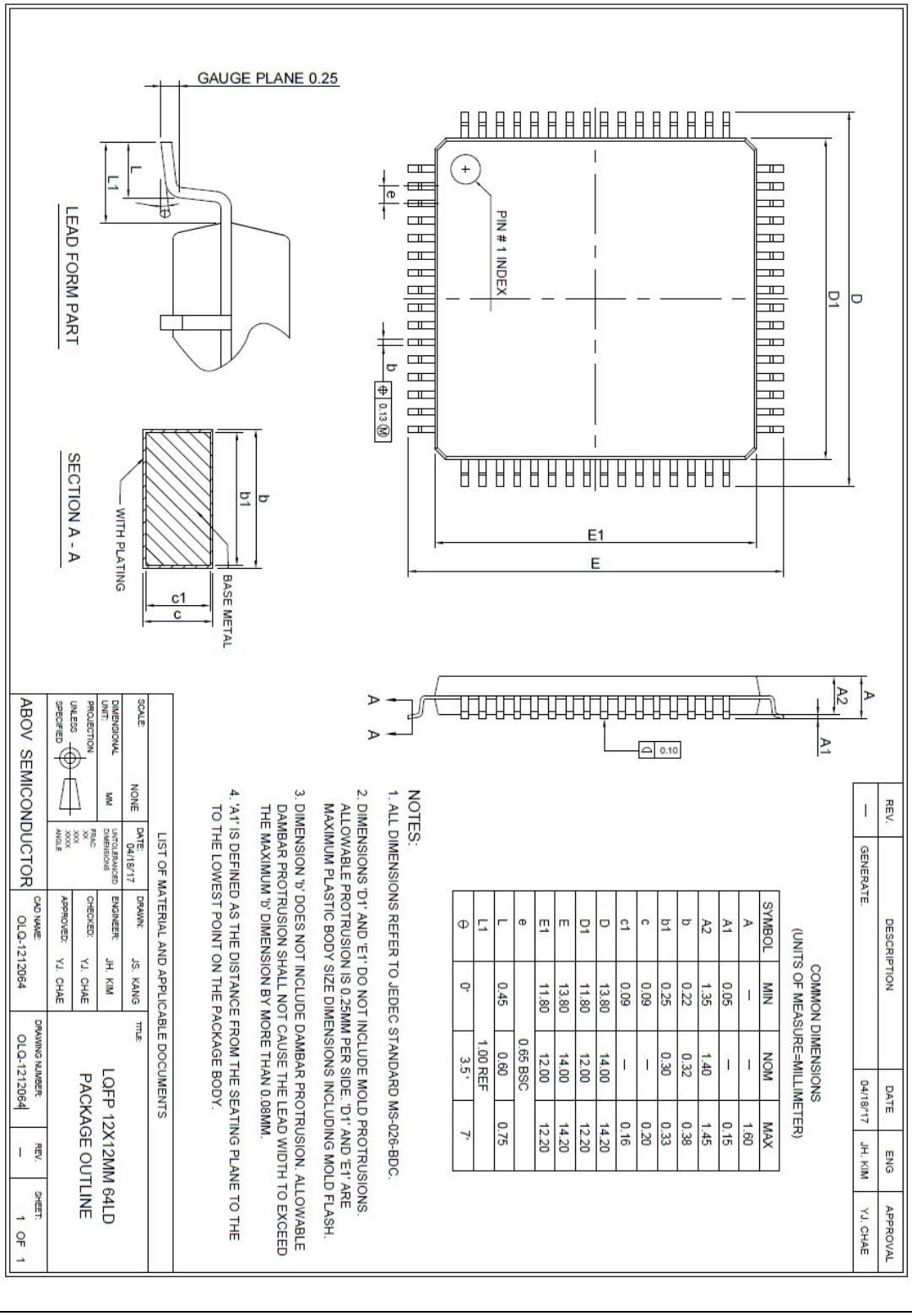


Figure 17.5. Package Dimension (64LQFP12)

17.6 Package Demension of 64LQFP10

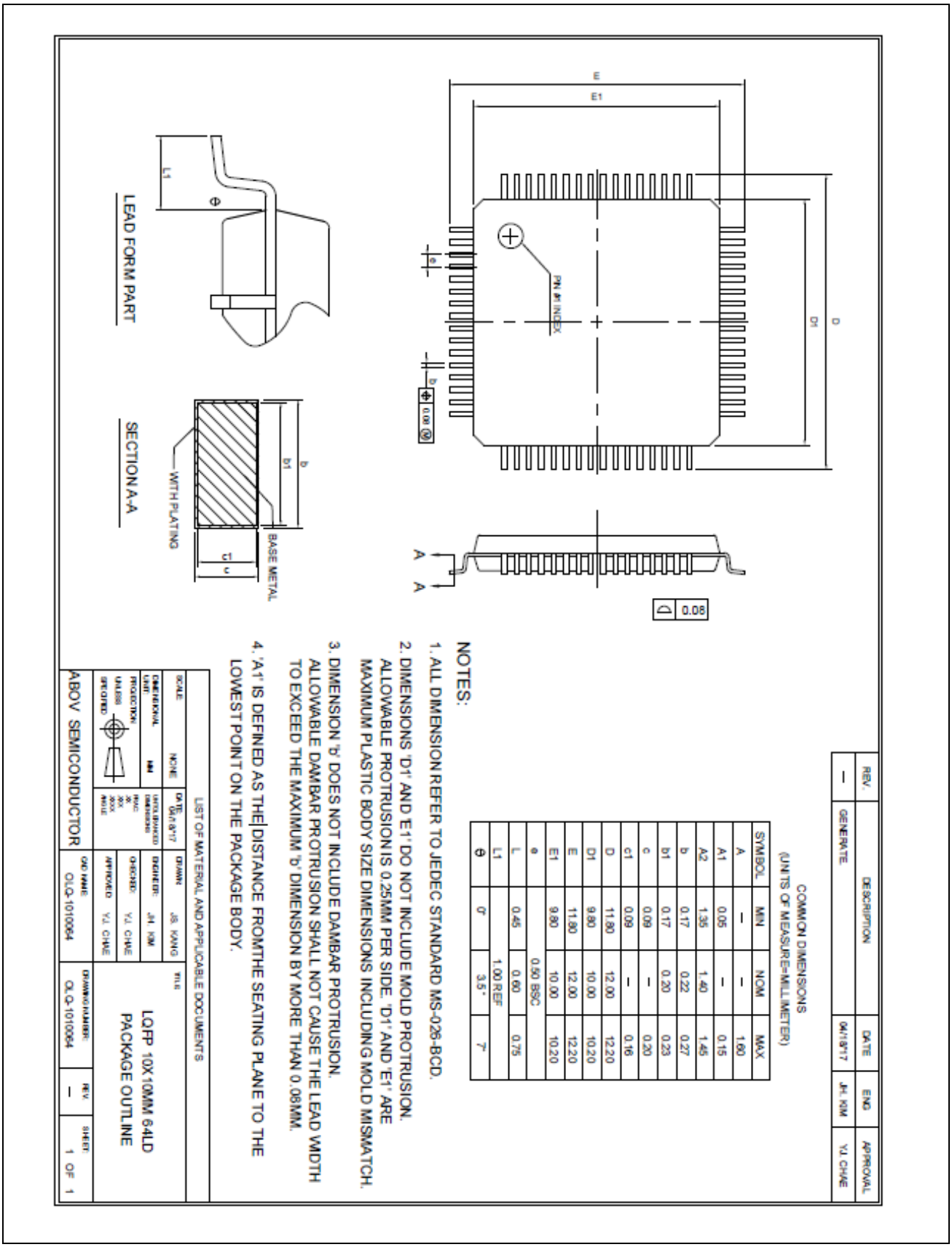


Figure 17.6. Package Dimension (64LQFP10)