16 MHz 8-bit A96G140/A96G148/A96A148 Microcontroller 64/32 Kbyte Flash memory, 12-bit ADC, 6 Timers, USART, USI, High Current Port

Datasheet Version 1.31

Features

Core

- 8-bit CISC M8051 core
  (8051 Compatible, 2 clocks per cycle)

64/32 Kbytes On-Chip FLASH

- Endurance : 30,000 times
- In-System Programming (ISP)

256 bytes IRAM / 2304 bytes XRAM

General Purpose I/O (GPIO)

Normal I/O : 46 Port (P0[7:0], P1[7:0], P2[7:0], P3[7:0], P4[7:0], P5[5:0])

- High sink current port : 8 ports P3[7:0]

Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watch Dog Timer (WDT) 8-bit × 1-ch
- 8-bit × 1-ch (T0)
- 16-bit × 5-ch (T1/T2/T3/T4/T5)

Programmable Pulse Generation

- Pulse generation (by T1/T2/T3/T4/T5)
- 8-bit PWM (by T0)

Watch Timer (WT)

- 3.91ms/0.25s/0.5s/1s /1min interval at 32.768kHz

Buzzer

- 8-bit × 1-ch

USI0/1 (USART + SPI + I2C)

- 8-bit USART × 2-ch or 8-bit SPI × 2-ch or I2C × 2-ch

USART2

- 8-bit USART × 1-ch or 8-bit SPI × 1-ch
- Receiver Time Out(RTO)
- 0% Error Baud Rate

12-bit A/D Converter

- 16 Input channels

Power On Reset

- Reset release level (1.32V)

Low Voltage Reset

- 16 levels detect
  (1.61/1.68/1.77/1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21/3.56/3.73/3.91/4.25V)

Low Voltage Indicator

- 13 levels detect
  (1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21/3.56/3.73/ 3.91/4.25V)

Interrupt Sources

- EINT0~7, EINT8, EINT10, EINT11, EINT12 (5)
- Timer(0/1/2/3/4/5) (6)
- WDT (1)
- BIT (1)
- WT (1)
- USART RX/TX (2)
- USI 2ch * RX/TX/I2C (6)
- ADC (1)
- LVI (1)

Internal RC Oscillator

- HSI 32MHz ±1.5% (TA= 0~ +55°C)
- HSI 32MHz ±2.0% (TA= -10~ +70°C)
- HSI 32MHz ±2.5% (TA=-40~ +85°C)
- HSI 32MHz ±5.0% (TA=-40~ +105°C)
- LSI 128kHz ±20% (TA= -40~ +85°C)
- LSI 128kHz ±30% (TA= -40~ +105°C)

Power Down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- 1.8V~ 5.5V (@32.768kHz Crystal)
- 2.2V~ 5.5V (@4 ~ 10MHz with Crystal)
- 2.4V~ 5.5V (@4 ~ 12MHz with Crystal)
- 1.8V~ 5.5V (@0.5 ~ 8.0MHz with Internal RC)
- 2.0V~ 5.5V (@0.5 ~ 16.0MHz with Internal RC)

16 MHz 8-bit A96G140/A96G148/A96A148 Microcontroller 64/32 Kbyte Flash memory, 12-bit ADC, 6 Timers, USART, USI, High Current Port

Minimum Instruction Execution Time

- 125ns (@16MHz main clock)
- 61us (@ 32.768kHz sub clock)

Operating temperature

- –40 ~ +85℃, –40 ~ +105℃

Oscillator Type

- 4 ~ 12MHz Crystal or Ceramic for main clock
- 32.768kHz Crystal for sub clock

Package Type

- 48 LQFP 7x7 mm, 48 QFN 6x6 mm
- 44 MQFP 10x10 mm
- 32 LQFP, 32 SOP
- 28 SOP, 28 TSSOP
- Pb-free package

Product selection table

Table 1. Device Summary

Part Number	Flash	XRAM	IRAM	Timer (PWM)	Communication function		ADC 12-bit (Channel)	GPIO	High Current Port	Package	Temperature Range
					USI	USART					
A96G140CL	64KB	2304 bytes	256 bytes	6	2	1	16	46	8	48 LQFP	-40°C ~ 85°C
A96G140CU				6	2	1	16	46	8	48 QFN	
A96G140SQ				6	2	1	16	42	8	44 MQFP	
A96G140KN				6	2	0	12	30	4	32 LQFP	
A96G140KD*				6	2	0	12	30	4	32 SOP	
A96G140GD*				6	2	0	11	26	4	28 SOP	
A96G140GR*				6	2	0	11	26	4	28 TSSOP	
A96G140CL2	64KB	2304 bytes	256 bytes	6	2	1	16	46	8	48 LQFP	-40°C ~ 105°C
A96G140CU2				6	2	1	16	46	8	48 QFN	
A96G140SQ2				6	2	1	16	42	8	44 MQFP	
A96G140KN2				6	2	0	12	30	4	32 LQFP	
A96G140KD2*				6	2	0	12	30	4	32 SOP	
A96G140GD2*				6	2	0	11	26	4	28 SOP	
A96G140GR2*				6	2	0	11	26	4	28 TSSOP	

16 MHz 8-bit A96G140/A96G148/A96A148 Microcontroller 64/32 Kbyte Flash memory, 12-bit ADC, 6 Timers, USART, USI, High Current Port

Table 1. Device Summary (Continued)

Part Number	Flash	XRAM	IRAM	Timer (PWM)	Communication function		ADC 12-bit (Channel)	GPIO	High Current Port	Package	Temperature Range
					USI	USART					
A96G148CL*	32KB	2304 bytes	256 bytes	6	2	1	16	46	8	48 LQFP	-40°C ~ 85°C
A96G148CU*				6	2	1	16	46	8	48 QFN	
A96G148SQ*				6	2	1	16	42	8	44 MQFP	
A96G148KN*				6	2	0	12	30	4	32 LQFP	
A96G148KD*				6	2	0	12	30	4	32 SOP	
A96G148GD*				6	2	0	11	26	4	28 SOP	
A96G148GR				6	2	0	11	26	4	28 TSSOP	
A96A148GD				6	2	0	10	26	8	28 SOP	
A96G148CL2*	32KB	2304 bytes	256 bytes	6	2	1	16	46	8	48 LQFP	-40°C ~ 105°C
A96G148CU2*				6	2	1	16	46	8	48 QFN	
A96G148SQ2*				6	2	1	16	42	8	44 MQFP	
A96G148KN2*				6	2	0	12	30	4	32 LQFP	
A96G148KD2*				6	2	0	12	30	4	32 SOP	
A96G148GD2*				6	2	0	11	26	4	28 SOP	
A96G148GR2				6	2	0	11	26	4	28 TSSOP	
A96A148GD2				6	2	0	10	26	8	28 SOP	

* For available options or further information on the devices with “*” marks, please contact the ABOV sales offices.

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1 Description

A96G140/A96G148/A96A148 is an advanced CMOS 8-bit microcontroller with 64/32Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A96G140/A96G148/A96A148 and peripheral counts are introduced.

Table 2. A96G140/A96G148/A96A148 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	8-bit CISC core (M8051, 2 clocks per cycle)
	Interrupt	Up to 23 peripheral interrupts supported. • EINT0 to 7, EINT8, EINT10, EINT11, EINT12 (5) • Timer (0/1/2/3/4/5) (6) • WDT (1) • BIT (1) • WT (1) • USART Rx/Tx (2) • USI 2-ch. *Rx/Tx/I2C (6) • ADC (1) • LVI (1)
Memory	ROM (FLASH) capacity	• 64/32 Kbytes FLASH with self-read and write capability • In-system programming (ISP) • Endurance: 30,000times
	IRAM	256Bytes
	XRAM	2304Bytes
Programmable pulse generation		• Pulse generation (by T1/T2/T3/T4/T5) • 8-bit PWM (by T0)
Buzzer		8-bit × 1-ch
Minimum instruction execution time		• 125ns (@ 16MHz main clock) • 61us (@ 32.768kHz sub clock)
Power down mode		• STOP mode • IDLE mode
General Purpose I/O (GPIO)		• Normal I/O: 46ports • High sink current port: 8ports P3[7:0]

Table 2. A96G140/A96G148/A96A148 Device Features and Peripheral Counts (continued)

Peripherals		Description
Reset	Power on reset	Reset release level: 1.2V
	Low voltage reset	• 16 levels detect • 1.61/1.68/1.77/1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21/3.56/3.73/3.91/4.25V
Low voltage indicator		• 13 levels detect • 1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21/3.56/3.73/3.91/4.25V
Watch Timer (WT)		3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Watchdog timer (WDT) 8-bit x 1-ch. • 8-bit x 1-ch (T0), 16-bit x 5-ch (T1/T2/ T3/T4/T5)
Communication function	USART2	• 8-bit USART x 1-ch or 8-bit SPI x 1-ch • Receiver timer out (RTO) • 0% error baud rate
	USI0/1	• USART + SPI + I2C • 8-bit USART x 2-ch or 8-bit SPI x 2-ch or I2C x 2-ch
12-bit A/D converter		16 input channels
Oscillator type		• 4MHz to 12MHz crystal or ceramic for main clock • 32.768kHz Crystal for sub clock
Internal RC oscillator		• HSI 32MHz ±1.5% (T_A= 0~ +50°C) • HSI 32MHz ±2.0% (T_A=-10~ +70°C) • HSI 32MHz ±2.5% (T_A=-40~ +85°C) • HSI 32MHz ±5.0% (T_A=-40~ +105°C) • LSI 128kHz ±20% (T_A= -40~ +85°C) • LSI 128kHz ±30% (T_A= -40~ +105°C)
Operating voltage and frequency		• 1.8V to 5.5V @ 32.768kHz with crystal • 2.2V to 5.5V @ 4MHz to 10MHz with crystal • 2.4V to 5.5V @ 4MHz to 12MHz with crystal • 1.8V to 5.5V @ 0.5MHz to 8.0MHz with internal RC • 2.0V to 5.5V @ 0.5MHz to 16.0MHz with internal RC
Operating temperature		-40℃ to +85℃, -40℃ to +105℃

Table 2. A96G140/A96G148/A96A148 Device Features and Peripheral Counts (continued)

Peripherals	Description
Package	• Pb-free packages • 48 LQFP 7x7 mm, 48 QFN 6x6 mm • 44 MQFP 10x10 mm • 32 LQFP, 32 SOP • 28 SOP, 28 TSSOP

1.2 A96G140/A96G148/A96A148 block diagram

In this section, A96G140/A96G148/A96A148 device with peripherals are described in a block diagram.

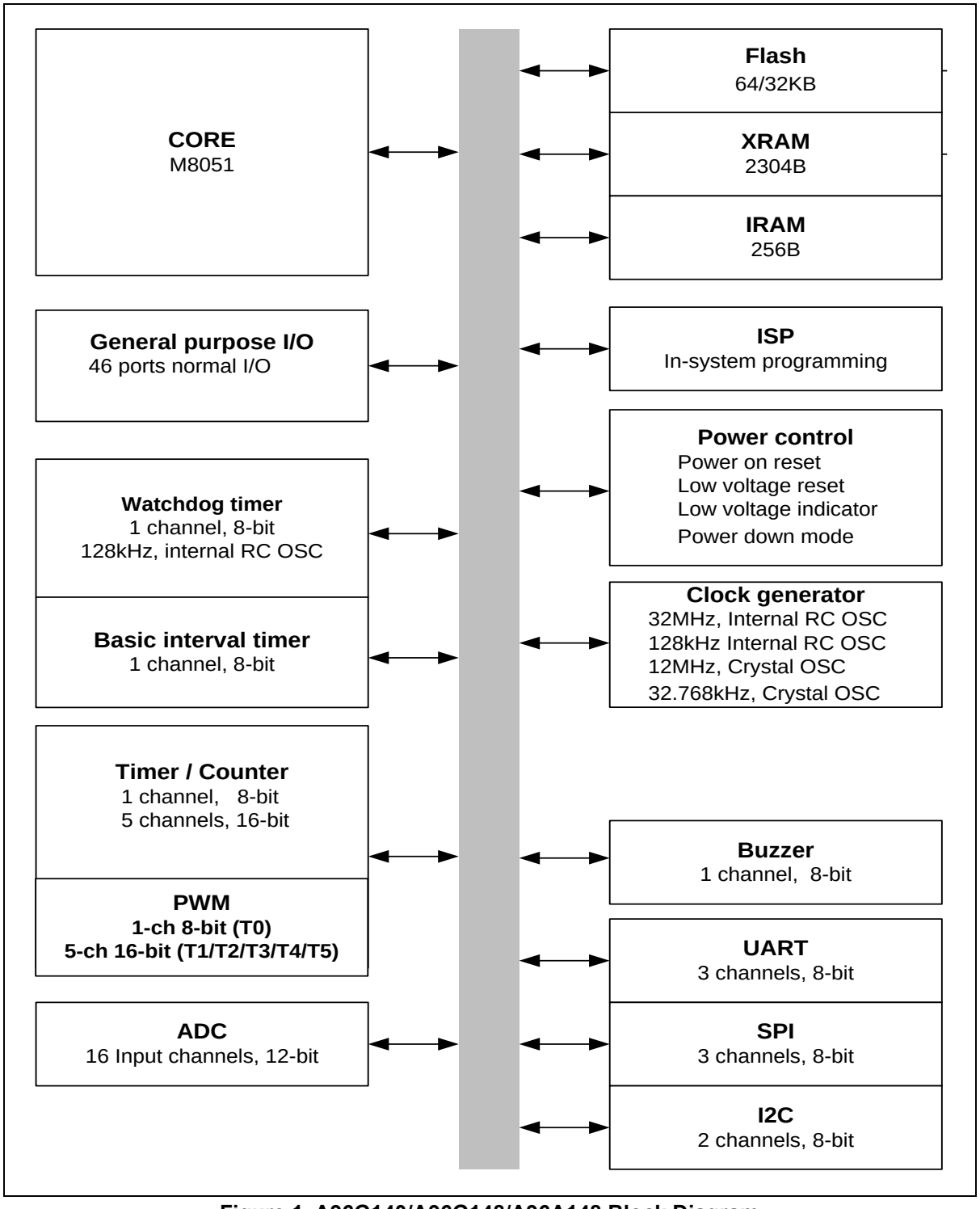
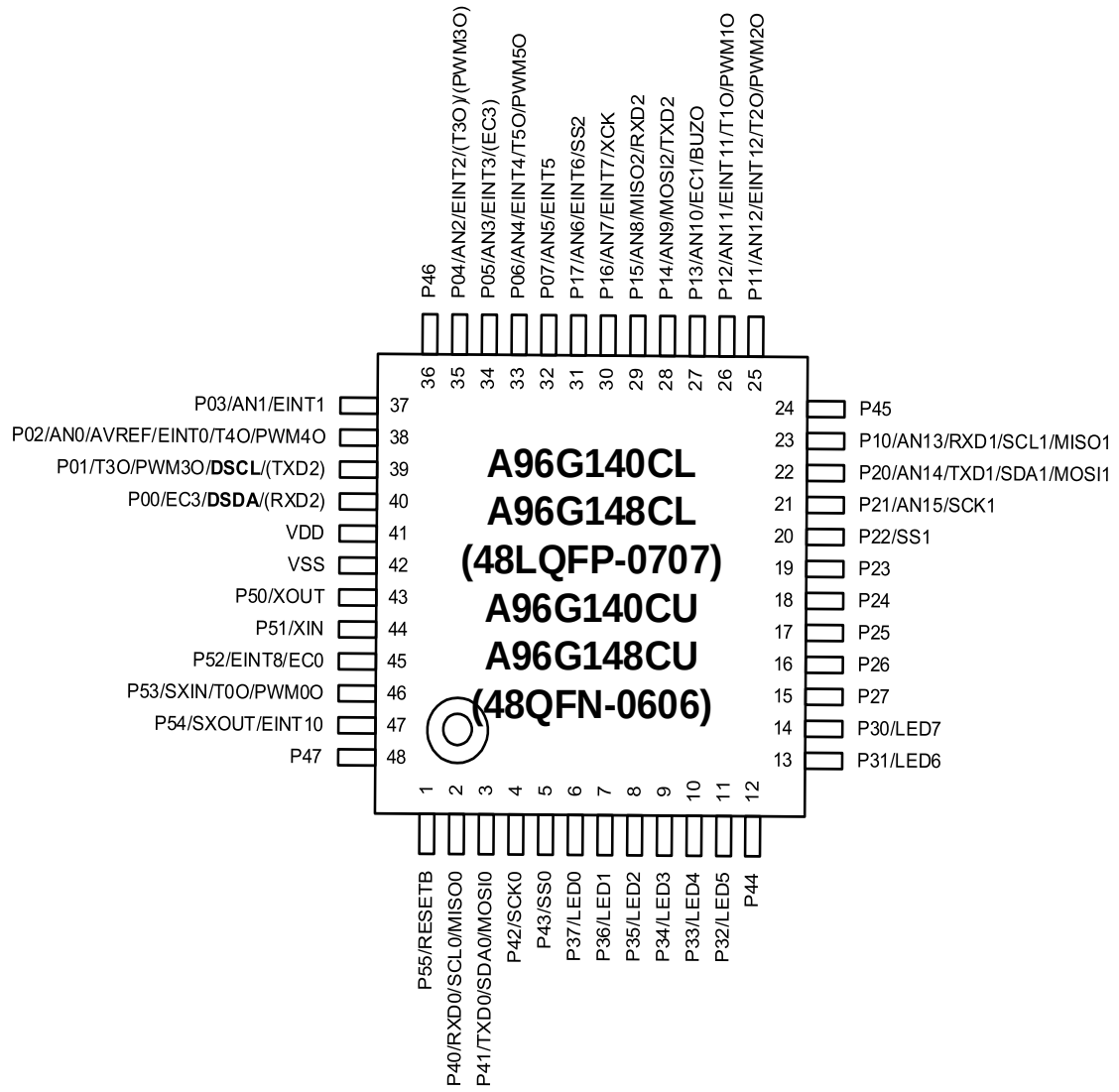


Figure 1. A96G140/A96G148/A96A148 Block Diagram

2 Pinouts and pin description

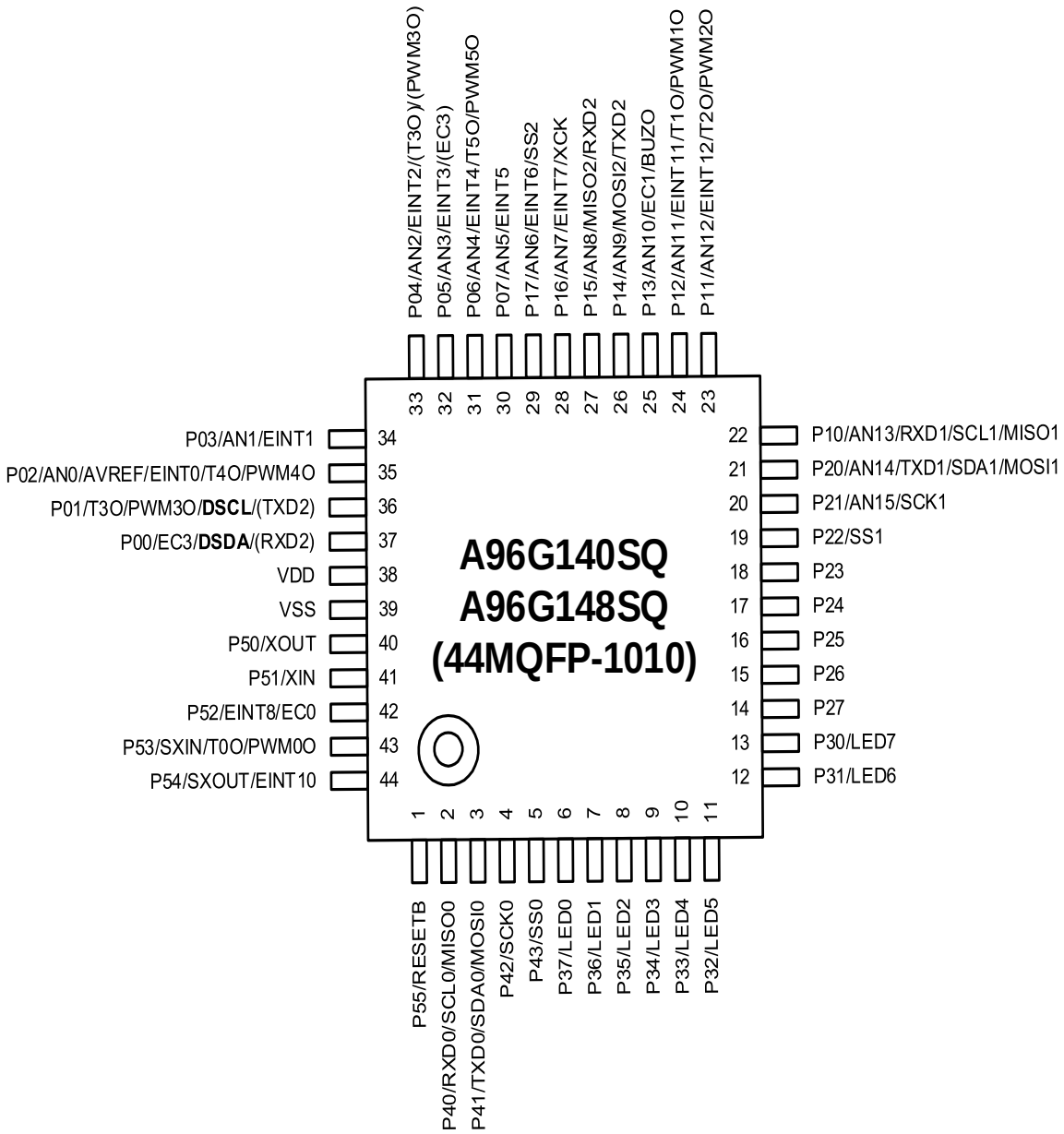
In this chapter, A96G140/A96G148/A96A148 device pinouts and pin descriptions are introduced.

2.1 Pinouts



NOTE: Programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.

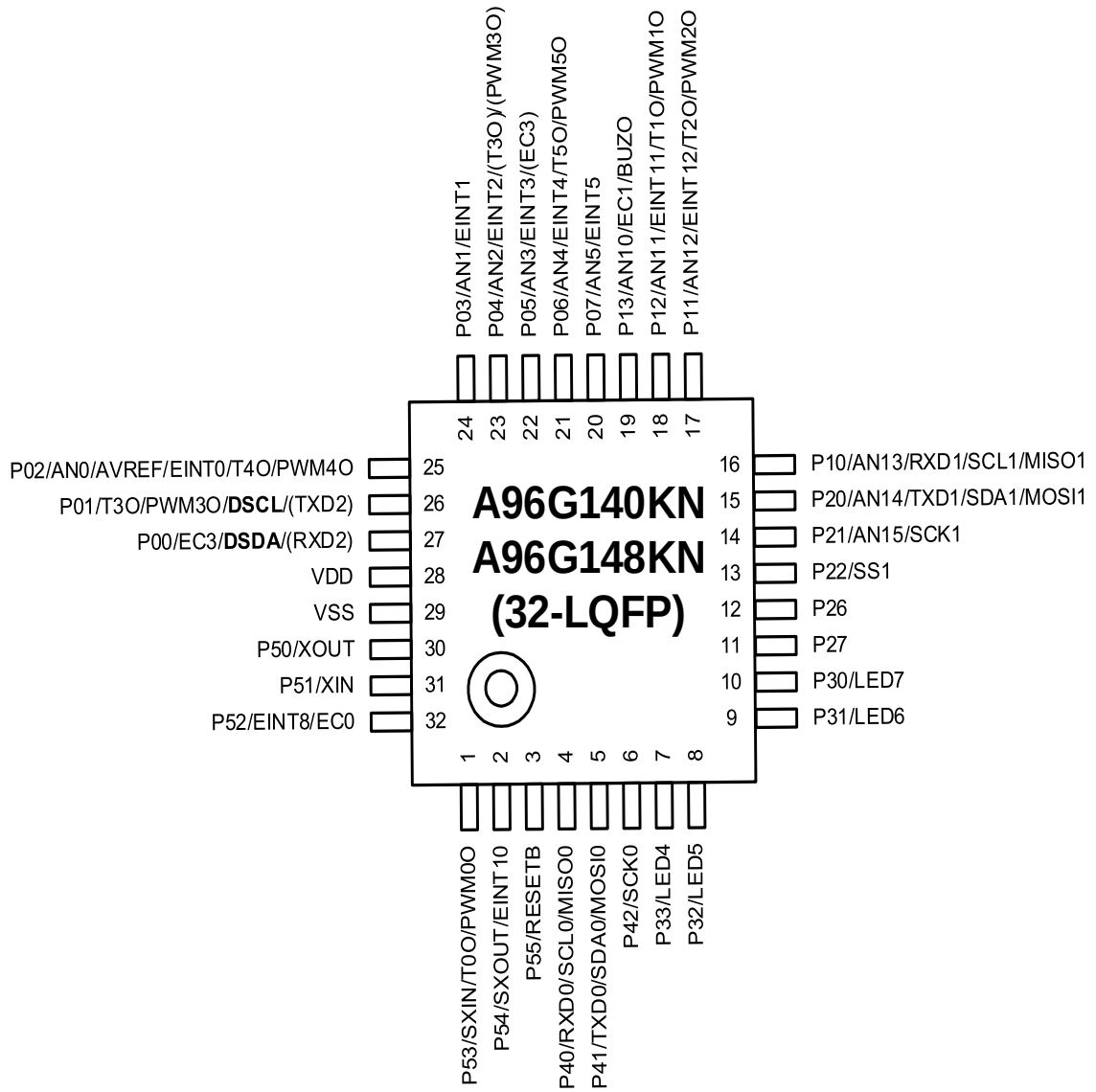
Figure 2. A96G140/A96G148 48LQFP/48QFN Pin Assignment



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P44-P47 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 44-pin package is used.

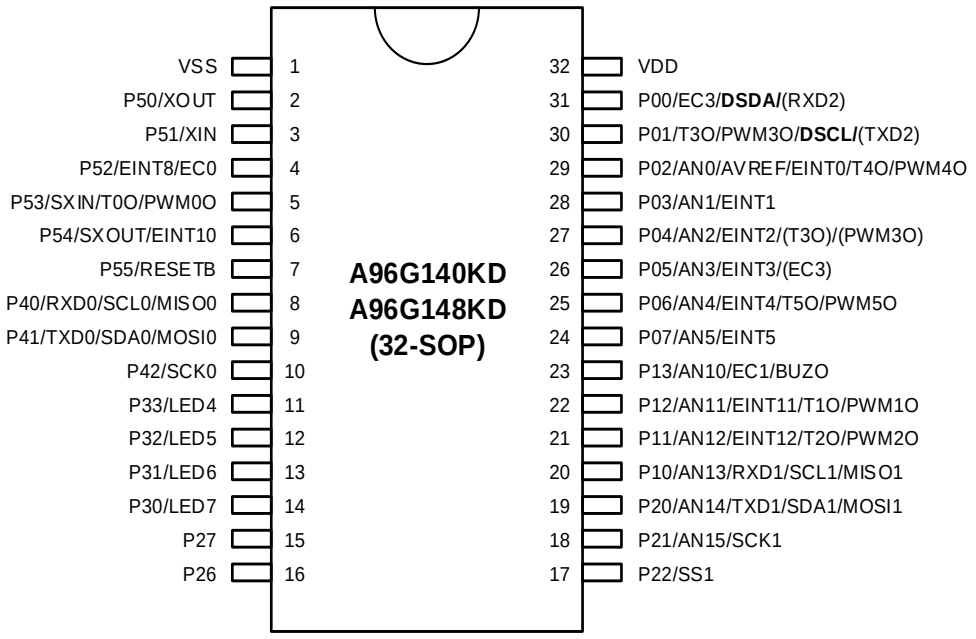
Figure 3. A96G140/A96G148 44MQFP-1010 Pin Assignment



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P14-P17, P23-P25, P34-P37 and P43-P47 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 32-pin package is used.

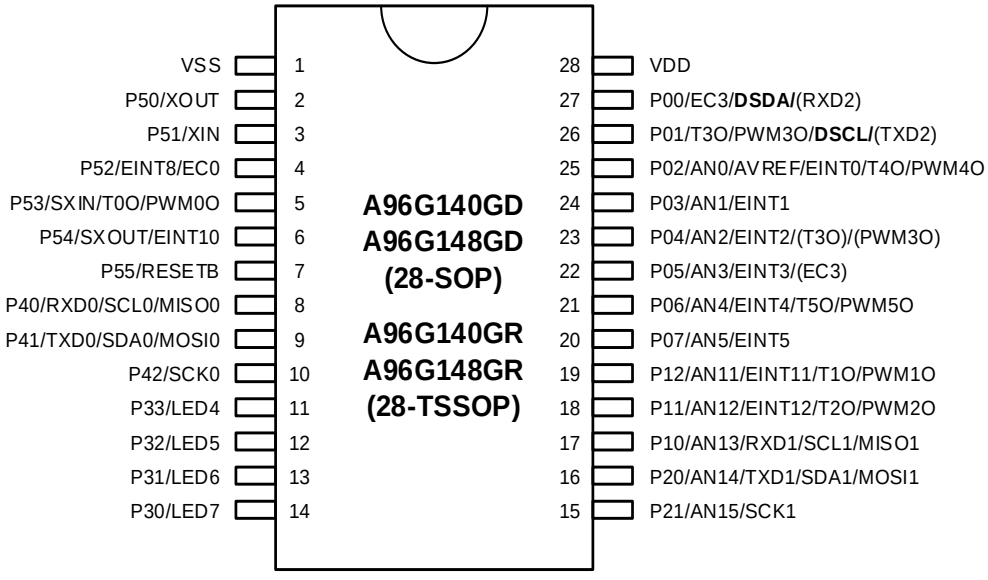
Figure 4. A96G140/A96G148 32LQFP Pin Assignment



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P14-P17, P23-P25, P34-P37 and P43-P47 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 32-pin package is used.

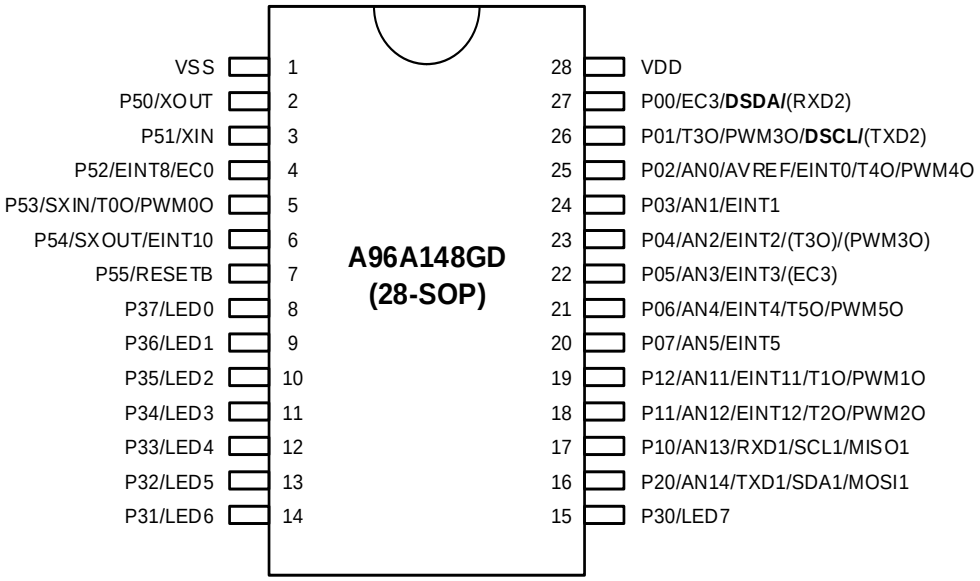
Figure 5. A96G140/A96G148 32SOP Pin Assignment



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P13-P17, P22-P27, P34-P37 and P43-P47 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 28-pin package is used.

Figure 6. A96G140/A96G148 28SOP Pin Assignment



NOTES:

3. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
4. The P13-P17, P22-P27, P34-P37 and P43-P47 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 28-pin package is used.

Figure 7. A96A148 28SOP Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

Pin no.						PIN Name	I/O(1)	Description	Remark
48	44	32 LQFP	32 SOP	28	28 A96A148				
40	37	27	31	27	27	P00*	IOUS	Port 0 bit 0 Input/output	
						EC3	I	Timer 3(Event Capture) input	
						DSDA	IOU	OCD debugger data input/output	Pull-up
						RXD2	I	USART2 data receive/SPI MISO	
39	36	26	30	26	26	P01*	IOUS	Port 0 bit 1 Input/output	
						T3O	O	Timer 3 interval output	
						PWM3O	O	Timer 3 PWM output	
						DSCL	IOU	OCD debugger clock	Pull-up
						TXD2	O	USART2 data transmit/SPI MOSI	
38	35	25	29	25	25	P02*	IOUS	Port 0 bit 2 Input/output	
						AN0	IA	ADC input ch-0	
						AVREF	P	A/D converter reference voltage	
						EINT0	I	External interrupt input ch-0	
						T4O	O	Timer 4 interval output	
						PWM4O	O	Timer 4 PWM output	
37	34	24	28	24	24	P03*	IOUS	Port 0 bit 3 Input/output	
						AN1	IA	ADC input ch-1	
						EINT1	I	External interrupt input ch-1	
35	33	23	27	23	23	P04*	IOUS	Port 0 bit 4 Input/output	
						AN2	IA	ADC input ch-2	
						EINT2	I	External interrupt input ch-2	
						T3O	O	Timer 3 interval output	
						PWM3O	O	Timer 3 PWM output	
34	32	22	26	22	22	P05*	IOUS	Port 0 bit 5 Input/output	
						AN3	IA	ADC input ch-3	
						EINT3	I	External interrupt input ch-3	
						EC3	I	Timer 3(Event Capture) input	
33	31	21	25	21	21	P06*	IOUS	Port 0 bit 6 Input/output	
						AN4	IA	ADC input ch-4	
						EINT4	I	External interrupt input ch-4	
						T5O	O	Timer 5 interval output	
						PWM5O	O	Timer 5 PWM output	

Table 3. Normal Pin Description (continued)

Pin no.						PIN Name	I/O(1)	Description	Remark
48	44	32 LQFP	32 SOP	28	28 A96A148				
32	30	20	24	20	20	P07*	IOUS	Port 0 bit 7 Input/output	
						AN5	IA	ADC input ch-5	
						EINT5	I	External interrupt input ch-5	
23	22	16	20	17	17	P10*	IOUS	Port 1 bit 0 Input/output	
						AN13	IA	ADC input ch-13	
						RXD1	I	USART1 data receive	
						SCL1	IO	I2C1 clock signal	
						MISO1	IO	USART1 SPI MISO	
25	23	17	21	18	18	P11*	IOUS	Port 1 bit 1 Input/output	
						AN12	IA	ADC input ch-12	
						EINT12	I	External interrupt input ch-12	
						T2O	O	Timer 2 interval output	
						PWM2O	O	Timer 2 PWM output	
26	24	18	22	19	19	P12*	IOUS	Port 1 bit 2 Input/output	
						AN11	IA	ADC input ch-11	
						EINT11	I	External interrupt input ch-11	
						T1O	O	Timer 1 interval output	
						PWM1O	O	Timer 1 PWM output	
27	25	19	23	-	-	P13*	IOUS	Port 1 bit 3 Input/output	
						AN10	IA	ADC input ch-10	
						EC1	I	Timer 1(Event Capture) input	
						BUZO	O	Buzzer output	
28	26	-	-	-	-	P14*	IOUS	Port 1 bit 4 Input/output	
						AN9	IA	ADC input ch-9	
						MOSI2	IO	USART2 SPI MOSI	
						TXD2	O	USART2 data transmit	
29	27	-	-	-	-	P15*	IOUS	Port 1 bit 5 Input/output	
						AN8	IA	ADC input ch-8	
						MISO2	IO	USART2 SPI MISO	
						RXD2	I	USART2 data receive	

Table 3. Normal Pin Description (continued)

Pin no.						PIN Name	I/O[1]	Description	Remark
48	44	32 LQFP	32 SOP	28	28 A96A148				
30	28	-	-	-	-	P16*	IOUS	Port 1 bit 6 Input/output	
						AN7	IA	ADC input ch-7	
						EINT7	I	External interrupt input ch-7	
						XCK	IO	USART2 clock signal	
31	29	-	-	-	-	P17*	IOUS	Port 1 bit 7 Input/output	
						AN6	IA	ADC input ch-6	
						EINT6	I	External interrupt input ch-6	
						SS2	IO	USART2 slave select signal	
22	21	15	19	16	16	P20*	IOUS	Port 2 bit 0 Input/output	
						AN14	IA	ADC input ch-14	
						TXD1	O	USART1 data transmit	
						SDA1	IO	I2C1 data signal	
						MOSI1	IO	USART1 SPI MOSI	
21	20	14	18	15	-	P21*	IOUS	Port 2 bit 1 Input/output	
						AN15	IA	ADC input ch-15	
						SCK1	IO	USART1 clock signal	
20	19	13	17	-	-	P22*	IOUS	Port 2 bit 2 Input/output	
						SS1	IO	USART1 slave select signal	
19	18	-	-	-	-	P23*	IOU	Port 2 bit 3 Input /output	
18	17	-	-	-	-	P24*	IOU	Port 2 bit 4 Input /output	
17	16	-	-	-	-	P25*	IOU	Port 2 bit 5 Input /output	
16	15	12	16	-	-	P26*	IOU	Port 2 bit 6 Input /output	
15	14	11	15	-	-	P27*	IOU	Port 2 bit 7 Input /output	
14	13	10	14	14	15	P30*	IOUS	Port 3 bit 0 Input /output	
						LED7	I	High sink current ports	
13	12	9	13	13	14	P31*	IOUS	Port 3 bit 1 Input /output	
						LED6	I	High sink current ports	
11	11	8	12	12	13	P32*	IOUS	Port 3 bit 2 Input /output	
						LED5	I	High sink current ports	
10	10	7	11	11	12	P33*	IOUS	Port 3 bit 3 Input /output	
						LED4	I	High sink current ports	

Table 3. Normal Pin Description (continued)

Pin no.						PIN Name	I/O[1]	Description	Remark
48	44	32 LQFP	32 SOP	28	28 A96A148				
9	9	-	-	-	11	P34*	IOUS	Port 3 bit 4 Input /output	
						LED3	I	High sink current ports	
8	8	-	-	-	10	P35*	IOUS	Port 3 bit 5 Input /output	
						LED2	I	High sink current ports	
7	7	-	-	-	9	P36*	IOUS	Port 3 bit 6 Input/output	
						LED1	I	High sink current ports	
6	6	-	-	-	8	P37*	IOUS	Port 3 bit 7 Input/output	
						LED0	I	High sink current ports	
2	2	4	8	8	-	P40*	IOUS	Port 4 bit 0 Input/output	
						RXD0	I	USART0 data receive	
						SCL0	IO	I2C0 clock signal	
						MISO0	IO	USART0 SPI MISO	
3	3	5	9	9	-	P41*	IOUS	Port 4 bit 1 Input/output	
						TXD0	O	USART0 data transmit	
						SDA0	IO	I2C data signal	
						MOSI0	IO	USART0 SPI MOSI	
4	4	-	10	10	-	P42*	IOUS	Port 4 bit 2 Input/output	
						SCK0	IO	USART0 clock signal	
5	5	-	-	-	-	P43*	IOUS	Port 4 bit 3 Input/output	
						SS0	IO	USART0 slave select signal	
12	-	-	-	-	-	P44*	IOUC	Port 4 bit 4 Input/output	
24	-	-	-	-	-	P45*	IOUC	Port 4 bit 5 Input/output	
36	-	-	-	-	-	P46*	IOUC	Port 4 bit 6 Input/output	
48	-	-	-		-	P47*	IOUC	Port 4 bit 7 Input/output	
43	40	30	2	2	2	P50*	IOUS	Port 5 bit 0 Input/output	
						XOUT	O	Main Oscillator Output	
44	41	31	3	3	3	P51*	IOUS	Port 5 bit 1 Input/output	
						XIN	I	Main Oscillator Input	
45	42	32	4	4	4	P52*	IOUS	Port 5 bit 2 Input/output	
						EINT8	I	External interrupt input ch-8	
						EC0	I	Timer 0(Event Capture) input	

Table 3. Normal Pin Description (continued)

Pin no.						PIN Name	I/O(1)	Description	Remark
48	44	32 LQFP	32 SOP	28	28 A96A148				
46	43	1	5	5	5	P53*	IOUS	Port 5 bit 3 Input/output	
						SXIN	I	Sub Oscillator Input	
						T0O	O	Timer 0 interval output	
						PWM0O	O	Timer 0 PWM output	
47	44	2	6	6	6	P54*	IOUS	Port 5 bit 4 Input/output	
						SXOUT	O	Sub Oscillator Input	
						EINT10	I	External interrupt input ch-10	
1	7	3	7	7	7	P55*	IOUS	Port 5 bit 5 Input/output	
						RESETB	IU	Reset pin	Pull-up
41	38	28	32	28	28	VDD	P	VDD	
42	39	29	1	1	1	VSS	P	VSS	

NOTES:

1. The P14–P17, P23–P25, P34–P37, and P43-P47 are not in the 32-pin package.
2. The P13–P17, P22–P27, P34–P37, and P43-P47 are not in the 28-pin package.
3. The P43 is not in the 48-pin package.
4. The P55/RESETB pin is configured as one of the P55 and RESETB pin by the “CONFIGURE OPTION.”
5. If the P00/EC3/DSDA and P01/T3O/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
6. The P00/EC3/DSDA and P01/T3O/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
7. The P50/XOUT, P51/XIN, P53/SXINT/T0O/PWM0O, and P54/SXOUT/EINT10 pins are configured as a function pin by software control.
8. (1) I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
9. The * means ‘Selected pin function after reset condition

3 Port structures

In this chapter, two port structures are introduced in figures 1 and 2 regarding general purpose I/O port and external interrupt I/O port respectively.

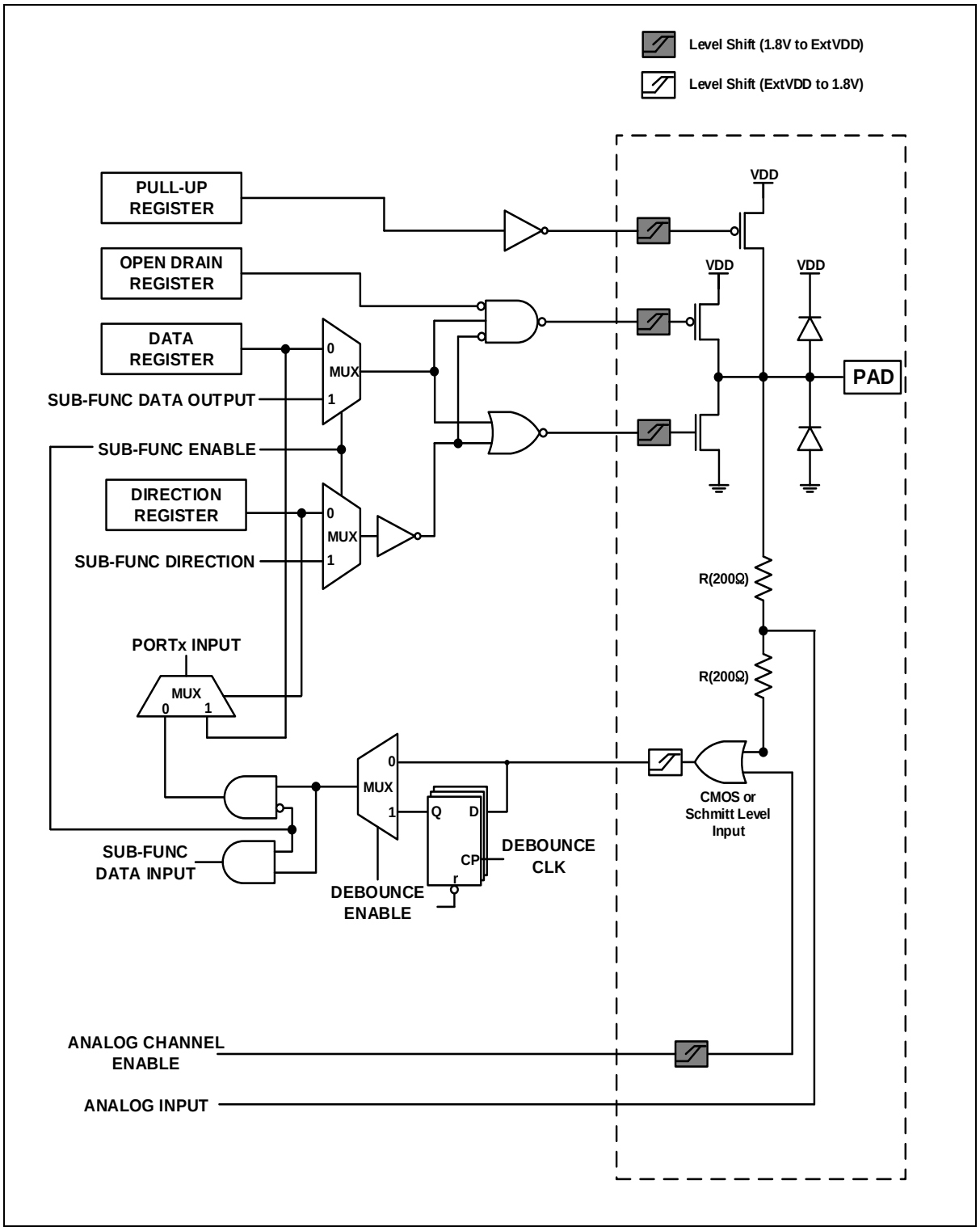


Figure 8. General Purpose I/O Port

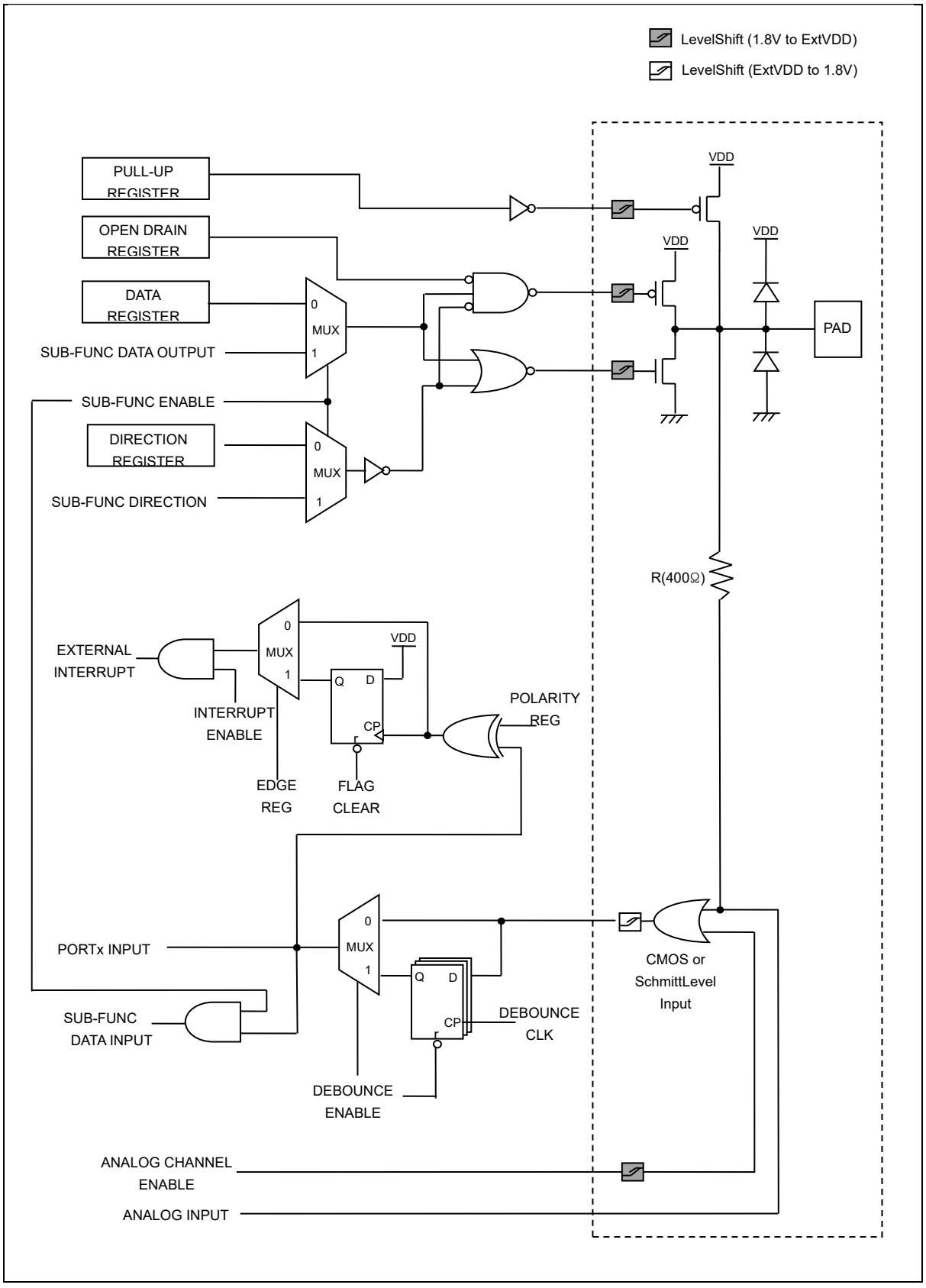


Figure 9. External Interrupt I/O Port

4 Central Processing Unit (CPU)

Central Processing Unit (CPU) of A96G140 is based on Mentor Graphics M8051EW core, which offers improved code efficiency and high performance.

4.1 Architecture and registers

Figure 10 shows a block diagram of the M8051EW architecture. As shown in the figure, the M8051EW supports both Program Memory and External Data Memory. In addition, it features a Debug Mode in which it can be driven through a dedicated debug interface.

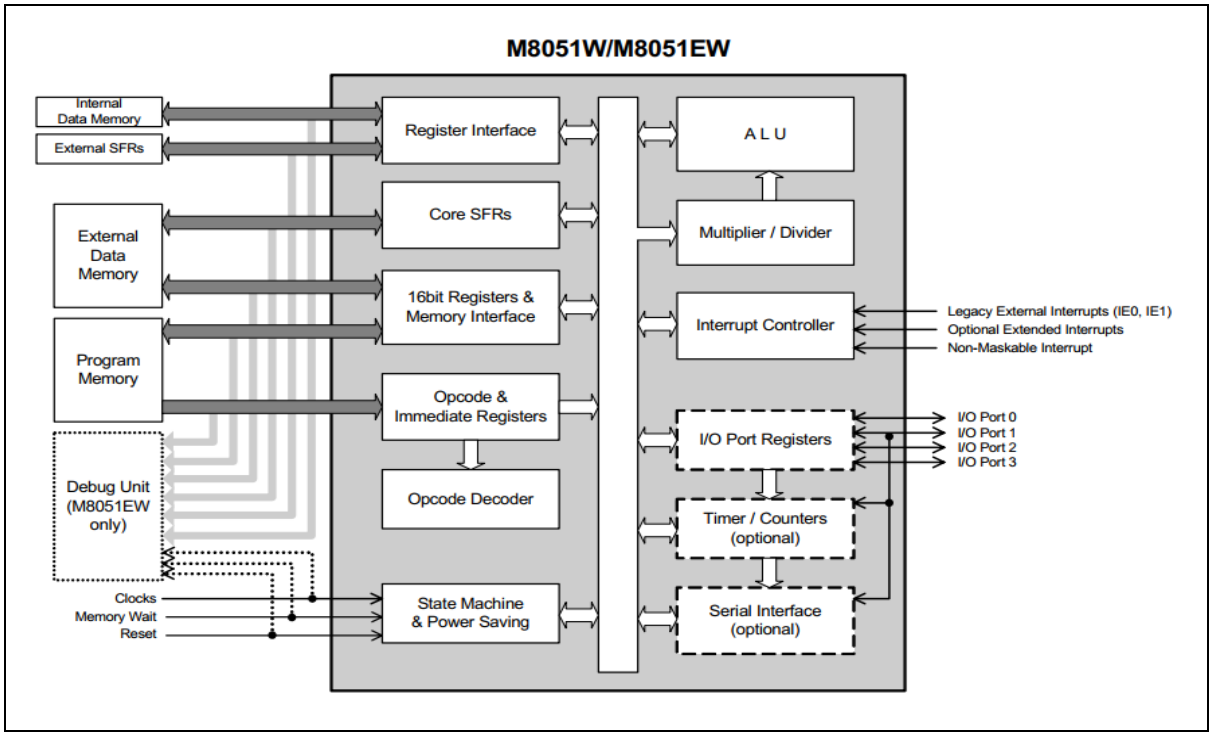


Figure 10. M8051EW Architecture

Main features of the M8051EW are listed below:

- Two clocks per machine cycle architecture
- Debug support (OCD and OCD II)
- Separate Program and External Data Memory interfaces or a single multiplexed interface
- Support for synchronous and asynchronous Program, External Data and Internal Data Memory
- Wait states support for slow Program and External Data Memory.

- 16-bit Data Memory address is generated through the Data Pointer register (DPTR register).
- 16-bit program counter is capable of addressing up to Flash size in each device.
- A single data pointer, two memory-mapped data pointers, or 2, 4 or 8 banked data pointers
- Support for 2 or 4 levels of priority scheme – up to 24 maskable Interrupt sources
- External Special Function Register (SFR) are memory mapped into Direct Memory at the address between 80 hex and FF hex.

4.2 Addressing

The M8051EW supports six types of addressing modes as listed below:

1. Direct addressing mode: In this mode, the operand is specified by the 8-bit address field. Only internal data and SFRs can be accessed using this mode.
2. Indirect addressing mode: In this mode, the operand is specified by addresses contained in a register. Two registers (R0 and R1) from the current bank or the Data Pointer may be used for addressing in this mode. Both internal and external Data Memory may be indirectly addressed.
3. Register addressing mode: In this mode, the operand is specified by the top 3 bits of the opcode, which selects one of the current bank of registers. Four banks of registers are available. The current bank is selected by the 3rd and 4th bits of the PSW.
4. Register specific addressing mode: In this mode, some instructions only operate on specific registers. This is defined by the opcode. In particular many accumulator operations and some stack pointer operations are defined in this manner.
5. Immediate DATA mode: In this mode, Instructions which use Immediate Data are 2 or more bytes long and the Immediate operand is stored in Program Memory as part of the instruction.

   Example) `MOV A, #100`

   It loads the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.
6. Indexed addressing mode: In this mode, only Program Memory can be addressed. It is intended for simple implementation of look-up tables. A 16-bit base register (either the PC or the DPTR) is combined with an offset stored in the accumulator to access data in Program Memory.

4.3 Instruction set

An instruction is a single operation of a processor that is defined by the instruction set. The M8051EW uses the instruction set of 8051 that is broadly classified into five functional categories:

1. Arithmetic instructions
2. Logical instructions
3. Data transfer instructions
4. Boolean instructions
5. Branching instructions

Major features of the instruction set are listed below. If you need detailed information about the instruction table, please refer to **Appendix** or **Instruction table**:

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes'.
- Each instruction takes either 1, 2 or 4 machine cycles to execute. 1 machine cycle comprises 2 CCLK clock cycles.
- An M8051EW-specific instruction "`MOVC @(DPTR++), A`" is provided to enable software to be downloaded into Program Memory where it is implemented as RAM. This instruction can also be used subsequently to modify contents of the Program Memory RAM.
- Arithmetic Instruction
- Logical Instruction
- Internal data memory
- External data memory
- Unconditional Jumps
- Subroutine calls and returns
- Conditional Jumps
- Boolean Instructions
- Flag

5 Memory organization

A96G140/A96G148/A96A148 addresses two separate address memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the Data Memory more rapidly. 16-bit Data Memory address is generated through the DPTR register.

A96G140/A96G148/A96A148 provides on-chip 64Kbytes of the ISP type flash program memory, which readable and writable. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 2304bytes.

5.1 Program memory

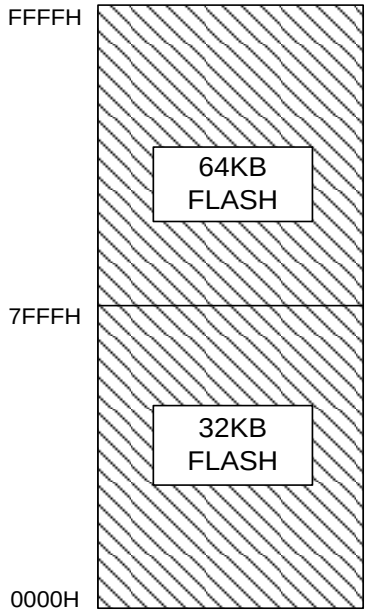
A 16-bit program counter is capable of addressing up to 64Kbytes, and A96G140/A96G148/A96A148 has just 64Kbytes program memory space.

Figure 9 shows a map of the lower part of the program memory.

After reset, CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in the program memory. An interrupt causes the CPU to jump to the corresponding location, where it commences execution of the service routine.

An external interrupt 11, for example, is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within an interval of 8-bytes.

Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.



NOTE: The 64Kbytes includes the Interrupt Vector Region.

Figure 11. Program Memory Map

5.2 Data memory

Internal data memory space is divided into three blocks, which are generally referred to as lower 128bytes, upper 128bytes, and SFR space. Internal data memory addresses are always one byte wide, which implies an address space of 256bytes. In fact, the addressing modes for the internal data memory can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space, while indirect addresses higher than 7FH access a different memory space. Thus as shown in figure 10, the upper 128bytes and SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in figure 11. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes of RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

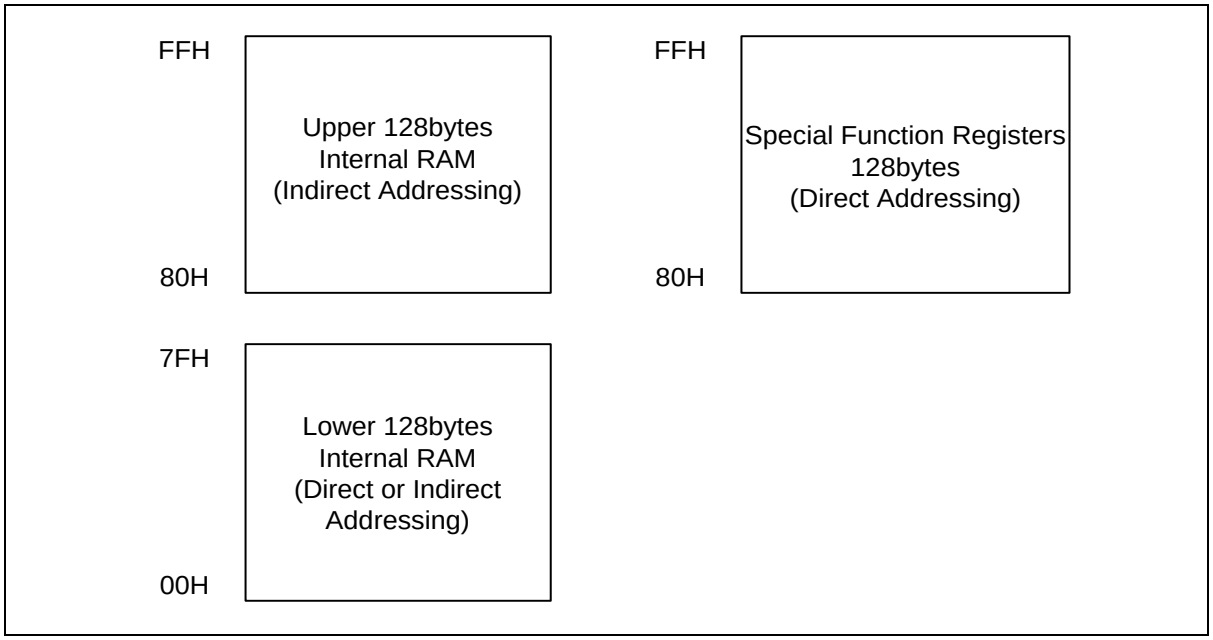


Figure 12. Data Memory Map

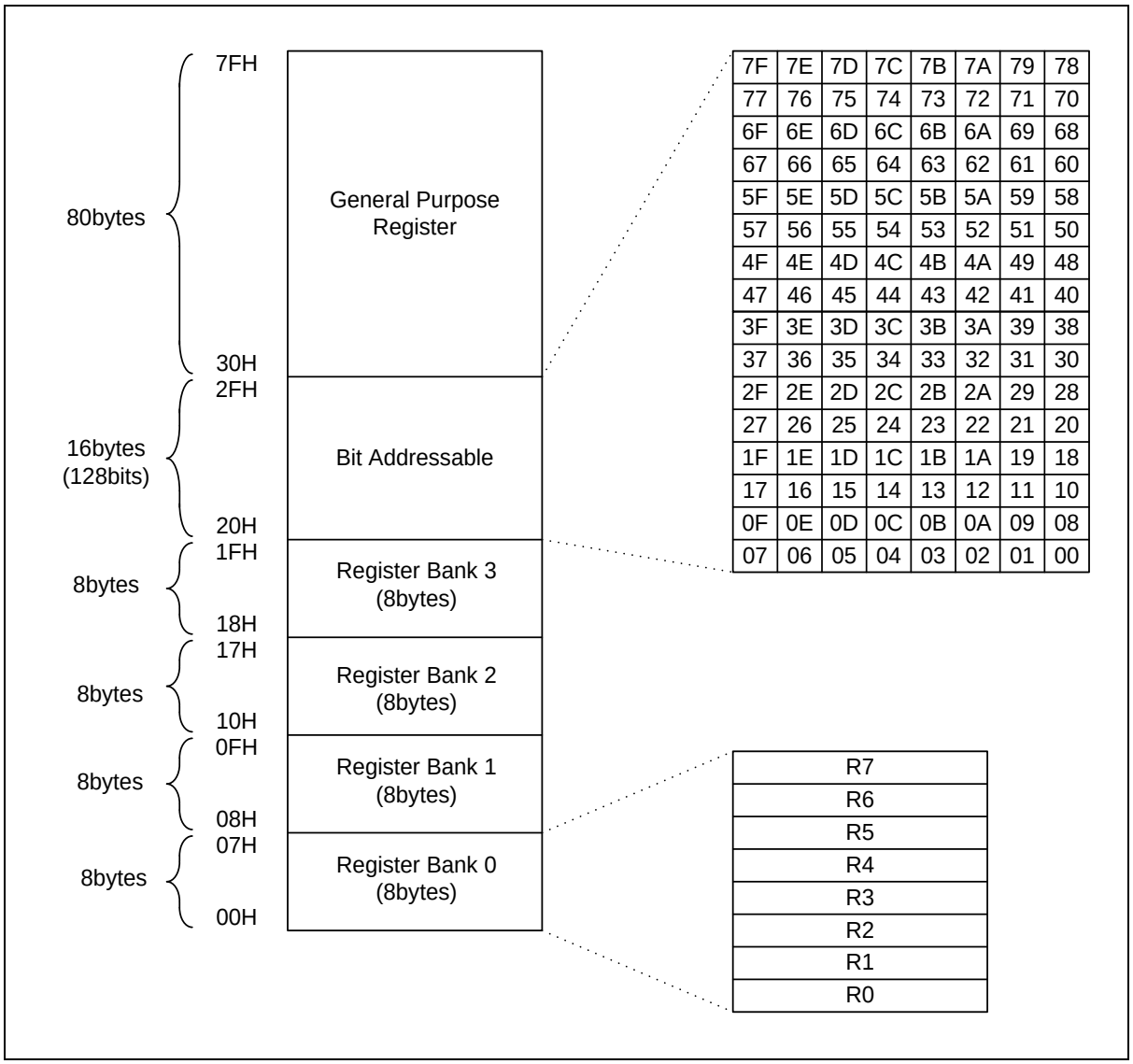


Figure 13. Lower 128bytes of RAM

5.3 External data memory

A96G140/A96G148/A96A148 has 2304bytes of XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

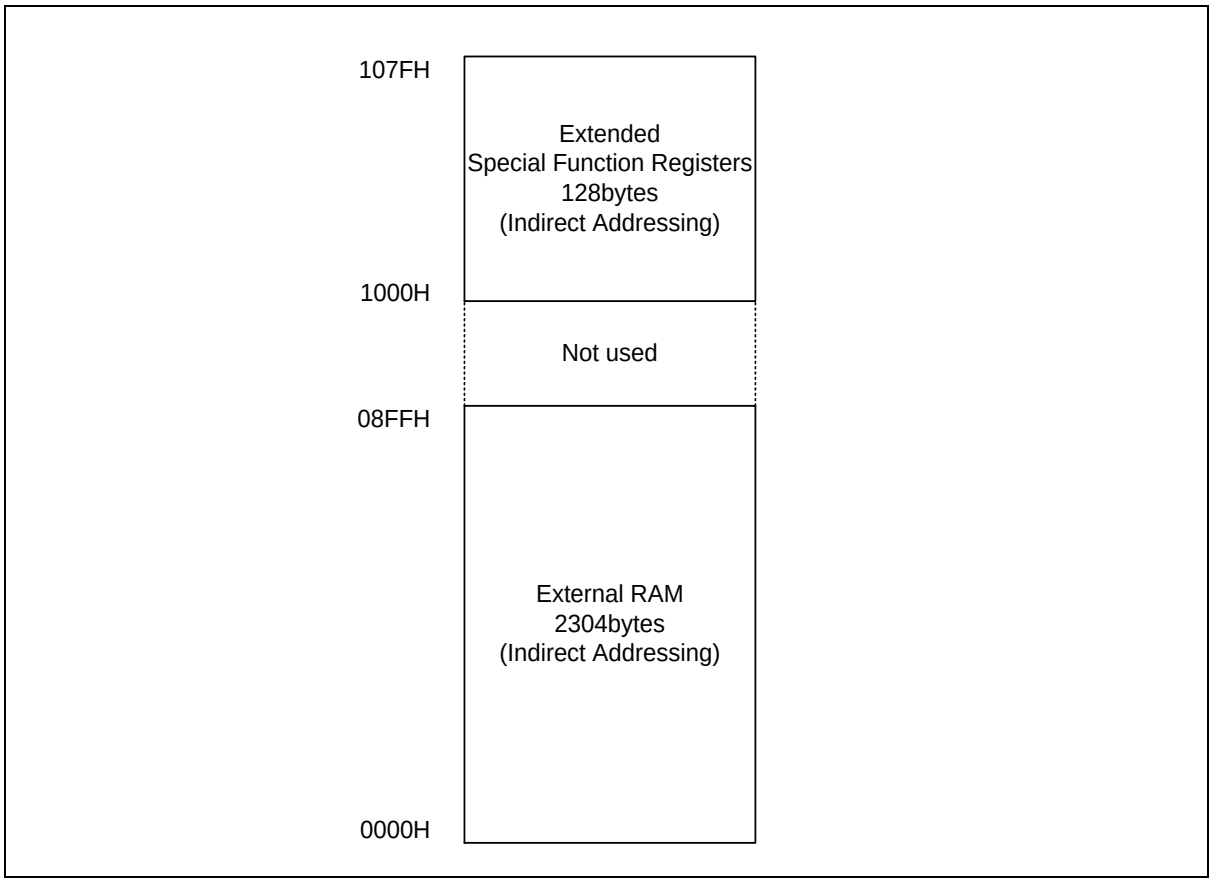


Figure 14. XDATA Memory Area

5.4 SFR map

5.4.1 SFR map summary

Table 4. SFR Map Summary

—	Reserved
	M8051 compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	–	–	UBAUD	UDATA	–	P5FSR
0F0H	B	USI1ST1	USI1ST2	USI1BD	USI1SDHR	USI1DR	USI1SCLR	USI1SCHR
0E8H	RSTFR	USI1CR1	USI1CR2	USI1CR3	USI1CR4	USI1SAR	P3FSR	P4FSR
0E0H	ACC	USI0ST1	USI0ST2	USI0BD	USI0SDHR	USI0DR	USI0SCLR	USI0SCHR
0D8H	LVRCR	USI0CR1	USI0CR2	USI0CR3	USI0CR4	USI0SAR	P0DB	P15DB
0D0H	PSW	P5IO	P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSR	–
0C8H	OSCCR	P4IO	–	UCTRL1	UCTRL2	UCTRL3	–	USTAT
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH

Table 4. SFR Map Summary (continued)

—	Reserved
	M8051 compatible

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	P5	P1IO	T0CR	T0CNT	T0DR/ T0CDR	–	–	–
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	P4	P0IO	EO	P4PU	EIPOL0L	EIPOL0H	EIFLAG1	EIPOL1
98H	P3	–	–	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	P4OD	P5PU	WTCR	BUZCR
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTE: 00H/8H, these registers are bit-addressable.

Table 5. XSFR Map Summary

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
1078H	—	—	—	—	—	—	—	—
1070H	—	—	—	—	—	—	—	—
1068H	—	—	—	—	—	—	—	—
1060H	—	—	—	—	—	—	—	—
1058H	—	—	—	—	—	—	—	—
1050H	—	—	—	—	—	—	—	—
1048H	—	—	—	—	—	—	—	—
1040H	—	—	—	—	—	—	—	—
1038H	XTFLSR	—	—	—	—	—	—	—
1030H	—	—	—	—	—	—	—	—
1028H	FEARH	FEARM	FEARL	FEDR	FETR	—	—	—
1020H	FEMR	FECR	FESR	FETCR	FEARM1	FEARL1	—	—
1018H	UCTRL4	FPCR	RTOCH	RTOCL	—	—	—	—
1010H	T5CRH	T5CRL	T5ADRH	T5ADRL	T5BDRH	T5BDRL	—	—
1008H	T4CRH	T4CRL	T4ADRH	T4ADRL	T4BDRH	T4BDRL	—	—
1000H	T3CRH	T3CRL	T3ADRH	T3ADRL	T3BDRH	T3BDRL	—	—

5.4.2 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	1	0	0	0	1	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	P4 Open-drain Selection Register	P4OD	R/W	0	0	0	0	0	0	0	0
95H	P5 Pull-up Resistor Selection Register	P5PU	R/W	–	–	0	0	0	0	0	0
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	0	0	0	0	0	0	1
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	0	0	0	0	0	0	0	0
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	P4 Pull-up Resistor Selection Register	P4PU	R/W	0	0	0	0	0	0	0	0
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	0	0	0	0	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	–	–	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
B0H	P5 Data Register	P5	R/W	–	–	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0
BBH	Timer 1 Counter High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	0	0	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	0	1	0	1	0	0	0
C9H	P4 Direction Register	P4IO	R/W	0	0	0	0	0	0	0	0
CBH	USART Control Register 1	UCTRL1	R/W	0	0	0	0	0	0	0	0
CCH	USART Control Register 2	UCTRL2	R/W	0	0	0	0	0	0	0	0
CDH	USART Control Register 3	UCTRL3	R/W	0	0	0	0	–	0	0	0
CFH	USART Status Register	USTAT	R/W	1	0	0	0	0	0	0	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	P5 Direction Register	P5IO	R/W	–	–	0	0	0	0	0	0
D2H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
D3H	P0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
D5H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
D6H	P2 Function Selection Register	P2FSR	R/W	–	–	–	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	–	–	–	0	0	0	0	0
D9H	USI0 Control Register 1	USI0CR1	R/W	0	0	0	0	0	0	0	0
DAH	USI0 Control Register 2	USI0CR2	R/W	0	0	0	0	0	0	0	0
DBH	USI0 Control Register 3	USI0CR3	R/W	0	0	0	0	0	0	0	0
DCH	USI0 Control Register 4	USI0CR4	R/W	0	–	–	0	0	–	0	0
DDH	USI0 Slave Address Register	USI0SAR	R/W	0	0	0	0	0	0	0	0
DEH	P0 De-bounce Enable Register	P0DB	R/W	0	0	0	0	0	0	0	0
DFH	P1/P5 De-bounce Enable Register	P15DB	R/W	–	–	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	USI0 Status Register 1	USI0ST1	R/W	0	0	0	0	–	0	0	0
E2H	USI0 Status Register 2	USI0ST2	R	0	0	0	0	0	0	0	0
E3H	USI0 Baud Rate Generation Register	USI0BD	R/W	1	1	1	1	1	1	1	1
E4H	USI0 SDA Hold Time Register	USI0SHDR	R/W	0	0	0	0	0	0	0	1
E5H	USI0 Data Register	USI0DR	R/W	0	0	0	0	0	0	0	0
E6H	USI0 SCL Low Period Register	USI0SCLR	R/W	0	0	1	1	1	1	1	1
E7H	USI0 SCL High Period Register	USI0SCHR	R/W	0	0	1	1	1	1	1	1
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	USI1 Control Register 1	USI1CR1	R/W	0	0	0	0	0	0	0	0
EAH	USI1 Control Register 2	USI1CR2	R/W	0	0	0	0	0	0	0	0
EBH	USI1 Control Register 3	USI1CR3	R/W	0	0	0	0	0	0	0	0
ECH	USI1 Control Register 4	USI1CR4	R/W	0	–	–	0	0	–	0	0
EDH	USI1 Slave Address Register	USI1SAR	R/W	0	0	0	0	0	0	0	0
EEH	Port3 Function Selection Register	P3FSR	R/W	0	0	0	0	0	0	0	0
EFH	P4 Function Selection Register	P4FSR	R/W	–	–	–	–	0	0	0	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	USI1 Status Register 1	USI1ST1	R/W	0	0	0	0	–	0	0	0
F2H	USI1 Status Register 2	USI1ST2	R	0	0	0	0	0	0	0	0
F3H	USI1 Baud Rate Generation Register	USI1BD	R/W	1	1	1	1	1	1	1	1
F4H	USI1 SDA Hold Time Register	USI1SHDR	R/W	0	0	0	0	0	0	0	1
F5H	USI1 Data Register	USI1DR	R/W	0	0	0	0	0	0	0	0
F6H	USI1 SCL Low Period Register	USI1SCLR	R/W	0	0	1	1	1	1	1	1
F7H	USI1 SCL High Period Register	USI1SCHR	R/W	0	0	1	1	1	1	1	1
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
FCH	USART Baud Rate Generation Register	UBAUD	R/W	1	1	1	1	1	1	1	1
FDH	USART Data Register	UDATA	R/W	0	0	0	0	0	0	0	0
FFH	P5 Function Selection Register	P5FSR	R/W	0	0	0	0	0	0	0	0

Table 7. XSFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1000H	Timer 3 Control High Register	T3CRH	R/W	0	–	0	0	–	–	–	0
1001H	Timer 3 Control Low Register	T3CRL	R/W	0	0	0	0	–	0	–	0
1002H	Timer 3 A Data High Register	T3ADRH	R/W	1	1	1	1	1	1	1	1
1003H	Timer 3 A Data Low Register	T3ADRL	R/W	1	1	1	1	1	1	1	1
1004H	Timer 3 B Data High Register	T3BDRH	R/W	1	1	1	1	1	1	1	1
1005H	Timer 3 B Data Low Register	T3BDRL	R/W	1	1	1	1	1	1	1	1
1006H	Reserved	–	–								
1007H	Reserved	–	–								
1008H	Timer 4 Control High Register	T4CRH	R/W	0	–	0	0	–	–	–	0
1009H	Timer 4 Control Low Register	T4CRL	R/W	0	0	0	0	–	0	–	0
100AH	Timer 4 A Data High Register	T4ADRH	R/W	1	1	1	1	1	1	1	1
100BH	Timer 4 A Data Low Register	T4ADRL	R/W	1	1	1	1	1	1	1	1
100CH	Timer 4 B Data High Register	T4BDRH	R/W	1	1	1	1	1	1	1	1
100DH	Timer 4 B Data Low Register	T4BDRL	R/W	1	1	1	1	1	1	1	1
100EH	Reserved	–	–	–							
100FH	Reserved	–	–	–							
1010H	Timer 5 Control High Register	T5CRH	R/W	0	–	0	0	–	–	–	0
1011H	Timer 5 Control Low Register	T5CRL	R/W	0	0	0	0	–	0	–	0
1012H	Timer 5 A Data High Register	T5ADRH	R/W	1	1	1	1	1	1	1	1
1013H	Timer 5 A Data Low Register	T5ADRL	R/W	1	1	1	1	1	1	1	1
1014H	Timer 5 B Data High Register	T5BDRH	R/W	1	1	1	1	1	1	1	1
1015H	Timer 5 B Data Low Register	T5BDRL	R/W	1	1	1	1	1	1	1	1
1018H	USART Control Register 4	UCTRL4	R/W	–	–	–	0	0	0	0	0
1019H	USART Floating Point Counter	FPCR	R/W	0	0	0	0	0	0	0	0
101AH	Receiver Time Out Counter High Register	RTOCH	R	0	0	0	0	0	0	0	0
101BH	Receiver Time Out Counter Low Register	RTOCL	R	0	0	0	0	0	0	0	0
1020H	Flash Mode Register	FEMR	R/W	0	–	0	0	0	0	0	0
1021H	Flash Control Register	FECR	R/W	0	–	0	0	0	0	1	1
1022H	Flash Status Register	FESR	R/W	1	–	–	–	0	0	0	0
1023H	Flash Time Control Register	FETCR	R/W	0	0	0	0	0	0	0	0
1024H	Flash Address Middle Register 1	FEARM1	R/W	0	0	0	0	0	0	0	0
1025H	Flash Address Low Register 1	FEARL1	R/W	0	0	0	0	0	0	0	0
1028H	Flash Address High Register	FEARH	R/W	0	0	0	0	0	0	0	0
1029H	Flash Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
102AH	Flash Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0
1038H	Main Crystal OSC Filter Selection Register	XTFLSR	R/W	–	–	0	0	0	0	0	0
107FH	Reserved	–	–	–							

6 I/O ports

A96G140/A96G148/A96A148 has ten groups of I/O ports (P0 ~ P5). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. P0 includes a function that can generate interrupt signals according to state of a pin.

6.1 P0 port

6.1.1 P0 port description

P0 is an 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

6.2 P1 port

6.2.1 P1 port description

P1 is an 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P15DB), P1 pull-up resistor selection register (P1PU), andP1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

6.3 P2 port

6.3.1 P2 port description

P2 is an 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) andP2 open-drain selection register (P2OD).Refer to the port function selection registers for the P2 function selection.

6.4 P3 port

6.4.1 P3 port description

P3 is an 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO) and P3 pull-up resistor selection register (P3PU). Refer to the port function selection registers for the P3 function selection.

6.5 P4 port

6.5.1 P4 port description

P4 is a 4-bit I/O port. P4 control registers consist of P4 data register (P4), P4 direction register (P4IO), P4 pull-up resistor selection register (P4PU) andP4 open-drain selection register (P4OD).Refer to the port function selection registers for the P4 function selection.

6.6 P5 port

6.6.1 P5 port description

P5 is a 6-bit I/O port. P5 control registers consist of P5 data register (P5), P5 direction register (P5IO) andP5 pull-up resistor selection register (P5PU). Refer to the port function selection registers for the P5 function selection.

7 Interrupt controller

A96G140/A96G148/A96A148 supports up to 23 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. In addition, they have four levels of priority assigned to themselves.

A non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources, and is not controllable by software.

Interrupt controller of A96G140/A96G148/A96A148 has following features:

- Request receive from the 23 interrupt sources
- 6 groups of priority
- 4 levels of priority
- Multi Interrupt possibility
- A request of higher priority level is served first, when multiple requests of different priority levels are received simultaneously.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency of 3 to 9 machine cycles in single interrupt system

A non-maskable interrupt is always enabled, while maskable interrupts are enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The A96G140/A96G148/A96A148 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Figure 13 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

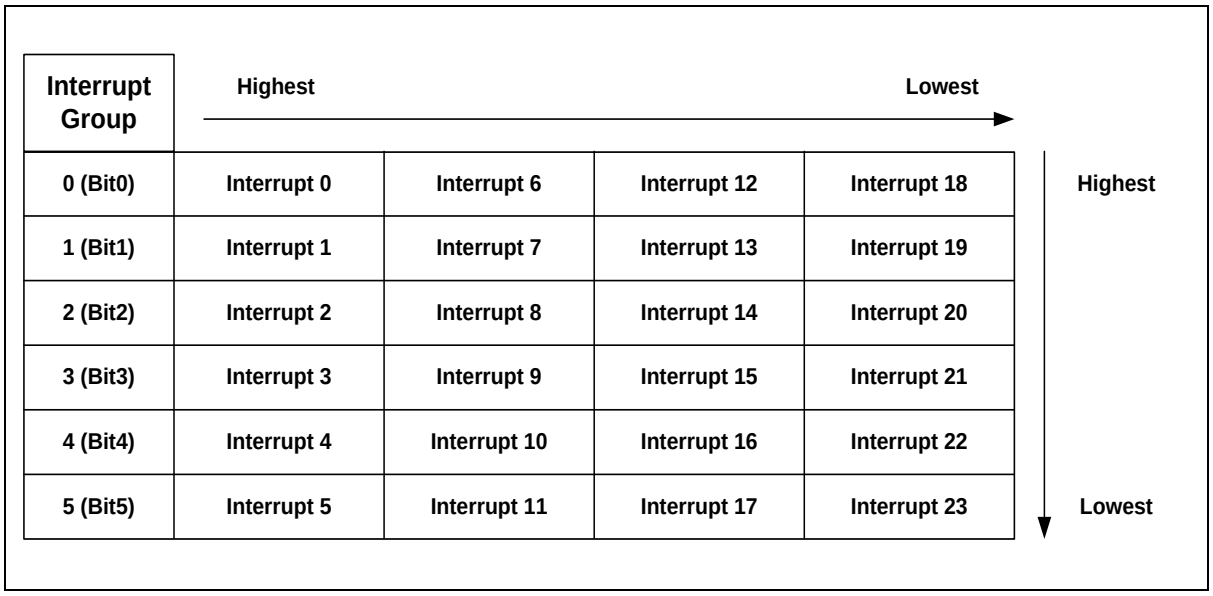
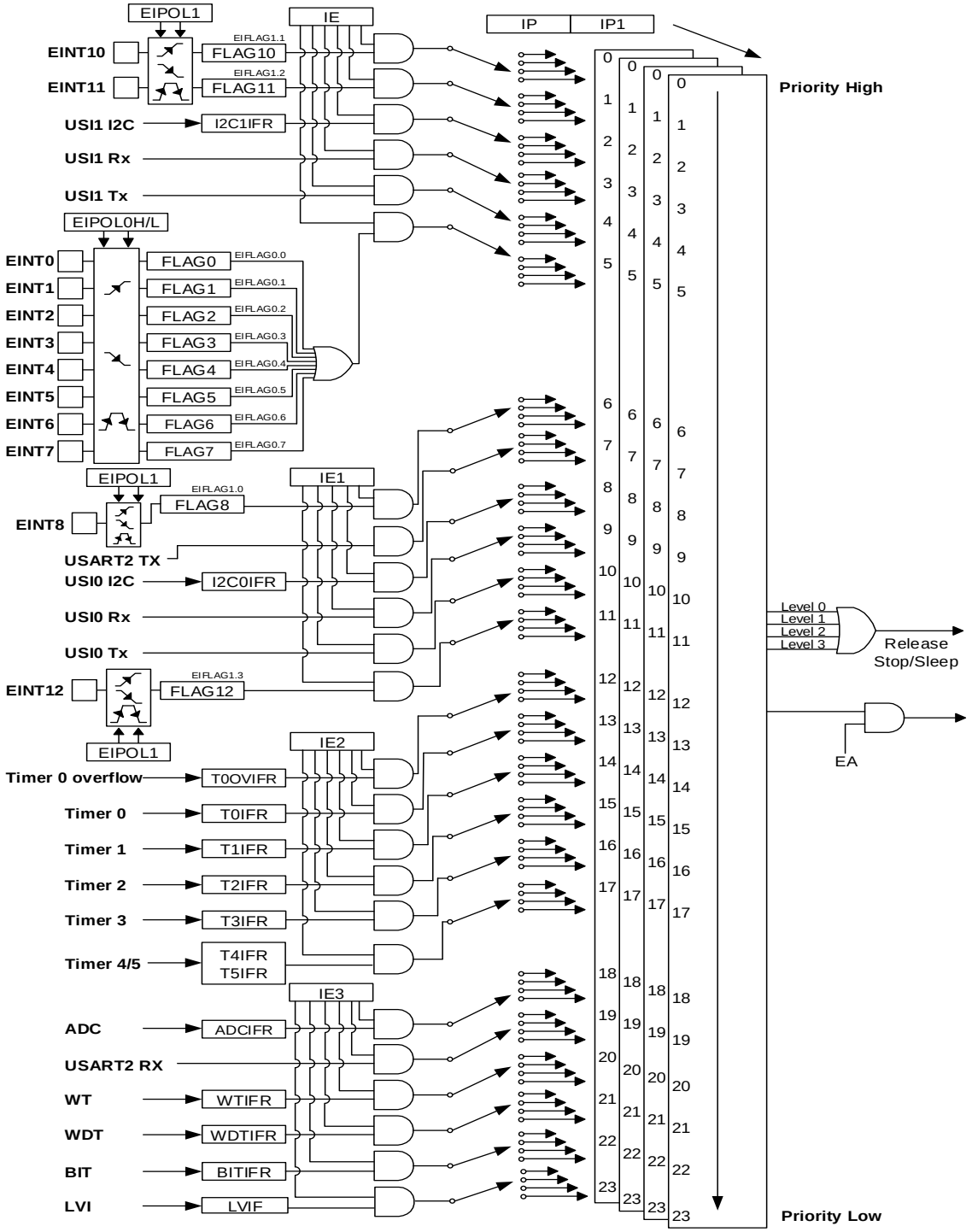


Figure 15. Interrupt Group Priority Level

7.1 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

Figure 16. Interrupt Controller Block Diagram

7.2 Interrupt vector table

Interrupt controller of A96G140/A96G148/A96A148 supports 24 interrupt sources as shown in table 8. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 8. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware Reset	RESETB	—	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
USI1 I2C Interrupt	INT2	IE.2	3	Maskable	0013H
USI1 Rx Interrupt	INT3	IE.3	4	Maskable	001BH
USI1 Tx Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 - 7	INT5	IE.5	6	Maskable	002BH
External Interrupt 8	INT6	IE1.0	7	Maskable	0033H
USART2 TX Interrupt	INT7	IE1.1	8	Maskable	003BH
USI0 I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
USI0 Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
USI0 Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 12	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
T4/T5 Match Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
USART2 RX Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
LVI Interrupt	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

8 Clock generator

As shown in figure 24, a clock generator produces basic clock pulses which provide a system clock for CPU and peripheral hardware.

It contains main/sub-frequency clock oscillator. The main/sub clock can operate easily by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. For this, it is necessary to place external clock signal into the XIN/SXIN pin and open XOUT/SXOUT pin.

Default system clock is 1MHz INT-RC Oscillator. To stabilize the system internally, 128kHz LOW INT-RC oscillator on POR is recommended.

Oscillators in the clock generator are introduced in the followings:

- Calibrated high speed internal RC oscillator (32MHz)
  - HSI OSC/2 (16MHz, default system clock)
  - HSI OSC/4 (8MHz)
  - HSI OSC/8 (4MHz)
  - HSI OSC/16 (2MHz)
  - HSI OSC/32 (1MHz)
  - HSI OSC/64 (0.5MHz)
- Main crystal oscillator (4~12MHz)
- Sub-crystal Oscillator (32.768kHz)
- Internal LSI oscillator (128kHz)

8.1 Clock generator block diagram

In this section, a clock generator of A96G140/A96G148/A96A148 is described in a block diagram.

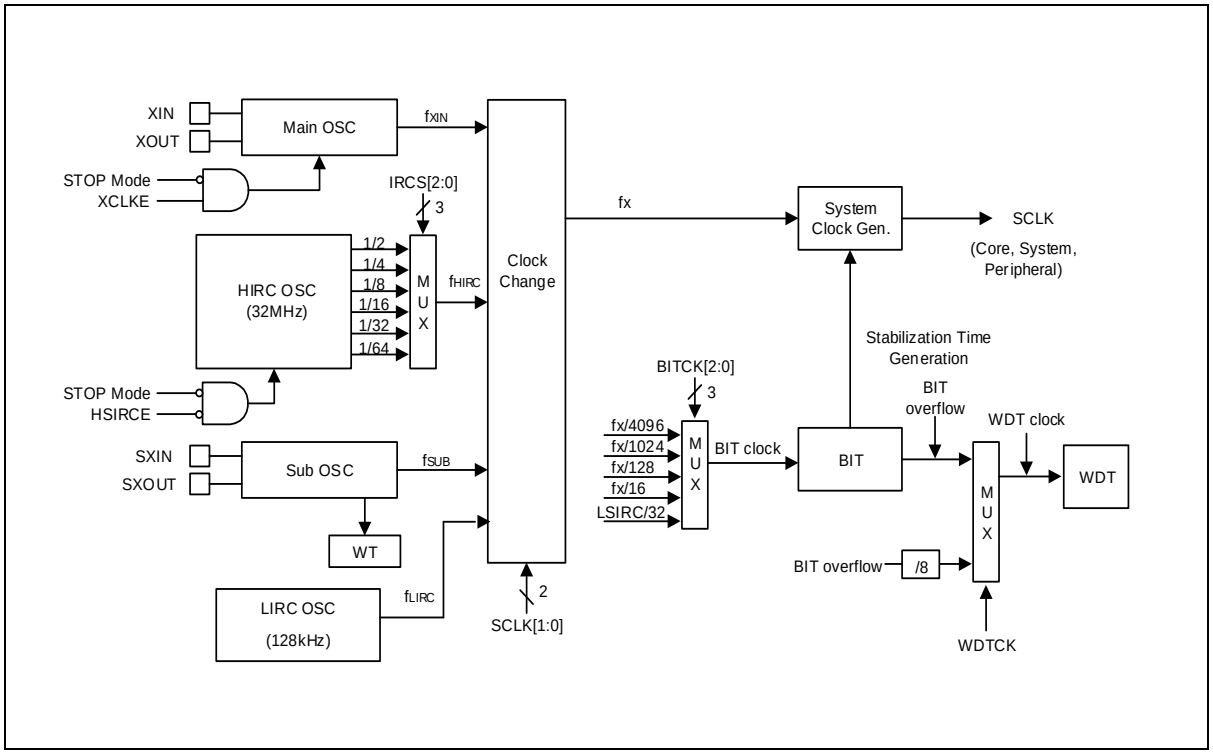


Figure 17. Clock Generator Block Diagram

9 Basic interval timer

A96G140/A96G148/A96A148 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting, and provides a basic interval timer interrupt (BITIFR).

BIT of A96G140/A96G148/A96A148 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

9.1 BIT block diagram

In this section, basic interval timer of A96G140/A96G148/A96A148 is described in a block diagram.

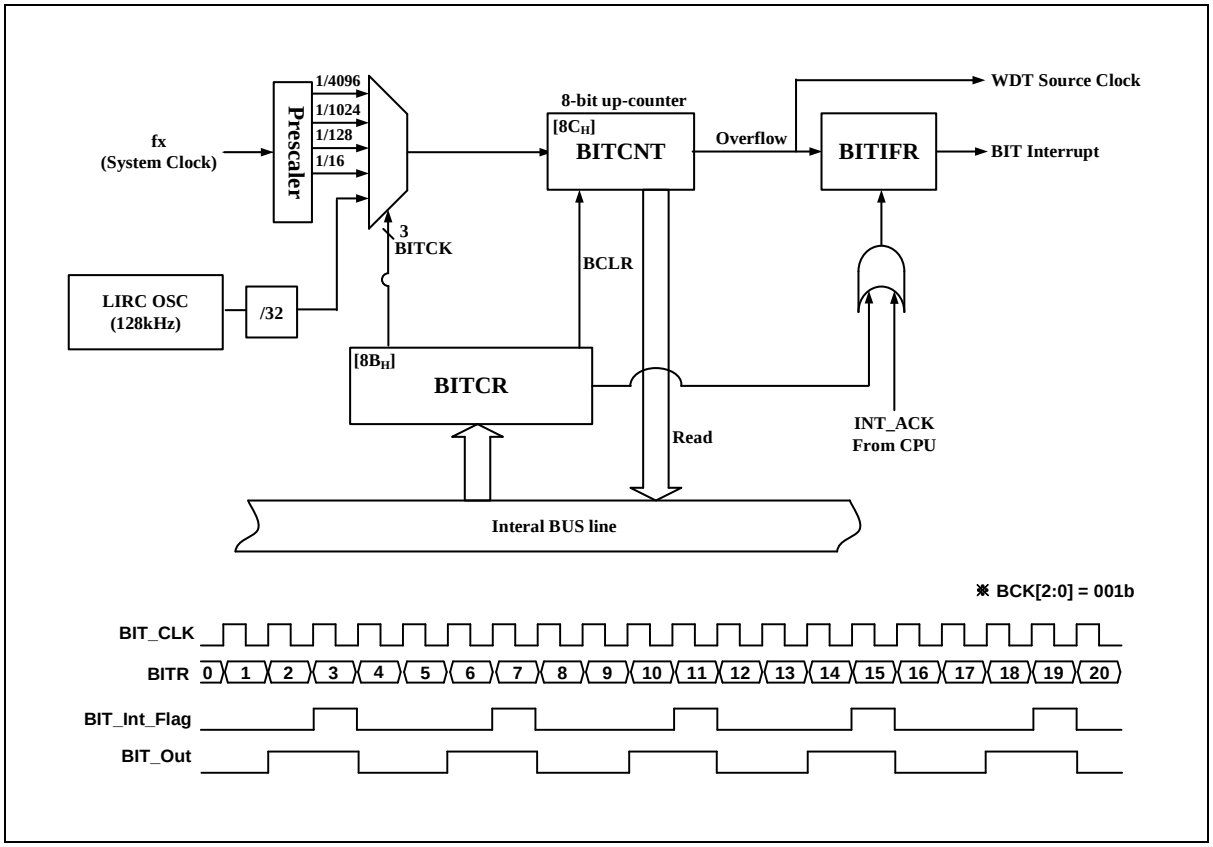


Figure 18. Basic Interval Timer Block Diagram

10 Watchdog timer

Watchdog timer (WDT) rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') by setting WDTCR[6] bit. If WDTCR[5] is set to '1', the WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

The WDT consists of an 8-bit binary counter and a watchdog timer data register. When value of the 8-bit binary counter is equal to the 8 bits of WDTCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset signal of CPU in accordance with a bit WDTRSON.

Input clock source of the WDT is BIT overflow. An interval between watchdog timer interrupts is decided by BIT overflow period and WDTDR set value. The equation can be described as the followings:

- WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

10.1 WDT block diagram

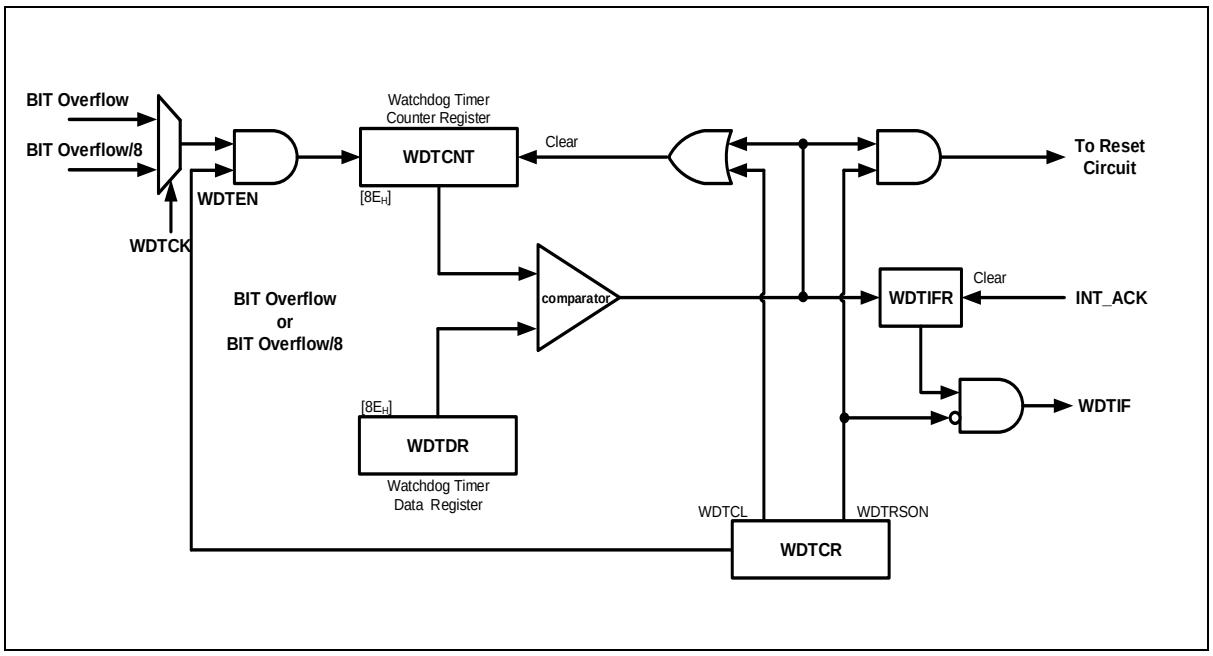


Figure 19. Watch Dog Timer Block Diagram

11 Watch timer

Watch timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register.

Although CPU is in STOP mode, a sub clock can be alive so that WT continues its operation. Watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to increase resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

11.1 WT block diagram

In this section, watch timer of A96G140/A96G148/A96A148 is described in a block diagram.

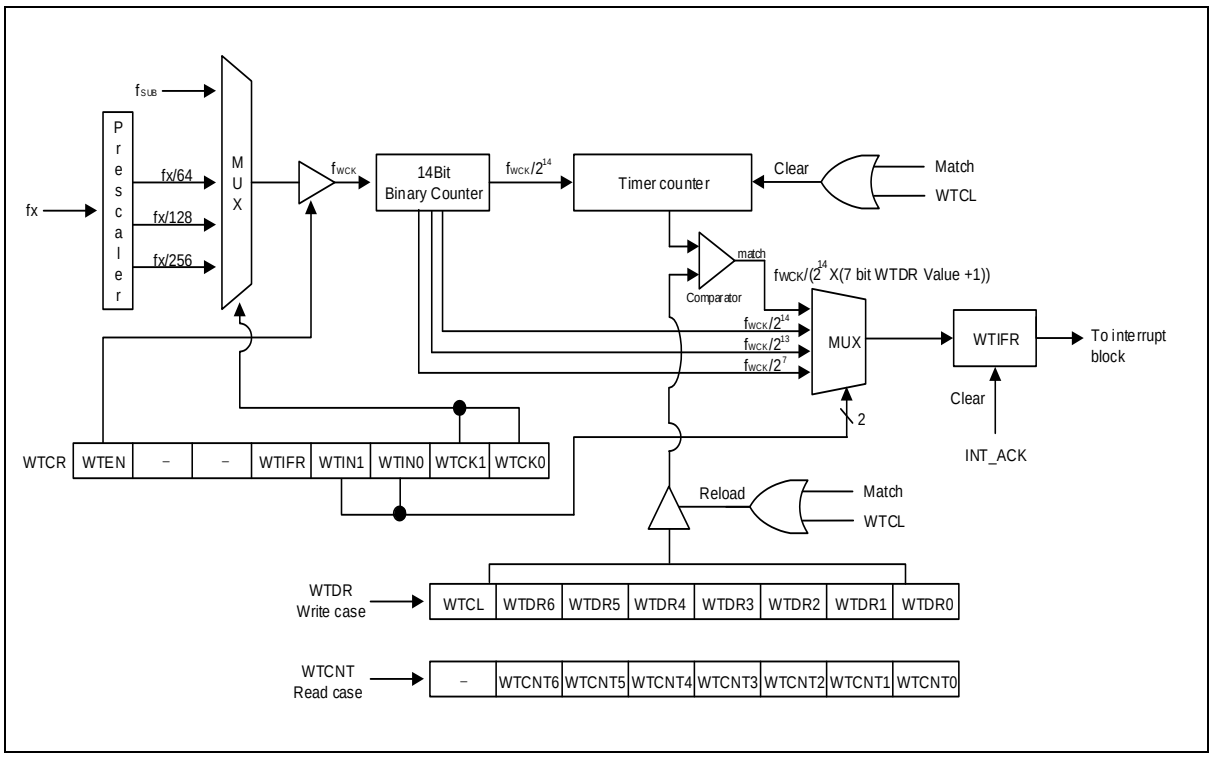


Figure 20. Watch Timer Block Diagram

12 Timer 0/1/2/3/4/5

12.1 Timer 0

An 8-bit timer 0 consists of a multiplexer, a timer 0 counter register, a timer 0 data register, a timer 0 capture data register and a timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

Timer 0 operates in one of three modes introduced in the followings:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

Timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by clock selection bits T0CK[2:0].

- TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048 and EC0

In capture mode, data is captured into input capture data register (T0CDR) by EINT10. In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. In addition, timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 9. Timer 0 Operating Mode

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

12.1.1 Timer 0 block diagram

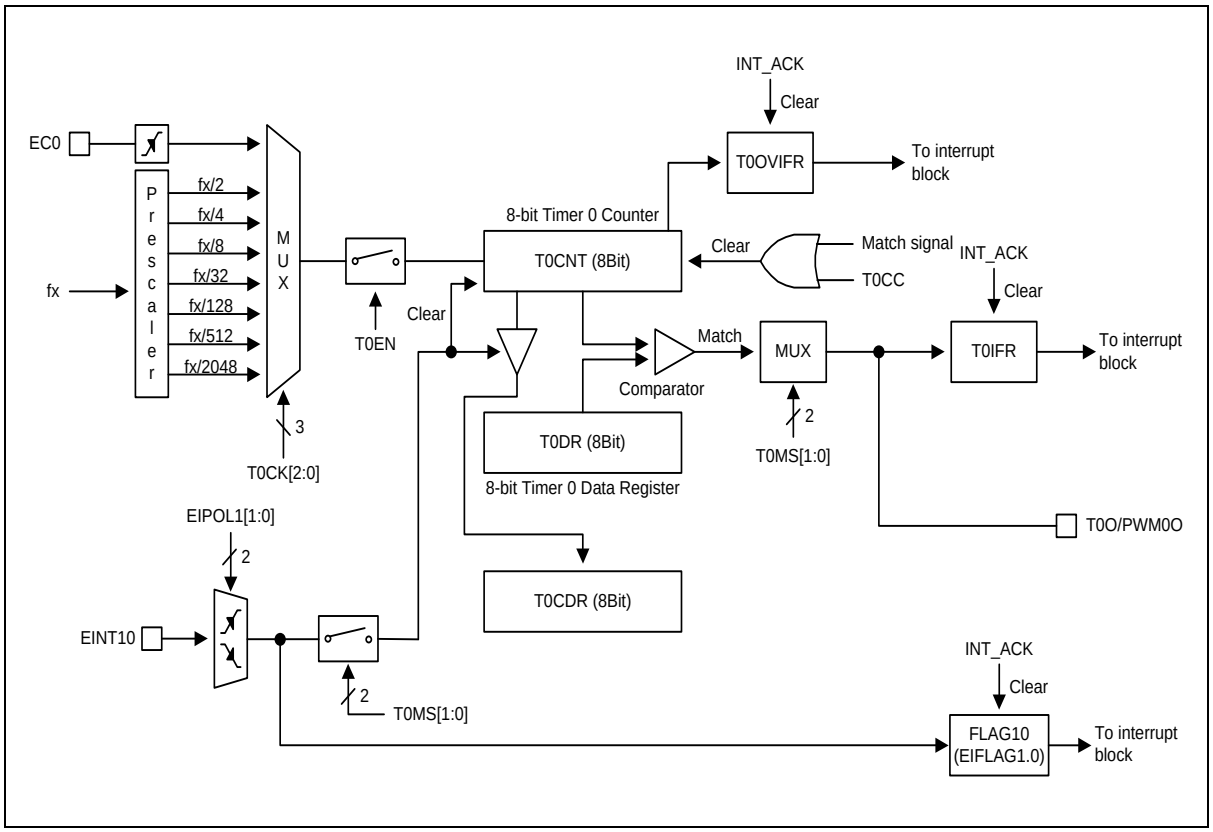


Figure 21. 8-bit Timer 0 Block Diagram

12.2 Timer 1

A 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL).

Timer 1 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock source: fX/1, 2, 4, 8, 64, 512, 2048 and EC1

In capture mode, the data is captured into input capture data register (T1BDRH/T1BDRL) by EINT11. Timer 1 results in the comparison between counter and data register through T1O port in timer/counter mode. In addition, Timer 1 outputs PWM waveform through PWM1Oport in the PPG mode.

Table 10. TIMER 1 Operating Modes

T1EN	P1FSRL[5:4]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.2.1 16-bit timer 1 block diagram

In this section, a 16-bit timer 1 is described in a block diagram.

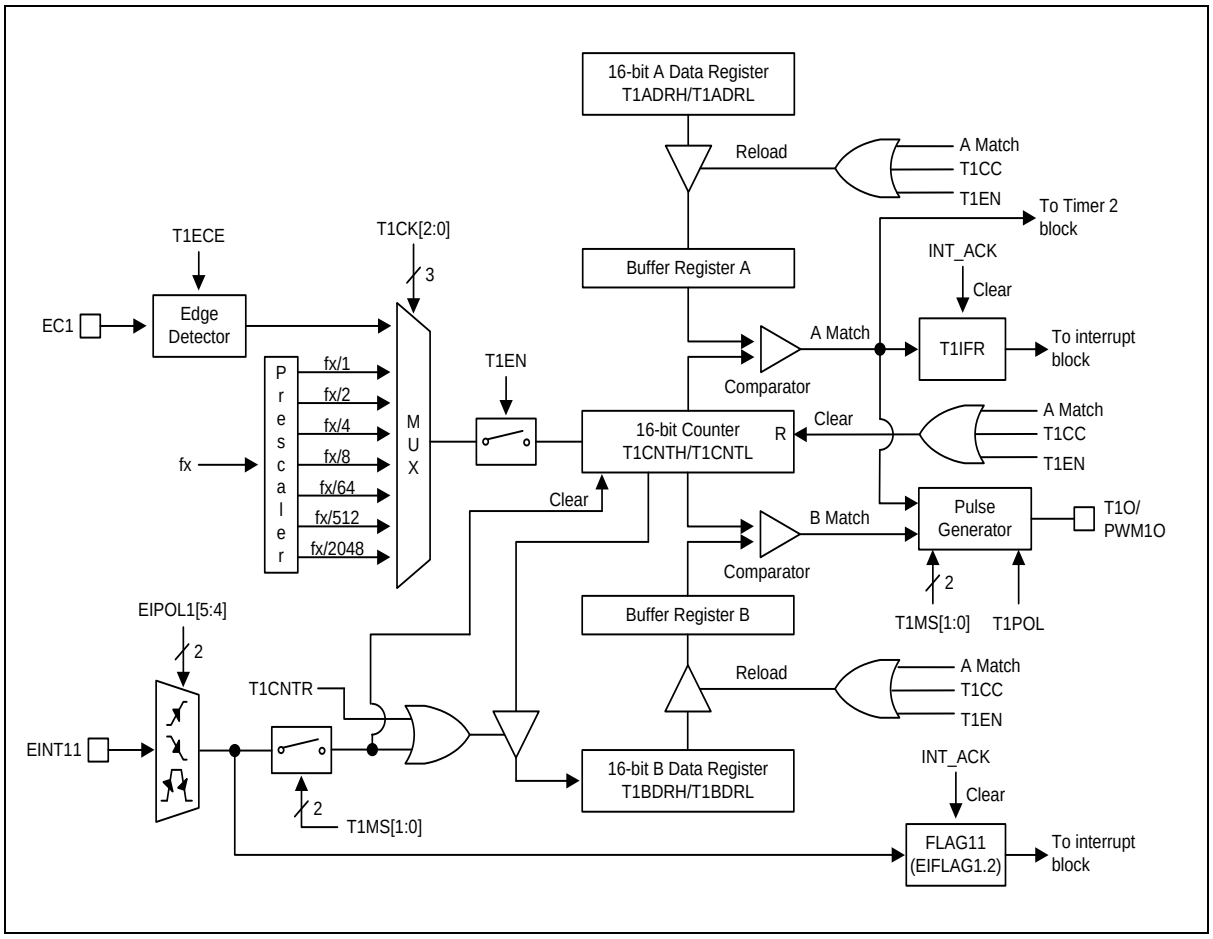


Figure 22. 16-bit Timer 1 Block Diagram

12.3 Timer 2

A 16-bit timer 2 consists of a multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

Timer 2 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be a divided clock of a system clock which is selected from prescaler output and T1 A Match (timer 1 A match signal). The clock source is selected by a clock selection logic, controlled by clock selection bits (T2CK[2:0]).

- TIMER 2 clock source: fX/1, fX/2, fX/4,fX/8,fX/32, fX/128, fX/512 and T1 A Match

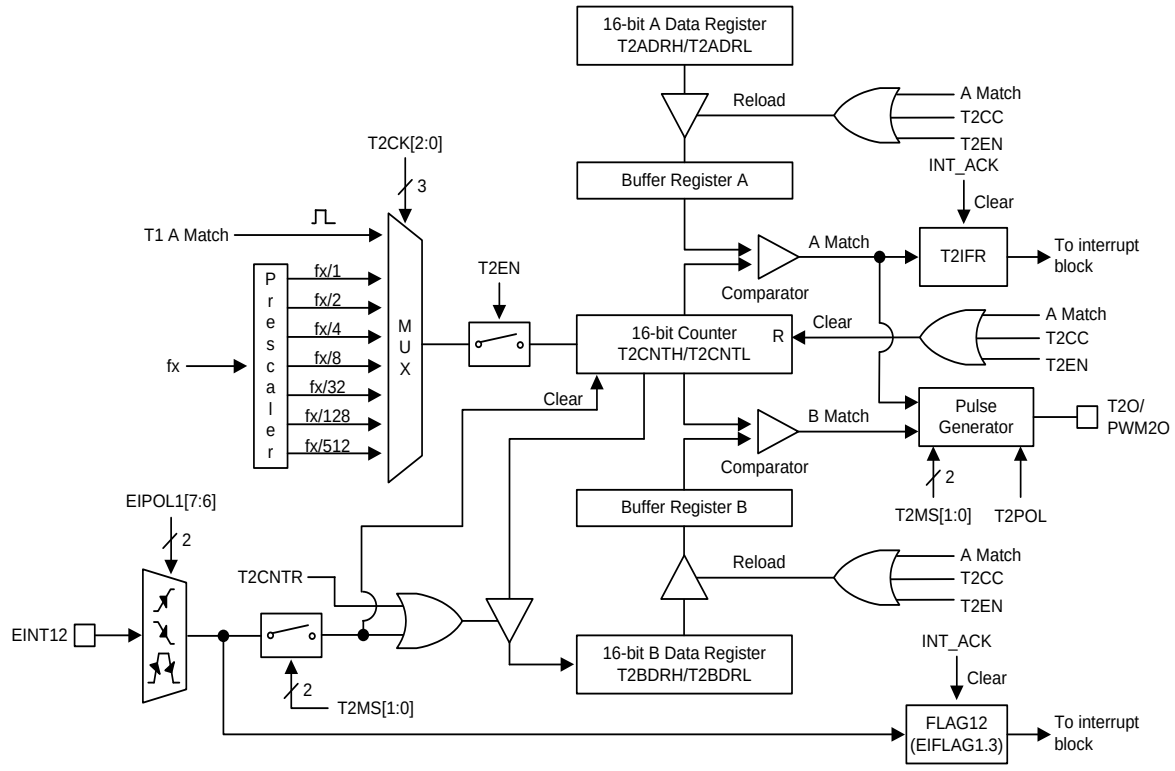
In capture mode, data is captured into input capture data registers (T2BDRH/T2BDRL) by EINT12. In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. In addition, the timer 2 outputs PWM waveform to PWM2O port in the PPG mode.

Table 11. TIMER 2 Operating Modes

T2EN	P1FSRL[3:2]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.3.1 16-bit timer 2 block diagram

In this section, a 16-bit timer 2 is described in a block diagram.



NOTE: T1 A Match is a pulse for the timer 2 clock source if it is selected.

Figure 23. 16-bit Timer 2 Block Diagram

12.4 Timer 3

A 16-bit timer 3 consists of a multiplexer, timer 3 A data high/low register, timer 3 B data high/low register and timer 3 control high/low register (T3ADRH, T3ADRL, T3BDRH, T3BDRL, T3CRH, and T3CRL).

Timer 3 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 3 can be clocked by an internal or an external clock source (EC3). The clock source is selected by a clock selection logic controlled by clock selection bits (T3CK[2:0]).

- TIMER 3 clock source: fX/1, fX/2, fX/4,fX/8,fX/64, fX/512, fX/2048 and EC3

In capture mode, data is captured into input capture data registers (T3BDRH/T3BDRL) by EINT3. Timer 3 results in the comparison between counter and data register through T3O port in timer/counter mode. In addition, timer 3 outputs PWM waveform through PWM3O port in the PPG mode.

Table 12. TIMER 3 Operating Modes

T3EN	P0FSRH[1:0]	T3MS[1:0]	T3CK[2:0]	Timer 3
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.4.1 16-bit timer 3 block diagram

In this section, a 16-bit timer 3 is described in a block diagram.

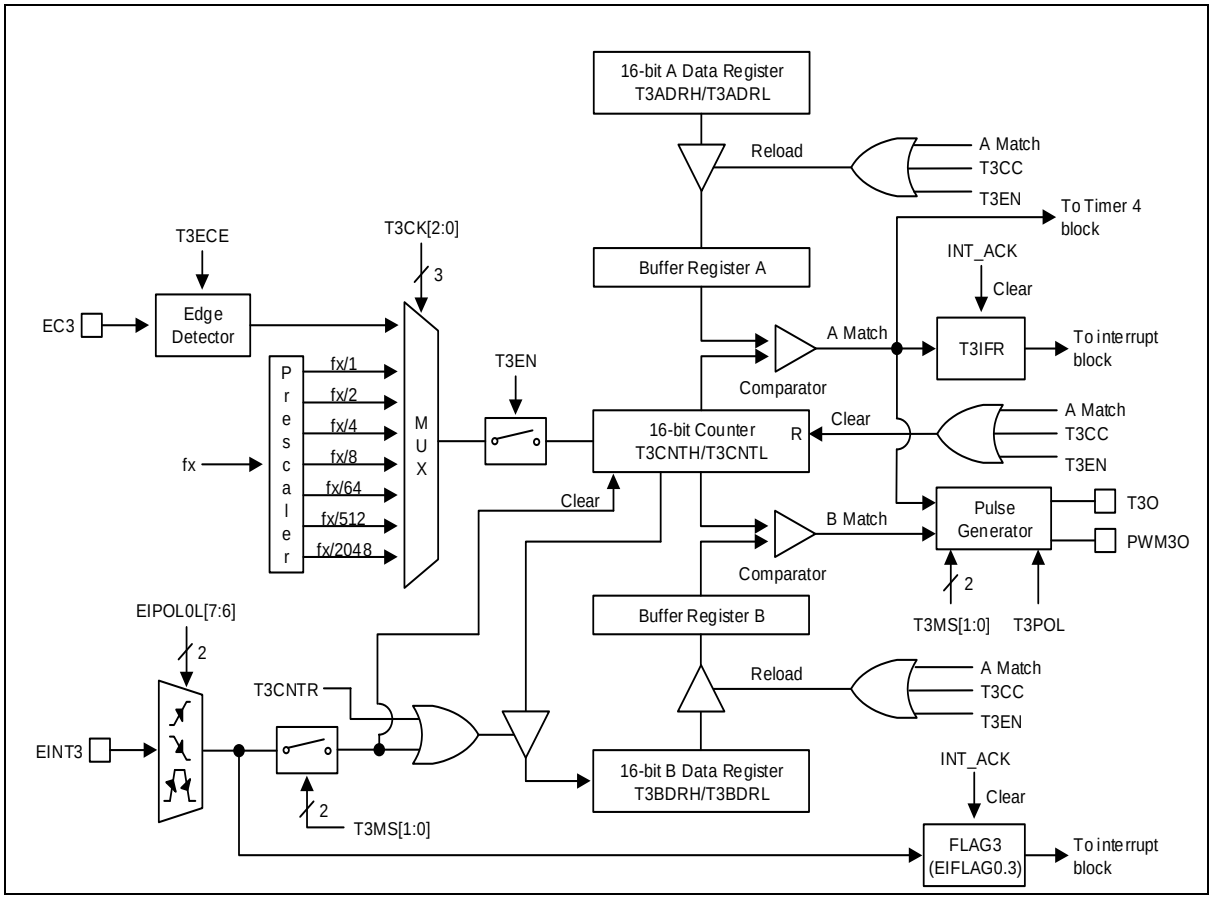


Figure 24. 16-bit Timer 3 Block Diagram

12.5 Timer 4

A 16-bit timer 4 consists of a multiplexer, timer 4 A data high/low register, timer 4 B data high/low register and timer 4 control high/low register (T4ADRH, T4ADRL, T4BDRH, T4BDRL, T4CRH, and T4CRL).

Timer 4 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 4 can be a divided clock of a system clock selected from prescaler output and T3 A Match (timer 3 A match signal). The clock source is selected by a clock selection logic controlled by clock selection bits (T4CK[2:0]).

- TIMER 4 clock source: fX/1, fX/2, fX/4, fX/8, fX/32, fX/128, fX/512 and T3 A Match

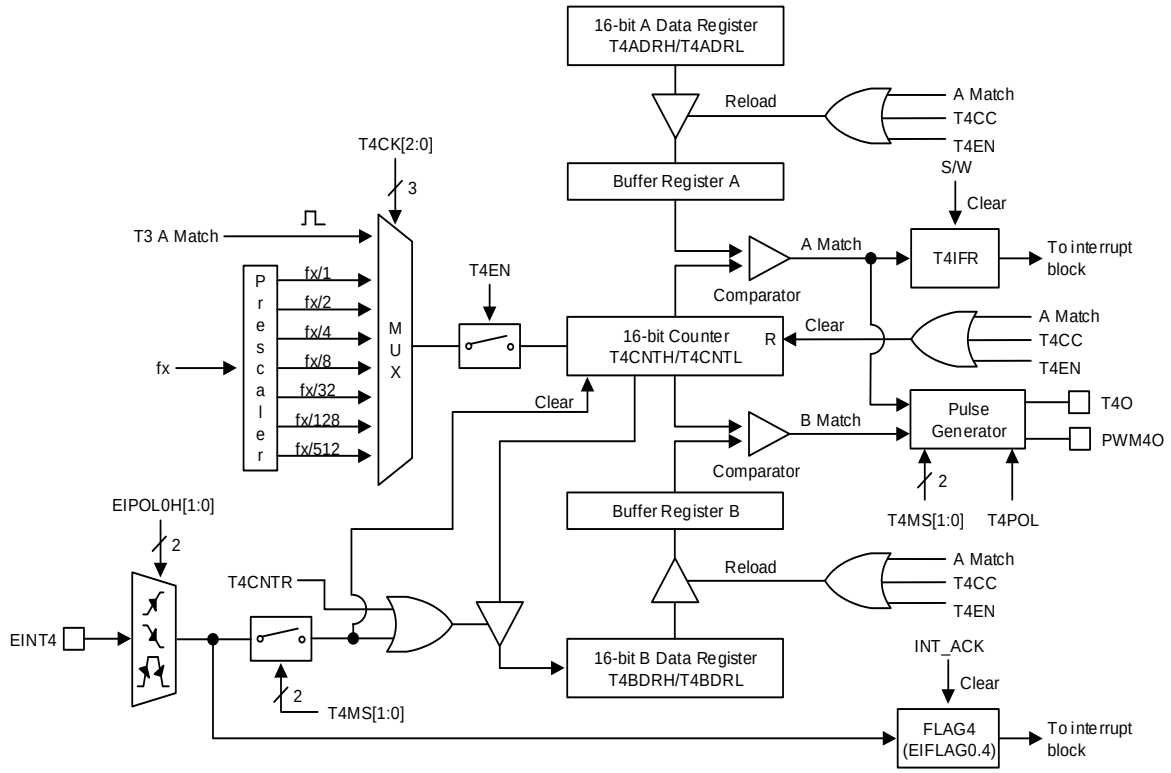
In capture mode, data is captured into input capture data registers (T4BDRH/T4BDRL) by EINT4. In timer/counter mode, whenever counter value is equal to T4ADRH/L, T4O port toggles. In addition, the TIMER 4 outputs PWM waveform to PWM4O port in the PPG mode.

Table 13. TIMER 4 Operating Modes

T4EN	P0FSRH[3:2]	T4MS[1:0]	T4CK[2:0]	Timer 4
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.5.1 16-bit timer 4 block diagram

In this section, a 16-bit timer 4 is described in a block diagram.



NOTE: T3 A Match is a pulse for the timer 4 clock source if it is selected.

Figure 25. 16-bit Timer 4 Block Diagram

12.6 Timer 5

A 16-bit timer 5 consists of a multiplexer, timer 5 A data high/low register, timer 5 B data high/low register and timer 5 control high/low register (T5ADRH, T5ADRL, T5BDRH, T5BDRL, T5CRH, and T5CRL).

Timer 5 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 5 can be a divided clock of a system clock selected from prescaler output. The clock source is selected by a clock selection logic controlled by clock selection bits (T5CK[2:0]).

- TIMER 5 clock source: fX/1, fX/2, fX/4, fX/8, fX/32, fX/128, fX/512 and HSI
-

In capture mode, data is captured into input capture data registers (T5BDRH/T5BDRL) by EINT5. In timer/counter mode, whenever counter value is equal to T5ADRH/L, T5O port toggles. In addition, the TIMER 5 outputs PWM waveform to PWM5O port in the PPG mode.

Table 14. TIMER 5 Operating Modes

T5EN	P0FSRH[5:4]	T5MS[1:0]	T5CK[2:0]	Timer 5
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.6.1 16-bit timer 5 block diagram

In this section, a 16-bit timer 5 is described in a block diagram.

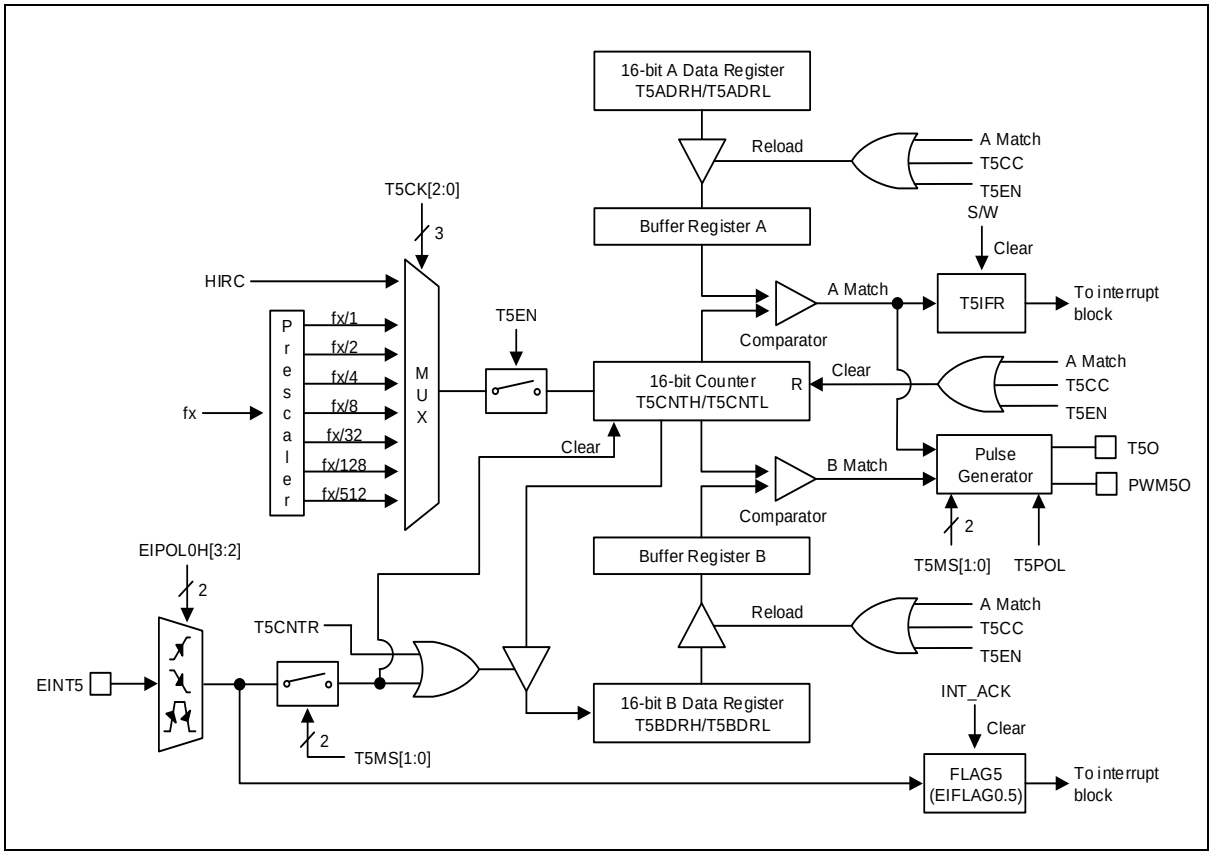


Figure 26. 16-bit Timer 5 Block Diagram

13 Buzzer driver

A buzzer of A96G140/A96G148/A96A148 consists of 8-bit counter, a buzzer data register (BUZDR), and a buzzer control register (BUZCR). It outputs square wave (61.035Hz to 125.0kHz @ 8MHz) through P13/AN10/EC1/BUZO pin, and its buzzer data register (BUZDR) controls the buzzer frequency (refer to the following expression). In a buzzer control register (BUZCR), BUCK[1:0] bits select a source clock divided by prescaler.

Table 15. Buzzer Frequency at 8MHz

$$f_{BUZ}(Hz) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125kHz	62.5kHz	31.25kHz	15.625kHz
0000_0001	62.5kHz	31.25kHz	15.625kHz	7.812kHz
...	…	…	…	…
1111_1101	492.126Hz	246.063Hz	123.031Hz	61.515Hz
1111_1110	490.196Hz	245.098Hz	122.549Hz	61.274Hz
1111_1111	488.281Hz	244.141Hz	122.07Hz	61.035Hz

13.1 Buzzer driver block diagram

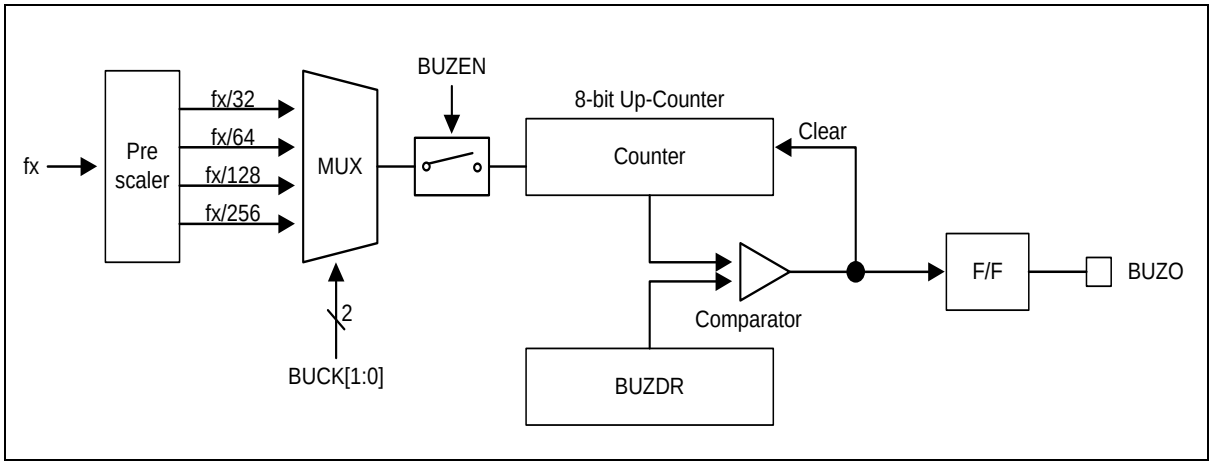


Figure 27. Buzzer Driver Block Diagram

14 12-bit ADC

Analog-to-digital converter (ADC) of A96G140/A96G148/A96A148 allows conversion of an analog input signal to corresponding 12-bit digital value. This A/D module has eight analog inputs. Output of the multiplexer becomes input into the converter which generates the result through successive approximation.

The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL).

ADSEL[3:0] bits are used to select channels to be converted. To execute A/D conversion, TRIG[2:0] bits should be set to ‘xxx’. Registers ADCDRH and ADCDRL contain the result of A/D conversion. When the conversion is completed, the result is loaded into ADCDRH and ADCDRL, A/D conversion status bit AFLAG is set to ‘1’, and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as ‘0’.

14.1 Block diagram

In this section, the 12-bit ADC is described in a block diagram, and an analog input pin and a power pin with capacitors respectively are introduced.

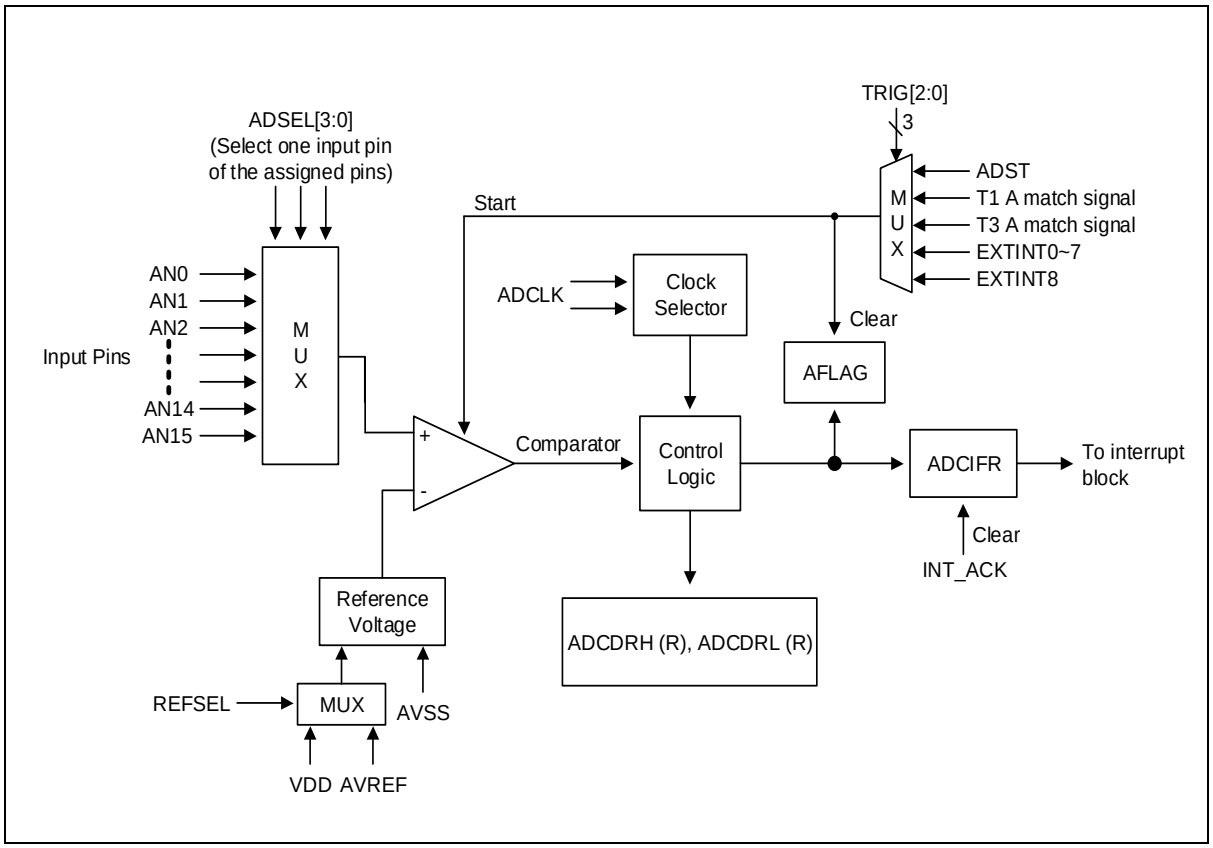


Figure 28. 12-bit ADC Block Diagram

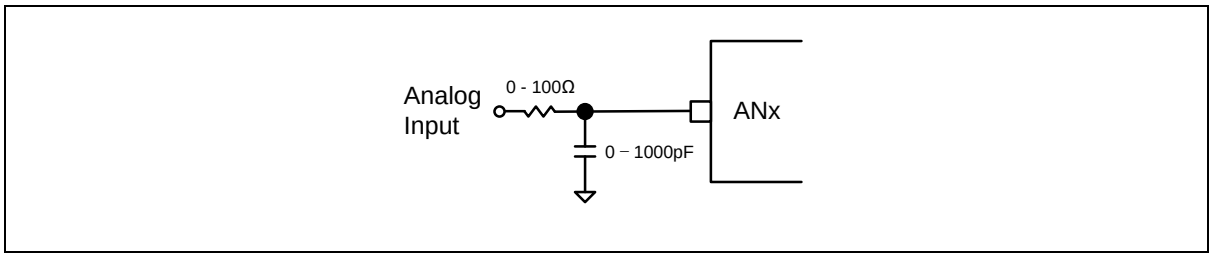


Figure 29. A/D Analog Input Pin with a Capacitor

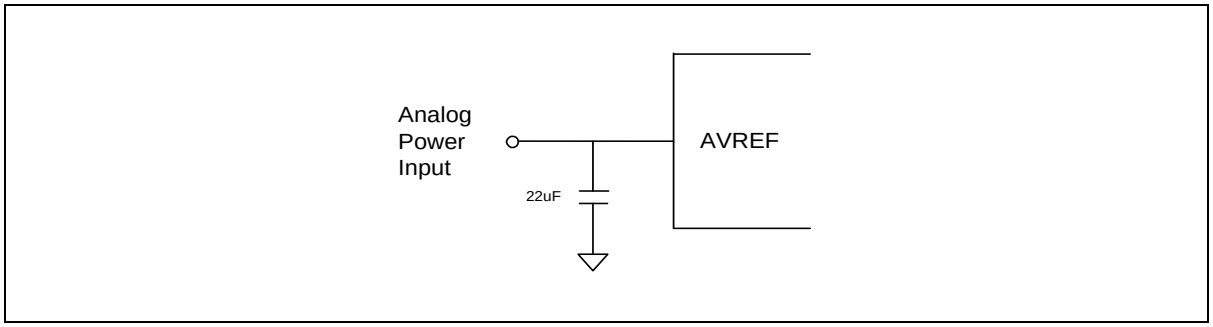


Figure 30. A/D Power (AVREF) Pin with a Capacitor

15 USI (USART + SPI + I2C)

USI stands for the combination of USART, SPI and I2C. A96G140/A96G148/A96A148 has two USI function blocks, USI0 and USI1, which are identical to each other functionally. Each USI block consists of USI control registers 1/2/3/4, USI status registers 1/2, USI baud-rate generation register, USI data register, USI SDA hold time register, USI SCL high period register, USI SCL low period register, and USI slave address register (USInCR1, USInCR2, USInCR3, USInCR4, USInST1, USInST2, USInBD, USInDR, USInSDHR, USInSCHR, USInSCLR, USInSAR). The ‘n’ means ‘0’ or ‘1’.

USI operates in one of the following modes selected by USIn selection bits (USInMS[1:0]):

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode
- I2C mode

15.1 USIn UART mode

Universal synchronous and asynchronous serial receiver and transmitter (USART) are highly flexible serial communication devices. Main features are listed below:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check are Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode

The USIn comprises clock generator, transmitter and receiver. Clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. A write buffer allows continuous transfer of data without any delay between frames.

Receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USInDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors.

15.2 USIn UART block diagram

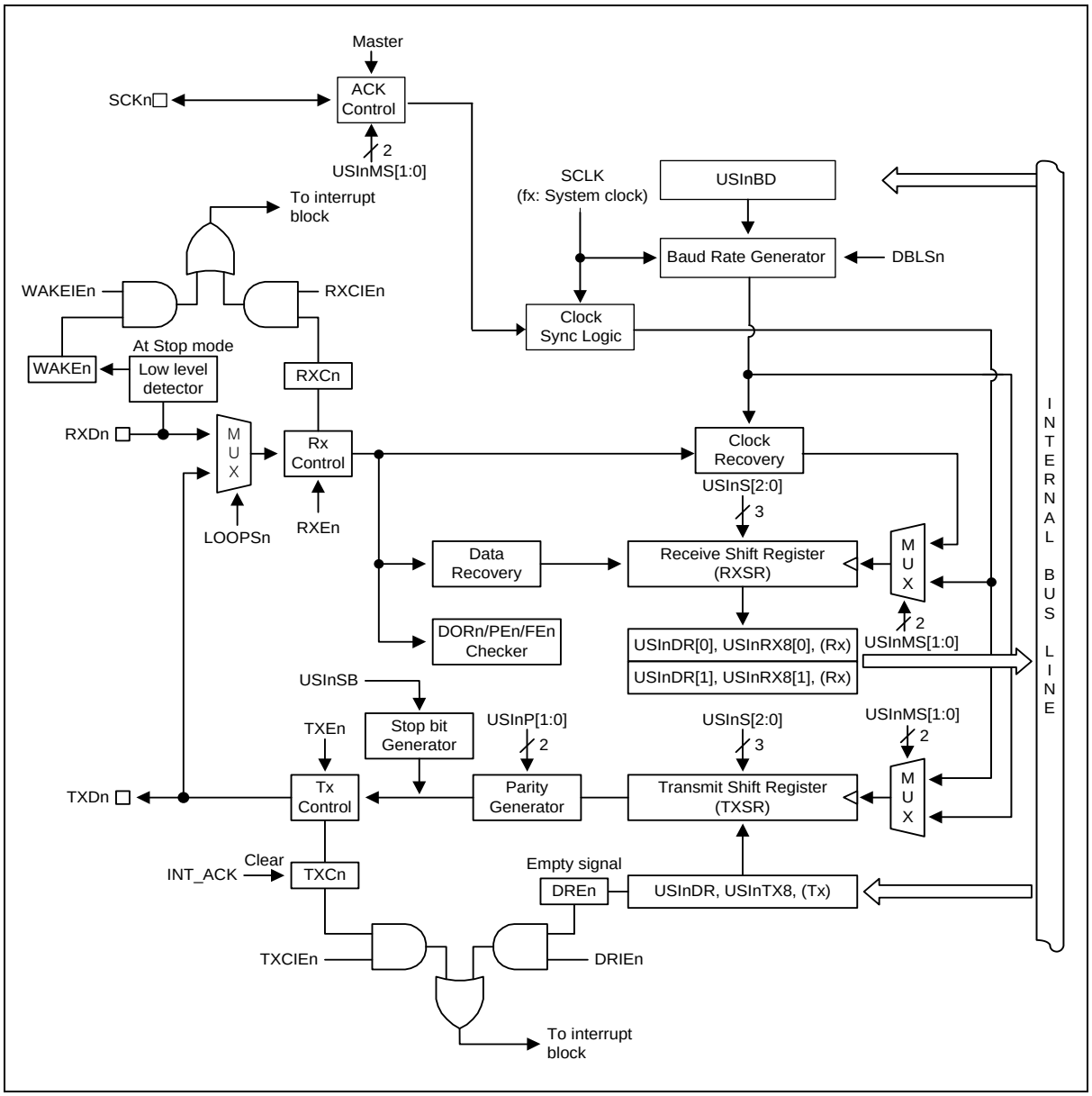


Figure 31. USIn USART Block Diagram (n = 0 and 1)

15.3 USIn SPI mode

The USIn can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

- Full duplex, three-wire synchronous data transfer
- Master and slave operation
- Supports all four SPIn modes of operation (mode 0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USInMS[1:0]=”11”), the slave select (SSn) pin becomes active LOW input in slave mode operation, or can be output in master mode operation if USInSSEN bit is set to ‘0’.

Note that during SPI mode of operation, the pin RXDn is renamed as MISOn and TXDn is renamed as MOSIn for compatibility to other SPI devices.

15.4 USIn SPI block diagram

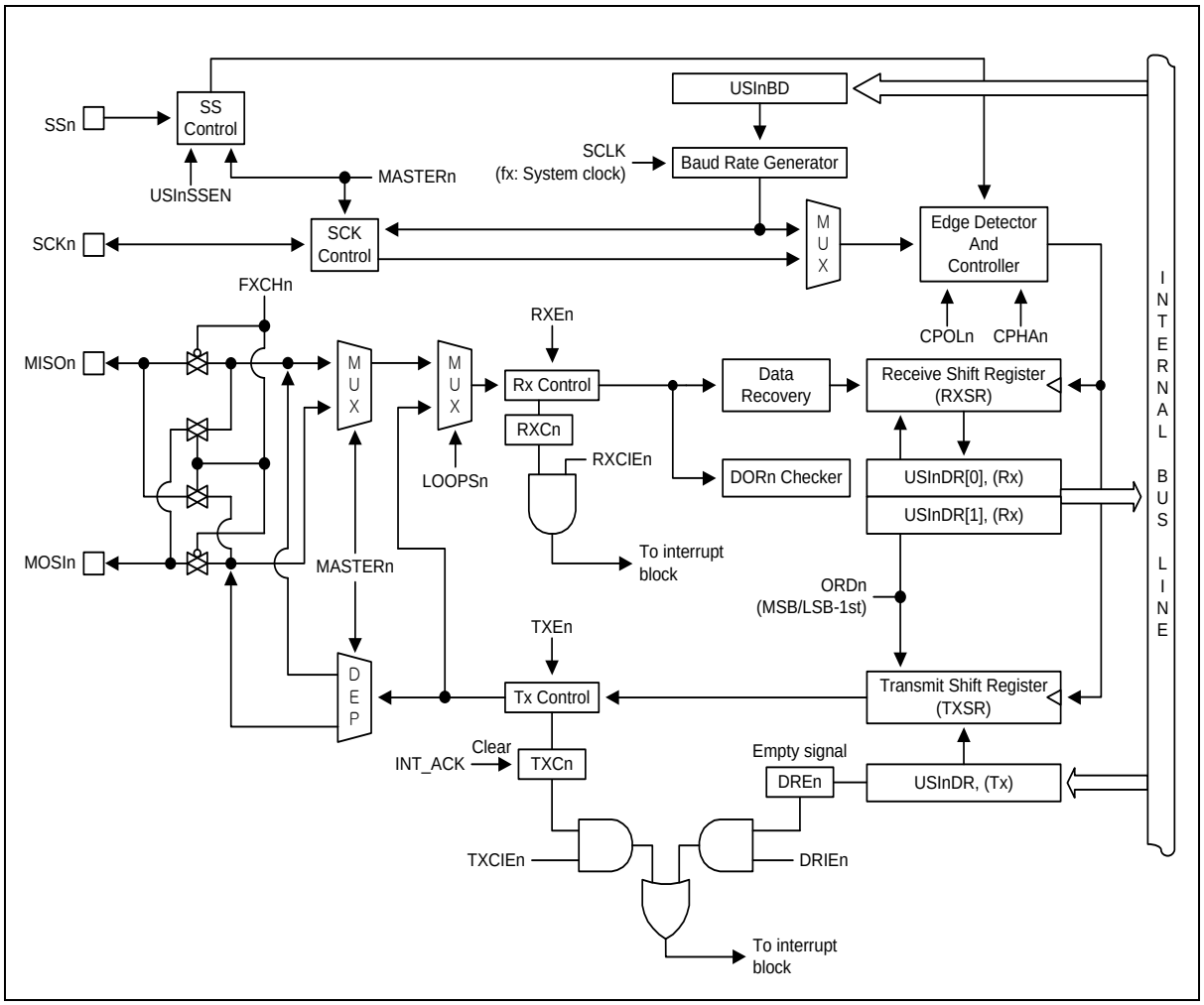


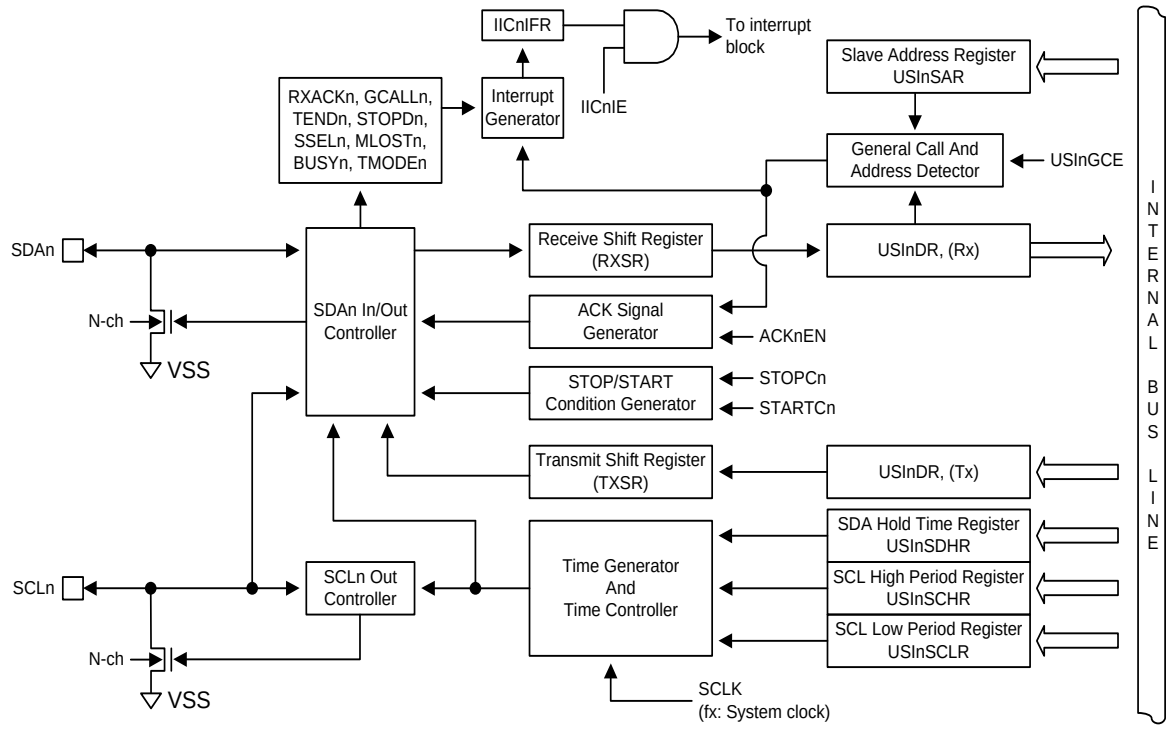
Figure 32. USIn SPI Block Diagram (n = 0 and 1)

15.5 USIn I2C mode

The USIn can be set to operate in industrial standard serial communication protocols mode. The I2C mode uses 2 bus lines serial data line (SDAn) and serial clock line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer read speed
- 7 bit address
- Both master and slave operation
- Bus busy detection

15.6 USIn I2C block diagram



NOTE: When the USIn block is an I2C mode and the corresponding port is a sub-function for SCLn/SDAn pin, The SCLn/SDAn pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 33. USIn I2C Block Diagram

16 USART2

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. USART2 of A96G140/A96G148/A96A148 features the followings:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

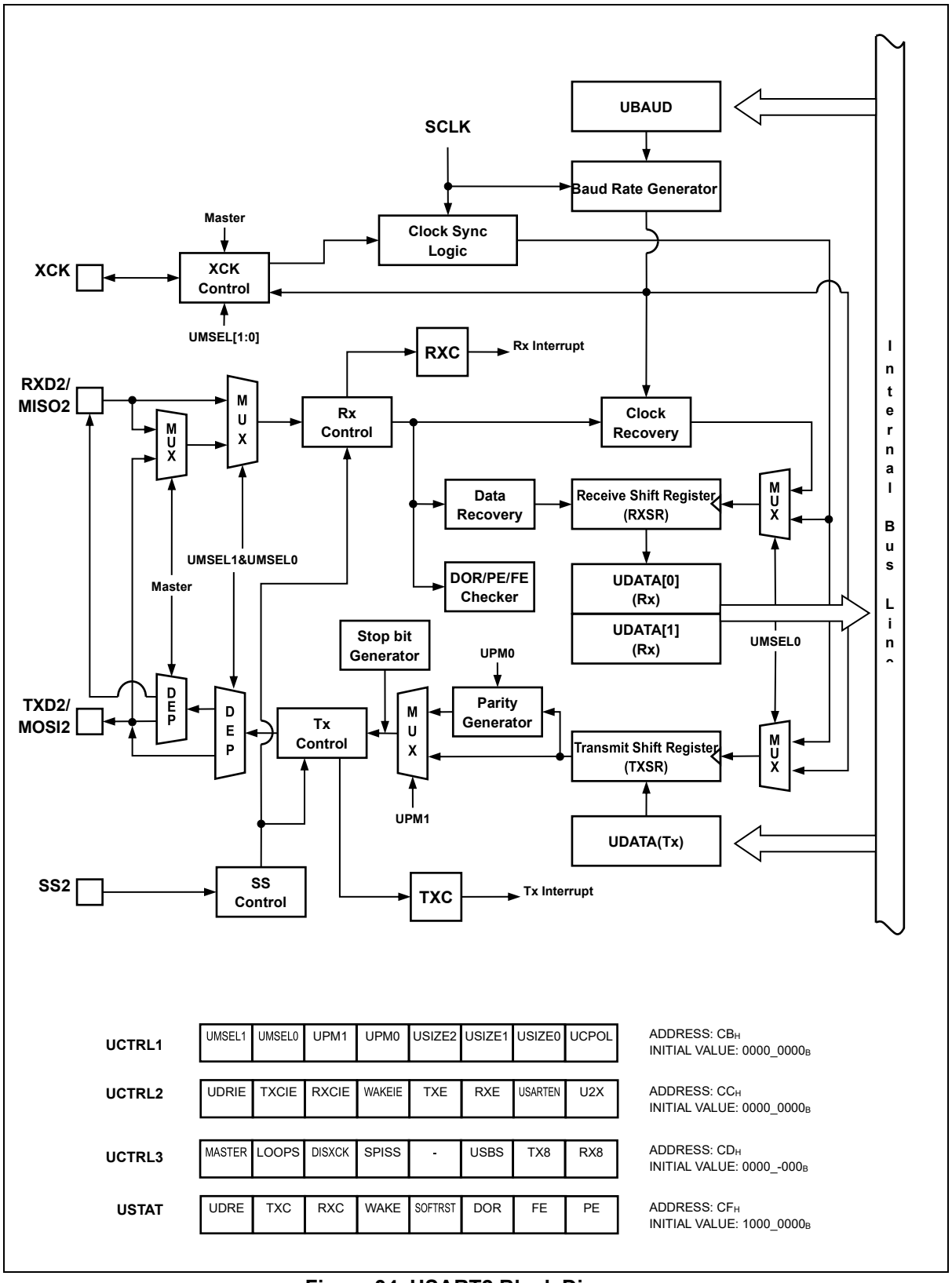
USART2 has three main parts such as a Clock Generator, Transmitter and Receiver.

Clock Generation logic consists of a synchronization logic for external clock input used by synchronous or SPI slave operation, and a baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

Receiver is the most complex part of the USART2 module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, the Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATA) and control logic. The Receiver supports the same frame formats as the Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

16.1 Block diagram



UCTRL1	UMSEL1	UMSEL0	UPM1	UPM0	USIZE2	USIZE1	USIZE0	UCPOL
UCTRL2	UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	USARTEN	U2X
UCTRL3	MASTER	LOOPS	DISXCK	SPISS	-	USBS	TX8	RX8
USTAT	UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE

ADDRESS: CB_H
INITIAL VALUE: 0000_0000_B

ADDRESS: CC_H
INITIAL VALUE: 0000_0000_B

ADDRESS: CD_H
INITIAL VALUE: 0000_-000_B

ADDRESS: CF_H
INITIAL VALUE: 1000_0000_B

Figure 34. USART2 Block Diagram

17 Power down operation

A96G140/A96G148/A96A148 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. A96G140/A96G148/A96A148 provides three kinds of power saving functions such as Main-IDLE mode, Sub-IDLE mode and STOP mode. During one of these three modes, program will be stopped.

17.1 Peripheral operation in IDLE/ STOP mode

Table 38 shows operation status of each peripheral in IDLE mode and STOP mode.

Table 16. Peripheral Operation Status during Power Down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU operations are disabled.	ALL CPU operations are disabled.
RAM	Retains.	Retains.
Basic Interval Timer	Operates continuously.	Stops (can be operated with WDTRC OSC).
Watch Dog Timer	Operates continuously.	Stops (can be operated with WDTRC OSC).
Watch Timer	Operates continuously.	Stops (can be operated with sub clock).
Timer0~4	Operates continuously.	Halts (only when the event counter mode is enabled, timer operates normally).
ADC	Operates continuously.	Stops.
BUZ	Operates continuously.	Stops.
USI0/1	Operates continuously.	Only operates with external clock.
Internal OSC (32MHz)	Oscillates.	Stops when the system clock (fx) is fHSI.
WDTRC OSC (128kHz)	Can be operated with setting value.	Can be operated programmable.
Main OSC (0.4~12MHz)	Oscillates.	Stops when fx = fXIN.
Sub OSC (32.768kHz)	Oscillates.	Can be operated programmable.
I/O Port	Retains.	Retains.
Control Register	Retains.	Retains.
Address Data Bus	Retains.	Retains.

Table 16. Peripheral Operation Status during Power Down Mode (continued)

Peripheral	IDLE mode	STOP mode
Release Method	• By RESET • All Interrupts	• By RESET • Timer Interrupt (EC0, EC1, EC3) • External Interrupt • USART2 by RX, WT (sub clock), WDT • USI0/1 by RX, I2C(Slave mode)

18 Reset

Table 40 shows hardware setting values of main peripherals.

Table 17. Hardware Setting Values in Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

A96G140/A96G148/A96A148 has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

18.1 Reset block diagram

In this section, reset unit is described in a block diagram.

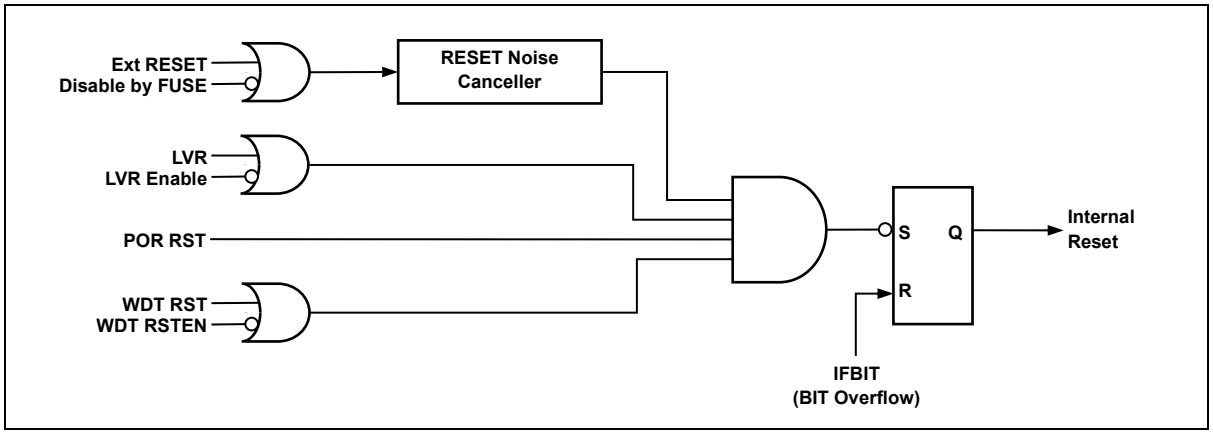


Figure 35. Reset Block Diagram

19 Memory programming

A96G140/A96G148/A96A148 has flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

Flash of A96G140/A96G148/A96A148 features the followings:

- Flash Size : 64Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 30,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

19.1 Memory map

19.1.1 Flash memory map

Program memory uses 64K bytes of flash memory. It is read by byte and written by byte or page. One page is 64-bytes

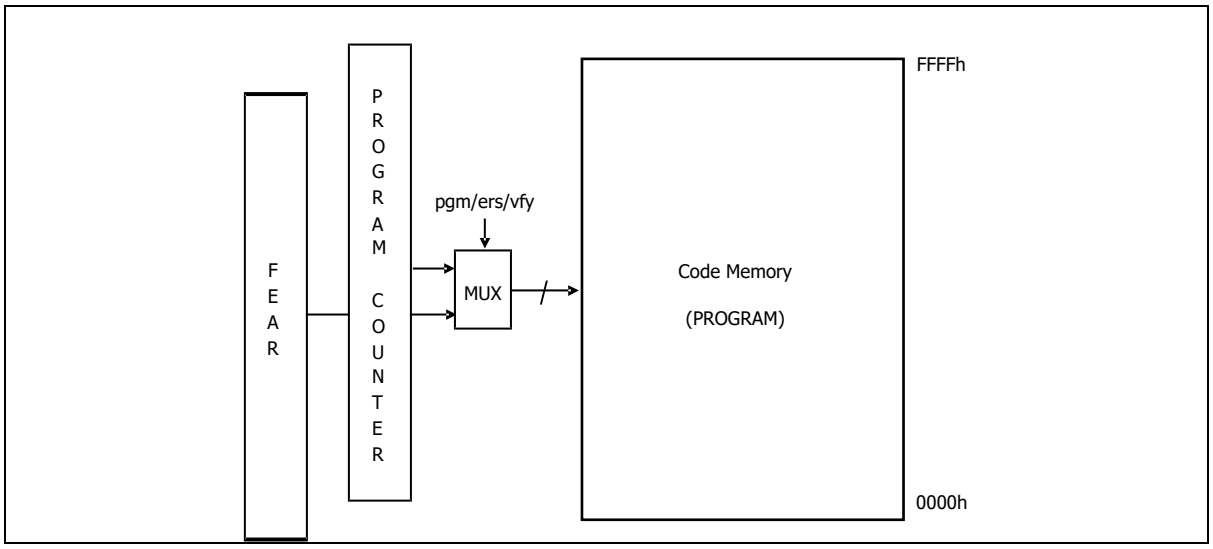


Figure 36. Flash Memory Map

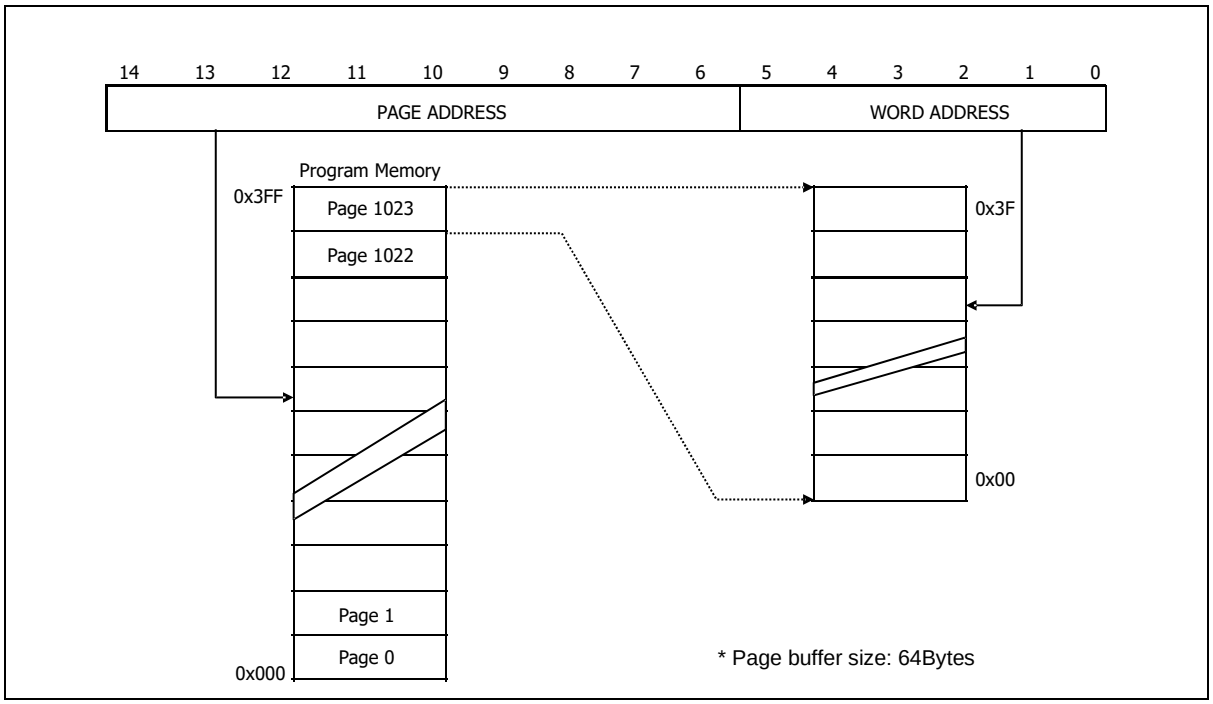


Figure 37. Address Configuration of Flash Memory

20 Electrical characteristics

20.1 Absolute maximum ratings

Table 18. Absolute Maximum Ratings

Parameter	Symbol	Rating[NOTE2]	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	42.5	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	112	mA	Maximum current ($\sum I_{OH}$)
	I_{OL1}	50	mA	Maximum current (I_{OL1} per I/O pin)
	$\sum I_{OL1}$	101	mA	Maximum current ($\sum I_{OL1}$)
	I_{OL2}	160	mA	Maximum current sunk by (I_{OL2} per I/O pin)
	$\sum I_{OL2}$	160	mA	Maximum current by LED Drive ($\sum I_{OL2}$)
Total Power Dissipation	P_T	800	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

NOTE:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The measured value for the parameters and conditions listed were confirmed by simulation.

20.2 Recommended operating conditions

Table 19. Recommended Operating Conditions

(T_A=-40°C ~ 85°C or T_A=-40°C ~ 105°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 32 ~ 38kHz	Sub Crystal	1.8	–	5.5	V
		f_X= 4 ~10MHz	Main Crystal	2.2	–	5.5	
		f_X= 4 ~12MHz		2.4	–	5.5	
		f_X= 0.5~16 MHz	Internal RC	1.8	–	5.5	
Operating Temperature	T_{OPR}	VDD=1.8~5.5V		-40	–	85	°C
				-40	–	105	

20.3 A/D converter characteristics

Table 20. A/D Converter Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=2.5V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Integral Linear Error	ILE	VDD=AVDD= 5.0V MCLK = 8MHz		–	±4	±8	LSB
Differential Linearity Error	DLE			–	±1	±2	
Offset Error of Top	EOT			–	±4	±8	
Offset Error of Bottom	EOB			–	±2	±4	
Conversion Time	t_{CON}	12-bit resolution, 8MHz		7.5	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		1.8	–	VDD	
Analog Input Leakage Current	I_{AN}	VDDREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}[NOTE4]	Enable	VDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

NOTES:

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.5V, the ADC resolution is worse.
4. The measured value for the parameters and conditions listed were confirmed by simulation.

20.4 Power on reset characteristics

Table 21. Power-on Reset Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR} NOTE	–	–	1.32	–	V
VDD Voltage Rising Time	t_R NOTE	–	0.05	–	50.0	V/ms
Minimum Pulse Width	t_{LW} NOTE	–	100			us
POR Current	I_{POR} NOTE	–	–	0.2	–	uA

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

20.5 Low voltage reset and low voltage indicator characteristics

Table 22. LVR and LVI Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels. But LVI can select other levels except 1.61/1.68/1.77V because the minimum operation voltage is 1.8V. VLVR/VLVI can be measured when voltage drops (falling level).		-	1.61	1.75	V
				1.55	1.68	1.81	
				1.63	1.77	1.91	
				1.73	1.88	2.03	
				1.84	2.00	2.16	
				1.96	2.13	2.30	
				2.10	2.28	2.46	
				2.26	2.46	2.66	
				2.47	2.68	2.89	
				2.59	2.81	3.03	
				2.82	3.06	3.30	
				2.95	3.21	3.47	
				3.28	3.56	3.84	
				3.43	3.73	4.03	
				3.60	3.91	4.22	
				3.91	4.25	4.59	
Hysteresis	△V	–		–	30	180	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

20.6 High Speed Internal RC oscillator characteristics

Table 23. High Speed Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.0 – 5.5V		–	32	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -10°C to +70°C				±2.0	
		T_A = -40°C to +85°C				±2.5	
		T_A = -40°C to +105°C				±5.0	
Clock Duty Ratio	TOD NOTE2	–		40	50	60	%
Stabilization Time	T_{HFS} NOTE2	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

NOTES:

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.
2. The measured value for the parameters and conditions listed were confirmed by simulation.

20.7 Low Speed Internal RC oscillator characteristics

Table 24. Low Speed Internal Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	fLSI	TA=-40°C ~ +85°C	102	128	154	kHz
		TA=-40°C ~ +105°C	90	128	166	
Stabilization Time	TLSI NOTE2	–	–	–	1	ms
LSI Current	ILSI	Enable	–	1	–	uA
		Disable	–	–	0.1	

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

20.8 DC characteristics

Table 25. DC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage	V_{IH}	All input pins	0.7VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins	–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD=4.5V, I_{OH}=-8.57mA, All output ports;	VDD-1.0	–	–	V
	V_{OH2}	VDD=4.5V, I_{OH}= -19 mA, P3x High sink current output	VDD-2.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 10mA, All output ports except V_{OL2}	–	–	1.0	V
	V_{OL2}	VDD=5.0V, I_{OL}= 160mA, T_A= 25°C P3x High sink current output	–	1.5	3	V
Input High Leakage Current	I_{IH}	All input ports	–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports / VDD=5.0V	25	50	100	KΩ
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V	0.76	1.3	10.51	MΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25°C, VDD=5V	6.25	13.53	36.98	
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz, VDD= 5V	–	2.5	-	mA
		f_{XIN}= 8MHz, VDD= 5V	–	2.0	-	
		f_{XIN}= 4MHz, VDD= 5V	–	1.5	-	
		f_{HSI}= 16MHz, VDD= 5V	0.7	-	4.0	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz, VDD= 5V	–	1.8	-	mA

Table 25. DC Characteristics (continued)

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter[NOTE]	Symbol	Conditions	MIN	TYP	MAX	Unit
		f_{XIN}= 8MHz, VDD= 5V	–	1.5	-	
		f_{HSI}= 16MHz, VDD= 5V	0.5	-	3.0	
	I_{DD3} (STOP1)	STOP @ WDT on, VDD= 5.5V, T_A= 25°C	–	-	22.0	uA
	I_{DD4}	STOP @ WDT off & LVR off,	–	-	7.0	

	(STOP2)	VDD= 5.5V, T_A= 25°C				

NOTES:

1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{HSI} and f_{LSI} are an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

20.9 AC characteristics

Table 26. AC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RSL} **NOTE**	Input, VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{INTH} **NOTE**, t_{INTL} **NOTE**	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High,Low Pulse Width	t_{ECWH} **NOTE**, t_{ECWL} **NOTE**	ECn, V_{DD} = 5V (n= 0, 1, 3)	200	–	–	
External Counter Transition Time	t_{REC} **NOTE**, t_{FEC} **NOTE**	ECn, V_{DD} = 5V (n= 0, 1, 3)	20	–	–	

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

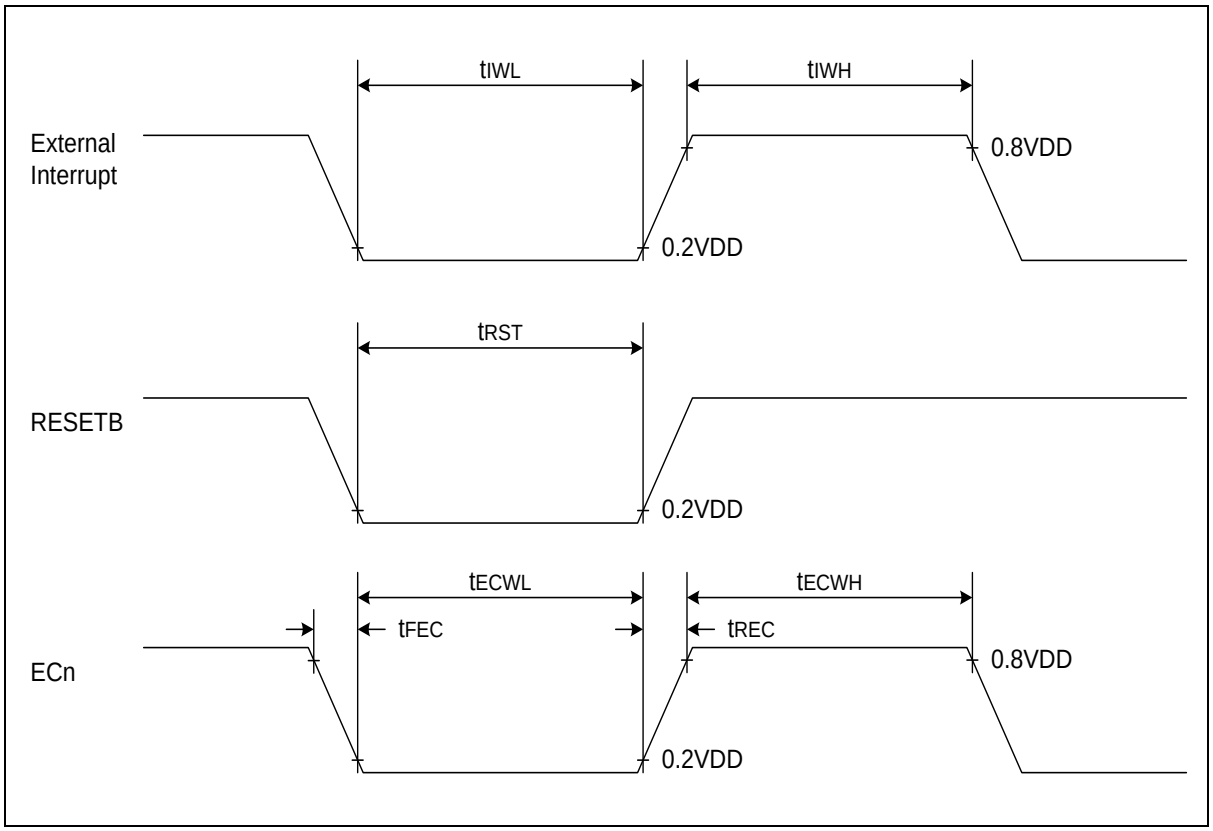


Figure 38. AC Timing

20.10 USART characteristics

The following table and figures show USART timing condition in SPI or Synchronous mode operation.

Table 27. USART Timing Characteristics in SYNC. or SPI Mode Operations

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter		Symbol	MIN	MAX	Unit
System clock period(0.5MHz~16MHz)		t_{SCLK}	62.5	2000	ns
Clock (XCK) period		t_{XCK}	4 x t_{SCLK}	1028 x t_{SCLK}	ns
Clock (XCK) high time		t_{XCKH}	2 x t_{SCLK}	514 x t_{SCLK}	ns
Clock (XCK) low time		t_{XCKL}	2 x t_{SCLK}	514 x t_{SCLK}	ns
Lead time	Master Slave	t_{LEAD} t_{LEAD}	0.5 x t_{XCK} 2 x t_{SCLK}	0.5 x t_{XCK} –	ns
Lag time	Master Slave	t_{LAG} t_{LAG}	0.5 x t_{XCK} 2 x t_{SCLK}	0.5 x t_{XCK} –	ns
Data setup time (inputs)	Master Slave	t_{SIM} t_{SIS}	2 x t_{SCLK} 2 x t_{SCLK}	2 x t_{SCLK} 2 x t_{SCLK}	ns
Data hold time (inputs)	Master Slave	t_{HIM} t_{HIS}	10 10	– –	ns
Data setup time (outputs)	Master Slave	t_{SOM} t_{SOS}	2 x t_{SCLK} 2 x t_{SCLK}	2 x t_{SCLK} 2 x t_{SCLK}	ns
Data hold time (outputs)	Master Slave	t_{HOM} t_{HOS}	-10 -10	– –	ns
Disable time		t_{DIS}	1 x t_{SCLK}	2 x t_{SCLK}	ns

NOTES:

1. In synchronous mode, Lead and Lag time for SS pin is ignored. And the case of “UCPHA=0” is also only applied to SPI mode
2. All timing is shown between 20% VDD and 80% VDD.

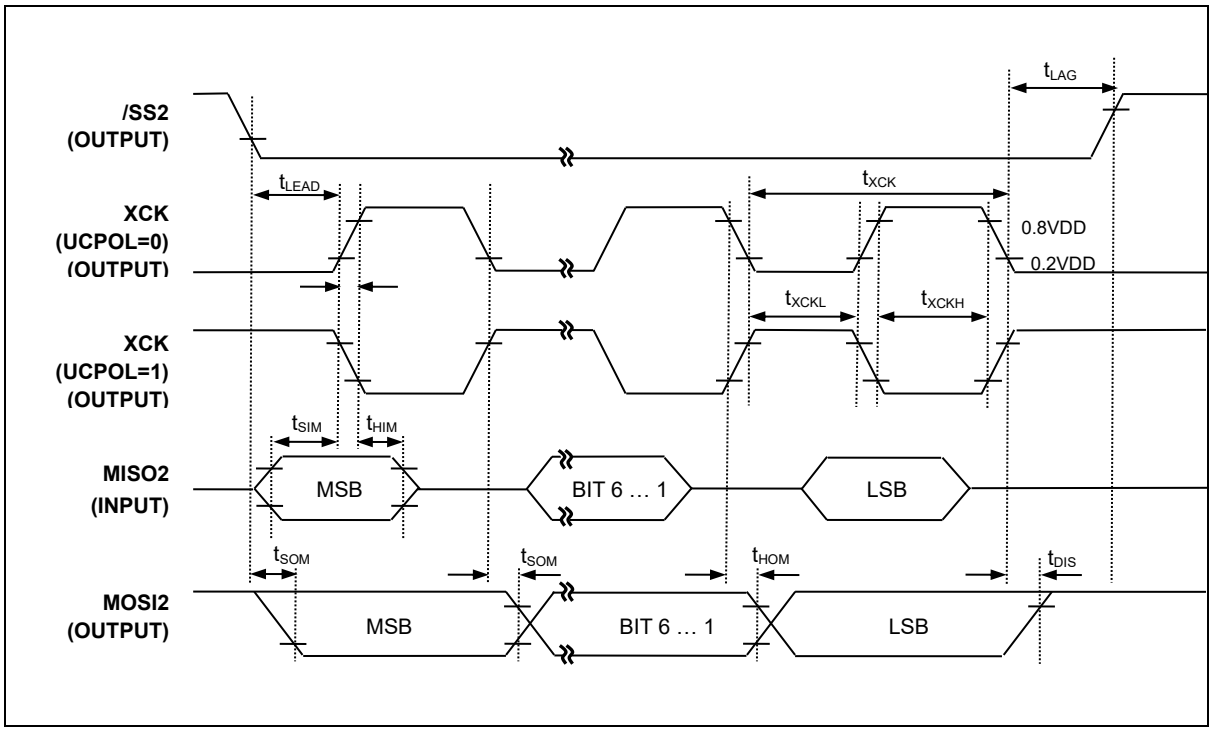
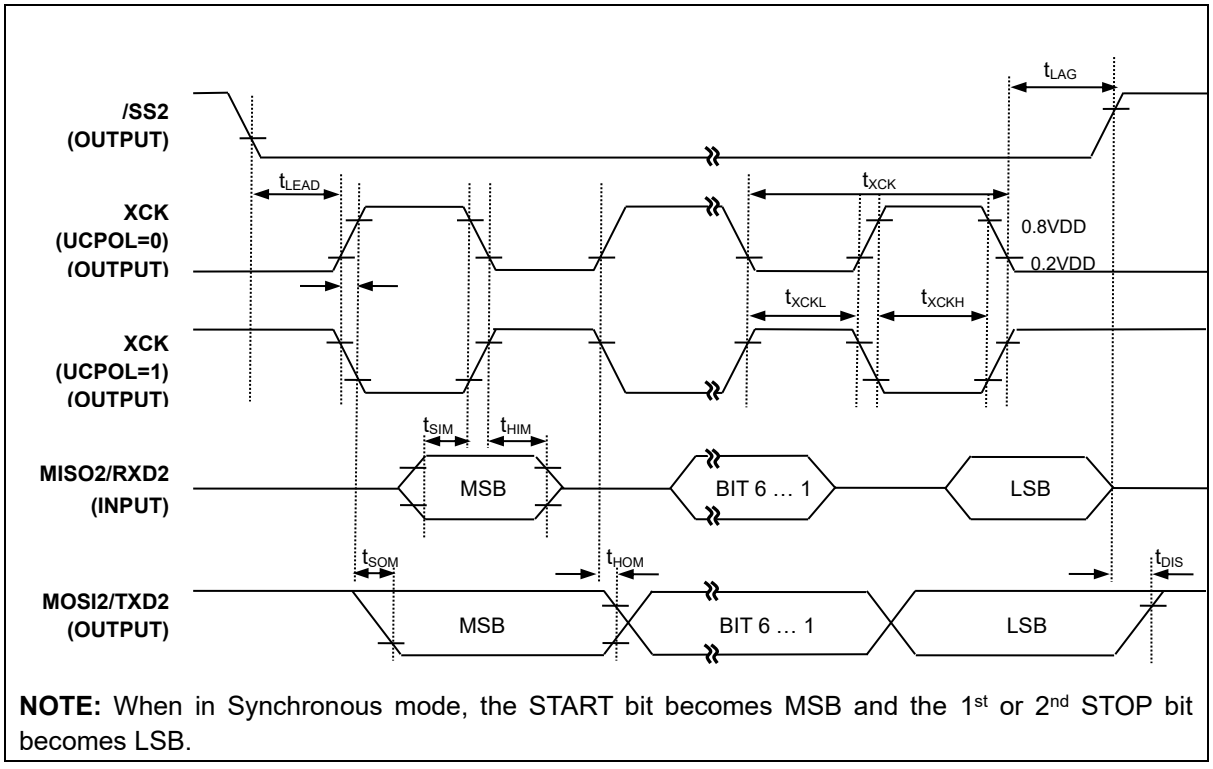


Figure 39. SPI master mode timing (UCPHA = 0, MSB first)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 40. SPI/Synchronous master mode timing (UCPHA = 1, MSB first)

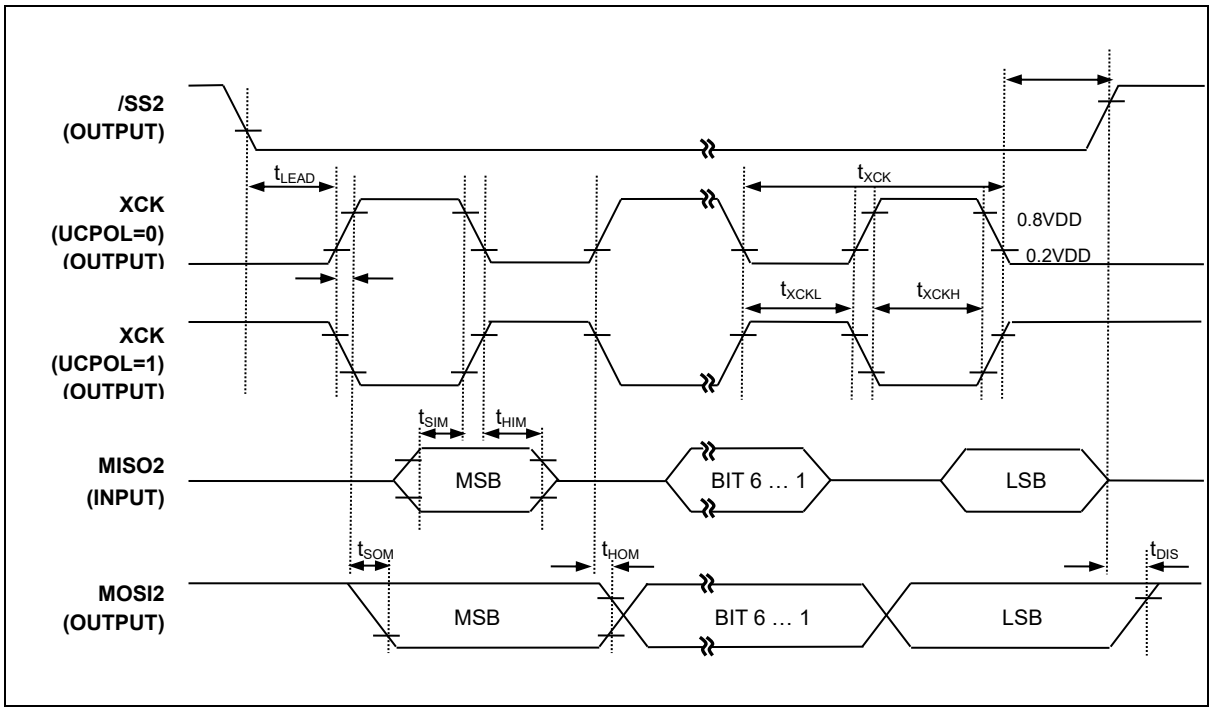
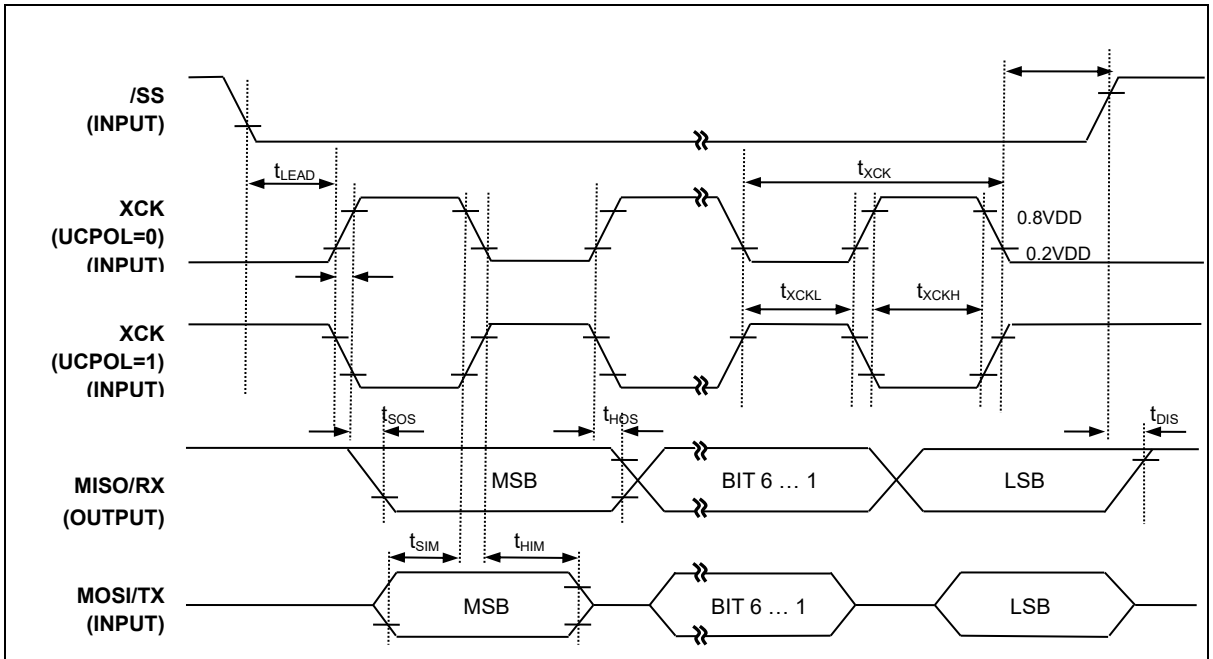


Figure 41 SPI slave mode timing (UCPHA = 0, MSB first)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 42 SPI/Synchronous slave mode timing (UCPHA = 1, MSB first)

20.11 SPI0/1 characteristics

Table 28. SPI0/1/2 Characteristics

(T_A=-40°C– +85°C or T_A=-40°C ~ 105°C, VDD=1.8V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK} NOTE	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL} NOTE	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD} NOTE	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS} NOTE	–	–	–	50	
Input Setup Time	t_{DIS} NOTE	–	100	–	–	
Input Hold Time	t_{DIH} NOTE	–	150	–	–	

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

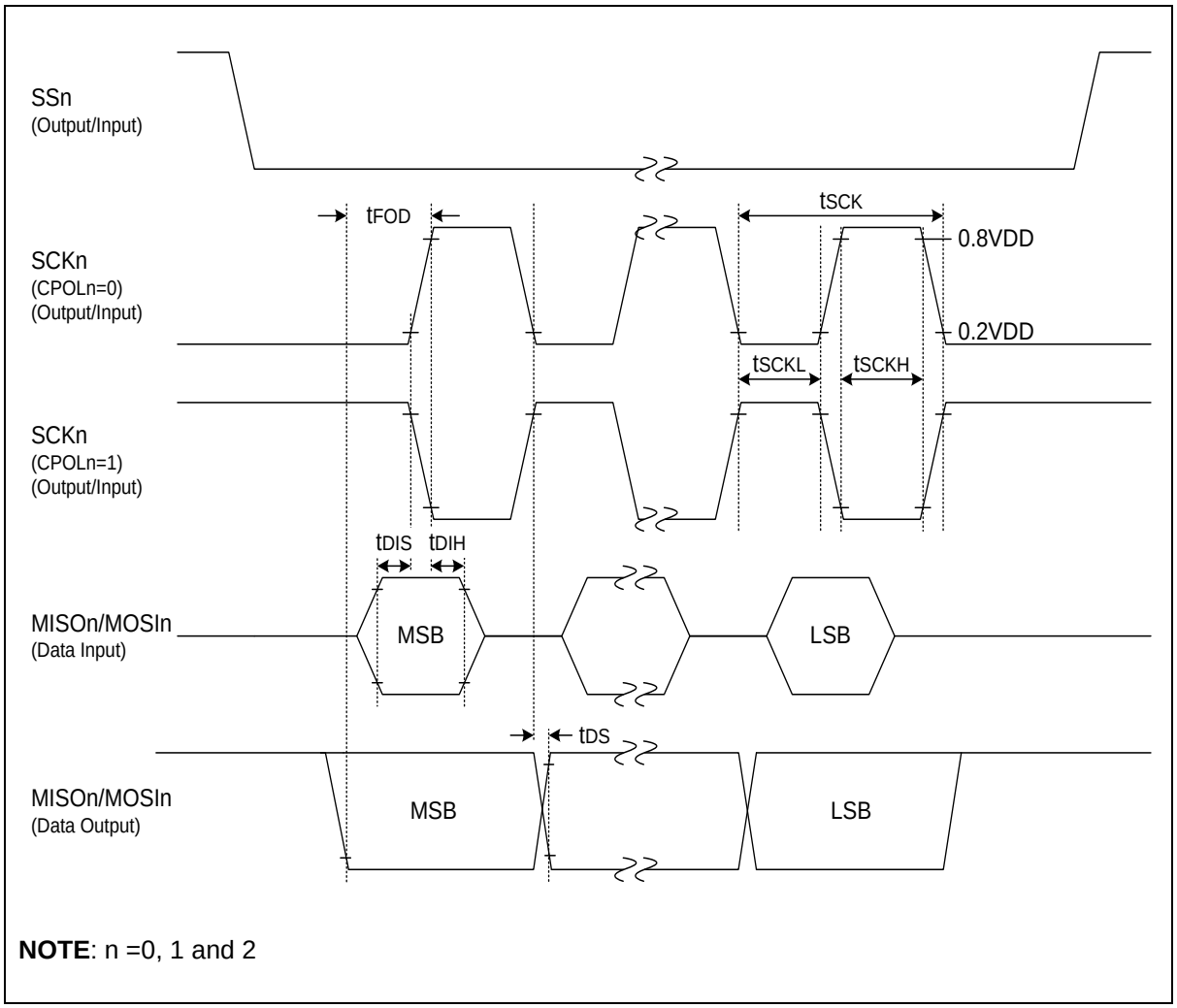


Figure 43. SPI0/1/2 Timing

20.12 UART0/1 characteristics

Table 29. UART0/1 Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, f_{XIN}=8MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	t_{CPU} x 16	2200	ns
Output data setup to clock rising edge	t_{S1}	810	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	t_{CPU} x 8	1280	ns

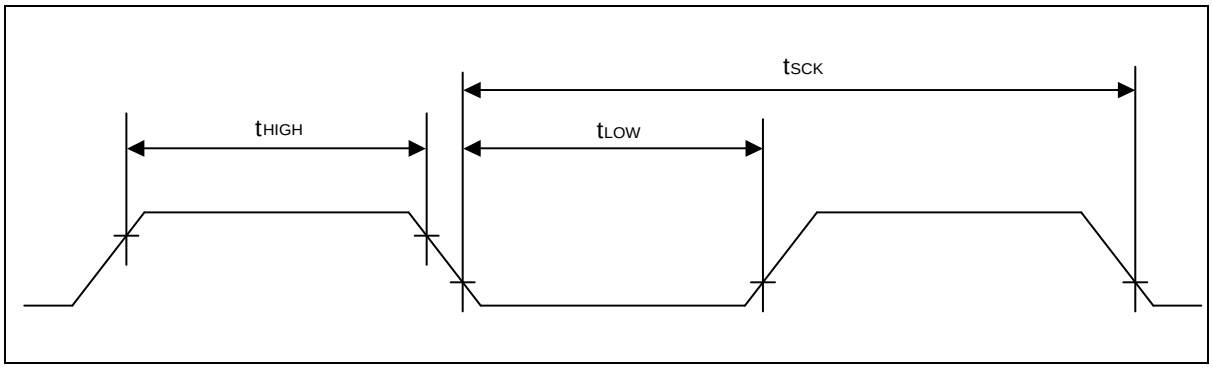


Figure 44. Waveform for UART0/1 Timing Characteristics

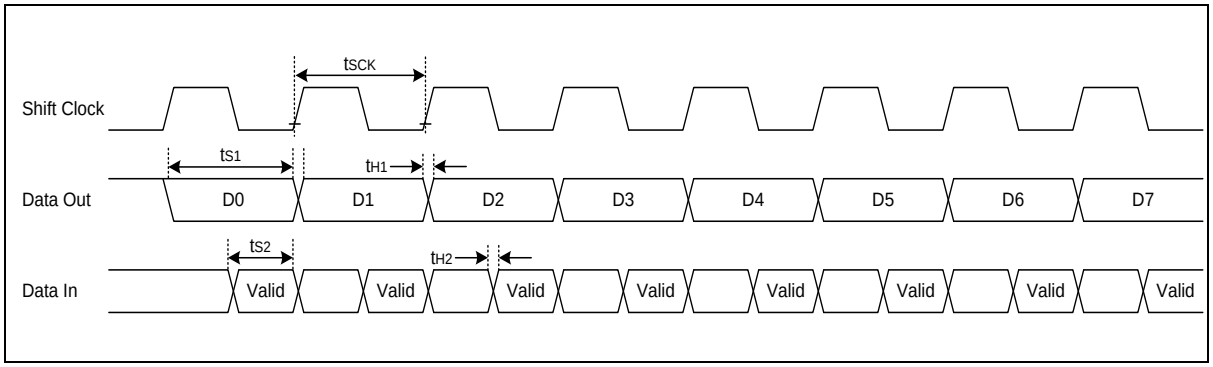


Figure 45. Timing Waveform for the UART0/1 Module

20.13 I2C0/1 characteristics

Table 30. I2C0/1 Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	tSCL[NOTE]	0	100	0	400	kHz
Clock High Pulse Width	tSCLH[NOTE]	4.0	–	0.6	–	us
Clock Low Pulse Width	tSCLL[NOTE]	4.7	–	1.3	–	

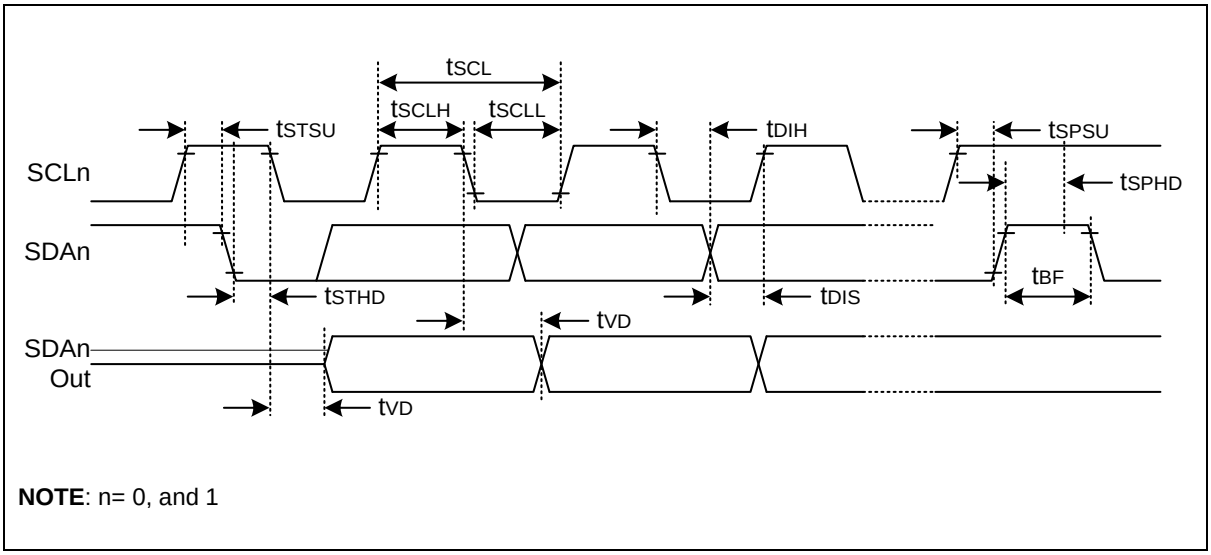
NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

Table 30. I2C0/1 Characteristics (continued)

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Bus Free Time	t_{BF}[NOTE]	4.7	–	1.3	–	us
Start Condition Setup Time	t_{STSU}[NOTE]	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}[NOTE]	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}[NOTE]	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}[NOTE]	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}[NOTE]	0	–	0	–	
Data Input Hold Time	t_{DIH}[NOTE]	0	–	0	1.0	
Data Input Setup Time	t_{DIS}[NOTE]	250	–	100	–	ns

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.



NOTE: n= 0, and 1

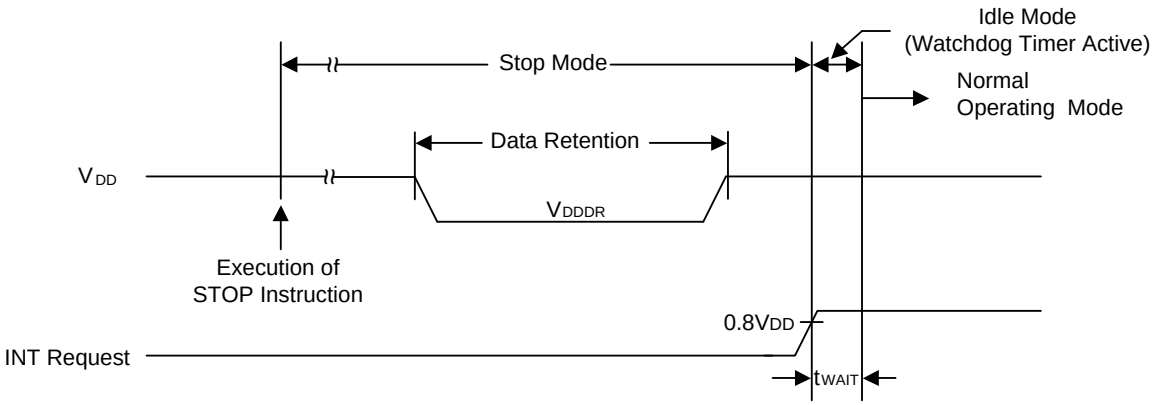
Figure 46. I2C0/1 Timing

20.14 Data retention voltage in stop mode

Table 31. Data Retention Voltage in Stop Mode

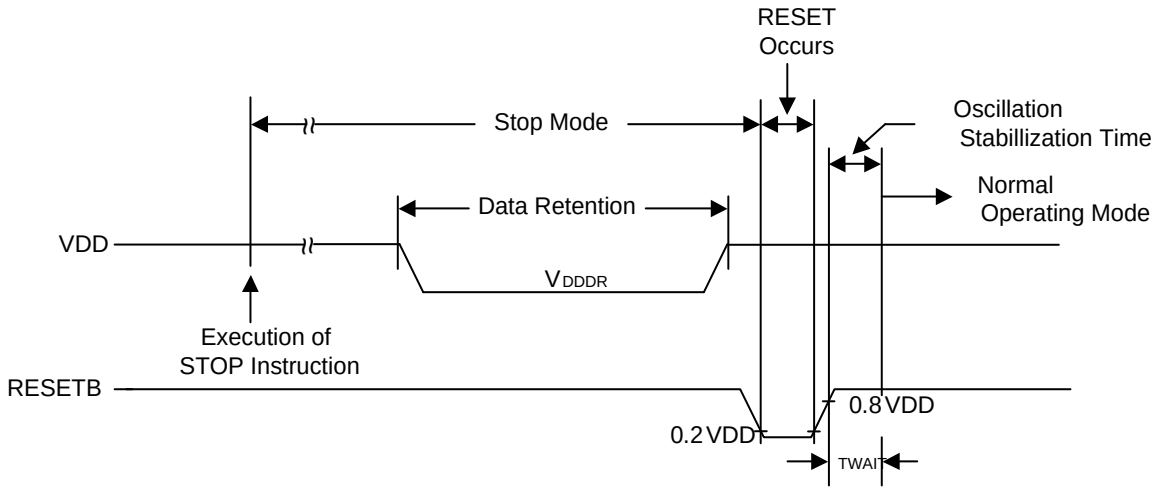
(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 47. Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 48. Stop Mode Release Timing when Initiated by RESETB

20.15 Internal flash ROM characteristics

Table 32. Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM} NOTE1	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE} NOTE1	–	–	–	30,000	times

NOTES:

1. The measured value for the parameters and conditions listed were confirmed by simulation.
2. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

20.16 Main clock oscillator characteristics

Table 33. Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.2V – 5.5V	4	–	10.0	MHz
		2.4V – 5.5V	4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	2.0V – 5.5V	4	–	10.0	MHz
		2.4V – 5.5V	4	–	12.0	
External Clock	XIN input frequency	2.0V – 5.5V	4	–	10.0	MHz
		2.4V – 5.5V	4	–	12.0	

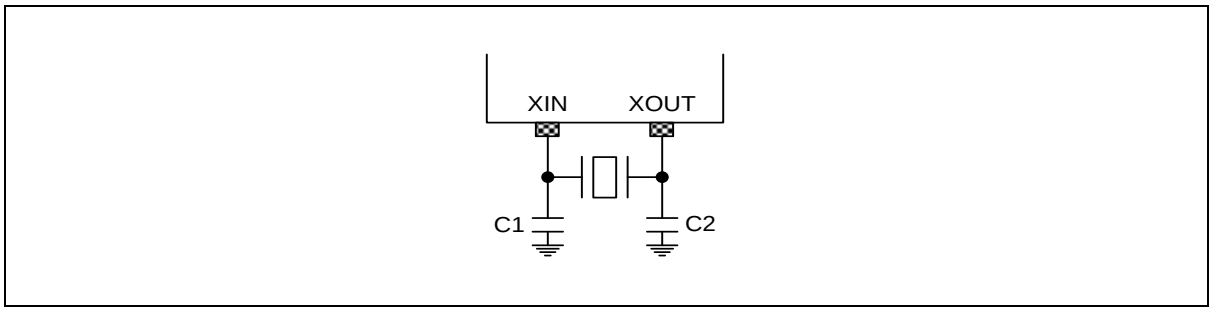


Figure 49. Crystal/Ceramic Oscillator

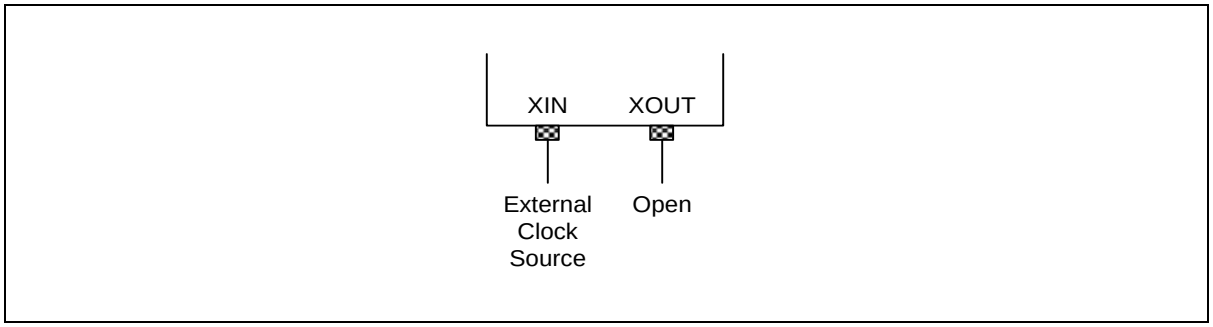


Figure 50. External Clock

20.17 Sub-clock oscillator characteristics

Table 34. Sub Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency NOTE	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency NOTE		32	–	100	kHz

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

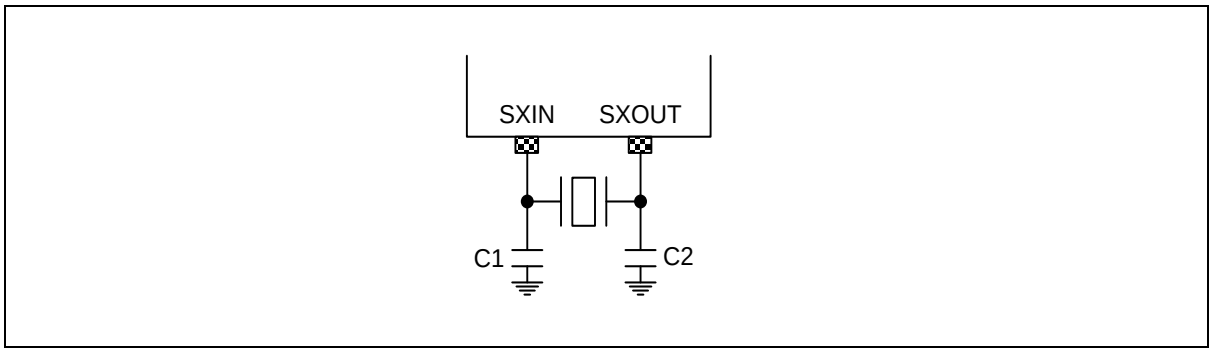


Figure 51. Crystal Oscillator

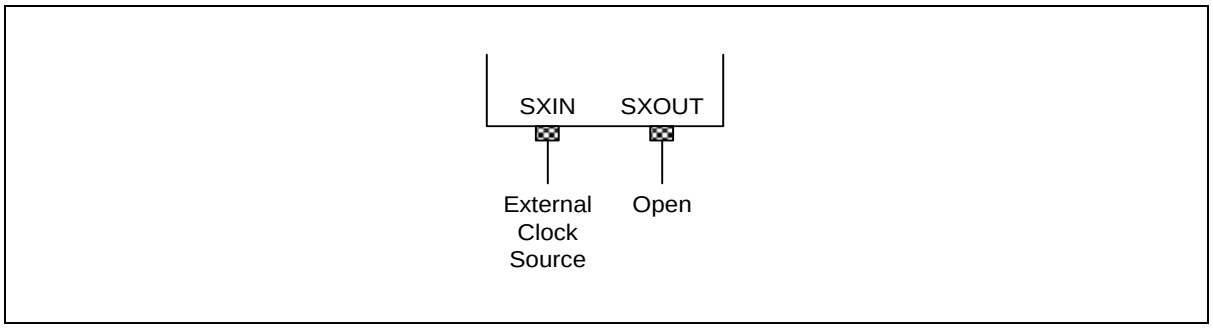


Figure 52. External Clock

20.18 Main oscillation stabilization characteristics

Table 35. Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal NOTE	fx > 4MHz, VDD = 2.7V ~ 5.5V,	–	–	15	ms
	fx > 1MHz, VDD = 1.8V, T_A=-40°C			60	
Ceramic NOTE	-	–	–	10	ms
External Clock	f_{XIN} = 4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

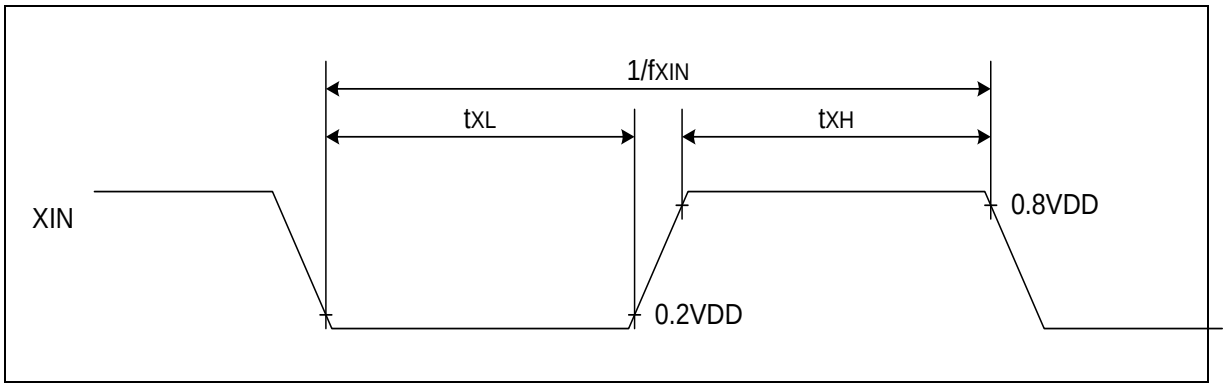


Figure 53. Clock Timing Measurement at XIN

20.19 Sub-oscillation characteristics

Table 36. Sub Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal NOTE	T_A=-40°C ~+85°C	–	–	10	s
	T_A= 25°C		500		ms
External Clock	f_{SXIN}=32 to 100 kHz SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

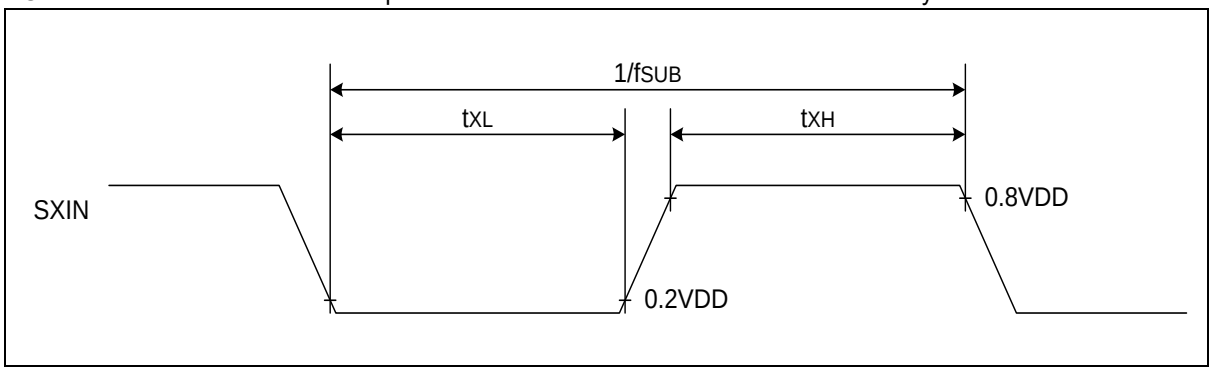


Figure 54. Clock Timing Measurement at SXIN

20.20 Operating voltage range

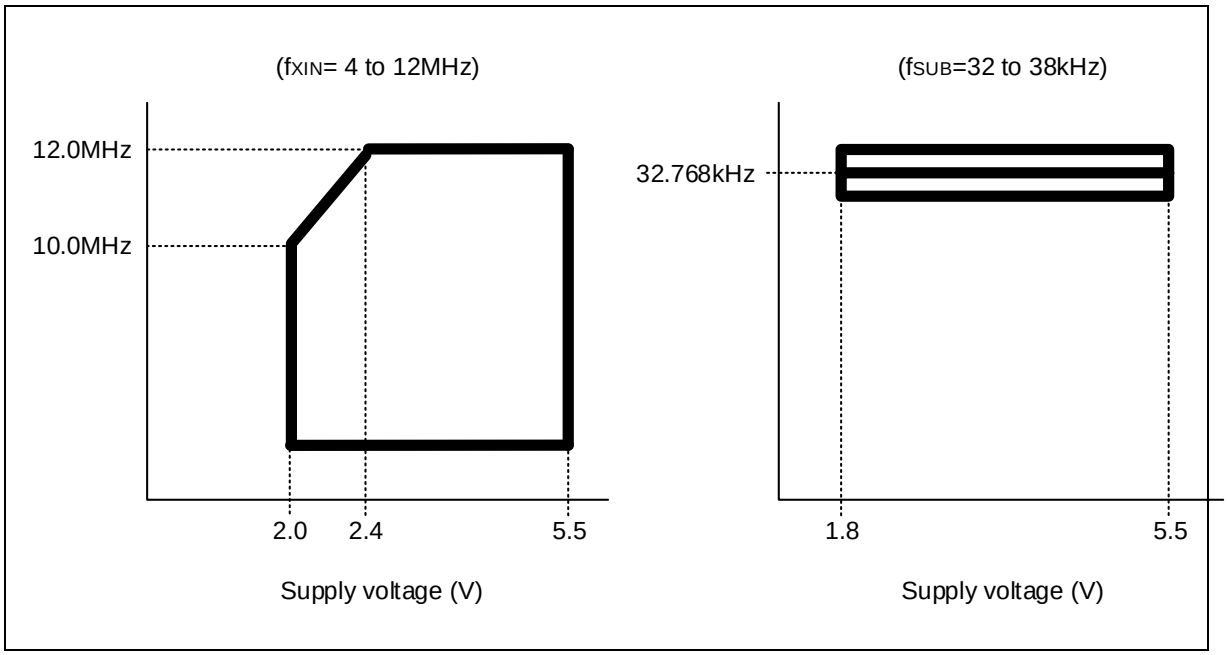


Figure 55. Operating Voltage Range

20.21 Recommended circuit and layout

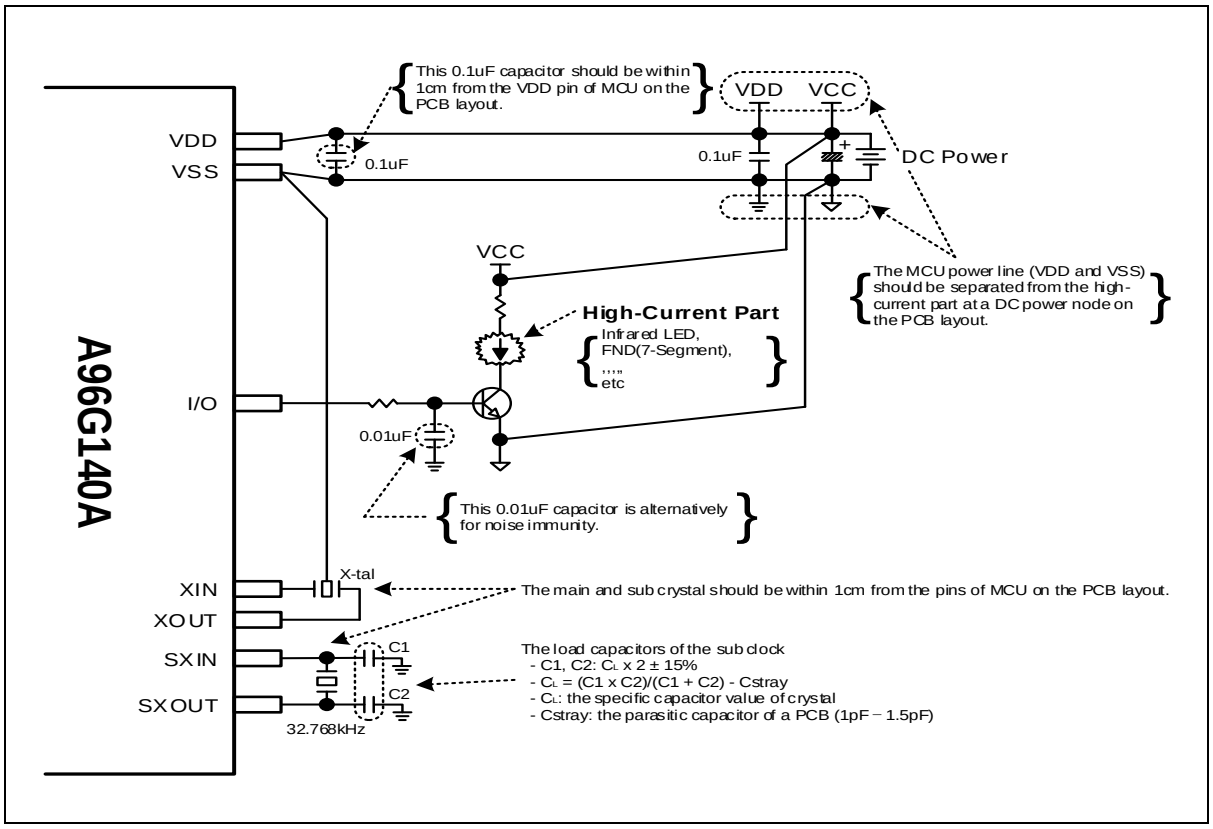


Figure 56. Recommended Voltage Range

Table 37. Reset Pin Component Values

Item	Component	Value
Pull-up/down resistor	R1	10KΩ
Filter capacitor	C1	Typ. 100nF (0.1uF, example)

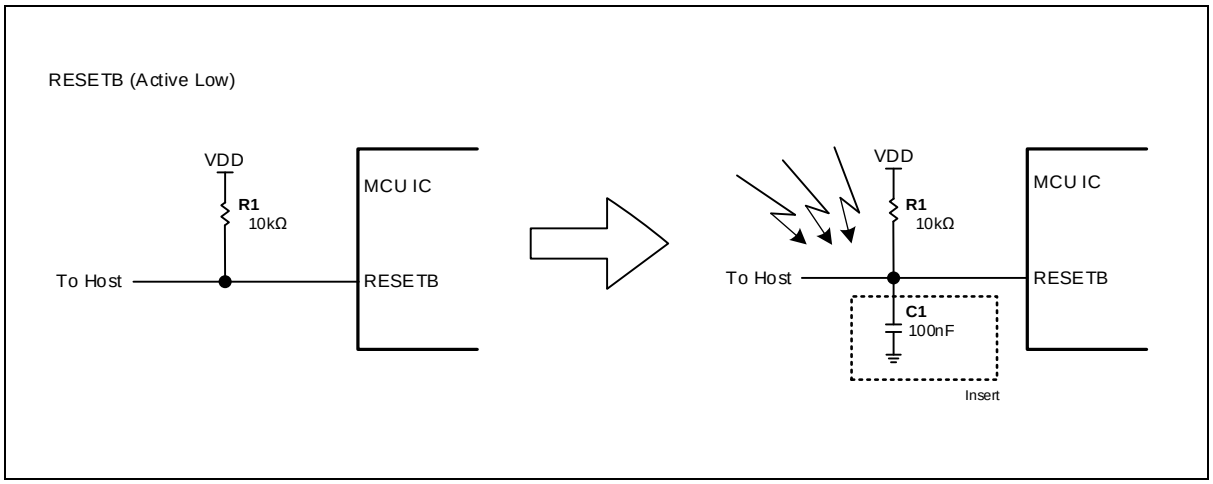


Figure 57. Filters used on a Reset Pin Diagram

20.22 Typical characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

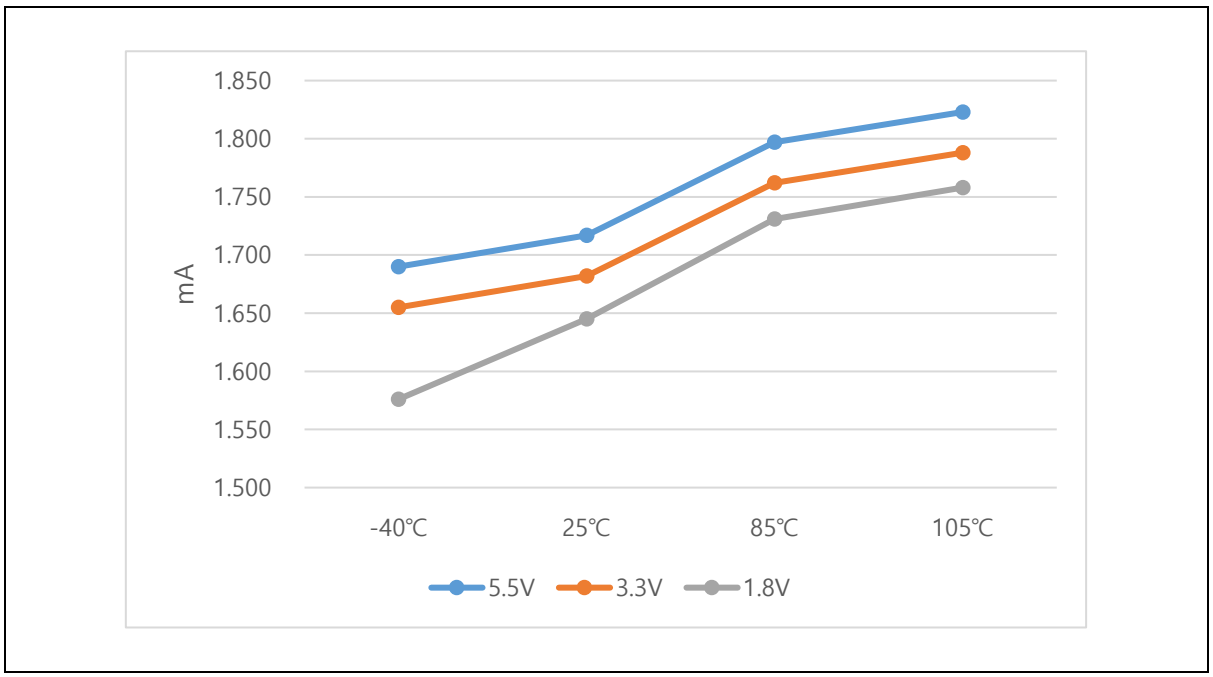


Figure 58. RUN (IDD1) Current

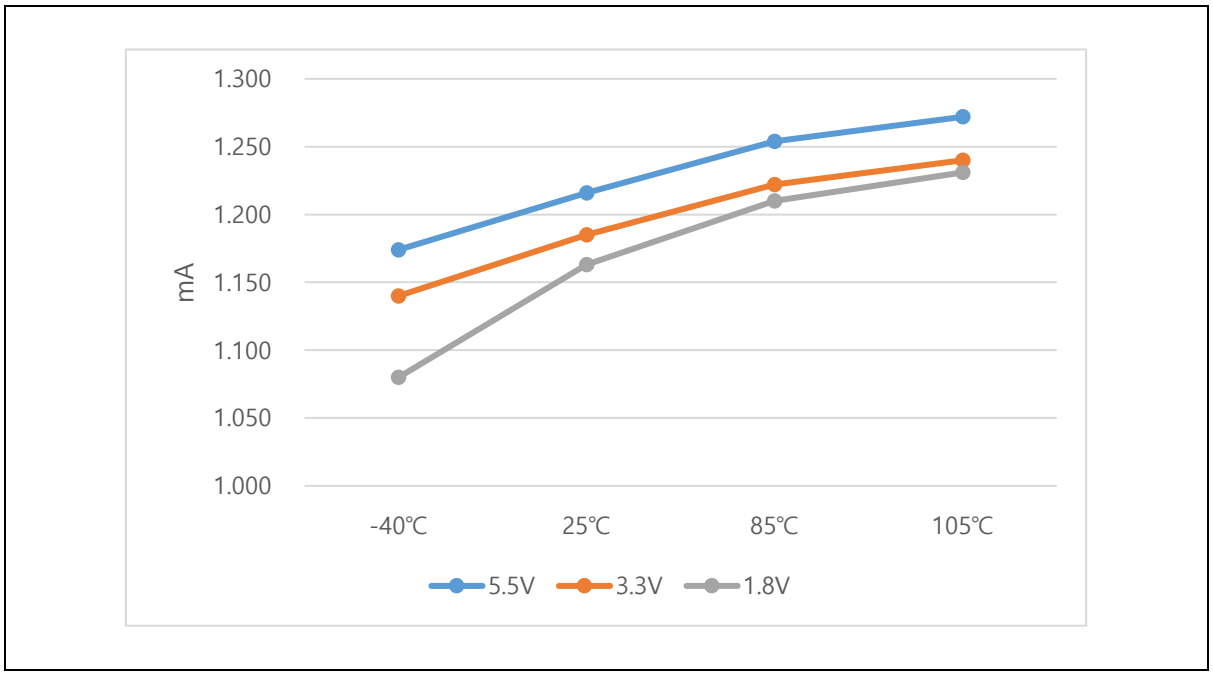


Figure 59. IDLE (IDD2) Current

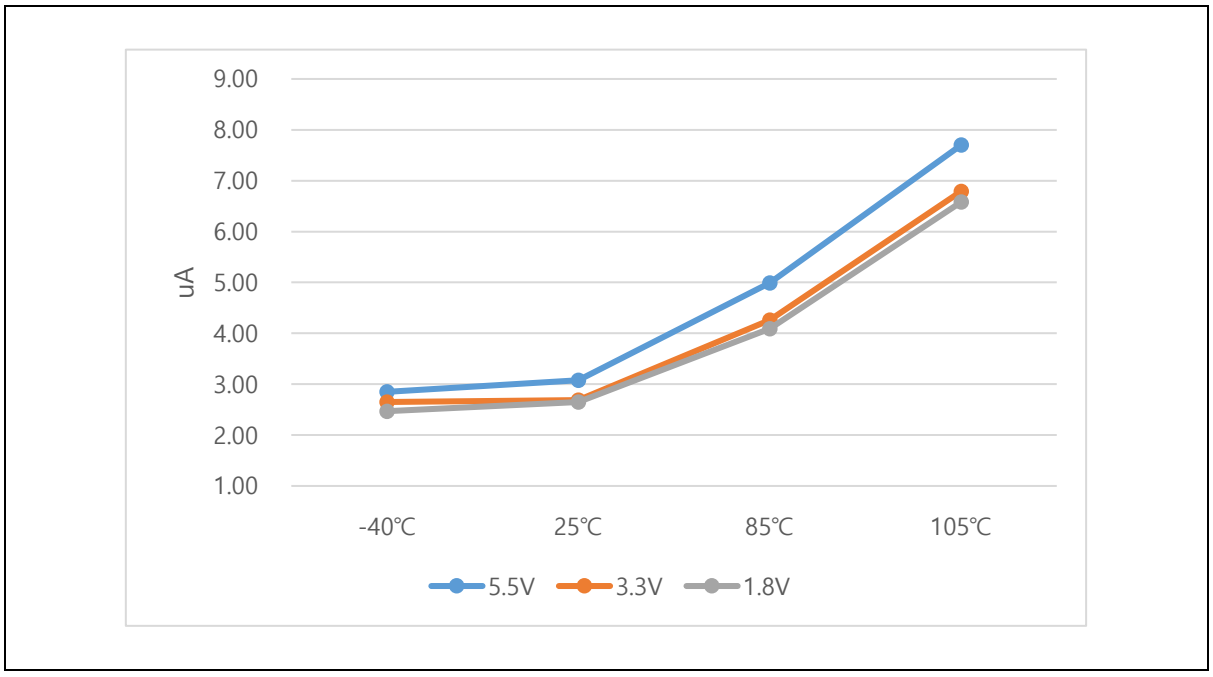


Figure 60. STOP1 (IDD3) Current

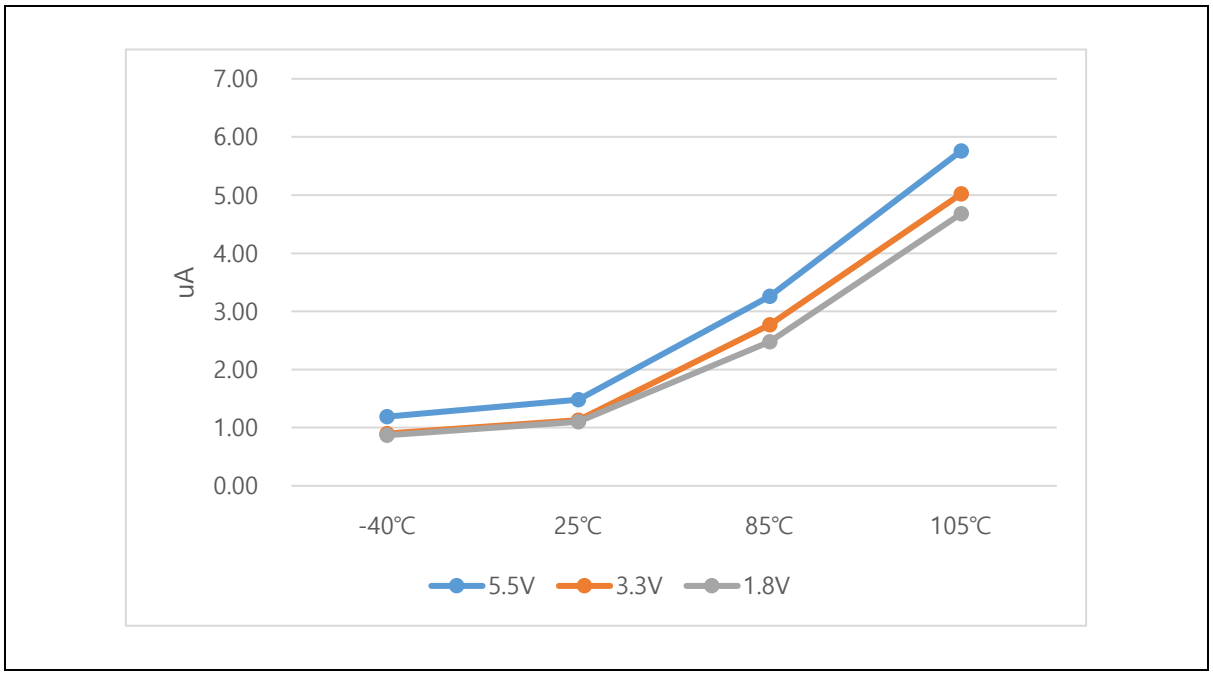


Figure 61. STOP2 (IDD4) Current

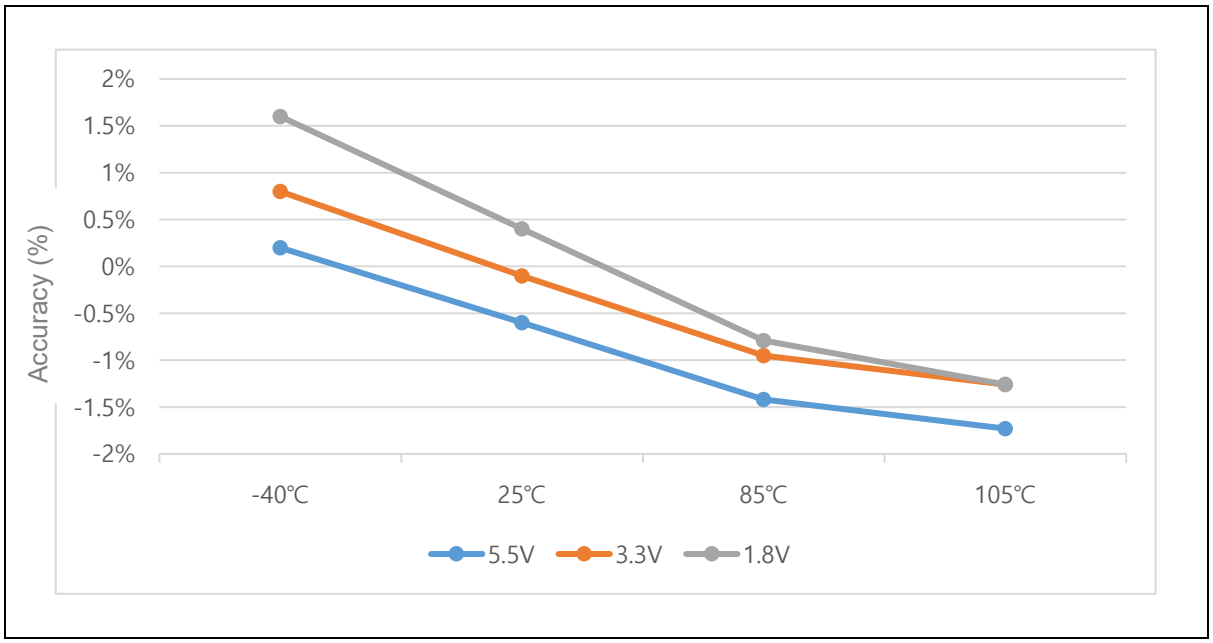


Figure 62. HSI Frequency

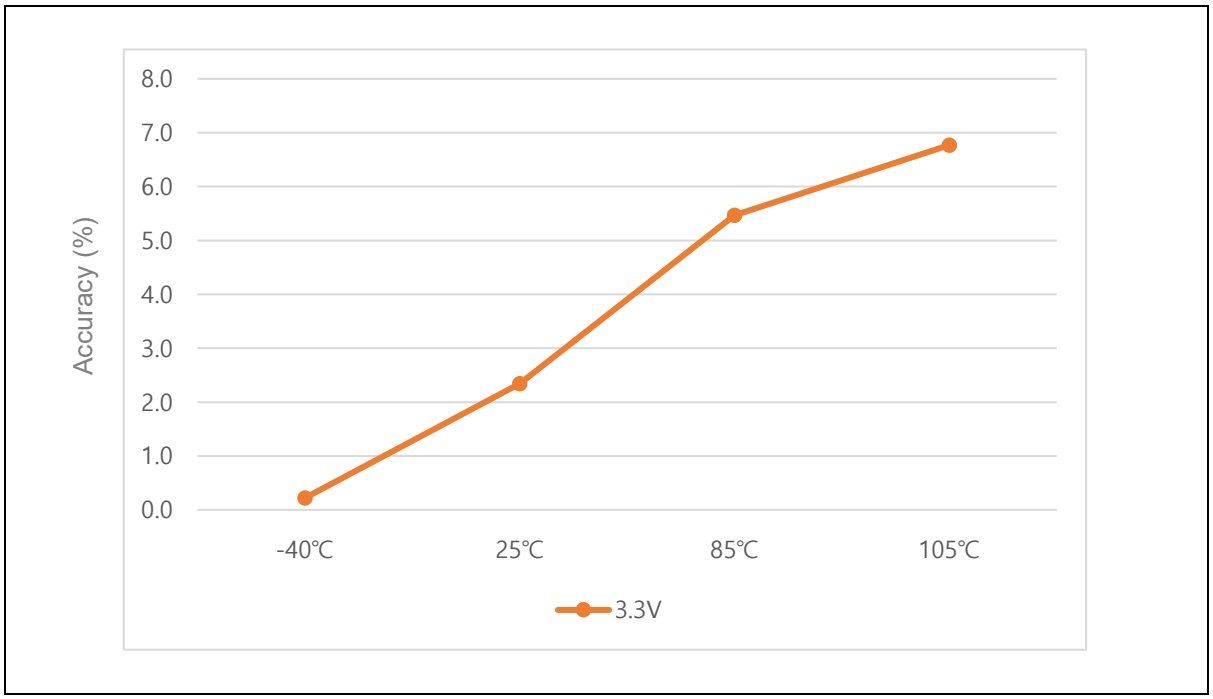


Figure 63. LSI Frequency

21 Development tools

This chapter introduces a wide range of development tools for microcontrollers. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire developer ecosystem of the customers.

21.1 Compiler

ABOV semiconductor does not provide any compiler for the A96G140/A96G148/A96A148. Regarding the compilers, it is recommended to consult with your compiler provider.

Since the A96G140/A96G148/A96A148 has the Mentor 8051 as a core, and ROM is smaller than 64Kbytes in size, a developer can use any standard 8051 compiler from other providers.

21.2 Core and debug tool information

ABOV's microcontroller uses OCD (On-Chip Debugger) interface for debugging, which is ABOV's own interface. The OCD not only monitors and controls the core, but also supports the read and write operations of external memory and devices. In addition, it supports memory monitoring and break functions.

Debug interfaces such as OCD interfaces enable microcontrollers to write to internal programmable memory, allowing them to support ISP (In-System Program) that makes possible to write as a single chip or as an embedded chip in the system. Table 38 provides information of the core and debug emulation interface.

Table 38. Information of Core and Debug Emulation Interfaces

	Description	Remark
Device Name	A9xXxxx	
Series	94/ 95/ 96/ 97 series	
Core	M8051/ CM8051	
Extended Stack Pointer	Yes/ no	94, 97 series only
Debug Interface	OCD 1/ OCD 2	
Number of Break Point	4/ 8	
Real-time Monitoring	Yes/ no	OCD 2 only
Run Flag Port	Yes/ no	OCD 2 option

NOTES:

1. The A96G140/A96G148/A96A148 has the 96 series core and OCD 1 interface.
2. The A96G140/A96G148/A96A148 can be operated with OCD II dongle too, because the OCD II dongle includes all of OCD1 functions.
3. The 95 series core is the old version of the 96 series core.

21.2.1 Feature of 94/96/97 series core

ABOV's 8-bit microcontroller contains the M8051/CM8051 core that is an improved version of the 8051. The M8051/CM8051 core is compatible with the 8051, and reduces time of operation cycles. It makes development easier by providing the OCD debug function.

ABOV's 8-bit microcontroller has a core of the 94-series, 96-series, or 97-series that is basically compatible with the 8051 series at the instruction set level. The cores in each series use different Debug Interfaces, as shown in Table 39.

Table 39. Cores and Debug Interfaces by Series

	Core	Debug Interface
96 Series	M8051	OCD 1
97 Series	M8051	OCD 2
94 Series	CM8051	OCD 2

Features of each series are compared in Table 40.

Table 40. Feature Comparison Chart By Series and Core

	96 Series	97 Series	94 Series
CPU Core	M8051	M8051	CM8051
Cycle Compatible with MCS51	1/6	1/6	No
OCD Function	OCD 1	OCD 2	OCD 2
Program BUS	8-bit		
Data Bus	8-bit IRAM/ XRAM separated		8-bit single SRAM
EA Auto Clear NOTE1	Yes	Yes	Yes
EA=0, Idle/ Stope Mode Wake up	Yes	Yes	Yes
Interrupt Priority NOTE2	6 group x 4 level	Interrupt x 4 level	Interrupt x 2 level
Nested Interrupt Priority	4 level	4 level	Interrupt x 2 level (max. 4 times)
SFR BUS (read/ write)	Two ports	Two ports	Single port
Stack Extension	X	O	O
Register	SRAM		
Register Bank	4		
CPU/ Flash Clock Ratio	x 1		
Pipeline	No	No	2-stage (IF + ID/ EX)
DHRY Stone Score (I8051: 1.00)	6.0	6.0	8.4
Average Instruction Set Exe. Cycle Compare with i8051	x 6.0	x 6.0	x 6.4
Power Consumption/ DHRY (@synthesis)	52.27uA/ MHz	52.27uA/ MHz	30.19 uA/ MHz

NOTES:

1. EA means that All Interrupt Enable bit or Disable bit (Standard 8051).
2. Group: When a programmer selects a specific interrupt (e.g. Interrupt1),
   Whole interrupts: 0, 6, 12, and 18 have higher priorities.
3. The A96G140/A96G148/A96A148 has the 96 series core and OCD 1 interface.
4. The A96G140/A96G148/A96A148 can be operated with the OCD II dongle too, because the OCD II dongle includes all functions of the OCD1.

ABOV's 8-bit microcontroller maintains binary compatibility with 8051 cores; however, the cores and series have differences in performances, core functionalities, and debug interfaces.

You can see the differences between each series in the following sections.

21.2.2 OCD type of 94/96/97 series core

Cores of the 96-series use the OCD 1 for debug interfaces, while cores of the 94-series and 97-series use the OCD 2 for debug interfaces. The OCD 1 and OCD 2 use the same method on the Hardware, however, the protocols are incompatible with each other.

In the OCD 2, it is able to measure the emulation time through the "Run Flag" pin.

Table 41. OCD Type of Each Series

	96-Series	97-Series	94-Series	Remark
OCD type	OCD 1	OCD 2	OCD 2	

In Table 42, debug interfaces of the OCD 1 and OCD 2 are compared.

Table 42. Comparison of OCD 1 and OCD 2

	Value	Description
OCD 1	Break point MAX.8	PC break only
OCD 2	Break point MAX.12	With RAM break — Code, XDATA, IDATA — 1/8/16/32bit compare
	Real-time monitoring	Code, XDATA, IDATA
	Frequency output	Examine CPU frequency
	Run Flag port	Option for run time measurement

96 Series – OCD 1

The 96 series supports basic operation of debug interfaces such as Run, Stop, Step, Break point, register reading/writing, Memory reading/writing, and SFR reading/writing.

94 Series and 97 Series – OCD 2

The 94 series and 97 series support the features listed below, as well as the features of the OCD 1 (however, their protocol is incompatible with the OCD1):

- RTM support: CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- Run Flag support: Emulation Time can be measured in OCD mode (using the Run Flag port).
- RAM Break support: IDATA, SFR, and XDATA break are added.

21.2.3 Interrupt priority of 94/96/97 series core

In the M8051, users can set interrupt priorities by group. The 96-series microcontroller with the basic M8051 core only supports interrupt priorities in group units. In the 94-series or 97-series microcontroller, users set interrupt priorities to have more functionalities than existing features, and can set individual priority for each interrupt source.

Table 43. Interrupt Priorities in Groups and Levels

Series	96-Series	97-Series	94-Series	Remark
Interrupt Priority	6 Grouped 4 Level	Fully 4 Level	Fully 4 Level	**96 Series:** IP/IP (Interrupt Priority Register) **94, 97 Series:** IPxL/IPxH (Interrupt Priority Register)

96 Series

- The priority by group is available only with IP/IP1 settings.
  - With the IP/IP1 settings, users can set the interrupt priorities in group units.
  - The interrupt priority in group units (4 interrupts in a group) can be changed to the level between 0 and 3 according to the value of the IP/IP1.

94, 97 Series

- The individual interrupt priority can be set by setting IPxL/IPxH (x = 0 to x = 3).
- The individual interrupt priority can be changed to the level between 0 and 3 according to value of the IPxL/IPxH (x = 0 to x = 3).

21.2.4 Extended stack pointer of 94/96/97 series core

The M8051 uses IRAM area for Stack Pointer. However, 94-series and 97-series microcontrollers use both IRAM area and XRAM area for the Stack Pointer by configuring additional registers.

The XSP and XSPCR registers are involved in this functionality as described below:

- By configuring the XSP/XSPCR register, you can use the XRAM area for the Stack Pointer.
  - The XSPCR decides whether to use XRAM for the Stack Pointer.
    - If XSPCR = ’0’, the IRAM is available for the Stack Pointer.
    - If XSPCR = ’1’, the XRAM is available for the Stack Pointer.
  - The XSP decides a position of XRAM Stack Pointer.
    - This is valid only if XSPCR = ’1’.

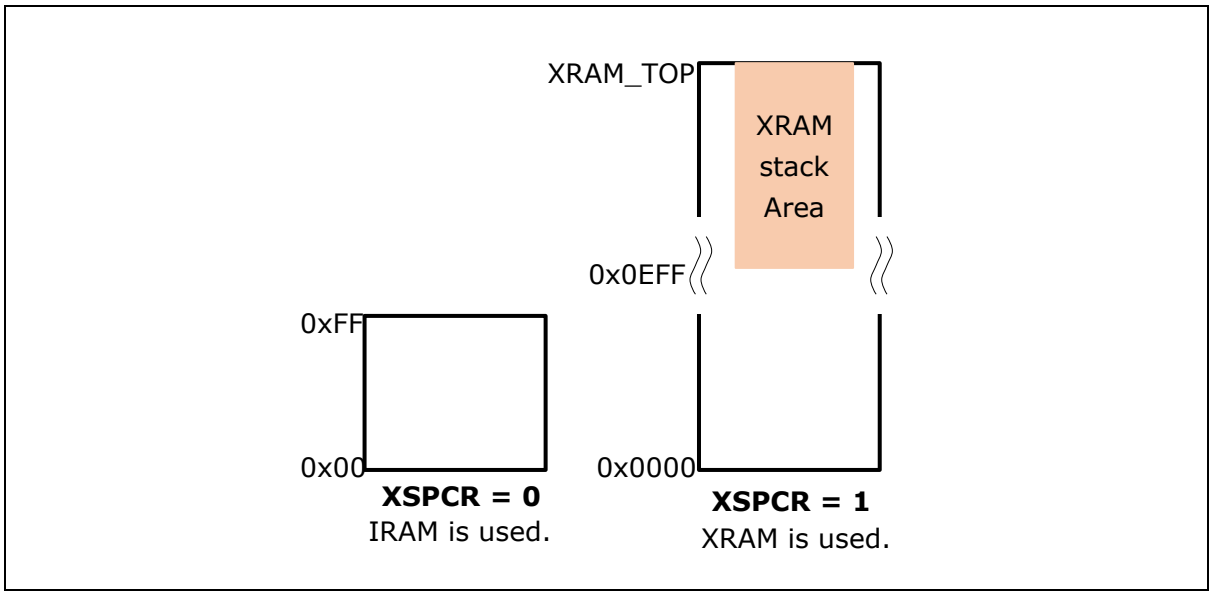


Figure 64. Configuration of Extended Stack Pointer

STACK_POINTER = {XSP[7:0],SP[7:0]} = XRAM_TOP – STACK_SIZE

Ex) If only 256bytes of XRAM is used for stack,

- XRAM_TOP = 4K(0x0FFF)
- STACK_SIZE = 256byte(0x0100)
- XSPCR = 1, XSP = 0x0E
- SP = 0xFF setting
- Stack Pointer Position = 0x0FFF - 0x0100 = 0x0EFF

21.3 OCD (On-chip debugger) emulator and debugger

Microcontrollers with 8051 cores have an OCD (On-Chip Debugger), a debug emulation block. The OCD is connected to a target microcontroller using two lines such as DSCL and DSDA. The DSCL is used for clock signal and the DSDA is used for bi-directional data.

The two lines work for the core management and control by doing register management and execution, step execution, break point and watch functions. In addition, they control and monitor the internal memory and the device by reading and writing.

Table 44. Debug Feature by Series

Series name	96-series	97-series	94-series
OCD function	OCD 1	OCD 2	OCD 2
Max. number of breakpoints	8	8	4
Saving stack in XRAM	No	Yes	Yes
Real time monitoring	No	Yes	Yes
Run flag support	No	Yes	Yes

The OCD 2 applied to the 94-series and 97-series provides the RTM (Real Time Monitoring) function that monitors internal memory and I/O status without stopping the debugging. In addition, the OCD 2 provides the breakpoint function (RAM Break Function) for the IDATA, SFR, and XDATA.

The following functions have been extended from the OCD 2:

- Emulation Time can be measured in OCD mode (using the Run Flag port).
- CODE, XDATA, and IDATA are updated during the Run Time (Real Time Monitoring available).
- IDATA, SFR, and XDATA break are added (RAM Break support).

Figure 65 shows the standard 10-pin connector of the OCD 1 and OCD 2.

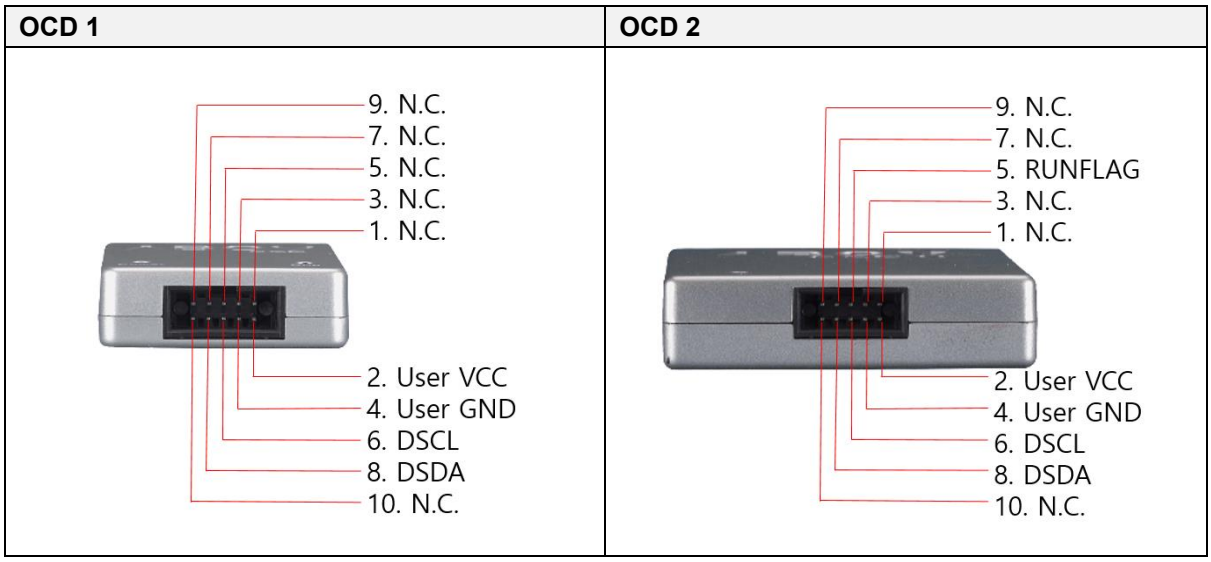


Figure 65. OCD 1 and OCD 2 Connector Pin Diagram

Table 45 describes the pins assigned to the OCD 1 and OCD 2.

Table 45. OCD 1 and OCD 2 Pin Description

Pin name	Microcontroller function in Debug Mode	
	I/O	Description
DSCL	I	Serial clock pin. Input only pin.
DSDA	I/O	• Serial data pin. • Output port when reading and input port when programming. • It can be assigned as input/push-pull output port.
VDD,VSS	—	Logic power supply pin.

The OCD emulator supports ABOV's 8051 series MCU emulation. The OCD uses two wires that are interfaces between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means that the OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista (32-bit). If you want to see more details, please visit ABOV's website (www.abovsemi.com), and download debugger S/W and OCD debugger manuals.

- Connection:
  - DSCL (A96G140/A96G148/A96A148 P01 port)
  - DSDA (A96G140/A96G148/A96A148 P00 port)

Figure 66 shows pinouts of OCD connector.

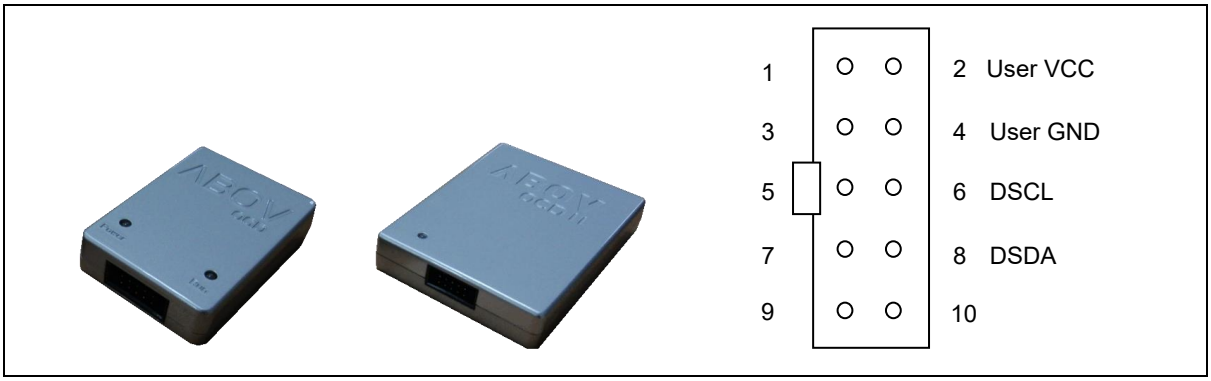


Figure 66. Debugger (OCD1/OCD2) and Pinouts

21.3.1 On-chip debug system

The A96G140/A96G148/A96A148 supports On-chip Debug (OCD) system. We recommend developing and debugging program with A96G1xx series. The OCD system of the A96G140/A96G148/A96A148 can be used for programming the non-volatile memories and on-chip debugging.

In this section, you can find detailed descriptions for programming via the OCD interface. Table 46 introduces features of the OCD.

Table 46. OCD Features

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

Figure 67 shows a block diagram of the OCD interface and On-chip Debug system.

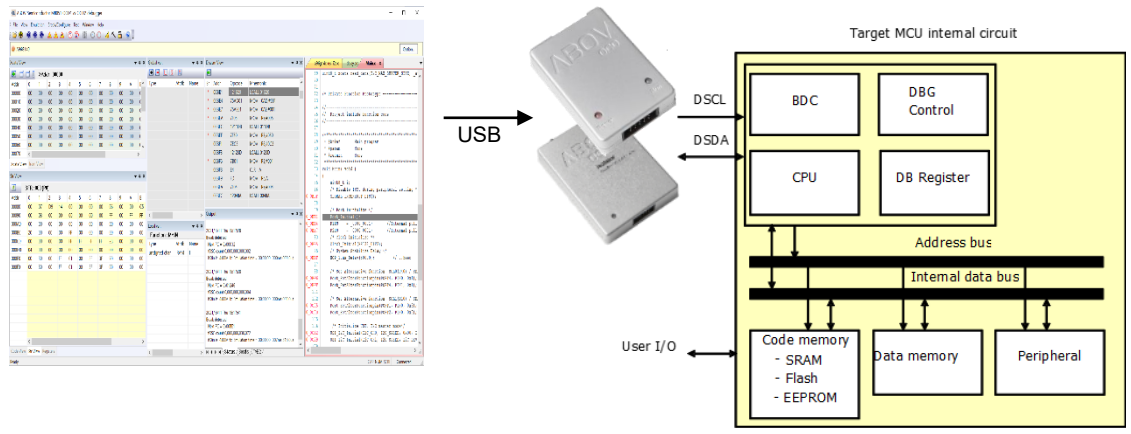


Figure 67. On-Chip Debugging System Block Diagram

Entering debug mode

While communicating through the OCD, you can enter the microcontroller into DEBUG mode by applying power to it. This means that the microcontroller enters DEBUG mode when you place specific signals to the DSCL and DSDA at the moment of initialization when the microcontroller is powered on. This requires that you can control power of the microcontroller (VCC or VDD) and need to be careful to place capacitive loads such as large capacity condensers on a power pin.

Please remember that the microcontroller can enter DEBUG mode only when power is applied, and it cannot enter DEBUG mode once the OCD is run.

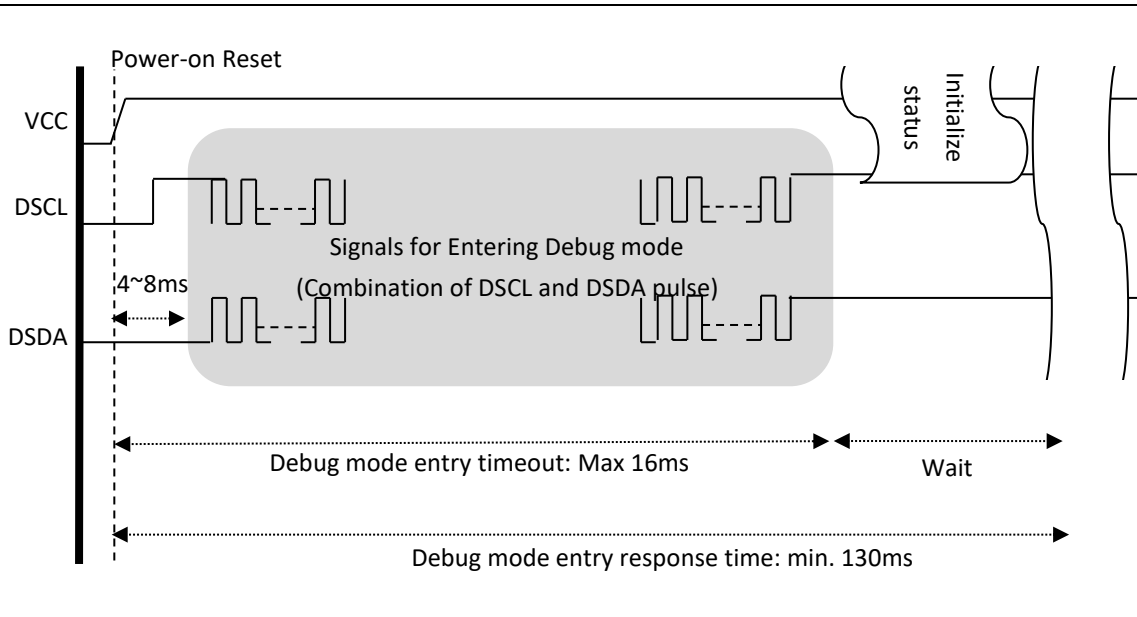


Figure 68. Timing Diagram of Debug Mode Entry

21.3.2 Two-wire communication protocol

For the OCD interface, the semi-duplex communication protocol is used through separate two wires, the DSCL and DSDA. The DSCL is used for serial clock signal and the DSDA is used for bi-directional serial address and data.

A unit packet of transmission data is 10-bit long and consists of a byte of data, 1-bit of parity, and 1-bit of acknowledge. A parity check bit and a receive acknowledge bit are transmitted to guarantee stability of the data communication. A communication packet includes a start bit and an end bit to indicate the start and end of the communication.

More detailed information of this communication protocol is listed below:

Basic transmission packet

- A 10-bit packet transmission using two-pin interface.
- A packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits a command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start and stop conditions notify start and stop of the background debugger command respectively.

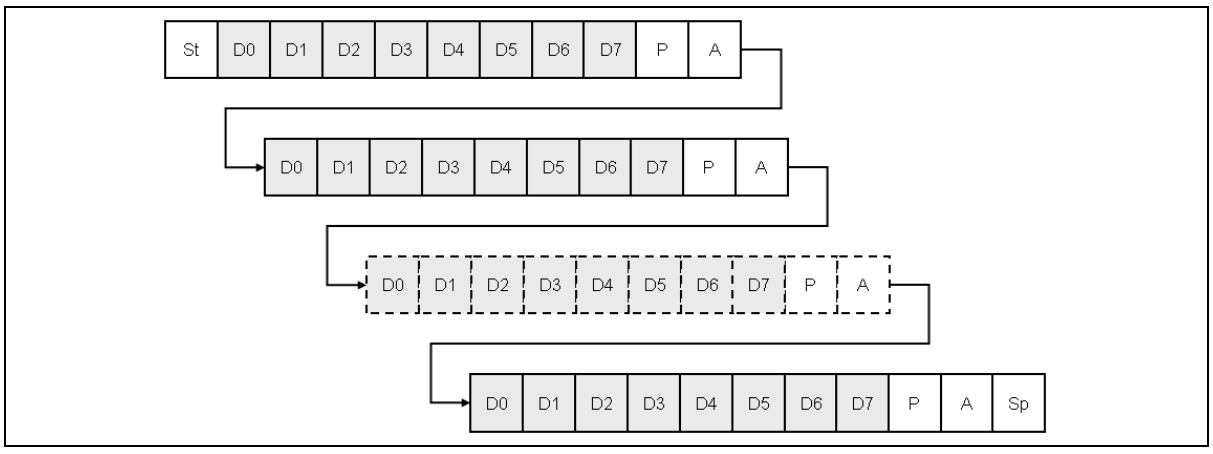


Figure 69. 10-bit Transmission Packet

Packet transmission timing

Figure 70 shows a timing diagram of a packet transmission using the OCD communication protocol.

A start bit in the figure means start of a packet and is valid when the DSDA falls from ‘H’ to ‘L’ while External Host maintains the DSCL to ‘H’. After the valid start bit, communication data is transferred and received between a Host and a microcontroller.

An end bit means end of the data transmission and is valid when the DSDA changes from ‘L’ to ‘H’ while a Debugger maintains the DSCL to ‘H’. Next, the microcontroller places the bus in a wait state and processes the received data.

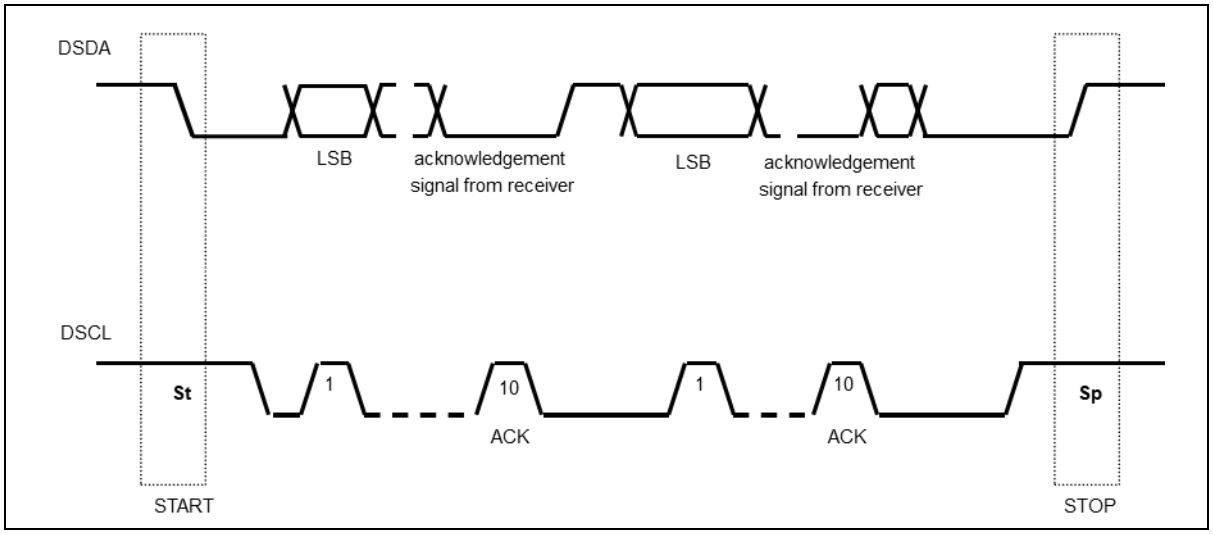


Figure 70. Data Transfer on OCD

Figure 71 shows a timing diagram of each bit based on state of the DSCL clock and the DSDA data. Similar to I2C signal, the DSDA data is allowed to change when the DSCL is ‘L’. If the data changes when the DSCL is ‘H’, the change means ‘START’ or ‘STOP’.

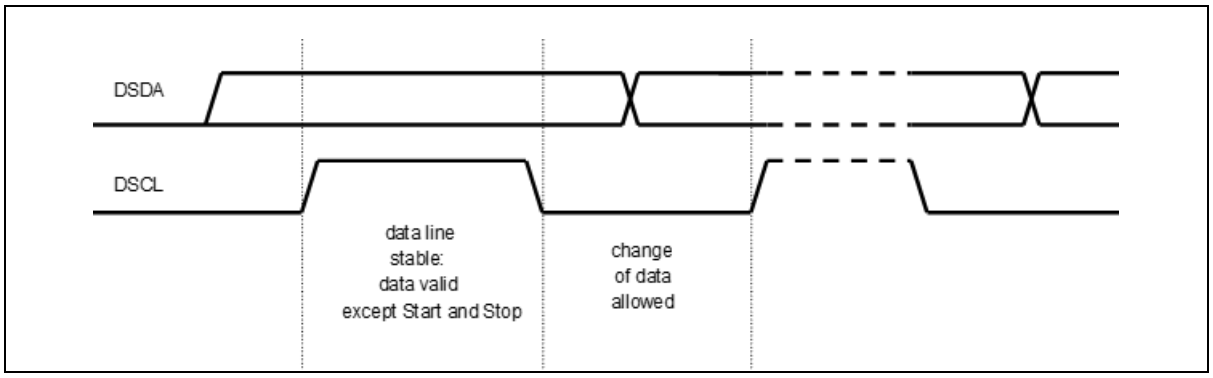


Figure 71. Bit Transfer on Serial Bus

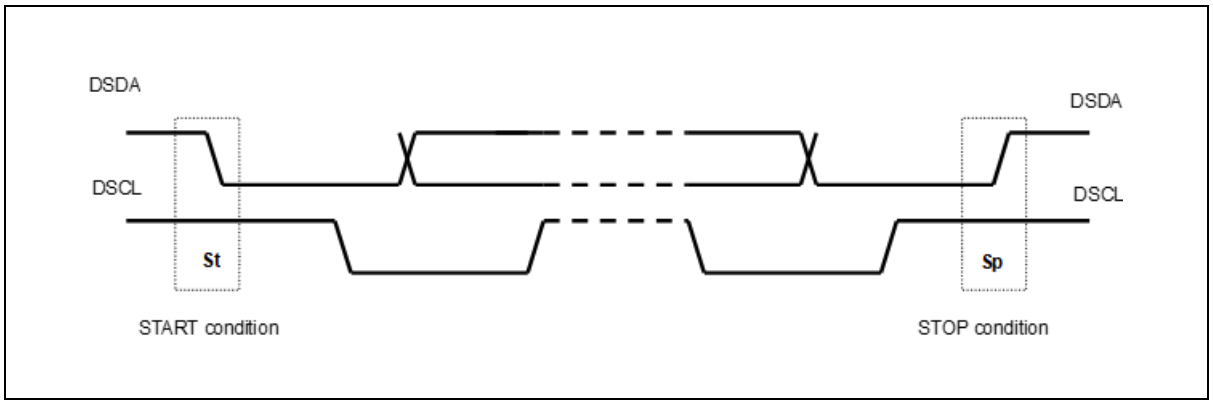


Figure 72. Start and Stop Conditions

During the OCD communication, each data byte is transferred in accompany with a parity bit. When data is transferred in succession, a receiver returns the acknowledge bit to inform that it received.

As shown in Figure 73, when transferring data, a receiver outputs the DSDA to ‘L’ to inform the normal reception of data. If a receiver outputs DSDA to ‘H’, it means error reception of data.

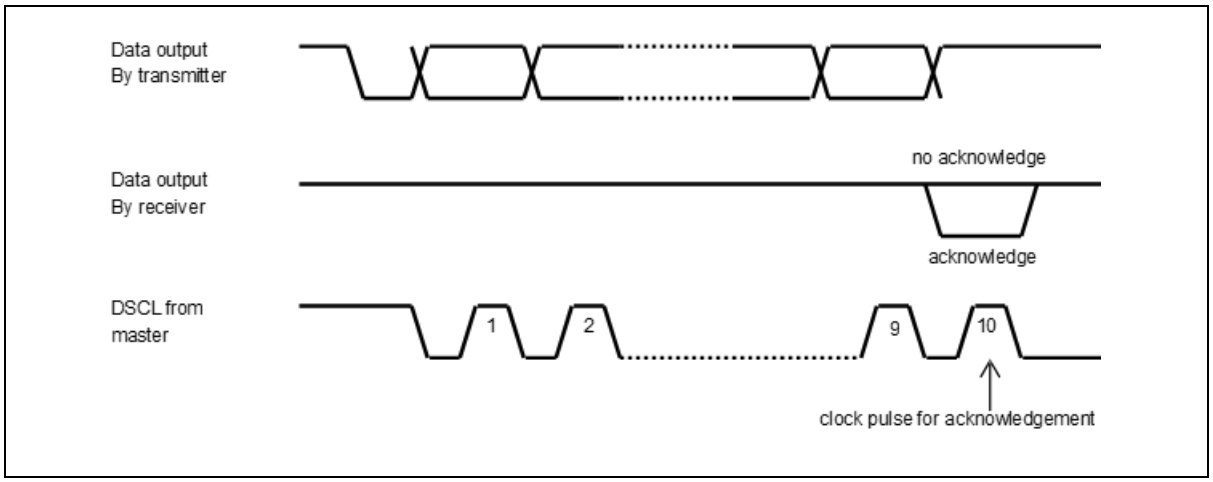


Figure 73. Acknowledge on Serial Bus

While the Host Debugger executes data communications, if a microcontroller needs communication delay or process delay, it can request communication delay to the Host Debugger.

Figure 74 shows timing diagrams where a microcontroller requests communication delay to the Host Debugger. If the microcontroller requests timing delay of the DSCL signal that the Host Debugger outputs, the microcontroller maintains the DSCL signal to ‘L’ to delay the clock change although the Host Debugger changes the DSCL to ‘H’.

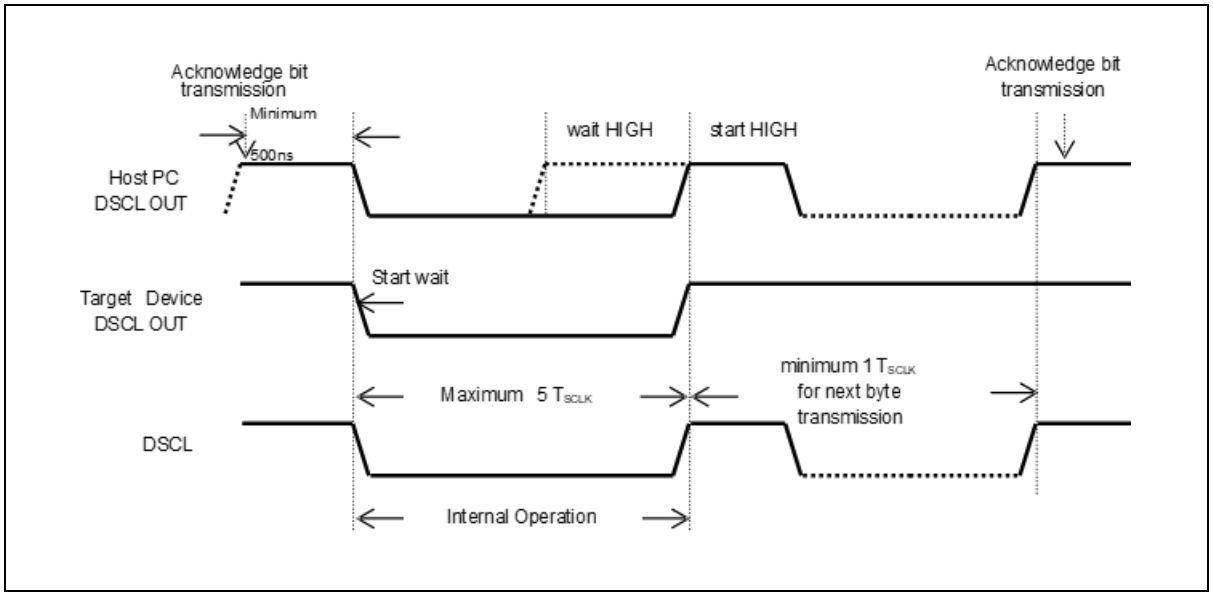


Figure 74. Clock Synchronization during Wait Procedure

21.4 Programmers

21.4.1 E-PGM+

E-PGM+ USB is a single programmer. You can program A96G140/A96G148/A96A148 directly using the E-PGM+.

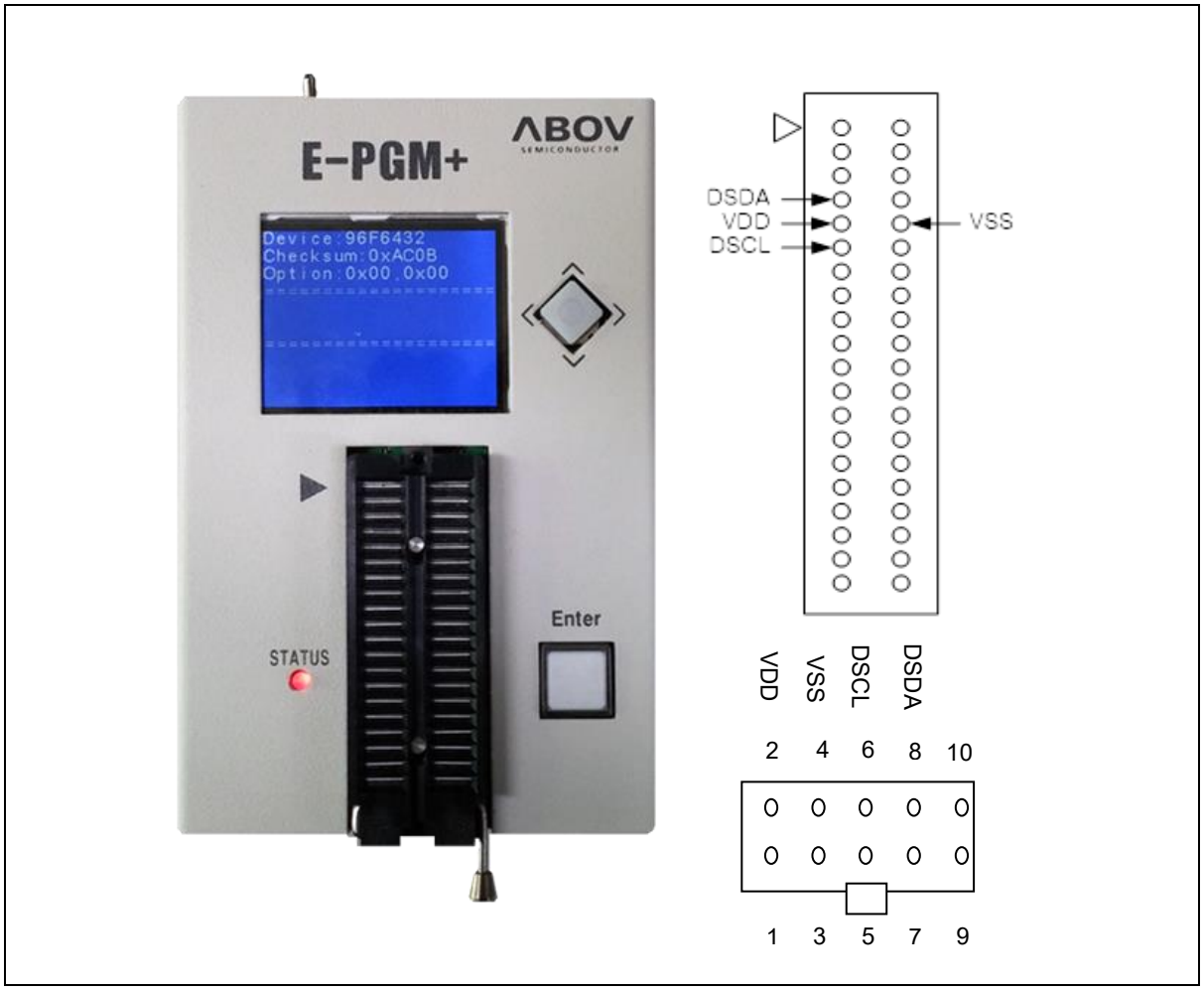


Figure 75. E-PGM+ (Single Writer) and Pinouts

21.4.2 OCD emulator

OCD emulator allows users to write code on the device too, since OCD debugger supports In System Programming (ISP). It doesn't require additional H/W, except developer's target system.

21.4.3 Gang programmer

E-Gang4 and E-Gang6 allow users to program multiple devices simultaneously. They can be run not only in PC controlled mode but also in standalone mode without the PC control.

USB interface is available, and it is easy to connect to the handler.

Figure 76. E-Gang4 and E-Gang6 (for Mass Production)

21.5 Flash programming

Program memory for A96G140/A96G148/A96A148 is Flash type. This Flash ROM is accessed through four pins such as DSCL, DSDA, VDD and VSS in serial data format. For detailed information about the Flash memory programming, please refer to **0.**

Memory programming.

Table 47 introduces corresponding pins and I/O status.

Table 47. Pins for Flash Programming

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

21.5.1 On-board programming

Microcontrollers need only four signal lines including VDD and VSS pins, to program the Flash ROM using serial protocol. Therefore, on-board programming is possible if the programming signal lines are considered at the time the PCB of application board is designed.

21.6 Connection of transmission

OCD's two-wire communication interfaces use the Open-Drain Method (Wire-AND Bi-Directional I/O).

Normally, it is recommended to place a resister greater than 4.7kΩ for the DSCL and DSDA respectively. The capacitive load is recommended to be less than 100pF. Outside these ranges, because the communication may not be accomplished, the connection to Debug mode is not guaranteed.

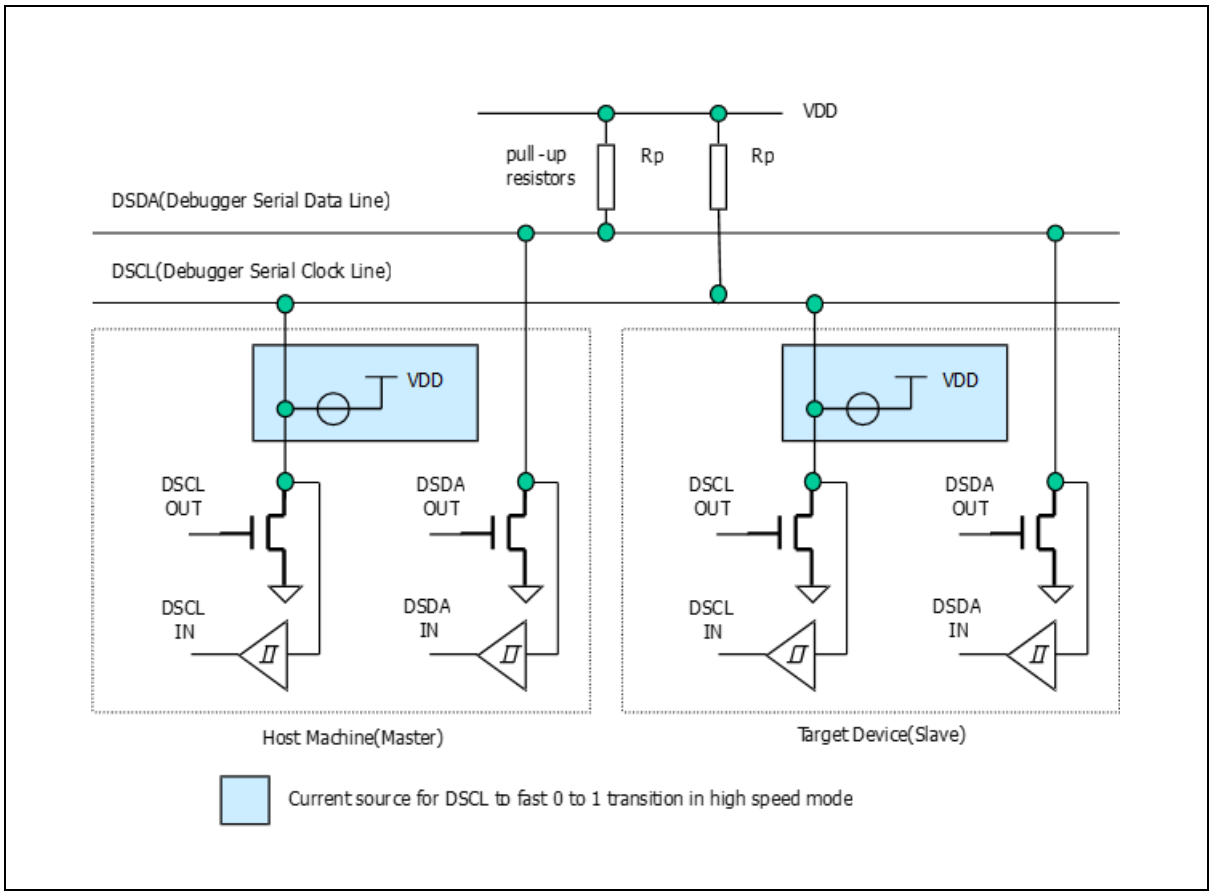


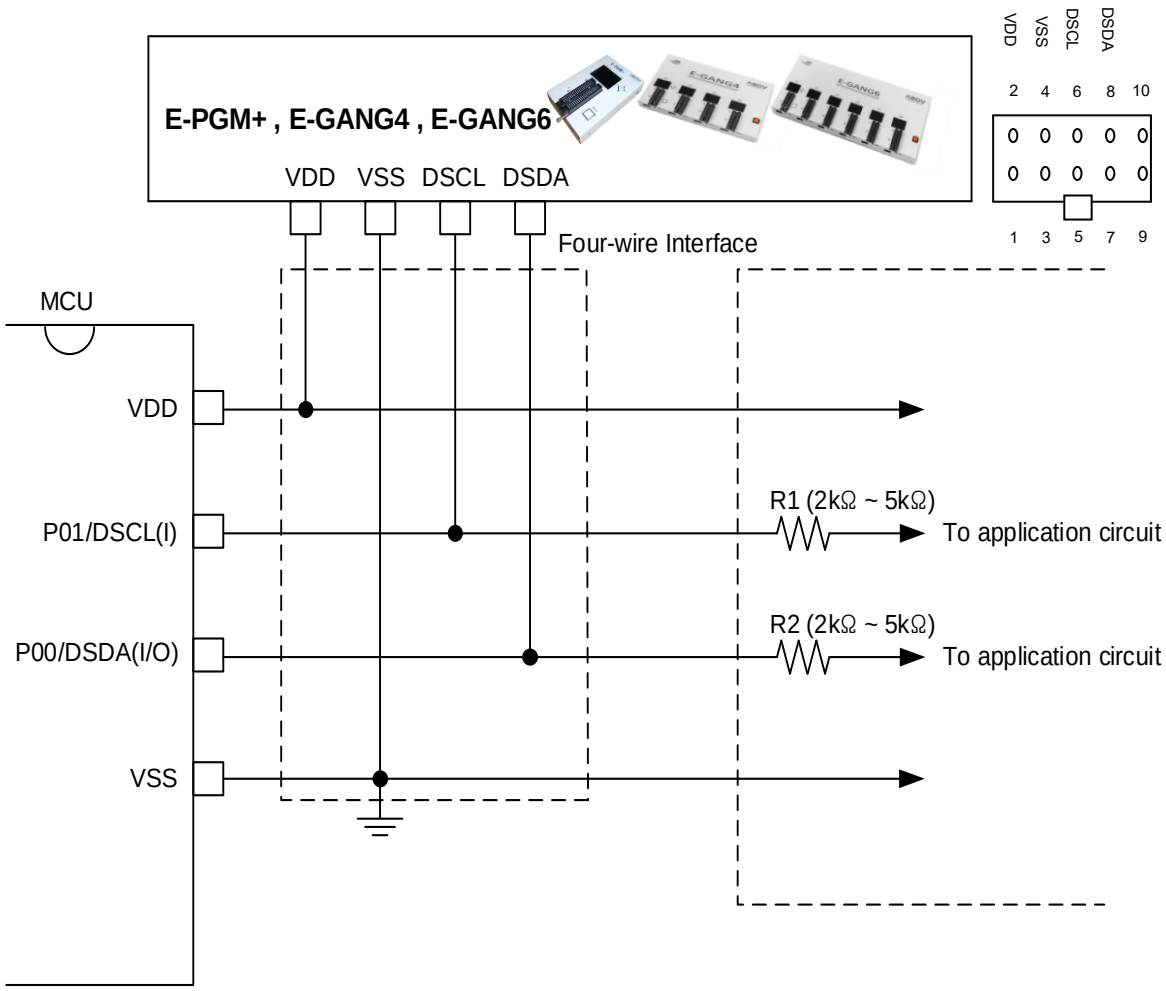
Figure 77. Connection of Transmission

21.7 Circuit design guide

To program Flash memory, programming tools require 4 signal lines, DSCL, DSDA, VDD, and VSS. When designing a PCB circuit, you should consider these 4 signal lines for on-board programming. In addition, you need to be careful when designing the related circuit of these signal pins, because rising/falling timing of the DSCL and DSDA is very important for proper programming.

When you use the OCD pins exclusively or share them with other functions, it needs to be careful, too. Figure 78 shows an example circuit where the OCD pins (DSCL and DSDA) are shared with other functions. They must be connected when debugging or executing In System Program (ISP).

Normally, the OCD pins are connected to outside to execute the predefined functions. Even when they are connected for debugging or executing ISP directly, the OCD pins are shared with other functions by using resistors as shown in Figure 78. By doing this, the OCD pins process the normal external signals and execute the OCD functions first when they are shared.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high-speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 78. PCB Design Guide for On-Board Programming

22 Package information

This chapter provides A96G140/A96G148/A96A148 package information.

22.1 48 LQFP package information

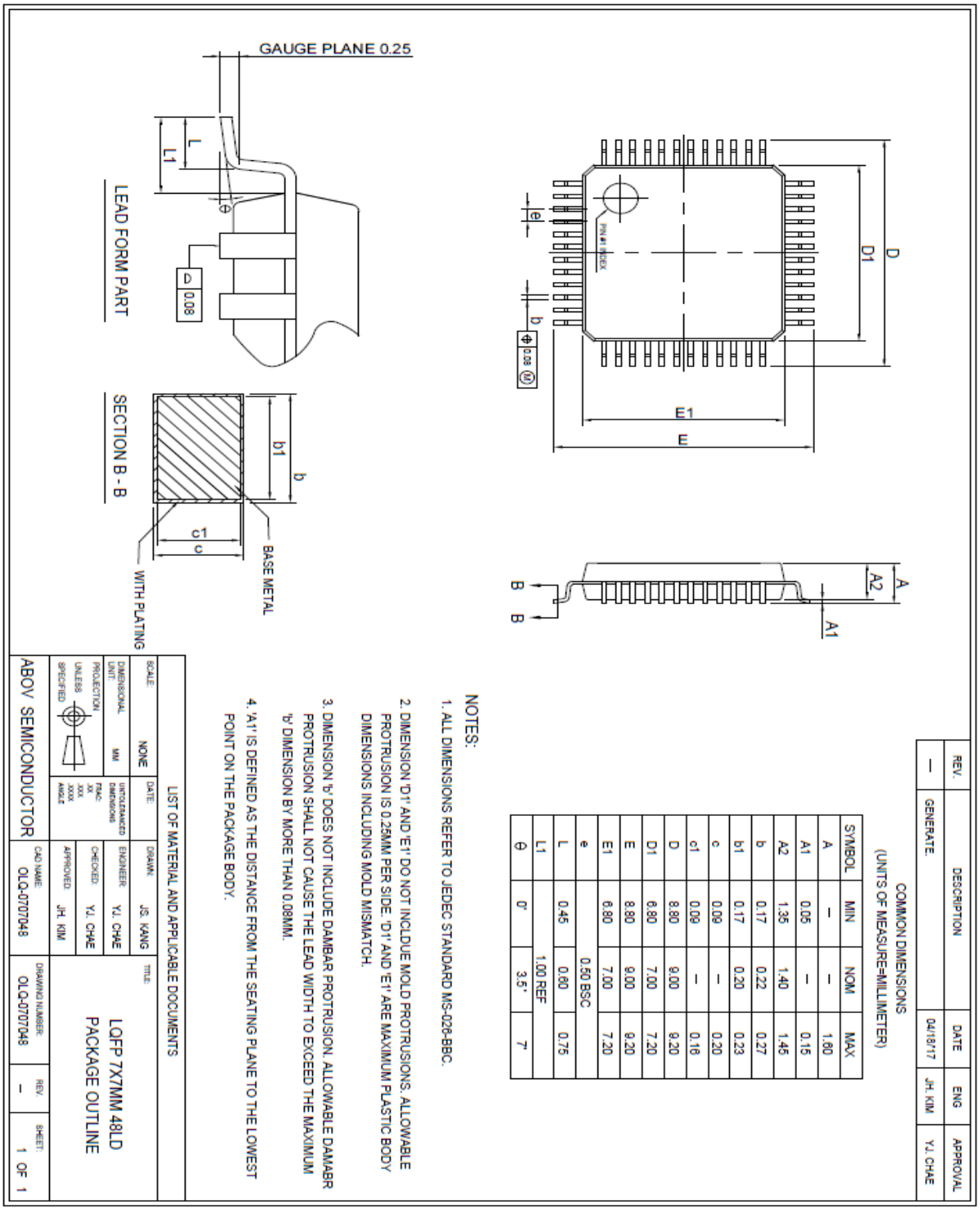


Figure 79 48 LQFP Package Outline

22.2 48 QFN package information

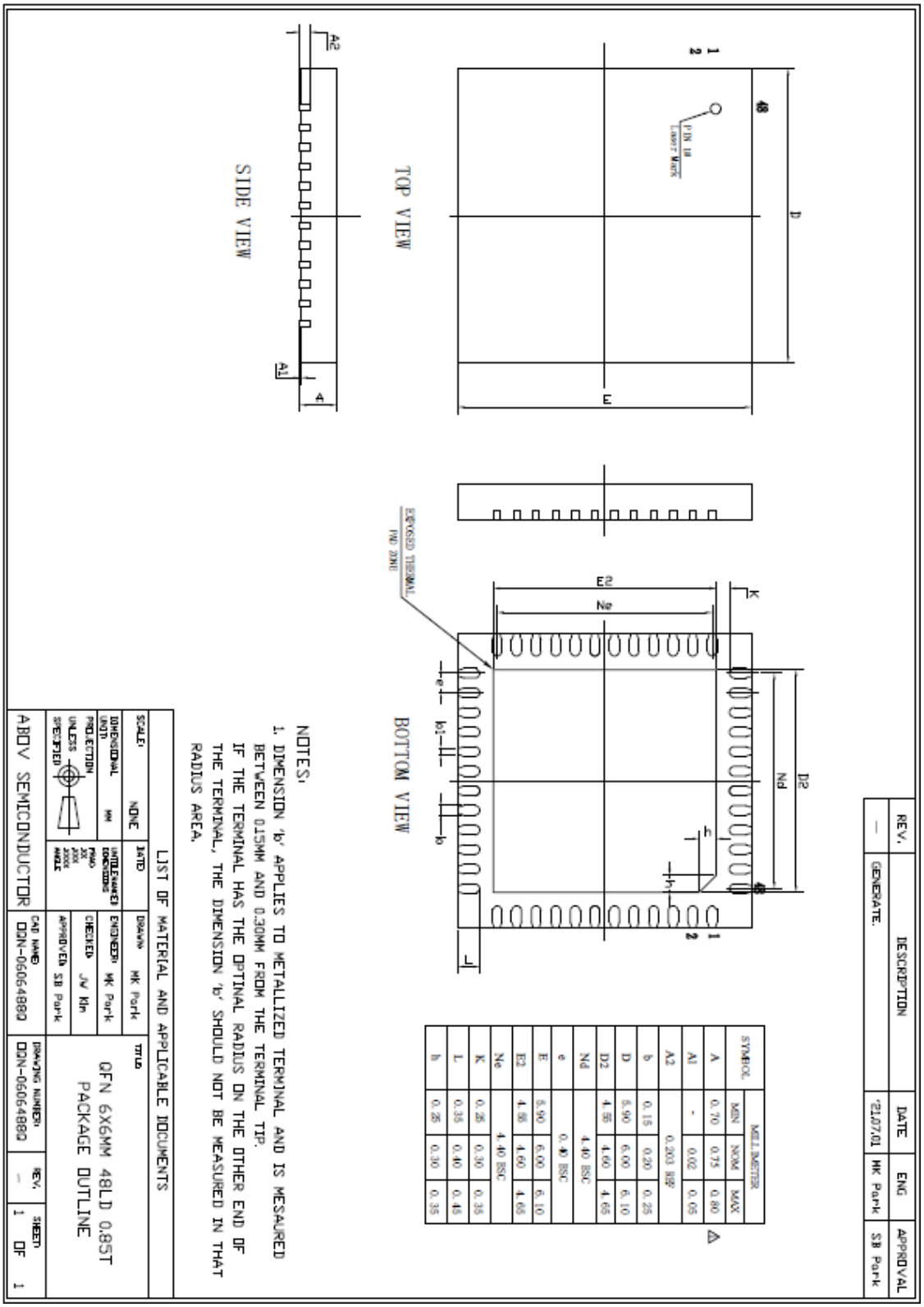


Figure 80 48 QFN Package Outline

22.3 44 MQFP package information

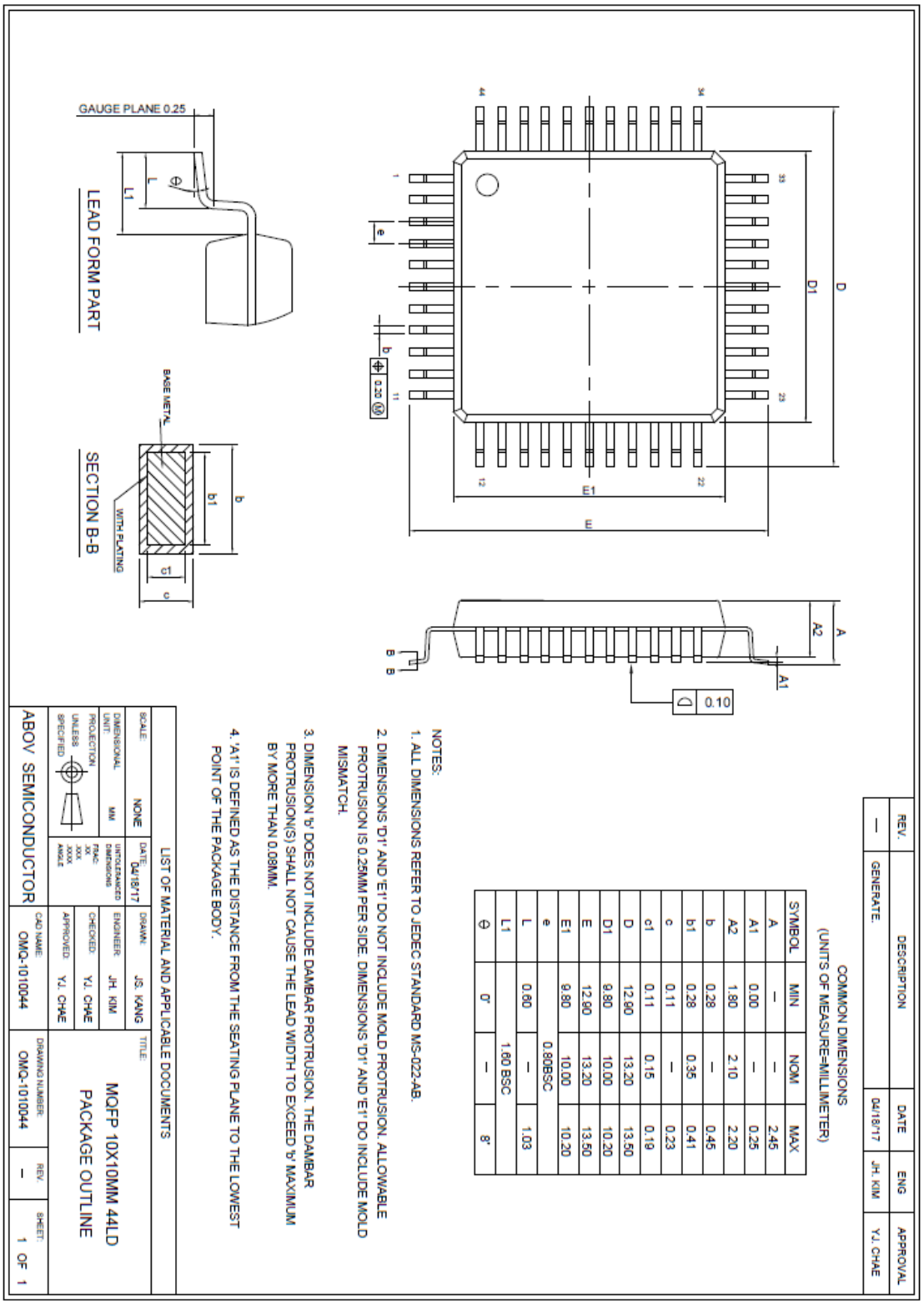


Figure 81 44 MQFP Package Outline

22.4 32 LQFP package information

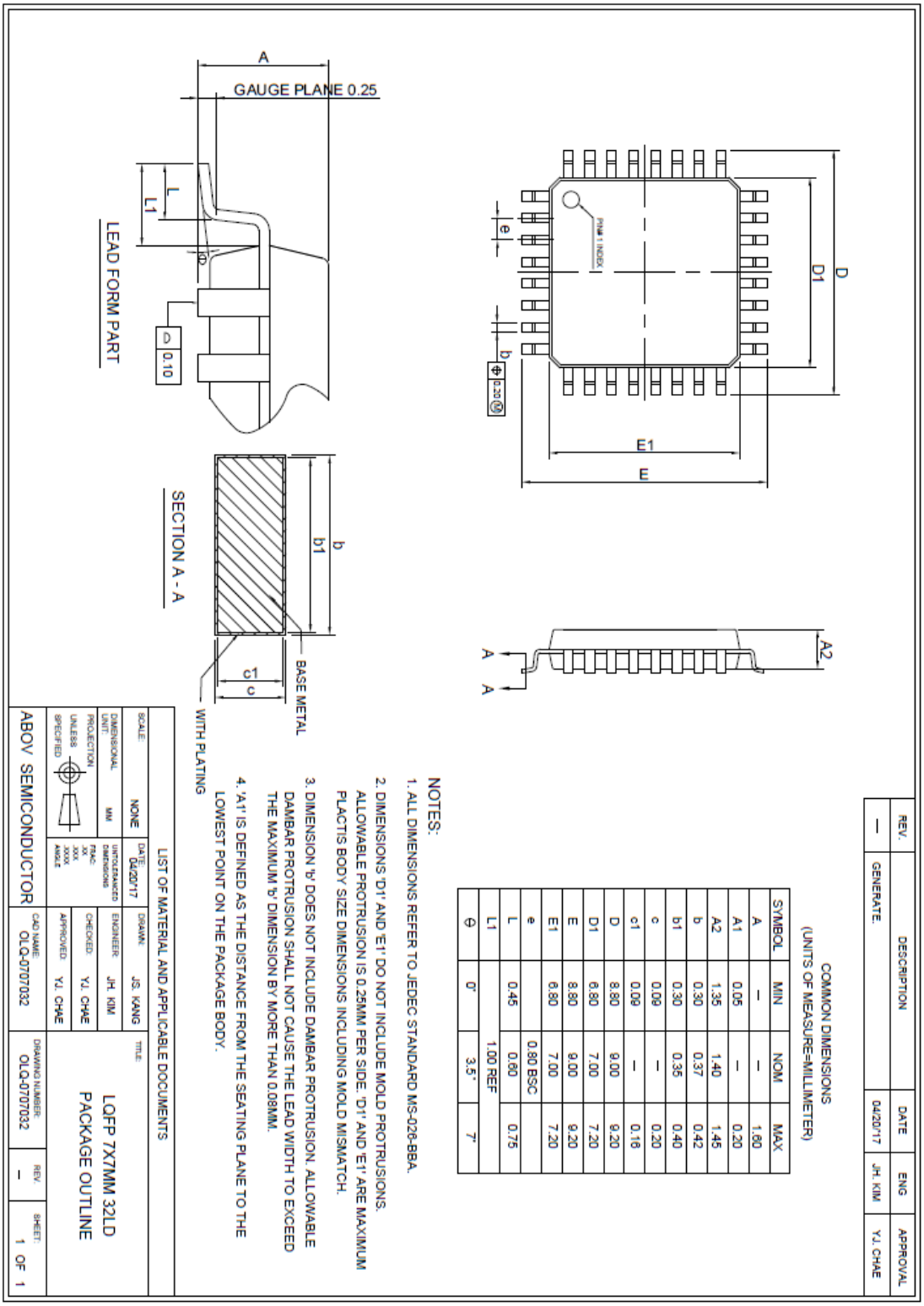


Figure 82 32 LQFP Package Outline

22.5 32 SOP package information

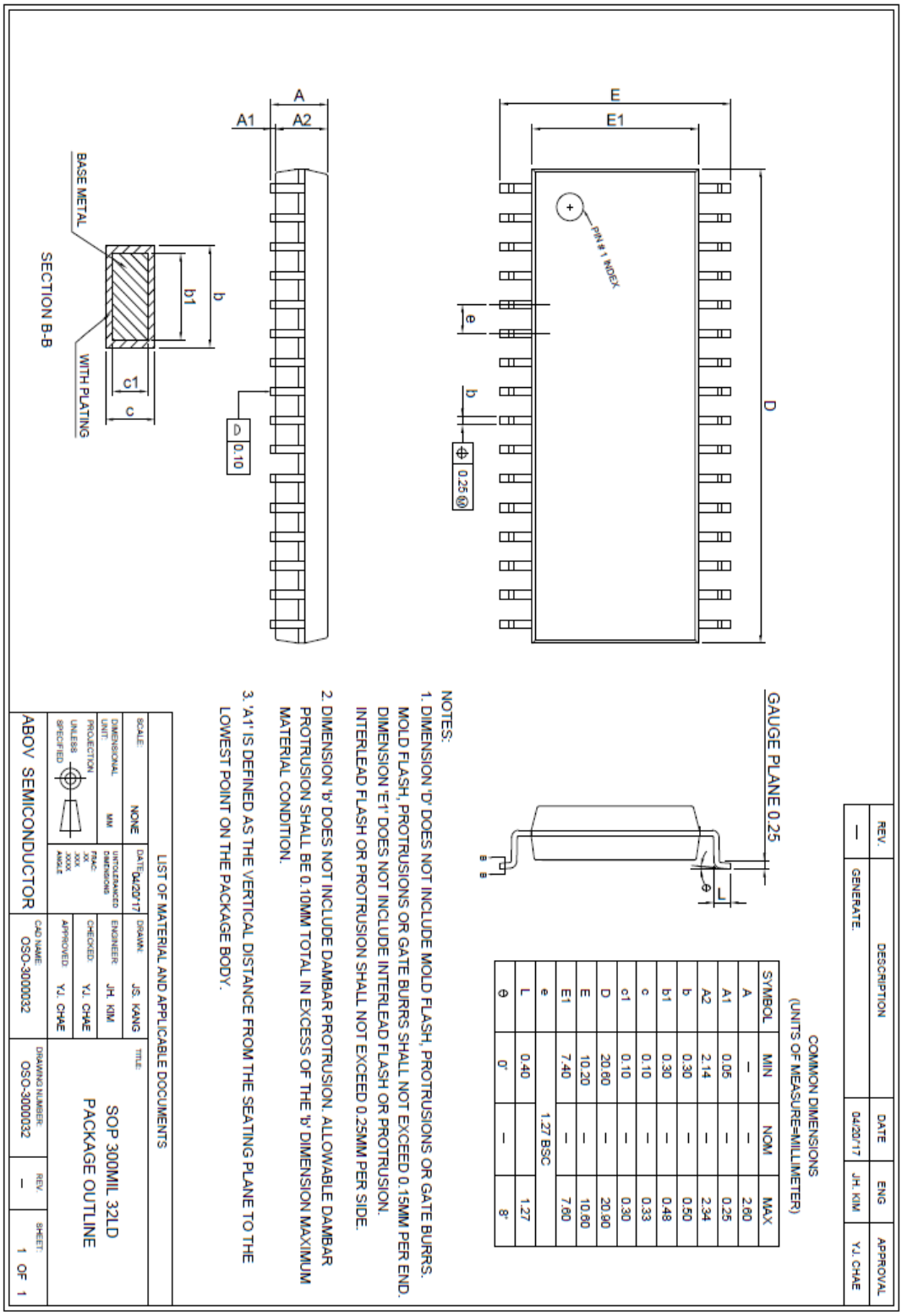


Figure 83 32 SOP Package Outline

22.6 28 SOP package information

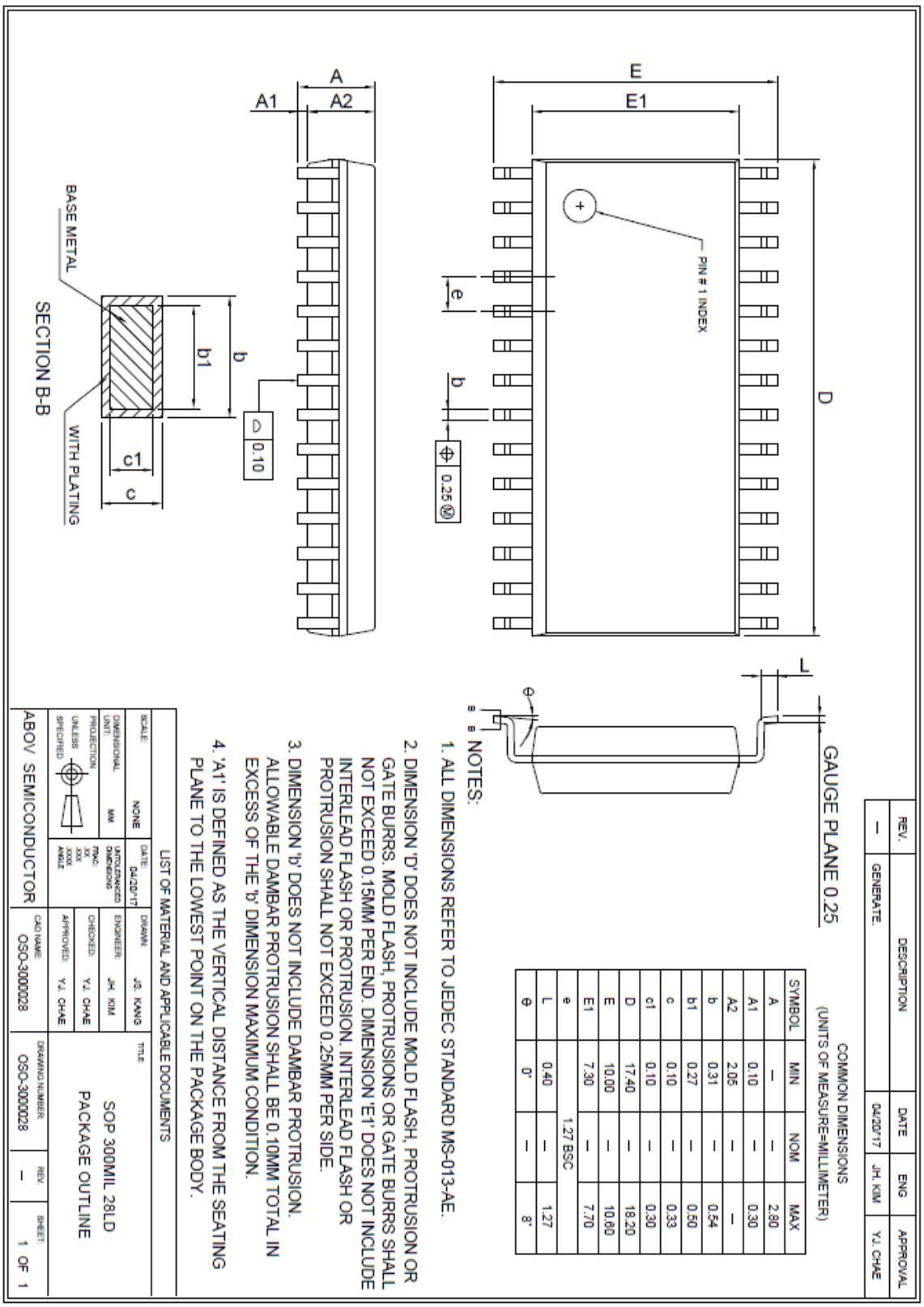


Figure 84 28 SOP Package Outline

22.7 28 TSSOP package information

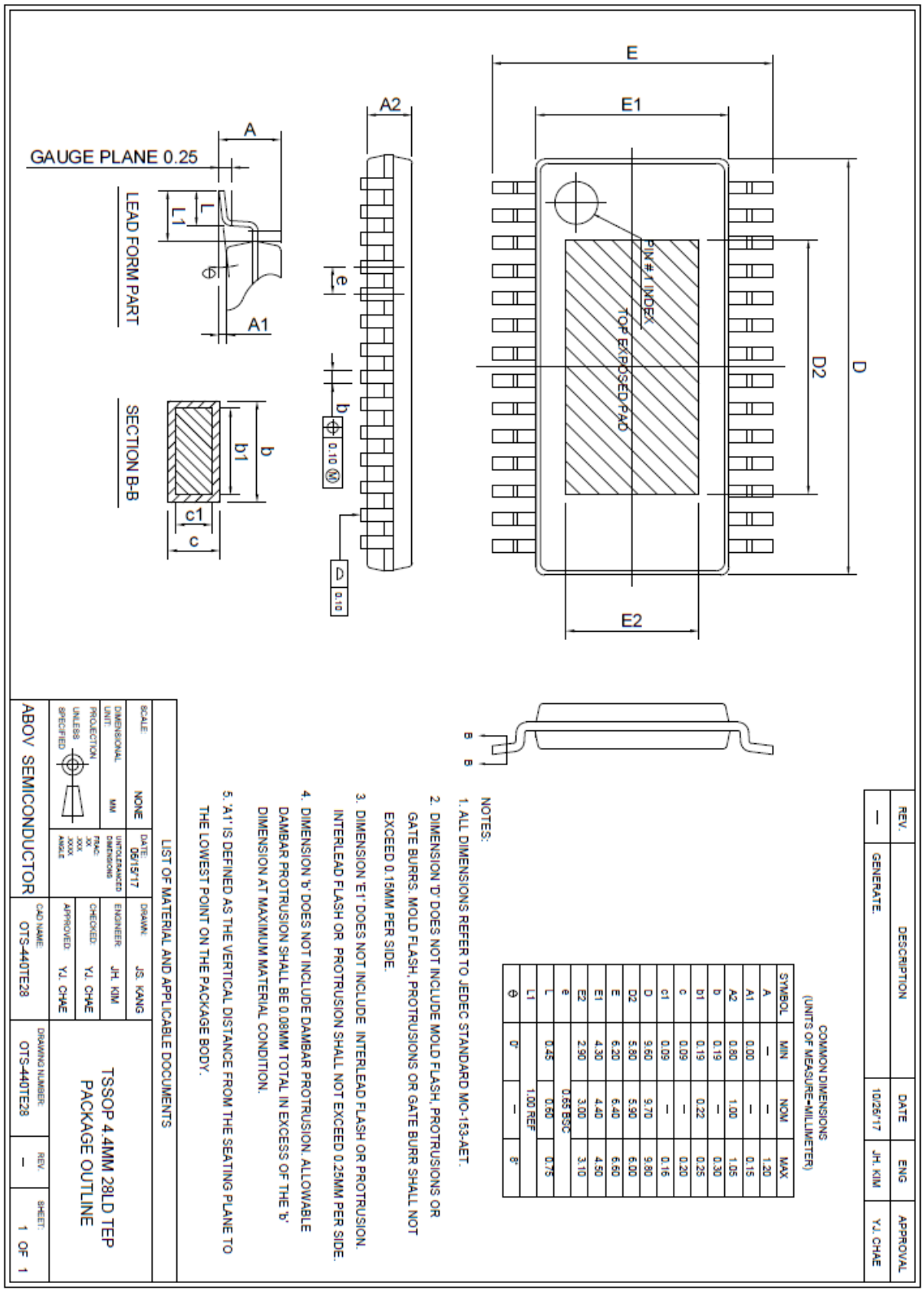


Figure 85 28 TSSOP Package Outline

23 Ordering information

Table 48. A96G140/A96G148/A96A148 Device Ordering Information

Device name	FLASH	XRAM	IRAM	ADC	I/O	Package	Temperature Range
A96G140CL	64K bytes	2304 bytes	256 bytes	16inputs	46	48 LQFP	-40°C ~ 85°C
A96G140CU				16inputs	46	48 QFN	
A96G140SQ				16inputs	42	44 MQFP	
A96G140KN				12inputs	30	32 LQFP	
A96G140KD*				12inputs	30	32 SOP	
A96G140GD*				11inputs	26	28 SOP	
A96G140GR*				11inputs	26	28 TSSOP	
A96G140CL2	64K bytes	2304 bytes	256 bytes	16inputs	46	48 LQFP	-40°C ~ 105°C
A96G140CU2				16inputs	46	48 QFN	
A96G140SQ2				16inputs	42	44 MQFP	
A96G140KN2				12inputs	30	32 LQFP	
A96G140KD2*				12inputs	30	32 SOP	
A96G140GD2*				11inputs	26	28 SOP	
A96G140GR2*				11inputs	26	28 TSSOP	
A96G148CL*	32K bytes	2304 bytes	256 bytes	16inputs	46	48 LQFP	-40°C ~ 85°C
A96G148CU*				16inputs	46	48 QFN	
A96G148SQ*				16inputs	42	44 MQFP	
A96G148KN*				12inputs	30	32 LQFP	
A96G148KD*				12inputs	30	32 SOP	
A96G148GD*				11inputs	26	28 SOP	
A96G148GR				11inputs	26	28 TSSOP	
A96A148GD				10inputs	26	28 SOP	
A96G148CL2*	32K bytes	2304 bytes	256 bytes	16inputs	46	48 LQFP	-40°C ~ 105°C
A96G148CU2*				16inputs	46	48 QFN	
A96G148SQ2*				16inputs	42	44 MQFP	
A96G148KN2*				12inputs	30	32 LQFP	
A96G148KD2*				12inputs	30	32 SOP	
A96G148GD2*				11inputs	26	28 SOP	
A96G148GR2				11inputs	26	28 TSSOP	
A96A148GD2				10inputs	26	28 SOP	

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

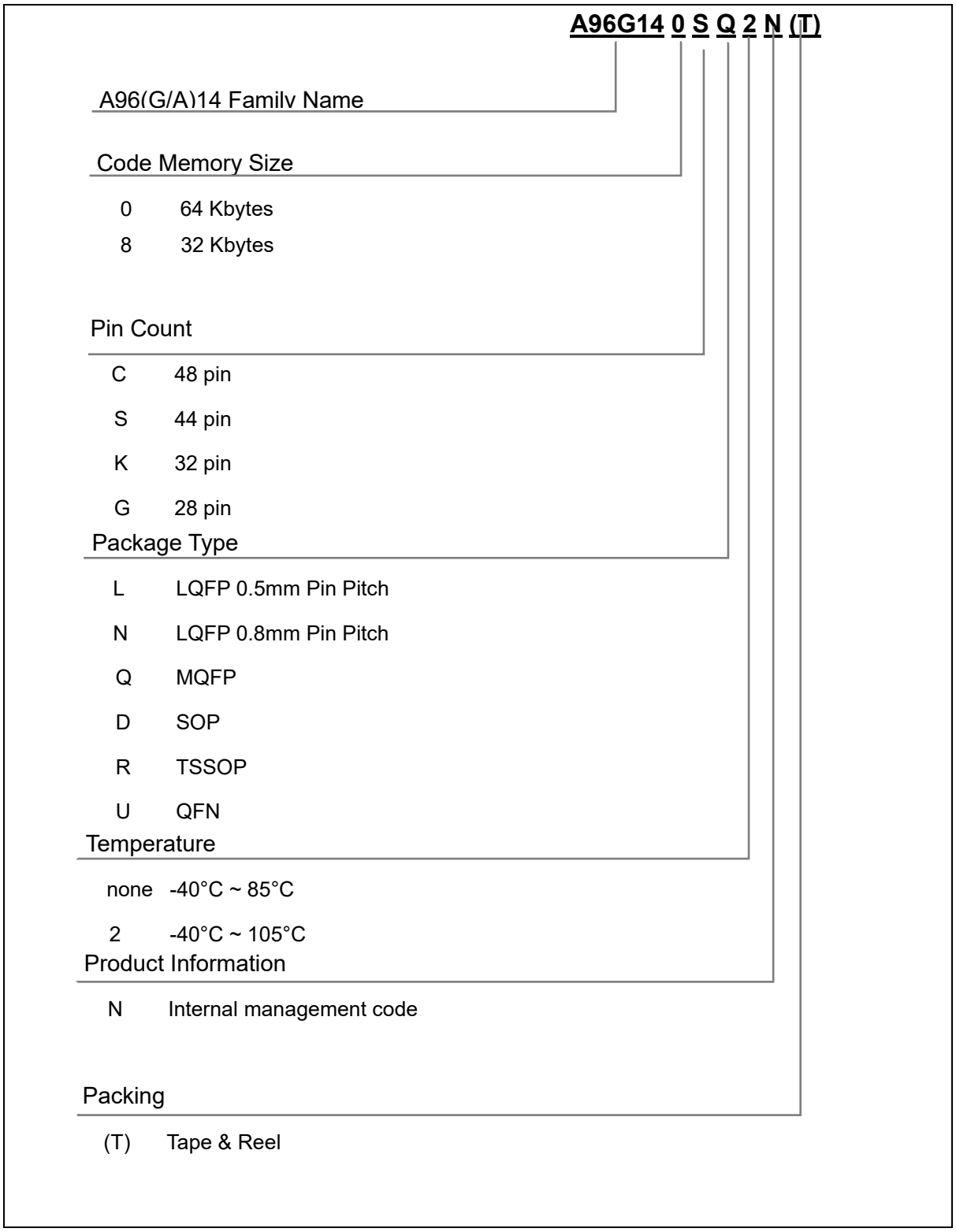


Figure 86. A96G140/A96G148/A96A148 Device Numbering Nomenclature

Appendix

Instruction table

Instructions are either1, 2 or 3bytes long as listed in the ‘Bytes’ column below. Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

Table 49. Instruction Table

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 49. Instruction Table (continued)

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 49. Instruction Table (continued)

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 49. Instruction Table (continued)

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 49. Instruction Table (continued)

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 49. Instruction Table (continued)

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00
ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, entries such as E8-EF indicate continuous blocks of hex opcodes used for 8 different registers. Register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as ‘11→F1’ (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

CJNE instructions use abbreviation of #d for immediate data; other instructions use #data as an abbreviation.

Revision history

Date	Revision	Description
2019.08.05	1.00	First creation
2019.10.02	1.10	Added Receive Time Out (RTO) and 0% Error Baud Rate features of USART on page 15. Corrected the device name from A96G140/A96G148KL to A96G140/A96G148/A96A148KN on page 19. Corrected the internal frequency from 16MHz to 32MHz in 7.6 High Internal RC Oscillator Characteristics on page 246. Added the additional description of UCTRL4 on page229.
2019.10.14	1.11	Deleted Special Test Mark (V, High voltage stressed) on page 284 Changed the minimum voltage of crystal OSC from 2.0V to 2.2V on page 15, 244 and 255. Added the contents of A96G148 with 32 Kbytes of FLASH.
2019.10.16	1.12	Corrected the maximum specification of OSC feedback resistor in 19.8 DC Characteristics on page 247.
2019.12.02	1.13	Modified the temperature specification to 85°C in 7.6 High Internal RC Oscillator Characteristics on page 246. Updated 19.4 Power-on Reset Characteristics on page 245 Updated 19.5 Low Voltage Reset and Low Voltage Indicator Characteristics on page 245
2020.02.04	1.14	Added the disclaimer and modified the distributor.
2020.02.06	1.15	Revised A96G140 to A96G140/A96G148
2020.02.18	1.16	Added to A96A148 device
2020.02.21	1.17	Corrected typographical errors
2020.03.13	1.18	Corrected typographical errors & Revise “Product selection table”
2020.04.02	1.19	Revised ″Ordering information″
2020.05.22	1.20	Revised “Low voltage reset and low voltage indicator characteristics”
2020.06.08	1.21	Corrected the I/O symbol of LED0 ~ LED7 to O at Table 3. Normal Pin Description. Updated Basic Interval Timer Block Diagram at Figure 18. Updated Watchdog Timer Block Diagram at Figure 19. Added the description of V_{LVD}/V_{LVI} at Table 22. LVR and LVI Characteristics. Extended maximum operating temperature up to 105°C as well as 85°C.
2020.07.20	1.22	Corrected the conditions of Supply Current at Table 25. DC Characteristics. Updated the table and figures for USART characteristics in 19 Electrical characteristics. Corrected the minimum A/D Conversion time to 7.5us at Table 20. A/D Converter Characteristics.
2020.08.31	1.23	Advanced Flash Endurance times from 10,000 to 30,000.
2020.09.28	1.24	Updated the initial value in Table 6. SFR Map. Updated a typo in Figure 116. Fast VDD Rising Time and Figure 117. Internal RESET Release Timing On Power-Up.
2021.01.26	1.25	Added the temperature condition of ″-10°C to 70°C″ at Table 23. High Speed Internal RC Oscillator Characteristics

		Corrected the configuration read timing at Figure 118. Configuration Timing when Power-on
2021.02.03	1.26	Corrected the configuration timing diagram at Figure 117. Configuration Timing when Power-on and Figure 123. Configuration Timing When LVR RESET.
2021.03.05	1.27	Added 48 QFN package in 22 Package information and 23 Ordering information.
2021.03.11	1.28	Changed the value of total power dissipation(P_T) from 600 mW to 800 mW in Absolute Maximum Ratings. Deleted the table of Input/Output Capacitance in Electrical Characteristics.
2021.04.23	1.29	Changed the figures of Package Outline Drawing in 22 Package information Chapter. Updated High Speed Internal RC Oscillator Tolerance at Table 54. High Speed Internal RC Oscillator Characteristics. Corrected the frequency unit from KHz to kHz.
2021.04.23	1.30	Added 4.Central Processing Unit chapter. Updated 21. Development tools chapter. Marked simulation data in 20. Electrical characteristics. Added Figure 57. Filters used on a Reset Pin Diagram and Table 37. Reset Pin Component Values on page 98. Added the graph of current consumption according to voltage by temperature at 20.22 Typical characteristics on page 99 to page 102. Changed 48 QFN package information in 22 Package information chapter.
2022.11.21	1.31	Updated font style of this document

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