A96L533/ A96L534 Datasheet

SoC for the Purpose of Fire Safety System, Multi Chip Package with LDO 3V

Datasheet Version 1.03

Features

CPU

- 8-bit CISC core (M8051, 2 clocks per cycle)

ROM (FLASH) capacity

- 8/16Kbytes Flash with self-read/ write capability: 10,000 cycles
- On Chip debug and ISP
- 256bytes IRAM, 256/ 768bytes XRAM
- 256bytes Data Flash: 100,000 cycles

Timer/ counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watchdog Timer (WDT) 8-bit × 1-ch
- 16-bit × 3-ch (T0/ T1/ T2)
- Pulse generation (by T0/ T1/ T2)

10-bit ADC

- 5 Input channels
- V_{BGR}: 0.92V ±3% (T_A = -40℃ to +85℃)
- LDO (MCU): 2.32V ±3.45% (T_A = 25℃)

OP-AMP

- 2 channels, Rail-to-rail output

16-Bit CRC/checksum generator

- Auto and User CRC/ Checksum mode

Reset

- Reset release level (MCU, VDD 1.4V)
- Low voltage reset (MCU)
  - 4 levels detect (1.60/ 2.20/ 2.40/ 2.70V)
- Reset release level (Logic, Vin 6.7V)

Constant sink current generator

- 2 channels 16-step selectable
- Max. 274mA sink current

USART (UART + SPI)

- 8bit UART x 1ch or 8bit SPI x 1ch

Interrupt sources

- 13 interrupts (External, Timer, WDT, BIT, USART, ADC)

Internal RC Oscillator

- 4MHz ±3.0% (T_A=-40 to +85°C)

Power-down mode

- STOP mode and IDLE mode

Operating Temperature

- -40 to +85℃

Package Type

- 16 SOPN, Pb-free package

VIN voltage range (Logic)

- Power Supply: 8.5V to 42V
- Signal Input: 0.0V to 42V

Low power consumption (Logic)

- Max. 90uA (@24V, Room Temp)

Low Drop-out (Logic)

- 3V ± 3% (@24V, -10°C to +60°C)

Application

- Fire safety system

Product selection table

Table 1. Device Summary

Part number	Flash	iRAM/ XRAM	USART	Timer	Data Flash	LDO	Const. current	Op-Amp	ADC	I/O	Package
A96L533AE	8KB	256/256B	1	3	256B	3V	2	2	5ch	12	16 SOPN
A96L534AE	16KB	256/768B	1	3	256B	3V	2	2	5ch	12	16 SOPN

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1 Description

A96L533/ A96L536 (A96L53x) is an MCP (Multi Chip Package) product that combines MCU and Logic. It consists of advanced CMOS 8-bit microcontroller with 8/16Kbytes of FLASH MCU product and 3V output Logic product.

A96L53x is a powerful microcontroller featuring low power consumption, and provides cost effective solutions to the stand-alone smoke detector applications. It supports Power-down modes to reduce power consumption.

1.1 Device overview

In this section, features of A96L53x and peripheral counts are introduced in Table 2.

Table 2. A96L53x Device Features and Peripheral Counts

Peripheral(MCU)		**A96L53x**
CPU		8-bit CISC core (M8051, 2 clocks per cycle)
Flash		• 8/16 Kbytes with self r/w capability • On chip debug and ISP • Endurance: 10,000 cycles
IRAM		256bytes
XRAM		256/768bytes
Data Flash		• 256bytes • Endurance: 100,000 cycles
GPIO		• Normal I/Os • 12 ports: P0[7:0], P1[5:0], (P11, P14 PAD only)
Timer/ counter		• BIT 8-bit x 1-ch • WDT 8-bit x 1-ch: 1KHz internal RC oscillator for WDT or LF internal RC oscillator for WDT • 16-bit x 3-ch (T0/T1/T2)
Programmable pulse generation		Pulse generation (by T0/T1/T2)
ADC		• 10-bit ADC, 5 input channels • V_{BGR}: 0.92V ±3%(T_A = -40℃ to +85℃) • LDO: 2.32V ±3.45%(T_A = 25℃)
Operational amplifier		• 2-ch • Rail-to-rail output
CRC and checksum generator		• 16-bit • Auto and user CRC/ checksum mode
Reset	Power on reset	Reset release level (1.4V)
	Low voltage reset	4 level detect (1.60V/ 2.20V/ 2.40V/ 2.70V)

Table 2. A96L53x Device Features and Peripheral Counts(continued)

Peripheral(MCU)	**A96L53x**
Constant sink current generator	• 2-ch • 16-steps selectable • Max. 274mA sink current
USART	UART + SPI • 8-bit UART x 1-ch • 8-bit SPI x 1-ch
Interrupt sources	• External interrupts: EINT0/1/2/3/10 (5) • Timer0/1/2,(3) • WDT(1) • BIT(1) • ADC (1) • USART Rx/ Tx (2)
Internal RC oscillator	4MHz ± 3.0% (T_A = -40℃ to +85℃)
Power down mode	STOP, IDLE
Operating voltage and frequency	• 2.0V to 3.6V @ 0.5 to 4.0MHz with HFIRC • 2.0V to 3.6V @ 32KHz with LFIRC • Voltage dropout converter included for core
Minimum instruction execution time	0.25us @ 4MHz HFIRC
Package type	• 16 SOPN • Pb-free package
Function (Logic)	**Description**
VIN voltage range	• Power supply 8.5V to 42V • Signal input 0.0V to 42V
Low power consumption	Max. 90uA (@24V, room temperature)
Low Dropout (LDO) voltage	3V ± 3% (@24V, -10℃ to 60℃)
LDO drive ability	20mA (@VOUT = 24V)
Under Voltage Lockout (UVLO)	Internal UVLO function
Line interface	• Comparator for line interface Rx • TR for line interface Tx
ESD performance	• 2000V human body model • 200V machine model
RF-EMS(IEC 61000-4-3)	LV3(10V/m)
Common	**Description**
Operating temperature	-40℃ to 85℃ ambient temperature

1.2 Block diagram

Figure 1 and Figure 2 describe A96L53x in block diagrams.

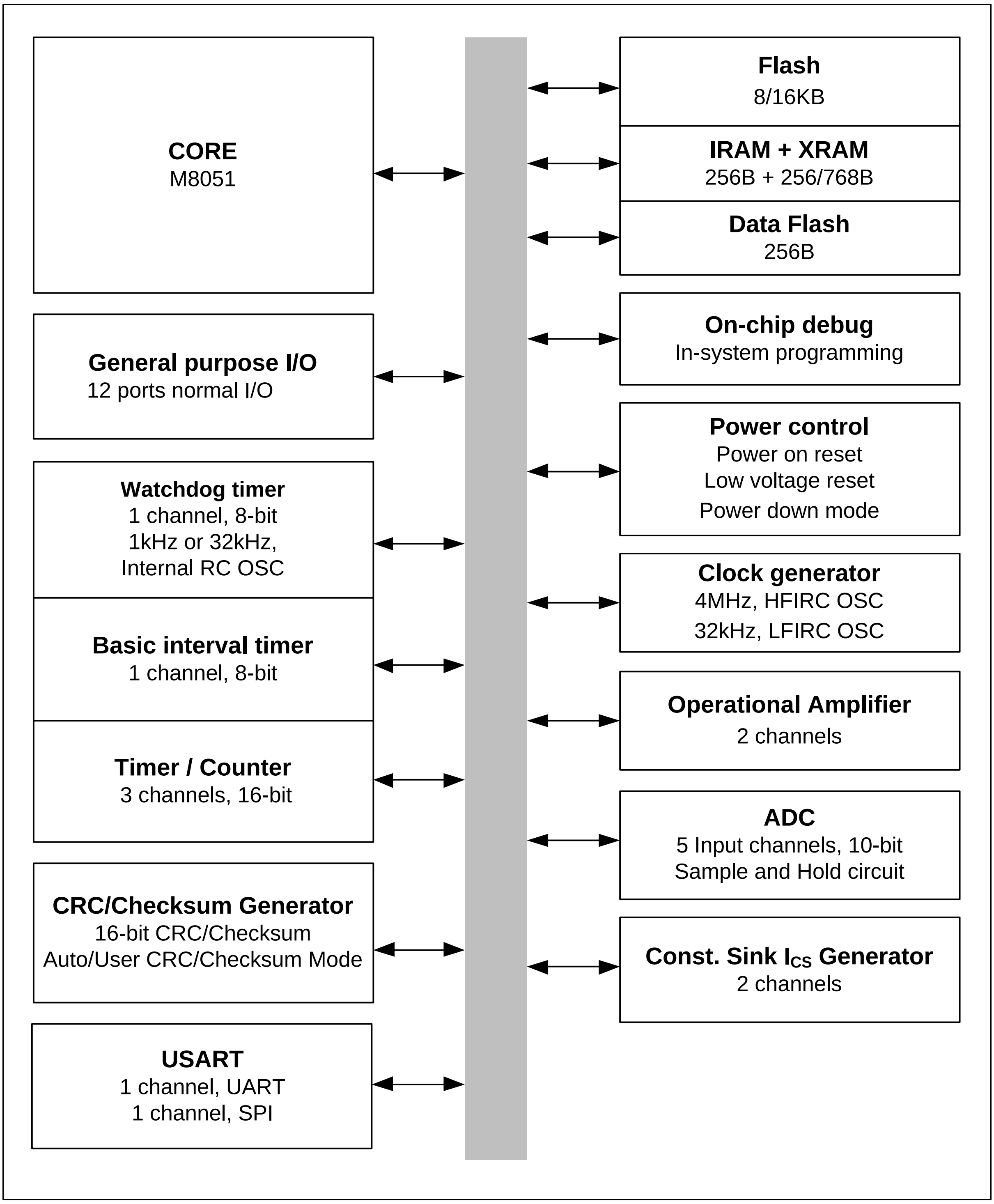


Figure 1. A96L53x Block Diagram (MCU Part)

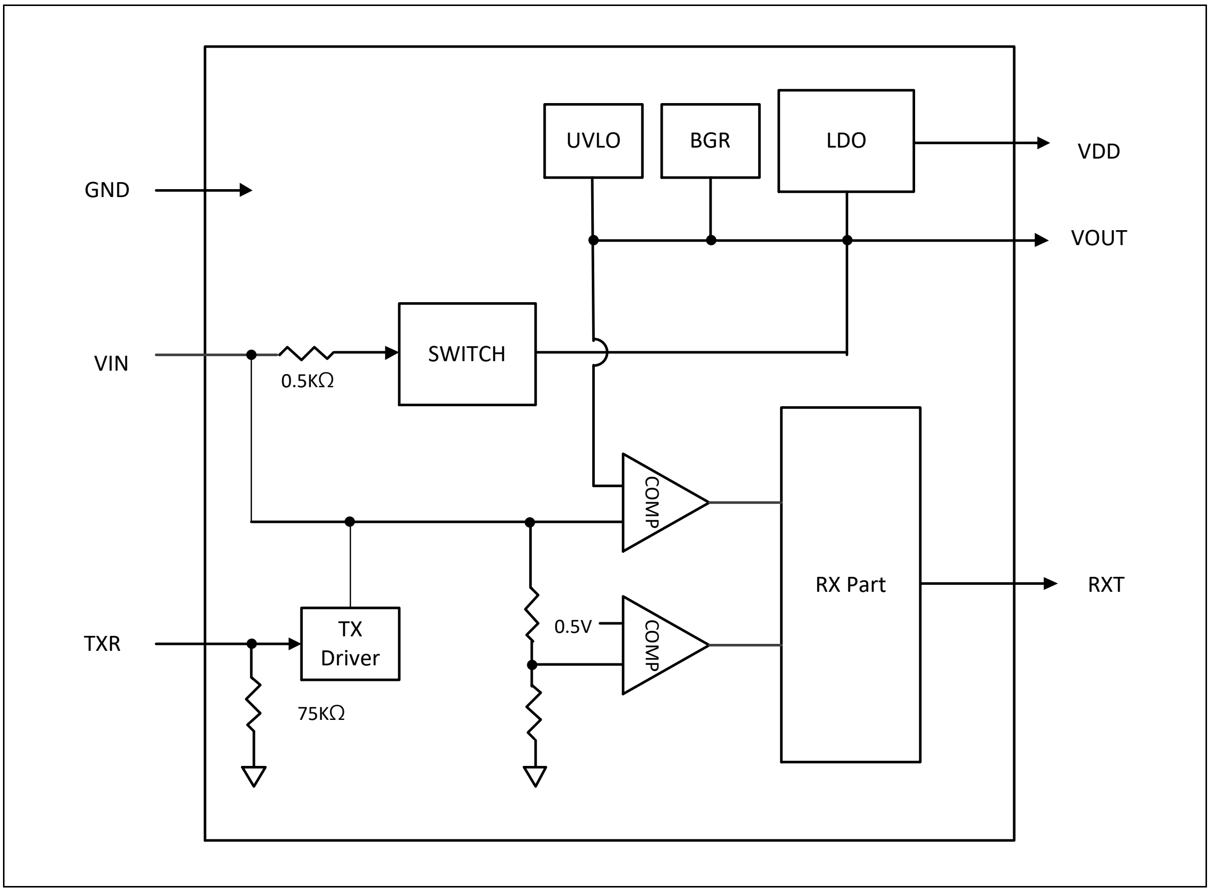


Figure 2. A96L53x Block Diagram (Logic Part)

1.3 Functional description

In the following sections, each feature of the A96L53x series microcontroller is briefly introduced.

1.3.1 CMOS 8051 core

A96L53x is an advanced CMOS 8-bit microcontroller with 8/ 16Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. Since A96L53x uses Mentor 8051 as a core and its ROM is smaller than 8/ 16Kbytes in size, a developer can use any standard 8051 compiler of other providers.

1.3.2 8/16Kbytes internal code Flash memory

A 16-bit program counter is capable of addressing up to 64Kbytes, and this device has 8/ 16Kbytes program memory space.

1.3.3 256bytes internal SRAM

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128bytes, upper 128bytes, and SFR space respectively.

1.3.4 256/768bytes XRAM

XRAM data has 256/ 768bytes. This depends on the device type.

1.3.5 Data Flash

The write/ erase cycles of the internal Data Flash can be increased significantly if it is divided into smaller and used in turn. If 256bytes are divided into 8 areas with 32bytes and each area from 1st to 8th is used for up to 100,000 cycles, the total number of erase/ write cycles can be 800,000.

1.3.6 I/O ports

A96L53x has two groups of I/O ports (P0 and P1). Each can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. In addition, P0 and P1 include a function that can generate interrupts according to the change of state of the pin.

1.3.7 Interrupt controller

A96L53x supports up to 13 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software.

1.3.8 Clock generator

The default system clock is 4MHz INT-RC Oscillator and the default division rate is one. To stabilize the system internally, the 4MHz INT-RC Oscillator is used on POR.

1.3.9 Basic Interval Timer (BIT)

A96L53x has one 8-bit Basic Interval Timer that is free-run and can’t stop. The Basic Interval Timer generates a time base for Watchdog Timer counting, and provides a Basic Interval Timer Interrupt (BITIFR).

1.3.10 Watchdog Timer (WDT)

The Watchdog Timer rapidly detects the CPU malfunction such as endless looping caused by noise or other similar causes, and resumes the CPU to the normal state.

1.3.11 Multi-purpose 16-bit timer

Four-channel 16-bit timers and one-channel low power general-purposed 16-bit timer support the functions below:

- 16-bit timer/ counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

1.3.12 10-bit Analog-to-Digital Converter (ADC)

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to corresponding 10-bit digital value. LDO23 can be used as a reference voltage of the ADC and can be output through an external pin.

1.3.13 Operational Amplifier (OP-AMP)

A96L53x has two channel Operational Amplifiers (OP-AMP). There are three registers for the OP-AMP which are OP-AMP Control Register 0 (AMPCR0), OP-AMP Control Register 1 (AMPCR1), and Chopper Control Register (CHPCR).

1.3.14 USART (UART and SPI)

USART supports UART and SPI mode. Only one of them can be used.

1.3.15 Constant sink current generator

Constant Sink Current Generator could provide constant current while I_{CS} voltage ranges from 1.8V to 3.6V. The constant current value is controlled by configuring the ICSDR0/ ICSDR1 registers, and the sink current is between 50mA and 290mA.

1.3.16 Flash CRC/checksum generator

The Flash CRC (Cyclic Redundancy Check) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial.

1.3.17 Power-down operation

A96L53x has two Power-down modes to minimize the power consumption of the device. In Power-down mode, the power consumption is reduced considerably. The device provides two kinds of power saving functions, IDLE mode and STOP mode. In these two modes, programs are stopped.

1.3.18 Reset

A96L53x has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0`)
- OCD Reset

1.4 Logic functional description

1.4.1 Initial function

The VDD voltage increases as the external power VIN voltage increases. If the VDD voltage is 2.4V, then the UVLO signal goes to high and by this signal, the internal reset is released.

1.4.2 Power charging

A96L53x has the inrush current limit that is set by PMOS transistor. If the VIN voltage level is higher than the VOUT voltage level, the switch turns on via the comparator. At this time, the capacitor C0 of VOUT becomes charged state, and if VOUT voltage is higher than or equal to VIN, the switch turns off.

1.4.3 LDO description

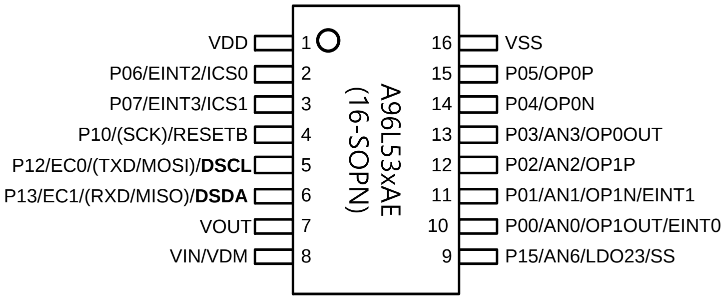
A96L53x includes one LDO (Low Drop Output voltage) for microcontroller and indicated LED driver power. In the initial operation phase, when the power/ signal line is connecting to VIN pin, the C0 capacitor on pin VOUT is charged.

2 Pinouts and pin descriptions

This chapter provides pinouts and pin descriptions of A96L53x series.

2.1 Pinouts

Figure 3 shows a pin diagram of 16 SOPN package.



NOTE: For the On-Chip Debugging, ISP assigns P1[2:3] pins for DSCL and DSDA respectively.

Figure 3. A96L53xAE 16 SOPN Pinouts

2.2 Pin description

Table 3. 16 SOPN Pin Description

Pin name	I/O	Function	@reset	Shared with
P00	I/O	The port 0 is a bit-programmable I/O port which can be configured as an input (P00/P01/P06/P07: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0/OP1OUT/EINT0
P01				AN1/OP1N/EINT1
P02				AN2/OP1P
P03				AN3/OP0OUT
P04				AN4/OP0N
P05				AN5/OP0P
P06				EINT2/ICS0
P07				EINT3/ICS1
P10	I/O	The port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	(SCK)/RESETB
P11 NOTE1				EINT10/RXT(PAD only)
P12				EC0/(TXD/MOSI)/DSCL
P13				EC1/(RXD/MISO)/DSDA
P14 NOTE2				TXR(PAD only)
P15				AN6/LDO23/SS
EINT0	I/O	External interrupt inputs	Input	P00/AN0/OP1OUT
EINT1				P01/AN1/OP1N
EINT2				P06/ICS0
EINT3				P07/ICS1

NOTES:

1. P11 does not have a port, only PAD inside IC. For RX of line interface communication, it is connected within the logic and IC. User must set it to external interrupt or input port.
2. P14 does not have a port, only PAD inside IC. For TX of line interface communication, it is connected between Logic and IC inside. Users must set it as an output port and use. If the users do not intend to communicate, the output must be set to low.

Table 3. 16 SOPN Pin Description (continued)

Pin name	I/O	Function	@reset	Shared with
EC0	I/O	Timer 0 event count input		P12/(TXD/MOSI)/DSCL
EC1	I/O	Timer 1 event count input		P13/(RXD/MISO)/DSDA
AN0	I/O	A/D converter analog input channels	Input	P00/OP1OUT/EINT0
AN1				P01/OP1N/EINT1
AN2				P02/OP1P
AN3				P03/OP0OUT
-				-
-				-
AN6				P15/LDO23/SS
LDO23	I/O	LDO voltage output	Input	P15/AN6/SS
OP0P	I/O	OP-AMP 0 positive input	Input	P05
OP0N	I/O	OP-AMP 0 negative input	Input	P04
OP0OUT	I/O	OP-AMP 0 output	Input	P03/AN3
OP1P	I/O	OP-AMP 1 positive input	Input	P02/AN2
OP1N	I/O	OP-AMP 1 negative input	Input	P01/AN1/EINT1
OP1OUT	I/O	OP-AMP 1 output	Input	P00/AN0/EINT0
TXD	I/O	UART data output	Input	P12/EC0/MOSI/DSCL
RXD	I/O	UART data input	Input	P13/EC1/MISO/DSDA
MOSI	I/O	SPI master output, slave input	Input	P12/EC0/TXD/DSCL
MISO	I/O	SPI master input, slave output	Input	P13/EC1/RXD/DSDA
SCK	I/O	SPI clock input/output	Input	P10/RESETB
SS	I/O	SPI slave select input	Input	P15/AN6/LDO23

Table 3. 16 SOPN Pin Description (continued)

Pin name	I/O	Function	@reset	Shared with
ICS0	I/O	Constant sink current pins	Input	P06/EINT2
ICS1				P07/EINT3
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION.	Input	P10/SCK
DSCL	I/O	On chip debugger clock input	Input	P12/EC0/(TXD/MOSI)
DSDA	I/O	On chip debugger data input/output	Input	P13/EC1/(RXD/MISO)
VDD, VSS	–	Power input pins VDD is Connected with Logic LDO	–	–
VDD (LDO)	–	Power output pin (From Logic). LDO Power input pin(To MCU)	–	–
VOUT	O	Internal Power Pin. Connect to Capacitor	Output	–
VIN/VDM	I	External Power Pin & Bridge Output Pin	Input	–

NOTES:

1. The P10/RESETB pin is configured as one of the P10/SCK and the RESETB pin by the “CONFIGURE OPTION”.
2. If the P13/DSDA and P12/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P13/DSDA and P12/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
4. LDO23 and Logic's LDO are different pins. LDO23 is a 2.3V output that can be used as the reference voltage of the ADC, which is generated from the MCU. Logic LDO is a 3V signal generated by Logic and is connected to the inside of IC through VDD of MCU.

3 Port structures

3.1 GPIO port structure

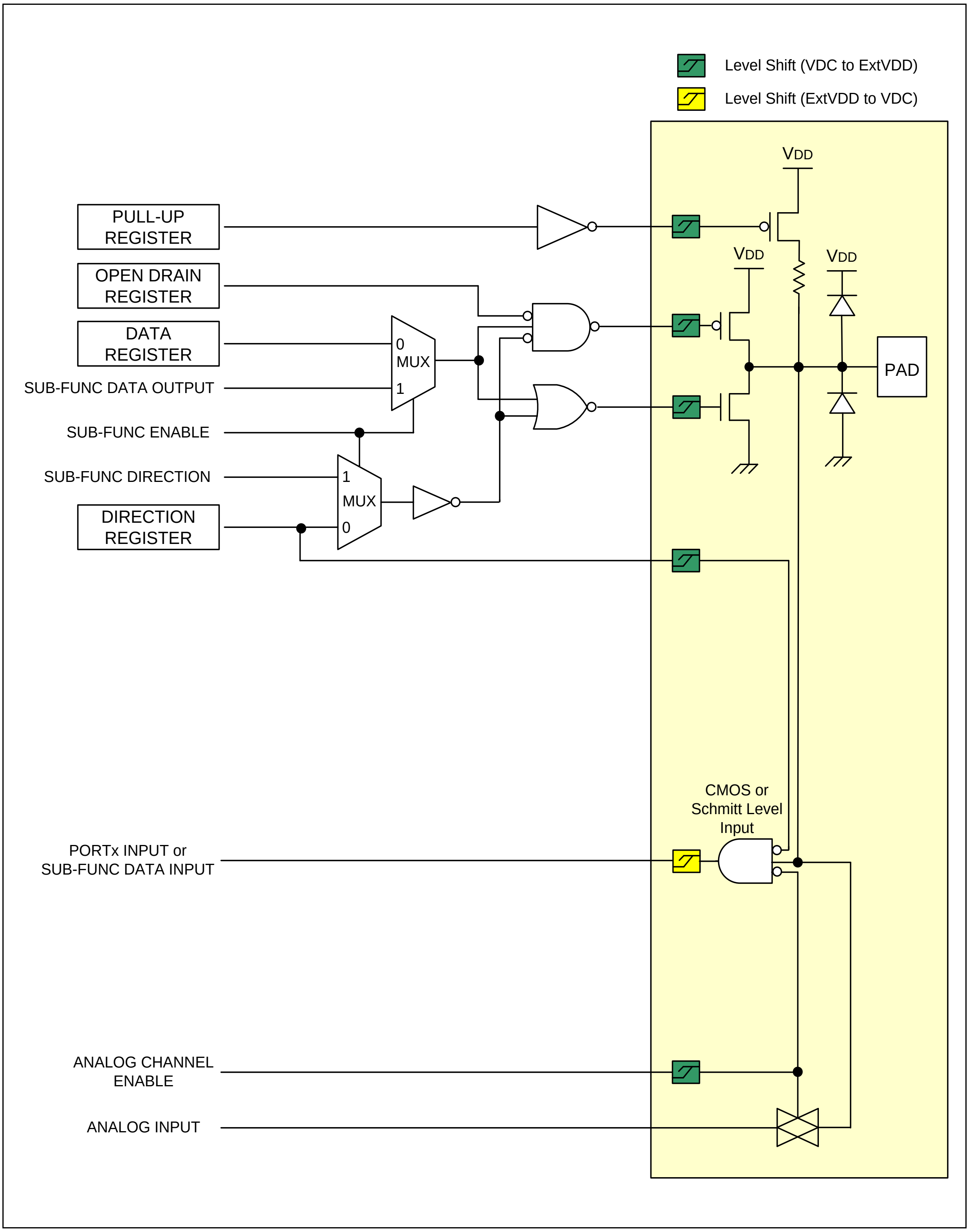


Figure 4. General Purpose I/O Port Structure

3.2 External interrupt I/O port structure

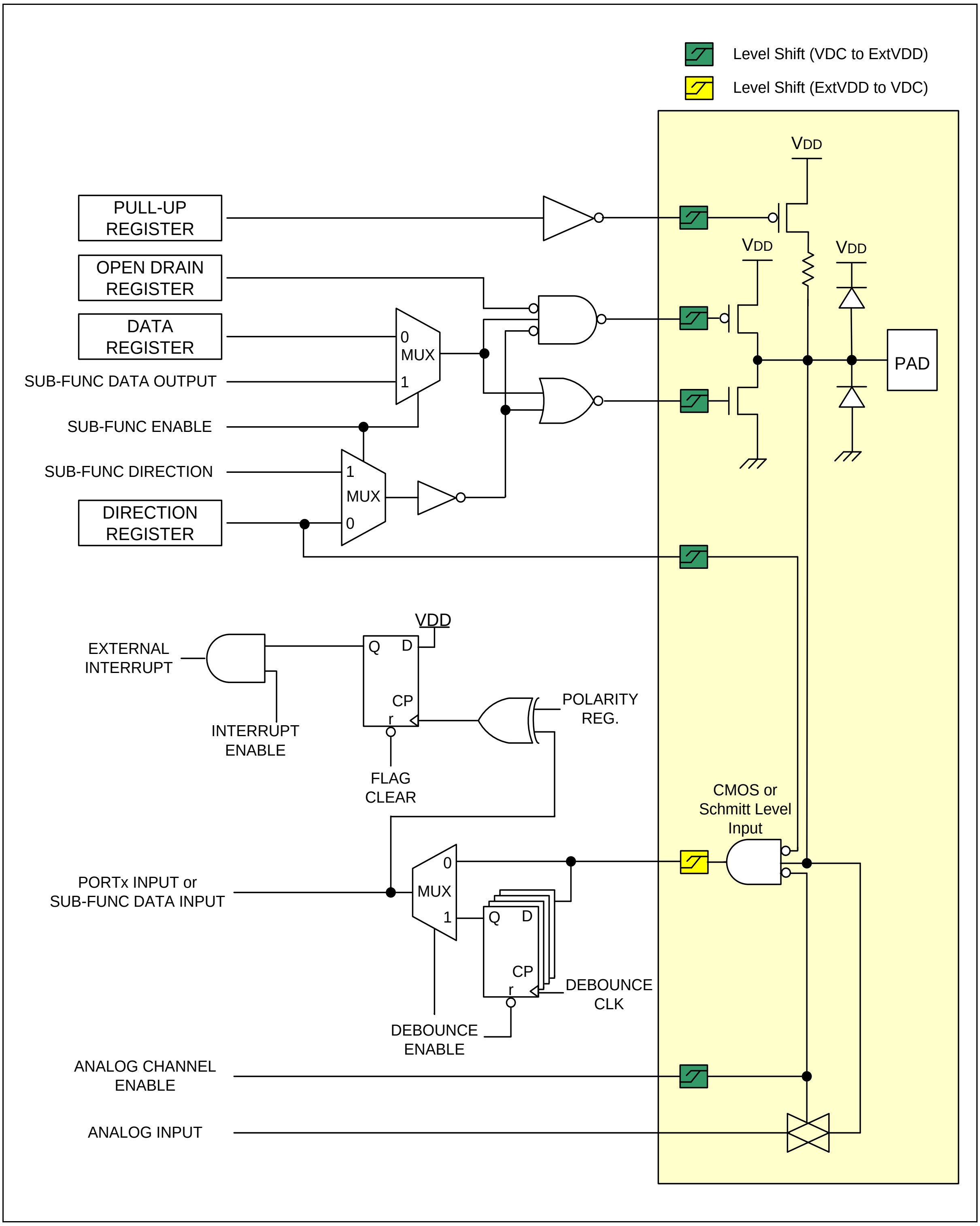


Figure 5. External Interrupt I/O Port Structure

3.3 Logic power port structure

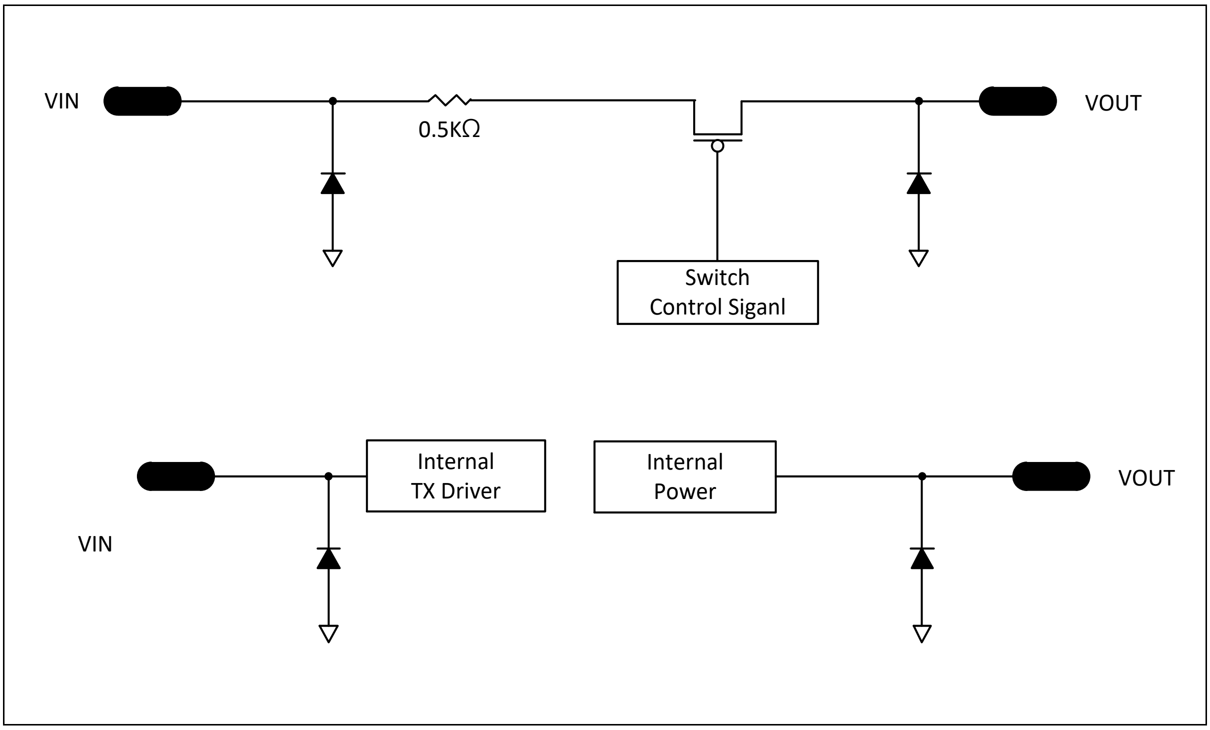


Figure 6. VOUT and VIN Port

4 Memory organization

A96L53x addresses three separate memory spaces:

- Program memory
- Data memory
- XRAM memory

By means of this logical separation of the memory, 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

A96L53x provides 8/16Kbytes of on-chip ISP type Flash program memory, which is readable and writable. Internal data memory (iRAM) is 256bytes and includes the stack area. External data memory (XRAM) is 256/ 768bytes.

4.1 Program memory

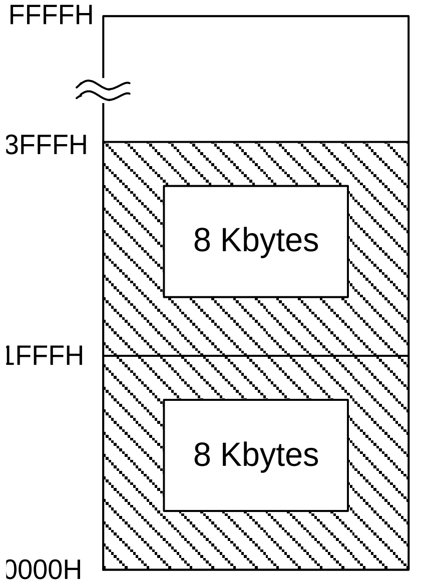
A 16-bit program counter is capable of addressing up to 64Kbytes, and A96L53x has 8/16Kbytes program memory space. After reset, the CPU begins the execution from location 0000H.

Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 1 is assigned to location 000BH. If the external interrupt 1 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory.

If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8byte interval. A longer service routine can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

Figure 7 shows a map of the lower part of the program memory.



NOTE: 8/16Kbytes memory includes Interrupt Vector Region.

Figure 7. Program Memory

The program memory is detailed in 18. Flash memory.

4.2 Internal data memory

Internal data memory is divided into three spaces as shown in Figure 8. Those three spaces are generally called as,

- Lower 128bytes
- Upper 128bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384bytes by using a simple trick. A direct address higher than 7FH accesses one memory space and an indirect address higher than 7FH accesses a different memory space. By means of this method, the upper 128bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in Figure 8.

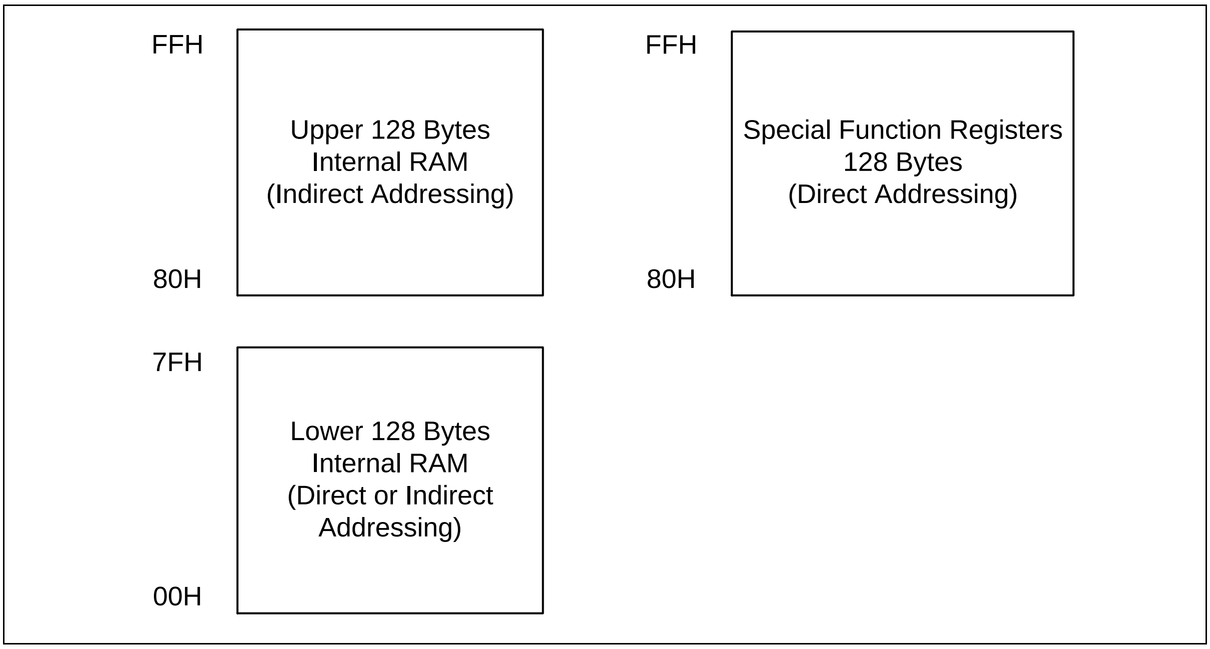
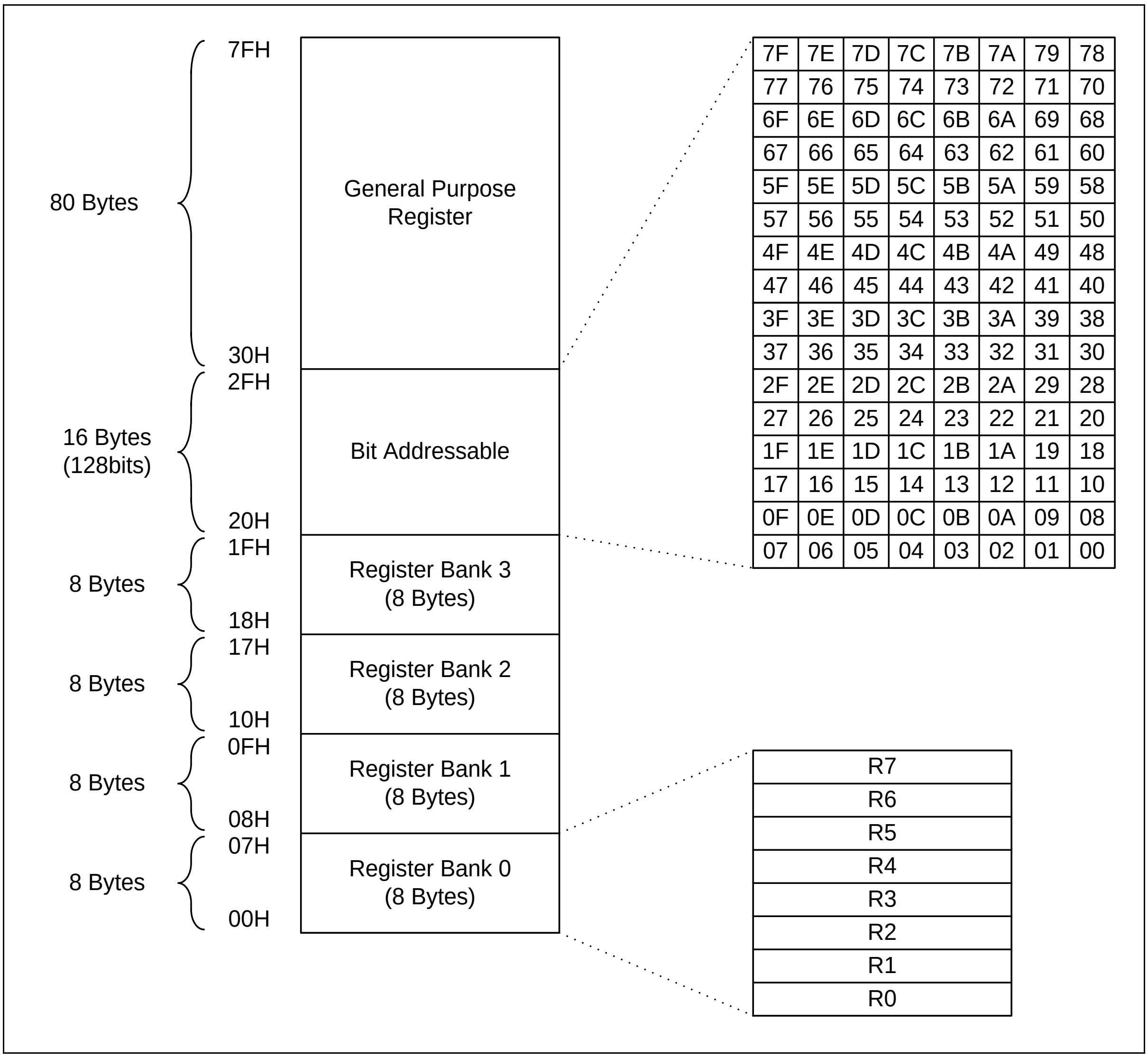


Figure 8. Internal Data Memory Map

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 8. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128bytes can be accessed by either direct or indirect addressing, while the upper 128bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.



7F	7E	7D	7C	7B	7A	79	78
77	76	75	74	73	72	71	70
6F	6E	6D	6C	6B	6A	69	68
67	66	65	64	63	62	61	60
5F	5E	5D	5C	5B	5A	59	58
57	56	55	54	53	52	51	50
4F	4E	4D	4C	4B	4A	49	48
47	46	45	44	43	42	41	40
3F	3E	3D	3C	3B	3A	39	38
37	36	35	34	33	32	31	30
2F	2E	2D	2C	2B	2A	29	28
27	26	25	24	23	22	21	20
1F	1E	1D	1C	1B	1A	19	18
17	16	15	14	13	12	11	10
0F	0E	0D	0C	0B	0A	09	08
07	06	05	04	03	02	01	00

Figure 9. Lower 128bytes Internal RAM

4.3 Extended SFR and data memory area

A96L53x has 256/768bytes XRAM and XSFR registers. Extended SFR area has no relation with RAM nor FLASH. This area can be read or written to using SFR in 8-bit units.

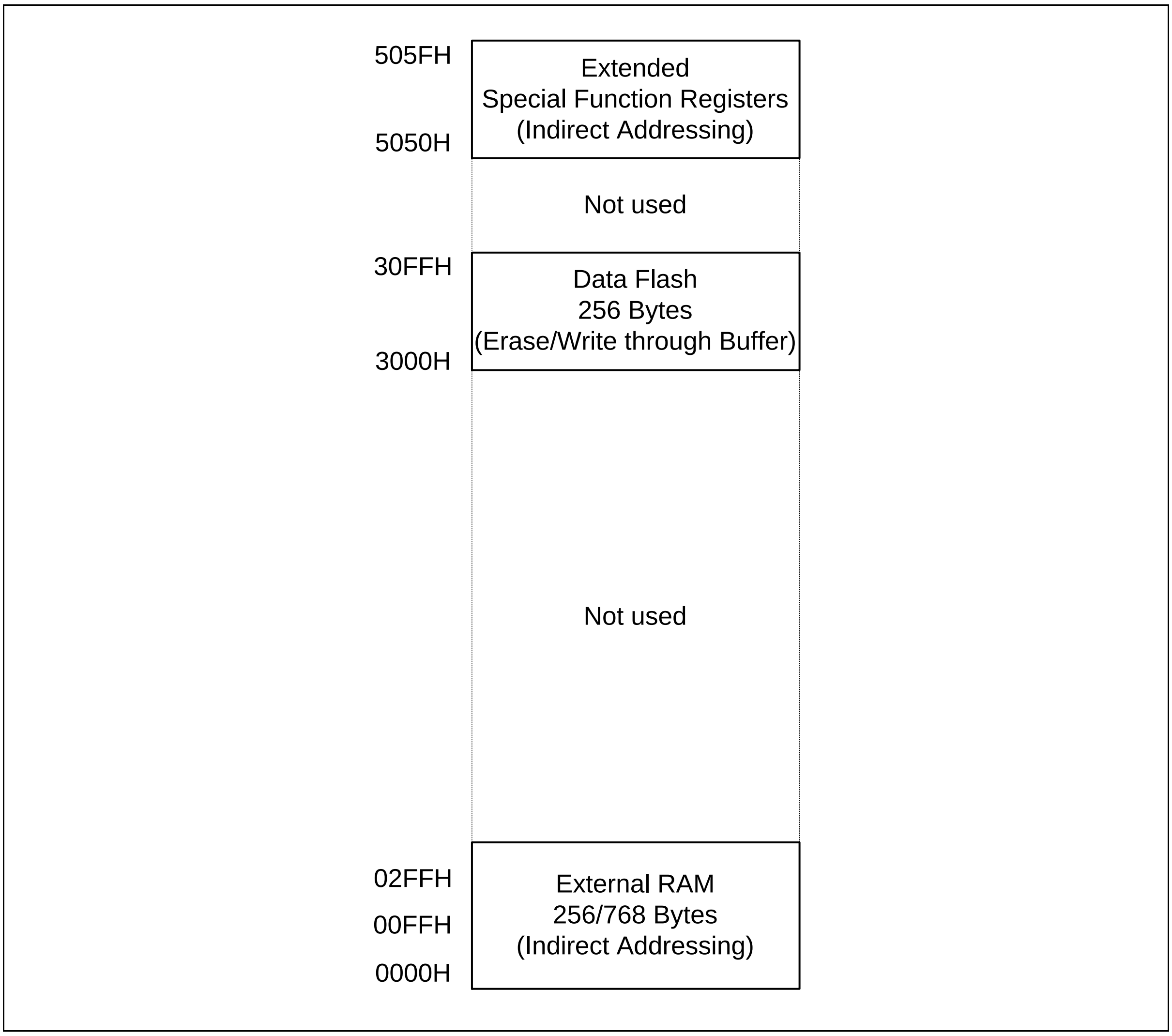


Figure 10. Extended SFR (XSFR) Area

4.4 Data Flash area

Data Flash area has no relation with RAM nor FLASH. This area can be read by using DPTR, and can be erased or written to by using a buffer.

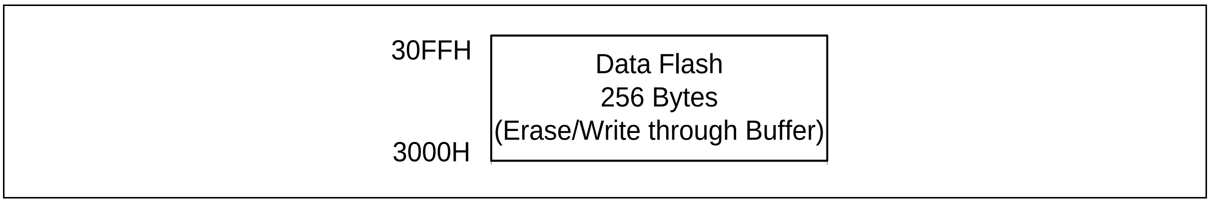


Figure 11. Data Flash Area

Detailed information about Data Flash, please refer to **18. Flash memory**.

4.5 SFR map

In this section, information of SFR map and map summaries are introduced through Table 4 to Table 7.

4.5.1 SFR map summary

Table 4. SFR Map Summary

–	Reserved	▨	M8051 compatible

	00H/8H[NOTE]	**01H/9H**	**02H/0AH**	**03H/0BH**	**04H/0CH**	**05H/0DH**	**06H/0EH**	**07H/0FH**
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	–
0F0H	B	–	DFSADRL	DFSADRH	DFIDR	DFMCR	–	–
0E8H	RSTFR	–	–	–	–	–	–	–
0E0H	ACC	–	ICSCR	ICSDR0	ICSDR1	–	–	–
0D8H	LVRCR	–	USTCR1	USTCR2	USTCR3	USTST	USTBD	USTDR
0D0H	PSW	–	Reserved	Reserved	Reserved	–	–	FCDIN
0C8H	OSCCR	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH	LDOCR	–
0C0H	–	–	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	–	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	–	–	T0CRL	T0CRH	T0ADRL	T0ADRH	T0BDRL	T0BDRH
0A8H	IE	IE1	IE2	IE3	–	CHPCR	AMPCR0	AMPCR1
0A0H	EIFLAG	Reserved	EO	–	EIPOL0	EIPOL1	–	–
98H	–	P1IO	P1OD	P1PU	P1FSRL	P1FSRH	P12DB	IRCIDR
90H	Reserved	P0IO	P0OD	P0PU	P0FSRL	P0FSRH	P0DB	IRCTRM
88H	P1	–	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	IRCTCR
80H	P0	SP	DPL	DPH	DPL1	DPH1	–	PCON

NOTE: Registers 00H/8H are bit-addressable.

4.5.2 Extended SFR map summary

Table 5. XSFR Map Summary

–	Reserved

	00H/8H	**01H/9H**	**02H/0AH**	**03H/0BH**	**04H/0CH**	**05H/0DH**	**06H/0EH**	**07H/0FH**
5058H	FCDRL	–	–	–	–	–	–	LVRIDR
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH

NOTE: Registers 00H/8H are bit-addressable.

4.5.3 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reserved	–	–	–							
87H	Power Control Register	PCON	R/W	–	–	–	–	–	–	0	0
88H	P1 Data Register	P1	R/W	–	–	0	0	0	0	0	0
89H	Reserved	–	–	–							
8AH	System and Clock Control Register	SCCR	R	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	0	0	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watchdog Timer Control Register	WDTCR	R/W	0	0	0	–	–	0	0	0
8EH	Watchdog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
8EH	Watchdog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	Internal RC Trim Control Register	IRCTCR	R/W	0	0	0	0	0	0	0	0
90H	Reserved	–	R/W	–	–	–	–	0	0	0	0
91H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
92H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
93H	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
94H	Port 0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
95H	Port 0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
96H	P0 Debounce Enable Register	P0DB	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	**Function**	**Symbol**	**R/W**	**@ Reset**							
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
97H	Internal RC Trim Register	IRCTRM	R/W	x	x	x	x	x	x	x	x
98H	Reserved	–	–	–							
99H	P1 Direction Register	P1IO	R/W	–	–	0	0	0	0	0	0
9AH	P1 Open-drain Selection Register	P1OD	R/W	–	–	0	0	0	0	0	0
9BH	P1 Pull-up Resistor Selection Register	P1PU	R/W	–	–	0	0	0	0	0	0
9CH	Port 1 Function Selection Low Register	P1FSRL	R/W	–	0	–	0	–	0	–	0
9DH	Port 1 Function Selection High Register	P1FSRH	R/W	–	–	–	–	0	0	0	0
9EH	P1 Debounce Enable Register	P1DB	R/W	–	–	0	0	–	0	0	0
9FH	Internal RC Trim Identification Register	IRCIDR	R/W	0	0	0	0	0	0	0	0
A0H	External Interrupt Flag Register	EIFLAG	R/W	0	0	0	0	0	0	0	0
A1H	Reserved	–	R/W	–	–	–	–	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–							
A4H	External Interrupt Polarity 0 Register	EIPOL0	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 1 Register	EIPOL1	R/W	–	–	0	0	0	0	0	0
A6H	Reserved	–	–	–							
A7H	Reserved	–	–	–							
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	–	–	–	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	–	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	–	0	0	–	–	–
ACH	Reserved	–	–	–							
ADH	Chopper Control Register	CHPCR	R/W	–	–	–	–	–	–	0	0
AEH	OP-AMP Control Register 0	AMPCR0	R/W	–	0	–	–	–	–	0	0
AFH	OP-AMP Control Register 1	AMPCR1	R/W	0	0	0	0	0	–	0	0
B0H	Reserved	–	–	–							
B1H	Reserved	–	–	–							
B2H	Timer 0 Control Low Register	T0CRL	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
B3H	Timer 0 Control High Register	T0CRH	R/W	0	–	0	0	–	–	–	0
B4H	Timer 0 A Data Low Register	T0ADRL	R/W	1	1	1	1	1	1	1	1
B5H	Timer 0 A Data High Register	T0ADRH	R/W	1	1	1	1	1	1	1	1
B6H	Timer 0 B Data Low Register	T0BDRL	R/W	1	1	1	1	1	1	1	1
B7H	Timer 0 B Data High Register	T0BDRH	R/W	1	1	1	1	1	1	1	1
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	Reserved	–	–	–							
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	0	0	0	0
BBH	Timer 1 Control High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1
C0H	Reserved	–	–	–							
C1H	Reserved	–	–	–							
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	0	0	0	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	0	–	–	0	1	0	–	–
C9H	Reserved	–	–	–							
CAH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
CBH	A/D Converter Control High Register	ADCCRH	R/W	0	–	–	–	0	0	0	0
CCH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
CDH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x
CEH	LDO Control Register	LDOCR	R/W	–	–	–	–	–	–	–	0
CFH	Reserved	–	–	–							
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							
D2H	Reserved	–	R/W	–	–	–	–	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D3H	Reserved	–	R/W	–	–	–	–	0	0	0	0
D4H	Reserved	–	R/W	0	0	0	0	0	0	0	0
D5H	Reserved	–	–	–							
D6H	Reserved	–	–	–							
D7H	Flash CRC Data In Register	FCDIN	R/W	0	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	0	–	–	–	–	0	0	0
D9H	Reserved	–	–	–							
DAH	USART Control Register 1	USTCR1	R/W	0	0	0	0	0	0	0	0
DBH	USART Control Register 2	USTCR2	R/W	0	0	0	0	0	0	0	0
DCH	USART Control Register 3	USTCR3	R/W	0	0	0	0	0	0	0	0
DDH	USART Status Register	USTST	R/W	1	0	0	0	0	0	0	0
DEH	USART Baud Rate Generation Register	USTBD	R/W	1	1	1	1	1	1	1	1
DFH	USART Data Register	USTDR	R/W	0	0	0	0	0	0	0	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Reserved	–	–	–							
E2H	Constant Sink Current Control Register	ICSCR	R/W	–	–	–	–	0	0	0	0
E3H	Constant Sink Current Data Register 0	ICSDR0	R/W	–	–	–	–	0	0	0	0
E4H	Constant Sink Current Data Register 1	ICSDR1	R/W	–	–	–	–	0	0	0	0
E5H	Reserved	–	–	–							
E6H	Reserved	–	–	–							
E7H	Reserved	–	–	–							
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–

Table 6. SFR Map (continued)

Address	**Function**	**Symbol**	**R/W**	**@ Reset**							
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F2H	Data Flash Sector Address Low Register	DFSADRL	R/W	0	0	0	–	–	–	–	–
F3H	Data Flash Sector Address High Register	DFSADRH	R/W	0	0	0	0	0	0	0	0
F4H	Data Flash Identification Register	DFIDR	R/W	0	0	0	0	0	0	0	0
F5H	Data Flash Mode Control Register	DFMCR	R/W	0	–	–	–	–	0	0	0
F6H	Reserved	–	–	–							
F7H	Reserved	–	–	–							
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Flash Sector Address High Register	FSADRH	R/W	–	–	–	–	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	–	–	–	–	0	0	0
FFH	Reserved	–	–	–							

4.5.4 Extended SFR map

Table 7. XSFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
5050H	Flash CRC Start Address High Register	FCSARH	R/W	–	–	–	–	–	–	–	0
5051H	Flash CRC End Address High Register	FCEARH	R/W	–	–	–	–	–	–	–	0
5052H	Flash CRC Start Address Middle Register	FCSARM	R/W	0	0	0	0	0	0	0	0
5053H	Flash CRC End Address Middle Register	FCEARM	R/W	0	0	0	0	0	0	0	0
5054H	Flash CRC Start Address Low Register	FCSARL	R/W	0	0	0	0	–	–	–	–
5055H	Flash CRC End Address Low Register	FCEARL	R/W	0	0	0	0	1	1	1	1
5056H	Flash CRC Control Register	FCCR	R/W	0	0	0	–	0	0	0	0
5057H	Flash CRC Data High Register	FCDRH	R	1	1	1	1	1	1	1	1
5058H	Flash CRC Data Low Register	FCDRL	R	1	1	1	1	1	1	1	1
- -											
505FH	LVR Write Identification Register	LVRIDR	R/W	0	0	0	0	0	0	0	0

5 Ports

5.1 I/O ports

A96L53x has two groups of I/O ports, P0 and P1. Each port can be easily configured as an input pin, an output, or an internal pull up and open-drain pin by software. The port configuration pursues to meet various system configurations and design requirements. P0 and P1 have a function generating interrupts in accordance with a change of state of the pin.

5.2 Port P0

5.2.1 Port description of P0

As an 8-bit I/O port, P0 controls the following registers:

- P0 data register (P0)
- P0 direction register (P0IO)
- P0 debounce enable register (P0DB)
- P0 pull-up resistor selection register (P0PU)
- P0 open-drain selection register (P0OD)
- P0 Function selection registers (P0FSRH/P0FSRL)

5.3 Port P1

5.3.1 Port description of P1

As a 6-bit I/O port, P1 controls the following registers:

- P1 data register (P1)
- P1 direction register (P1IO)
- P1 pull-up resistor selection register (P1PU)
- P1 debounce enable register (P1DB)
- P1 open-drain selection register (P1OD)
- P1 Function selection registers (P1FSRH/P1FSRL)

Caution

P11 and P14 pins do not exist outside the package. Be careful in setting because they are internally connected to Logic's RXT PAD and TXR PAD. After reset, it is recommended to set P11 as input and P14 as output low. If there is no separate line interface communication, set P14 as output low.

6 Interrupt controller

Up to 13 interrupt sources are available in A96L53x. Allowing software control, each interrupt source can be enabled by defining separate enable register bit associated with it. In addition, it has four levels of priority, and specially, the non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources and cannot be controlled by software.

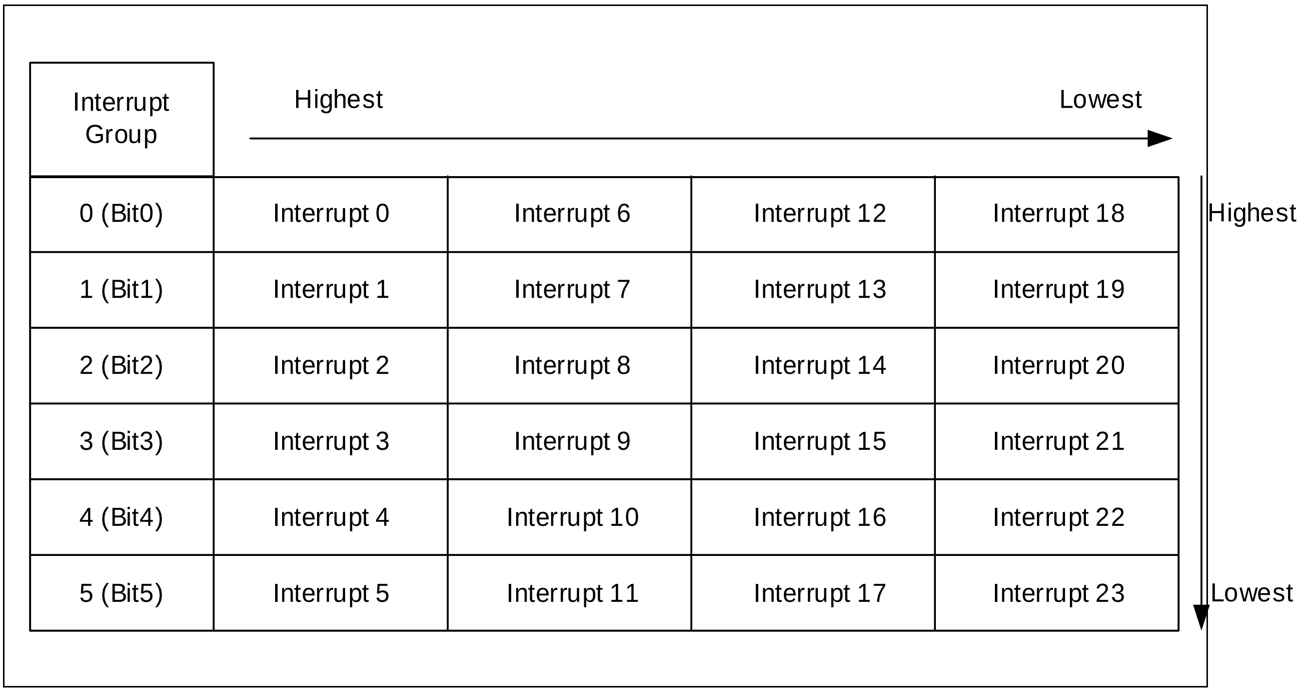
The interrupt controller features the followings:

- Receives the requests from 13 interrupt sources.
- 6 group priority
- 4 priority levels
- Multi interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit.
- Interrupt latency can range from 3 to 9 machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupt enable registers (IE, IE1, IE2, IE3). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control. The EA bit must be set to ‘1’ to enable interrupts as introduced in the followings:

- When the EA is set to ‘0’ ➔ All interrupts are disabled.
- When the EA is set to ‘1’ ➔ A particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

The EA is always cleared to ‘0’ when jumping to an interrupt service vector, and set to ‘1’ when executing the [RETI] instruction. A96L53x supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of the four levels according to the IP and IP1 registers.



Interrupt Group				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23

Figure 12. Interrupt Group Priority Level

Figure 12 introduces interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by 2 bits of the Interrupt Priority (IP) registers: 1 bit from the IP register and another 1 bit from the IP1 register.

Interrupt Service Routine serves the interrupt that has higher priority first. If two requests of different priority levels are received simultaneously, the request with higher priority level is served prior to the lower one.

6.1 External interrupt

External interrupts on pins INT0 to INT10 receive various interrupt requests in accordance with the external interrupt polarity 0 register (EIPOL0) and external interrupt polarity 1 register (EIPOL1) as shown in Figure 13.

Each external interrupt source has a corresponding enable/disable bit. The external interrupt flag register (EIFLAG) provides the status information of the external interrupts.

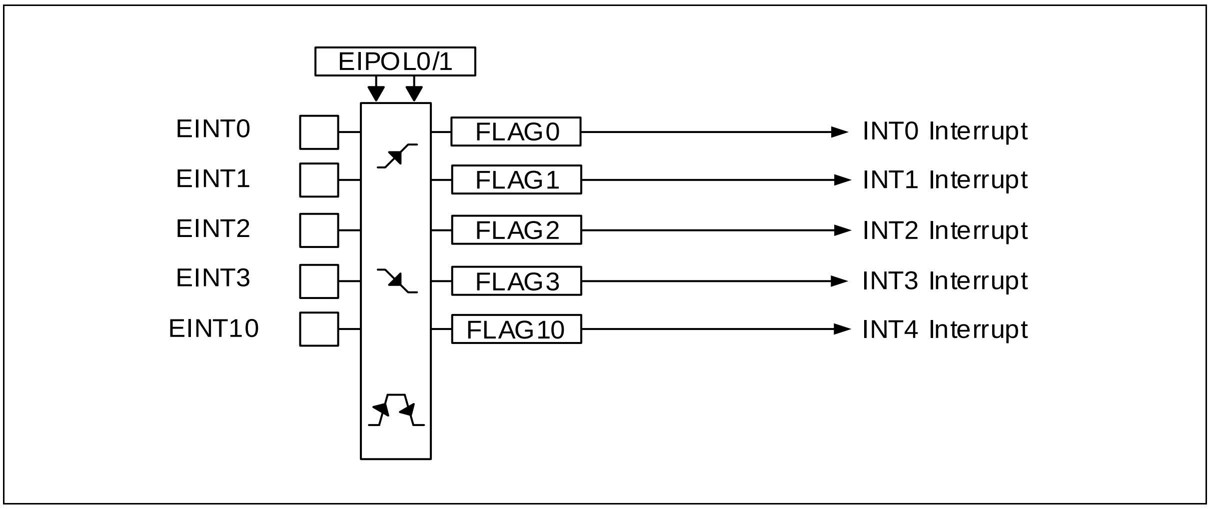


Figure 13. External Interrupt Description

6.2 Block diagram

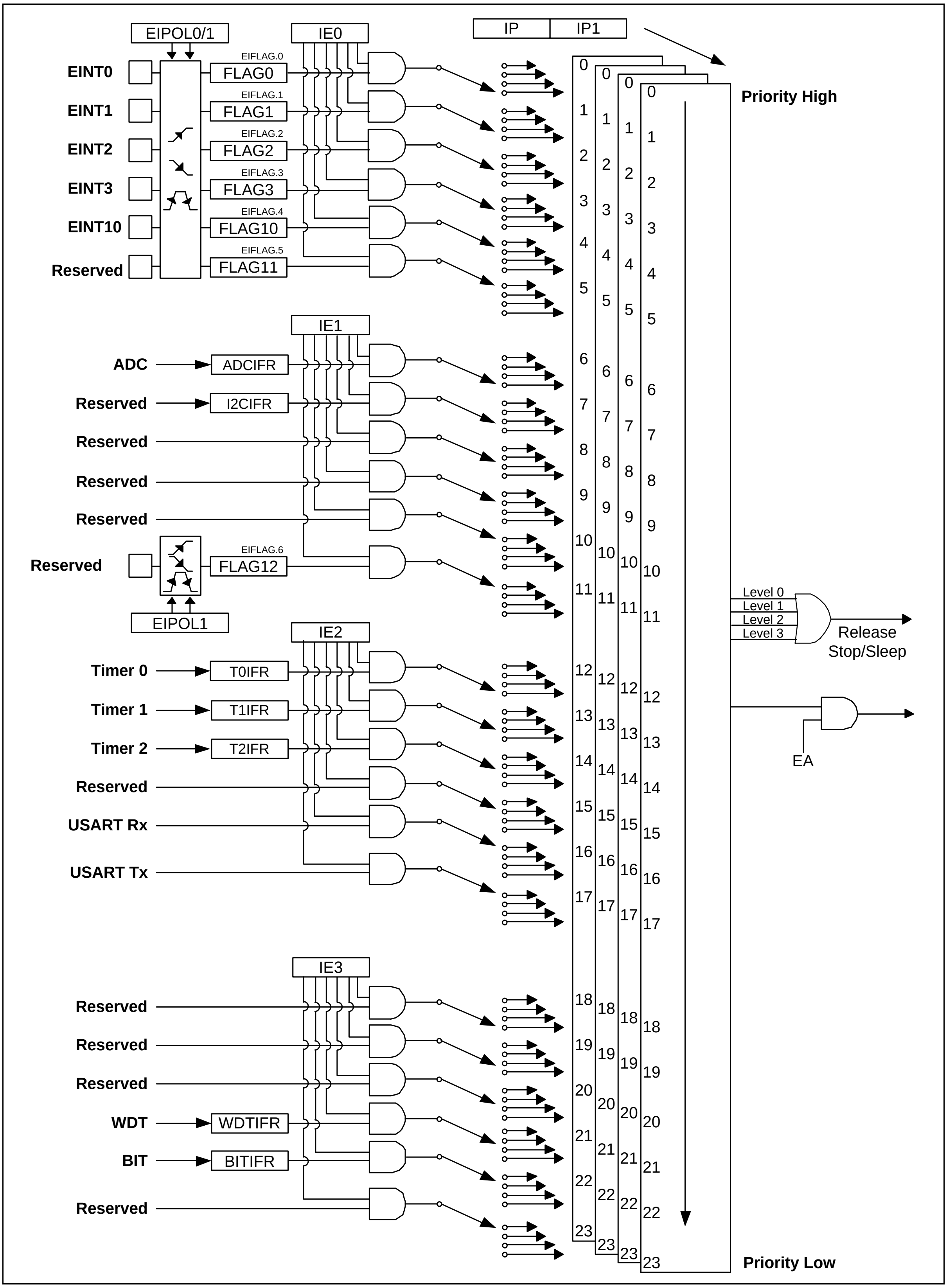


Figure 14. Interrupt Controller Block Diagram

A release signal for STOP mode and IDLE mode can be generated by all interrupt sources which are enabled without reference to priority level. An interrupt request is delayed while data is written to one of the registers IE, IE1, IE2, IE3, IP, IP1, and PCON.

6.3 Interrupt vector table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack, and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address.

Interrupt controller supports 13 interrupt sources and each interrupt source has a determined priority order as shown in Table 8.

Table 8. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector address
Hardware RESET	RESETB	-	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
External Interrupt 2	INT2	IE.2	3	Maskable	0013H
External Interrupt 3	INT3	IE.3	4	Maskable	001BH
External Interrupt 10	INT4	IE.4	5	Maskable	0023H
-	INT5	IE.5	6	Maskable	002BH
ADC Interrupt	INT6	IE1.0	7	Maskable	0033H
-	INT7	IE1.1	8	Maskable	003BH
–	INT8	IE1.2	9	Maskable	0043H
–	INT9	IE1.3	10	Maskable	004BH
–	INT10	IE1.4	11	Maskable	0053H
-	INT11	IE1.5	12	Maskable	005BH
T0 Interrupt	INT12	IE2.0	13	Maskable	0063H
T1 Interrupt	INT13	IE2.1	14	Maskable	006BH
T2 Interrupt	INT14	IE2.2	15	Maskable	0073H
–	INT15	IE2.3	16	Maskable	007BH
USART Rx Interrupt	INT16	IE2.4	17	Maskable	0083H
USART Tx Interrupt	INT17	IE2.5	18	Maskable	008BH
–	INT18	IE3.0	19	Maskable	0093H
–	INT19	IE3.1	20	Maskable	009BH
–	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
–	INT23	IE3.5	24	Maskable	00BBH

To execute the maskable interrupts, both EA bit and the corresponding IEx bit associated with a specific interrupt source must be set to ‘1’. When an interrupt request is received, a particular interrupt request flag is set to ‘1’ and maintains its status until CPU accepts the interrupt. After the interrupt acceptance, the interrupt request flag is cleared automatically.

7 Clock generator

As shown in Figure 15, a clock generator produces basic clock pulses which provide a CPU and peripherals with a system clock.

A default system clock is a 1MHz HF INT-RC Oscillator and default division rate is four. To stabilize system internally, the 1MHz HF INT-RC Oscillator is used on POR.

A96L53x has three types of oscillators:

- Calibrated HF Internal RC Oscillator (4MHz)
  - HF INT-RC OSC/8 (0.5MHz)
  - HF INT-RC OSC/4 (1MHz, default system clock)
  - HF INT-RC OSC/2 (2MHz)
  - HF INT-RC OSC/1 (4MHz)
- Internal WDTRC Oscillator (1KHz)
- LF INT-RC Oscillator(32KHz)

7.1 Block diagram

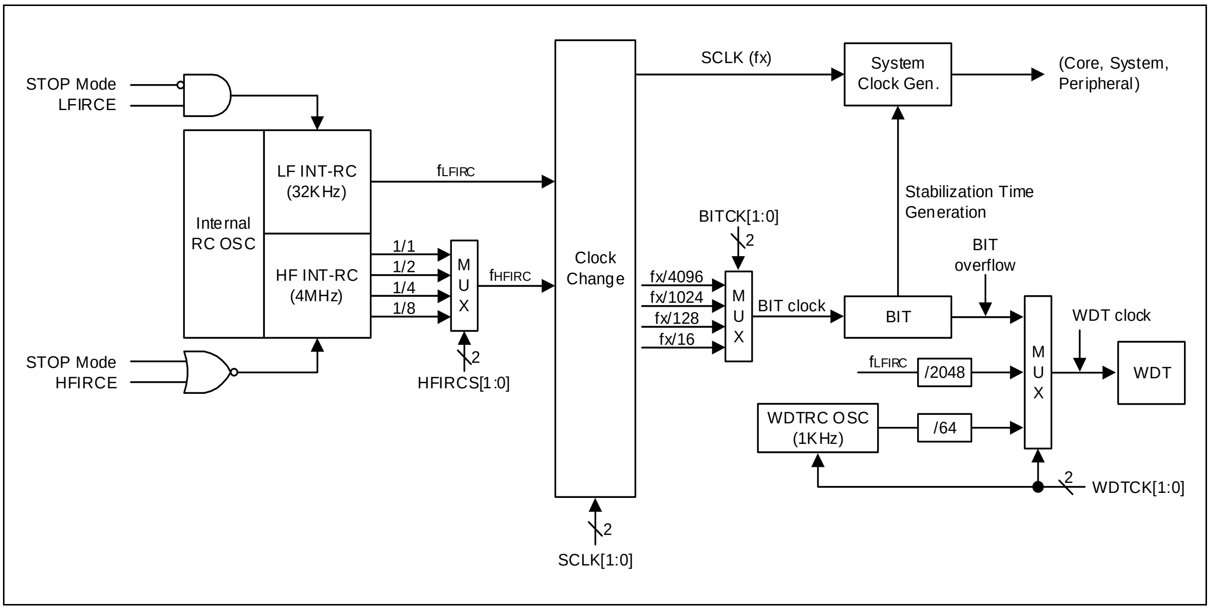


Figure 15. Clock Generator in Block Diagram

8 Basic Interval Timer (BIT)

A96L53x has a free running 8-bit Basic Interval Timer (BIT). The BIT generates a time base for Watchdog Timer counting, and provides the Basic Interval Timer Interrupt (BITIFR).

The BIT of A96L53x features the followings:

- During Power On, the BIT gives a stable clock generation time.
- On exiting Stop mode, the BIT gives a stable clock generation time.
- As a timer, the BIT generates a timer interrupt.

8.1 Block diagram

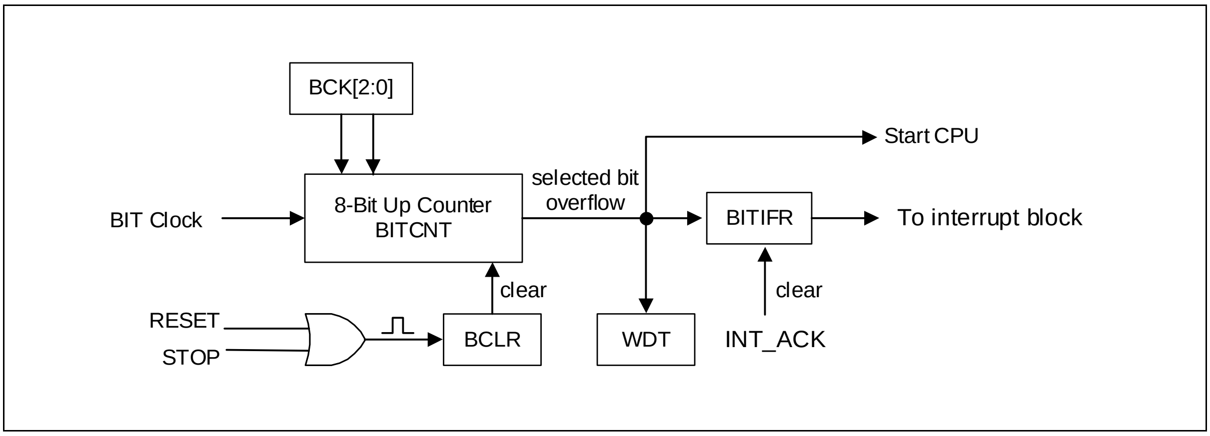


Figure 16. Basic Interval Timer in Block Diagram

9 Watchdog Timer (WDT)

Watchdog Timer (WDT) is used to rapidly detect the CPU malfunctions such as endless looping caused by noise. In addition, it is used to resume the CPU in a normal state.

The Watchdog Timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the Watchdog Timer is not being used for the detection of the CPU malfunctions, it can be used as a timer generating an interrupt at fixed intervals.

The Watchdog Timer can be used in a free running 8-bit timer mode or in a Watchdog Timer mode by setting the WDTRSON bit, which is the 5th bit of the WDTCR register (WDTCR[5]). If the WDTCR[5] is set to ‘1’, the Watchdog Timer counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to ‘0’ automatically.

The Watchdog Timer consists of an 8-bit binary counter and a Watchdog Timer data register. When value of the 8-bit binary counter is equal to the 8 bits of the WDTCNT register, an interrupt request flag is generated. This can be used as a Watchdog Timer interrupt or a reset of the CPU in accordance with the WDTRSON bit.

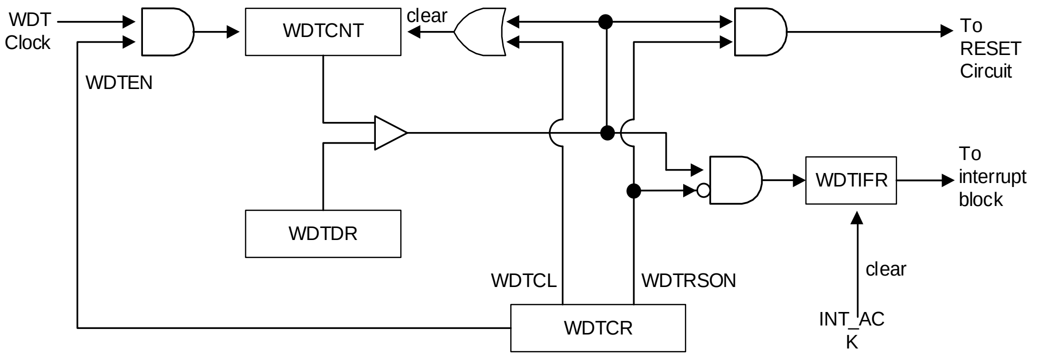
The input clock sources of the Watchdog Timer are BIT overflow, LFIRC, and WDTRC. Interval of the Watchdog Timer interrupt is decided by the BIT overflow period and WDTDR set value. The WDT interrupt interval is derived from the following calculations:

$$\text{WDT Interrupt Interval} = (\text{BIT Interrupt Interval}) \text{ X } (\text{WDTDR Value}+1)$$

$$\text{WDT Interrupt Interval} = 2048/f_{LFIRC} \text{ x } (\text{WDTDR Value}+1) \text{ when LFIRC}$$

$$\text{WDT Interrupt Interval} = 64/f_{WDTRC} \text{ x } (\text{WDTDR Value}+1) \text{ when WDTRC}$$

9.1 Block diagram



NOTE: Watchdog Timer clock depends on the WDTCK bit in the WDTCR register.

Figure 17. Watchdog Timer in Block Diagram

10 TIMER 0/1/2

16-bit TIMER 0/1/2 have a multiplexer and six registers such as Timer 0/1/2A Data Register High/Low, Timer 0/1/2B Data Register High/Low, and Timer 0/1/2 Control Register High/Low (TnADRH, TnADRL, TnBDRH, TnBDRL, TnCRH, and TnCRL).

The TIMER 0/1/2 operate in one of four operating modes shown in the followings:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into the input capture data registers (TnBDRH/TnBDRL) by the EINT10/EINT11/EINT12. The TIMER 0/1/2 output a comparison result of the counter and data register through TnO port in timer/counter mode. (The TIMER 0/1/2 output PWM wave form through PWMnO port in PPG mode).

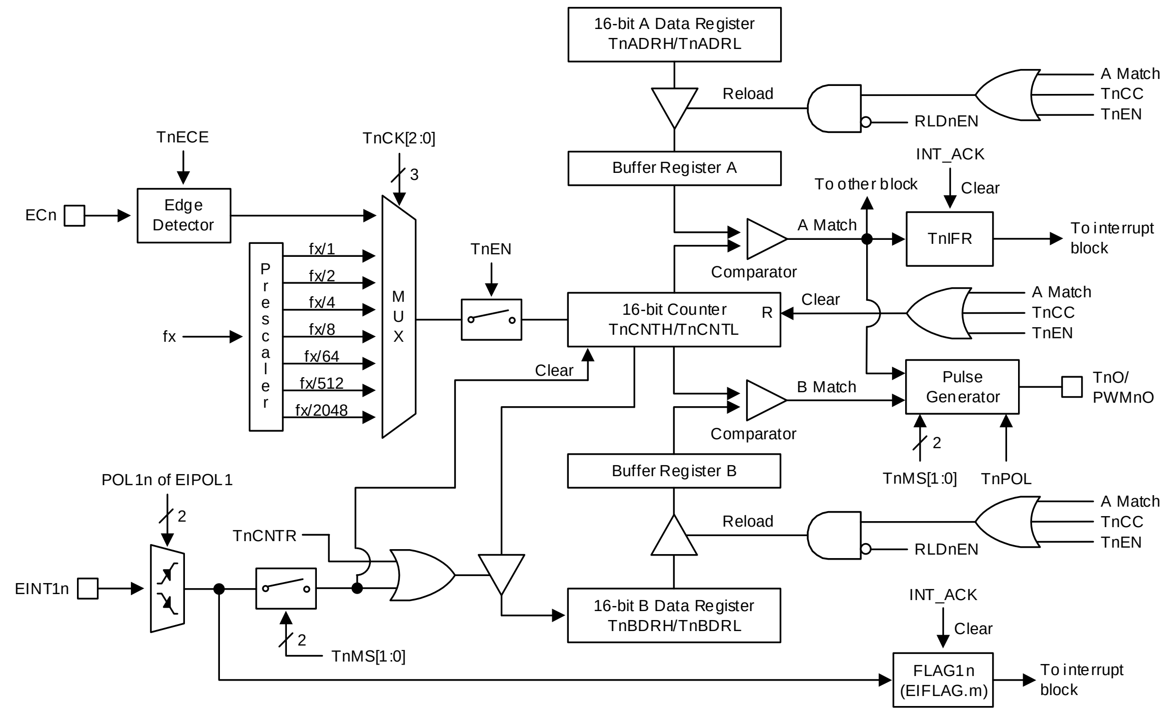
A timer/counter 0/1/2 uses an internal clock or an external clock (ECn) as an input clock source. The clock sources are introduced below, and one is selected by the clock selection logic which is controlled by the clock selection bits (TnCK[2:0]).

Timer 0/1/2 clock sources: f_X/1, 2, 4, 8, 64, 512, 2048 and ECn

Table 9. TIMER 0/1/2 Operating Modes

TnEN	P1FSRL[2](T0)/ P1FSRH[1:0](T1)	TnMS[1:0]	TnCK[2:0]	Timer n
1	1/01/01	00	XXX	16 Bit Timer/Counter Mode
1	0/00/00	01	XXX	16 Bit Capture Mode
1	1/01/01	10	XXX	16 Bit PPG Mode(one-shot mode)
1	1/01/01	11	XXX	16 Bit PPG Mode(repeat mode)

10.1 Block diagram



NOTES:

1. The TnEN bit is automatically cleared to logic ‘0’ after one pulse is generated in PPG one-shot mode.
2. The RLDnEN bit must be ‘0b’ when the TnEN bit is changed from ‘0b’ to ‘1b’.

Figure 18. 16-bit Timer n in Block Diagram (n = 0, 1, and 2/ m=4, 5, and 6)

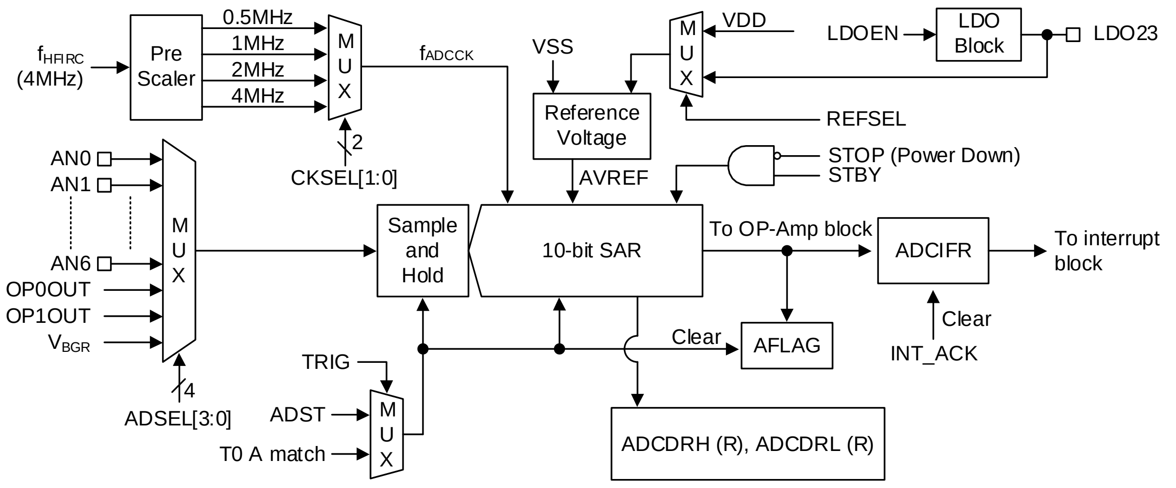
11 10-bit A/D Converter (ADC)

Analog-to-Digital (A/D) Converter allows conversion of an analog input signal to a corresponding 10-bit digital output. The A/D module has 9 analog inputs, and the output of the multiplexer becomes the input into the converter, which generates a result via successive approximation.

The A/D module has four registers as listed below. Each register can be selected for the corresponding channel by setting the ADSEL[3:0]. When the conversion is complete, the ADCDRH and ADCDRL registers contain the results of the conversion, the conversion status bit AFLAG is set to ‘1’, and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as ‘0’.

- A/D converter control high register (ADCCRH)
- A/D converter control low register (ADCCRL)
- A/D converter data high register (ADCDRH)
- A/D converter data low register (ADCDRL)
- LDO control register (LDOCR)

11.1 Block diagram



NOTES:

1. The conversion clock is 14-clock including ADC sample and hold.
2. For ADC sample/hold and conversion, at least 8usec is required.
3. When the LDO is enabled, a 0.1uF capacitor should be connected between LDO23 pin and VSS.
4. The LDO should only be used as the reference voltage of A/D Converter and OP-AMP.

Figure 19. 10-bit ADC Block Diagram

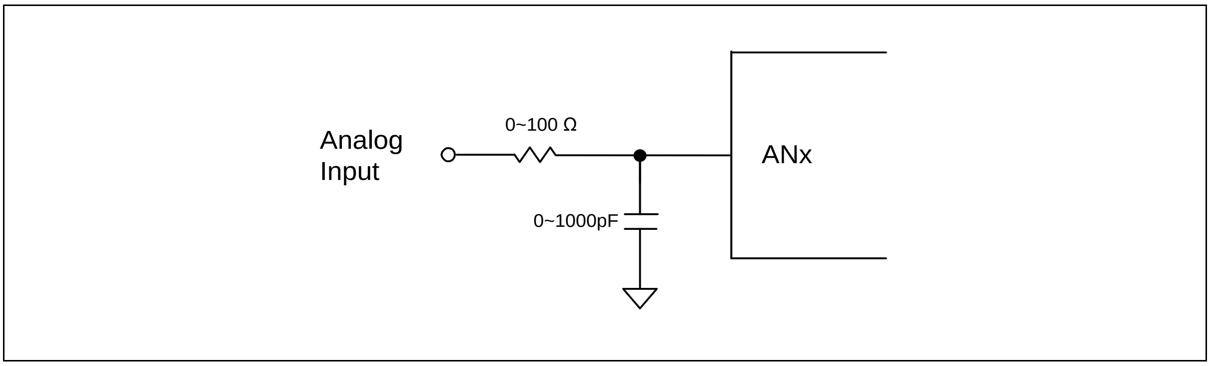


Figure 20. AD Analog Input Pin with Capacitor

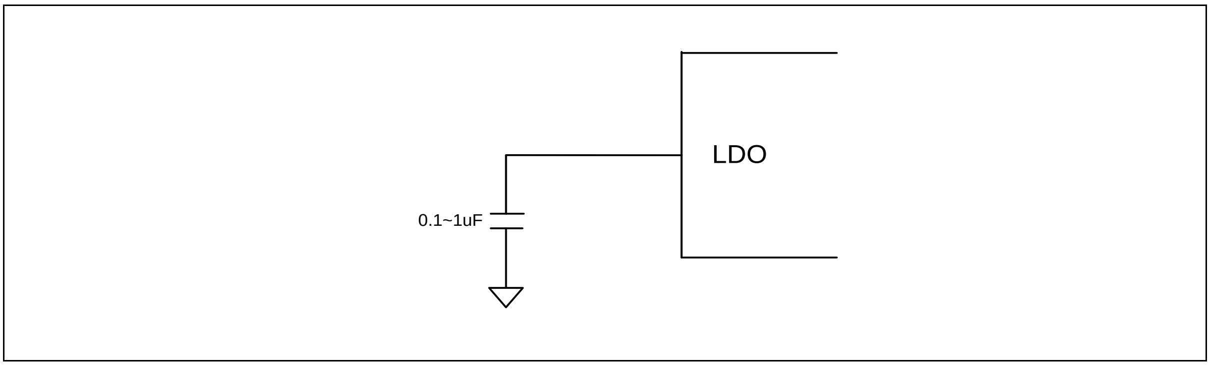
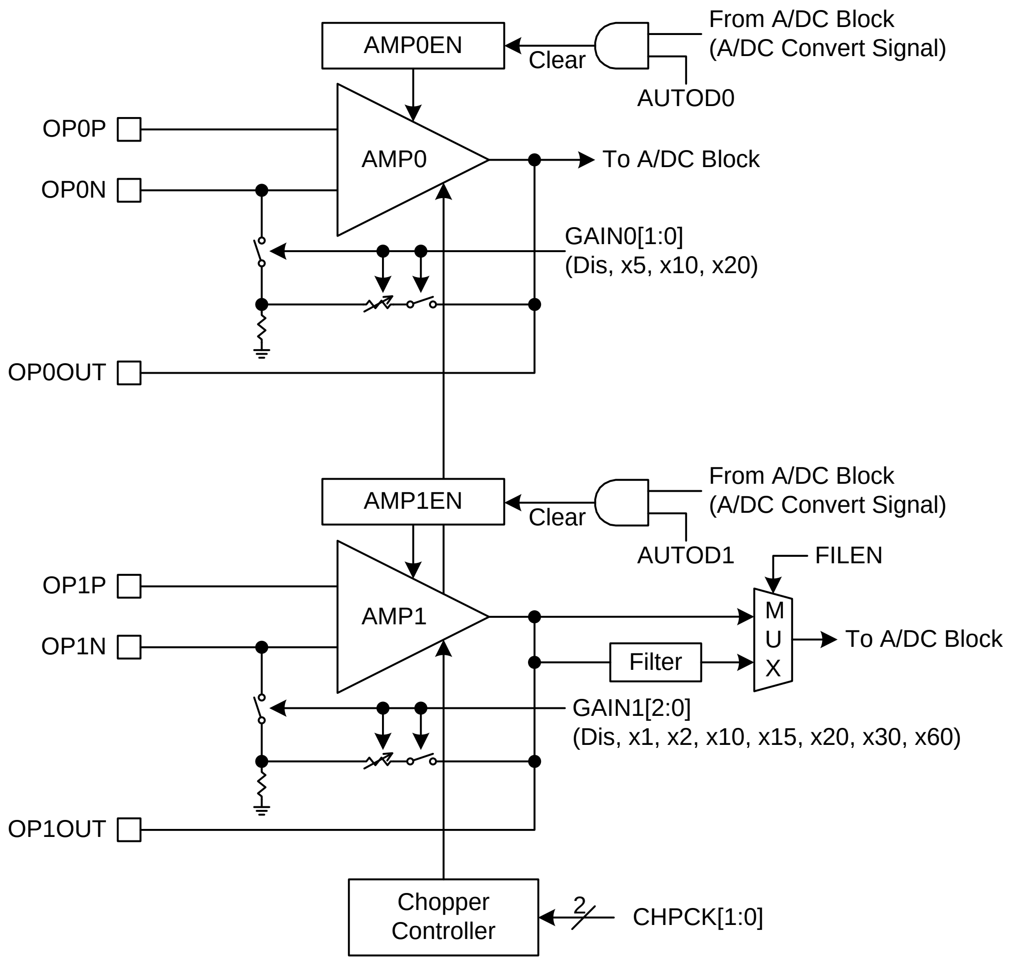


Figure 21. LDO23 Pin with Capacitor

12 Operational Amplifier (OP-AMP)

A96L53x offers two channels of an operational amplifier (OP-AMP). The OP-AMP consists of three registers such as OP-AMP Control Register 0 (AMPCR0), OP-AMP Control Register 1 (AMPCR1), and Chopper Control Register (CHPCR).

12.1 Block diagram



NOTE: Feedback resistors for gain on each Amp are disconnected during one or more Amp and gain are disabled.

Figure 22. OP AMP Block Diagram

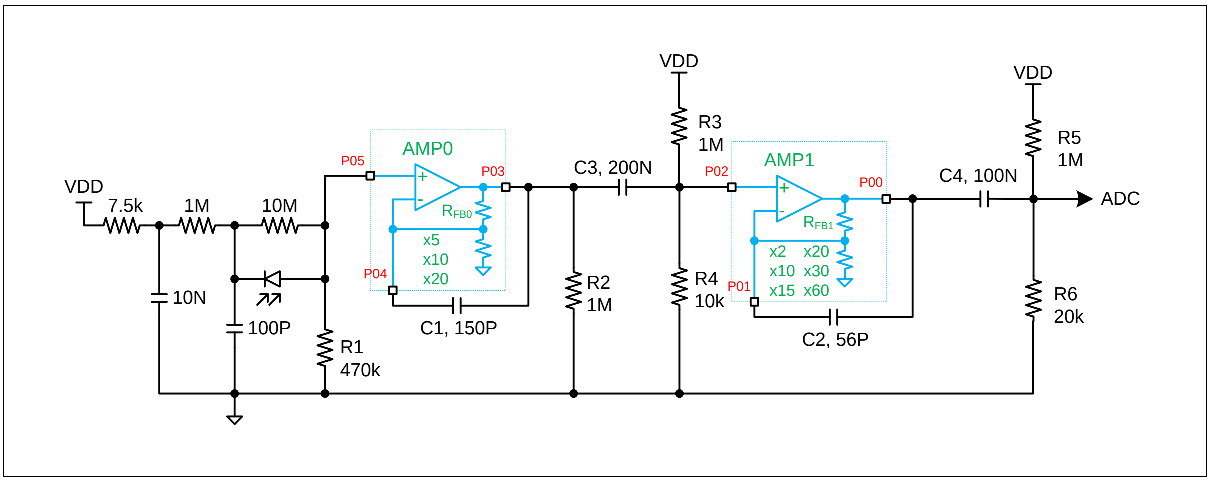


Figure 23. Recommend Circuit for Internal Gain

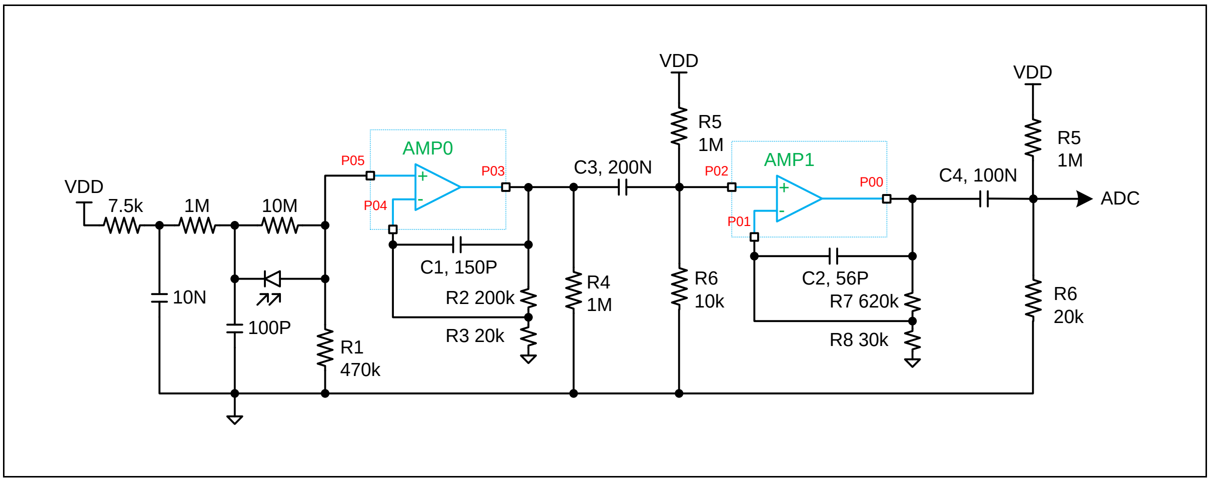


Figure 24. Recommend Circuit for External Gain

13 USART

USART (Universal Synchronous/Asynchronous Receiver/Transmitter) is a microchip that facilitates communication through a computer’s serial port using RS-232C protocol. A96L53x incorporates a USART function block inside. The USART function block consists of USART Control Register1/2/3/4, USART Status Register, USART Baud-Rate Generation Register and USART Data Register.

The USART has three operating modes as listed below, and the operating mode is selected by the USTMS[1:0]:

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode

13.1 USART UART mode

Universal Asynchronous serial Receiver and Transmitter (UART) is a highly flexible serial communication device. Its main features are listed below:

- Full duplex operation (Independent Serial Receive and Transmit Registers)
- Baud rate generator
- Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits.
- Odd or even parity generation and parity check supported by hardware.
- Data overrun detection
- Framing error detection
- Three separate interrupts on TX complete, TX data register empty and RX complete

The UART has a baud rate generator, a transmitter and a receiver: The baud rate generator is used for asynchronous operation. The transmitter consists of a single write buffer, a serial shift register, parity generator and control logic, and is used for handling different serial frame formats. The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module because of its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition, the receiver has a parity checker, a shift register, a two-level receive FIFO (USTDR) and control logic. The receiver supports identical frame formats to the transmitter’s and can detect frame errors, data overrun and parity errors.

13.2 UART block diagram

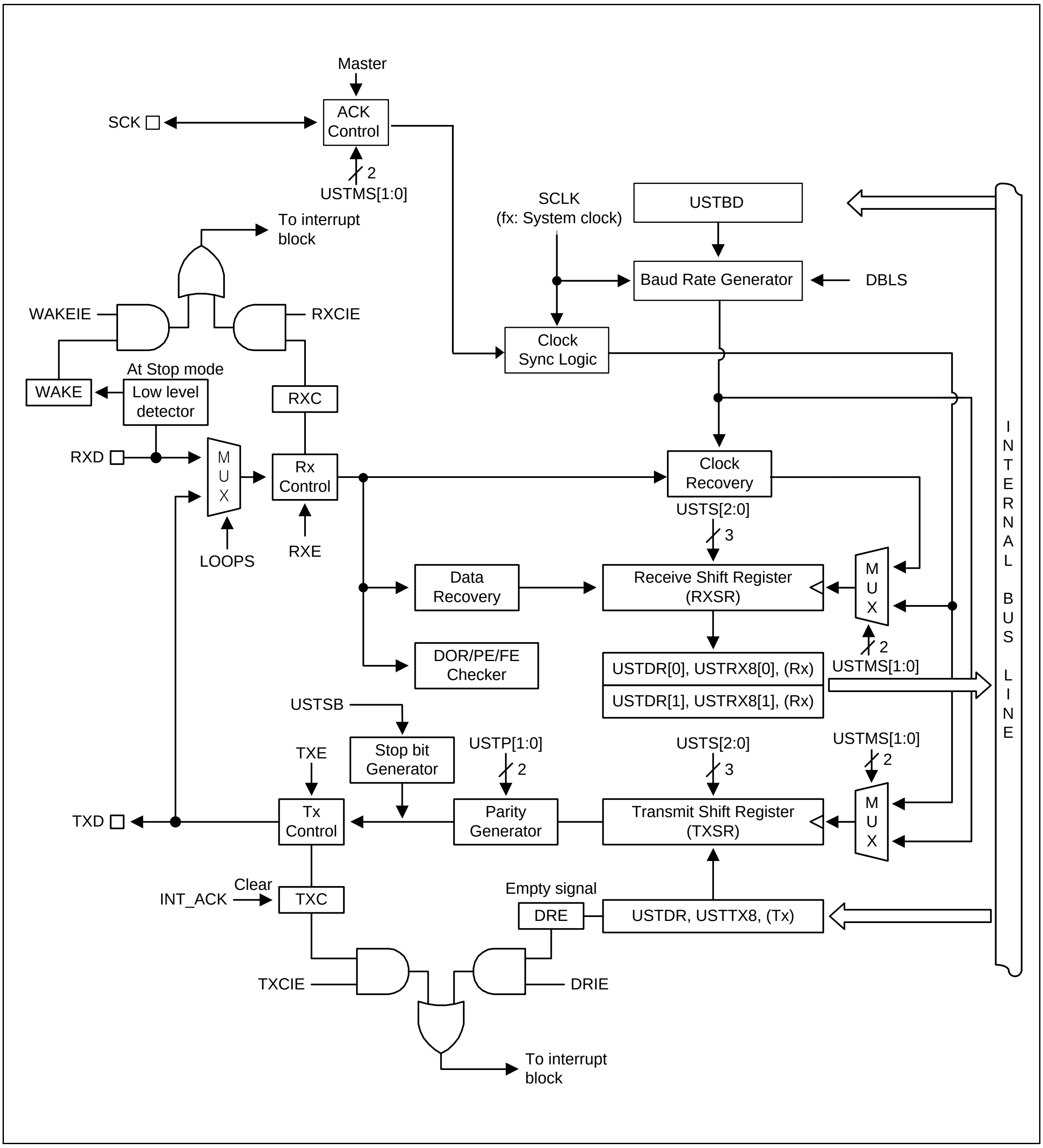


Figure 25. UART Block Diagram

13.3 USART SPI mode

The USART can be configured to operate in industrial standard SPI compliant mode.

The SPI mode has the following features:

- Full duplex, three-wire synchronous data transfer
- Mater and Slave operations
- Supports all four SPI modes of operation (mode 0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USTMS[1:0] = ”11”), the Slave Select (SS) pin becomes active LOW input in Slave mode operation, or can be output in Master mode operation if USTSSEN bit is set to ‘0’.

Note that during SPI mode of operation, the RXD pin is renamed as MISO and the TXD pin is renamed as MOSI for compatibility to other SPI devices.

13.4 SPI block diagram

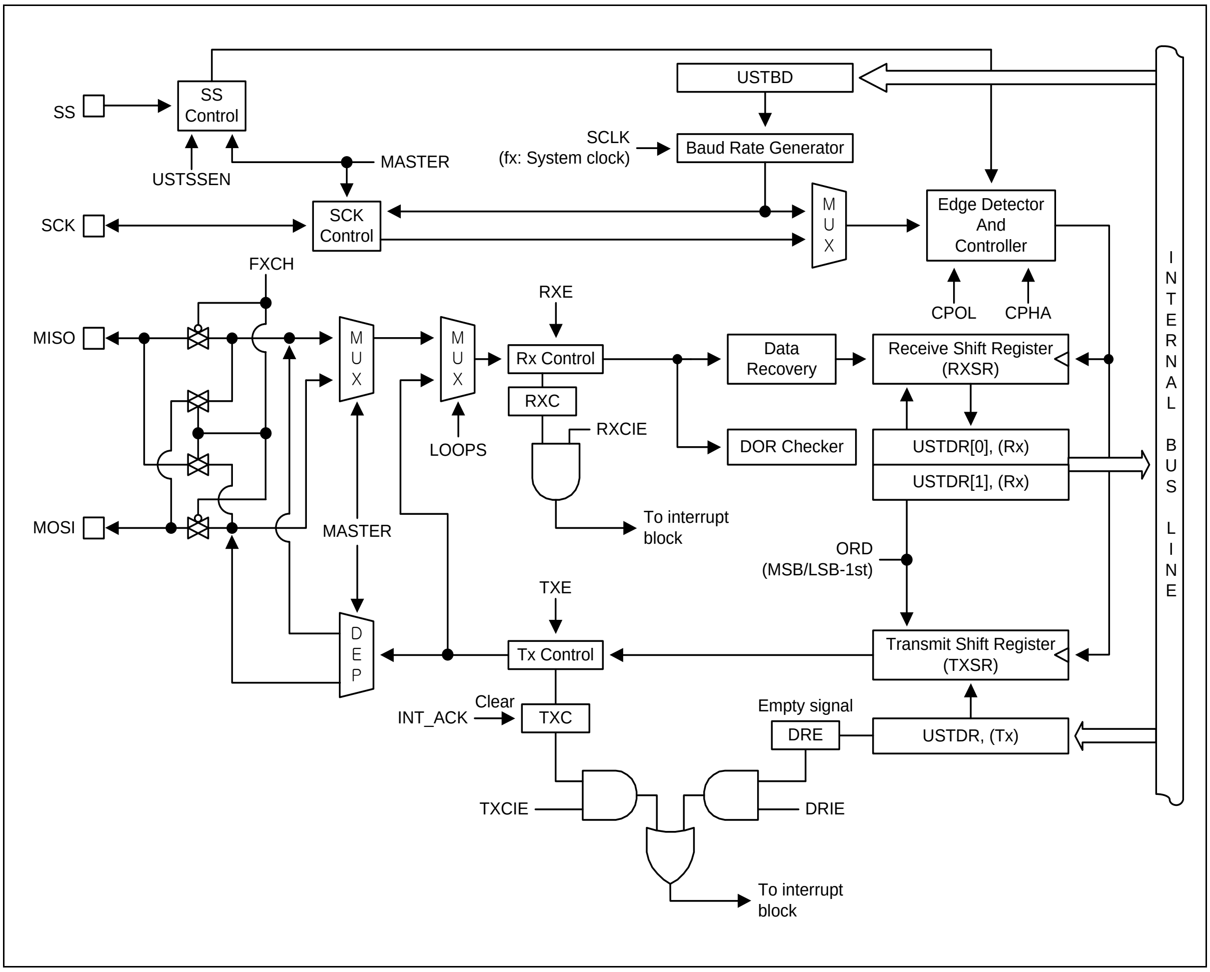
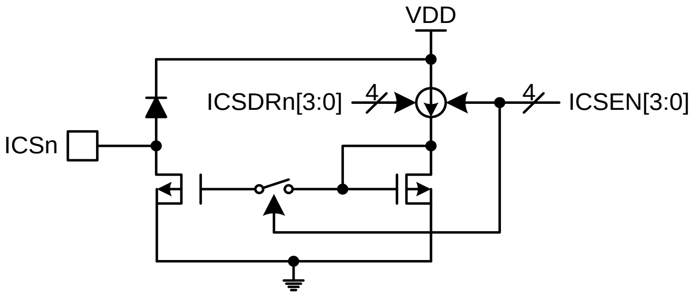


Figure 26. SPI Block Diagram

14 Constant sink current generator

Constant sink current generator supplies constant current regardless of variable I_{CS} voltage ranging from 2.0V to 3.6V. The constant current value is controlled by registers ICSDR0 and ICSDR1, and the sink current ranges from 49mA to 274mA.

14.1 Block diagram



NOTE: If a sink current generator of an ICSn pin is disabled by ICSCR[3:0], the corresponding ICSn pin is high and the current flowing is zero.

Figure 27. Constant Sink Current Generator Block Diagram (n=0 and 1)

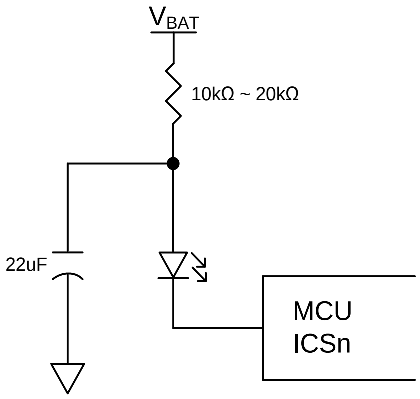


Figure 28. Constant Sink Current Generator Pin with Capacitor

15 Flash CRC and checksum generator

Flash CRC (Cyclic Redundancy Check) generator of A96L53x generates 16-bit CRC code bits from Flash and a generator polynomial. The CRC code for each input data frame is appended to the frame.

Specifically CRC-based technique is used to verify data transmission or storage integrity. In the scope of the functional safety standards, this technique offers a means of verifying the Flash memory integrity. The Flash CRC generator helps compute a signature of software during runtime, to be compared with a reference signature.

The CRC generator has following features:

- Auto CRC and User CRC mode
- CRC clock: f_{HFIRC}, $f_{HFIRC}/2$, $f_{HFIRC}/4$, $f_{HFIRC}/8$ and fx (system clock)
- CRC-16 polynomial: 0x8C81 ($X^{16} + X^{15} + X^{11} + X^{10} + X^{7} +1$)

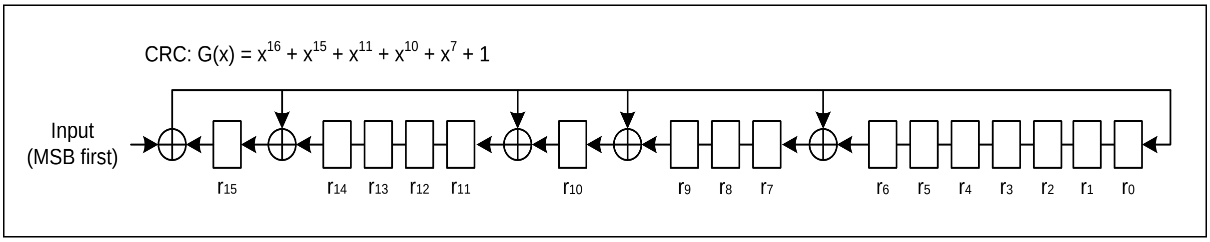


Figure 29. CRC-16 Polynomial Structure

15.1 Block diagram

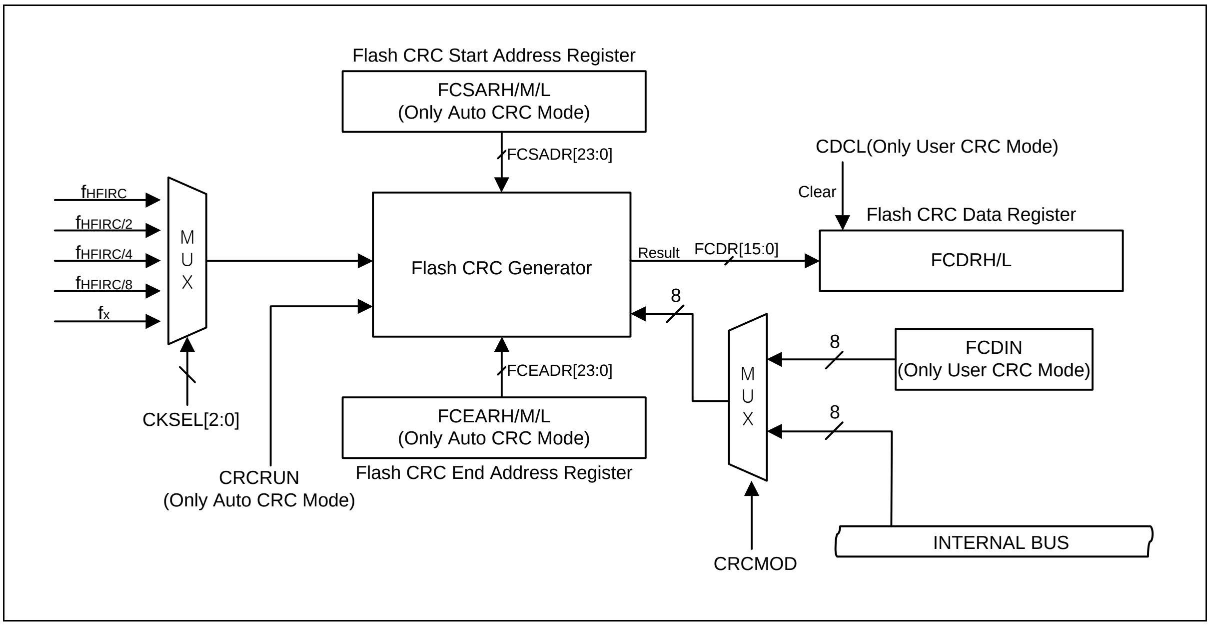


Figure 30. Flash CRC/Checksum Generator Block Diagram

16 Power down operation

A96L53x offers two Power-down modes (IDLE and STOP) to minimize power consumption. During the two power saving modes, programs are stopped and power consumption is reduced considerably.

16.1 Peripheral operation in IDLE mode or STOP mode

The peripheral's operation during IDLE/STOP mode is introduced in Table 10.

Table 10. Peripheral Operation during Power-down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watchdog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC, LFIRC OSC)
Timer0 to 1	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
USART	Operates Continuously	Stop
Siren	Operates Continuously	Stop
Line Interface	Operates Continuously	Stop
Internal OSC	Oscillation	Stop
WDTRC OSC (1KHz)	Can be operated with setting value	Can be operated with setting value
Constant Sink Current	Retain	Retain
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC2), External Interrupt, WDT, USART

17 Reset

When a reset event occurs, an internal register is selected to be initialized in accordance with a reset value. Each reset value introduced in Table 11 indicates a corresponding On Chip Hardware that is to be initialized.

Table 11. Reset Value and the Relevant On Chip Hardware

On Chip Hardware	Reset Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral clock	On
Control register	Refer to peripheral registers.

A96L53x has 5 types of reset sources as listed in the followings:

- External RESETB
- Power On RESET (POR)
- WDT overflow reset (in a case of WDTEN='1')
- Low voltage reset (in a case of LVREN='0')
- OCD RESET

17.1 Block diagram

Figure 31 shows a block diagram of a reset module.

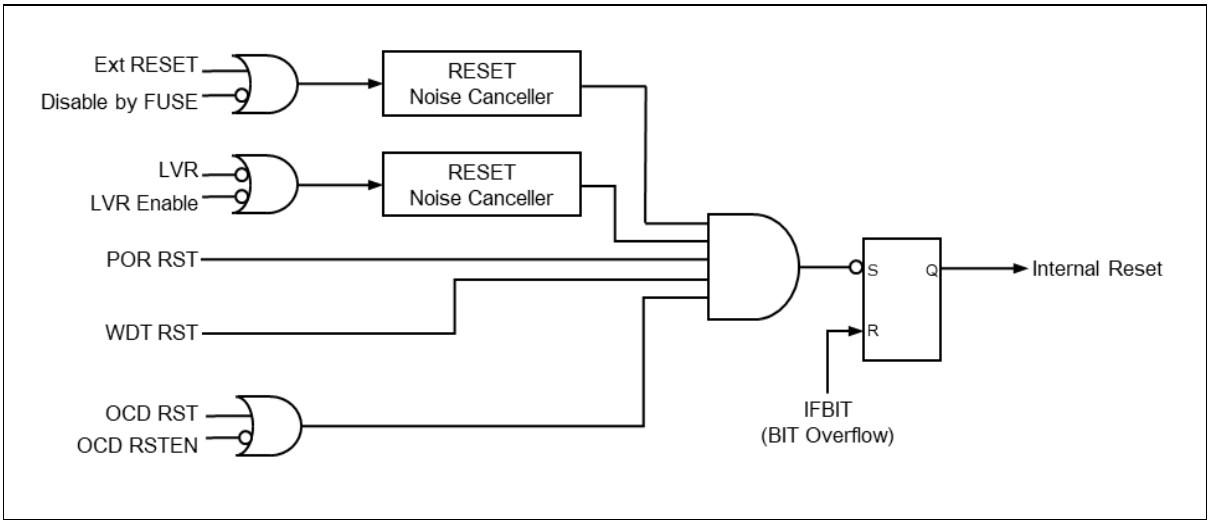


Figure 31. Reset Block Diagram

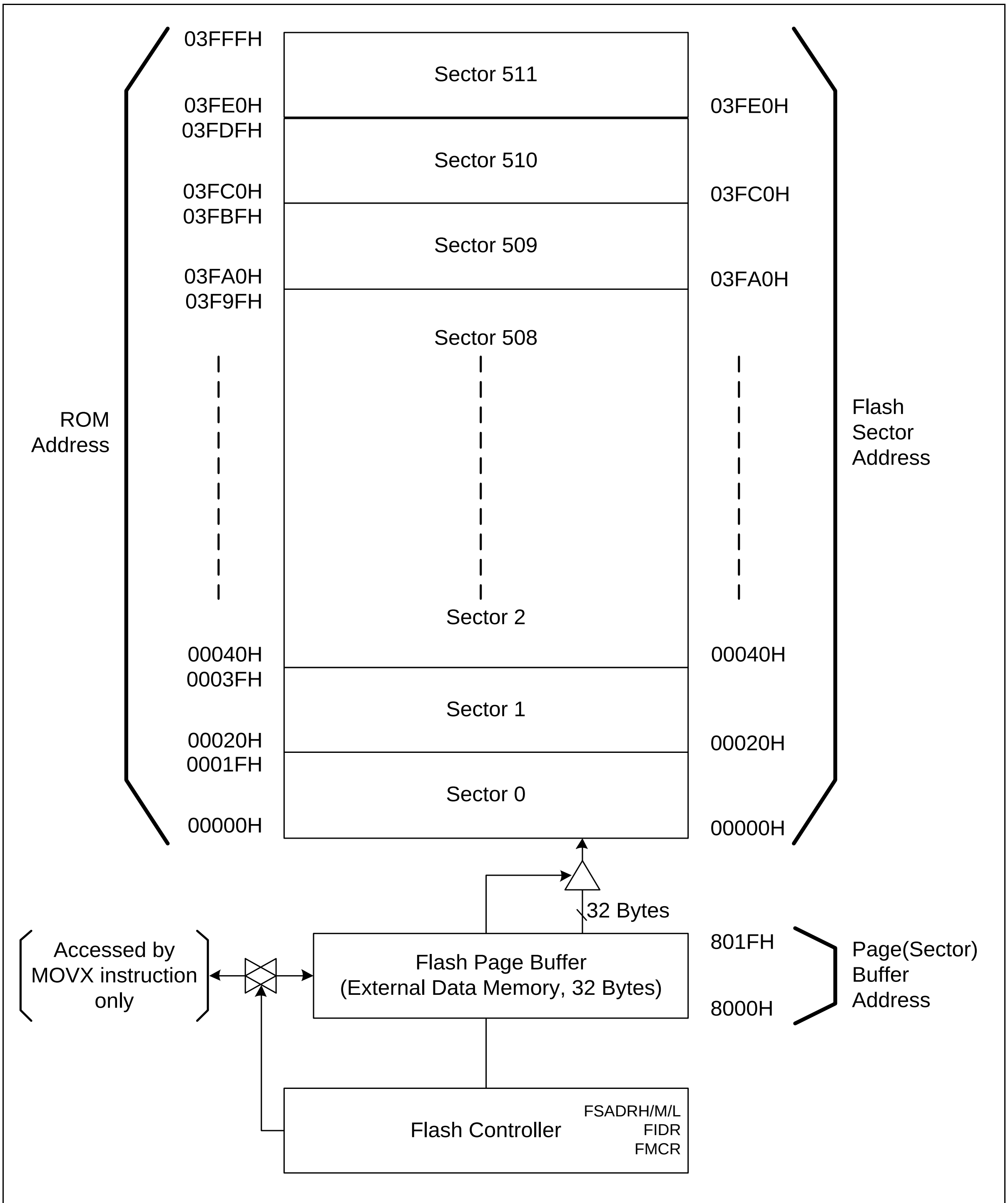
18 Flash memory

A96L53x incorporates Flash memory inside. Program can be written, erased, and overwritten on the Flash memory that is mounted on a board. The Flash memory can be read by ‘MOVC’ instruction and programmed in OCD, serial ISP mode or user program mode.

Main features of the Flash memory are summarized below:

- Flash Size: 8/16 Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for Flash memory

18.1 Flash program ROM structure



NOTES:

1. The Flash doesn’t support the byte-erase mode.
2. The Flash shouldn’t be entered in erase/write mode during data Flash program.
3. The Flash shouldn’t be entered in erase/write mode during data Flash program. So before the Flash program starts, the Data Flash Busy Bit (DFMBUSY) should be checked whether the bit is “1b”or not. If the bit is “1b”, do not start Flash program.
4. Note that the number of sectors is 255 as the Flash area of A96L533 is up to 1FFFh.

Figure 32. Flash Program ROM Structure

19 Data Flash memory

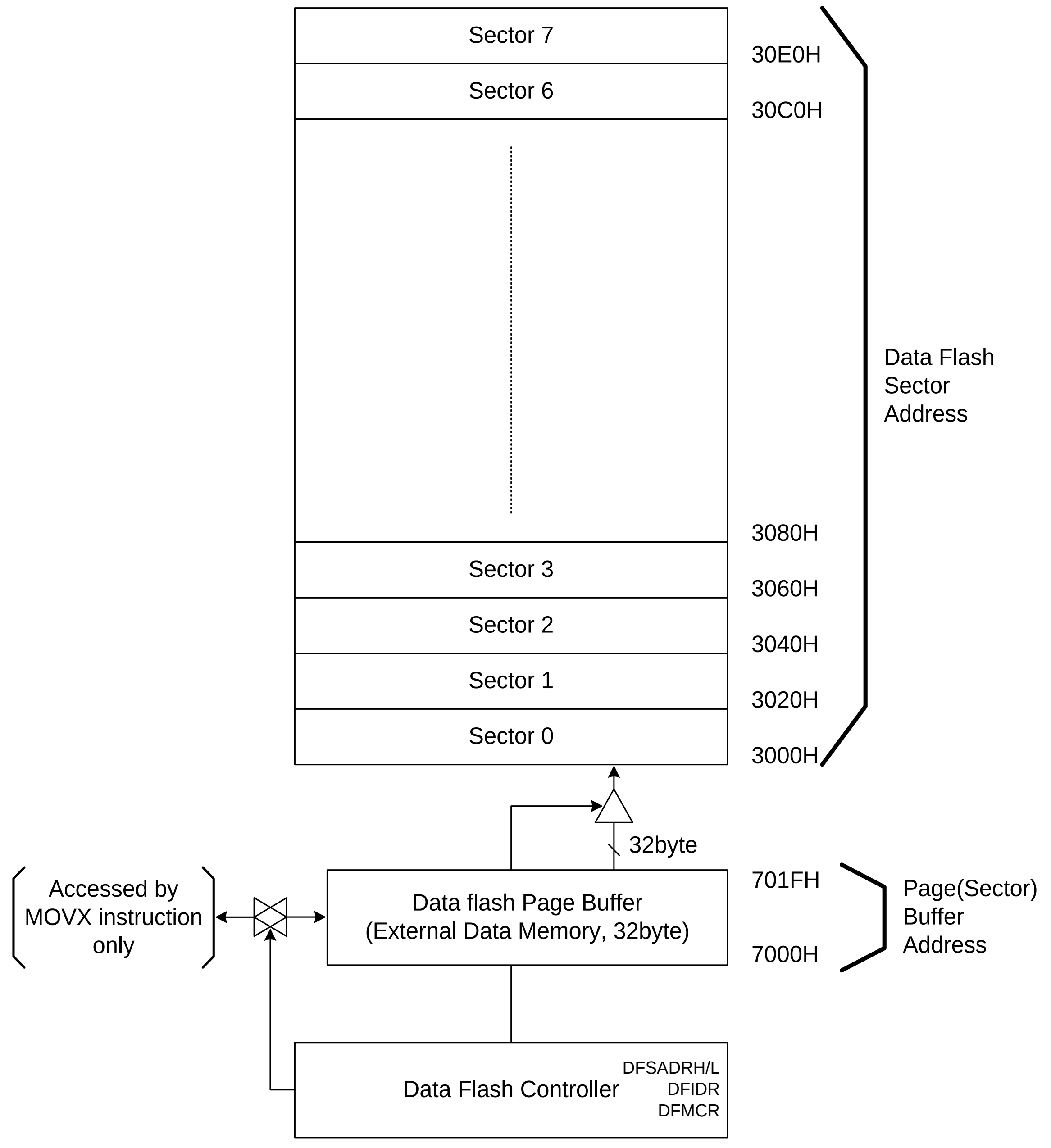
A96L53x includes Data Flash memory of 256bytes. It can be written, erased, and overwritten. The Data Flash memory can be read by the ‘MOVX’ instruction.

The Data Flash memory of A96L53x features the followings:

- Data Flash size: 256bytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature for memory

The write/erase cycles of the internal Data Flash can be increased significantly if it is divided into smaller and used in turn. If 256bytes are divided into 8 areas with 32bytes and each area from 1st to 8th is used for up to 100,000 cycles, the total number of erase/ write cycles can be 800,000.

Figure 33 describes the relationship between Data Flash page buffer, Data Flash controller, and Data Flash sector addresses.



NOTES:

1. The data Flash memory does not support byte-erase mode.
2. The data Flash is in extended data memory area.
3. If Idle and Stop are executed on data Flash erase/write, the erase/write is forcibly terminated. So before entering Idle and Stop mode, the Data Flash Busy Bit (DFMBUSY) should be checked whether the bit is “1b” or not. If the bit is “1b”, do not enter Idle or Stop mode.

Figure 33. Data Flash Structure

20 Logic functional description

20.1 Initial function

The VDD voltage increases as the external power VIN voltage increases. If the VDD voltage is 2.4V, then the UVLO signal goes to high and by this signal, the internal reset is released.

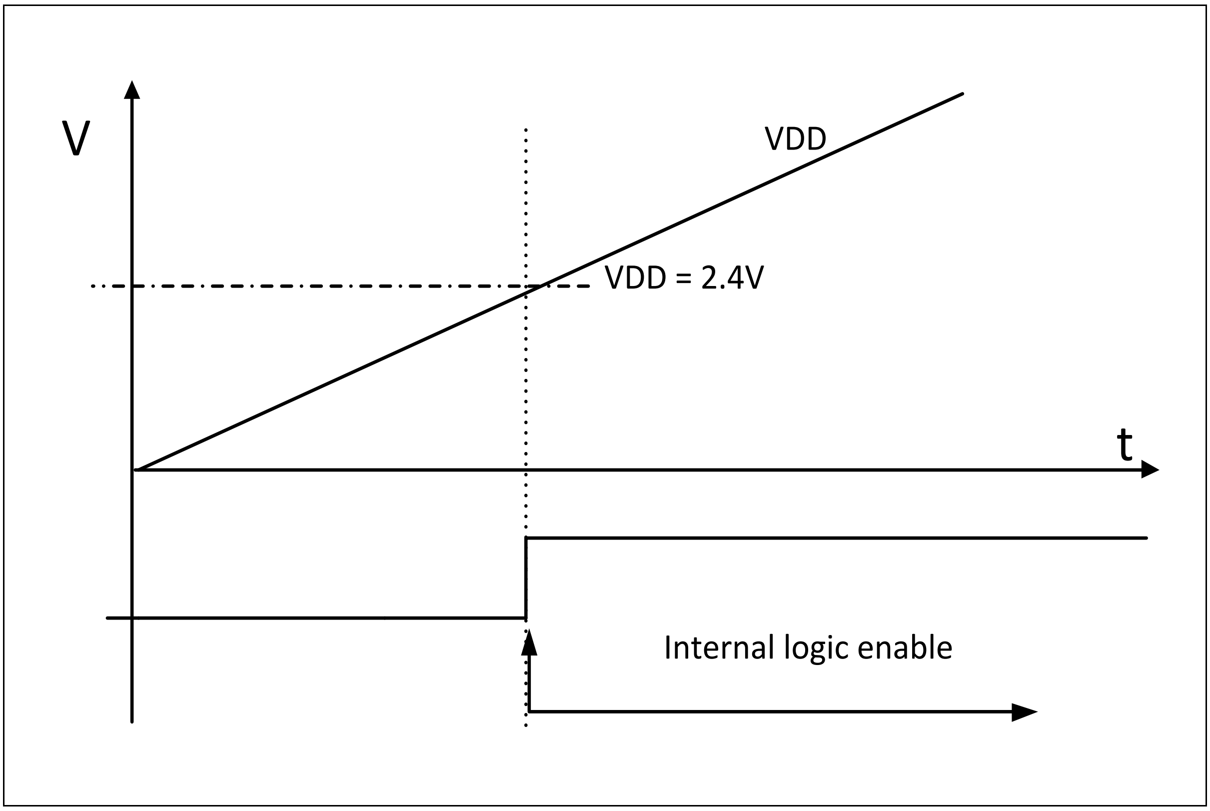


Figure 34. Reset Released by VDD

20.2 Power charging

A96L53x has the inrush current limit that is set by PMOS transistor. If the VIN voltage level is higher than the VOUT voltage level, the switch turns on via the comparator. At this time, the capacitor C0 of VOUT becomes charged state, and if VOUT voltage is higher than or equal to VIN, the switch turns off.

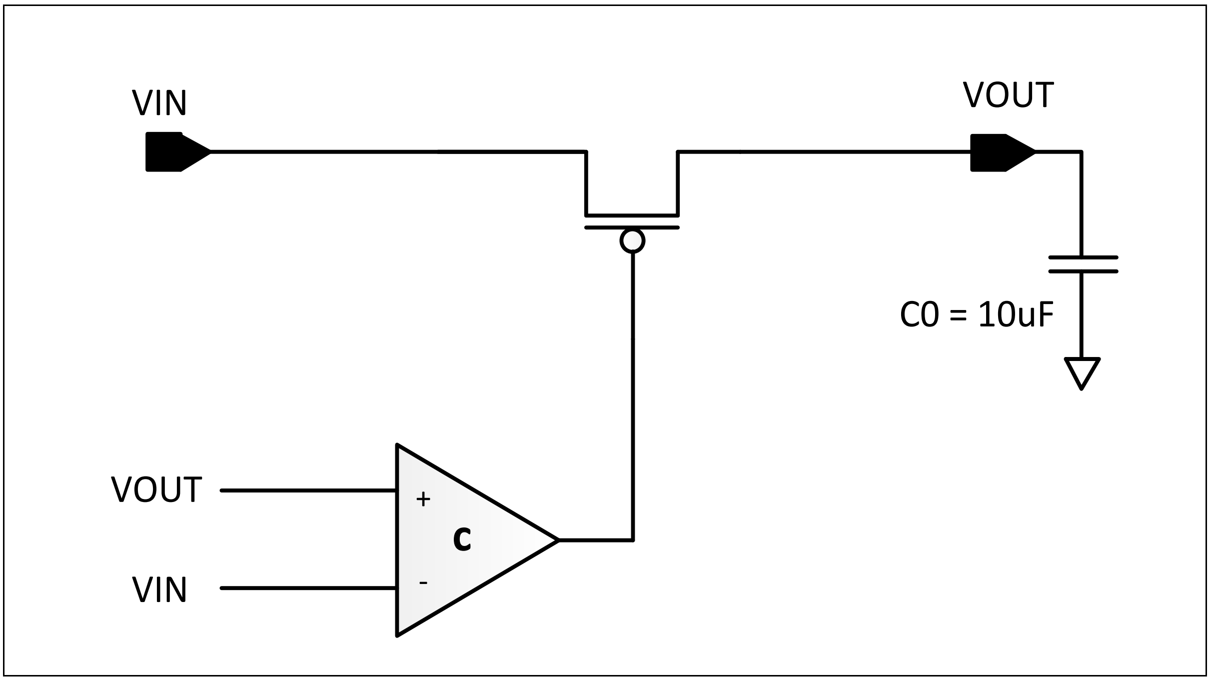


Figure 35. Power Charging by VIN and VOUT

20.3 RXT, RXR function

In case of line interface communication, data can be transferred by changing the VIN voltage. In the previous method, external comparator and resistor components were required. A96L53x supports this function inside the IC.

When the voltage difference between VOUT and VIN is bigger than 7.5V, the pin state changes to High through RXT pin and communication with Target MCU is performed through the RXT pin. If VOUT is operating voltage (8.5V or more) and VIN is lower than 7.5V, the RXT pin state becomes High. The period is called the TX period, and the TXR pin is used to change the VIN voltage at the target MCU.

An N-MOS transistor is built in the IC, and A96L53x has an internal comparator that operates as the timing diagram shown in Figure 36.

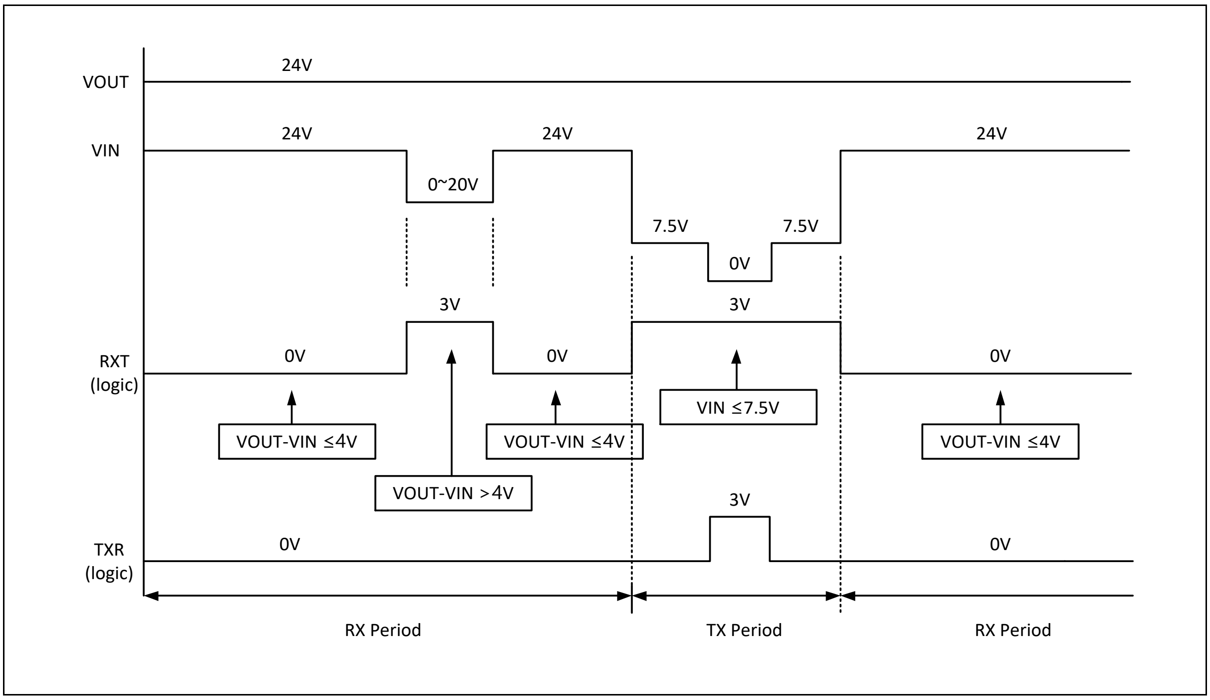


Figure 36. Timing Diagrams of RXT and TXR

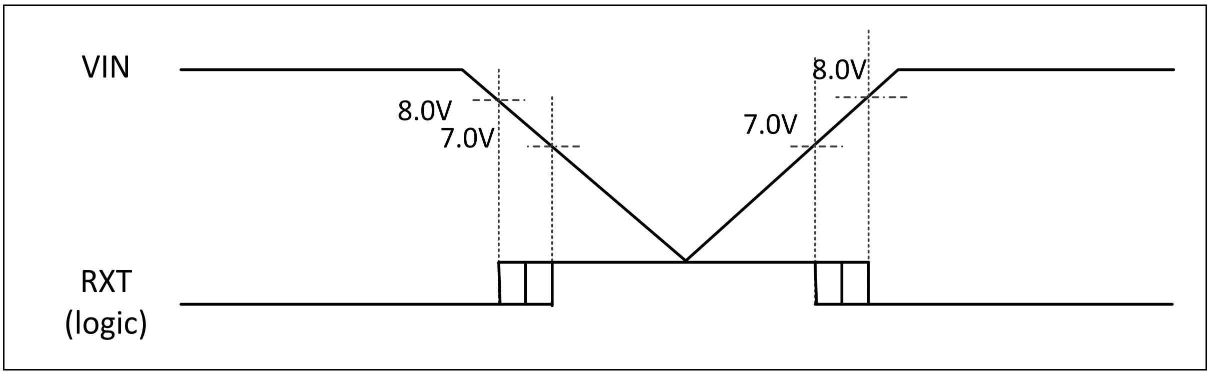


Figure 37. VIN and RXT Timing Diagram

NOTE: RXT and TXR are functions inside Logic, and A96L53x IC does not come out of the pin.

20.4 LDO description

A96L53x includes one LDO (Low Drop Output voltage) for microcontroller and indicated LED driver power. In the initial operation phase, when the power/signal line is connecting to VIN pin, the C0 capacitor on pin VOUT is charged.

The BGR circuit generates the VREF voltage. The LDO circuit can generate the LDO voltage by using the VREF voltage. The capacitor size of the C0 should be greater than or equal to the C1.

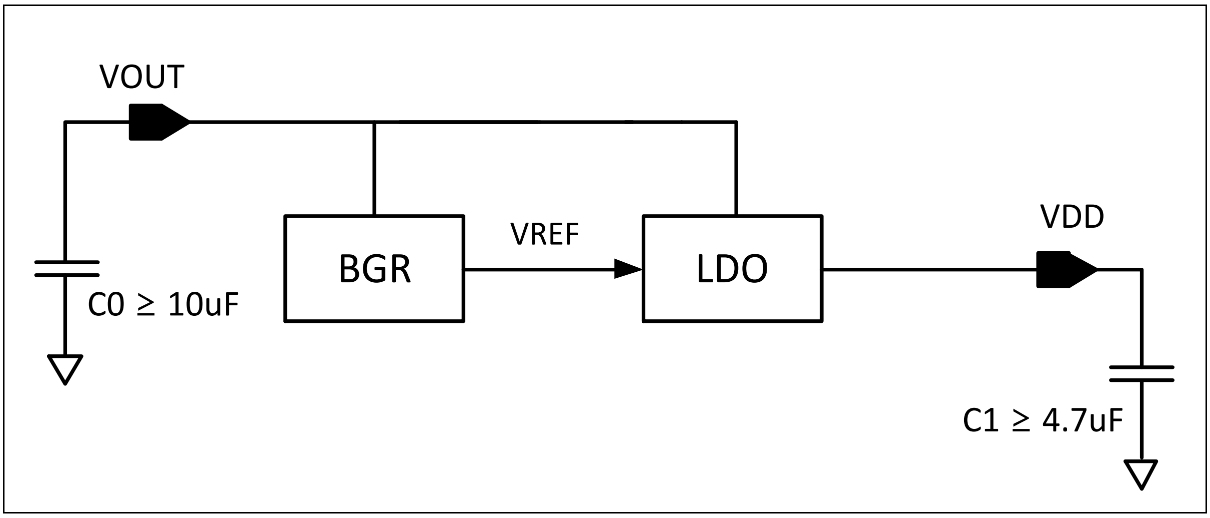


Figure 38. Block Diagram of LDO

21 Electrical characteristics

21.1 Absolute maximum ratings

Table 12. Absolute Maximum Ratings (MCU)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	VDD	-0.3 to +4.0	V	–
Normal Voltage Pin	VI	-0.3 to VDD+0.3	V	Voltage on any pin with respect to VSS
	VO	-0.3 to VDD+0.3	V	
	IOH	-20	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	∑IOH	-80	mA	Maximum current (∑I_{OH})
	IOL	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	∑IOL	120	mA	Maximum current (∑I_{OL})
Constant Sink Pin	IOL	390	mA	Maximum current sink by ICS0 and ICS1
Total Power Dissipation	PT	600	mW	–
Storage Temperature	TSTG	-65 to +150	°C	–

Table 13. Absolute Maximum Ratings (Logic)

Parameter [NOTE]	Symbol	Rating	Unit
Supply Voltage	VIN	-0.5 to +47	V
	VSS	-0.5 to +0.5	V
Input/ Output Pin Voltage	VIO	-0.5 to +35	V
LDO Output Current	IVDD	40	mA
Ground Current	IGND	40	mW
Total Power Dissipation	PT	300	mW
Storage Temperature	TSTG	-55 to +150	℃

Caution

Stresses beyond those listed under ‘Absolute Maximum Ratings’ may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

21.2 Operating conditions

The device must be used in the operating conditions that comply with the parameters in Table 14.

Table 14. Recommended Operating Conditions

(T_A= -40℃ to 85℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	fx=0.5 to 4.0MHz, HFIRC	2.0	—	3.6	V
		fx=32KHz, LFIRC	2.0	—	3.6	
Supply Voltage	VIN		8.5		42	V
Operating Temperature	T_{OPR}	VDD=2.0 to 3.6V	-40 NOTE	—	85	℃

NOTE: Electrolytic capacitors degrade at low temperatures, so consider using tantalum capacitors at low temperatures.

21.3 ADC characteristics

Table 15. ADC Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	—	—		—	10	—	bit
Integral Linear Error	ILE	AVREF= 2.2V to 3.6V f_{ADCCK}=2MHz		—	—	±3	LSB
Differential Linearity Error	DLE			—	—	±1	
Top Offset Error	TOE			—	—	±5	
Zero Offset Error	ZOE			—	—	±5	
Conversion Time	t_{CON}	AVREF= 2.2V to 3.6V		14	—	—	us
Analog Input Voltage	V_{AN}	—		VSS	—	VDD	V
Sample/ Hold Time	t_{SH}	—		3	—	—	us
Band Gap Reference Voltage	V_{BGR}	T_A = +25℃		-3	0.92	+3	%
A/DC Input Leakage Current	IAN	VDD=3V		—	—	2	uA
A/DC Current	I_{ADC}	Enable	VDD=3V	—	200	350	uA
		Disable		—	—	0.1	uA

NOTES:

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, under 2.7V resolution has no test.)

21.4 LDO23 characteristics

Table 16. LDO23 Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	–	2.6	–	3.6	V
Output Voltage	V_{LDO23}	T_A = +25℃	2.24	2.32	2.40	V
LDO Output Current	I_{LDO23}	V_{DD}=3V, CL=0.1uF, T_A = +25℃	2	–	–	mA
Stabilization Time	t_{STA}		–	–	100	us
LDO Block Current	I_{LDO}	Enable VDD=3V, No load	–	30	50	uA
		Disable	–	–	0.1	

21.5 Power on Reset

Table 17. Power on Reset Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

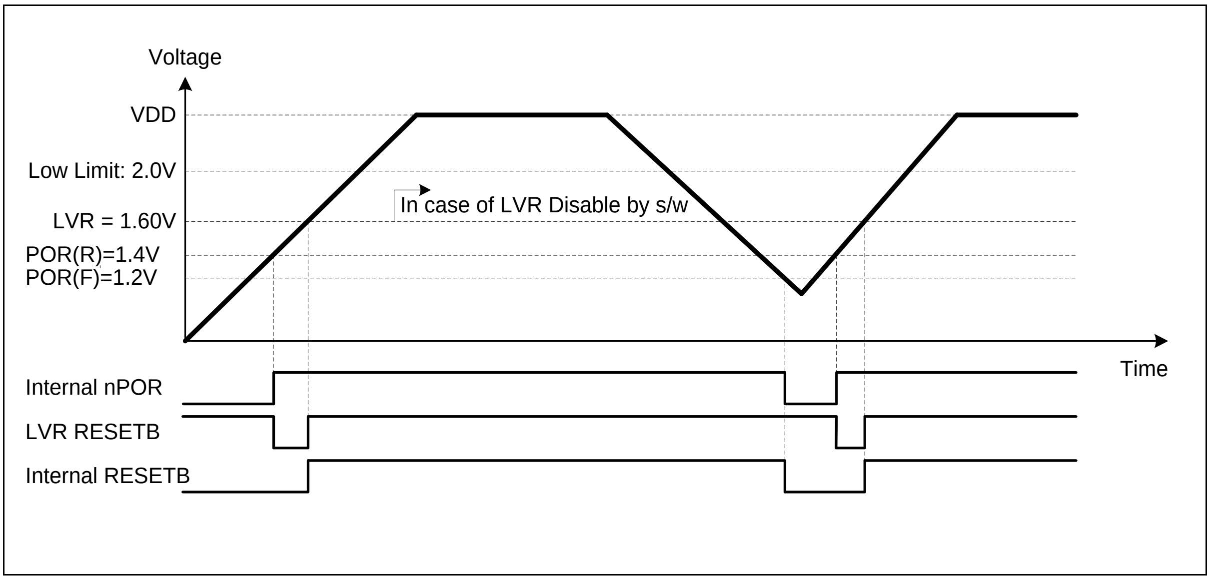


Figure 39. Power-On Reset Timing

21.6 Low voltage reset characteristics

Table 18. LVR Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Detection Level	V_{LVR}	The LVR can select all levels.		–	1.60	1.89	V
				2.05	2.20	2.35	
				2.20	2.40	2.60	
				2.45	2.70	2.95	
Hysteresis	△V	–		–	10	100	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR Current	I_{LVR}	Enable	VDD= 3V	–	0.8	1.6	uA
		Disable		–	–	0.1	

21.7 Operational amplifier 0/1 characteristics

Table 19. Operational Amplifier 0/1 Characteristic (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{OF}	VDD=3.0V		—	±10	±100	uV
Input Offset Current	I_{OF}	VDD=3.0V, VCM=0V		—	15	50	pA
Common-mode Rejection Ratio	CMRR	VDD=3.0V, DC VCM=0V to VDD-1.2V		80	100	—	dB
Power Supply Rejection Ration	PSRR	VDD=3.0V		80	100	—	
Open Loop Voltage Gain	—	VDD=3.0V		100	120	—	dB
Gain Error	ERR	VDD=3.0V, VIN ≥ 0.1V, x10 VIN<(Input x Gain)		—	—	1	%
Input Common-mode Voltage Range	V_{IN}	VDD=3.0V		0	—	VDD-1.2	V
Output Voltage Range	V_O	VDD=3.0V, RL=10KΩ		VSS +0.1	—	VDD-0.1	V
Output Short Circuit Current	ISCH	VDD=3.0V, Absolute		—	9	—	mA
	ISCL			—	12	—	
Gain Bandwidth	f_{GB}	VDD=3.0V		1	2	—	MHz
Voltage Follower Pulse Response	T_{AR}	VDD=3.0V, Small Signal		—	5	10	us
OP-AMP 0/1 Total Current	I_{AMP}	Enable	VDD=3.0V, No Load	—	220	300	uA
		Disable		—	—	0.1	
Enable Time of AMP0/1	t_{ON}	VDD=3.0V, Gain=x20/x30, RL=10KΩ with 50pF		—	—	150	us
Input Noise Voltage Density	e_{ni}	Input Referred	f=1Hz	—	0.1	—	uV/rtHz
		Input Referred	f=1KHz	—	50	—	nV/rtHz
Slew Rate	S_R	VDD=3.0V, RL=10K, CL=50pF		—	0.7	—	V/us
Phase Margin	P_M	VDD=3.0V, RL=10K, CL=50pF		—	60	—	Degrees
Chopping Clock	f_{CHOP}	—		125	—	167	kHz

21.8 High frequency internal RC oscillator characteristics

Table 20. High Frequency Internal RC Oscillator Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{HFIRC}	VDD=3.0V	—	4	—	MHz
Tolerance	—	T_A = -10°C to +50°C, with user (S/W) trim.	—	—	±1.0	%
		T_A = -10°C to +50°C			±2.0	
		T_A = -40°C to +85°C			±3.0	
Clock Duty Ratio	T_{OD}	—	40	50	60	%
Stabilization Time	T_{FS}	—	—	—	4	us

21.9 Low frequency internal RC oscillator characteristics

Table 21. Low Frequency Internal RC Oscillator Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Frequency	f_{LFIRC}	VDD=2.0V – 3.6V		—	32	—	kHz
Tolerance	—	T_A = -40°C to +85°C	With 0.1uF bypass capacitor	—	—	±10	%
Clock Duty Ratio	T_{OD}	—		40	50	60	%
Stabilization Time	T_{FS}	—		—	—	120	us
LFIRC Current	I_{LFIRC}	Enable	VDD=3V	—	1	—	uA
		Disable		—	—	0.1	

21.10 Internal Watchdog Timer RC oscillator characteristics

Table 22. Internal WDTRC Oscillator Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{WDTRC}	—	0.5	1	2	kHz
Stabilization Time	t_{WDTS}	—	—	—	1	ms
WDTRC Current	I_{WDTRC}	Enable	—	1	—	uA
		Disable	—	—	0.1	

21.11 DC characteristics

Table 23. DC Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V, f_{HFIRC}=4MHz)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH1}	All input pins except VIH2, RESETB		0.8VDD	—	VDD	V
	V_{IH2}	P01,P03–P05		0.7VDD	—	VDD	
Input Low Voltage	V_{IL1}	All input pins except VIL2, RESETB		—	—	0.2VDD	V
	V_{IL2}	P01,P03–P05		—	—	0.3VDD	
Output High Voltage	V_{OH}	VDD=3V, All output ports, IOH = – 4mA		VDD-1.0	—	—	V
Output Low Voltage	V_{OL}	VDD=3V, IOL = 6mA		—	—	1.0	V
Input High Leakage Current	I_{IH}	All output ports		—	—	1.0	uA
Input Low Leakage Current	I_{IL}	All output ports		-1.0	—	—	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A=25℃, All Input ports	VDD=3.0V	25	50	100	kΩ
	R_{PU2}	VI=0V, T_A=25℃, RESETB	VDD=3.0V	100	200	400	kΩ
Supply Current	I_{DD1} (RUN)	f_{HFIRC} = 4MHz	VDD=3V±10%	—	400	600	uA
		f_{HFIRC} = 2MHz		—	240	360	
		f_{HFIRC} = 1MHz		—	170	250	
	I_{DD2} (IDLE)	f_{HFIRC} = 4MHz	VDD=3V±10%	—	100	150	uA
		f_{HFIRC} = 2MHz		—	90	135	
		f_{HFIRC} = 1MHz		—	75	110	
	I_{DD3} (Run)	VDD=3V, f_{LFIRC}=32KHz, TA=25℃		—	40	65	uA
	I_{DD4} (Idle)	VDD=3V, f_{LFIRC}=32KHz, TA=25℃		—	2	5	uA
	I_{DD5}	STOP, VDD= 3V±10%, T_A= 25℃		—	0.5	3.0	uA
		STOP, VDD= 3V±10%, T_A= 25℃, LFIRC on		—	1.5	4.0	

NOTES:

1. Where the f_{HFIRC} is a high frequency internal RC oscillator and the f_{LFIRC} is a low frequency.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current include the current of the power-on reset (POR) block.

Table 24. DC Characteristics (Logic)

(T_A=25℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VIN	-	8.5	24	42	V
LDO Output Voltage	VDD	IOUT=1mA VOUT=24V @ T=25°C	2.91	3.0	3.09	V
	dVDD	IOUT=1mA to 5mA, VOUT=24V	-	15	20	mV
		IOUT=5mA to 20mA, VOUT=24V	-	15	45	
LDO Output Tolerance	Vtol	VDD=3.0V @-10 to 60°C NOTE1	-3		3	%
PSRR	PSRR	F=100Hz NOTE2	50			dB
TXR Pull-down	IiH	VDD=3V	20	40	60	uA
Inrush Current	IVIN1	VIN=0V to 24V, @rise time 10ms		24	35	mA
TXR Current	IVIN2	VIN=7V, VOUT = 24V	60			mA
Input High Voltage TXR	Vih	VDD=3V	0.8*VDD		VDD	V
Input Low Voltage TXR	Vil	VDD=3V	0		0.2*VDD	V
Output High Voltage RXT	Voh	VDD=3V, Ioh= -1mA	0.8*VDD		VDD	V
Output Low Voltage RXT	Vol	VDD=3V, Iol=1mA	0		0.2*VDD	V
VIN Input Voltage for RXT High	VRXH1	VOUT =8.5V	7.0		8.0	V
VOUT-VIN Voltage for RXT High	VRXH2	VOUT=24V	4.0		6.0	V
Static Current	IVIN	VIN=24V, VOUT = 24V, TXR = 0V, @T=25°C		60	90 NOTE3	uA

NOTES:

1. The measured value for the parameters and conditions listed were confirmed by Laboratory environment. In test conditions, it is measured in a room temperature environment.
2. The measured value for the parameters and conditions listed were confirmed by simulation.
3. This value is the maximum standby current value in the logic part. For MCP products combined with MCU, the maximum value is 93uA.

21.12 Constant sink current electrical characteristics

Table 25. Constant Sink Current Electrical Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Constant Sink Current	I_{CS}	VDD=3V V_{ICS}=1.5V T_A=25℃	ICSDR[3:0] = 0	-7%	49	+7%	mA
			ICSDR[3:0] = 1	-7%	65	+7%	
			ICSDR[3:0] = 2	-7%	80	+7%	
			ICSDR[3:0] = 3	-7%	96	+7%	
			ICSDR[3:0] = 4	-7%	111	+7%	
			ICSDR[3:0] = 5	-7%	127	+7%	
			ICSDR[3:0] = 6	-7%	142	+7%	
			ICSDR[3:0] = 7	-7%	158	+7%	
			ICSDR[3:0] = 8	-7%	173	+7%	
			ICSDR[3:0] = 9	-7%	188	+7%	
			ICSDR[3:0] = 10	-7%	203	+7%	
			ICSDR[3:0] = 11	-7%	218	+7%	
			ICSDR[3:0] = 12	-7%	232	+7%	
			ICSDR[3:0] = 13	-7%	246	+7%	
			ICSDR[3:0] = 14	-7%	260	+7%	
			ICSDR[3:0] = 15	-7%	274	+7%	
		VDD=3V V_{ICS}=1V to 2.0V	ICSDR[3:0] = n n: 0 to 15	-15%	Typ.	+15%	
		VDD=2.7V to 3.6V V_{ICS}=1V to VDD-1.0V	ICSDR[3:0] = n n: 0 to 15	-20%	Typ.	+20%	

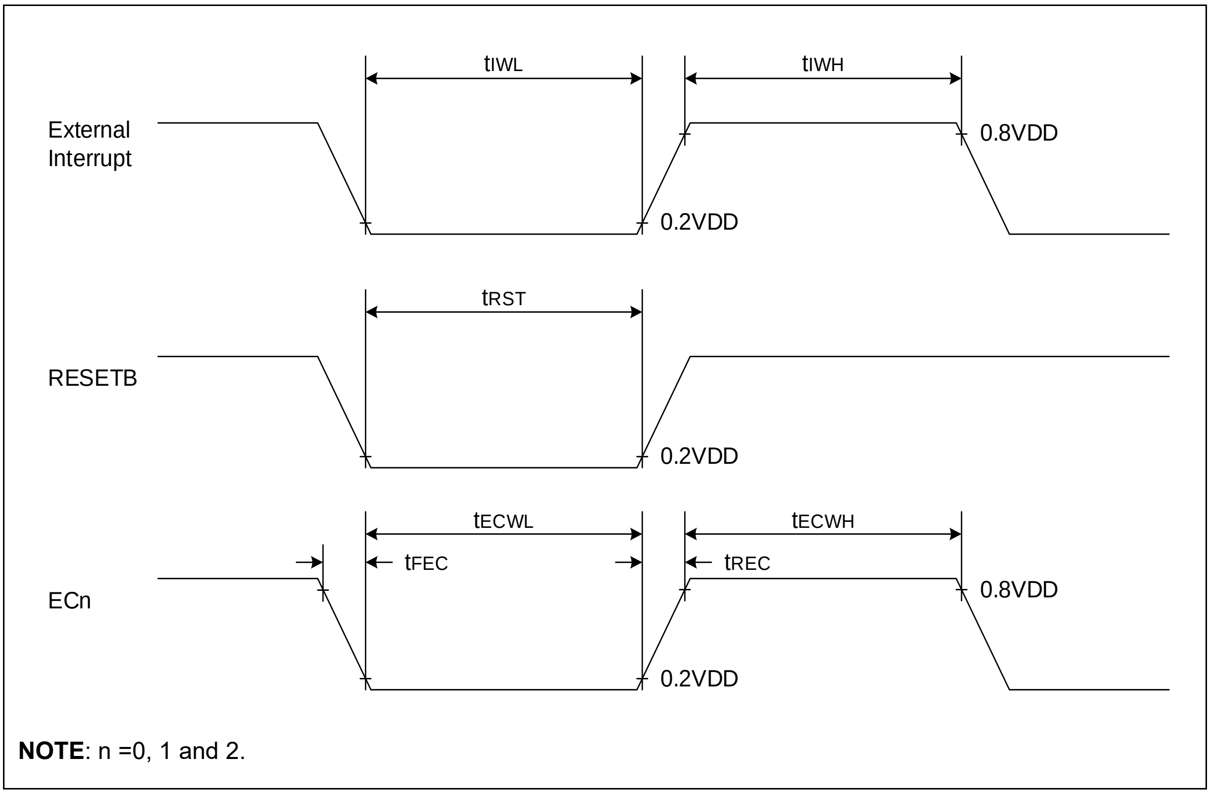
NOTE : The higher the sink current of ICSDR, the higher the LDO value. Under the condition of ICSDR[3:0] = 15, the LDO value increases by +1% typical.

21.13 AC characteristics

Table 26. AC Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB Input Low Width	t_{RST}	VDD = 3V	10	—	—	us
Interrupt Input High, Low Width	t_{IWH}, t_{IWL}	All interrupt, VDD = 3V	200	—	—	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 3V Where n=0, 1, and 2	200	—	—	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 3V Where n=0, 1, and 2	20	—	—	
Wake-up from Idle/ Stop Mode	t_{WU0}	From HFIRC	—	—	16	us
	t_{WU1}	From LFIRC	—	—	1000	us



NOTE: n =0, 1 and 2.

Figure 40. AC Timing

21.14 SPI characteristics

Table 27. SPI Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	1000	—	—	ns
Input Clock Pulse Period		External SCK source	1000	—	—	
Output Clock High, Low Pulse Width	t_{SCKH} t_{SCKL}	Internal SCK source	400	—	—	
Input Clock High, Low Pulse Width		External SCK source	400	—	—	
First Output Clock Delay Time	t_{FOD}	Internal/external SCK source	500	—	—	
Output Clock Delay Time	t_{DS}	—	—	—	125	
Input Setup Time	t_{DIS}	—	500	—	—	
Input Hold Time	t_{DIH}	—	500	—	—	

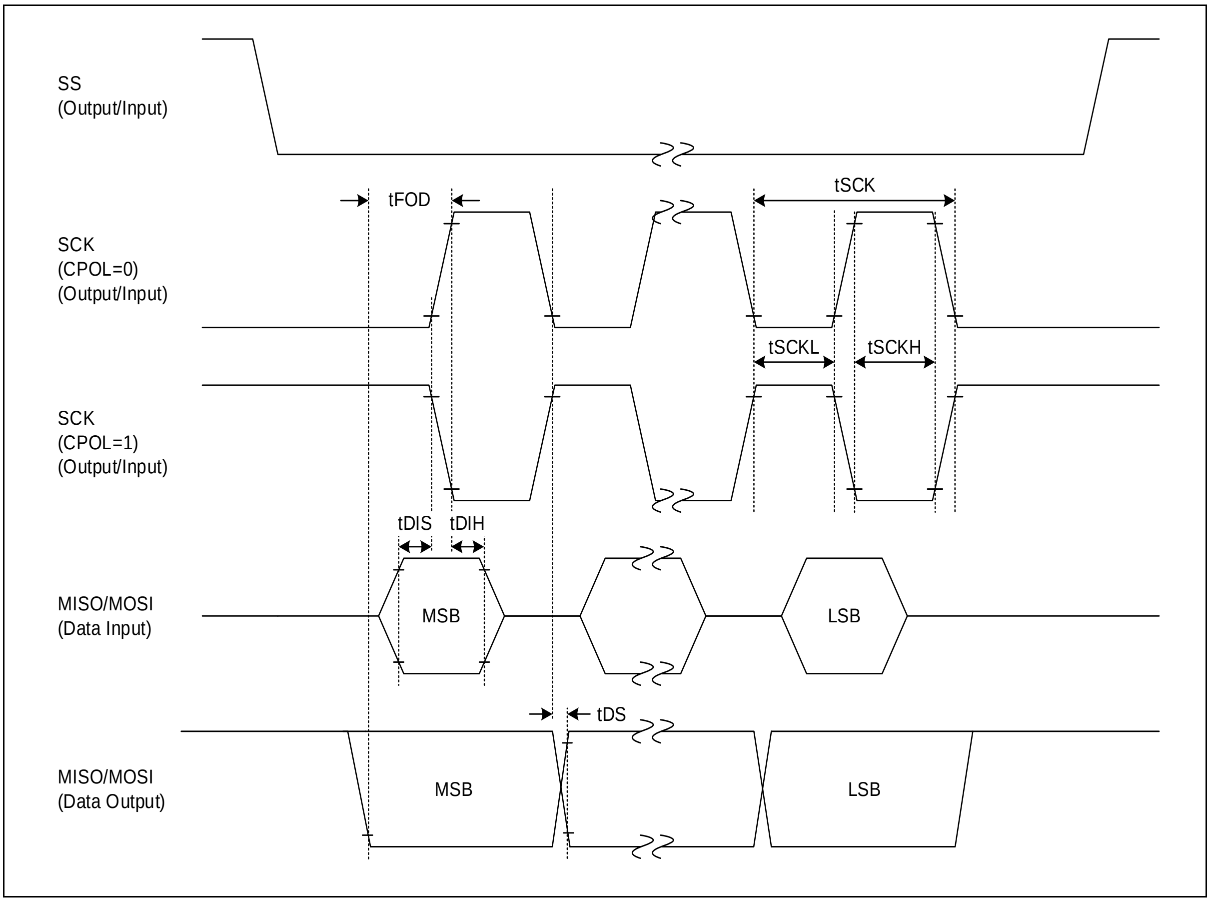


Figure 41. SPI Timing

21.15 UART timing characteristics

Table 28. UART Timing Characteristics (MCU)

(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V, fx=1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial Port Clock Cycle Time	t_{SCK}	13.92	t_{CPU} x 16	18.08	us
Output Data Setup To Clock Rising Edge	t_{S1}	6.5	t_{CPU} x 13	—	
Clock Rising Edge To Input Data Valid	t_{S2}	—	—	6.5	
Output Data Hold After Clock Rising Edge	t_{H1}	t_{CPU} – 0.1	t_{CPU}	—	
Input Data Hold After Clock Rising Edge	t_{H2}	0	—	—	
Serial Port Clock High, Low Level Width	t_{HIGH}, t_{LOW}	5.5	t_{CPU} x 8	10.5	

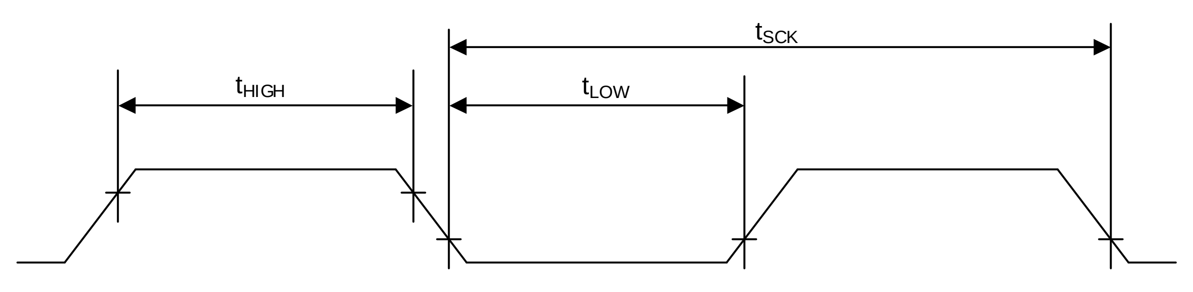


Figure 42. UART Timing Characteristics

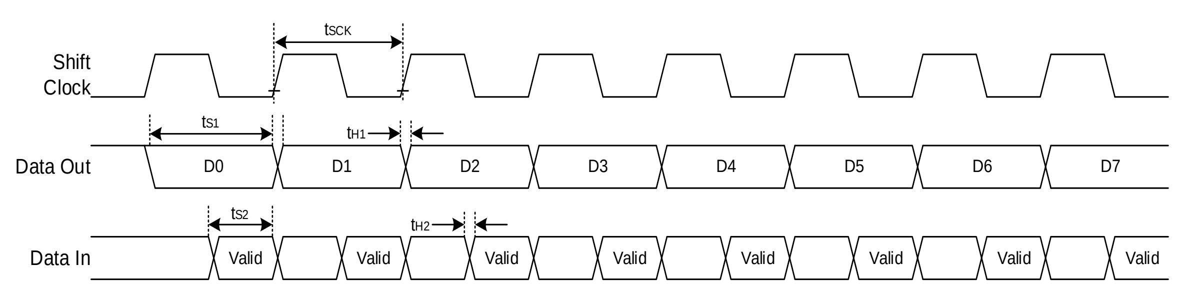


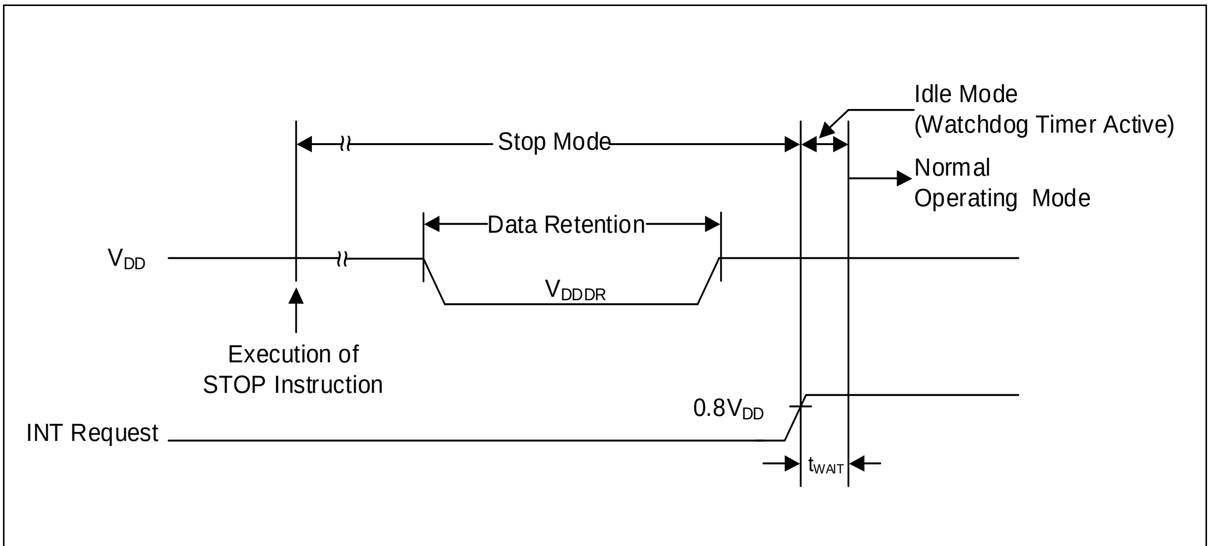
Figure 43. Timing Waveform of UART Module

21.16 Data retention voltage in STOP mode

Table 29. Data Retention Voltage in STOP Mode (MCU)

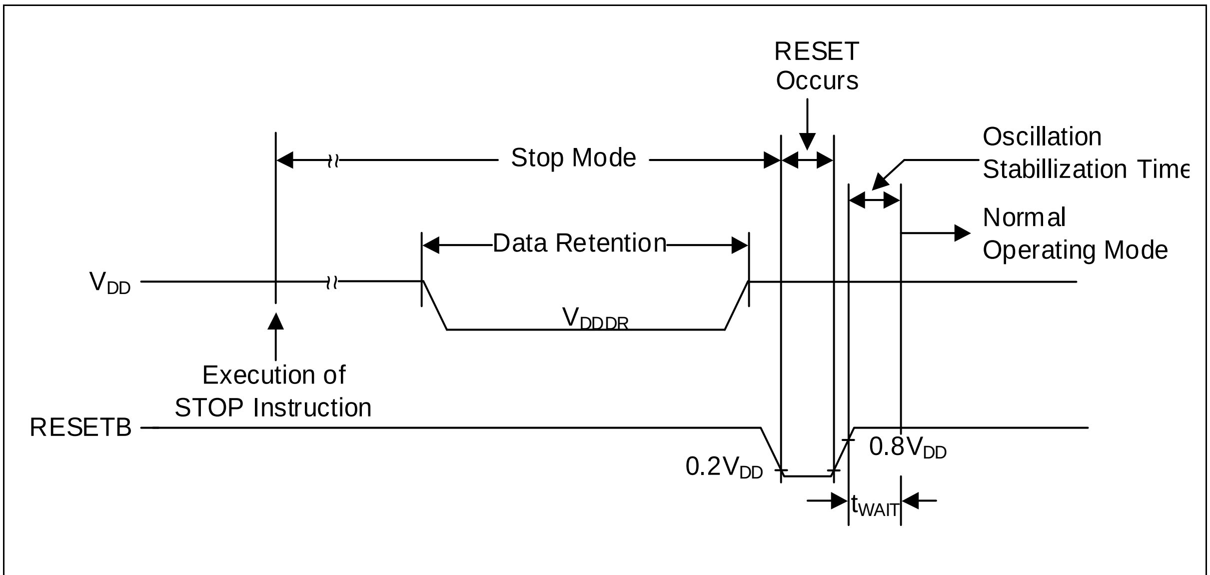
(T_A=-40℃ to +85℃, VDD=2.0V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DDDR}	—	2.0	—	3.6	V
Data Retention Supply Current	I_{DDDR}	VDDR= 2.0V (T_A= 25°C), STOP mode	—	—	1	uA



NOTE: t_{WAIT} is the same as (the selected bit overflow of BIT) x 1/ (BIT clock)

Figure 44. STOP Mode Release Timing when Initiated by an Interrupt



NOTE: t_{WAIT} is the same as (4096 x 4 x 4/f_{HFIRC}) = (16.4 ms at fx=4MHz)

Figure 45. STOP Mode Release Timing when Initiated by RESETB

21.17 Internal Flash characteristics

Table 30. Internal Flash Characteristics(MCU)

(T_A= +25℃, VDD=2.0V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector Write Time	t_{FSW}	—	—	2.5	2.7	ms
Sector Erase Time	t_{FSE}	—	—	2.5	2.7	
Code Write Protection Time	t_{FHL}	—	—	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	—	—	—	5	us
Flash Program Voltage	V_{PGM}	On erase/write	2.0	—	3.6	V
System Clock Frequency	f_{SCLK}	—	0.5	—	—	MHz
Endurance of Write/ Erase	N_{FWE}	Sector erase, Byte write	10,000	—	—	cycles

21.18 Internal data Flash characteristics

Table 31. Internal Data Flash Characteristics(MCU)

(T_A= +25℃, VDD=2.0V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector Write Time	t_{DFSW}	—	—	2.5	2.7	ms
Sector Erase Time	t_{DFSE}	—	—	2.5	2.7	
Page Buffer Reset Time	t_{DFBR}	—	—	—	5	us
Data Flash Program Voltage	V_{DPGM}	On erase/write	2.0	—	3.6	V
System Clock frequency	f_{SCLK}	—	0.5	—	—	MHz
Endurance of Write/ Erase	NE_{WE}	Sector erase, Byte write	100,000	—	—	cycles

21.19 Input/output capacitance characteristics

Table 32. I/O Capacitance Characteristics(MCU)

(T_A=-40℃ to +85℃, VDD=.0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	fx=1MHz unmeasured pins are connected to VSS.	—	—	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

21.20 UVLO characteristics

Table 33. UVLO Characteristics (Logic)

(T_A=-40℃ to +85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
RESET Release Level		-	-	2.4 NOTE	-	V

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

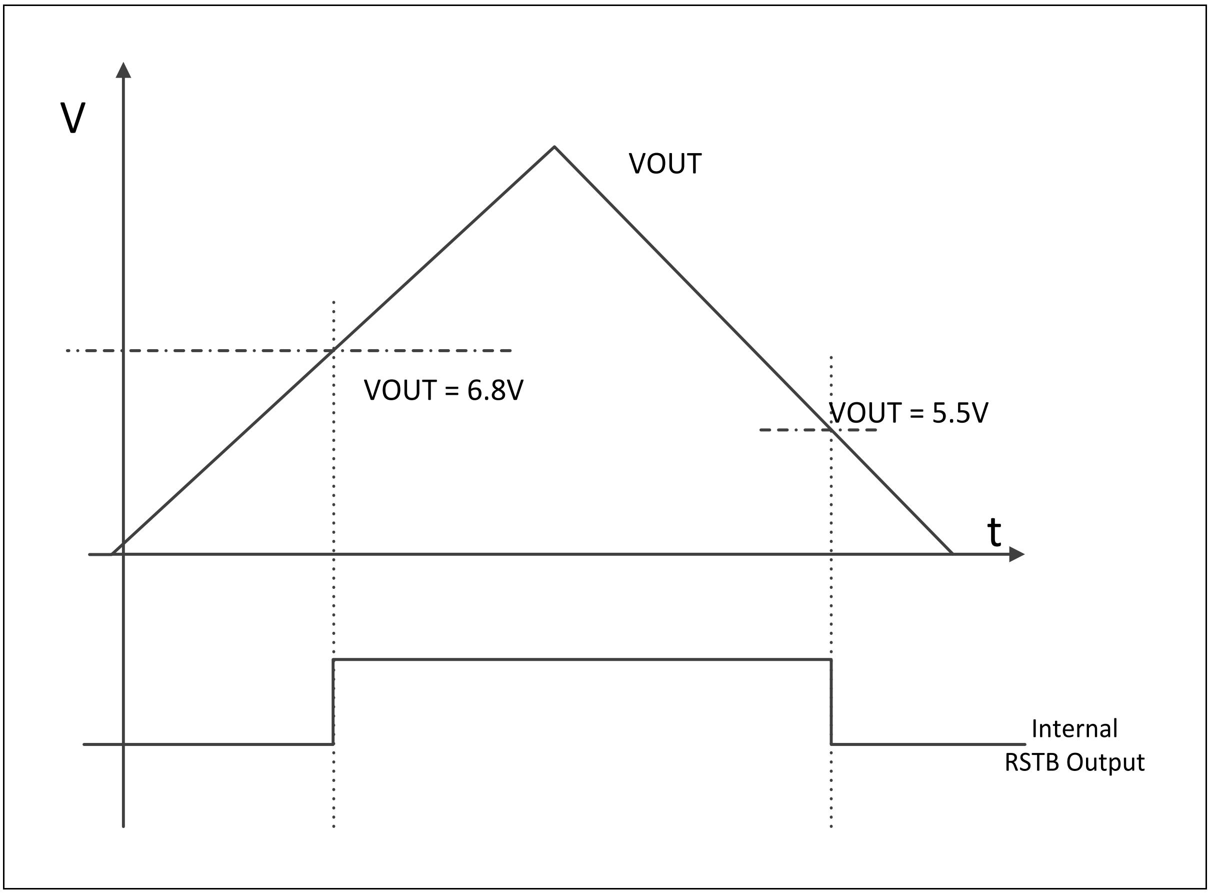


Figure 46. Internal UVLO Timing Diagrams

21.21 Recommended circuit and layout

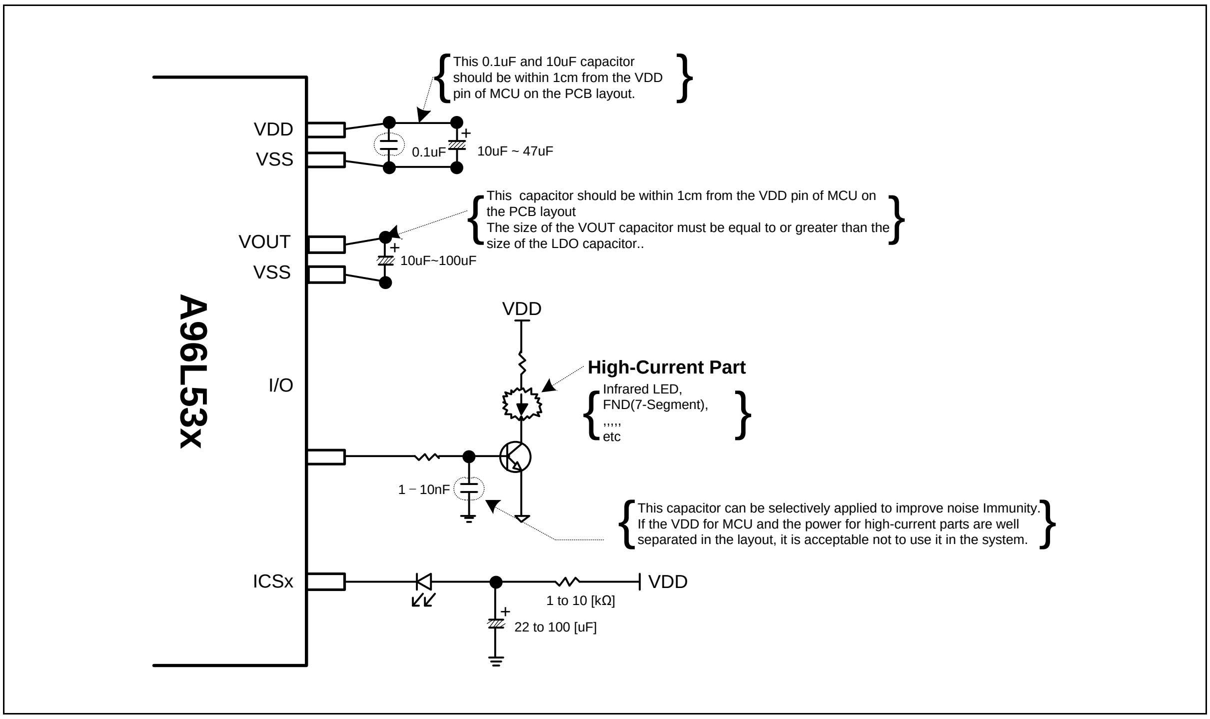
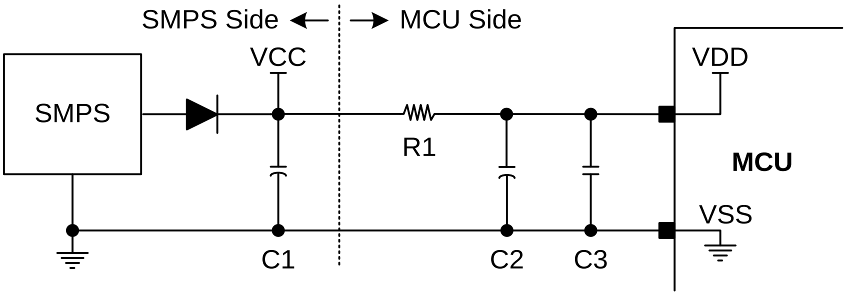


Figure 47. Recommended Circuit and Layout

In order to use it as a smoke detector application, generally IR LED is used and Blue LED is used. In some cases, one LED is used depending on the user's purpose. ICSx can be used to suit the purpose of use, or an external transistor can be additionally configured. Refer to 21.5.4 Example circuit for a circuit diagram suitable for this.

21.22 Recommended circuit and layout with SMPS power



NOTES:

1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470uF/ 25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10Ω to 20Ω
   - Recommended C2: 47uF/ 25V more
   - The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2uF more
   - The C3 should be within 1cm from the VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of MCU.

Figure 48. Recommended Circuit and Layout with SMPS Power

21.23 Typical characteristics

Below figures and tables introduced in this section can be used only for design guidance, and are not tested or guaranteed. In graphs or tables some data may exceed specified operating range, and can be used only for information. The device is guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation. The graph values below are the current values of MCU alone, and the current values of the MCP product increase up to 90uA in the product.

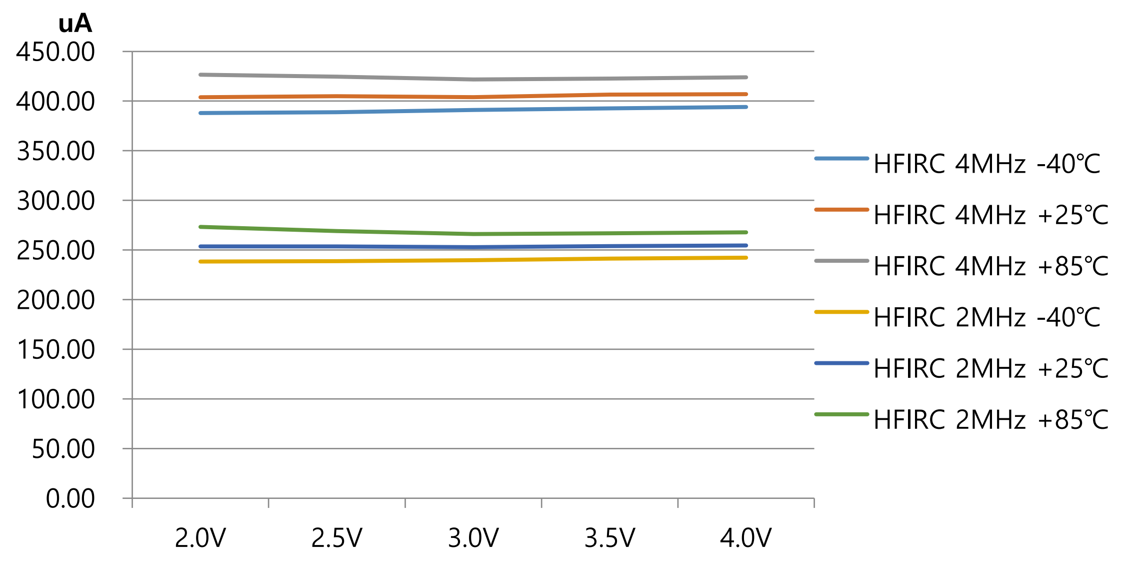


Figure 49. RUN (IDD1) Current

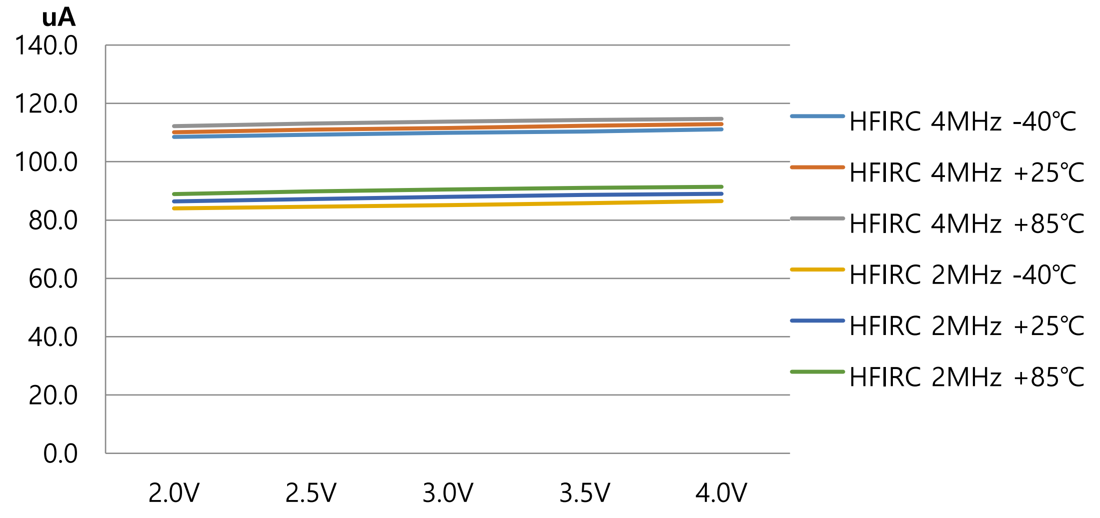


Figure 50. IDLE (IDD2) Current

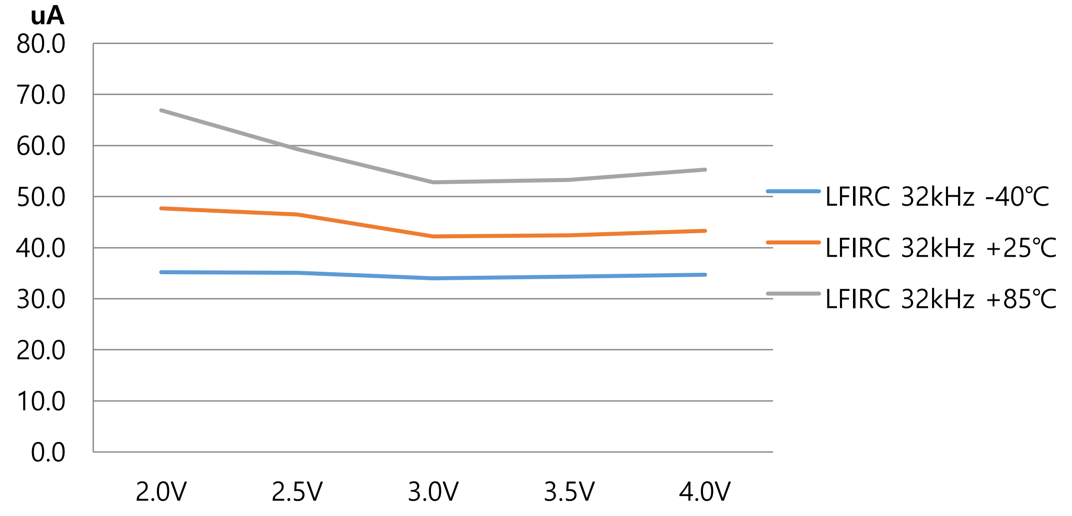


Figure 51. RUN (IDD3) Current

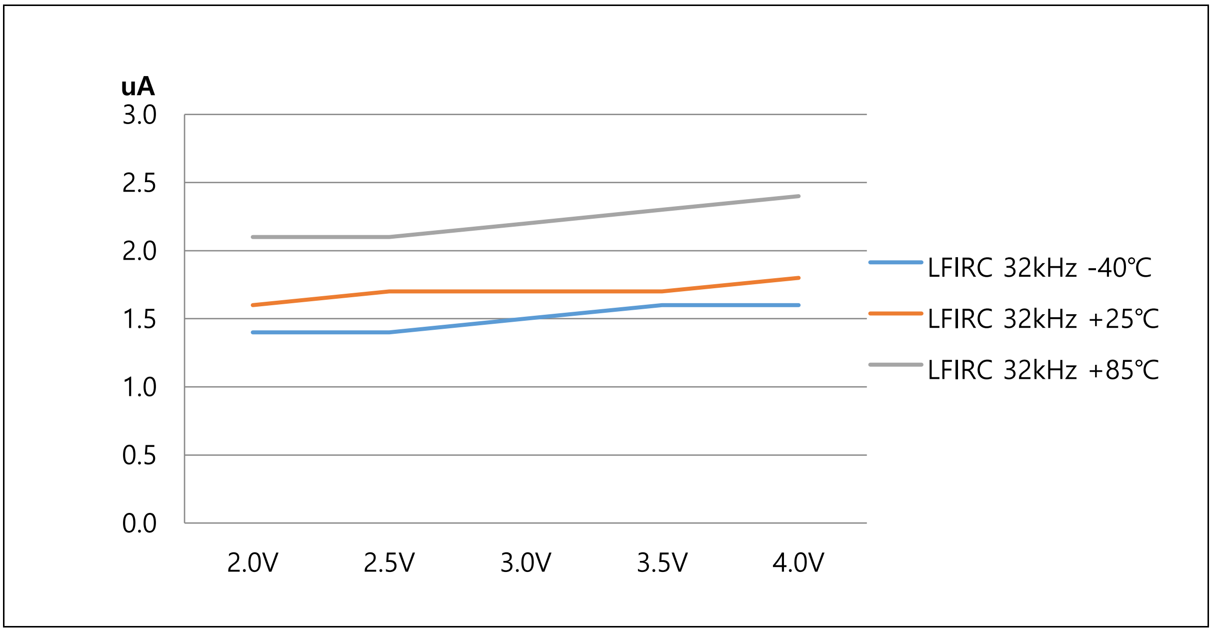


Figure 52. IDLE (IDD4) Current

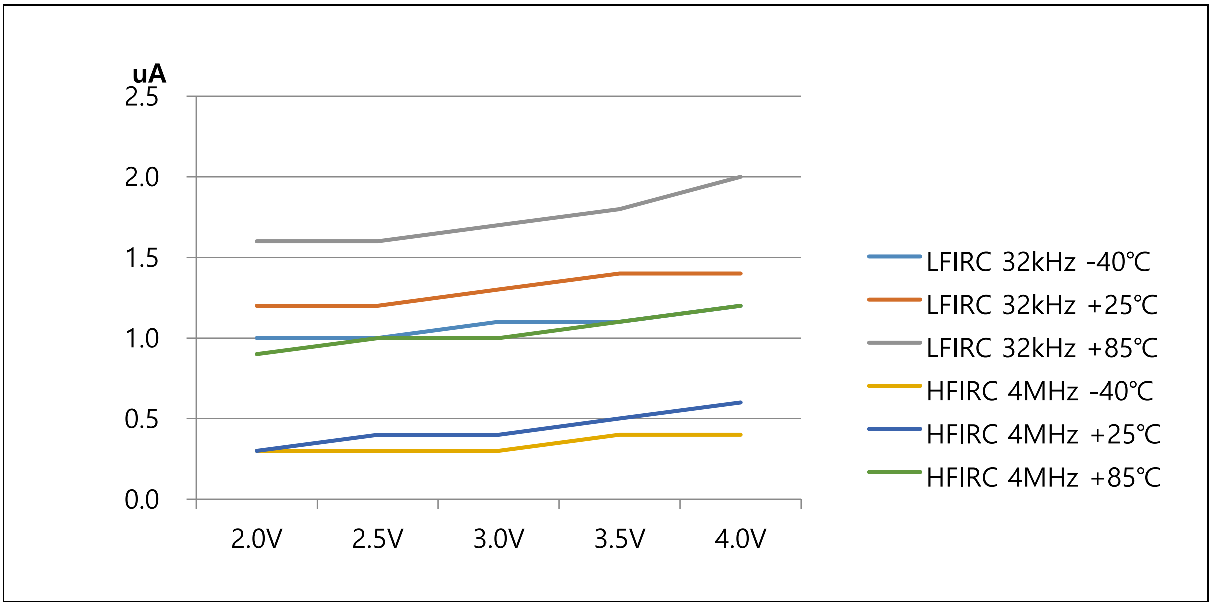


Figure 53. STOP (IDD5) Current

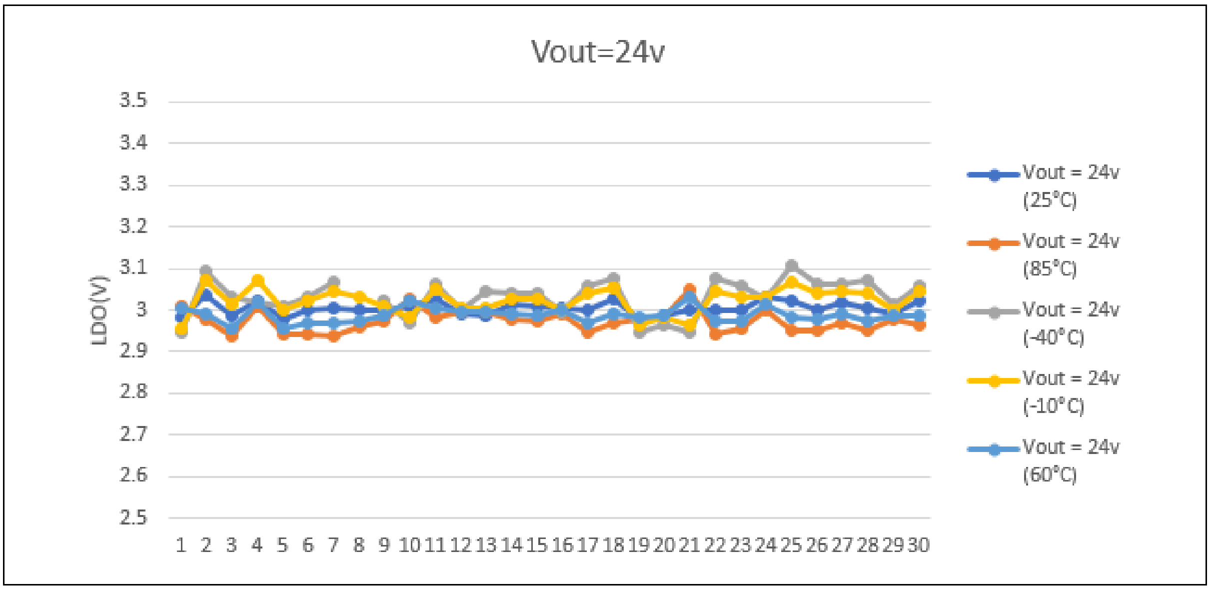


Figure 54. LDO Voltage of 30 Samples

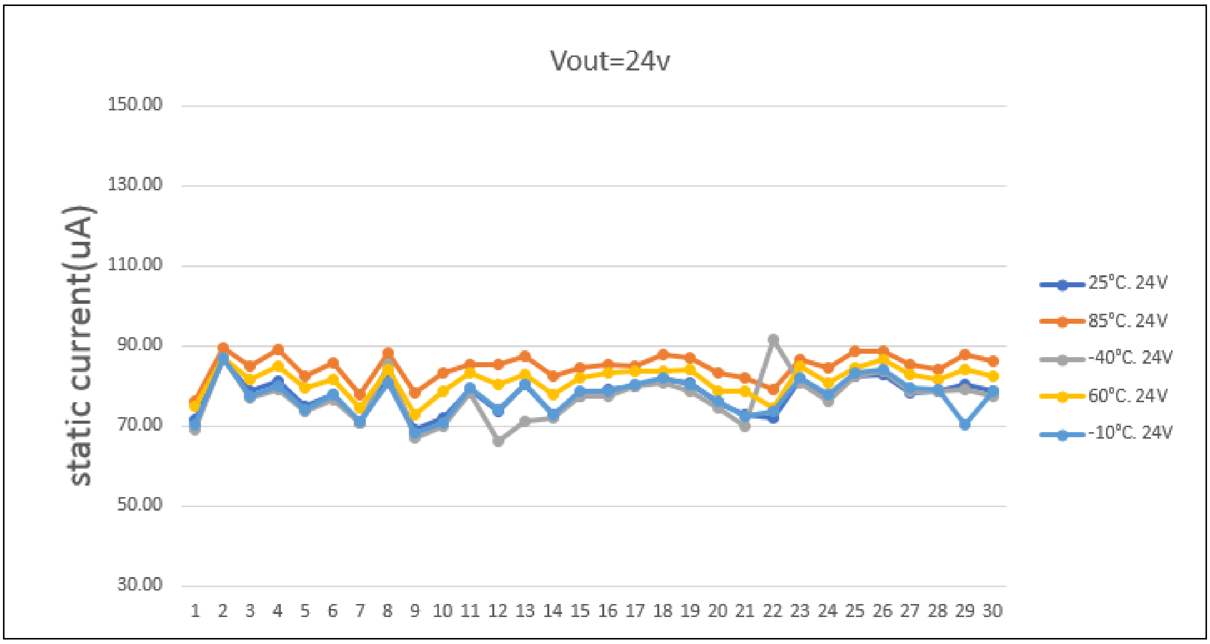
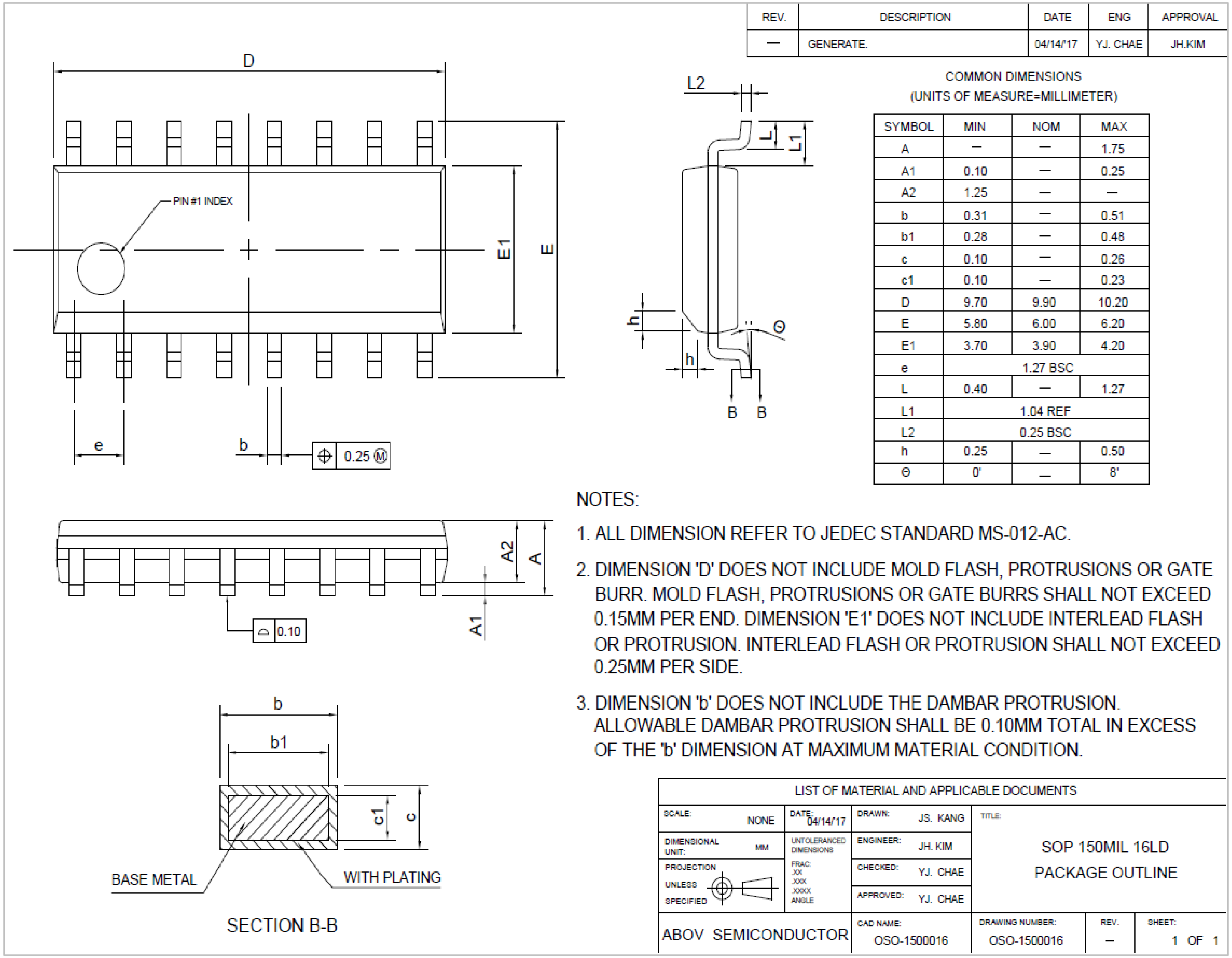


Figure 55. Static Current of 30 Samples

22 Package information

22.1 16 SOPN package information



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/14/'17	YJ. CHAE	JH.KIM

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
b1	0.28	—	0.48
c	0.10	—	0.26
c1	0.10	—	0.23
D	9.70	9.90	10.20
E	5.80	6.00	6.20
E1	3.70	3.90	4.20
e	1.27 BSC		
L	0.40	—	1.27
L1	1.04 REF		
L2	0.25 BSC		
h	0.25	—	0.50
Θ	0°	—	8°

NOTES:

1. ALL DIMENSION REFER TO JEDEC STANDARD MS-012-AC.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. DIMENSION 'b' DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

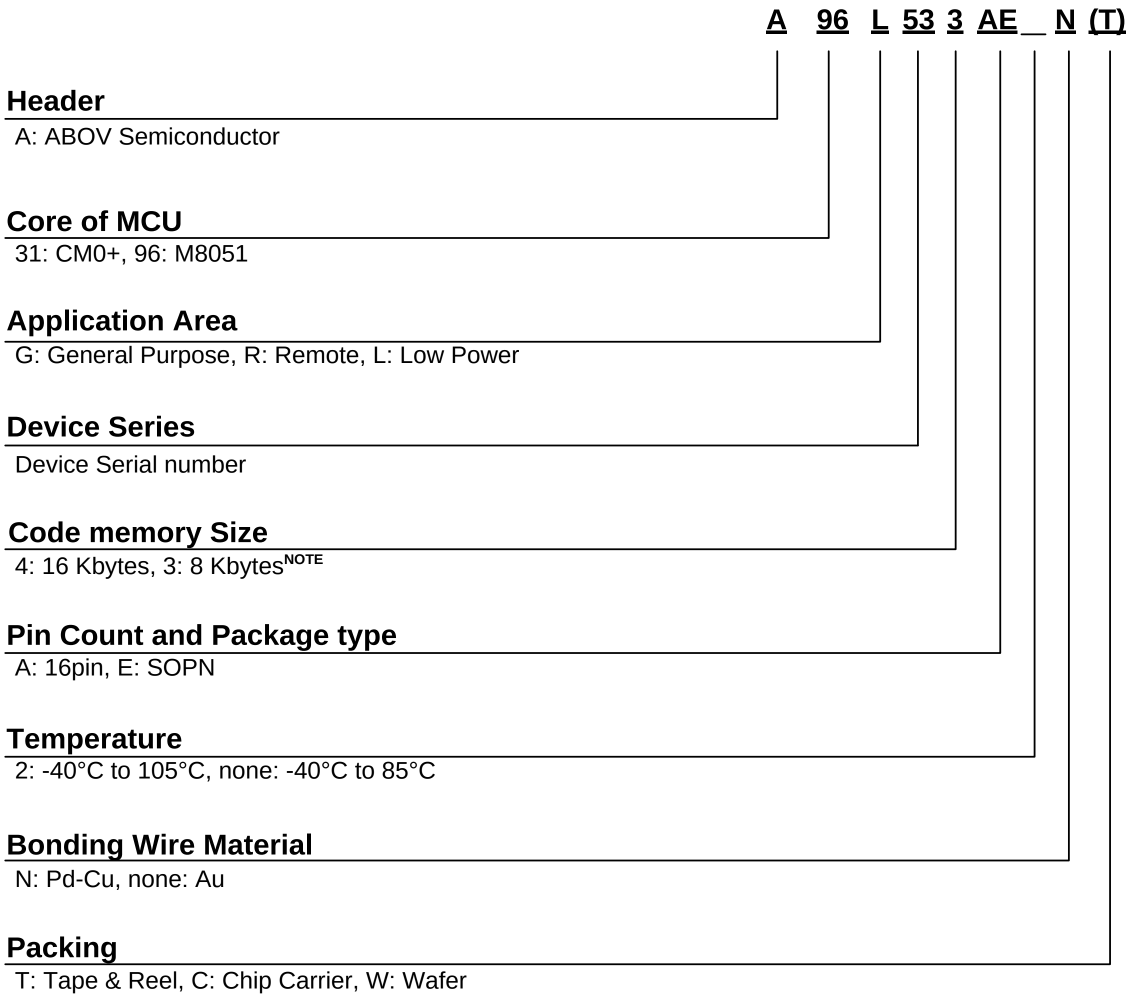
SCALE: NONE
DATE: 04/14/'17
DRAWN: JS. KANG
TITLE: SOP 150MIL 16LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM
UNTOLERANCED DIMENSIONS
FRAC:
.XX
.XXX
.XXXX
ANGLE
ENGINEER: JH. KIM
PROJECTION UNLESS SPECIFIED
CHECKED: YJ. CHAE
APPROVED: YJ. CHAE
ABOV SEMICONDUCTOR
CAD NAME: OSO-1500016
DRAWING NUMBER: OSO-1500016
REV. —
SHEET: 1 OF 1

Figure 56. 16 SOPN Package Outline

23 Ordering information

Table 34. A96L53x Device Ordering Information

Device name	Flash	IRAM/XRAM	Data Flash	ADC	I/O ports	Package type
A96L533AE	8 Kbytes	256/256bytes	256bytes	5 inputs	12	16 SOPN
A96L534AE	16 Kbytes	256/768bytes	256bytes	5 inputs	12	16 SOPN



Header
A: ABOV Semiconductor

Core of MCU
31: CM0+, 96: M8051

Application Area
G: General Purpose, R: Remote, L: Low Power

Device Series
Device Serial number

Code memory Size
4: 16 Kbytes, 3: 8 Kbytes[NOTE]

Pin Count and Package type
A: 16pin, E: SOPN

Temperature
2: -40°C to 105°C, none: -40°C to 85°C

Bonding Wire Material
N: Pd-Cu, none: Au

Packing
T: Tape & Reel, C: Chip Carrier, W: Wafer

NOTE In special ordering, the code memory size may be different from other MCUs. For more information on any aspect of this device, please contact your nearest distributor or ABOV sales office.

Figure 57. A96L53x Device Numbering Nomenclature

24 Development tools

This chapter introduces wide range of development tools for A96L53x. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

24.1 Compiler

ABOV semiconductor does not provide any compiler for A96L53x. However, since A96L53x has Mentor 8051 as its CPU core, you can use all kinds of third party's standard 8051 compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Please visit our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

24.2 OCD (On-Chip Debugger) emulator and debugger

The OCD emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means the OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the OCD is provided in **24.5 Circuit design guide**. More detailed information about the OCD, please visit our website www.abovsemi.com and download the debugger S/W and documents.

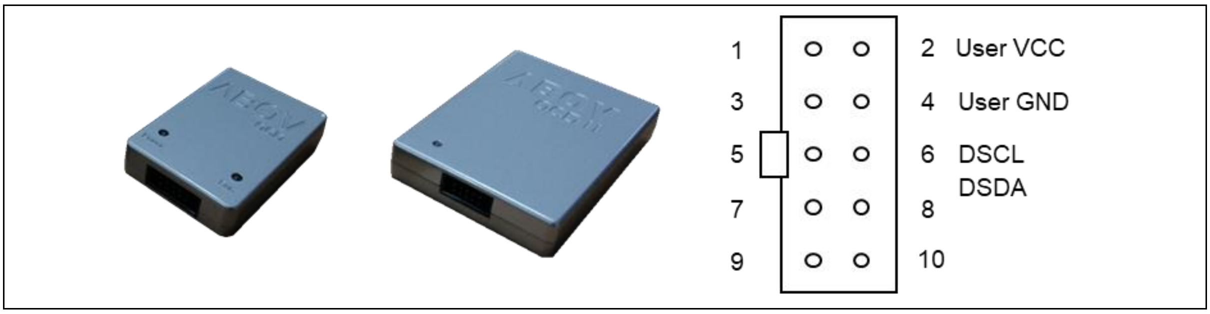


Figure 58. OCD and Pin Descriptions

Following is the OCD mode connections:

- DSCL (A96L53x P12 port)
- DSDA (A96L53x P13 port)

24.3 Programmer

24.3.1 E-PGM+

E-PGM+ is a single programmer, and allows users to program on the device directly.

- Support ABOV / ADAM devices
- 2 to 5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

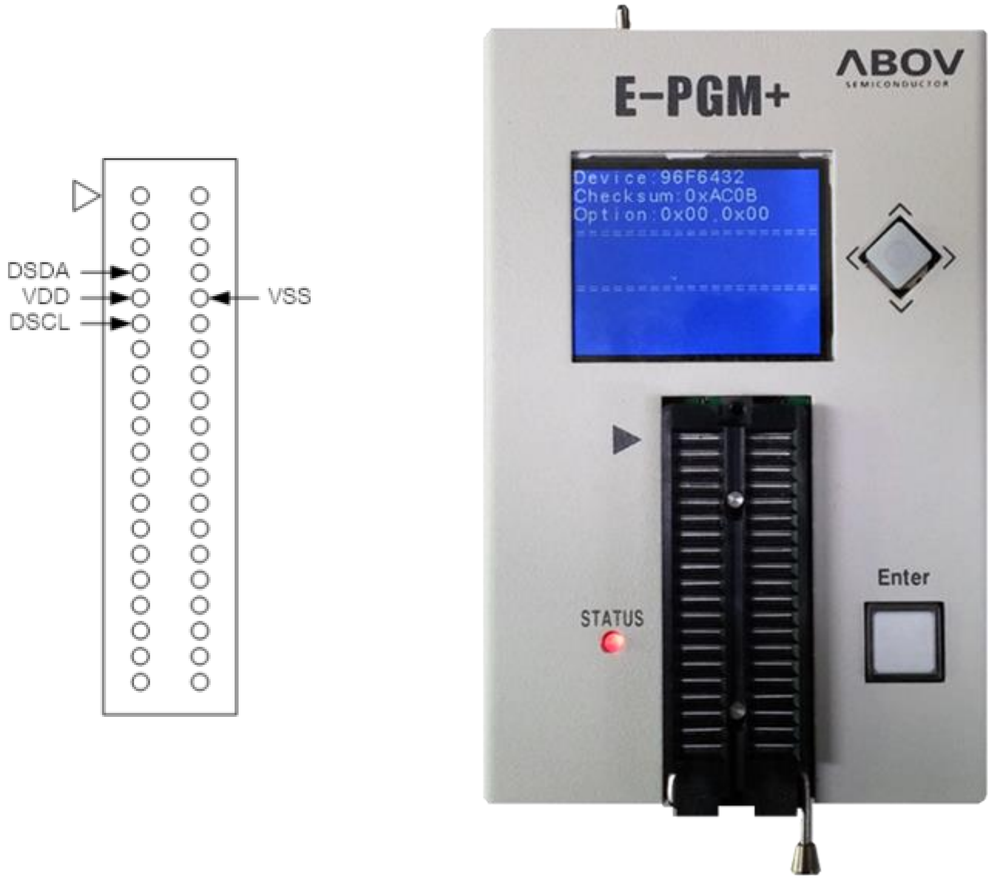


Figure 59. E-PGM+ (Single Writer) and Pin Descriptions

24.3.2 OCD emulator

OCD emulator allows users to write code on the device too, since the OCD debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

24.3.3 Gang programmer

E-Gang4 and E-Gang6 allow users to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Table 35. Specification of E-Gang4 and E-Gang6

Gang programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x35mm	148.2 x 22.5 x35mm
Weight	2.0kg	2.8kg
Input voltage	DC Adaptor 15V/2A	DC Adaptor 15V/2A
Operating temperature	-10 to 40℃	-10 to 40℃
Storage temperature	-30 to 80℃	-30 to 80℃
Water proof	No	No

Figure 60. E-Gang4 and E-Gang6 (for Mass Production)

24.4 MTP programming

Program memory of A96L53x is an MTP type. This Flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format.

Table 36 introduces each pin and corresponding I/O status.

Table 36. Pins for MTP Programming

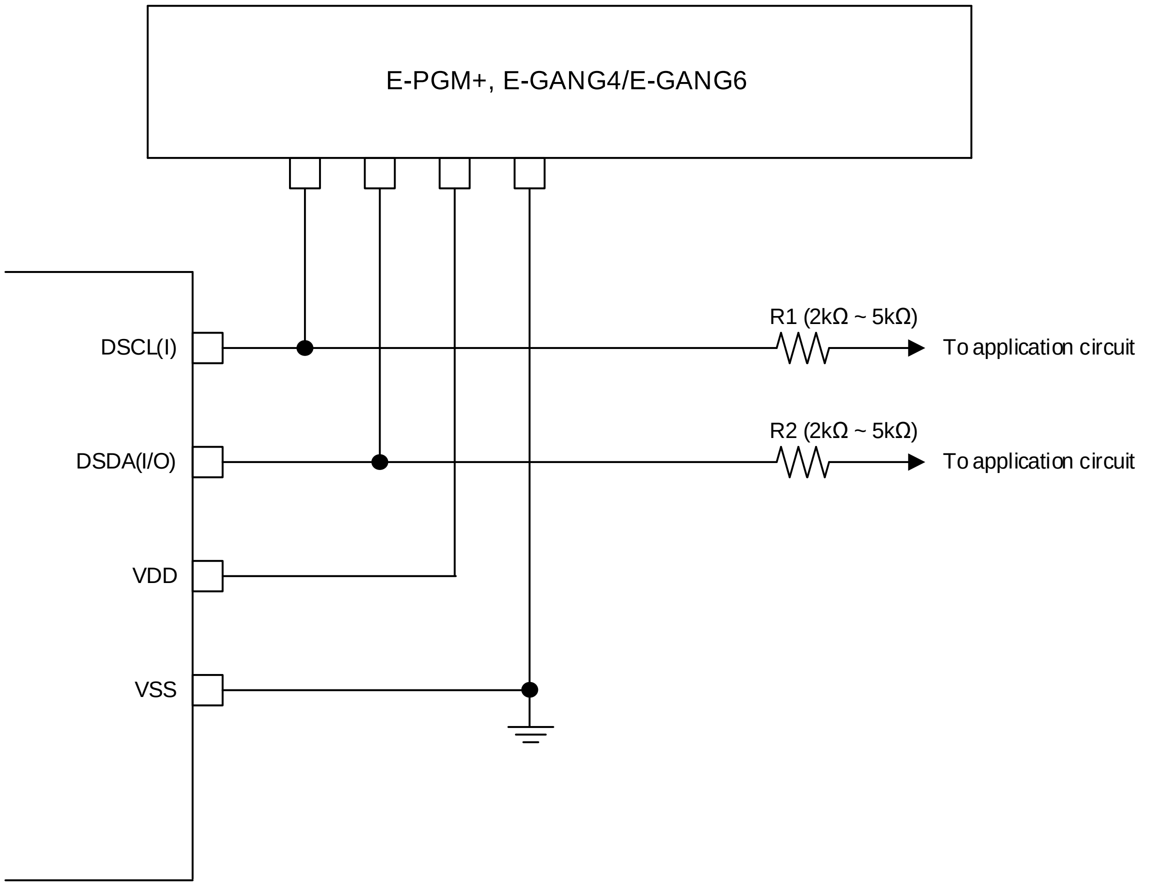
Pin name	**Main chip pin name**	**During programming**	
		I/O	**Description**
DSCL	P12	I	Serial clock pin. Input only pin.
DSDA	P13	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

24.4.1 On-board programming

A96L53x needs only four signal lines including VDD and VSS pins for programming Flash with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

24.5 Circuit design guide

When programming Flash memory, the programming tool needs 4 signal lines; DSCL, DSDA, VDD, and VSS. When designing a PCB circuit, users should consider the usage of these 4 signal lines for the on-board programming.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 61. PCB Design Guide for On-Board Programming

24.5.1 On-Chip Debug system

Detail descriptions for programming via the OCD interface can be found in the following figure. Table 37 introduces features of the OCD and Figure 62 shows a block diagram of the OCD interface and the On-chip Debug system.

Table 37. Features of OCD

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and Data Flash memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, Data Flash, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

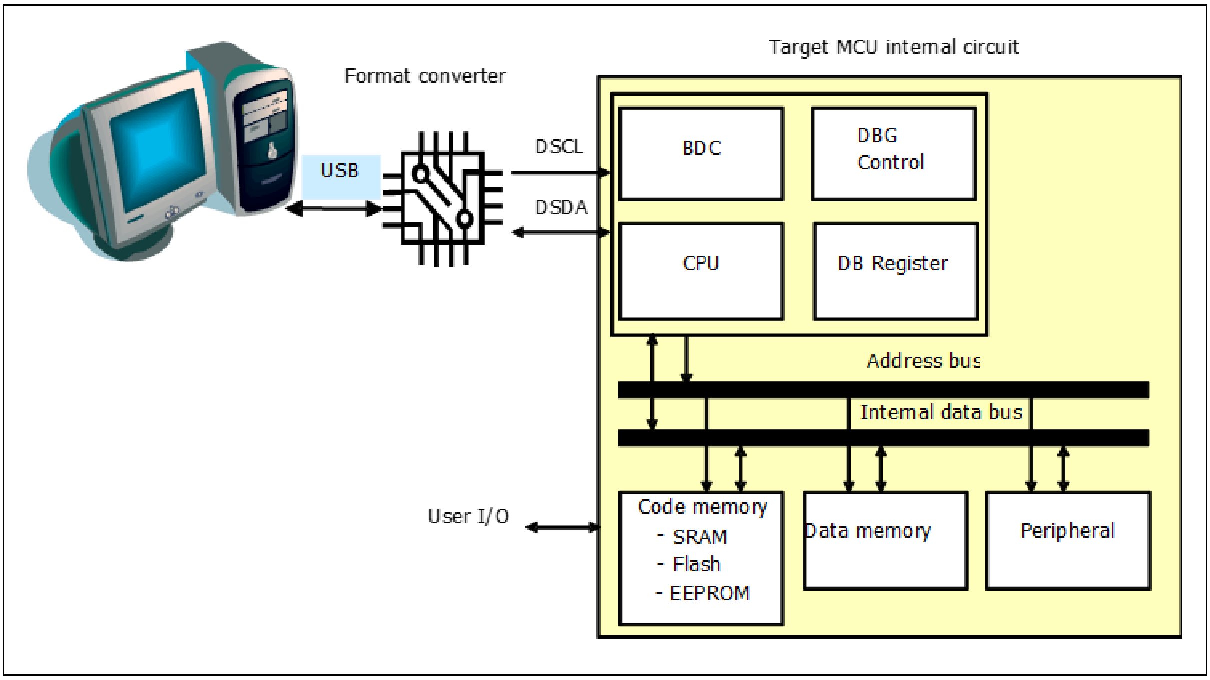


Figure 62. On-Chip Debugging System in Block Diagram

24.5.2 Two-pin external interface

Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of ‘1’ for 8-bit data in transmitter.
- Receiver generates acknowledge bit as ‘0’ when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is ‘1’ at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

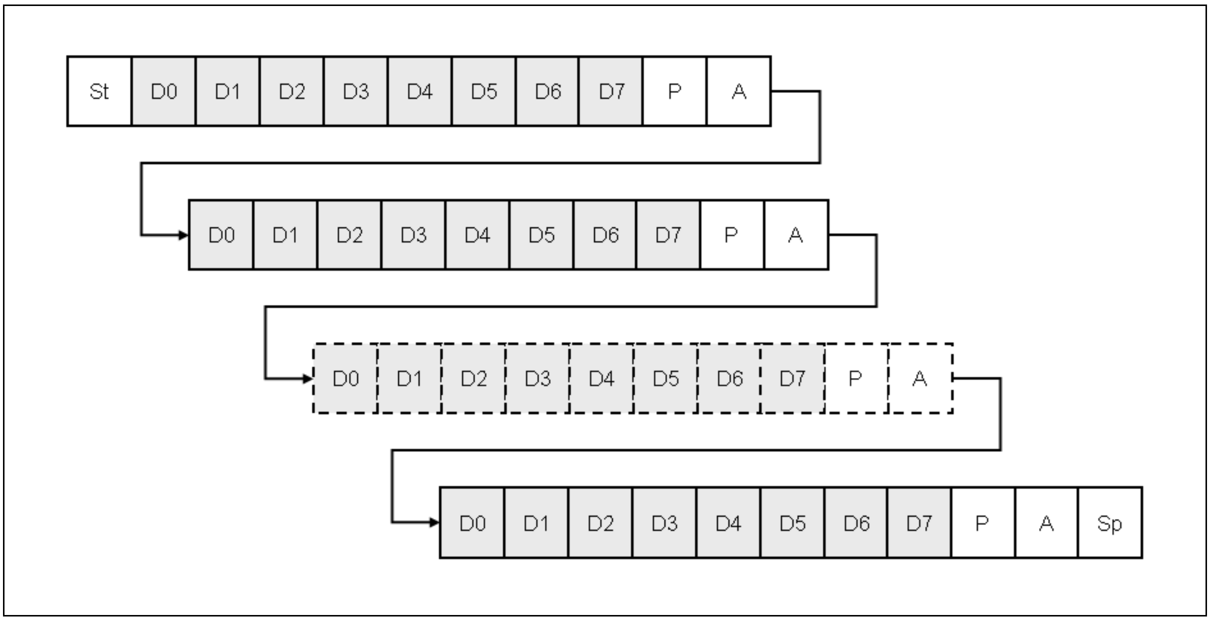


Figure 63. 10-bit Transmission Packet

Packet transmission timing

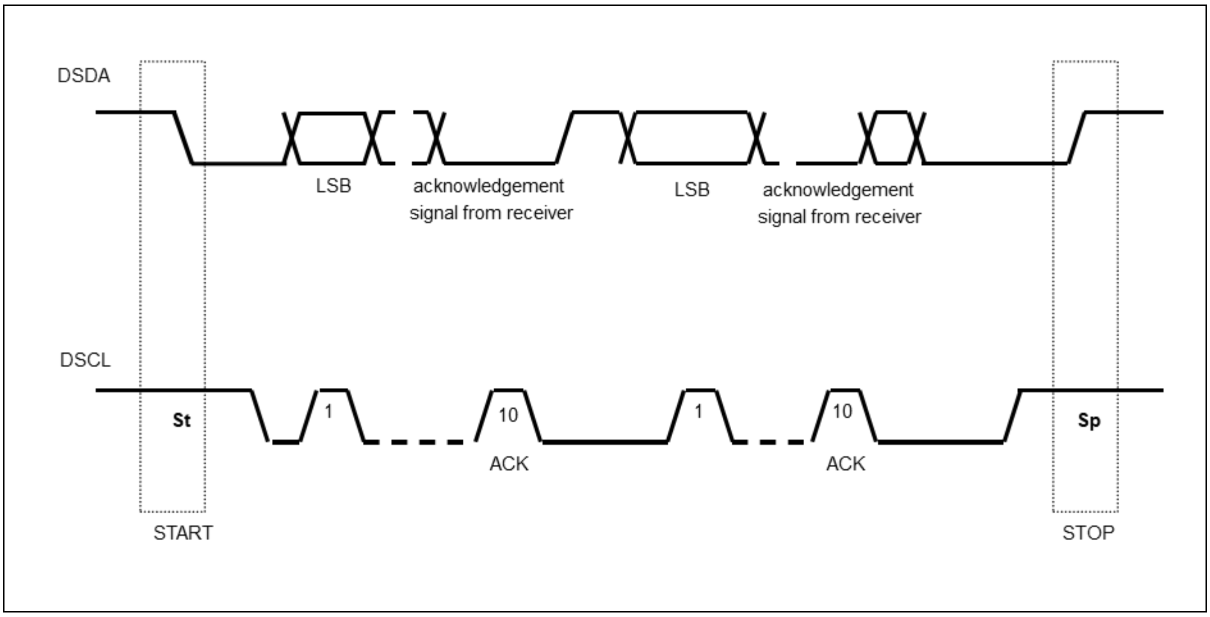


Figure 64. Data Transfer on Twin Bus

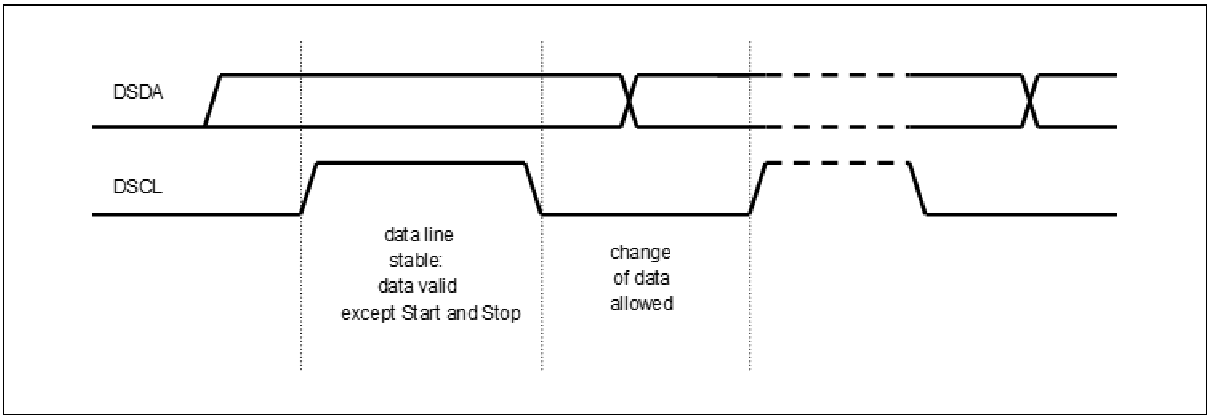


Figure 65. Bit Transfer on Serial Bus

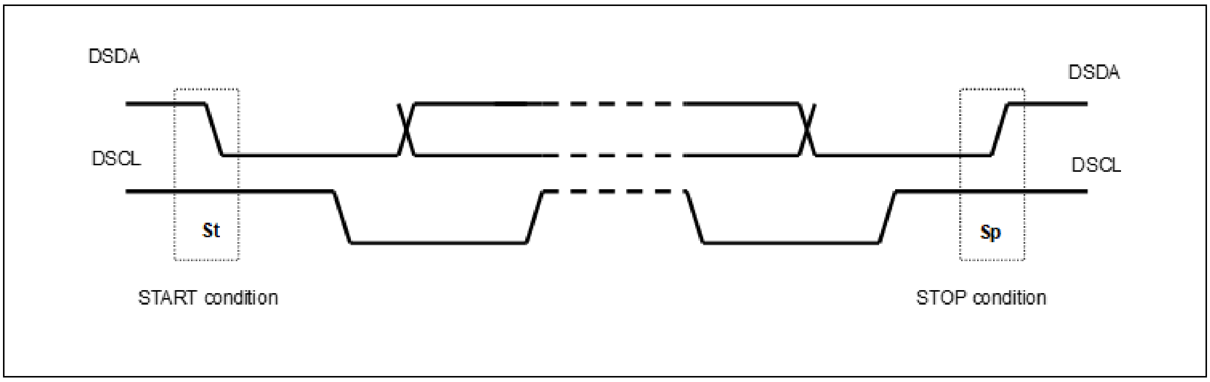


Figure 66. Start and Stop Condition

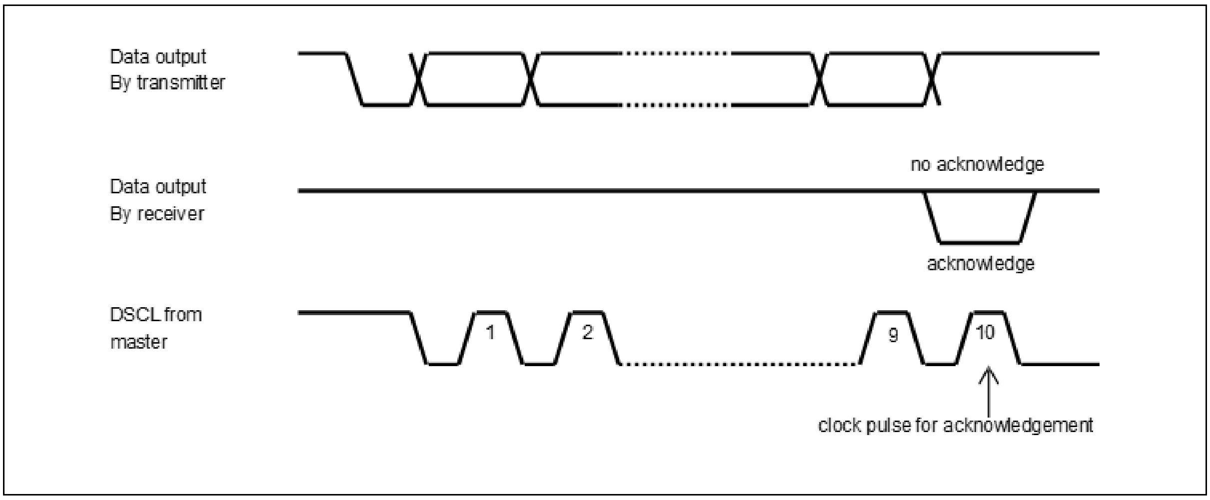


Figure 67. Acknowledge on Serial Bus

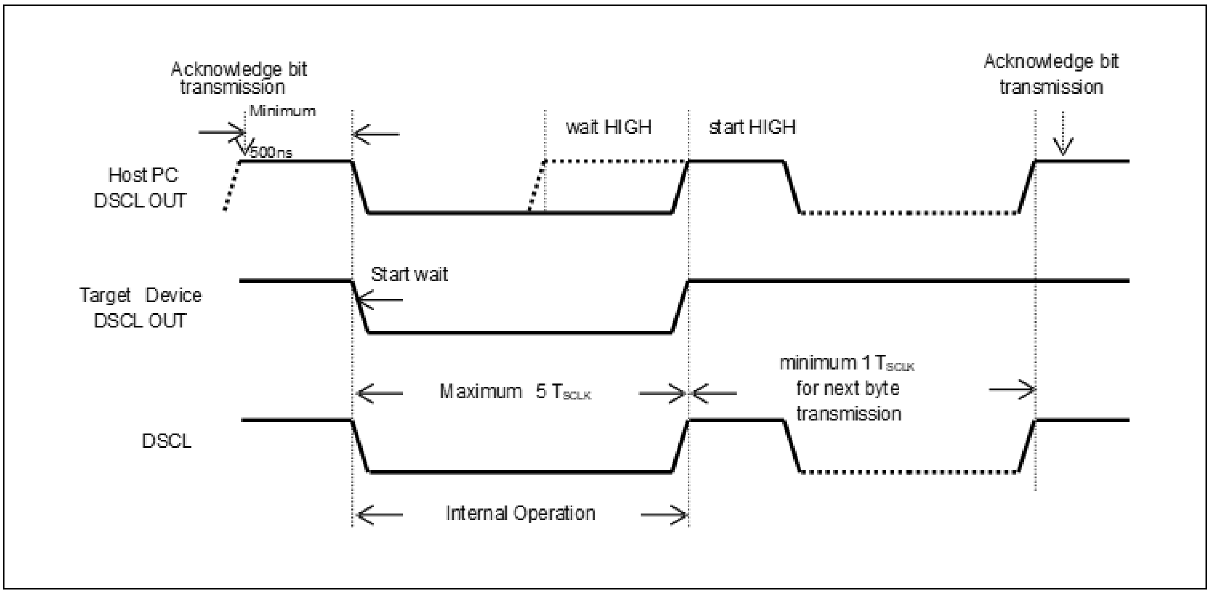


Figure 68. Clock Synchronization during Wait Procedure

24.5.3 Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

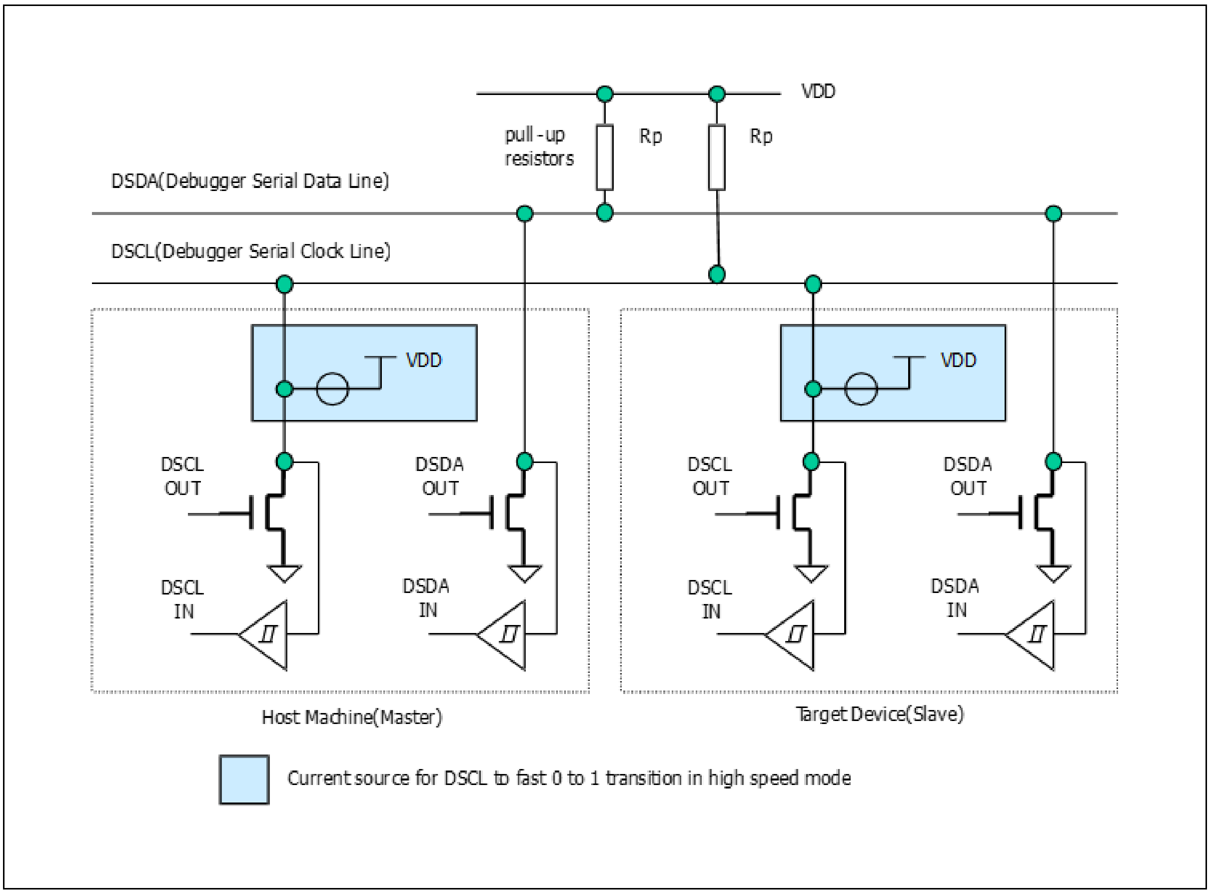


Figure 69. Connection of Transmission

24.5.4 Example circuit

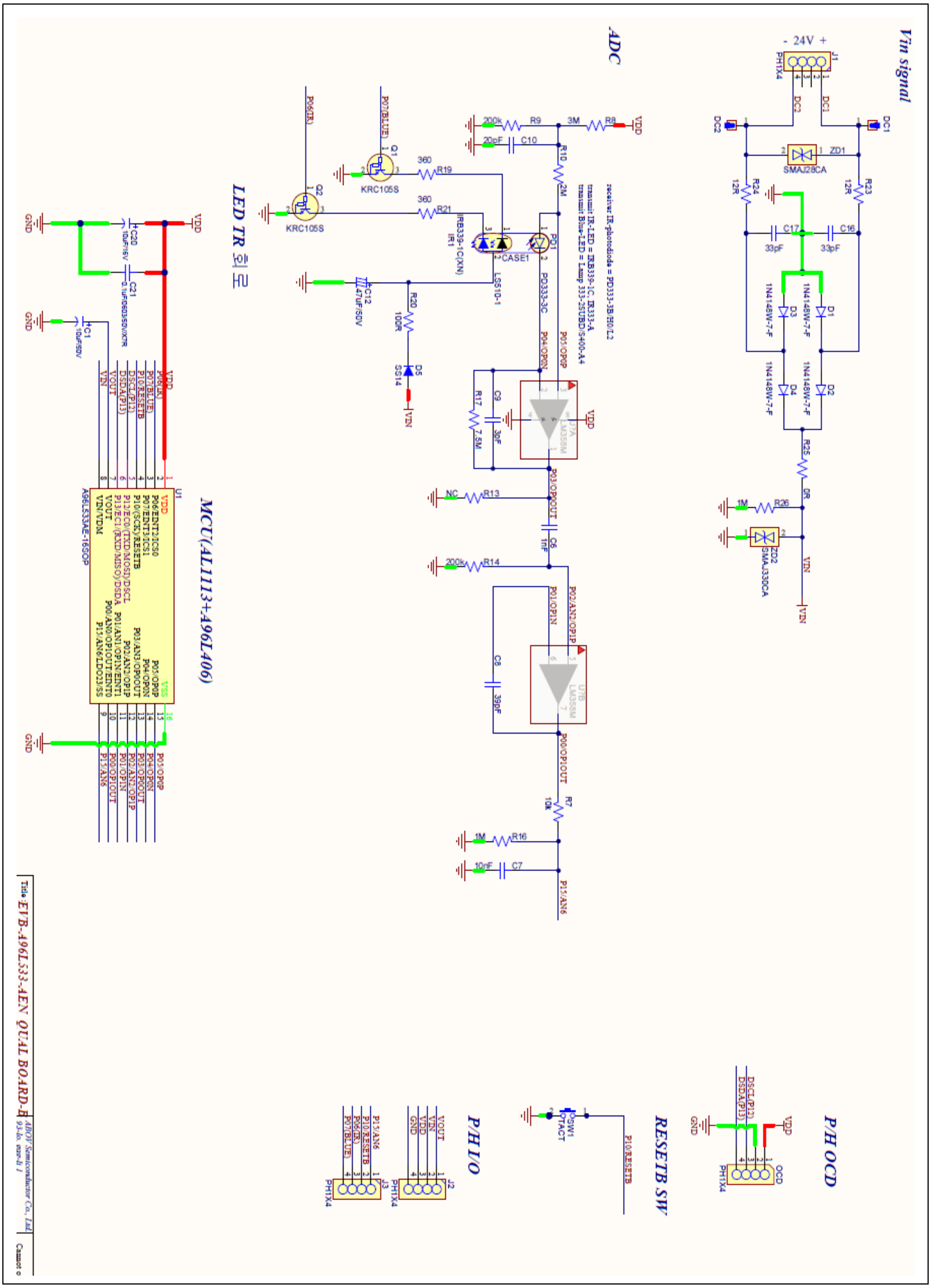


Figure 70. Example Circuit using IR LED and Blue LED

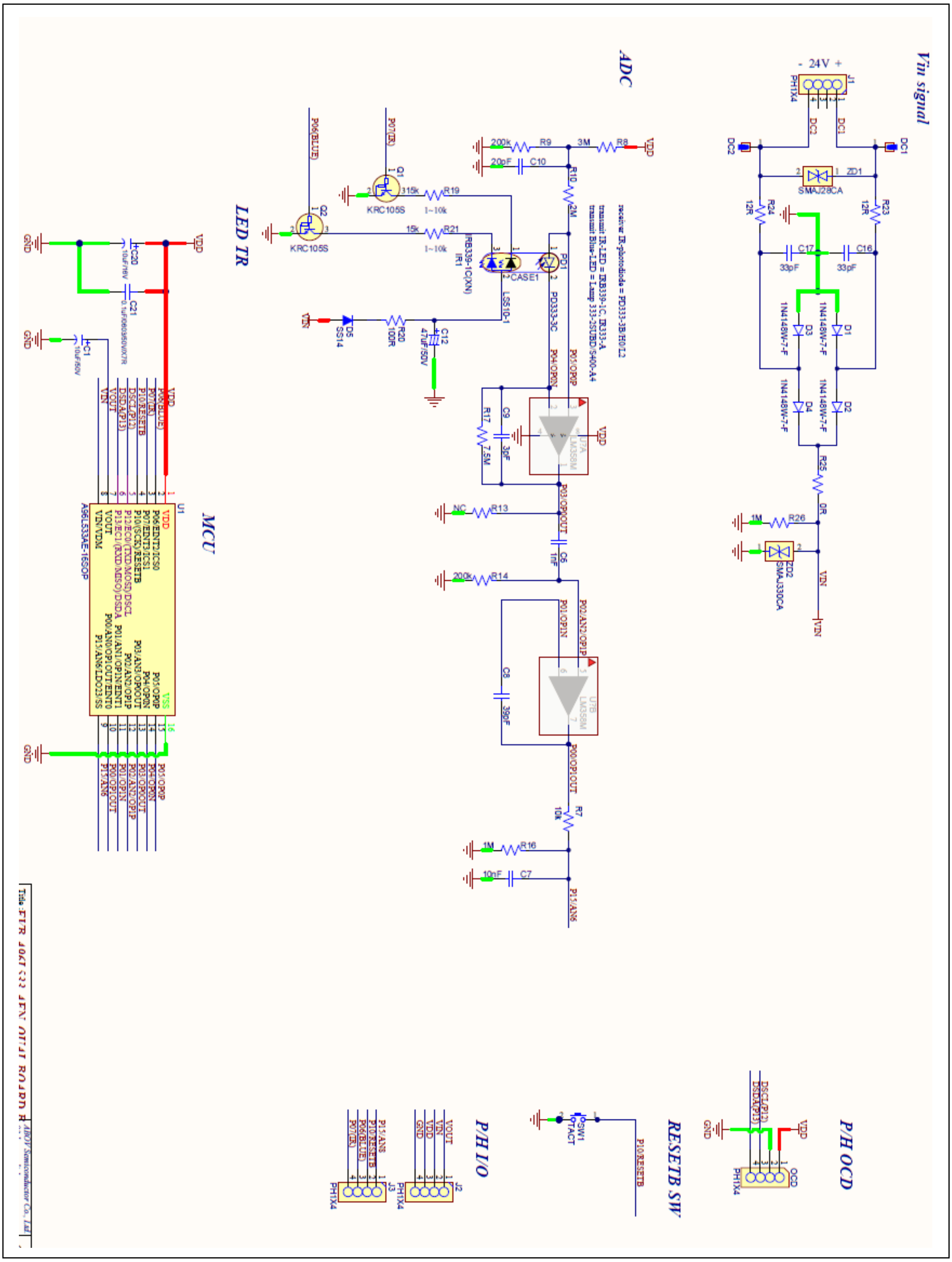


Figure 71. Example Circuit using only IR LED

Appendix

A. Configure option

Register description: configure option control

CONFIGURE OPTION 1: ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value: 00H

R_P	Code Read Protection	
	0	Disable
	1	Enable
HL	Code Write Protection	
	0	Disable
	1	Enable
VAPEN	Vector Area (00H – FFH) Write Protection	
	0	Disable Protection (Erasable by instruction)
	1	Enable Protection (Not erasable by instruction)
RSTS	Select RESETB pin	
	0	Disable RESETB pin (P10)
	1	Enable RESETB pin

CONFIGURE OPTION 2 for 16 Kbytes Flash memory: ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN	Enable Specific Area Write Protection	
	0	Disable (Erasable by instruction)
	1	Enable (Not erasable by instruction)

PASS [2:0] Select Specific Area for Write Protection

NOTE: When PAEN = ‘1’, it is applied.

PASS2	PASS1	PASS0	
0	0	0	0.7 Kbytes (Address 0100H – 03FFH)
0	0	1	1.7 Kbytes (Address 0100H – 07FFH)
0	1	0	2.7 Kbytes (Address 0100H – 0BFFH)
0	1	1	3.8 Kbytes (Address 0100H – 0FFFH)
1	0	0	13.7 Kbytes (Address 0100H – 37FFH)
1	0	1	14.7 Kbytes (Address 0100H – 3BFFH)
1	1	0	15.2 Kbytes (Address 0100H – 3DFFH)
1	1	1	15.5 Kbytes (Address 0100H – 3EFFH)

CONFIGURE OPTION 2 for 8 Kbytes Flash memory: ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN Enable Specific Area Write Protection

0 Disable (Erasable by instruction)

1 Enable (Not erasable by instruction)

PASS [2:0] Select Specific Area for Write Protection

NOTE: When PAEN = ‘1’, it is applied.

PASS2	PASS1	PASS0	
0	0	0	0.7 Kbytes (Address 0100H – 03FFH)
0	0	1	1.7 Kbytes (Address 0100H – 07FFH)
0	1	0	2.7 Kbytes (Address 0100H – 0BFFH)
0	1	1	3.8 Kbytes (Address 0100H – 0FFFH)
1	0	0	5.7 Kbytes (Address 0100H – 17FFH)
1	0	1	6.7 Kbytes (Address 0100H – 1BFFH)
1	1	0	7.2 Kbytes (Address 0100H – 1DFFH)
1	1	1	7.5 Kbytes (Address 0100H – 1EFFH)

B. Instruction table

- Instructions are either 1, 2 or 3bytes long as listed in the ‘Bytes’ column in tables shown below.
- Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following tables in this section.
- 1 machine cycle comprises 2 system clock cycles.

Table 38. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 39. Instruction Table: Logical

Logical				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 40. Instruction Table: Data Transfer

Data Transfer				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 41. Instruction Table: Boolean

Boolean				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 42. Instruction Table: Branching

Branching				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 43. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

Table 44. Instruction Table: Additional Instructions

Additional instructions (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, and the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

Revision history

Version	Date	Description
1.00	Dec.11, 2020	First creation
1.01	Aug. 19.2021	Fixed OP-AMP 0/1 Total current
1.02	Oct. 12. 2021	Fixed VRXH2 values
1.03	Nov. 10. 2022	Revised the font of this document

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
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