A96L623 Datasheet

SoC for Purpose of Fire Safety System 8-bit MCU, Power Line Transceiver, 10-bit ADC, and OP-Amp

DS Rev. 1.10

Features

Core and memory

- 8-bit CISC M8051 core (8051 Compatible, 2 clocks per cycle)
- 8 Kbytes On-Chip FLASH (ISP)
- 256 bytes IRAM, 256 bytes XRAM
- 256 bytes Data flash

General Purpose I/O (GPIO)

- Normal I/O: 10 Port

Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watch Dog Timer (WDT) 8-bit × 1-ch
- 16-bit × 3-ch (T0/T1/T2)

Programmable Pulse Generation

- Pulse generation (by T0/T1/T2)

Line Interface

- Three Rx types and Five Tx modes

10-bit A/D Converter

- 5 Input channels
- Sample and hold circuit

Operational Amplifier

- 2 channels, Rail-to-rail output

USART (UART + SPI)

- 8-bit UART × 1-ch or 8-bit SPI × 1-ch

Constant Sink Current Generator

- 2 channels, 16-step selectable
- Max. 287mA sink current

Temperature Sensor

- Frequency variation: 3.2 kHz/°C

16-bit CRC/Checksum Generator

Power on Reset

- Reset release level (1.4V)

Low Voltage Reset

Level detection (2.4V)

Interrupt Sources

- External Interrupts (EINT0/1/11/12)(4)
- Timer(0/1/2) (3), WDT (1), BIT (1), TS (1)
- USART RX/TX (2), ADC (1), TXI/RXI (2)

Internal RC Oscillator

- 4MHz ±3.0% (T_A=-40~ +85°C)

Power down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- VIN: 8.5V to 42V (@0.5 to 4MHz with IRC)

Built-In Power Line Transceiver

- Up to 42V VIN input voltage
- Comparator for line interface Rx
- Tr for line interface Tx
- 5.0V LDO for VDD

Operating Temperature

- –40 ~ +85℃

Package Type

- 16 SOPN, Pb-free package

Product selection table

Table 1. Device Summary

Part number	Flash	IRAM/ XRAM	Data Flash	USART	Line Interface	Timer	ICS	Op-Amp	ADC	I/O	PLT	Package
A96L623AE	8KB	256/256B	256B	1	1	3	2	2	5ch	10	1	16 SOPN

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1 Description

A96L623 is an advanced CMOS 8-bit microcontroller with a power line transceiver. It has 8Kbytes of FLASH, 256bytes data flash, 5V LDO for power of core and peripherals. This is a powerful SoC device which provides low power consumption and cost effect solution to smoke detector applications. A96L623 supports power down modes reducing power consumption.

Table 2 introduces features of A96L623 and peripheral counts.

1.1 Device overview

Table 2. A96L623 Device Features and Peripheral Counts

Peripheral		**A96L623**
CPU		8-bit CISC core (M8051, 2 clocks per cycle)
Flash		8 Kbytes with self r/w capability On chip debug and ISP Endurance: 10,000 cycles
IRAM		256 bytes
XRAM		256 bytes
Data Flash		256 bytes Endurance: 100,000 cycles
GPIO		Normal I/Os 18 ports: P0[4:0], P1[4:0]
Timer/ counter		BIT 8-bit x 1-ch WDT 8-bit x 1-ch: 1KHz internal RC oscillator for WDT 16-bit x 3-ch (T0/T1/T2)
Programmable pulse generation		Pulse generation (by T0/T1/T2)
ADC		10-bit ADC, 5 input channels
Operational amplifier		2-ch Rail-to-rail output
CRC and checksum generator		16-bit Auto and user CRC/ checksum mode
Reset	Power on reset	Reset release level (1.4V)
	Low voltage reset	Level detection (2.4V)
Constant sink current generator		2-ch 16-steps selectable Max. 287mA sink current

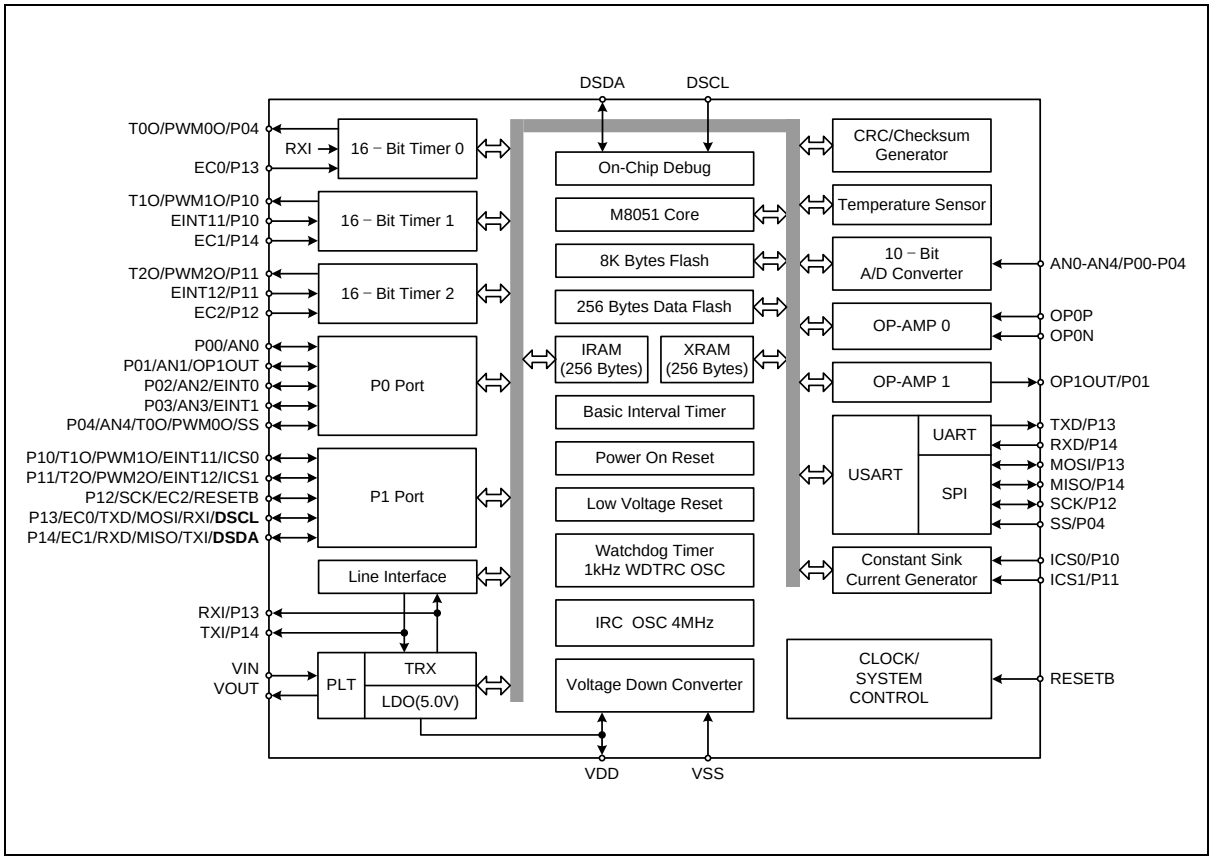
Table 2. A96L623 Device Features and Peripheral Counts (continued)

Peripheral	A96L623
USART	UART + SPI 8-bit UART x 1-ch 8-bit SPI x 1-ch
Temperature sensor	Frequency variation: 3.2 kHz/℃
Interrupt sources	External interrupts: EINT0/1/11/12, 4 Timer0/1/2, 3 WDT, 1 BIT, 1 ADC, 1 USART Rx/ Tx, 2 TXI/RXI, 2 TS, 1
Internal RC oscillator	4MHz ± 3.0% (TA = -40℃ to +85℃)
Power down mode	STOP, IDLE
Operating voltage and frequency	VIN: 8.5V to 42V @ 0.5 to 4.0MHz with IRC Voltage dropout converter included for core
Minimum instruction execution time	0.25us @ 4MHz IRC
Built-in Power Line Transceiver	Up to 42V VIN input voltage Comparator for line interface Rx Tr for line interface Tx 5.0V ± 1.0% (TA = +25℃) LDO for VDD
Operating temperature	-40℃ to +85℃
Package type	16 SOPN Pb-free package

1.2 Block diagram

Figure 1 describes A96L623 in a block diagram.

Figure 1. A96L623 Block Diagram

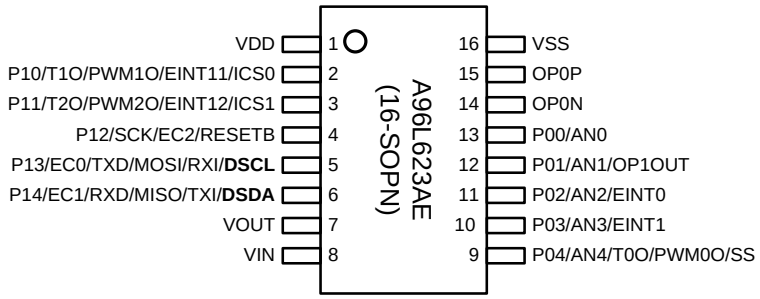


2 Pinouts and pin descriptions

In this chapter, A96L623 pinouts and pin descriptions are introduced.

2.1 Pinouts

Figure 2. A96L623AE 16 SOPN Pinouts



NOTE:

1. For the On-Chip Debugging, ISP assigns P1[3:4] pins for DSCL and DSDA respectively.

2.2 Pin description

Table 3. 16 SOPN Pin Description

Pin name	I/O	Function	@reset	Shared with
P00	I/O	The port 0 is a bit-programmable I/O port which can be configured as an input (P02/P03: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0
P01				AN1/OP1OUT
P02				AN2/EINT0
P03				AN3/EINT1
P04				AN4/T0O/PWM0O/SS
P10	I/O	The port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	T1O/PWM1O/EINT11/ICS0
P11				T2O/PWM2O/EINT12/ICS1
P12				SCK/EC2/RESETB
P13				EC0/TXD/MOSI/RXI/DSCL
P14				EC1/RXD/MISO/TXI/DSDA
EINT0	I/O	External interrupt inputs	Input	P02/AN2
EINT1				P03/AN3
EINT11	I/O	External interrupt input and Timer 1 capture input		P10/T1O/PWM1O/ICS0
EINT12	I/O	External interrupt input and Timer 2 capture input		P11/T2O/PWM2O/ICS1
T0O	I/O	Timer 0 interval output	Input	P04/AN4/PWM0O/SS
T1O	I/O	Timer 1 interval output	Input	P10/PWM1O/EINT11/ICS0
T2O	I/O	Timer 2 interval output	Input	P11/PWM2O/EINT12/ICS1
PWM0O	I/O	Timer 0 pulse output	Input	P04/AN4/T0O/SS
PWM1O	I/O	Timer 1 pulse output	Input	P10/T1O/EINT11/ICS0
PWM2O	I/O	Timer 2 pulse output	Input	P11/T2O/EINT12/ICS1
EC0	I/O	Timer 0 event count input	Input	P13/TXD/MOSI/RXI/DSCL
EC1	I/O	Timer 1 event count input	Input	P14/RXD/MISO/TXI/DSDA
EC2	I/O	Timer 2 event count input	Input	P12/SCK/RESETB
DSCL	I/O	On chip debugger clock input	Input	P13/EC0/TXD/MOSI/RXI
DSDA	I/O	On chip debugger data input/output	Input	P14/EC1/RXD/MISO/TXI

Table 3. 16 SOPN Pin Description (continued)

Pin name	I/O	Function	@reset	Shared with
AN0	I/O	A/D converter analog input channels	Input	P00
AN1				P01/OP1OUT
AN2				P02/EINT0
AN3				P03/EINT1
AN4				P04/T0O/PWM0O/SS
OP0P	I	OP-AMP 0 positive input	Input	–
OP0N	I	OP-AMP 0 negative input	Input	–
OP1OUT	I/O	OP-AMP 1 output	Input	P01/AN1
TXD	I/O	UART data output	Input	P13/EC0/MOSI/RXI/DSCL
RXD	I/O	UART data input	Input	P14/EC1/MISO/TXI/DSDA
MOSI	I/O	SPI master output, slave input	Input	P13/EC0/TXD/RXI/DSCL
MISO	I/O	SPI master input, slave output	Input	P14/EC1/RXD/TXI/DSDA
SCK	I/O	SPI clock input/output	Input	P12/EC2/RESETB
SS	I/O	SPI slave select input	Input	P04/AN4/T0O/PWM0O
ICS0	I/O	Constant sink current pins	Input	P10/T1O/PWM1O/EINT11
ICS1				P11/T2O/PWM2O/EINT12
VOUT	–	High voltage power pin. A 4.7uF capacitor must be connected between this pin and VSS.	–	–
VIN	–	High voltage power pin. Connect to bridge output.	–	–
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P12/EC2/SCK
VDD	–	LDO voltage output. A 4.7uF capacitor must be connected between this pin and VSS.	–	–
VSS	–	Ground pin	–	–

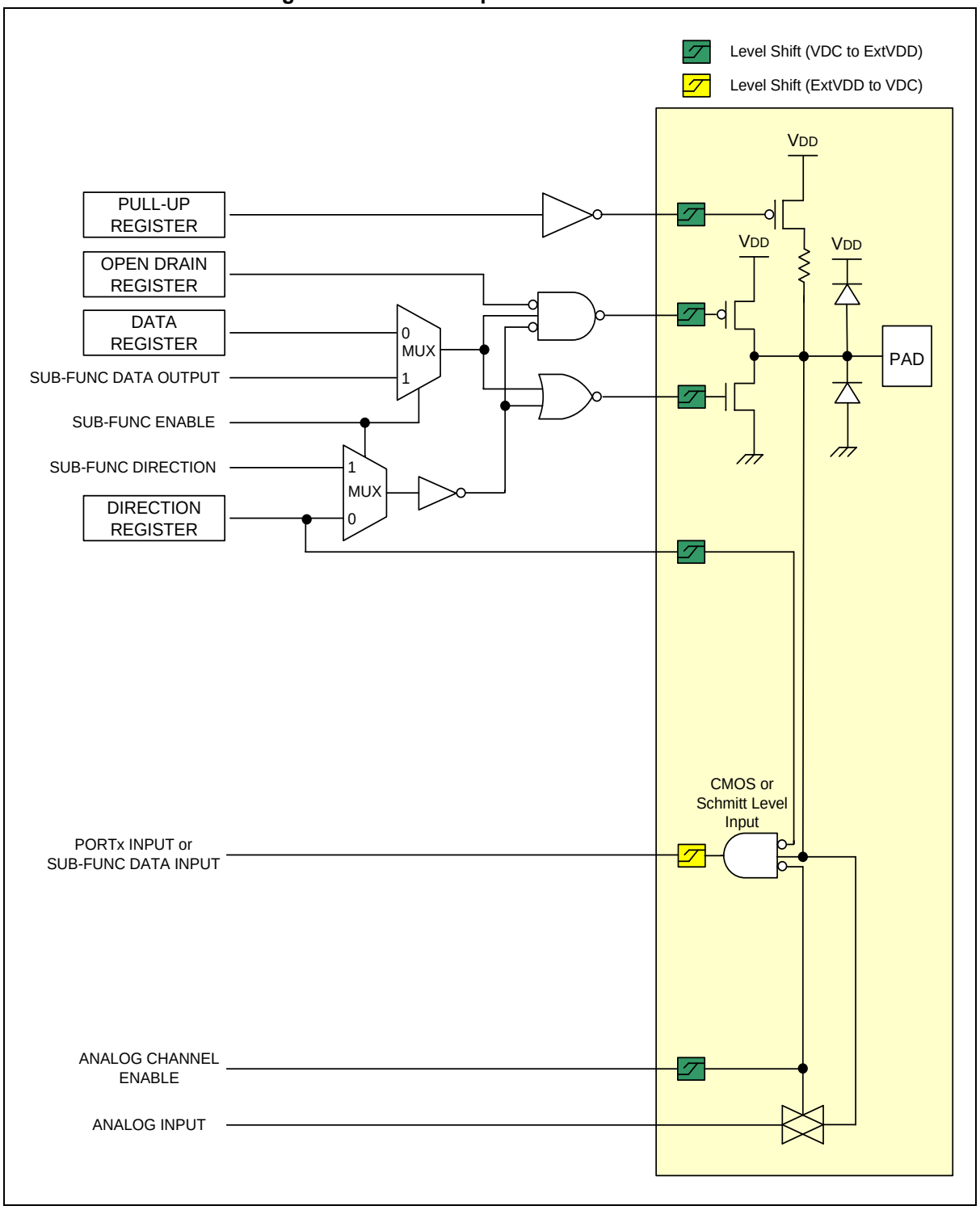
NOTES:

1. The P12/RESETB pin is configured as one of the P12/EC2/SCK and the RESETB pin by the “CONFIGURE OPTION”.
2. If the P14/DSDA and P13/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P14/DSDA and P13/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.

3 Port structures

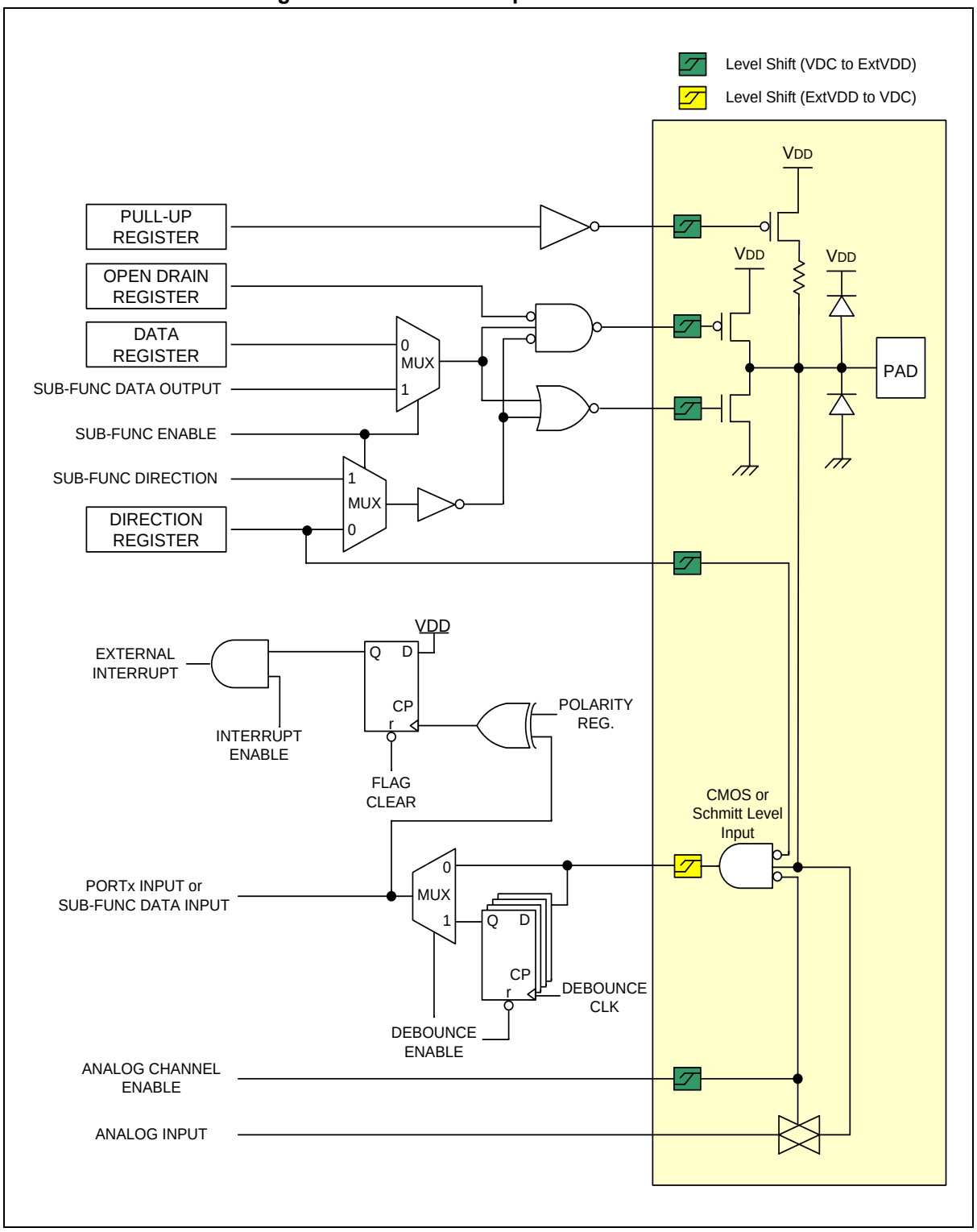
3.1 GPIO port structure

Figure 3. General Purpose I/O Port Structure



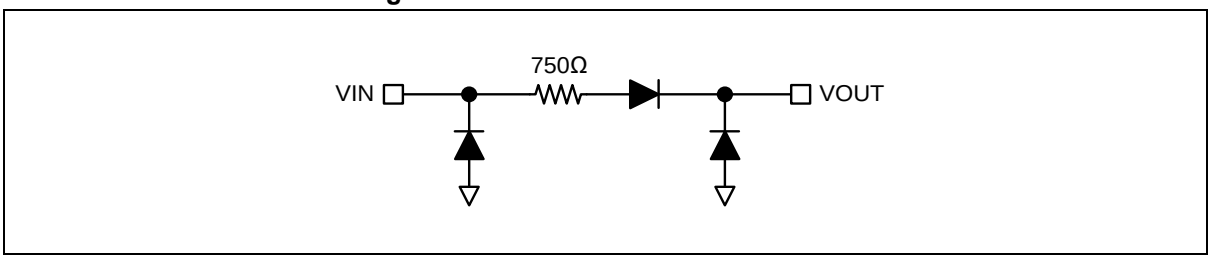
3.2 External interrupt I/O port structure

Figure 4. External Interrupt I/O Port Structure



3.3 VIN and VOUT port structure

Figure 5. VIN and VOUT Port Structure



4 Memory organization

A96L623 addresses three separate memory spaces:

- Program memory
- Data memory
- XRAM memory

By means of this logical separation of the memory, 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

A96L623 provides on-chip 8 Kbytes of the ISP type flash program memory, which is readable and writable. Internal data memory (IRAM) is 256 bytes and it includes the stack area. External data memory (XRAM) is 256 bytes.

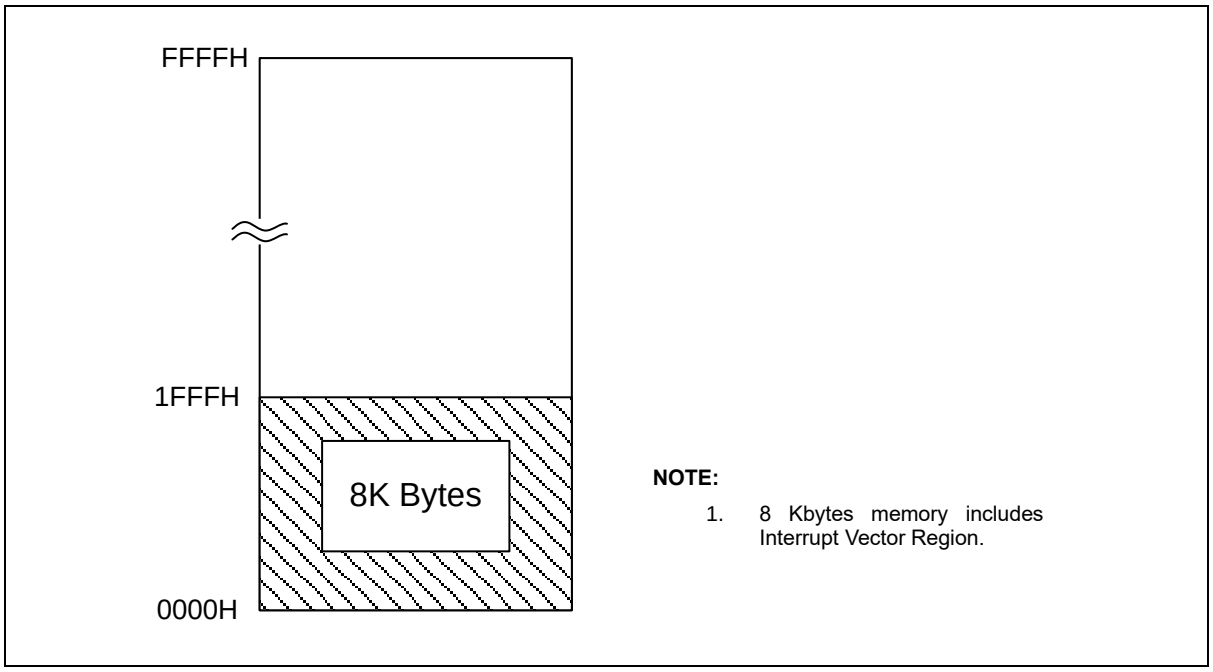
4.1 Program memory

A 16-bit program counter is capable of addressing up to 64 Kbytes, but A96L623 has only 8 Kbytes program memory space. After reset, CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 1 is assigned to location 000BH. If the external interrupt 1 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8 byte interval.

A longer service routine can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use. Figure 6 shows a map of the lower part of the program memory.

Figure 6. Program Memory



More detailed description of program memory is introduced in Chapter 22. Flash Memory.

4.2 Internal data memory

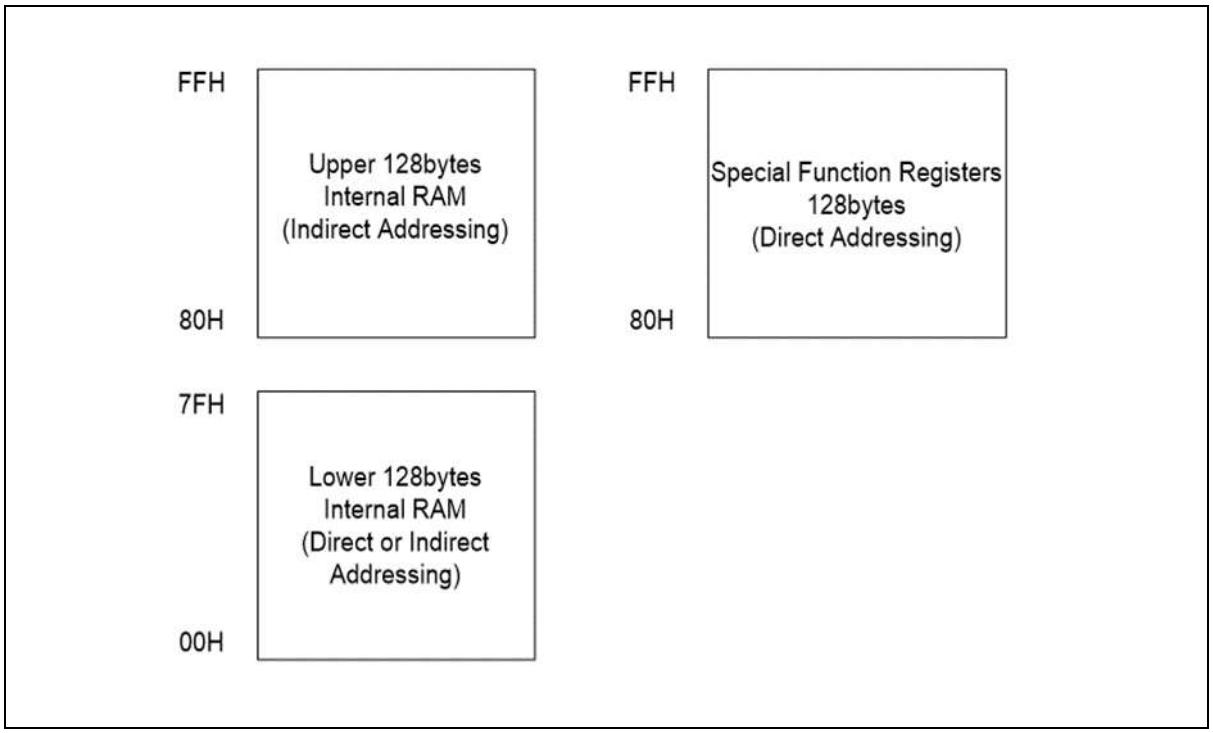
Internal data memory is divided into three spaces as shown in Figure 7. Those three spaces are generally called as,

- Lower 128 bytes
- Upper 128 bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256 bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. By means of this method, the upper 128 bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in Figure 7.

Figure 7. Internal Data Memory Map

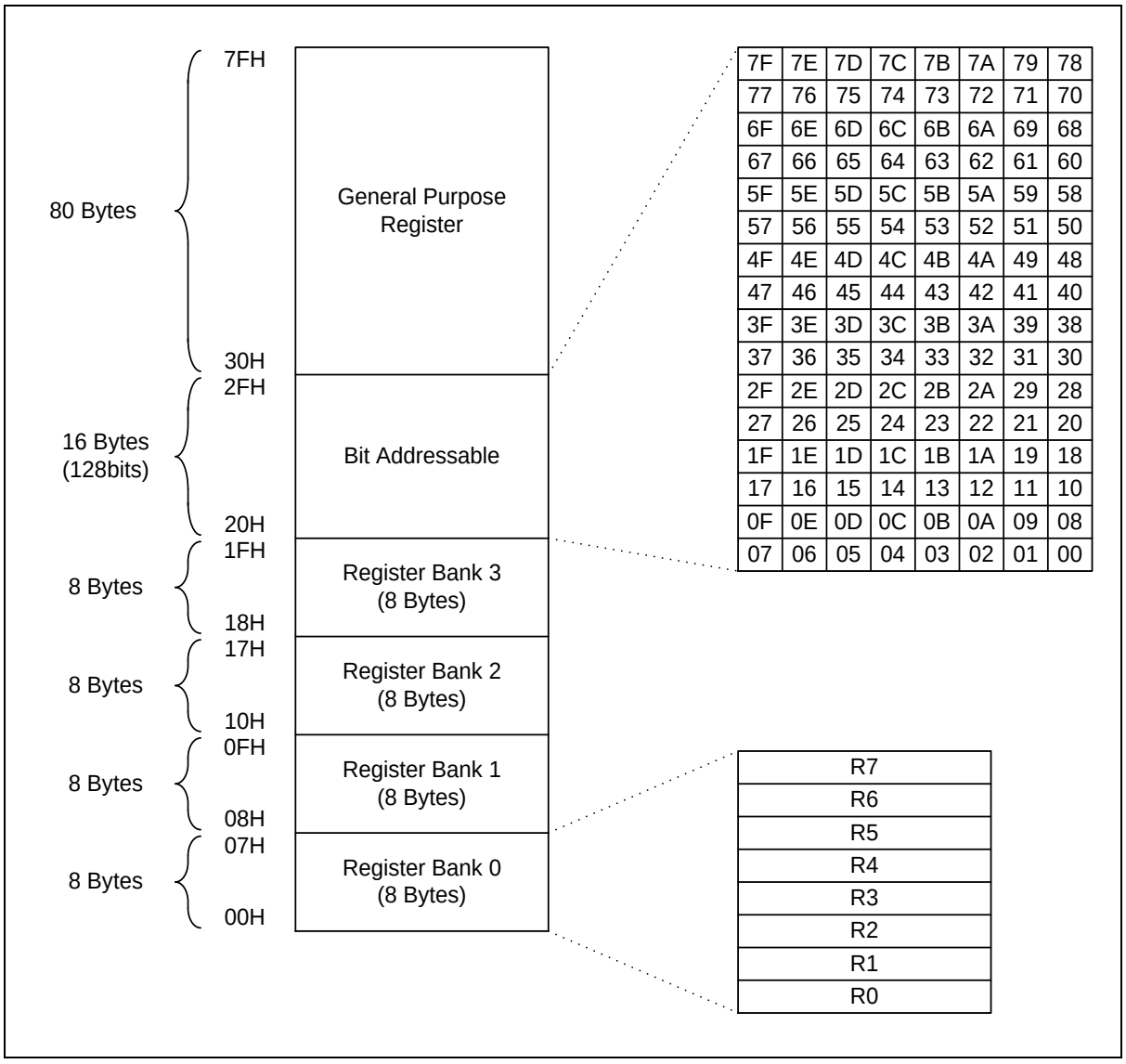


The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 8. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128 bytes can be accessed by either direct or indirect addressing, while the upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

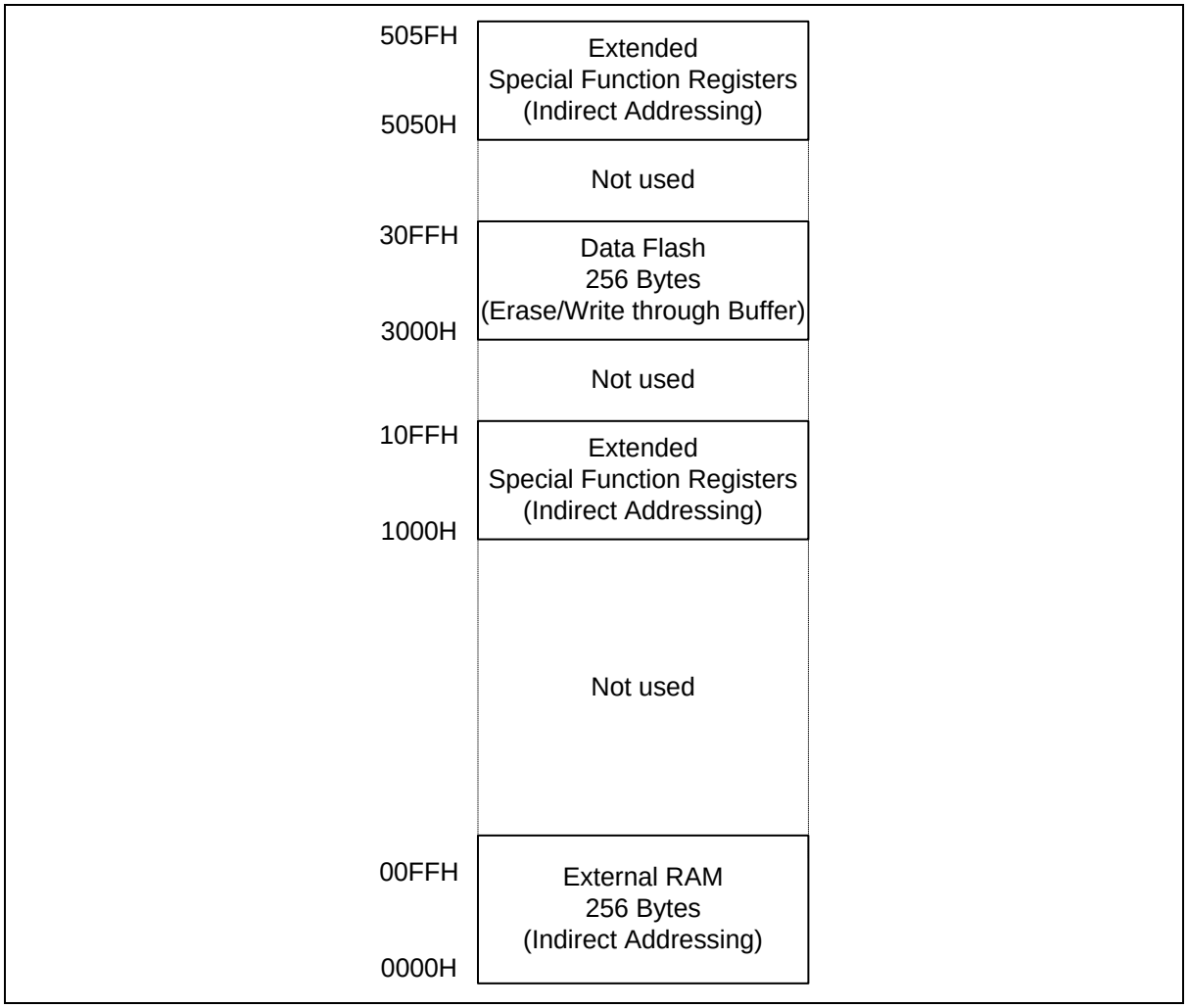
Figure 8. Lower 128 bytes Internal RAM



4.3 Extended SFR and data memory area

A96L623 has 256/768 bytes XRAM and XSFR registers. Extended SFR area has no relation with RAM nor FLASH. This area can be read or written to by using SFR in 8-bit unit.

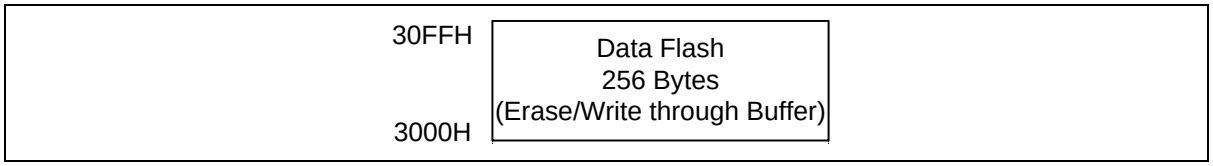
Figure 9. Extended SFR (XSFR) Area



4.4 Data Flash area

Data flash area has no relation with RAM nor FLASH. This area can be read by using DPTR. Data flash area can be erased or written to by using a buffer.

Figure 10. Data Flash Area



Detailed information about Data flash, please refer to Chapter 23. Data Flash Memory.

4.5 SFR map

In this section, information of SFR map and map summaries are introduced through Table 4, Table 5, Table 6, and Table 7.

4.5.1 SFR map summary

Table 4. SFR Map Summary

	00H/8H[NOTE]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	–
0F0H	B	–	DFSADRL	DFSADRH	DFIDR	DFMCR	–	–
0E8H	RSTFR	TSCR	TSIDRL	TSIDRH	TSODR0	TSODR1	TSODR2	–
0E0H	ACC	–	ICSCR	ICSDR0	ICSDR1	–	–	–
0D8H	LVRCR	–	USTCR1	USTCR2	USTCR3	USTST	USTBD	USTDR
0D0H	PSW	–	–	–	–	–	–	FCDIN
0C8H	OSCCR	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH	–	–
0C0H	–	–	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	–	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	–	–	T0CRL	T0CRH	T0ADRL	T0ADRH	T0BDRL	T0BDRH
0A8H	IE	IE1	IE2	IE3	SWCR	CHPCR	AMP0CR	AMP1CR
0A0H	EIFLAG	–	EO	–	EIPOL0	EIPOL1	OP0FSR	–
98H	–	P1IO	P1OD	P1PU	P1FSRL	P1FSRH	P1DB	IRCIDR
90H	PLTCR	P0IO	P0OD	P0PU	P0FSRL	P0FSRH	P0DB	IRCTRM
88H	P1	–	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	IRCTCR
80H	P0	SP	DPL	DPH	DPL1	DPH1	–	PCON

– Reserved M8051 compatible

NOTE:

1. Registers 00H/8H are bit-addressable.

4.5.2 Extended SFR map summary

Table 5. XSFR Map Summary

	00H/8H	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
5058H	FCDRL	–	–	–	–	–	–	LVRIDR
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH
……	–	–	–	–	–	–	–	–
1098H	–	–	–	–	–	–	–	RXIRR
……	–	–	–	–	–	–	–	–
1078H	T30FREQ0	T30FREQ1	T30FREQ2	T85FREQ0	T85FREQ1	T85FREQ2	–	–
……	–	–	–	–	–	–	–	–
1018H	TMINRL	TMINRH	TMAXRL	TMAXRH	TENDRL	TENDRH	–	LITXTINF
1010H	TTXDRL	TTXDRH	TTXRRL	TTXRRH	TRXARL	TRXARL	TDLYRL	TDLYRH
1008H	LICAPL	LICAPH	TTXARL	TTXARH	TTXBRL	TTXBRH	TTXCRL	TTXCRH
1000H	LICR0	LICR1	LICR2	LISTATR	RXBLEN	LIRXDR	TXBLEN	LITXDR

– Reserved

4.5.3 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	–	–	–	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reserved	–	–	–							
87H	Power Control Register	PCON	R/W	–	–	–	–	–	–	0	0
88H	P1 Data Register	P1	R/W	–	–	–	0	0	0	0	0
89H	Reserved	–	–	–							
8AH	System and Clock Control Register	SCCR	R	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	0	0	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
8EH	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	Internal RC Trim Control Register	IRCTCR	R/W	0	0	0	0	0	0	0	0
90H	Power Line Transceiver Control Register	PLTCR	R/W	–	–	–	0	–	–	–	0
91H	P0 Direction Register	P0IO	R/W	–	–	–	0	0	0	0	0
92H	P0 Open-drain Selection Register	P0OD	R/W	–	–	–	0	0	0	0	0
93H	P0 Pull-up Resistor Selection Register	P0PU	R/W	–	–	–	0	0	0	0	0
94H	Port 0 Function Selection Low Register	P0FSRL	R/W	–	0	–	0	0	0	–	0
95H	Port 0 Function Selection High Register	P0FSRH	R/W	–	–	–	–	–	–	0	0
96H	P0 Debounce Enable Register	P0DB	R/W	0	0	–	–	–	–	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
97H	Internal RC Trim Register	IRCTRM	R/W	x	x	x	x	x	x	x	x
98H	Reserved	–	–	–							
99H	P1 Direction Register	P1IO	R/W	–	–	–	0	0	0	0	0
9AH	P1 Open-drain Selection Register	P1OD	R/W	–	–	–	0	0	0	0	0
9BH	P1 Pull-up Resistor Selection Register	P1PU	R/W	–	–	–	0	0	0	0	0
9CH	Port 1 Function Selection Low Register	P1FSRL	R/W	0	0	–	0	0	0	0	0
9DH	Port 1 Function Selection High Register	P1FSRH	R/W	–	–	–	–	–	–	0	0
9EH	P1 Debounce Enable Register	P1DB	R/W	–	–	–	–	–	–	0	0
9FH	Internal RC Trim Identification Register	IRCIDR	R/W	0	0	0	0	0	0	0	0
A0H	External Interrupt Flag Register	EIFLAG	R/W	0	0	0	0	0	0	0	0
A1H	Reserved	–	–	–							
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–							
A4H	External Interrupt Polarity 0 Register	EIPOL0	R/W	–	–	–	–	0	0	0	0
A5H	External Interrupt Polarity 1 Register	EIPOL1	R/W	–	–	0	0	0	0	0	0
A6H	OP-AMP0 Feedback Selection Register	OP0FSR	R/W	0	–	0	0	0	0	0	0
A7H	Reserved	–	–	–							
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	–	–	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	–	0	0	–	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	–	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	0	0	0	–	–	–
ACH	Switch Control Register	SWCR	R/W	–	–	0	0	0	0	0	0
ADH	Chopper Control Register	CHPCR	R/W	–	–	–	0	–	–	0	0
AEH	OP-AMP 0 Control Register	AMP0CR	R/W	–	–	–	–	–	–	0	0
AFH	OP-AMP 1 Control Register	AMP1CR	R/W	–	0	0	0	–	–	0	0
B0H	Reserved	–	–	–							
B1H	Reserved	–	–	–							

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
B2H	Timer 0 Control Low Register	T0CRL	R/W	0	0	0	0	0	0	0	0
B3H	Timer 0 Control High Register	T0CRH	R/W	0	–	0	0	–	–	–	0
B4H	Timer 0 A Data Low Register	T0ADRL	R/W	1	1	1	1	1	1	1	1
B5H	Timer 0 A Data High Register	T0ADRH	R/W	1	1	1	1	1	1	1	1
B6H	Timer 0 B Data Low Register	T0BDRL	R/W	1	1	1	1	1	1	1	1
B7H	Timer 0 B Data High Register	T0BDRH	R/W	1	1	1	1	1	1	1	1
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	Reserved	–	–	–							
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	0	0	0	0
BBH	Timer 1 Control High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1
C0H	Reserved	–	–	–							
C1H	Reserved	–	–	–							
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	0	0	0	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	–	–	0	1	–	–	–
C9H	Reserved	–	–	–							
CAH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	–	0	0	0	0	0
CBH	A/D Converter Control High Register	ADCCRH	R/W	0	–	–	–	0	0	0	0
CCH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
CDH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x
CEH	Reserved	–	–	–							
CFH	Reserved	–	–	–							
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	Reserved	–	–	–							
D5H	Reserved	–	–	–							
D6H	Reserved	–	–	–							
D7H	Flash CRC Data In Register	FCDIN	R/W	0	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	0	–	–	–	–	–	–	0
D9H	Reserved	–	–	–							
DAH	USART Control Register 1	USTCR1	R/W	0	0	0	0	0	0	0	0
DBH	USART Control Register 2	USTCR2	R/W	0	0	0	0	0	0	0	0
DCH	USART Control Register 3	USTCR3	R/W	0	0	0	0	0	0	0	0
DDH	USART Status Register	USTST	R/W	1	0	0	0	0	0	0	0
DEH	USART Baud Rate Generation Register	USTBD	R/W	1	1	1	1	1	1	1	1
DFH	USART Data Register	USTDR	R/W	0	0	0	0	0	0	0	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Reserved	–	–	–							
E2H	Constant Sink Current Control Register	ICSCR	R/W	–	–	–	–	0	0	0	0
E3H	Constant Sink Current Data Register 0	ICSDR0	R/W	–	–	–	–	0	0	0	0
E4H	Constant Sink Current Data Register 1	ICSDR1	R/W	–	–	–	–	0	0	0	0
E5H	Reserved	–	–	–							
E6H	Reserved	–	–	–							
E7H	Reserved	–	–	–							
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	TS Control Register	TSCR	R/W	–	–	–	0	–	–	0	0
EAH	TS Interval Data Low Register	TSIDRL	R/W	1	1	1	1	1	1	1	1
EBH	TS Interval Data High Register	TSIDRH	R/W	1	1	1	1	1	1	1	1
ECH	TS Output Data Register 0	TSODR0	R	0	0	0	0	0	0	0	0
EDH	TS Output Data Register 1	TSODR1	R	0	0	0	0	0	0	0	0
EEH	TS Output Data Register 2	TSODR2	R	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
EFH	Reserved	–	–	–							
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Reserved	–	–	–							
F2H	Data Flash Sector Address Low Register	DFSADRL	R/W	0	0	0	–	–	–	–	–
F3H	Data Flash Sector Address High Register	DFSADRH	R/W	0	0	0	0	0	0	0	0
F4H	Data Flash Identification Register	DFIDR	R/W	0	0	0	0	0	0	0	0
F5H	Data Flash Mode Control Register	DFMCR	R/W	0	–	–	–	–	0	0	0
F6H	Reserved	–	–	–							
F7H	Reserved	–	–	–							
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Flash Sector Address High Register	FSADRH	R/W	–	–	–	–	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	–	–	–	–	0	0	0
FFH	Reserved	–	–	–							

4.5.4 Extended SFR map

Table 7. XSFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
1000H	Line Interface Control Register 0	LICR0	R/W	0	0	0	–	0	0	0	0
1001H	Line Interface Control Register 1	LICR1	R/W	–	–	–	–	–	0	0	0
1002H	Line Interface Control Register 2	LICR2	R/W	–	–	–	–	0	0	0	0
1003H	Line Interface Status Register	LISTATR	R/W	0	0	0	0	0	0	0	0
1004H	Receive bits Length Counter	RXBLEN	R	0	0	0	0	0	0	0	0
1005H	Line Interface Receive Data Register	LIRXDR	R	0	0	0	0	0	0	0	0
1006H	Transmit bits Length Counter	TXBLEN	R/W	0	0	0	0	0	0	0	0
1007H	Line Interface Transmit Data Register	LITXDR	R/W	0	0	0	0	0	0	0	0
1008H	Line Interface Capture Data Low Register	LICAPL	R	0	0	0	0	0	0	0	0
1009H	Line Interface Capture Data High Register	LICAPH	R	0	0	0	0	0	0	0	0
100AH	Transmit Time A Data Low Register	TTXARL	R/W	0	0	0	0	0	0	0	0
100BH	Transmit Time A Data High Register	TTXARH	R/W	0	0	0	0	0	0	0	0
100CH	Transmit Time B Data Low Register	TTXBRL	R/W	0	0	0	0	0	0	0	0
100DH	Transmit Time B Data High Register	TTXBRH	R/W	0	0	0	0	0	0	0	0
100EH	Transmit Time C Data Low Register	TTXCRL	R/W	0	0	0	0	0	0	0	0
100FH	Transmit Time C Data High Register	TTXCRH	R/W	0	0	0	0	0	0	0	0
1010H	Transmit Time D Data Low Register	TTXDRL	R/W	0	0	0	0	0	0	0	0
1011H	Transmit Time D Data High Register	TTXDRH	R/W	0	0	0	0	0	0	0	0
1012H	Transmit Time Rx Data Low Register	TTXRRL	R/W	0	0	0	0	0	0	0	0
1013H	Transmit Time Rx Data High Register	TTXRRH	R/W	0	0	0	0	0	0	0	0
1014H	Receive Time A Data Low Register	TRXARL	R/W	0	0	0	0	0	0	0	0
1015H	Receive Time A Data High Register	TRXARH	R/W	0	0	0	0	0	0	0	0
1016H	Delay Time Data Low Register	TDLYRL	R/W	0	0	0	0	0	0	0	0
1017H	Delay Time Data High Register	TDLYRH	R/W	0	0	0	0	0	0	0	0
1018H	Minimum Time Data Low Register	TMINRL	R/W	0	0	0	0	0	0	0	0
1019H	Minimum Time Data High Register	TMINRH	R/W	0	0	0	0	0	0	0	0
101AH	Maximum Time Data Low Register	TMAXRL	R/W	0	0	0	0	0	0	0	0
101BH	Maximum Time Data High Register	TMAXRH	R/W	0	0	0	0	0	0	0	0
101CH	End Time Data Low Register	TENDRL	R/W	0	0	0	0	0	0	0	0
101DH	End Time Data High Register	TENDRH	R/W	0	0	0	0	0	0	0	0

Table 7. XSFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
101EH	Reserved	–	–	–							
101FH	Line Interface Transmit Toggle Information Register	LITXTINF	R/W	0	0	0	0	0	0	0	0

1078H	TS Output Frequency Register 0 at 30℃	T30FREQ0	R	x	x	x	x	x	x	x	x
1079H	TS Output Frequency Register 1 at 30℃	T30FREQ1	R	x	x	x	x	x	x	x	x
107AH	TS Output Frequency Register 2 at 30℃	T30FREQ2	R	x	x	x	x	x	x	x	x
107BH	TS Output Frequency Register 0 at 85℃	T85FREQ0	R	x	x	x	x	x	x	x	x
107CH	TS Output Frequency Register 1 at 85℃	T85FREQ1	R	x	x	x	x	x	x	x	x
107DH	TS Output Frequency Register 2 at 85℃	T85FREQ2	R	x	x	x	x	x	x	x	x
----------											
109FH	RXI Signal Read Register	RXIRR	R	–	–	–	–	–	–	–	0

5050H	Flash CRC Start Address High Register	FCSARH	R/W	–	–	–	–	–	–	–	0
5051H	Flash CRC End Address High Register	FCEARH	R/W	–	–	–	–	–	–	–	0
5052H	Flash CRC Start Address Middle Register	FCSARM	R/W	0	0	0	0	0	0	0	0
5053H	Flash CRC End Address Middle Register	FCEARM	R/W	0	0	0	0	0	0	0	0
5054H	Flash CRC Start Address Low Register	FCSARL	R/W	0	0	0	0	–	–	–	–
5055H	Flash CRC End Address Low Register	FCEARL	R/W	0	0	0	0	1	1	1	1
5056H	Flash CRC Control Register	FCCR	R/W	0	0	0	–	0	0	0	0
5057H	Flash CRC Data High Register	FCDRH	R	1	1	1	1	1	1	1	1
5058H	Flash CRC Data Low Register	FCDRL	R	1	1	1	1	1	1	1	1

505FH	LVR Write Identification Register	LVRIDR	R/W	0	0	0	0	0	0	0	0

5 Ports

5.1 I/O ports

A96L623 has two groups of I/O ports, P0 and P1. Each port can be easily configured as an input pin, an output, or an internal pull up and open-drain pin by software. The port configuration pursues to meet various system configurations and design requirements.

5.2 Port description of P0

As a 5-bit I/O port, P0 controls the following registers:

- P0 data register (P0)
- P0 direction register (P0IO)
- P0 debounce enable register (P0DB)
- P0 pull-up resistor selection register (P0PU)
- P0 open-drain selection register (P0OD)
- P0 Function selection registers (P0FSRH/P0FSRL)

5.3 Port description of P1

As a 5-bit I/O port, P1 controls the following registers:

- P1 data register (P1)
- P1 direction register (P1IO)
- P1 pull-up resistor selection register (P1PU)
- P1/P2 debounce enable register (P1DB)
- P1 open-drain selection register (P1OD)
- P1 Function selection registers (P1FSRH/P1FSRL)

6 Interrupt controller

Up to 16 interrupt sources are available in the A96L623. Allowing software control, each interrupt source can be enabled by defining separate enable register bit associated with it. It can also have four levels of priority assigned. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources and is not controllable by software.

The interrupt controller features the followings:

- Receives requests from 16 interrupt sources
- 6 group priority
- 4 priority levels
- Multi interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit
- Interrupt latency varies ranging from 3 to 9 machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control. It must be set to ‘1’ to enable interrupts as introduced in the followings:

- When EA is set to ‘0’ ➔ all interrupts are disabled.
- When EA is set to ‘1’ ➔ a particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

EA is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. A96L623 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of the four levels according to IP and IP1.

Figure 11. Interrupt Group Priority Level

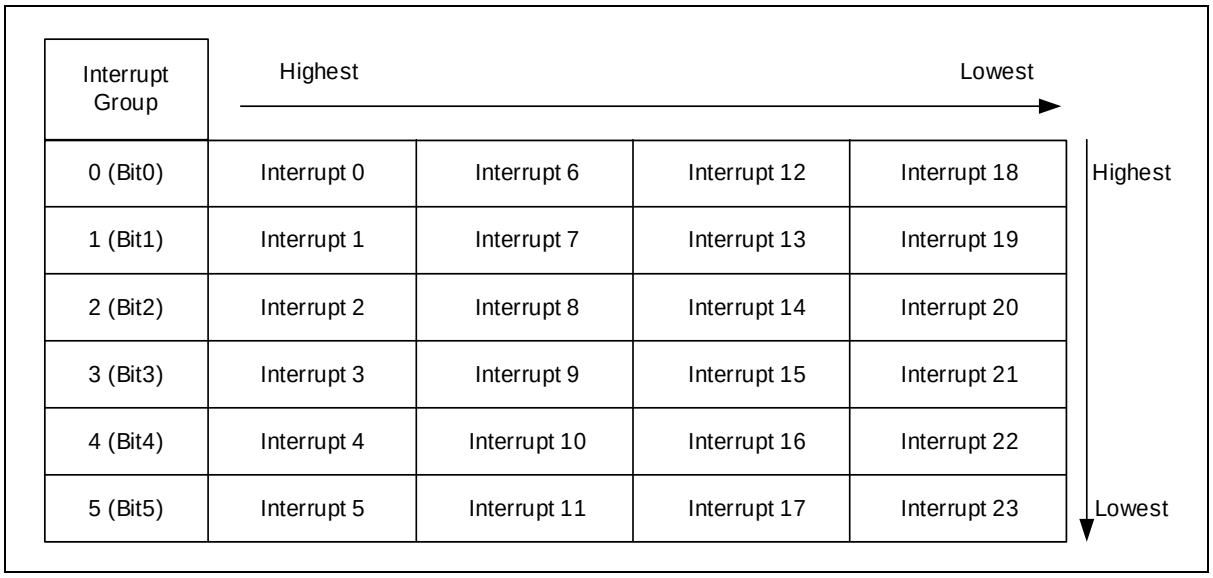


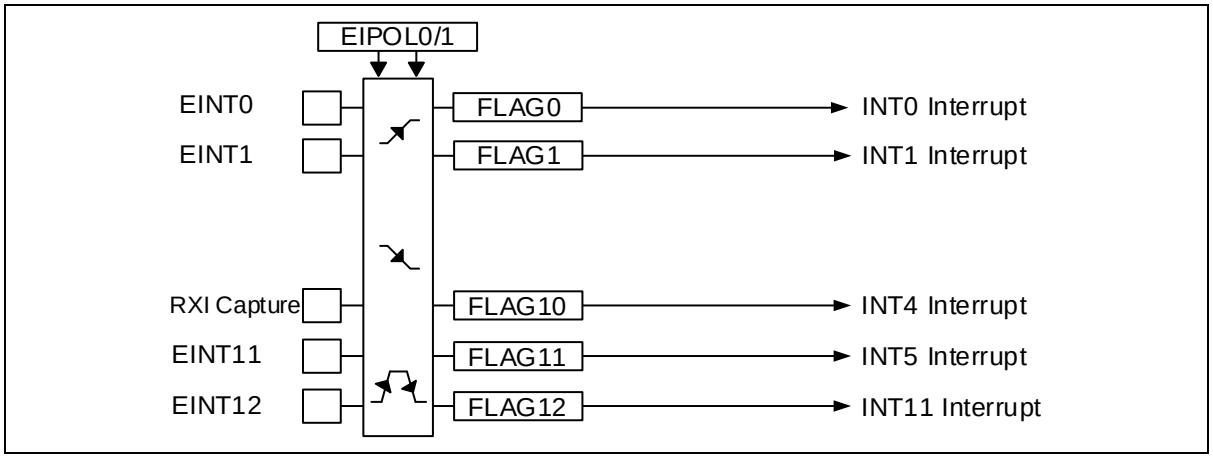
Figure 11 introduces interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by 2 bits of Interrupt Priority (IP) registers: 1 bit from IP and another 1 bit from IP1.

Interrupt Service Routine serves an interrupt having higher priority first. If two requests of different priority levels are received simultaneously, the request with higher priority level is served prior to the lower one.

6.1 External interrupt

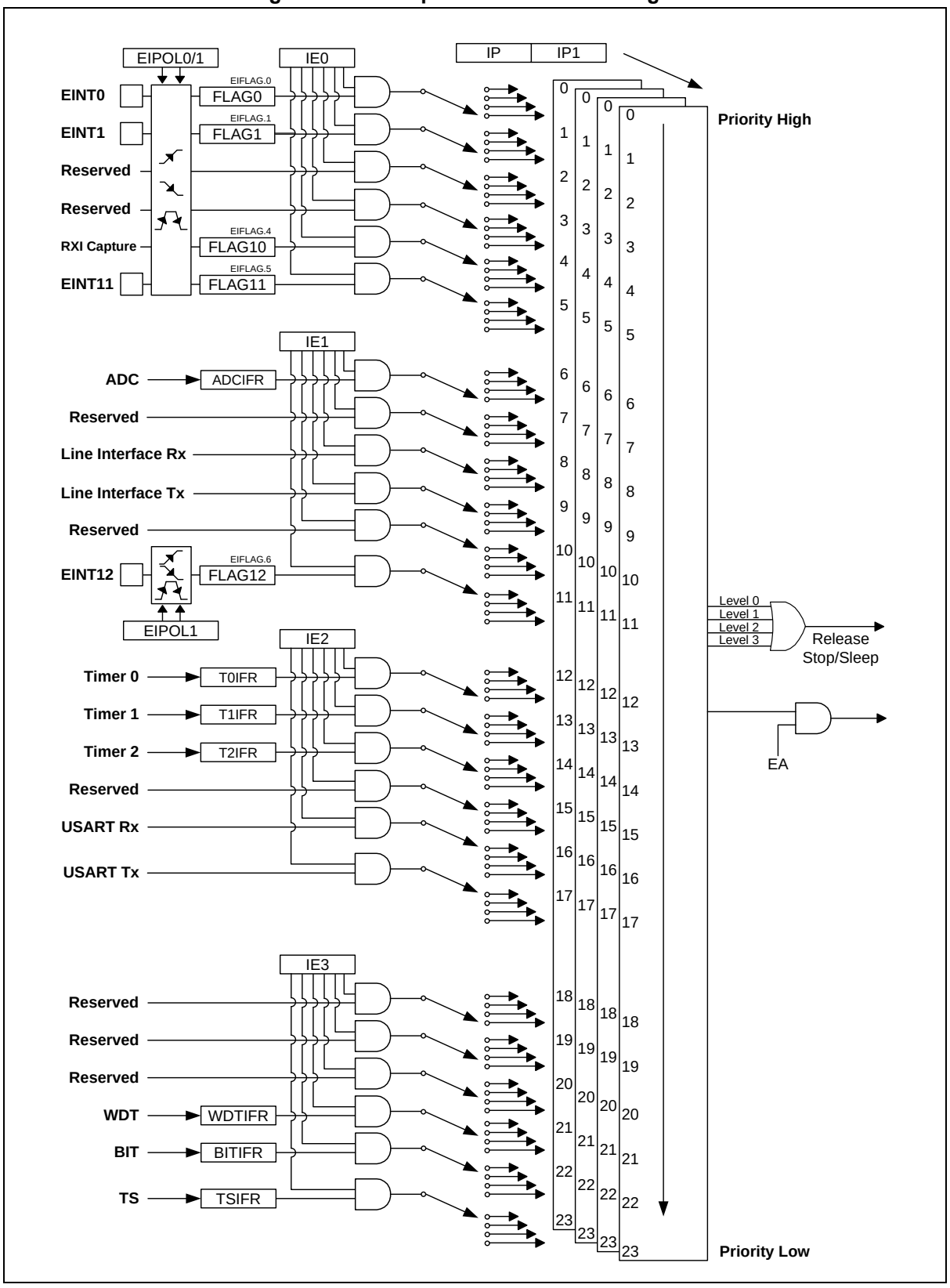
External interrupts on pins of INT0 to INT5 receive various interrupt requests in accordance with the external interrupt polarity 0 register (EIPOL0) and external interrupt polarity 1 register (EIPOL1) as shown in Figure 12. Each external interrupt source has enable/disable bits. An external interrupt flag register (EIFLAG) provides status of the external interrupts.

Figure 12. External Interrupt Description



6.2 Interrupt controller block diagram

Figure 13. Interrupt Controller Block Diagram



In Figure 13, release signal for STOP and IDLE mode can be generated by all interrupt sources which are enabled without reference to priority level. An interrupt request will be delayed while data is written to one of the registers IE, IE1, IE2, IE3, IP, IP1, and PCON.

6.3 Interrupt vector table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack, and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address.

The Interrupt controller supports 24 interrupt sources and each interrupt source has a determined priority order as shown in Table 8.

Table 8. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector address
Hardware RESET	RESETB	-	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
–	INT2	IE.2	3	Maskable	0013H
–	INT3	IE.3	4	Maskable	001BH
RXI Capture Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 11	INT5	IE.5	6	Maskable	002BH
ADC Interrupt	INT6	IE1.0	7	Maskable	0033H
–	INT7	IE1.1	8	Maskable	003BH
Line Interface Rx	INT8	IE1.2	9	Maskable	0043H
Line Interface Tx	INT9	IE1.3	10	Maskable	004BH
–	INT10	IE1.4	11	Maskable	0053H
External Interrupt 12	INT11	IE1.5	12	Maskable	005BH
T0 Interrupt	INT12	IE2.0	13	Maskable	0063H
T1 Interrupt	INT13	IE2.1	14	Maskable	006BH
T2 Interrupt	INT14	IE2.2	15	Maskable	0073H
–	INT15	IE2.3	16	Maskable	007BH
USART Rx Interrupt	INT16	IE2.4	17	Maskable	0083H
USART Tx Interrupt	INT17	IE2.5	18	Maskable	008BH
–	INT18	IE3.0	19	Maskable	0093H
–	INT19	IE3.1	20	Maskable	009BH
–	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
TS Interrupt	INT23	IE3.5	24	Maskable	00BBH

To execute the maskable interrupts, both EA bit and a corresponding bit of IEx associated with a specific interrupt source must be set to ‘1’. When an interrupt request is received, a particular interrupt request flag is set to ‘1’ and maintains its status until CPU accepts the interrupt. After the interrupt acceptance, the interrupt request flag will be cleared automatically.

7 Clock generator

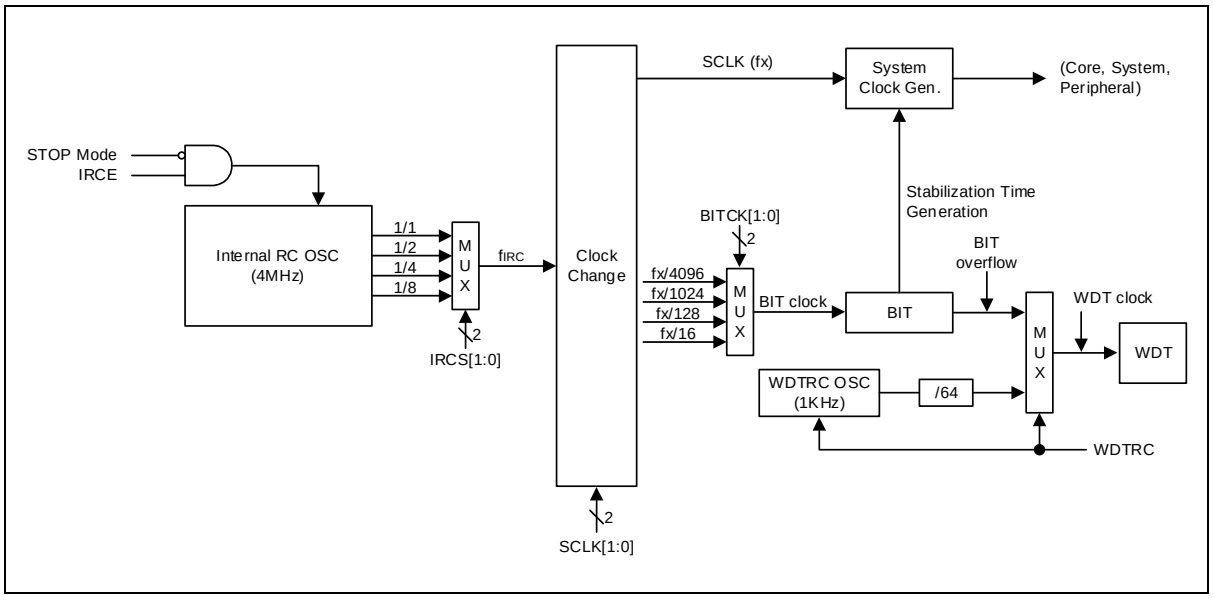
As shown in Figure 14, a clock generator produces basic clock pulses which provide a CPU and peripherals with a system clock. A default system clock is a 1MHz INT-RC oscillator and default division rate is four. To stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

A96L623 incorporates two types of oscillators:

- Calibrated Internal RC Oscillator (4MHz)
  - INT-RC OSC/8 (0.5MHz)
  - INT-RC OSC/4 (1MHz, default system clock)
  - INT-RC OSC/2 (2MHz)
  - INT-RC OSC/1 (4MHz)
- Internal WDTRC Oscillator (1KHz)

7.1 Block diagram

Figure 14. Clock Generator in Block Diagram



8 Basic Interval Timer (BIT)

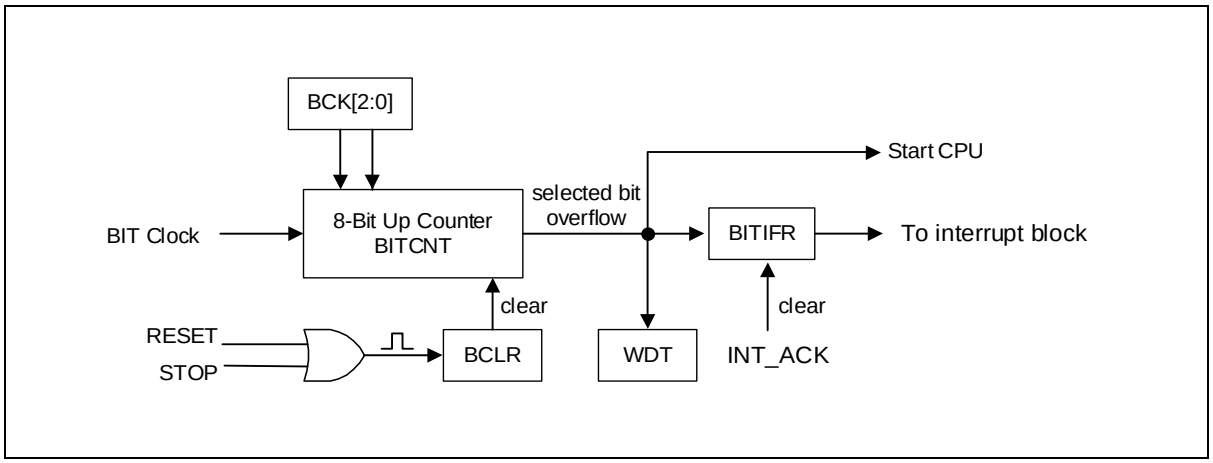
A96L623 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting, and provides a basic interval timer interrupt (BITIFR).

BIT of A96L623 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

8.1 Block diagram

Figure 15. Basic Interval Timer in Block Diagram



9 Watchdog Timer (WDT)

Watchdog Timer (WDT) is used to rapidly detect the CPU malfunctions such as endless looping caused by noise. In addition, it is used to resume the CPU in a normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the WDT is not being used for the detection of the CPU malfunctions, it can be used as a timer generating an interrupt at fixed intervals.

The WDT can be used in a free running 8-bit timer mode or in a watch dog timer mode by setting WDTRSON bit, which is WDTCR[5]. If '1' is written to WDTCR[5], WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

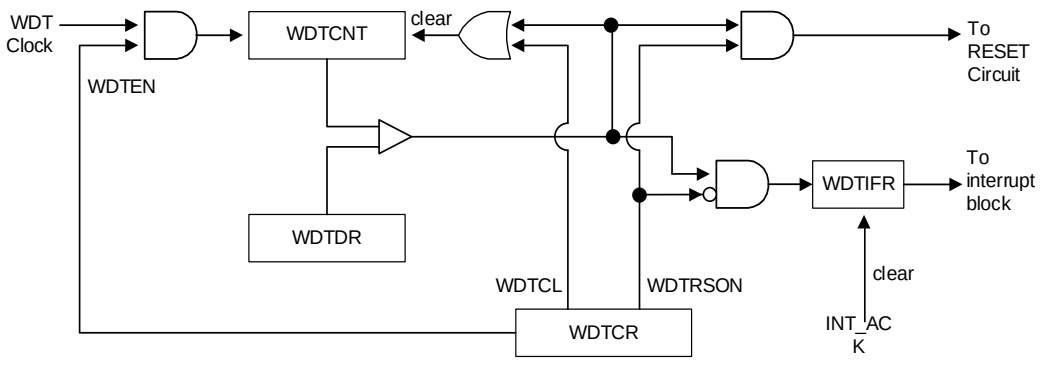
The WDT consists of an 8-bit binary counter and a watchdog timer data register. When value of an 8-bit binary counter is equal to the 8 bits of WDTCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset of CPU in accordance with a bit WDTRSON.

The input clock source of watch dog timer is BIT overflow and WDTRC. Interval of watchdog timer interrupt is decided by the BIT overflow period and WDTDR set value. Equation of the WDT interrupt interval is described in the followings:

- WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)
- WDT Interrupt Interval = 64/f_{WDTRC} x (WDTDR Value+1) when WDTRC

9.1 Block diagram

Figure 16. Watchdog Timer in Block Diagram



NOTE:

1. Watchdog timer clock depends on WDTCK bit in WDTCR register.

10 TIMER 0

A 16-bit timer 0 incorporates a multiplexer and six registers such as timer 0 A data register high/low, timer 0 B data register high/low, and timer 0 control register high/low (T0ADRH, T0ADRL, T0BDRH, T0BDRL, T0CRH, T0CRL).

TIMER 0 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into input capture data register (T0BDRH/T0BDRL) by RXI Signal. Timer 0 outputs the comparison result between counter and data register through T0O port in timer/counter mode. Timer 0 outputs PWM wave form through PWM0O port in the PPG mode).

A timer/counter 0 uses an internal clock or an external clock (EC0) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T0CK[2:0]).

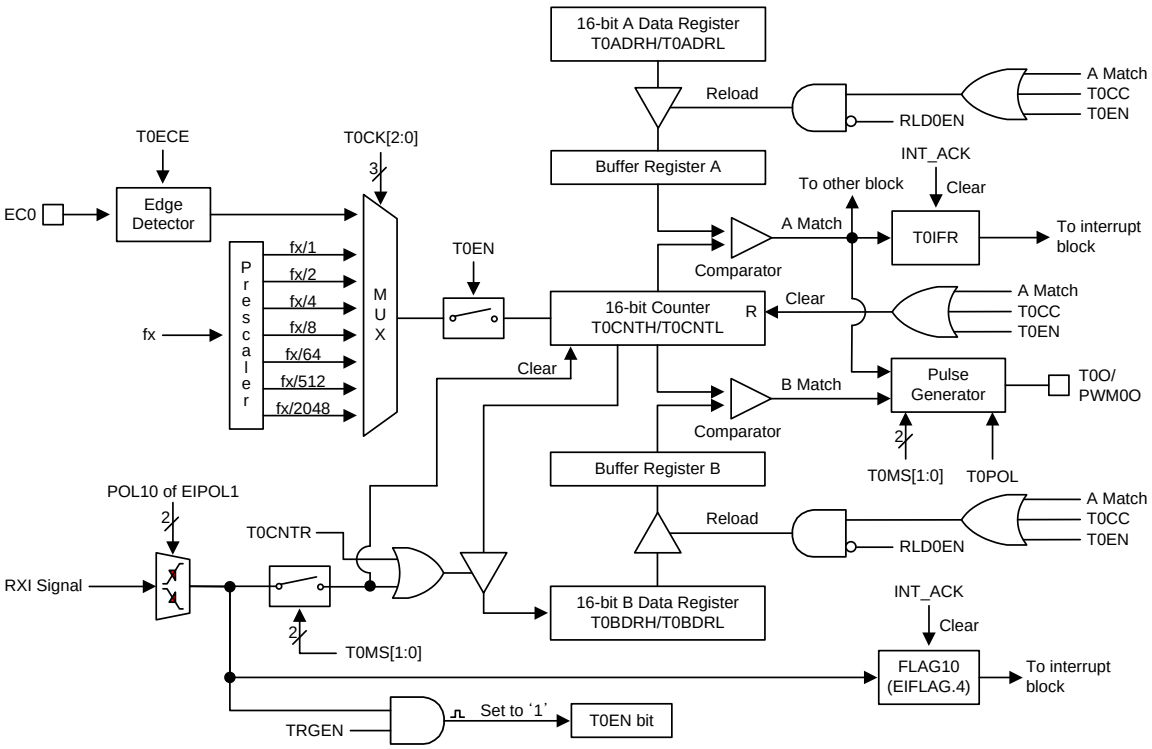
- Timer 0 clock sources: f_X/1, 2, 4, 8, 64, 512, 2048 and EC0

Table 9. TIMER 0 Operating Modes

T0EN	P0FSRH[1:0]	T0MS[1:0]	T0CK[2:0]	Timer 0
1	01	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	01	10	XXX	16 Bit PPG Mode(one-shot mode)
1	01	11	XXX	16 Bit PPG Mode(repeat mode)

10.1 Block diagram

Figure 17. 16-bit Timer 0 in Block Diagram



NOTES:

1. T0EN is automatically cleared to logic '0' after one pulse is generated at a PPG one-shot mode.
2. RLD0EN bit must be '0b' when T0EN bit is changed from '0b' to '1b'.
3. The RXI signal comes from the power line transceiver (PLT).

11 TIMER 1/2

A 16-bit timer 1/2 incorporates a multiplexer and six registers such as timer 1/2 A data register high/low, timer 1/2 B data register high/low, and timer 1/2 control register high/low (TnADRH, TnADRL, TnBDRH, TnBDRL, TnCRH, TnCRL).

TIMER 1/2 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into input capture data register (TnBDRH/TnBDRL) by EINT11/EINT12. Timer 1/2 outputs the comparison result between counter and data register through TnO port in timer/counter mode. Timer 1/2 outputs PWM wave form through PWMnO port in the PPG mode).

A timer/counter 1/2 uses an internal clock or an external clock (ECn) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (TnCK[2:0]).

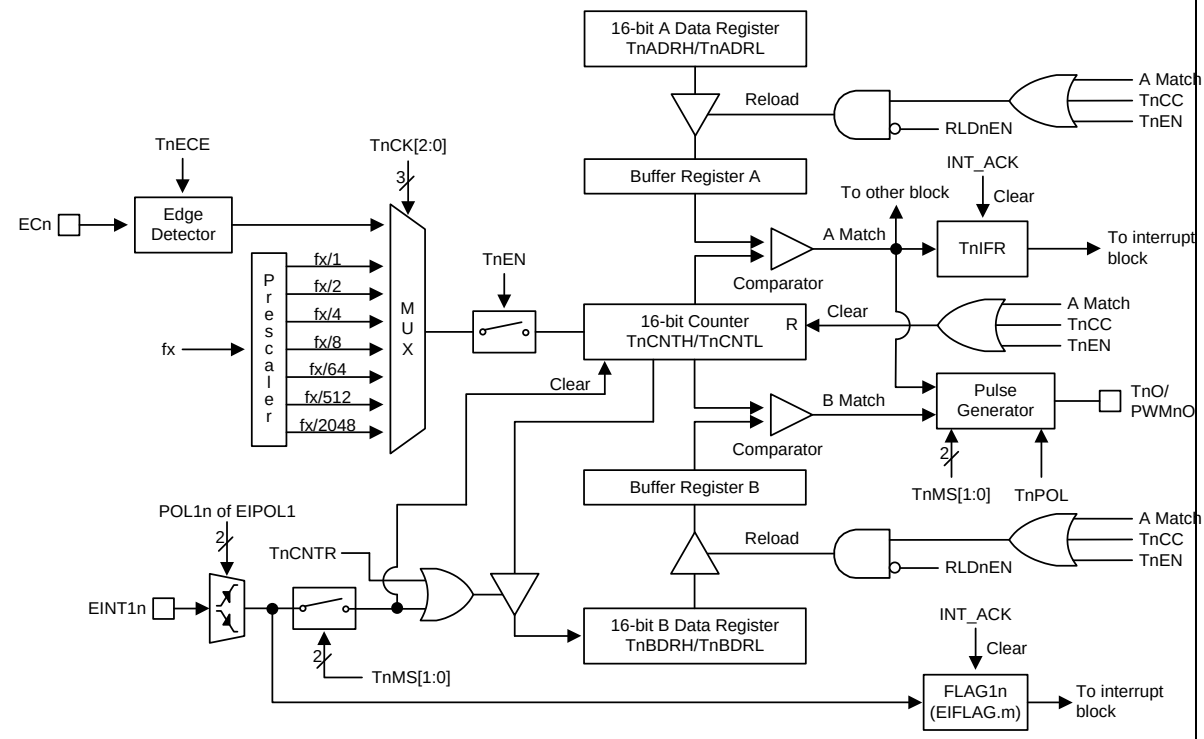
- Timer 1/2 clock sources: f_X/1, 2, 4, 8, 64, 512, 2048 and ECn

Table 10. TIMER 1/2 Operating Modes

TnEN	P1FSRL[1:0](T1)/ P1FSRL[3:2](T2)	TnMS[1:0]	TnCK[2:0]	Timer n
1	01/01	00	XXX	16 Bit Timer/Counter Mode
1	00/00	01	XXX	16 Bit Capture Mode
1	01/01	10	XXX	16 Bit PPG Mode(one-shot mode)
1	01/01	11	XXX	16 Bit PPG Mode(repeat mode)

11.1 Block diagram

Figure 18. 16-bit Timer n in Block Diagram (Where n = 1 and 2, m = 5 and 6)



NOTES:

1. TnEN is automatically cleared to logic ‘0’ after one pulse is generated at a PPG one-shot mode.
2. RLDnEN bit must be ‘0b’ when TnEN bit is changed from ‘0b’ to ‘1b’.
3. It should be set the debounce function of related port, when using the timer capture mode.

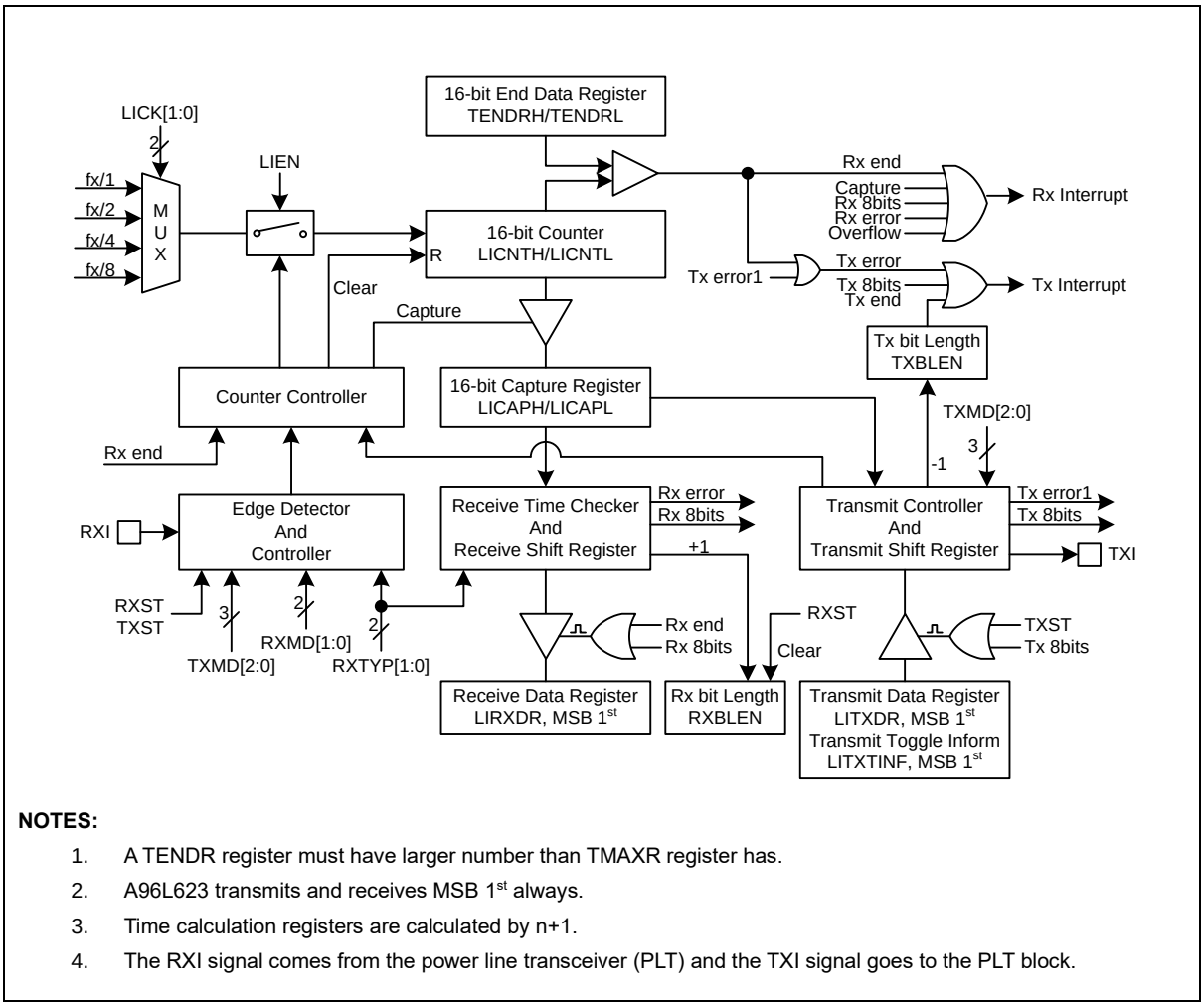
12 Line Interface

A96L623 offers two operating modes for line interfaces as shown in the followings:

- Receive mode (RX Type 0~2)
- Transmit mode (TX Mode 0~4)

12.1 Block diagram

Figure 19. Line Interface in Block Diagram



NOTES:

1. A TENDR register must have larger number than TMAXR register has.
2. A96L623 transmits and receives MSB 1st always.
3. Time calculation registers are calculated by n+1.
4. The RXI signal comes from the power line transceiver (PLT) and the TXI signal goes to the PLT block.

13 10-bit A/D Converter

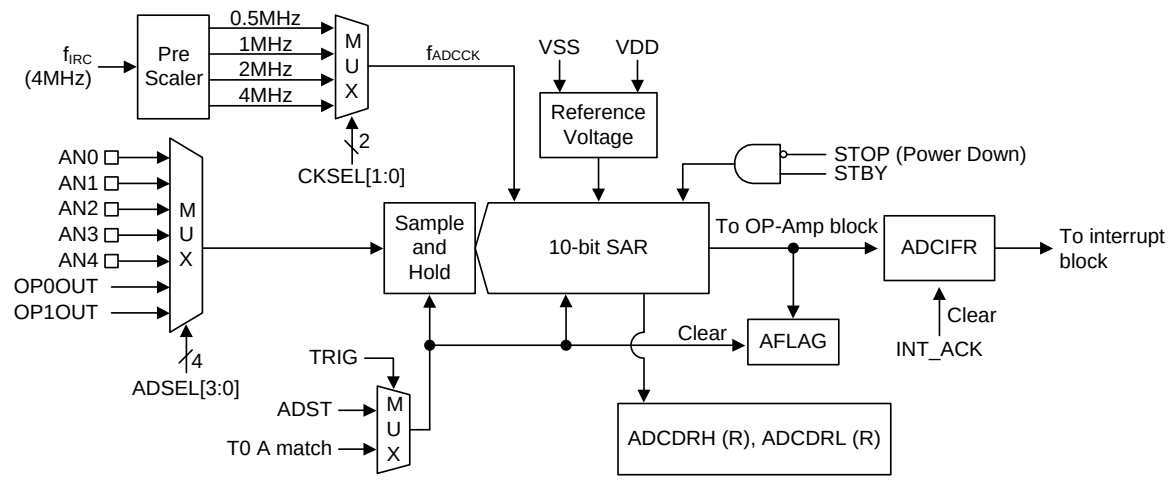
Analog-to-digital (A/D) converter allows conversion of an analog input signal to a corresponding 10-bit digital output. The A/D module has 9 analog inputs, and the output of the multiplexer becomes the input into the converter, which generates a result via successive approximation.

The A/D module incorporates four registers as listed in the followings. Each register can be selected for the corresponding channel by setting ADSEL[3:0]. When conversion is completed, two registers ADCDRH and ADCDRL contain the results of the conversion, the conversion status bit AFLAG is set to '1', and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as '0'.

- A/D converter control high register (ADCCRH)
- A/D converter control low register (ADCCRL)
- A/D converter data high register (ADCDRH)
- A/D converter data low register (ADCDRL)

13.1 Block diagram

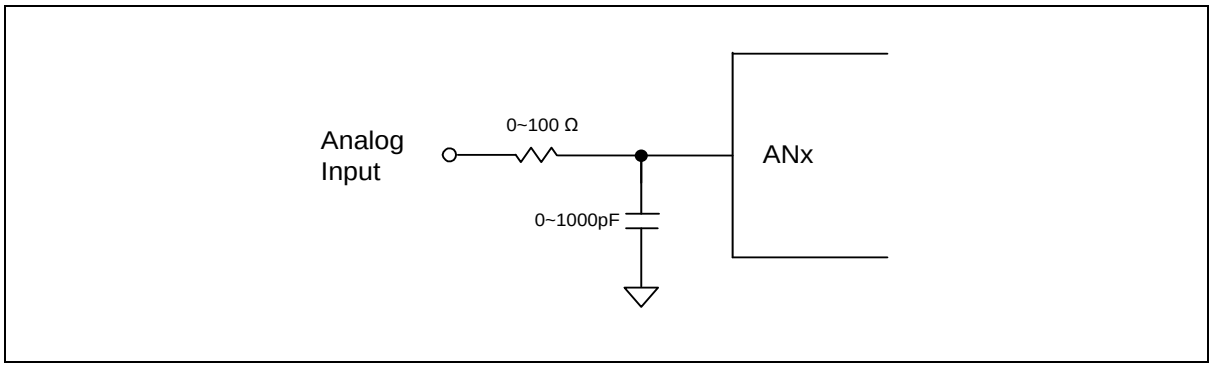
Figure 20. 10-bit ADC Block Diagram



NOTES:

1. The conversion clock is 14-clock including ADC sample and hold.
2. The time of ADC sample/hold and conversion is at least 8usec.

Figure 21. AD Analog Input Pin with Capacitor



14 Operational amplifier

A96L623 offers two channels of an operational amplifier (OP-Amp). OP-Amp consists of five registers such as OP-AMP control register 0 (AMPCR0), OP-AMP control register 1 (AMPCR1), Switch control register (SWCR), Chopper control register (CHPCR), and OP-Amp 0 feedback selection register (OP0FSR).

14.1 Block diagram

Figure 22. OP Amp Block Diagram

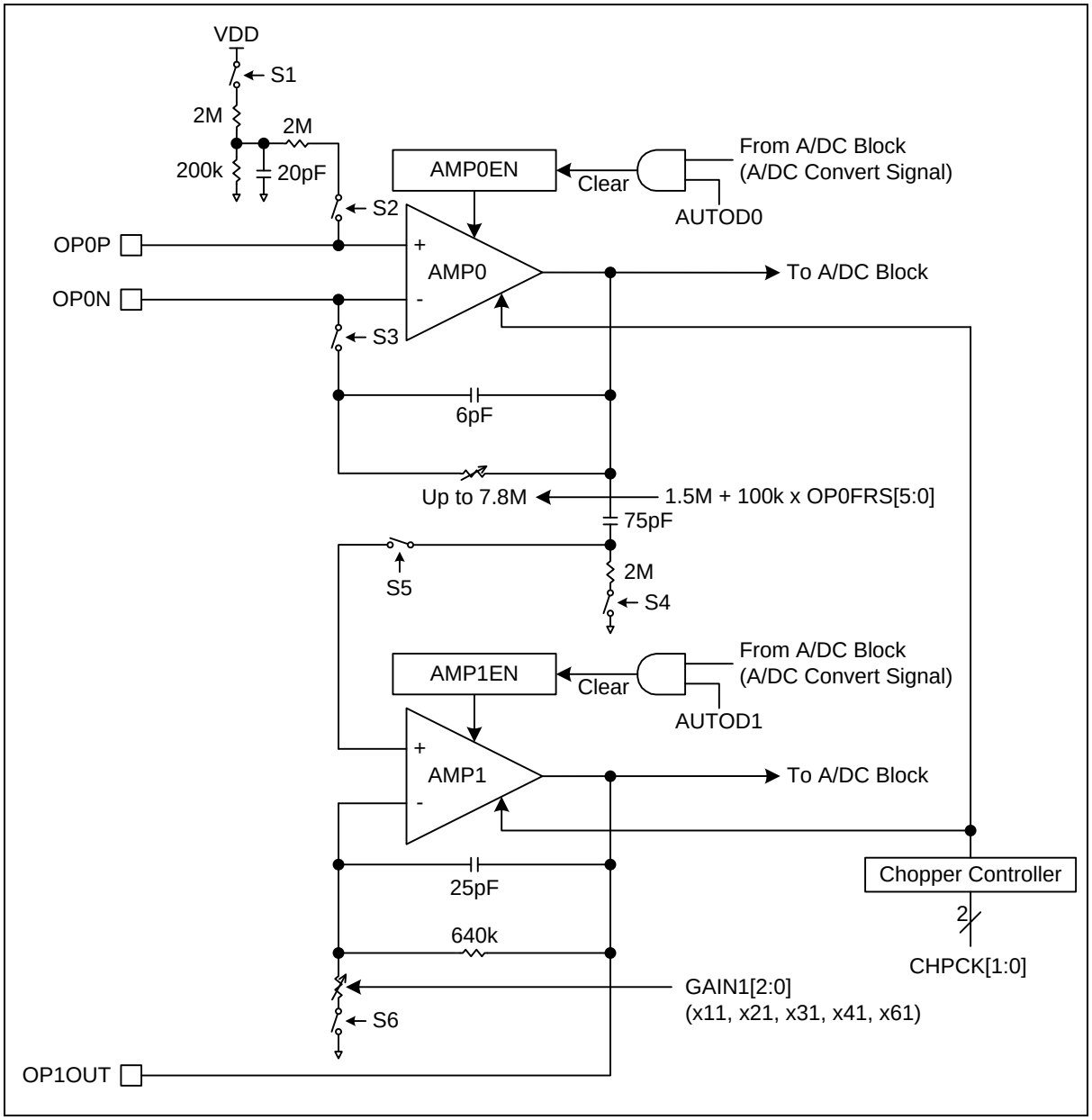


Figure 23. Recommend Circuit for Smoke Detector.

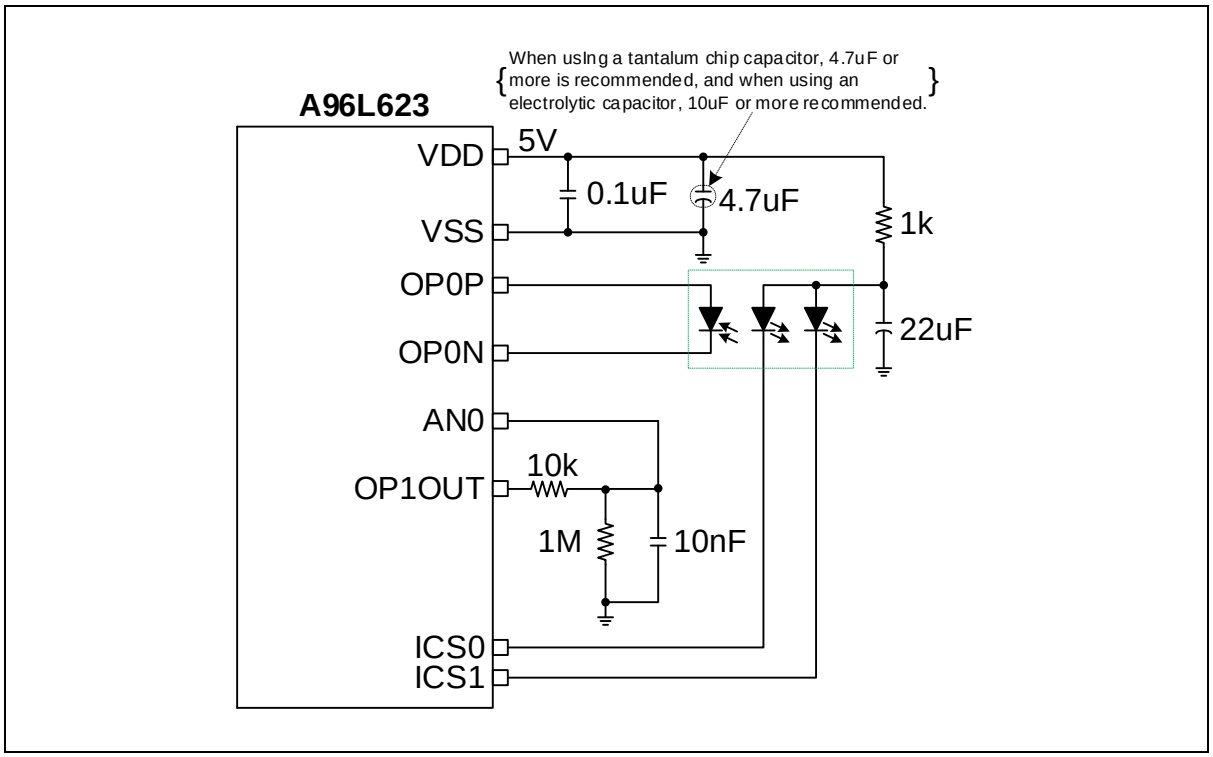
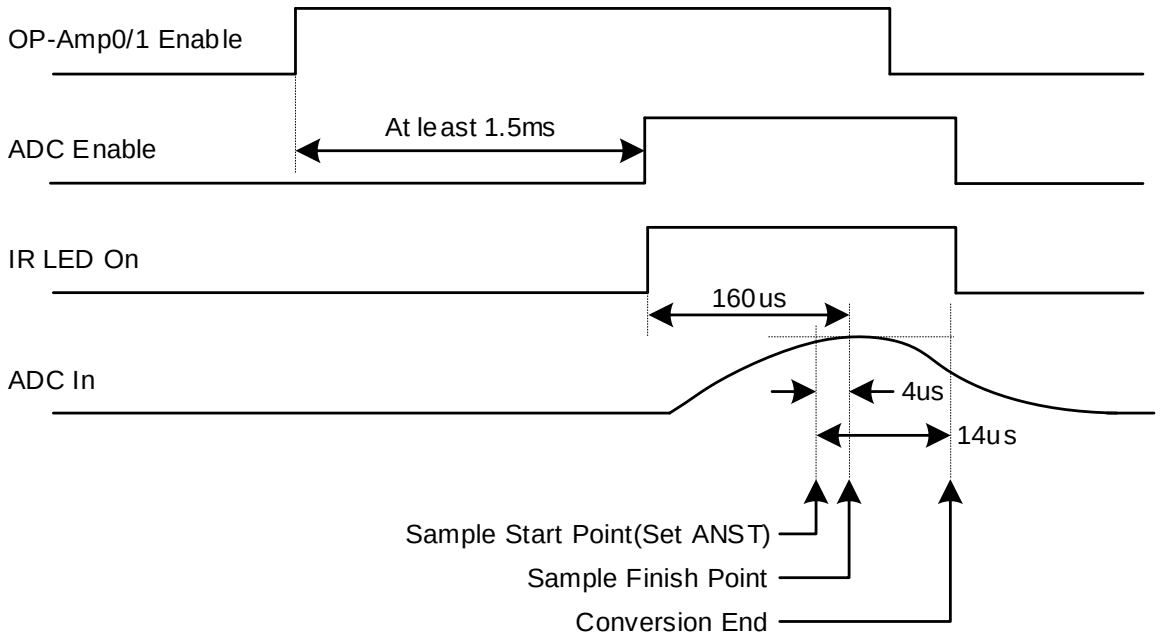


Figure 24. OP-Amp and ADC Start Timing Chart



NOTE:

1. The ADC clock is configured as 2MHz at the above timing chart for example.

15 USART

USART (Universal Synchronous/Asynchronous Receiver/Transmitter) is a microchip that facilitates communication through a computer's serial port using RS-232C protocol. A96L623 incorporates a USART function block inside. The USART function block consists of USART control register1/2/3, USART status register, USART baud-rate generation register and USART data register.

Operation mode is selected by the operation mode of USART selection bits (USTMS[1:0]).

It has three operating modes as listed in the followings:

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode

15.1 USART UART mode

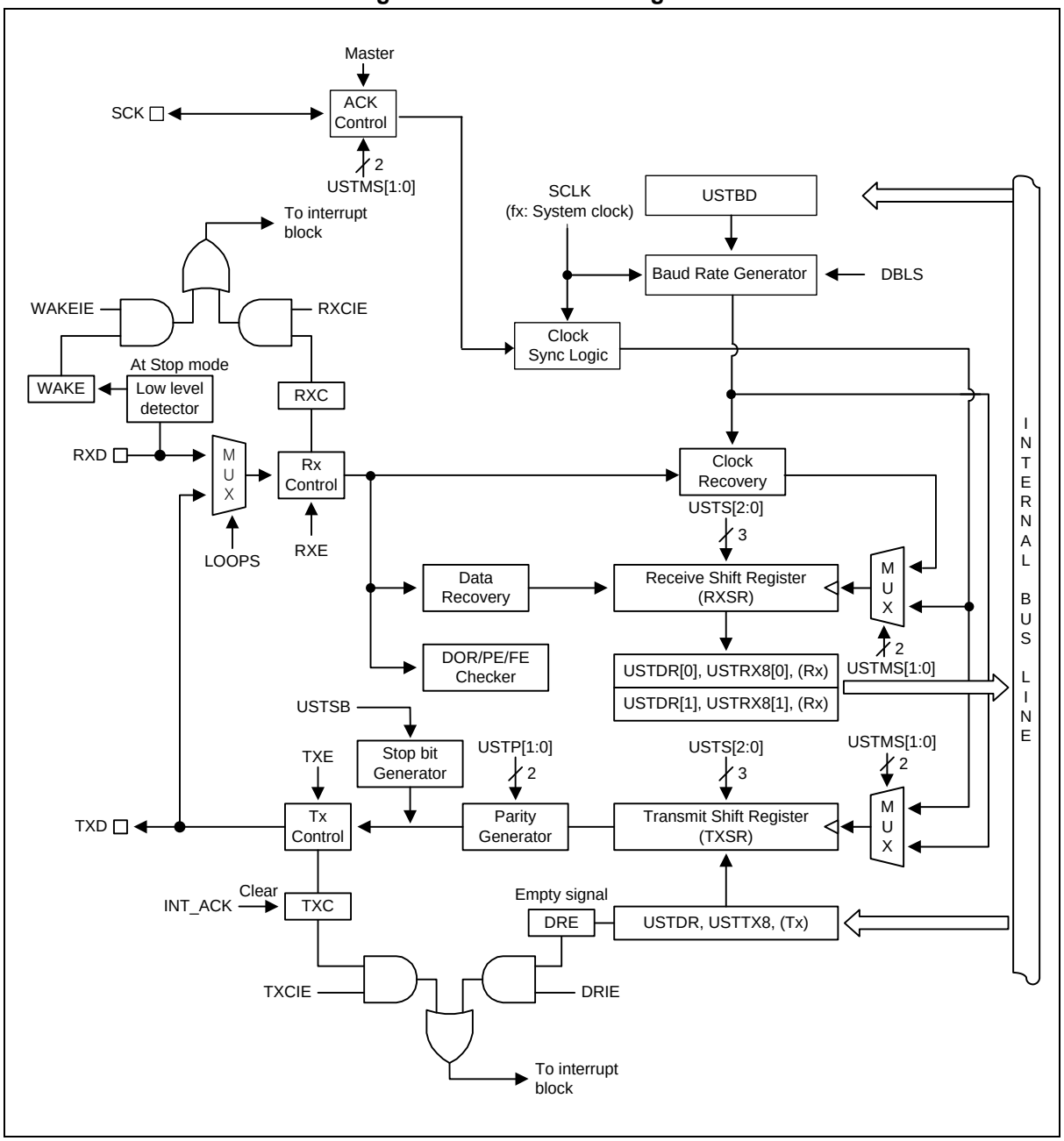
Universal Asynchronous serial Receiver and Transmitter (UART) is a highly flexible serial communication device. Its main features are listed below:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data Overrun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete

The UART has a baud rate generator, a transmitter and a receiver. A baud rate generator is used for asynchronous operation. A transmitter consists of a single write buffer, a serial shift register, parity generator and control logic, and is used for handling different serial frame formats. A write buffer allows continuous transfer of data without any delay between frames. A receiver is the most complex part of the UART module because of its clock and data recovery units. A recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USTDR) and control logic. The receiver supports identical frame formats to the transmitter's and can detect frame error, data overrun and parity errors.

15.2 UART block diagram

Figure 25. UART Block Diagram



15.3 USART SPI mode

USART can be configured to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

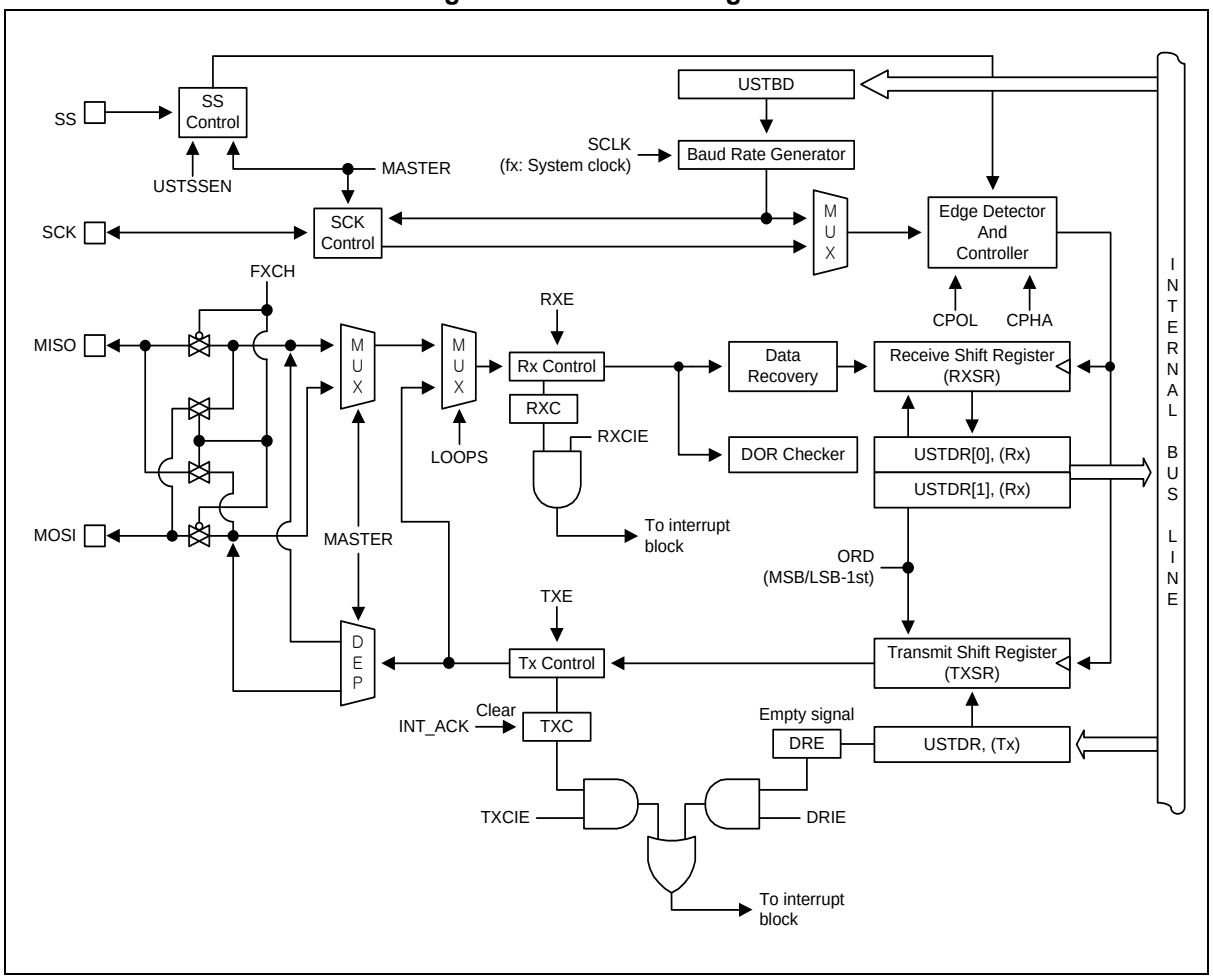
- Full Duplex, Three-wire synchronous data transfer
- Mater and Slave Operation
- Supports all four SPI modes of operation (mode 0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USTMS[1:0]=”11”), the slave select (SS) pin becomes active LOW input in slave mode operation, or can be output in master mode operation if USTSSEN bit is set to ‘0’.

Note that during SPI mode of operation, the pin RXD is renamed as MISO and TXD is renamed as MOSI for compatibility to other SPI devices.

15.4 SPI block diagram

Figure 26. SPI Block Diagram

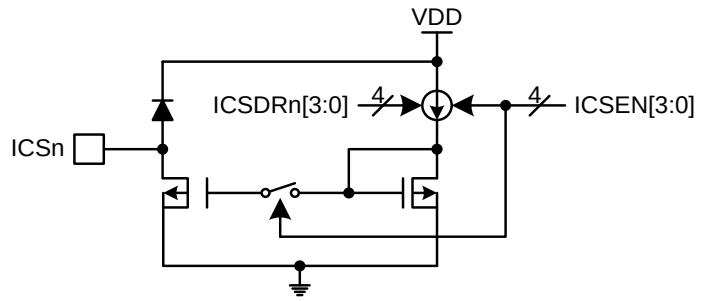


16 Constant sink current generator

Constant sink current generator supplies constant current regardless of variable I_{CS} voltage ranging from 1.5V to 3.6V. The constant current value is controlled by registers ICSDR0 and ICSDR1, and the sink current ranges from 51mA to 287mA.

16.1 Block diagram

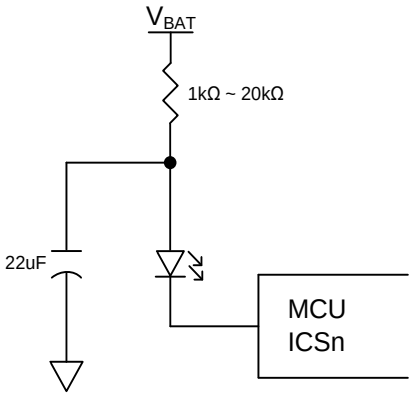
Figure 27. Constant Sink Current Generator Block Diagram (n=0 and 1)



NOTES:

1. If a sink current generator of an ICSn pin is disabled by ICSCR[3:0], the corresponding ICSn pin is high and the current flowing is zero.
2. The turn-on time of the ICSn must be less than 500us and the turn-on interval of the ICSn must be greater than 500us.

Figure 28. Constant Sink Current Generator Pin with Capacitor



17 Flash CRC and Checksum generator

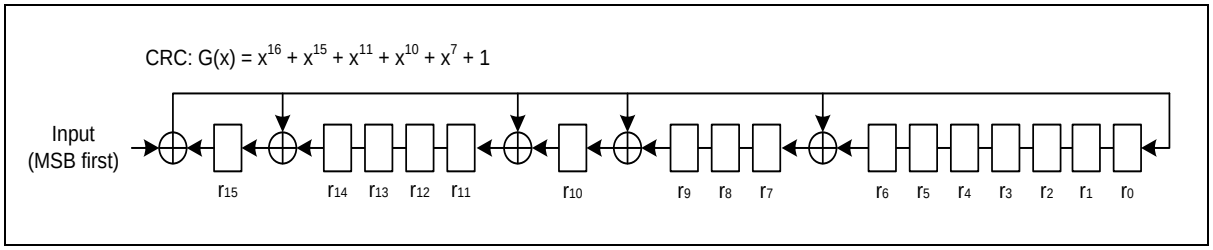
Flash CRC (Cyclic Redundancy Check) generator of A96L623 generates 16-bit CRC code bits from flash and a generator polynomial. The CRC code for each input data frame is appended to the frame.

Specifically CRC-based technique is used to verify data transmission or storage integrity. In the scope of the functional safety standards, this technique offers a means of verifying the Flash memory integrity. The flash CRC generator helps compute a signature of software during runtime, to be compared with a reference signature.

The CRC generator has the following features:

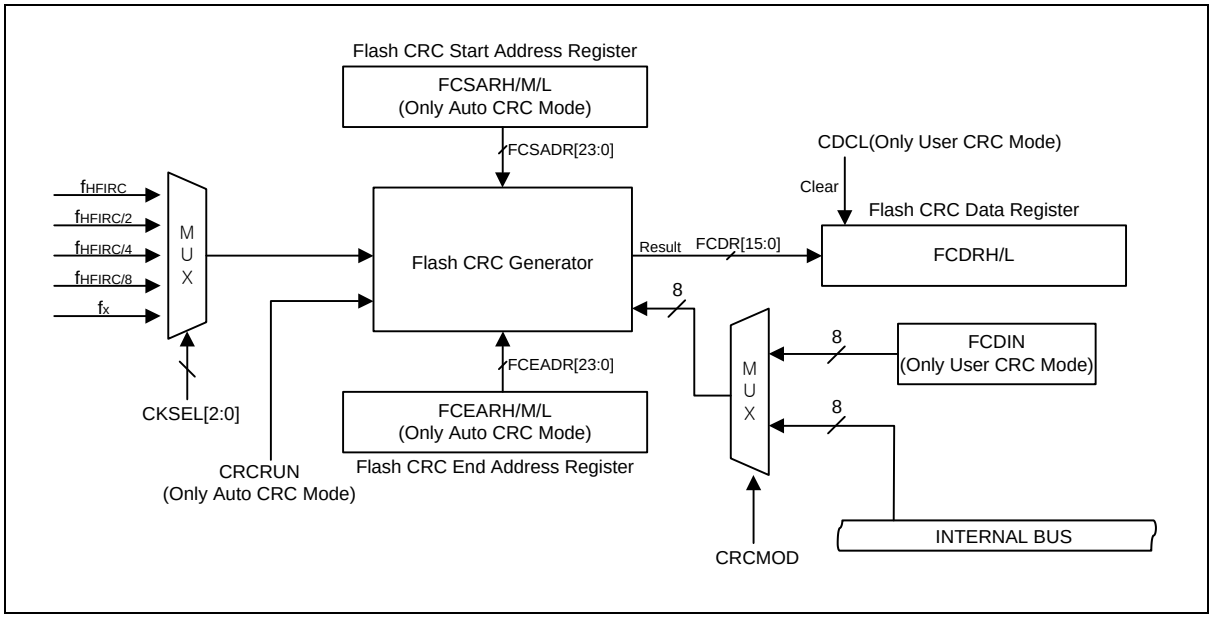
- Auto CRC and User CRC Mode
- CRC Clock : f_{IRC}, $f_{IRC}/2$, $f_{IRC}/4$, $f_{IRC}/8$ and fx (System clock)
- CRC-16 polynomial: 0x8C81 ($X^{16} + X^{15} + X^{11} + X^{10} + X^7 + 1$)

Figure 29. CRC-16 Polynomial Structure



17.1 Block diagram

Figure 30. Flash CRC/Checksum Generator Block Diagram

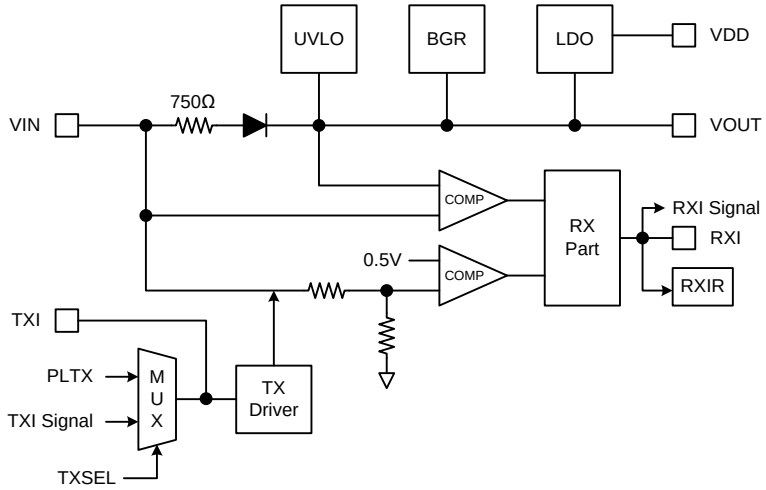


18 Power Line Transceiver

The power line transceiver has a 5V LDO for analog and digital peripherals, comparator to receive data through power line, and Tx driver to transmit data. The PLT supports communication through the power line and supplies the necessary power to each peripheral inside the MCU.

18.1 Block diagram

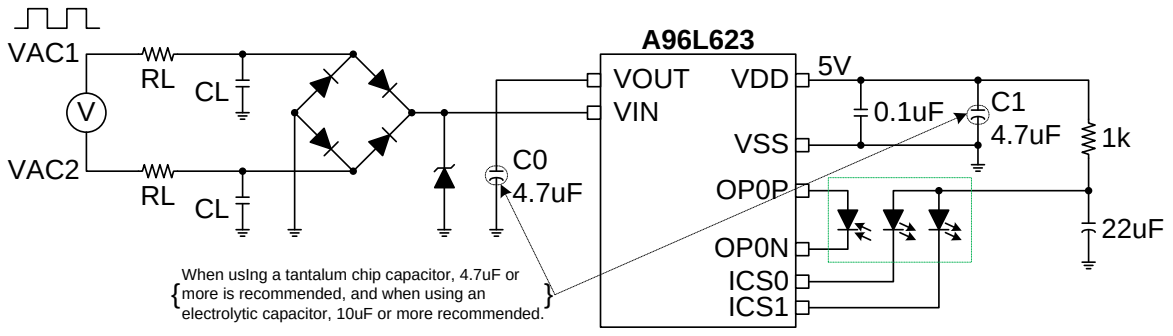
Figure 31. Power Line Transceiver Block Diagram



NOTES:

1. The TXI signal comes from the line interface block.
2. The RXI signal goes to the line interface block and the T0 block.

Figure 32. Application Circuit for PLT



Bridge Diode	Resistor (RL)	Capacitor (CL)
1N4007	12Ω	300pF
1N4148	12Ω	33pF

VAC Power	Zener Diode BV
24V	30V
28V	34V

19 Temperature Sensor

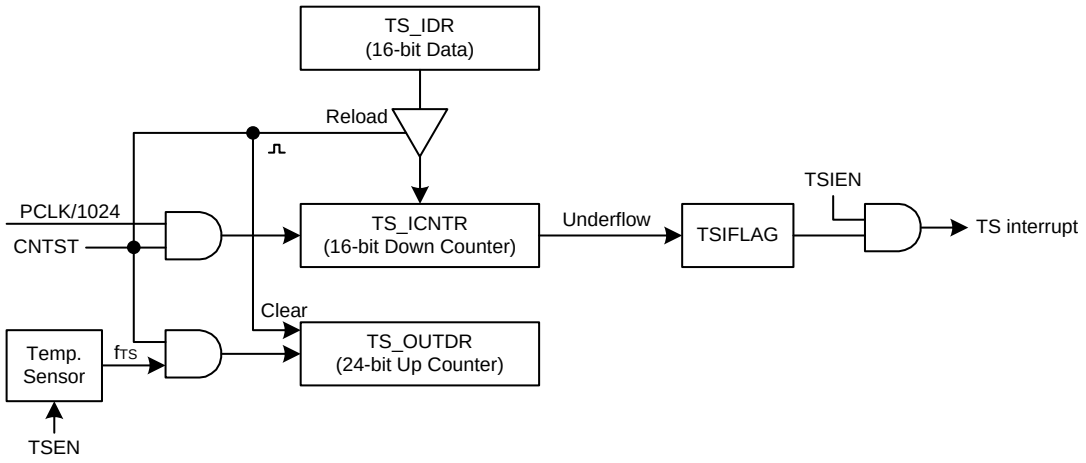
The temperature sensor is a ring-oscillator type and can be used to measure the junction temperature of the device. The nominal frequency at 25℃ is about 1.2MHz and it varies from 0.75 to 1.45 [MHz] as the temperature changes from -20 to +85 [℃].

The TS of A96L623 has following features:

- -20 to 85 [℃] wide range operating temperature
- 16-bit interval down counter to count the frequency of TS
- 24-bit data register to save the counted value of TS frequency

19.1 Block Diagram

Figure 33. Temperature Sensor Block Diagram



NOTE:

1. The CNTST bit will be cleared to “0b” after the underflow of TS_ICNTR.

20 Power down operation

A96L623 offers two power-down modes to minimize power consumption of itself. Programs under the two power saving modes IDLE and STOP, are stopped and power consumption is reduced considerably.

20.1 Peripheral operation in IDLE/STOP mode

Peripheral's operations during IDLE/STOP mode is introduced in Table 11.

Table 11. Peripheral Operation during Power-down Mode

Peripheral	IDLE mode	STOP mode
CPU	All CPU operation are disable	All CPU operation are disable
RAM	Retain	Retain
Basic Interval Timer	Operates continuously	Stop
Watchdog Timer	Operates continuously	Stop (Can be operated with WDTRC OSC)
Timer0 ~ 1	Operates continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates continuously	Stop
USART	Operates continuously	Stop
Line interface	Operates continuously	Stop
Temperature sensor	Operates continuously	Retain
Internal OSC	Oscillation	Stop
WDTRC OSC (1KHz)	Can be operated with setting value	Can be operated with setting value
Constant sink current	Retain	Retain
Power Line Transceiver	Operates continuously	Operates continuously
I/O port	Retain	Retain
Control register	Retain	Retain
Address data bus	Retain	Retain
Release method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC2), External Interrupt, WDT, USART

21 Reset

When a reset event occurs, an internal register is selected to be initialized in accordance with a reset value. Each reset value introduced in Table 12 indicates a corresponding On Chip Hardware that is to be initialized.

Table 12. Reset Value and the Relevant On Chip Hardware

On Chip Hardware	Reset Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral clock	On
Control register	Refer to peripheral registers.

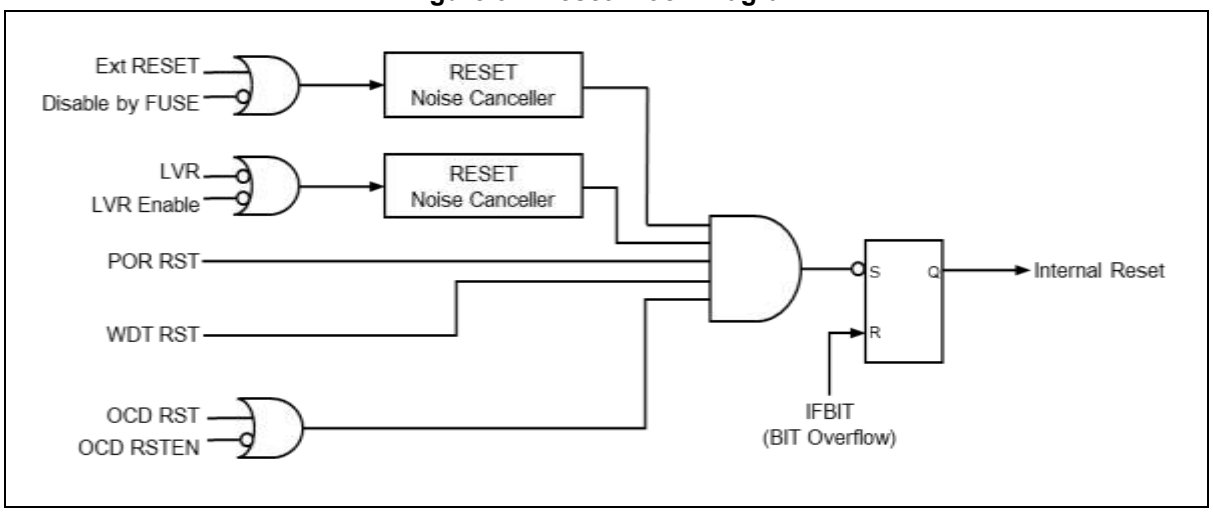
A96L623 has 5 types of reset sources as listed in the followings:

- External RESETB
- Power On RESET (POR)
- WDT overflow reset (in a case of WDTEN='1')
- Low voltage reset (in a case of LVREN='0')
- OCD RESET

21.1 Reset block diagram

Figure 34 shows a reset block of A96L623.

Figure 34. Reset Block Diagram



22 Flash memory

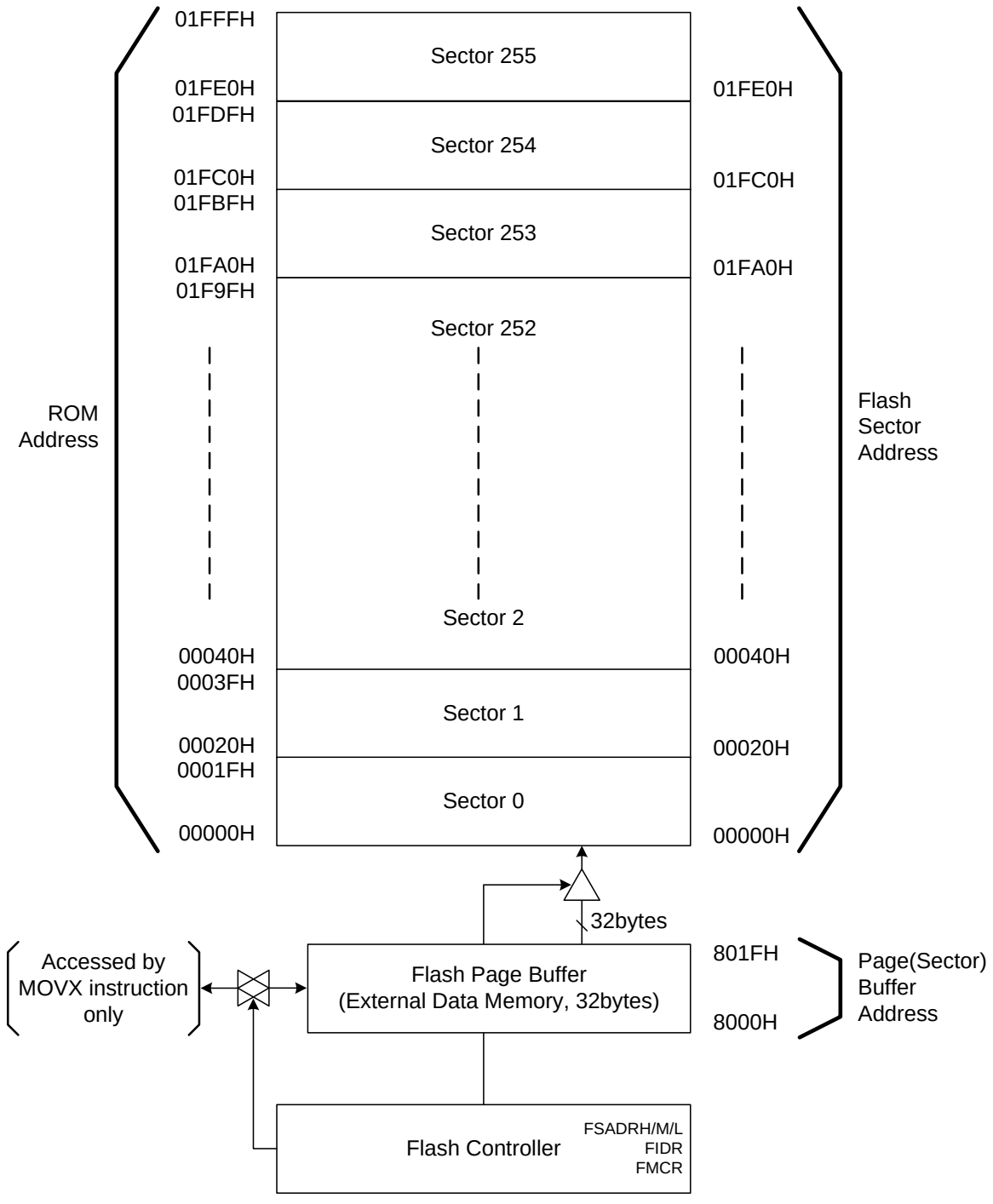
A96L623 incorporates flash memory inside. Program can be written, erased, and overwritten on the flash memory while it is mounted on a board. The flash memory can be read by ‘MOVC’ instruction and programmed in OCD, serial ISP mode or user program mode.

Followings are the main features of the Flash memory:

- Flash Size : 8Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory

22.1 Flash program ROM structure

Figure 35. Flash Program ROM Structure



NOTES:

1. The flash memory doesn't support byte erase mode.
2. The flash shouldn't be entered in erase/write mode during data flash program. So before the flash program start, the data flash busy bit (DFMBUSY) should be checked whether the bit is "1b"or not. If the bit is "1b", do not start flash program.

23 Data Flash memory

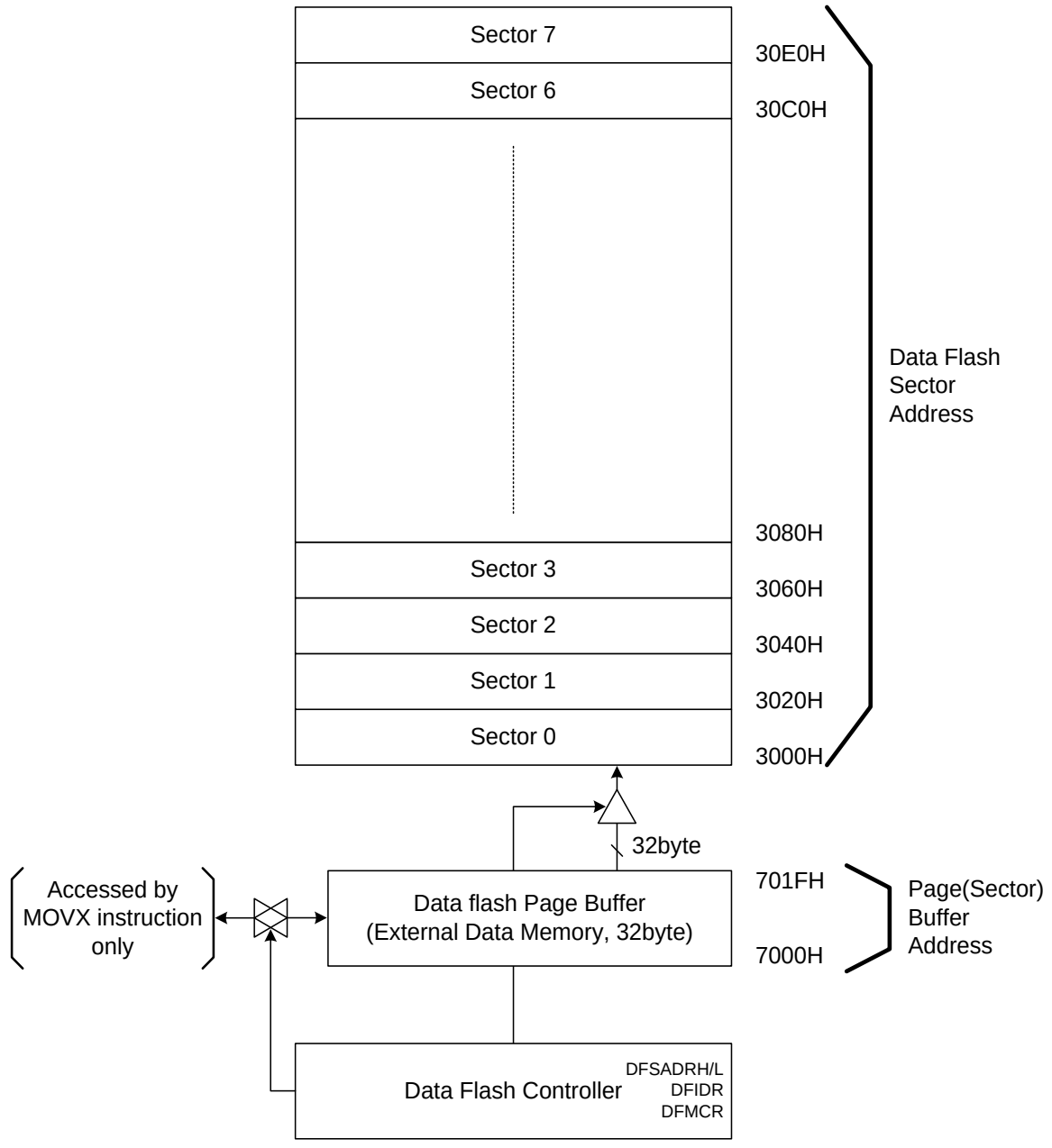
The A96L623 includes Data Flash memory of 256bytes. It can be written, erased, and overwritten. The Data Flash memory can be read by ‘MOVX’ instruction.

- Data Flash Size: 256bytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature for memory

The write/erase cycles of the internal Data Flash can be increased significantly if it is divided into smaller and used in turn. If 256bytes are divided into 8 areas with 32bytes and the each area from 1st to 8th is used up to 100,000 cycles, the total erase/write is for 800,000 cycles.

Figure 36 describes the relationship between Data Flash page buffer, Data Flash controller, and Data Flash sector addresses.

Figure 36. Data Flash Structure



NOTES:

1. The data flash memory doesn't support byte erase mode.
2. The data flash is in extended data memory area.
3. If Idle and Stop are executed on data flash erase/write, the erase/write is forcibly terminated. So before entering Idle and Stop mode, the data flash busy bit (DFMBUSY) should be checked whether the bit is "1b" or not. If the bit is "1b", do not enter Idle and Stop mode.

24 Electrical characteristics

24.1 Absolute maximum ratings

Table 13. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	VIN	-0.3 ~ +44	V	–
Normal voltage Pin	VI	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS VDD: Internal LDO output voltage (5.0V)
	VO	-0.3 ~ VDD+0.3	V	
	IOH	-20	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	∑IOH	-40	mA	Maximum current ($\sum I_{OH}$)
	IOL	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	∑IOL	120	mA	Maximum current ($\sum I_{OL}$)
Constant sink pin	IOL	390	mA	Maximum current sink by ICS0 and ICS1
Total power dissipation	PT	600	mW	–
Operating temperature	TOP	-40 ~ +85		–
Storage temperature	TSTG	-65 ~ +150	°C	–

Caution: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

24.2 ADC characteristics

Table 14. ADC Characteristics

T_A=-40℃ to +85℃, VIN=8.5V to 42V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	—	—	—	10	—	bit
Integral linear error	ILE	f_{ADCCK}=2MHz	—	—	±3	LSB
Differential linearity error	DLE		—	—	±1	
Top offset error	TOE		—	—	±5	
Zero offset error	ZOE		—	—	±5	
Conversion time	t_{CON}	—	14	—	—	us
Analog input voltage	V_{AN}	—	VSS	—	VDD	V
Sample/ hold time	t_{SH}	—	3	—	—	us
A/DC input leakage current	IAN	—	—	—	2	uA
A/DC current	I_{ADC}	Enable	—	500	750	uA
		Disable	—	—	0.1	uA

NOTES:

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (VDD).

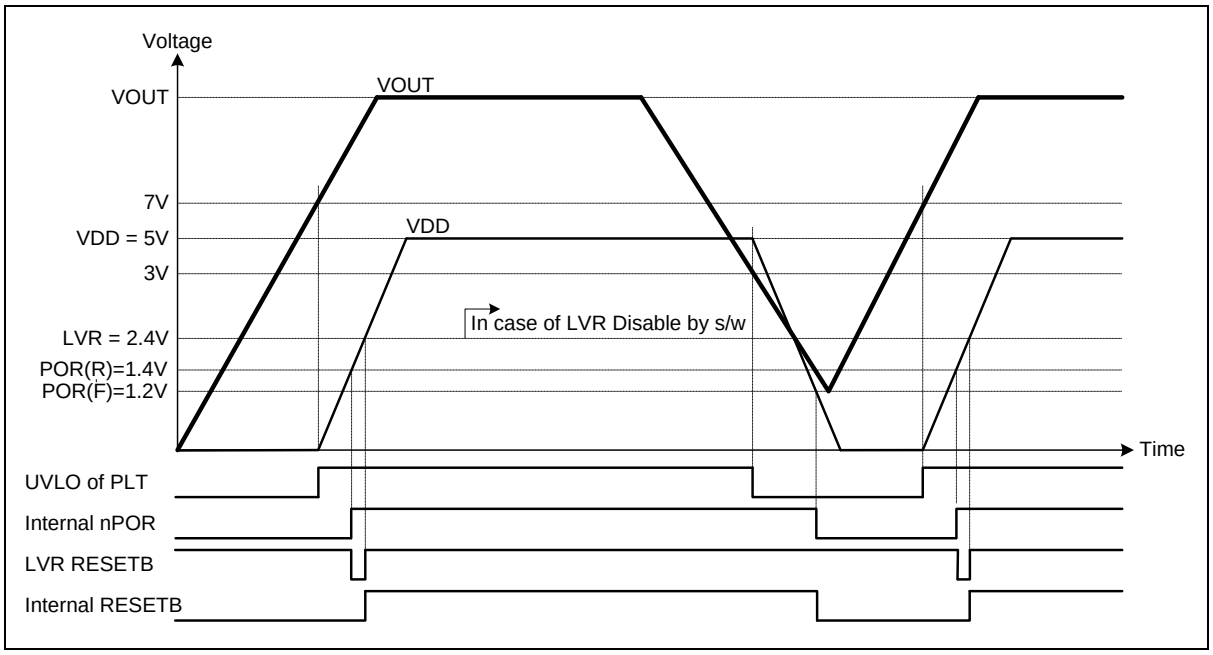
24.3 Power on Reset

Table 15. Power on Reset Characteristics

(T_A=-40℃ to +85℃, VDD=2.7V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET release level	V_{POR}	–	–	1.4	–	V
VOUT voltage rising time	t_{ROUT}	0.2V to 10V	0.01	–	50	V/ms
VDD voltage rising time	t_R	0.2V to 2.7V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	0.2	–	uA

Figure 37. Power-On Reset and UVLO Timing



24.4 Low voltage reset characteristics

Table 16. LVR Characteristics

(T_A=-40℃ to +85℃, VIN=8.5V V to 42V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection level	V_{LVR}	VDD	_	2.4	3.0	V
Hysteresis	△V	–	–	10	100	mV
Minimum pulse width	t_{LW}	–	100	–	–	us
LVR current	I_{LVR}	Enable	_	0.8	1.6	uA
		Disable	_	–	0.1	

24.5 Operational amplifier 0/1 characteristics

Table 17. Operational Amplifier 0/1 Characteristic

(T_A=-40℃ to +85℃, VIN=24V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input offset voltage	V_{OF}	VDD=5.0V		—	±10	±100	uV
Input offset current	I_{OF}	VDD=5.0V, VCM=0V		—	15	50	pA
Common-mode rejection ratio	CMRR	VDD=5.0V, DC VCM=0V to VDD-1.2V		80	100	—	dB
Power supply rejection ration	PSRR	VDD=5.0V		80	100	—	
Open loop voltage gain	—	VDD=5.0V		100	120	—	dB
Gain error	ERR	VDD=5.0V, VIN ≥ 0.1V, x11 VIN<(Input x Gain)		—	—	1	%
Input Common-mode voltage range	V_{IN}	VDD=5.0V		0	—	VDD-1.2	V
Output voltage range	V_O	VDD=5.0V, RL=10kΩ		VSS+0.1	—	VDD-0.1	V
Output short circuit current	ISCH	VDD=5.0V, Absolute		—	20	—	mA
	ISCL			—	20	—	
Gain bandwidth	f_{GB}	VDD=5.0V		0.5	1	—	MHz
Voltage follower pulse response	T_{AR}	VDD=5.0V, Small Signal		—	5	10	us
OP-AMP 0/1 total current	I_{AMP}	Enable	VDD=5.0V, No Load	—	150	220	uA
		Disable		—	—	0.1	
Enable time of AMP0/1	t_{ON}	VDD=5.0V, Gain=x31, RL=10KΩ with 50pF		—	—	150	us
Input noise voltage density	e_{ni}	Input Referred f=1Hz		—	100	—	nV/rtHz
		Input Referred f=1KHz		—	100	—	nV/rtHz
Slew rate	S_R	VDD=5.0V, RL=10K, CL=50pF		—	0.7	—	V/us
Input Capacitance	C_{IN}	Common mode, T_A = 25°C		—	6	—	pF
Phase margin	P_M	VDD=5.0V, RL=10K, CL=50pF		—	65	—	Degrees
Chopping clock	f_{CHOP}	—		125	—	167	kHz

24.6 Internal RC oscillator characteristics

Table 18. Internal RC Oscillator Characteristics

(T_A=-40℃ to +85℃, VIN=42V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{IRC}	—	—	4	—	MHz
Tolerance	—	T_A = -10°C to +50°C, with user (S/W) trim.	—	—	±1.0	%
		T_A = -10°C to +50°C			±2.0	
		T_A = -40°C to +85°C			±3.0	
Clock duty ratio	T_{OD}	—	40	50	60	%
Stabilization time	T_{FS}	—	—	—	4	us

24.7 Internal watchdog timer RC oscillator characteristics

Table 19. Internal WDTRC Oscillator Characteristics

(T_A=-40℃ to +85℃, VIN=24V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{WDTRC}	—	0.5	1	2	kHz
Stabilization time	t_{WDTS}	—	—	—	1	ms
WDTRC current	I_{WDTRC}	Enable	—	1	—	uA
		Disable	—	—	0.1	

24.8 Temperature Sensor characteristics

Table 20. Temperature Sensor Characteristics

(T_A=-20℃ to +85℃, VIN=24V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature linearity	T_{LIN}	–	–	±4	–	°C
Frequency variation	ΔF	(F(T2) – F(T1)) ÷ (T2 – T1)	1.8	3.2	5.7	kHz/℃
Frequency deviation	–	ΔF ÷ F(30)	0.21	0.29	0.35	%
Sensor current	I_{TS}	Enable	–	10	20	uA
		Disable	–	–	10	nA
Startup time	t_{START}	–	–	–	500	usec

NOTES:

1. Temperature = {(F(T) – F(30)) ÷ ΔF} + 30 [℃] Where: T1 = 30℃, T2 = 85℃
2. F(T1) [kHz] is the temperature sensor output frequency acquired at 30℃.
3. F(T2) [kHz] is the temperature sensor output frequency acquired at 85℃.
4. F(T) [kHz] is the temperature sensor output frequency acquired at an arbitrary temperature.

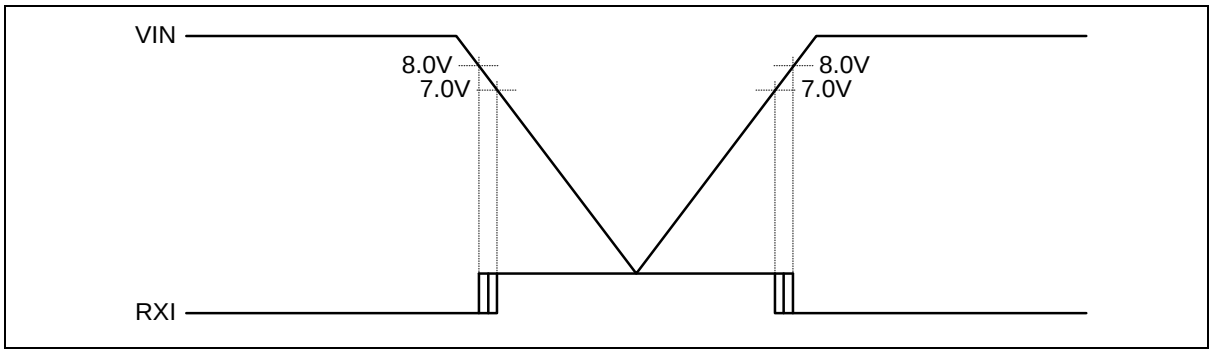
24.9 Power Line Transceiver Characteristics

Table 21. Power Line Transceiver Characteristics

(T_A=+25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VIN	–	8.5	24	42	V
LDO Output Voltage	VDD	IOUT = 1mA, VOUT = 24V	4.85	5.0	5.15	V
	dVDD	IOUT = 1mA to 5mA, VOUT = 24V	–	15	20	mV
		IOUT = 5mA to 20mA, VOUT = 24V	–	15	45	
LDO Output Tolerance	Vtol	VDD = 5.0V @ -10 to +60°C	-3	–	+3	%
PSRR	–	f = 100Hz	50	–	–	dB
VIN Serial Resistor	RIN	–	0.55	0.75	0.95	kΩ
Inrush Current	IVIN1	VIN = 0V to 24V, @Rise time 10ms	–	24	35	mA
TXI Current	IVIN2	VIN = 7V, VOUT = 24V	60	–	–	mA
Min. VIN Input Voltage for RXI High	VRXH1	VOUT = 8.5V	6.0	–	8.0	V
Min. (VOUT – VIN) Voltage for RXI High	VRXH2	VOUT = 24V	4.0	–	8.0	V

Figure 38. VIN and RXI Timing



24.10 DC characteristics

Table 22. DC Characteristics

(T_A=-40℃ to +85℃, VIN=24V, VDD=5V, VSS=0V, f_{IRC}=4MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH1}	All input pins except VIH2, RESETB	0.8VDD	—	VDD	V
	V_{IH2}	P00, P01, and P04	0.7VDD	—	VDD	
Input low voltage	V_{IL1}	All input pins except VIL2, RESETB	—	—	0.2VDD	V
	V_{IL2}	P00, P01, and P04	—	—	0.3VDD	
Output high voltage	V_{OH}	All output ports, IOH = – 4mA	VDD-1.0	—	—	V
Output low voltage	V_{OL}	All output ports, IOL = 10mA	—	—	1.0	V
Input high leakage current	I_{IH}	All output ports	—	—	1.0	uA
Input low leakage current	I_{IL}	All output ports	-1.0	—	—	uA
Pull-up resistor	R_{PU1}	VI=0V, T_A=25℃, All Input ports	25	50	100	kΩ
	R_{PU2}	VI=0V, T_A=25℃, RESETB	150	250	400	kΩ
Supply current	I_{DD1} (RUN)	f_{IRC} = 4MHz	—	500	750	uA
		f_{IRC} = 2MHz	—	340	510	
		f_{IRC} = 1MHz	—	260	390	
	I_{DD2} (IDLE)	f_{IRC} = 4MHz	—	180	270	uA
		f_{IRC} = 2MHz	—	150	225	
		f_{IRC} = 1MHz	—	140	210	
	I_{DD5}	STOP, T_A= 25℃	—	60.5	93.0	uA

NOTES:

1. Where the f_{IRC} is an internal RC oscillator.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current include the current of the power-on reset (POR) block and the power line transceiver.

24.11 Constant sink current electrical characteristics

Table 23. Constant Sink Current Electrical Characteristics

(T_A=-40℃ to +85℃, VIN=24V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Constant sink current	I_{CS}	V_{ICS}=2.0V T_A=25℃	ICSDR[3:0] = 0	-7%	51	+7%	mA
			ICSDR[3:0] = 1	-7%	67	+7%	
			ICSDR[3:0] = 2	-7%	83	+7%	
			ICSDR[3:0] = 3	-7%	99	+7%	
			ICSDR[3:0] = 4	-7%	115	+7%	
			ICSDR[3:0] = 5	-7%	131	+7%	
			ICSDR[3:0] = 6	-7%	147	+7%	
			ICSDR[3:0] = 7	-7%	163	+7%	
			ICSDR[3:0] = 8	-7%	179	+7%	
			ICSDR[3:0] = 9	-7%	195	+7%	
			ICSDR[3:0] = 10	-7%	211	+7%	
			ICSDR[3:0] = 11	-7%	227	+7%	
			ICSDR[3:0] = 12	-7%	242	+7%	
			ICSDR[3:0] = 13	-7%	257	+7%	
			ICSDR[3:0] = 14	-7%	272	+7%	
			ICSDR[3:0] = 15	-7%	287	+7%	
		V_{ICS}=1.5V to 2.5V	ICSDR[3:0] = n n: 0 to 15	-15%	Typ.	+15%	
		V_{ICS}=2.5V to 3.6V	ICSDR[3:0] = n n: 0 to 15	-20%	Typ.	+20%	

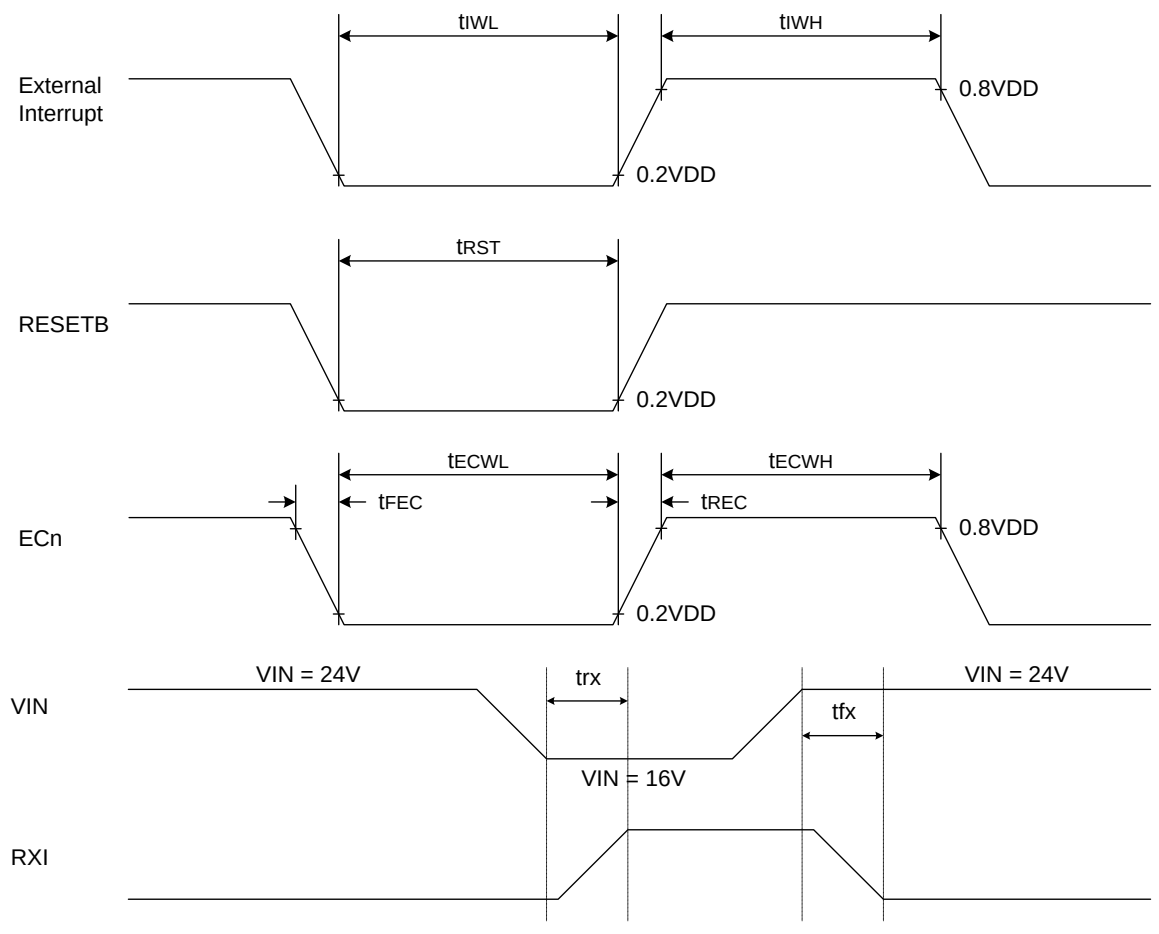
24.12 AC characteristics

Table 24. AC Characteristics

(T_A=-40℃ to +85℃, VIN=8.5V to 42V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB input low width	t_{RST}	—	10	—	—	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt	200	—	—	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	ECn, Where n=0, 1, and 2	200	—	—	
External counter transition time	t_{REC}, t_{FEC}	ECn, Where n=0, 1, and 2	20	—	—	
Wake-up from idle/stop mode	t_{WU0}	From IRC	16	—	—	us
RXI response time	trx, tfx	VOUT = 24V	—	4	—	us

Figure 39. AC Timing



NOTE:

1. n =0, 1 and 2.

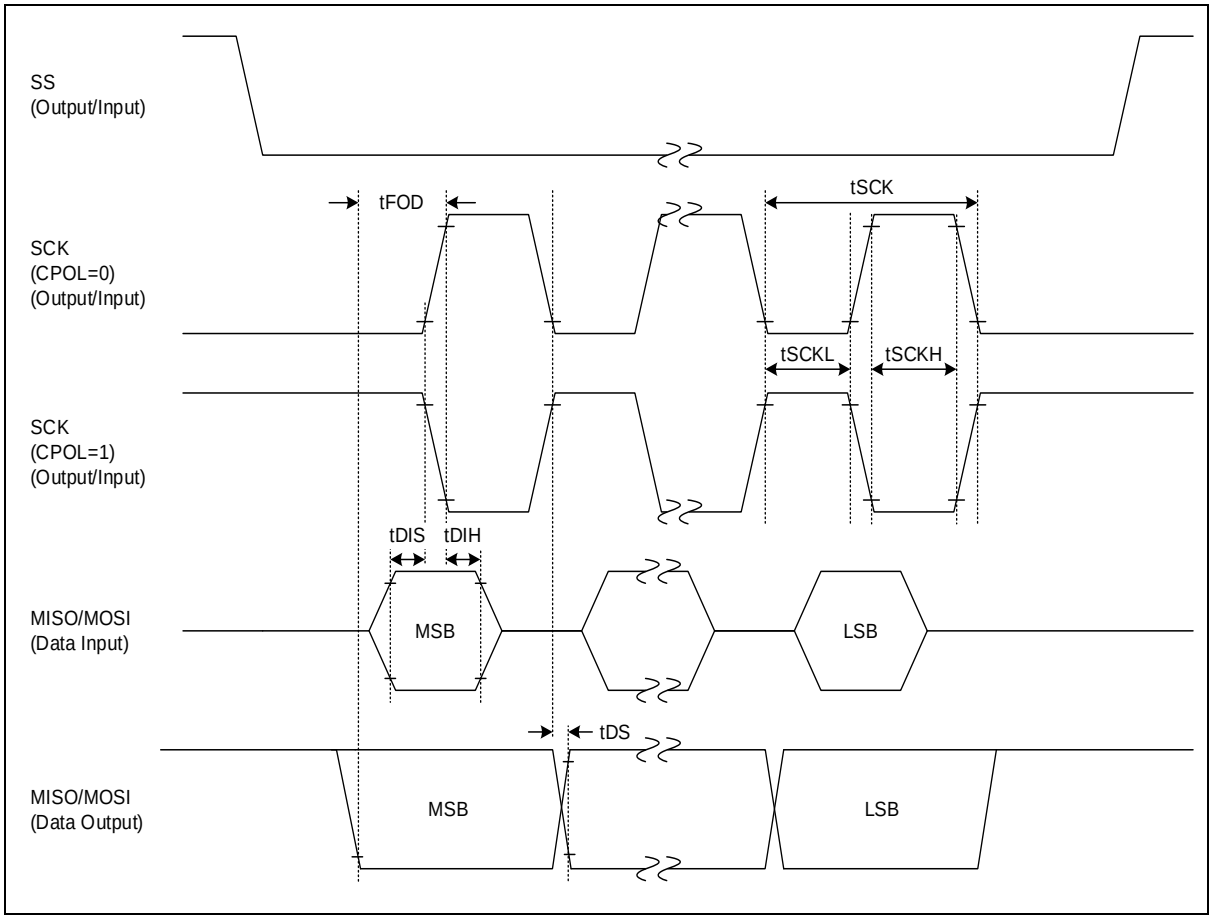
24.13 SPI characteristics

Table 25. SPI Characteristics

(T_A=-40℃ to +85℃, VIN=24V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output clock pulse period	t_{SCK}	Internal SCK source	1000	—	—	ns
Input clock pulse period		External SCK source	1000	—	—	
Output clock high, low pulse width	t_{SCKH} t_{SCKL}	Internal SCK source	400	—	—	
Input clock high, low pulse width		External SCK source	400	—	—	
First output clock delay time	t_{FOD}	Internal/external SCK source	500	—	—	
Output clock delay time	t_{DS}	—	—	—	125	
Input setup time	t_{DIS}	—	500	—	—	
Input hold time	t_{DIH}	—	500	—	—	

Figure 40. SPI Timing



24.14 UART timing characteristics

Table 26. UART Timing Characteristics

(T_A=-40℃ to +85℃, VIN=24V, fx=1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial port clock cycle time	t_{SCK}	13.92	t_{CPU} x 16	18.08	us
Output data setup to clock rising edge	t_{S1}	6.5	t_{CPU} x 13	—	
Clock rising edge to input data valid	t_{S2}	—	—	6.5	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 0.1	t_{CPU}	—	
Input data hold after clock rising edge	t_{H2}	0	—	—	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	5.5	t_{CPU} x 8	10.5	

Figure 41. UART Timing Characteristics

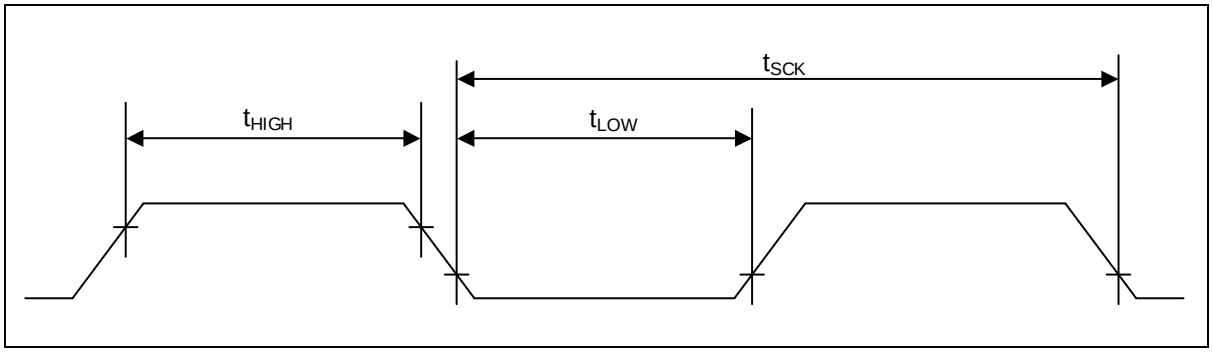
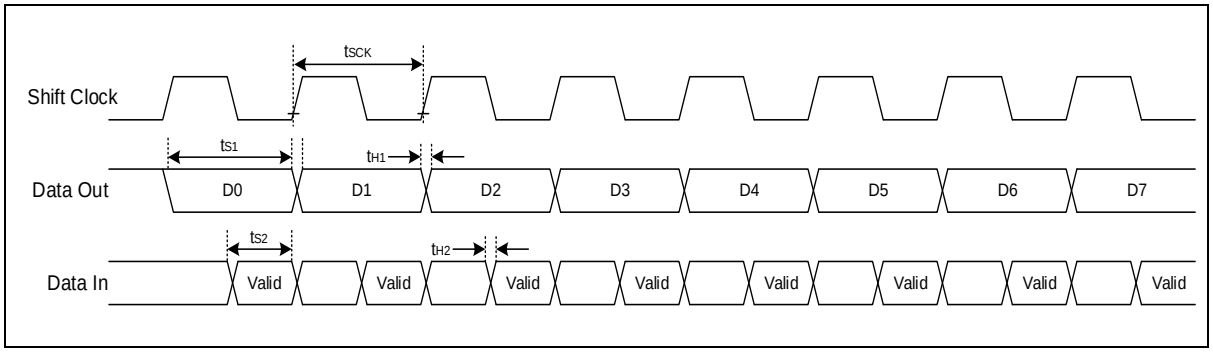


Figure 42. Timing Waveform of UART Module



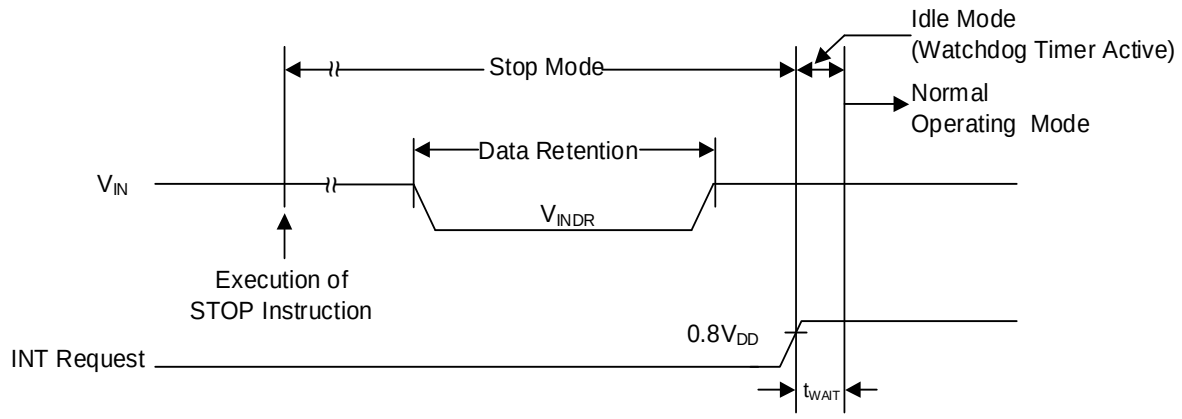
24.15 Data retention voltage in STOP mode

Table 27. Data Retention Voltage in STOP Mode

(T_A=-40℃ to +85℃, VIN=8.5V to 42V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{INDR}	—	8.5	—	42	V
Data retention supply current	I_{INDR}	VINDR = 8.5V (T_A= 25°C), STOP mode	—	—	61	uA

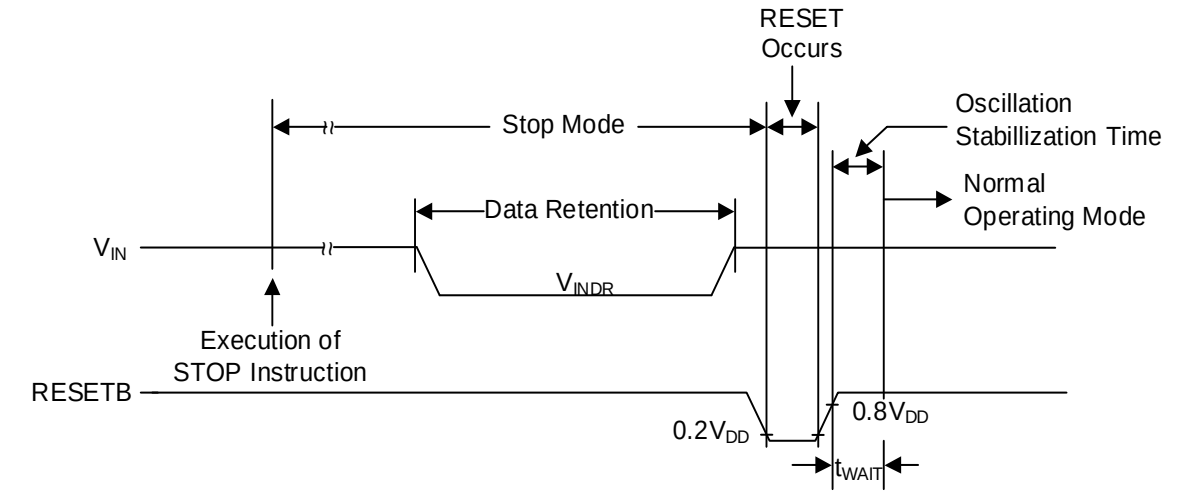
Figure 43. STOP Mode Release Timing when Initiated by an Interrupt



NOTE:

1. t_{WAIT} is the same as (the selected bit overflow of BIT) x 1/ (BIT clock)

Figure 44. STOP Mode Release Timing when Initiated by RESETB



NOTE:

1. t_{WAIT} is the same as (4096 x 4 x 4/f_{IRC}) = (16.4 ms at fx=4MHz)

24.16 Internal flash characteristics

Table 28. Internal Flash Characteristics

(T_A= +25℃, VIN=8.5V to 42V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector write time	t_{FSW}	—	—	3.0	3.5	ms
Sector erase time	t_{FSE}	—	—	3.0	3.5	
Code write protection time	t_{FHL}	—	—	3.0	3.5	
Page buffer reset time	t_{FBR}	—	—	—	5	us
Flash program Voltage	V_{PGM}	On erase/write	—	5	—	V
System clock frequency	f_{SCLK}	—	0.5	—	—	MHz
Endurance of write/erase	N_{FWE}	Sector erase, byte write	10,000	—	—	cycles

24.17 Internal Data Flash characteristics

Table 29. Internal Data Flash Characteristics

(T_A= +25℃, VIN=8.5V to 42V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector write time	t_{DFSW}	—	—	3.0	3.5	ms
Sector erase time	t_{DFSE}	—	—	3.0	3.5	
Page buffer reset time	t_{DFBR}	—	—	—	5	us
Data Flash program voltage	V_{DPGM}	On erase/write	—	5	—	V
System clock frequency	f_{SCLK}	—	0.5	—	—	MHz
Endurance of write/erase	NE_{WE}	Sector erase, byte write	100,000	—	—	cycles

24.18 Input/output capacitance characteristics

Table 30. I/O Capacitance Characteristics

(T_A=-40℃ to +85℃, VIN=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	fx=1MHz Unmeasured pins are connected to VSS.	—	—	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

24.19 Typical characteristics

Figures and tables introduced in this chapter can be used only for design guidance, and are not tested or guaranteed. In graphs or tables some data may exceed specified operating range, and can be only for information. The device is guaranteed to operate properly only within the specified range.

The data presented in this chapter is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

Figure 45. RUN (IDD1) Current

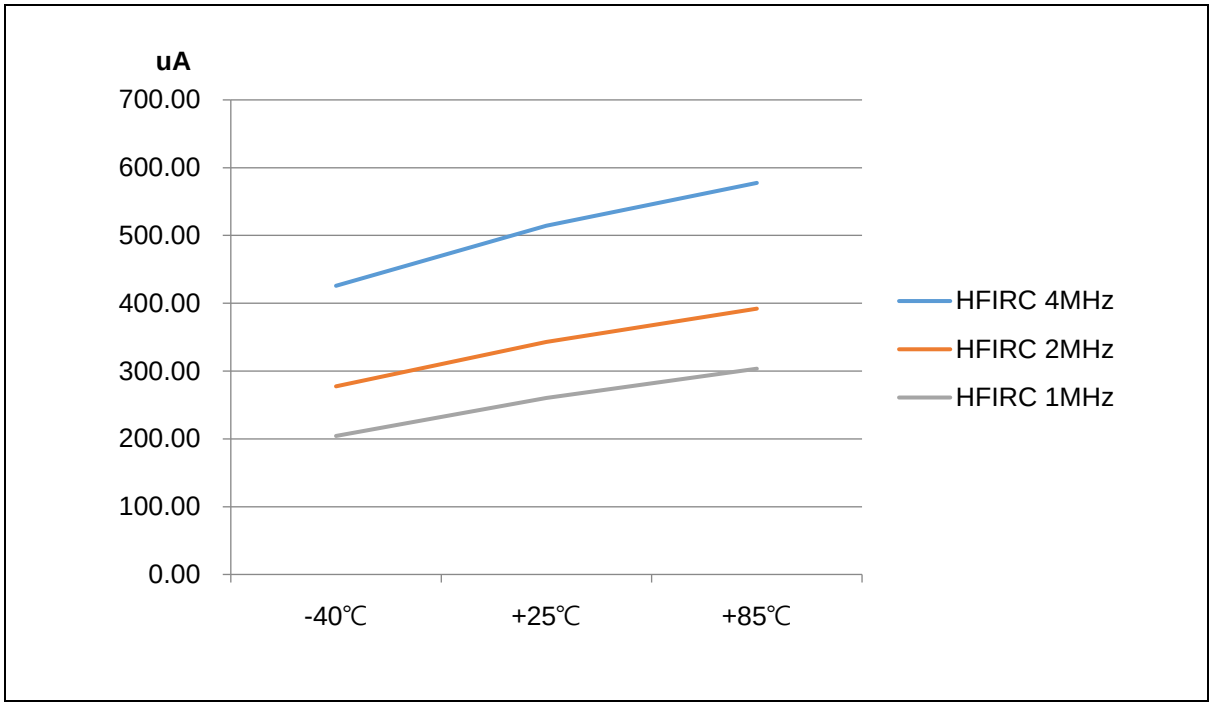


Figure 46. IDLE (IDD2) Current

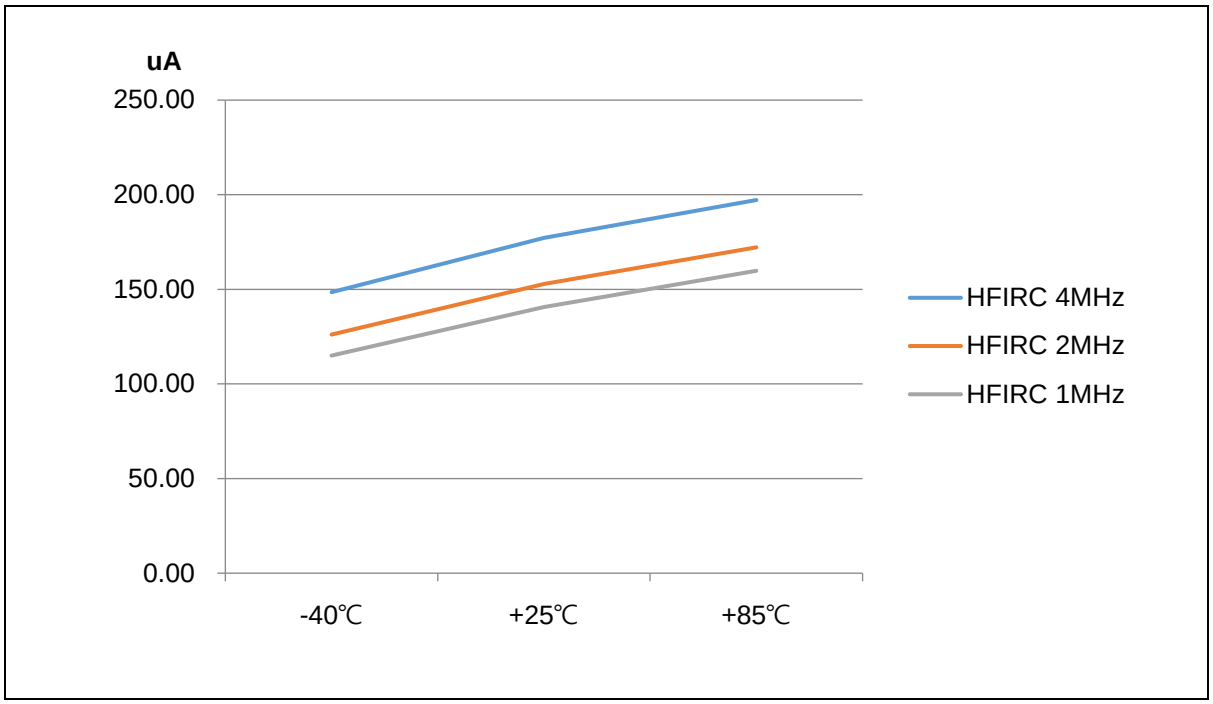
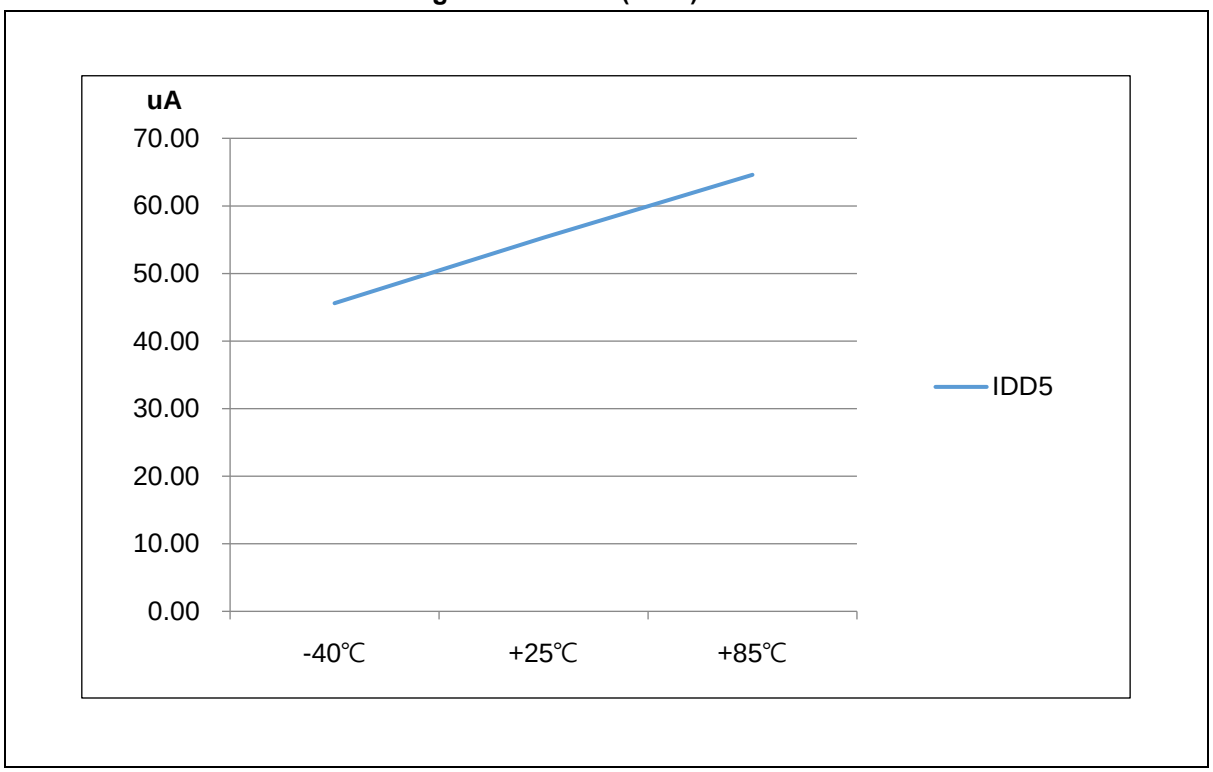


Figure 47. STOP (IDD5) Current



25 Recommended circuit and layout

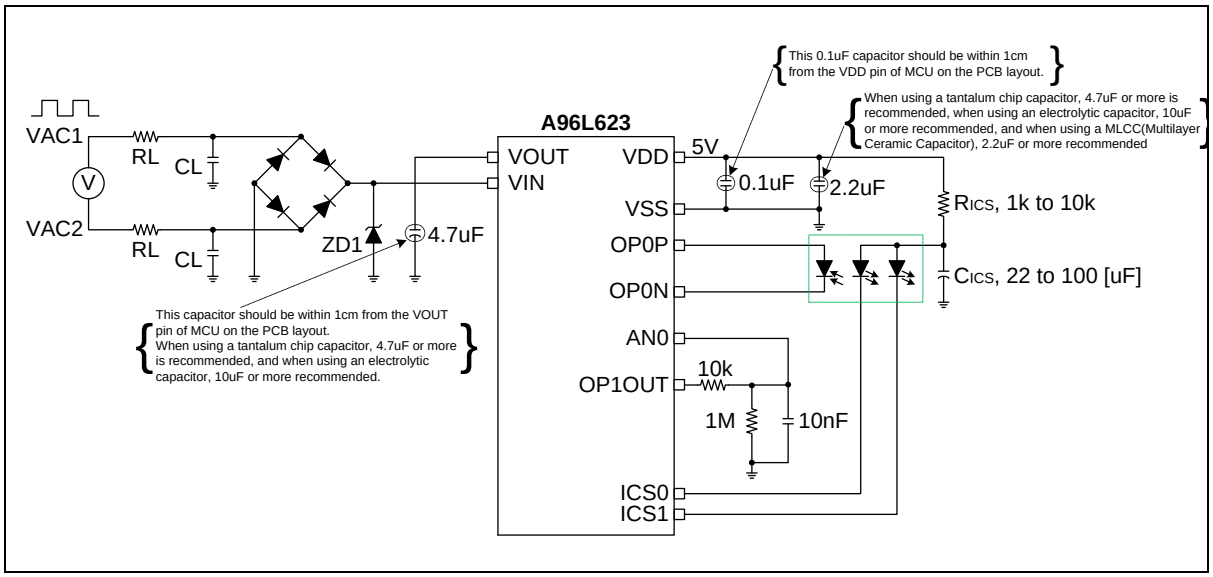
The Figure 48 is a recommended circuit and layout for network type smoke detector.

- R_{ICS} and C_{ICS}: Adjust the values according to the cycle of turning on ICSn.

  The applicable power source is up to 5V (VDD).

- ZD1: Apply a Zener diode of 30V or less to improve noise immunity.

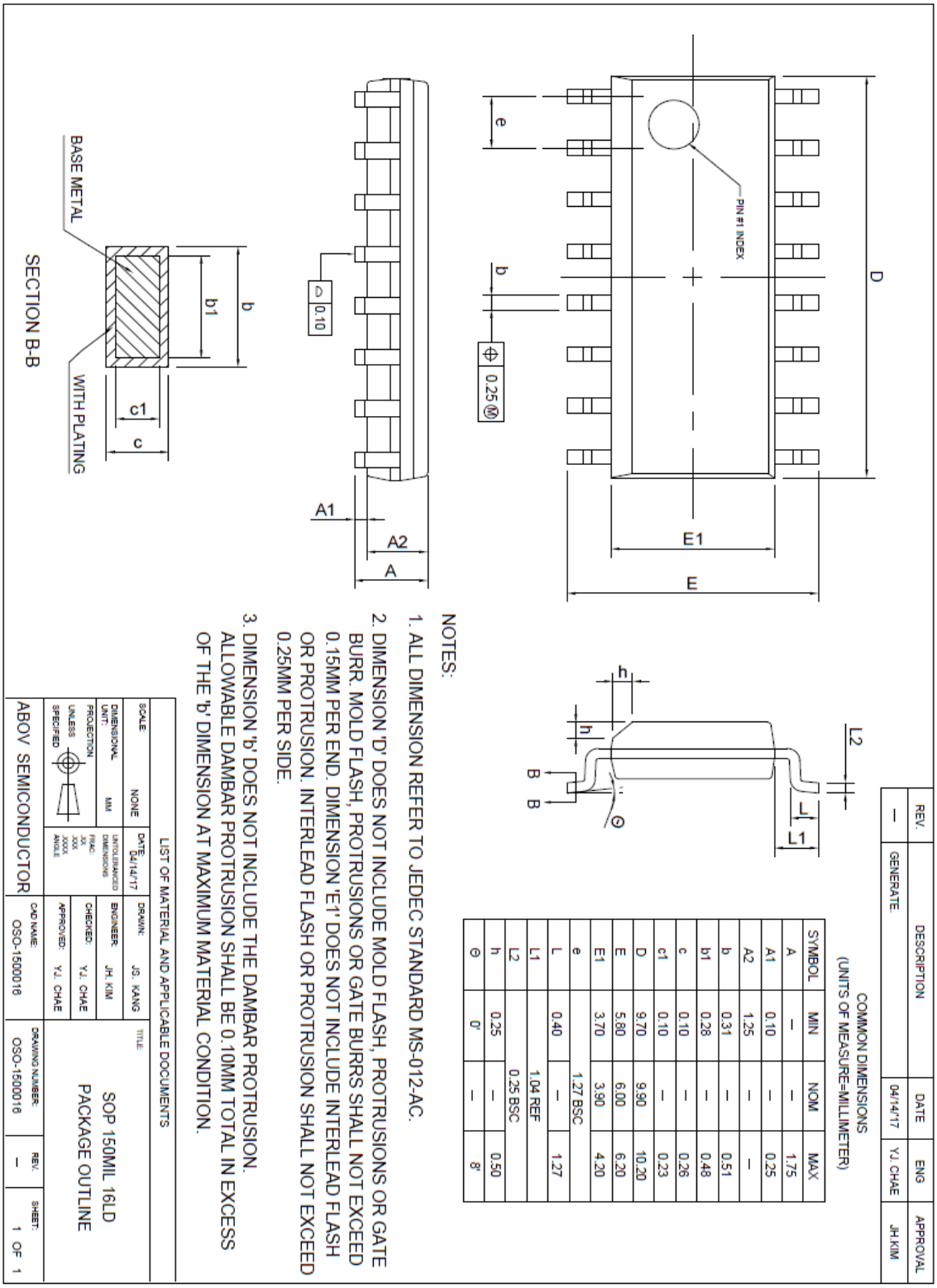
Figure 48. Recommended Circuit and Layout



26 Package information

26.1 16 SOPN package information

Figure 49. 16 SOPN Package Outline

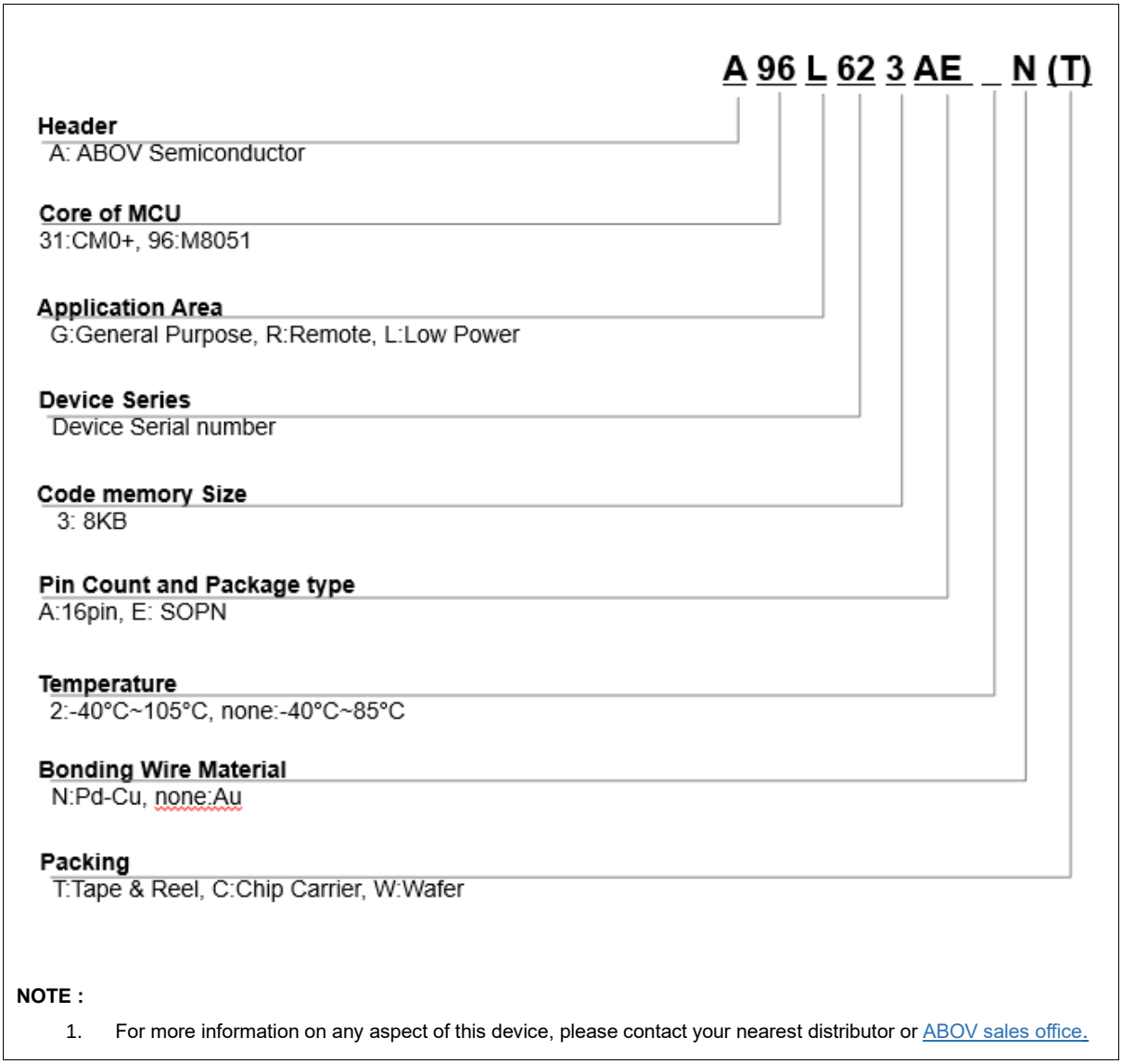


27 Ordering information

Table 31. A96L623 Device Ordering Information

Device name	Flash	IRAM/XRAM	Data Flash	ADC	I/O ports	Package type
A96L623AE	8 Kbyte	256/256 bytes	256 bytes	5 inputs	10	16 SOPN

Figure 50. A96L623 Device Numbering Nomenclature



NOTE :

1. For more information on any aspect of this device, please contact your nearest distributor or ABOV sales office.

28 Development tools

This chapter introduces wide range of development tools for A96L623. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

28.1 Compiler

ABOV semiconductor does not provide any compiler for A96L623. However, since A96L623 has Mentor 8051 as its CPU core, you can use all kinds of third party's standard 8051 compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Please visit our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

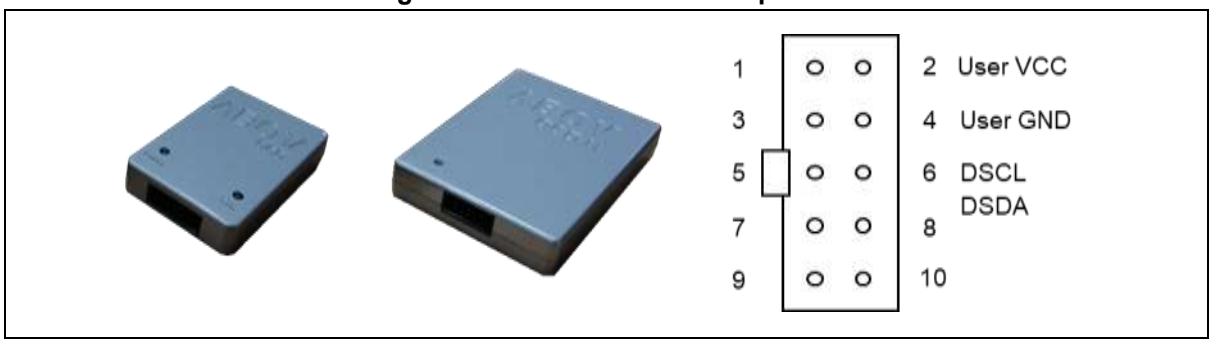
28.2 OCD (On-Chip Debugger) emulator and debugger

The OCD emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the OCD is provided in section 27.5 Circuit design guide later part in this chapter. More detailed information about the OCD, please visit our website www.abovsemi.com and download the debugger S/W and documents.

Figure 51. OCD and Pin Descriptions



Following is the OCD mode connections:

- DSCL (A96L623 P13 port)
- DSDA (A96L623 P14 port)

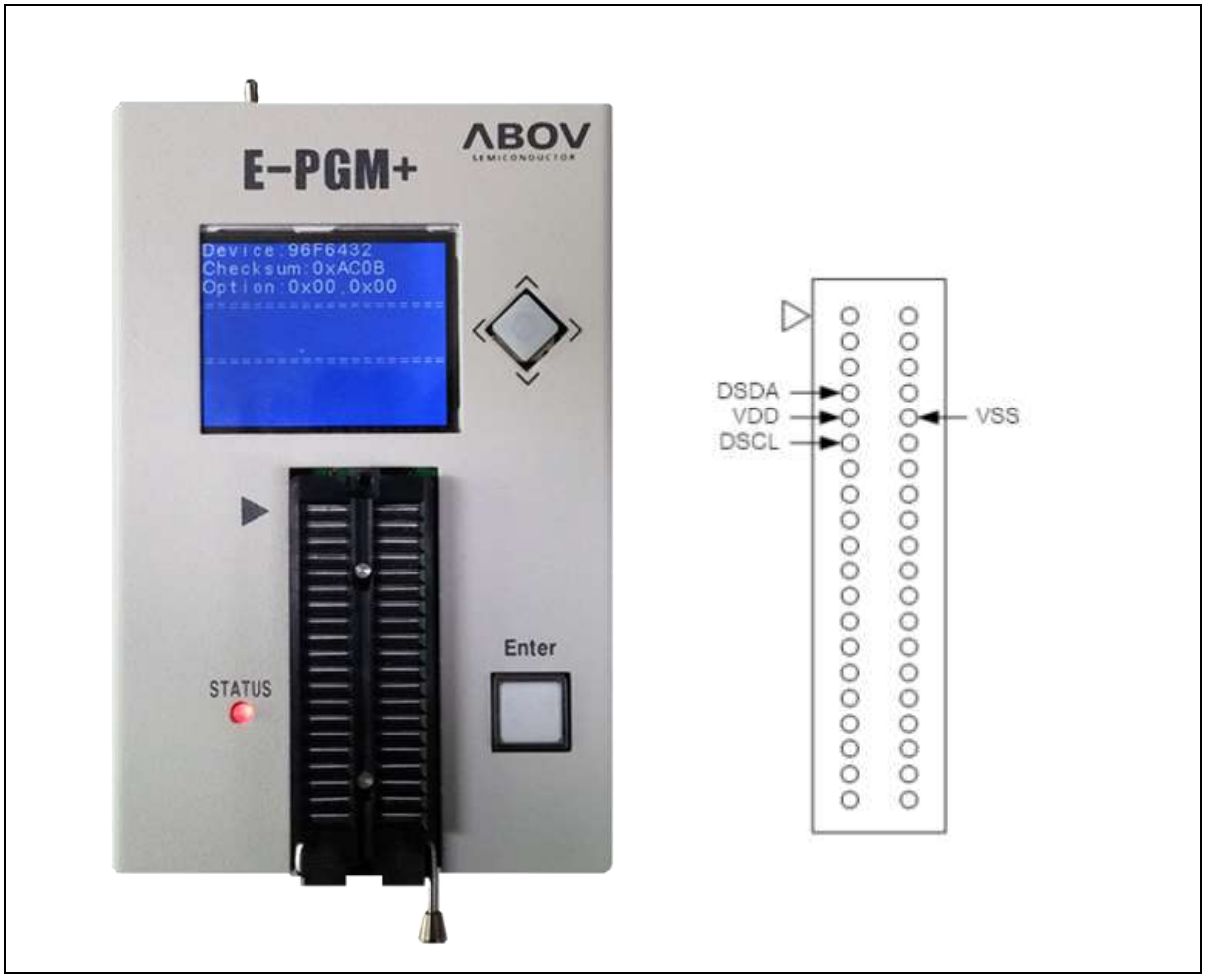
28.3 Programmer

28.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32-bit MCU @ 72MHz
- Buffer memory : 1MB

Figure 52. E-PGM+ (Single Writer) and Pin Descriptions



28.3.2 OCD emulator

OCD emulator allows a user to write code on the device too, since OCD debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

28.3.3 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Table 32. Specification of E-Gang4 and E-Gang6

Gang programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x35mm	148.2 x 22.5 x35mm
Weight	2.0kg	2.8kg
Input voltage	DC Adaptor 15V/2A	DC Adaptor 15V/2A
Operating temperature	-10 ~ 40℃	-10 ~ 40℃
Storage temperature	-30 ~ 80℃	-30 ~ 80℃
Water proof	No	No

Figure 53. E-Gang4 and E-Gang6 (for Mass Production)

28.4 MTP programming

Program memory of A96L623 is an MTP Type. This flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. Table 33 introduces each pin and corresponding I/O status.

Table 33. Pins for MTP Programming

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P13	I	Serial clock pin. Input only pin.
DSDA	P14	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

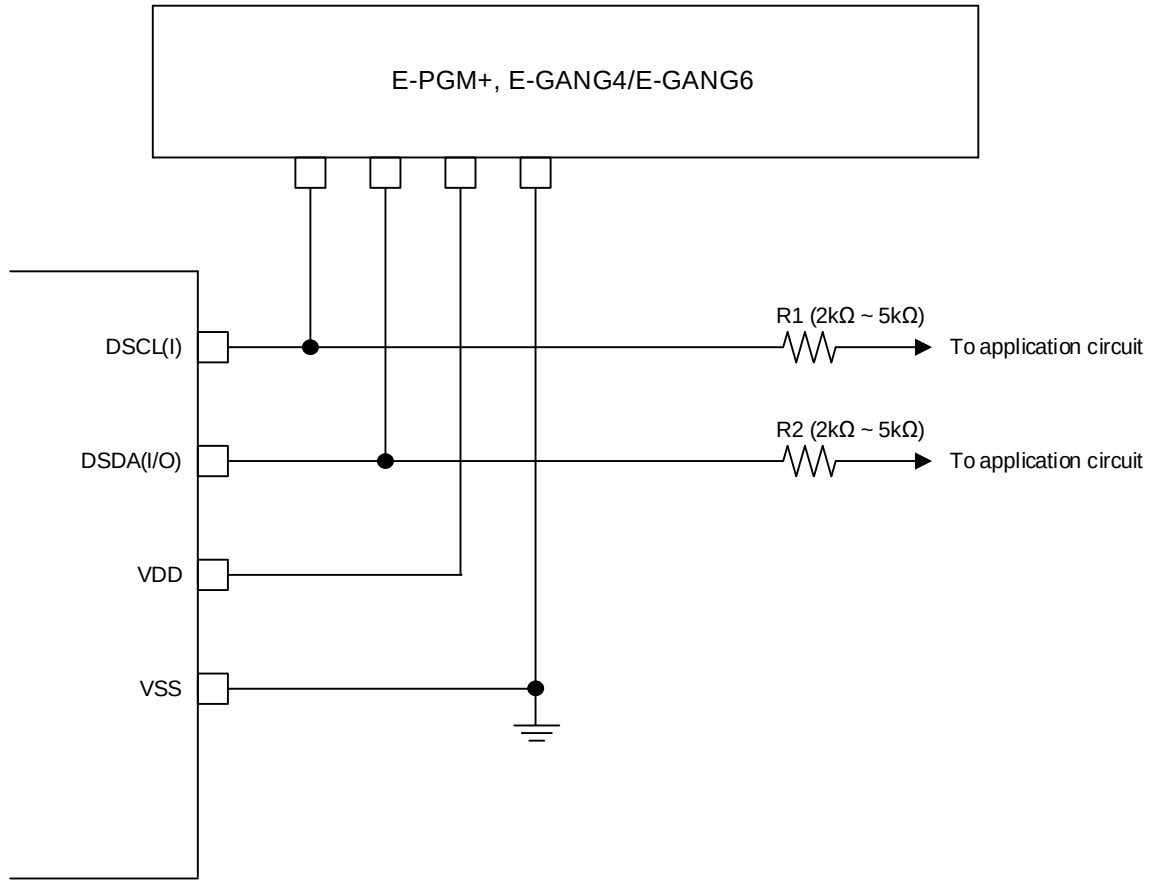
28.4.1 On-board programming

The A96L623 needs only four signal lines including VDD and VSS pins for programming flash with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

28.5 Circuit design guide

When programming Flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. When you design a PCB circuit, you should consider the usage of these 4 signal lines for the on-board programming.

Figure 54. PCB Design Guide for On-Board Programming



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

28.5.1 On-Chip Debug system

Detail descriptions for programming via the OCD interface can be found in the following figures. Table 34 introduces features of OCD and

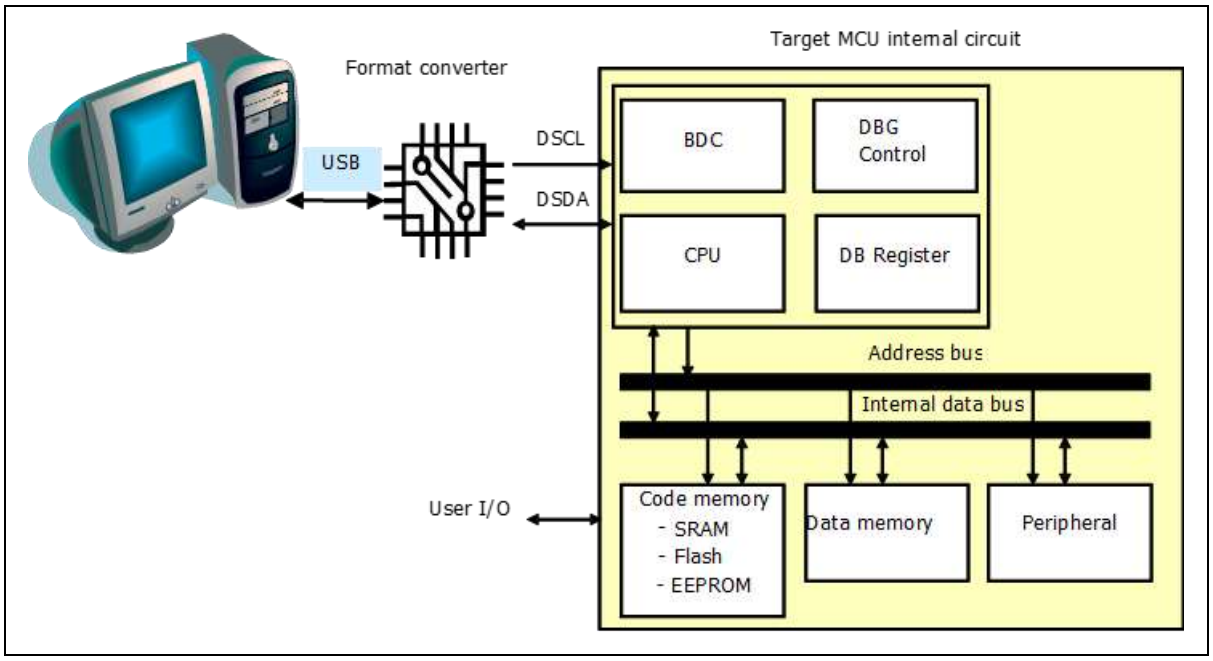
Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, Data Flash, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

Figure 55 shows a block diagram of the OCD interface and the On-chip Debug system.

Table 34. Features of OCD

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, Data Flash, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

Figure 55. On-Chip Debugging System in Block Diagram

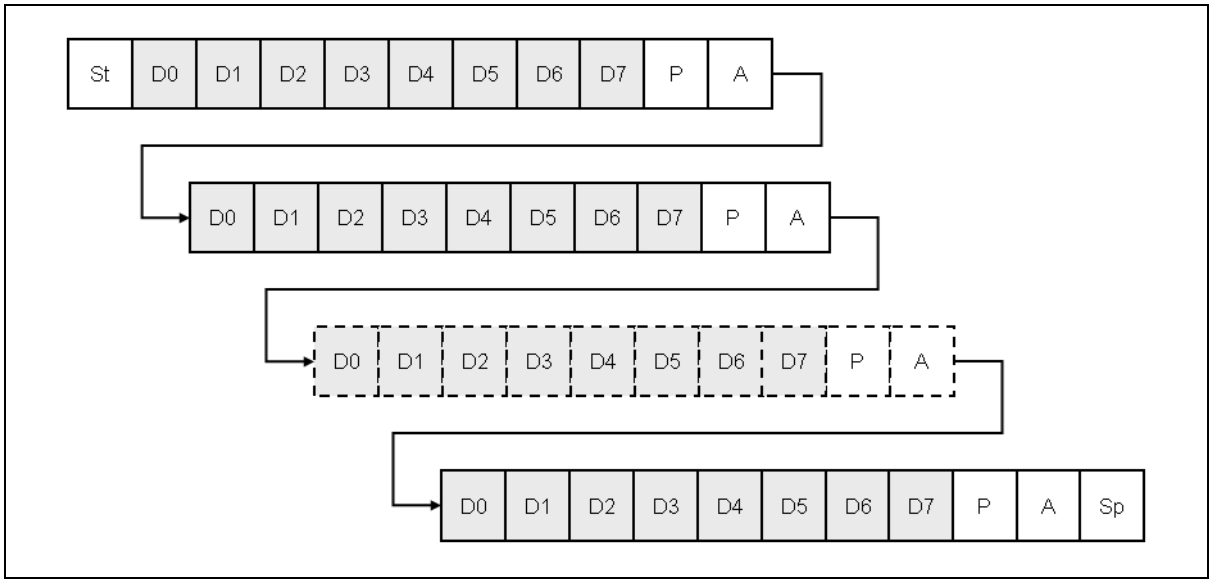

Target MCU internal circuit
Format converter
USB
DSCL
DSDA
BDC
DBG
Control
CPU
DB Register
Address bus
Internal data bus
User I/O
Code memory
- SRAM
- Flash
- EEPROM
Data memory
Peripheral

28.5.2 Two-pin external interface

Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

Figure 56. 10-bit Transmission Packet



Packet transmission timing

Figure 57. Data Transfer on Twin Bus

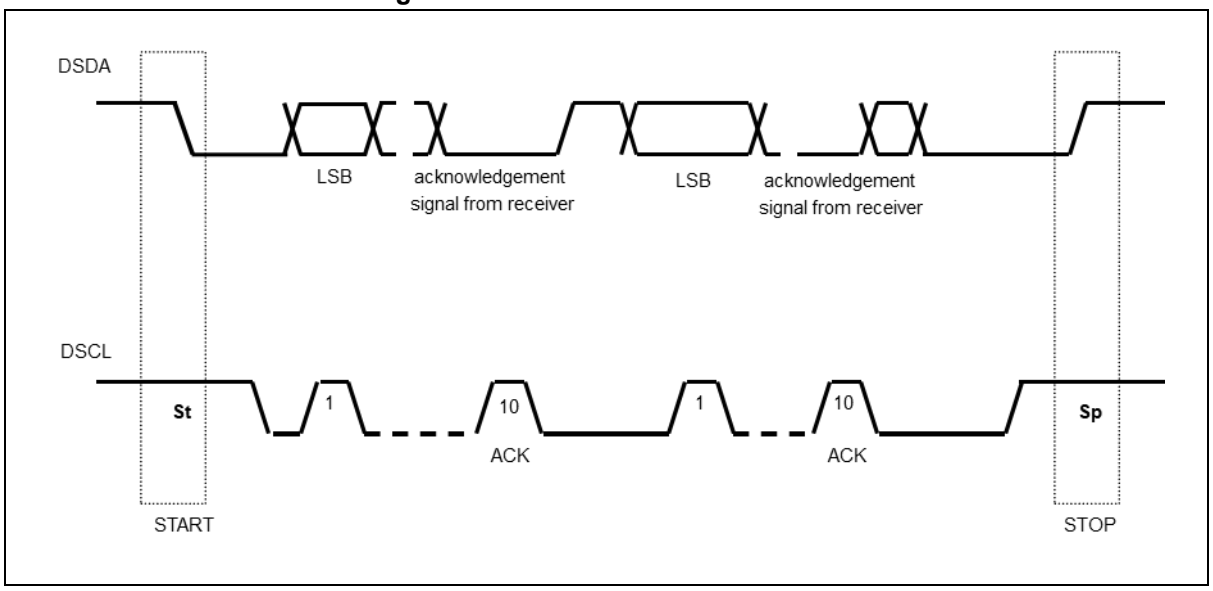


Figure 58. Bit Transfer on Serial Bus

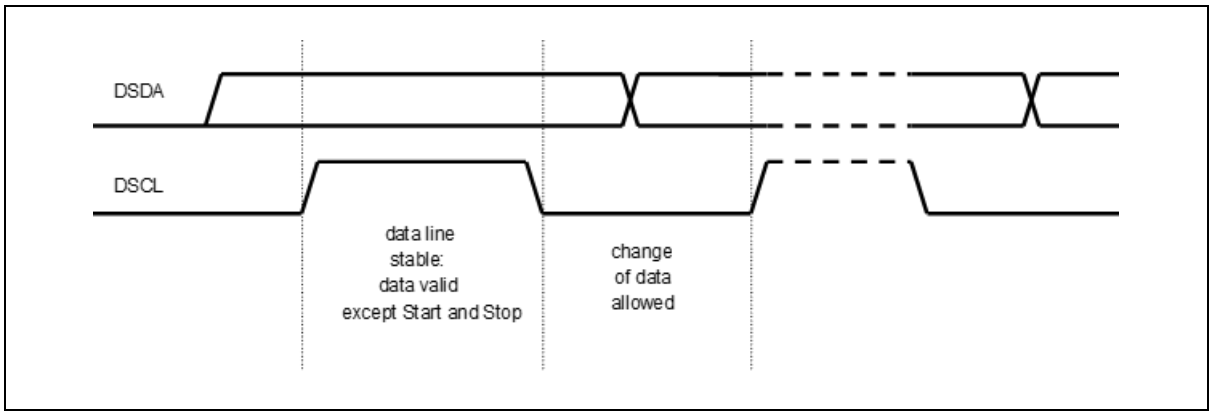


Figure 59. Start and Stop Condition

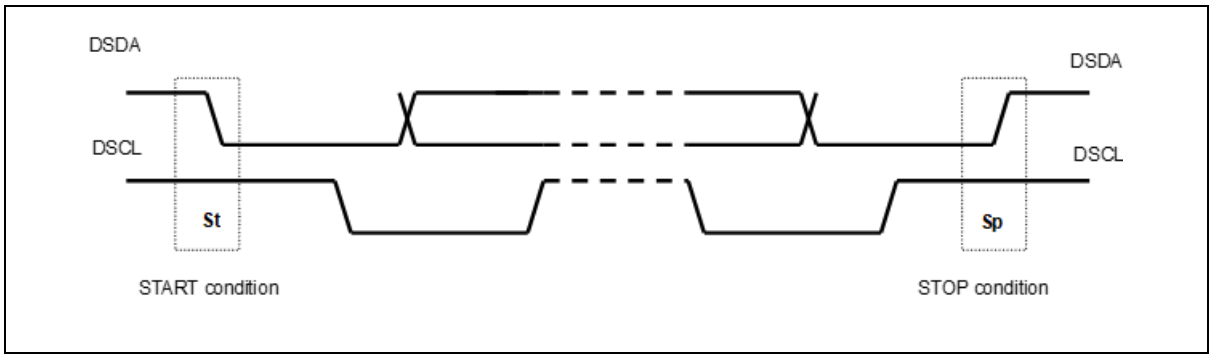


Figure 60. Acknowledge on Serial Bus

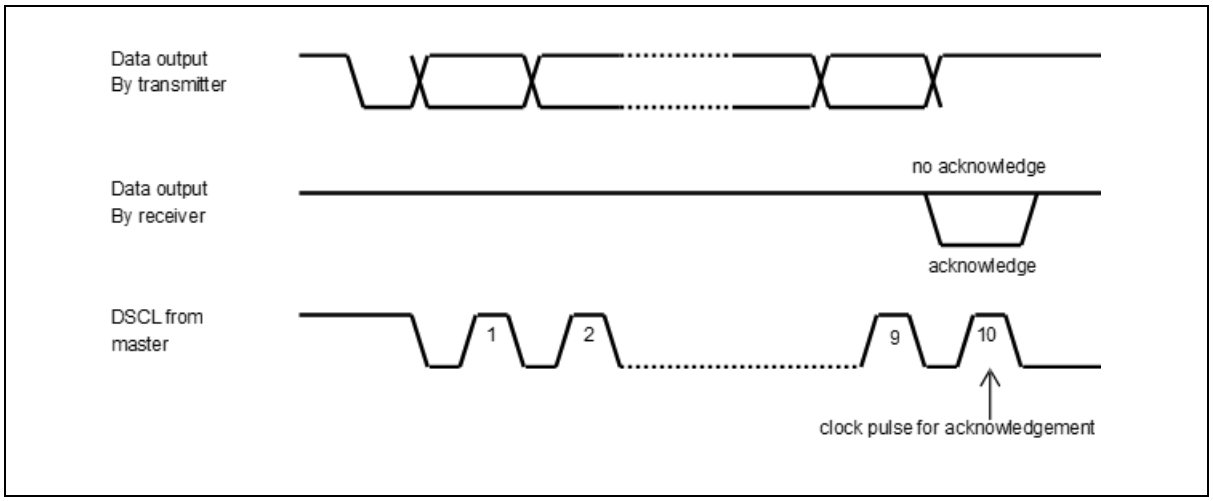
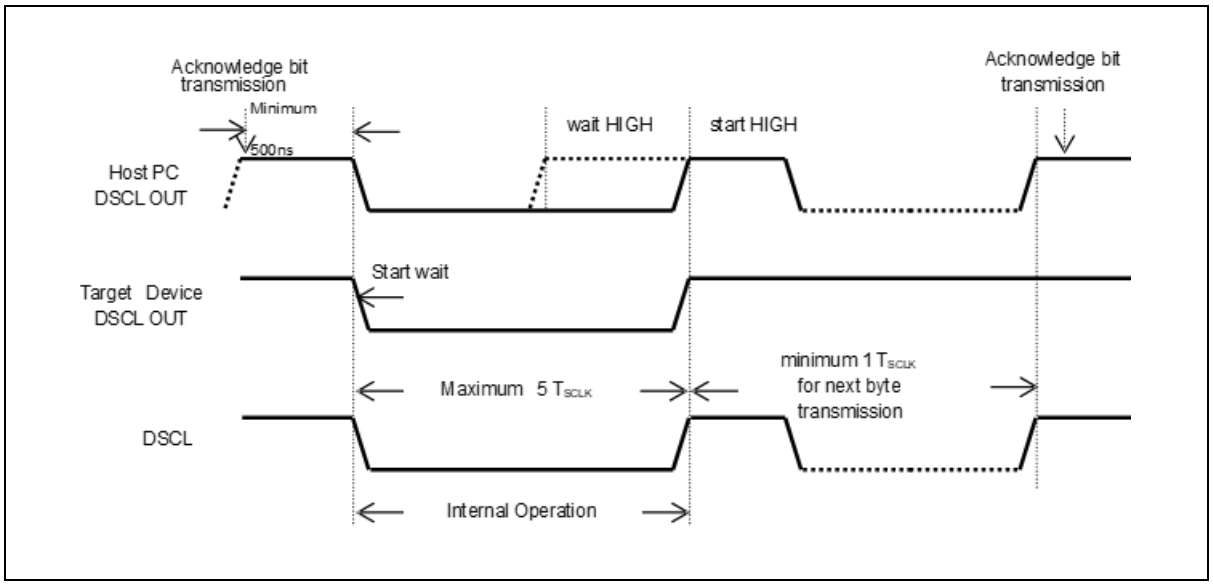


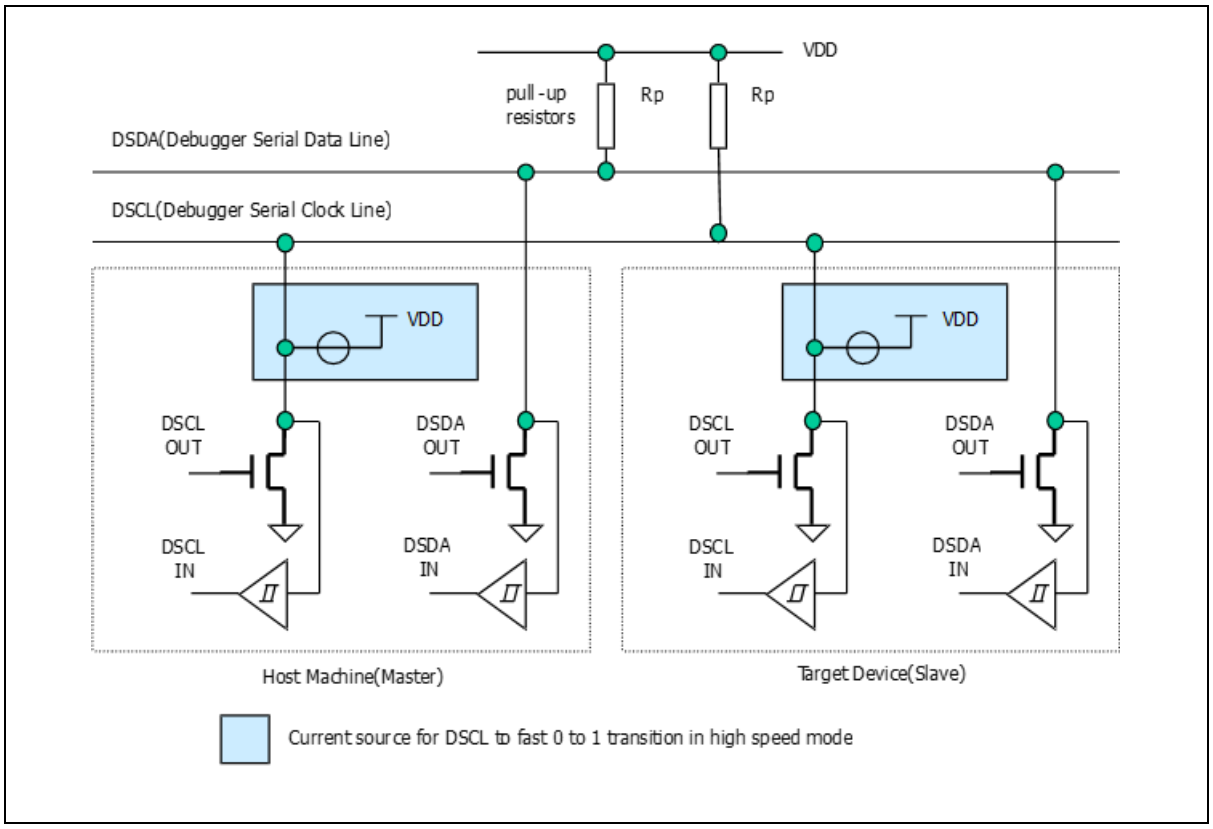
Figure 61. Clock Synchronization during Wait Procedure



28.5.3 Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

Figure 62. Connection of Transmission



Appendix

A. Configure option

Register description: configure option control

CONFIGURE OPTION 1: ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value: 00H

R_P	Code Read Protection	
	0	Disable
	1	Enable
HL	Code Write Protection	
	0	Disable
	1	Enable
VAPEN	Vector Area (00H – FFH) Write Protection	
	0	Disable Protection (Erasable by instruction)
	1	Enable Protection (Not erasable by instruction)
RSTS	Select RESETB pin	
	0	Disable RESETB pin (P12)
	1	Enable RESETB pin

CONFIGURE OPTION 2 for 16-kBytes flash memory: ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN	Enable Specific Area Write Protection	
	0	Disable (Erasable by instruction)
	1	Enable (Not erasable by instruction)
PASS [2:0]	Select Specific Area for Write Protection	

NOTE:

1. When PAEN = '1', it is applied.

PASS2	PASS1	PASS0	
0	0	0	0.7Kbytes (Address 0100H – 03FFH)
0	0	1	1.7Kbytes (Address 0100H – 07FFH)
0	1	0	2.7Kbytes (Address 0100H – 0BFFH)
0	1	1	3.7KBytes (Address 0100H – 0FFFH)
1	0	0	5.7Kbytes (Address 0100H – 17FFH)
1	0	1	6.7Kbytes (Address 0100H – 1BFFH)
1	1	0	7.2Kbytes (Address 0100H – 1DFFH)
1	1	1	7.5KBytes (Address 0100H – 1EFFH)

B. Instruction table

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column in tables shown below.
- Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following tables in this section.
- 1 machine cycle comprises 2 system clock cycles.

Table 35. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 36. Instruction Table: Logical

Logical				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 37. Instruction Table: Data Transfer

Data transfer				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 38. Instruction Table: Boolean

Boolean				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 39. Instruction Table: Branching

Branching				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 40. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

Table 41. Instruction Table: Additional Instructions

Additional instructions (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, and the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

Revision history

Date	Version	Description
April.12, 2021	0.00	First creation
Sept. 13, 2021	0.02	Second edition
Sept. 30, 2021	0.03	Third edition
Sept. 30, 2021	0.04	Fourth edition
Nov. 26, 2021	0.90	Fifth edition
May. 18, 2022	1.00	Sixth edition
Oct. 27, 2022	1.10	Seventh edition

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