CMOS single-chip 8-bit MCU with Remote control and IR learning

A96R150

Data Sheet

V1.01

Nov, 2022

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 96Kbytes Flash Code Memory
  - 2560bytes XRAM + 256bytes IRAM
- **Built-in Analog Function**
  - Power-On Reset
  - Low Voltage Detect (Brown Out Detect) Reset
  - Internal 12MHz RC Oscillator (±1.0%, after tuning T_A = -20 ~ +70°C)
  - Watchdog Timer RC Oscillator (1MHz)
- **Peripheral Features**
  - USART 8-bit x 1-ch, SPI 8-bit x 1-ch, I2C 8-bit x 1ch
  - Internal IR driver, Internal IR learning
- **I/O and Packages**
  - Up to 21 programmable I/O lines with 20QFN 24/28TSSOP
  - 20QFN 24/28TSSOP
- **Operating Conditions**
  - 1.71V to 3.6V Voltage Range
  - -25°C to 85°C Temperature Range
- **Application**
  - IR blaster, IR receiver, Remote controller

Revision History

Version	Date	Revision list
0.0	2018.08.31	-.
0.1	2018.09.06	POD update, Pin description update
0.2	2018.10.16	BODI update, P3 usage update
1.0	2018.12.14	Updated 7.18 Main Clock Oscillator Characteristics. Updated BODR usage Updated -25 to 85ºC temperature range added Updated XSFR Flash Lock/Unlock registers Updated Figure 13.4. .(VDD rising time) Add note comment Updated voltage range of IR learning Updated IR learning range(2.4~3.6V) Update BODR range. 1.51~1.67V Update BODI range. 1.94~2.08V Update PMISC0. Delete USART option Update Flash Erase/Write voltage 1.71~3.6V Release version
1.01	2022.11.10	Revised the font of this document

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Version 1.01

Published by L Group

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1 Overview

1.1 Description

The A96R150 is an advanced CMOS 8-bit microcontroller with FLASH (96KB). This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 96K bytes of FLASH, 256 bytes of IRAM, 2560 bytes of XRAM, general purpose I/O, 8/16-bit timer/counter, watchdog timer, watch timer, SPI, USART, I2C, on-chip POR and LVI(BOD), 8/16-bit PWM output, on-chip oscillator, Internal IR driver and IR learning circuit including OP-AMP. The A96R150 also supports power saving modes to reduce power consumption.

1.2 Features

- **CPU**
  - 8-bit CISC core (8051 Compatible, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 96KB Flash with self-read and write capability
  - In-System Programming(ISP)
  - Endurance : 10,000 times
  - Retention : 10 years
- **256 bytes IRAM**
- **2560 bytes XRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 21 Ports (28TSSOP)
  - Normal I/O : 17 Ports (20QFN)
- **Boot Loader Protection**
- **Internal IR driver**

– Carrier generator

- **Internal IR Learning with OP-AMP**
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit × 1-ch
  - Watch Dog Timer (WDT) 8-bit × 1-ch

  1MHz internal RC oscillator for WDT
  - WT for IR learning
  - 8-bit × 2-ch (T0/T1)
  - 16-bit × 2-ch (T2/T3)
- **Programmable Pulse Generation**
  - Pulse generation (by T0/T2)
  - 16-bit PWM (by T2/T3)
- **SPI**
  - 8-bit × 1-ch
- **USART**
  - 8-bit × 1-ch
- **I2C**
  - I2C × 1-ch
- **Power On Reset**
  - Reset release level (Typ 1.2V)
- **Low Voltage Reset**
  - 1.60V(reset or indicator)
- **Low Voltage Indicator**
  - 3 levels brownout detect (2.01V / 2.25V / 2.45V)
- **Interrupt Sources**
  - External Interrupts (EINT0 ~EINT5) (6)
  - Timer(0/1/2/3) (4)
  - Remocon(1)
  - IRI (1)
  - USART Tx, Rx (2)
  - SPI (Shared USART)(1)
  - I2C (1)
  - WT(1)
  - WDT (1)
  - BIT (1)
  - FLASH (1)
  - LVI(BOD) (1)
  - Keyscan(1)
  - Pin Change Interrupt(1)
- **Internal RC Oscillator**

  Internal RC-OSC frequency: after tuning
  - ±0.5% @25°C
  - ±1.0% @-20~70°C
  - ±2.0% @-25~85°C
- **Operation Voltage and Frequency**
  - 1.71~3.6V(@1~4MHz with Crystal, Resonator)
  - 2.0~3.6V(@8MHz with Crystal, Resonator)
  - 2.5~3.6V(@12Mhz with Crystal, Resonator)
- **Power Down Mode**
  - STOP mode
- **Minimum Instruction Execution Time**
  - 167ns (@12MHz clock, 2clocks per cycle)
- **Operating Temperature**
  - –25 ~ +85℃
- **Package Type**
  - 20QFN,24/28TSSOP

1.3 Ordering information

Device Name	Flash	XRAM	IRAM	Package
A96R150FUN	96KB	2560 bytes	256 bytes	20 QFN
A96R150LRN				24 TSSOP
A96R150GRN				28 TSSOP

Table 1.1 Ordering Information of A96R150

1.3.1 Device Nomenclature

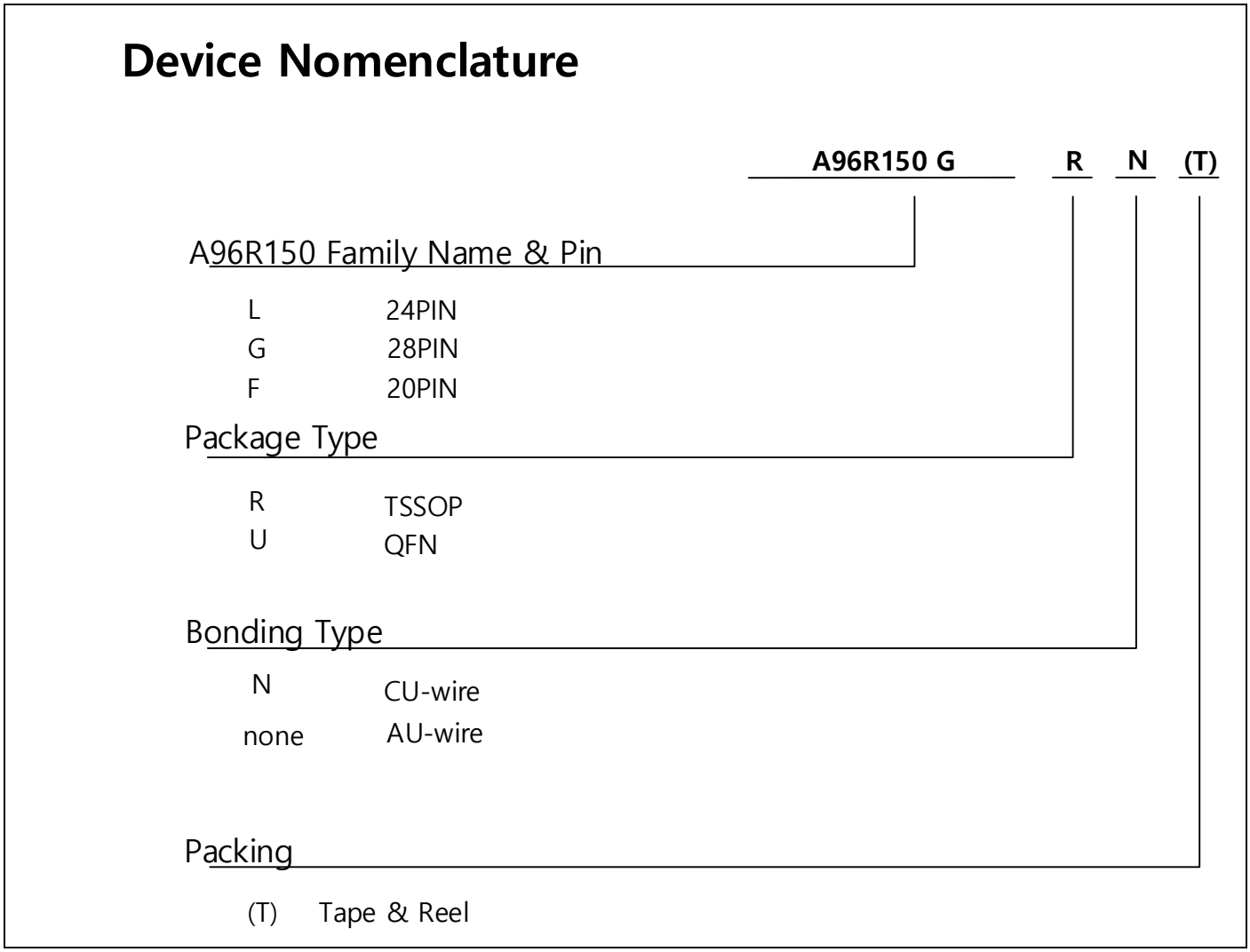


Figure 1.1 Device Nomenclature

1.4 Development tools

1.4.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compiler provider.
The A96R150 core is Mentor 8051 and the ROM size is larger than 64KB. Therefore, developer can use the progressed 8051 compiler which support code banking.

1.4.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD interface uses two-wire connection between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.
The OCD debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit) operating system. If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (http://www.abov.co.kr).

Connection:

DSCL (A96R150 P2[0] port)
DSDA (A96R150 P2[1] port)

OCD connector diagram: Connect OCD with user system

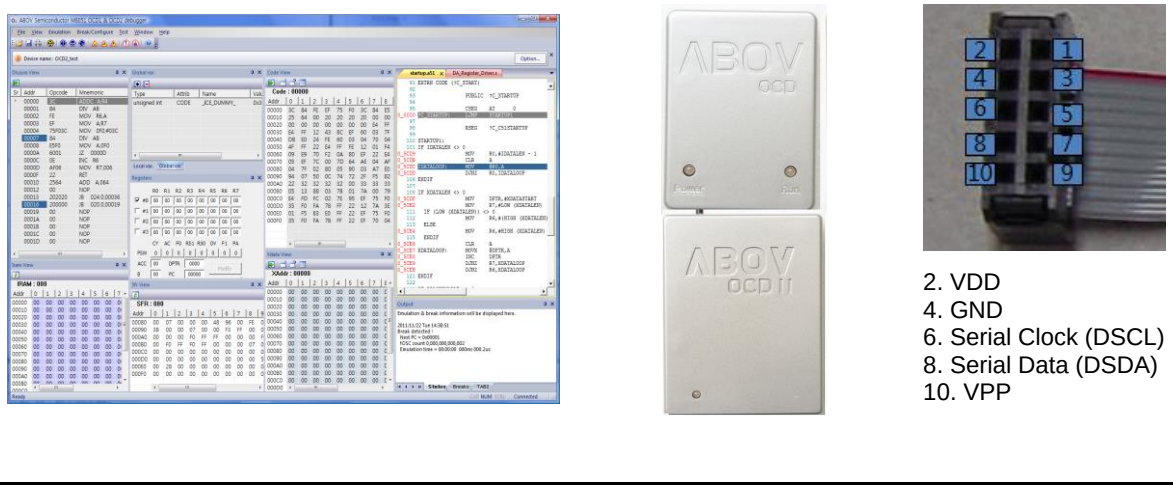


Figure 1.1 debugger and pin description

1.4.3 Programmer

To program or download user code into the ROM of A96R150, ABOV semiconductor provides several tools. As a single programmer which can program only one chip at a time, there are E-PGM+ and PGMPlusLC-II. On the other hand, you can program multi-chips at a time by using a gang programmer. Gang programmer, E-GANG6, can program up to 6 devices simultaneously

1.4.3.1 E-PGM+

E-PGM+ is a single write tool for ABOV MCUs.

Features :

Support ABOV / ADAM devices

2~5 times faster than S-PGM+

Main controller : 32 bit MCU @72MHz

Buffer memory : 1MB

Figure 1.2 E-PGM+

1.4.3.2 PGMPlusLC-II

PGMPlusLC-II is for ISP (In System Programming). It is used to program or erase the MCU which is already mounted on the target board using 10pin cable.

Features :

PGMPlusLC-II is low cost writing tool

USB interface is supported

No need for USB driver installation

Connect to the external power adaptor (5V@2A)

Fast 32-bit Cortex-M3 MCU is used

Support high voltage up to max 18V

PGMPlusLC-II is based on PC environment

PGMPlusLC-II is faster than PGMplusLC

Transmission Speed of 64KB/s

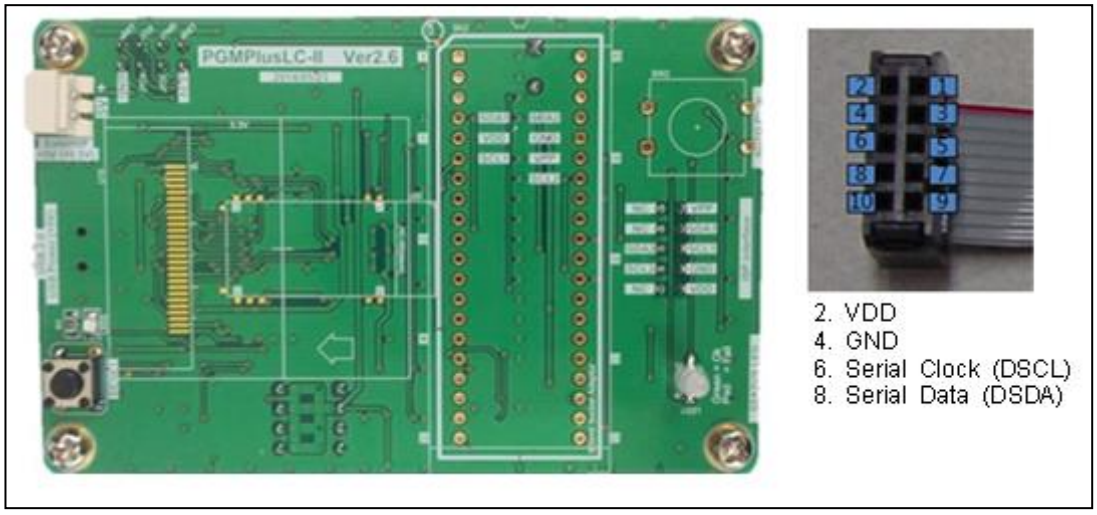


Figure 1.3 PGMPlusLC-II

1.4.3.3 E-GANG4(6)

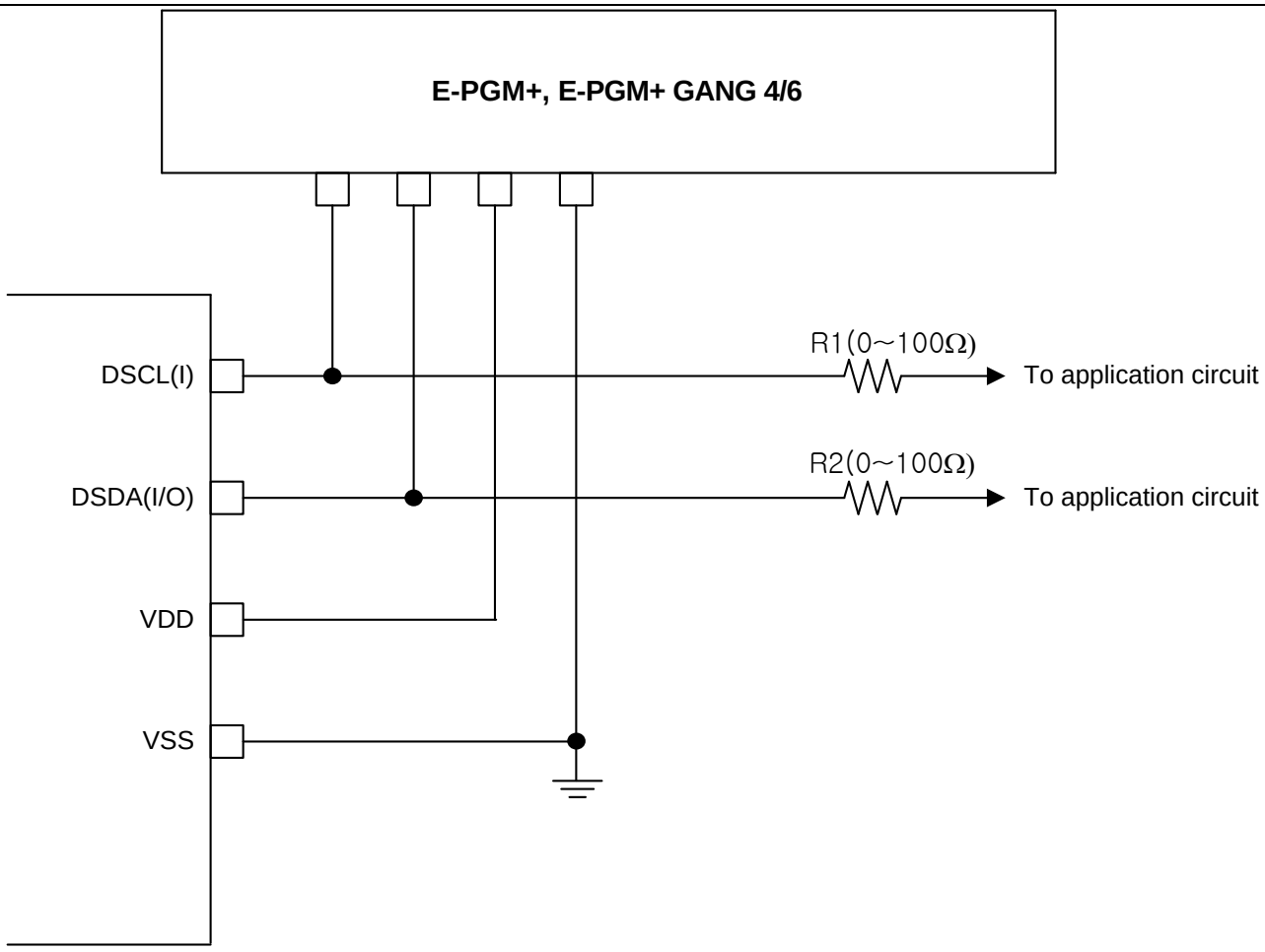
The gang programmer, E-GANG4/(6) can program maximum4(6) MCUs at a time. So it is mainly used in mass production line. As gang programmer is standalone type, it does not require host PC.

Figure 1.4 Gang programmer

1.4.4 Circuit design guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.

The value of R1 and R2 is recommended value and it varies with circuit of system.

Figure 1.4 PCB Design guide for on board programming

2 Block diagram

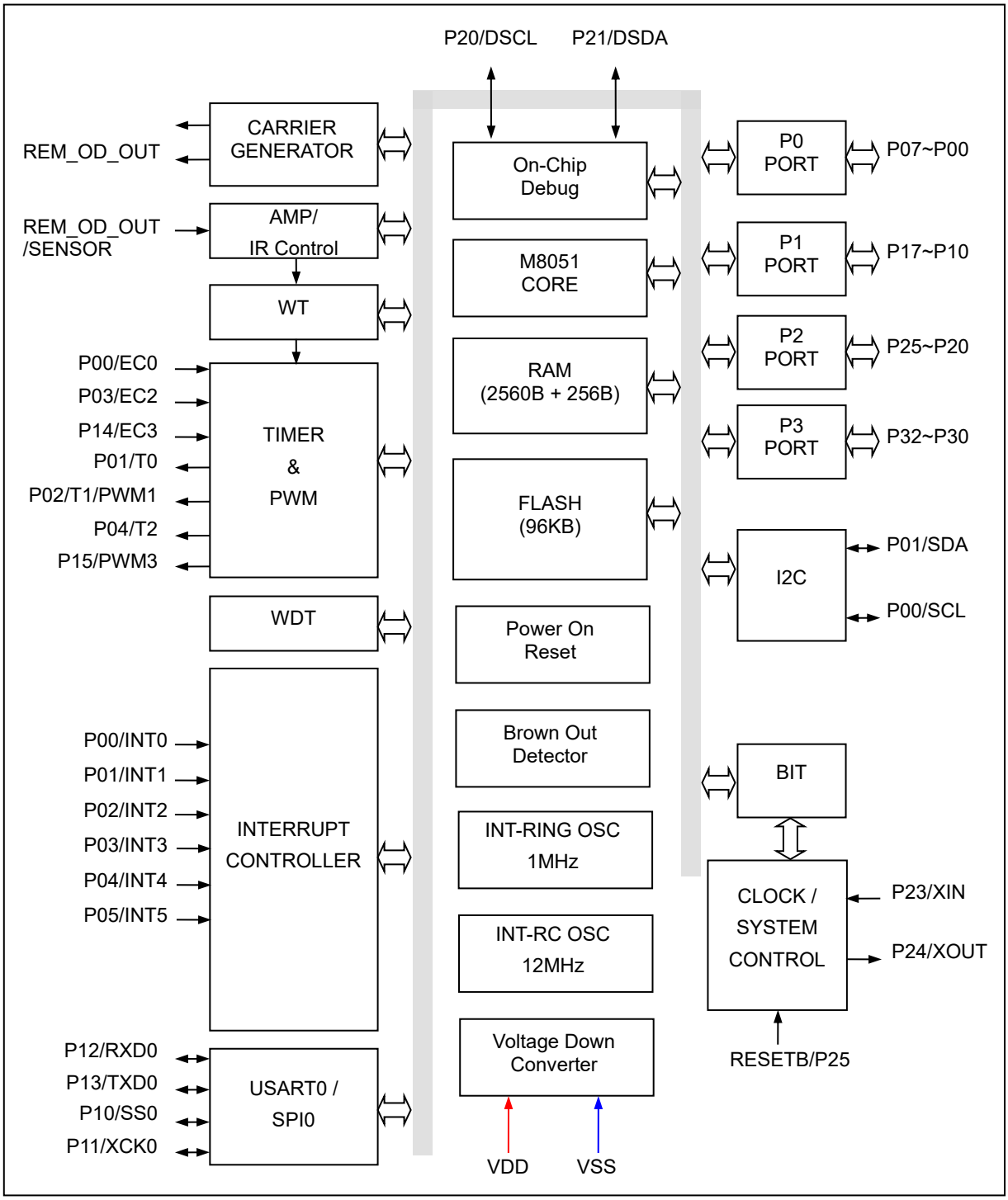


Figure 2.1 Block diagram of A96R150

3 Pin assignment

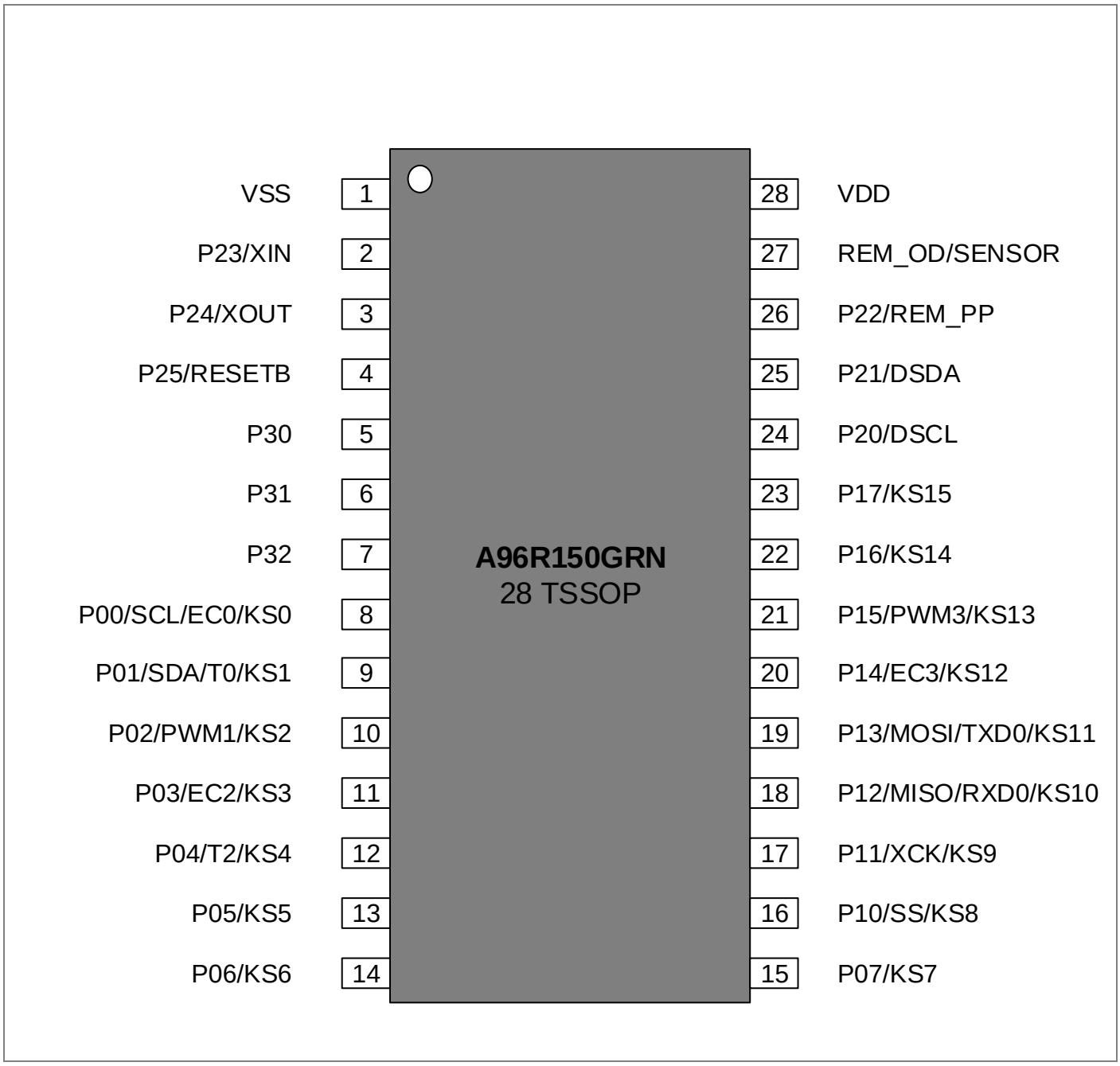


Figure 3.1 28TSSOP Pin-out of A96R150

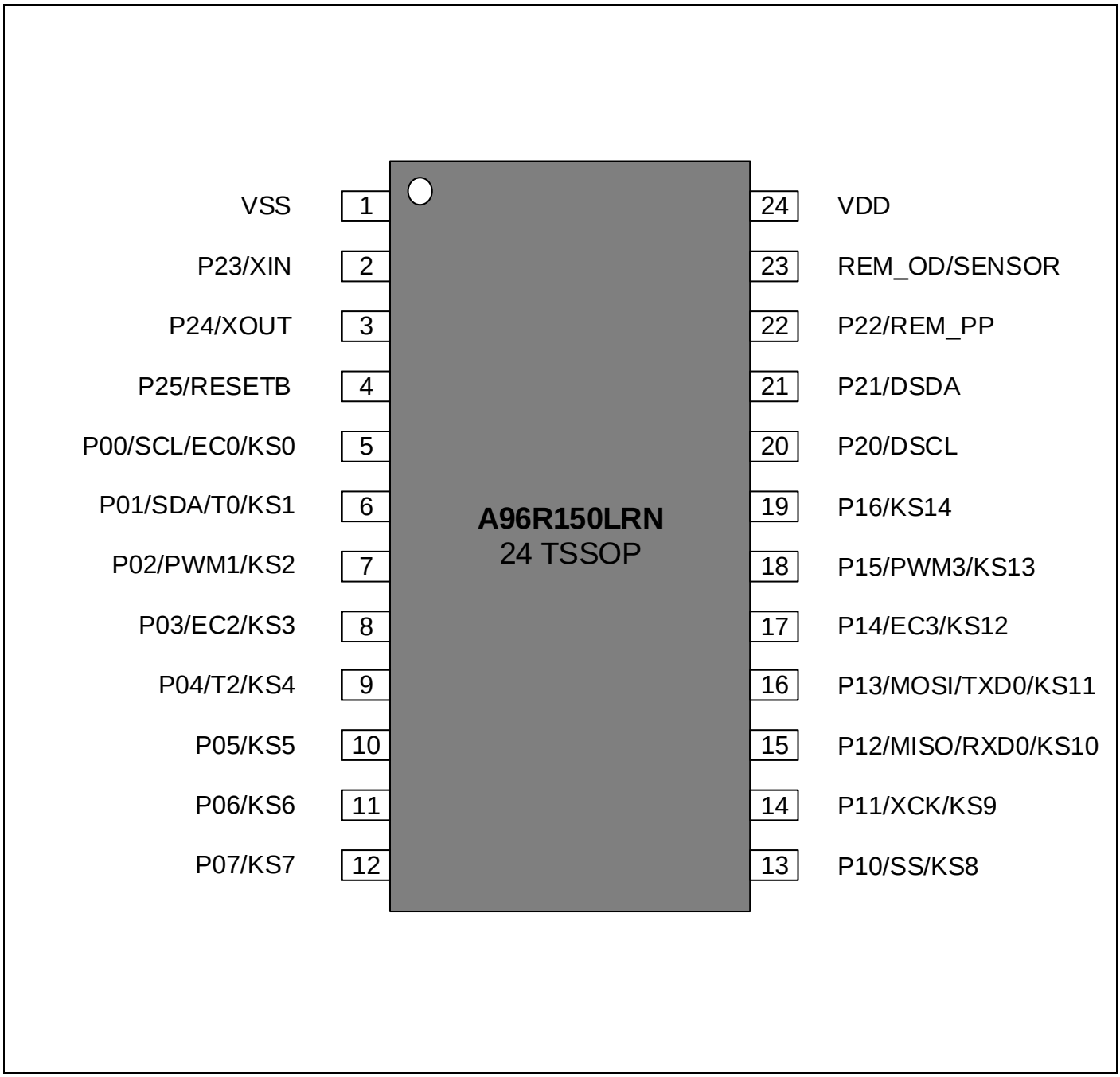


Figure 3.2 24TSSOP Pin-out of A96R150

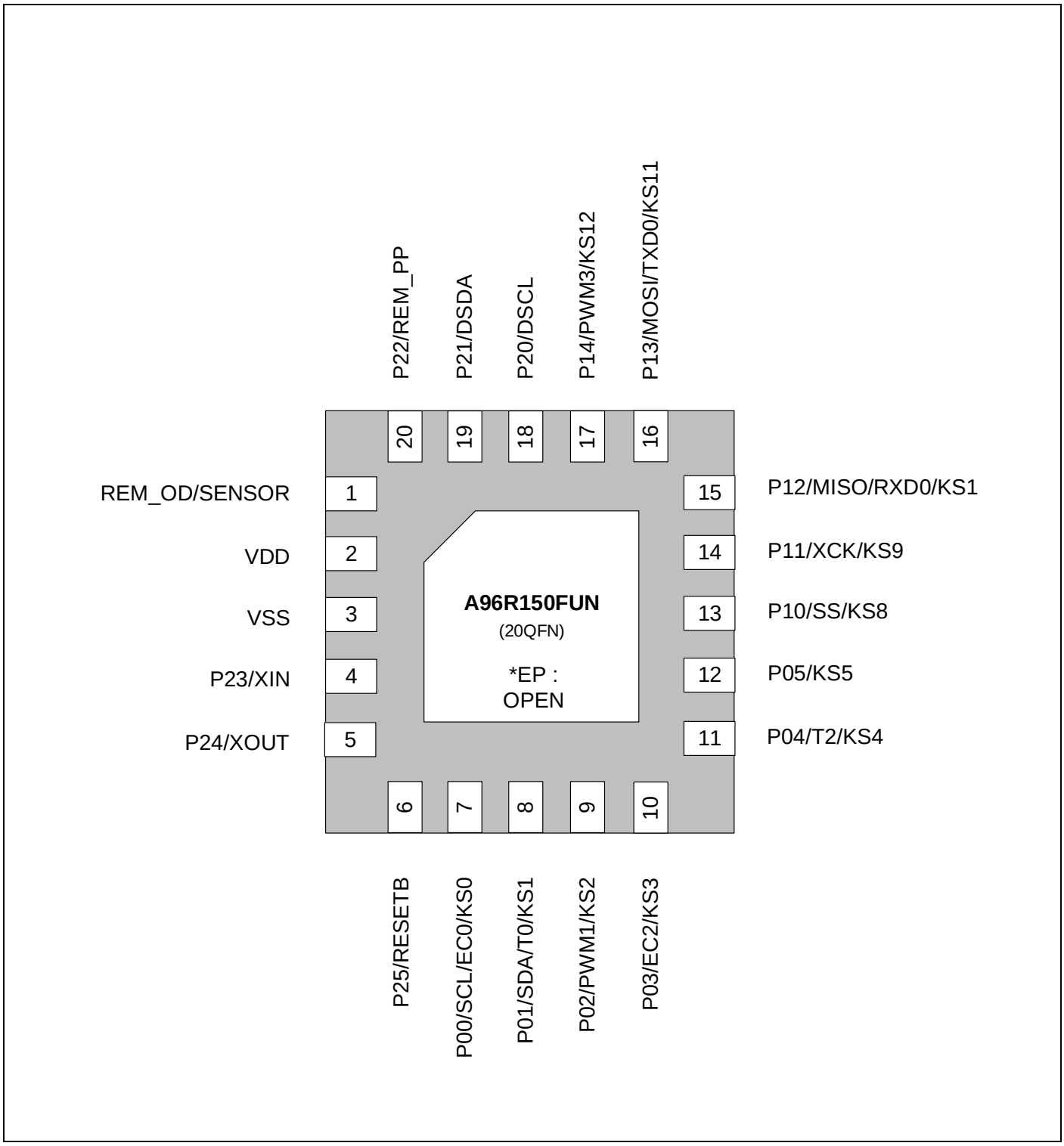


Figure 3.3 20QFN Pin-out of A96R150

4 Package Diagram

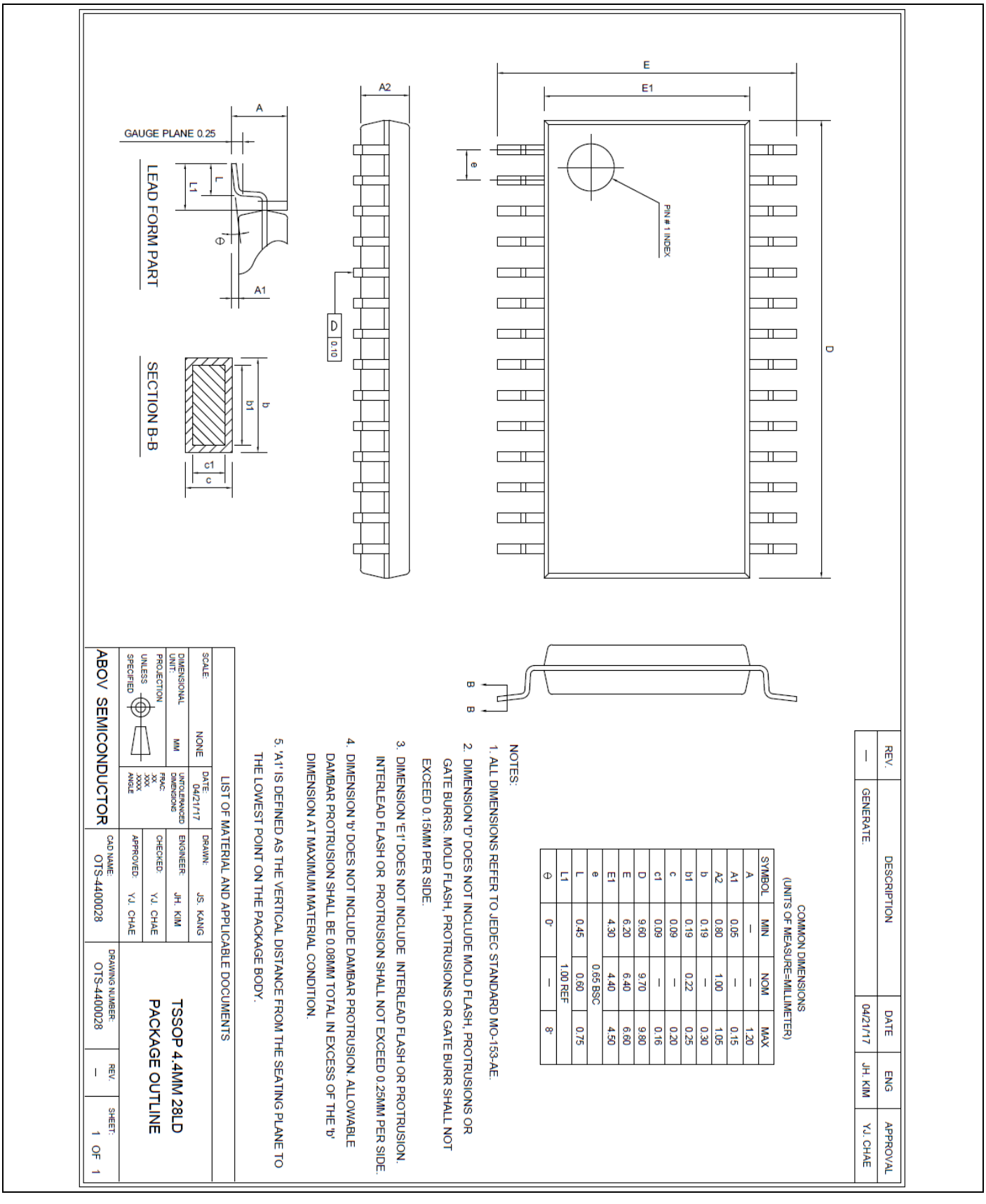
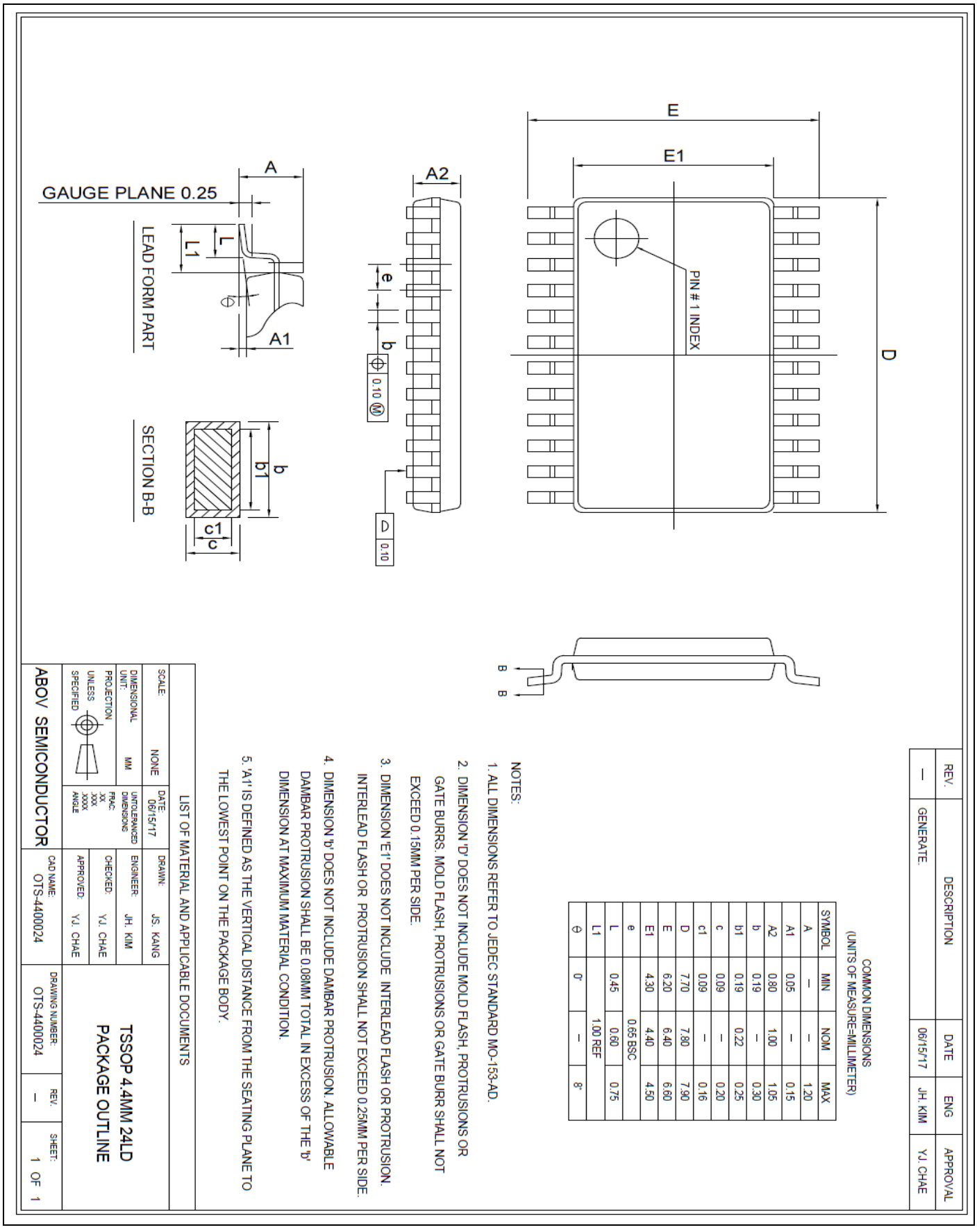


Figure 4.1 PKG DIMENSION (28 TSSOP)



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	06/15/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	—	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153-AD.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURR SHALL NOT EXCEED 0.15MM PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. 'A1' IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 06/15/17	DRAWN: JS. KANG	
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION	FRAC: XX ±X XXX ±XXX ANGLE	CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: YJ. CHAE	

ABOV SEMICONDUCTOR

CAD NAME: OTS-4400024

TSSOP 4.4MM 24LD
PACKAGE OUTLINE

DRAWING NUMBER: OTS-4400024 | REV: — | SHEET: 1 OF 1

Figure 4.2 PKG DIMENSION (24 TSSOP)

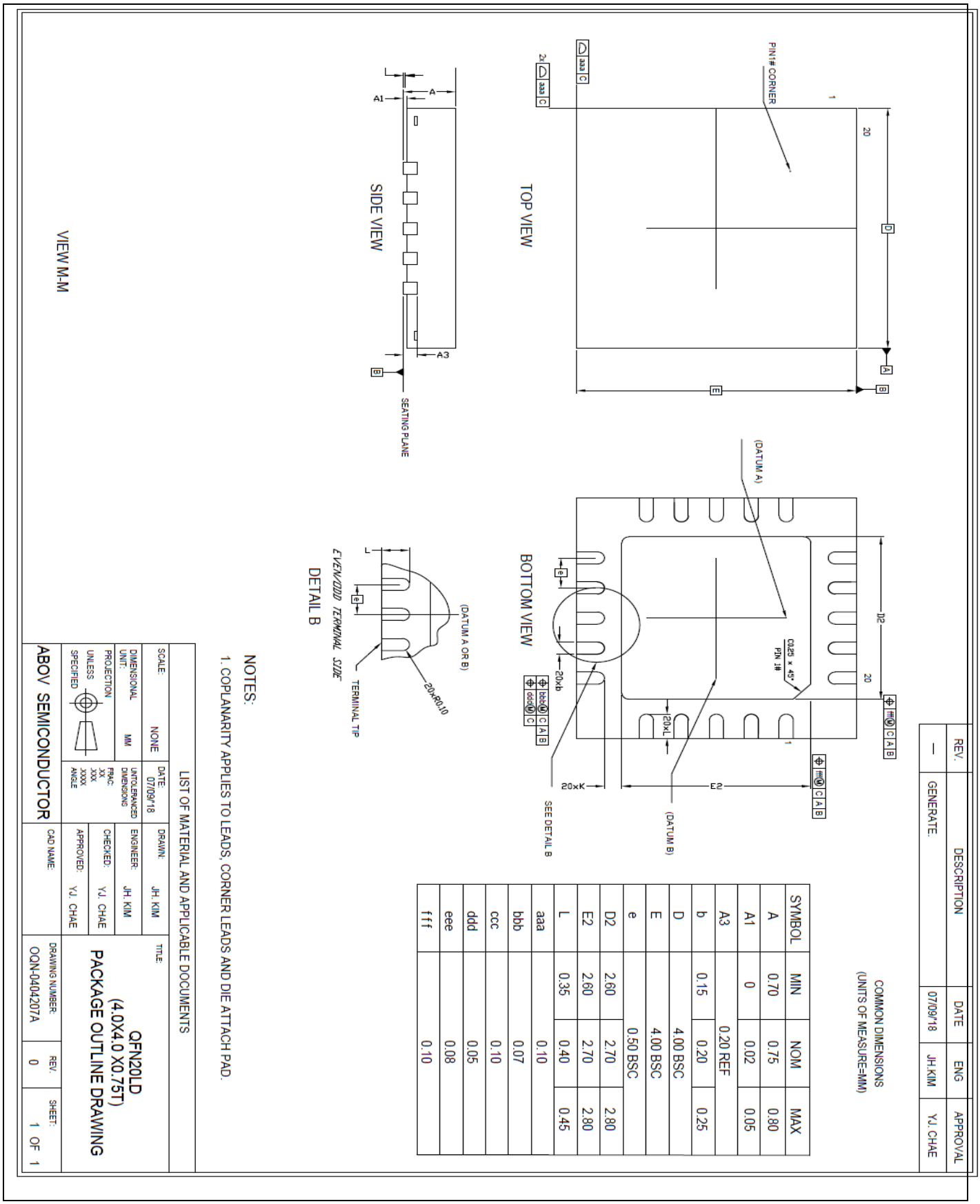


Figure 4.3 PKG DIMENSION (20 QFN)

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	- 6-bit I/O port, P0. - Can be set in input or output mode bitwise. - Internal pull-up resistor can be activated by setting PxnPU bit in PxPU register when this port is used as input port. - Can be configured as an open drain output mode by setting PxnOD bit in PxOD register.	Input	INT0 NOTE1 / SCL/EC0/KS0
P01				INT1 NOTE1 / SDA/T0/KS1
P02				INT2 NOTE1 / PWM1/KS2
P03				INT3 NOTE1 / EC2/KS3
P04				INT4 NOTE1 /T2/KS4
P05				INT5 NOTE1 /T1
P06				KS6 NOTE4
P07				KS7 NOTE4
P10	I/O	6-bit I/O port, P1. - Can be set in input or output mode bitwise. - Internal pull-up resistor can be activated by setting PxnPU bit in PxPU register when this port is used as input port. - Can be configured as an open drain output mode by setting PxnOD bit in PxOD register.	Input	SS/KS8
P11				XCK/KS9
P12				MISO/KS10
P13				MOSI/KS11
P14				PWM3/KS12
P15				/KS13 NOTE4
P16				KS0/KS14 NOTE4
P17				KS15
P25	I/O	6-bit I/O port, P2. - Can be set in input or output mode bitwise. - Internal pull-up/pull-down resistor can be activated by setting PxnPU bit in PxPU register when this port is used as input port. - Can be configured as an open drain output mode by setting PxnOD bit in PxOD register.		RESETB
P24				XOUT
P23				XIN
P22				REM_PP_OUT NOTE2
P21				DSDA
P20				DSCL
P32		3-bit I/O port, P3. - Can be set in input or output mode bitwise. - Internal pull-up resistor can be activated by setting PxnPU bit in PxPU register when this port is used as input port. - Can be configured as an open drain output mode by setting PxnOD bit in PxOD register.	input	NOTE3
P31				NOTE3
P30				NOTE3
REM_OD_OUT	I/O	1-bit I/O port. - REM open-drain output	input	SENSOR
VSS	P	Ground	-	
VDD	P	Main power supply		

Table 5.1 Normal Pin description

NOTE1 If EIPSx is controlled, the interrupt port (INTx) is changed to any port.

NOTE2 Pull-down for P22, Pull-up for P27, P26, P25, P24, P23, P21, 20

NOTE3 P30, P31, P32 and P17 are used at 28 TSSOP package type.

NOTE4 P06, P07, P15 and P16 are used at 24 TSSOP, 28 TSSOP package types.

NOTE : When using 20QFN package, be sure to define the configuration for unused pins. For example, you should set up Input Pull-up. Including P3 Port

6 Port Structures

6.1 General Purpose I/O Port

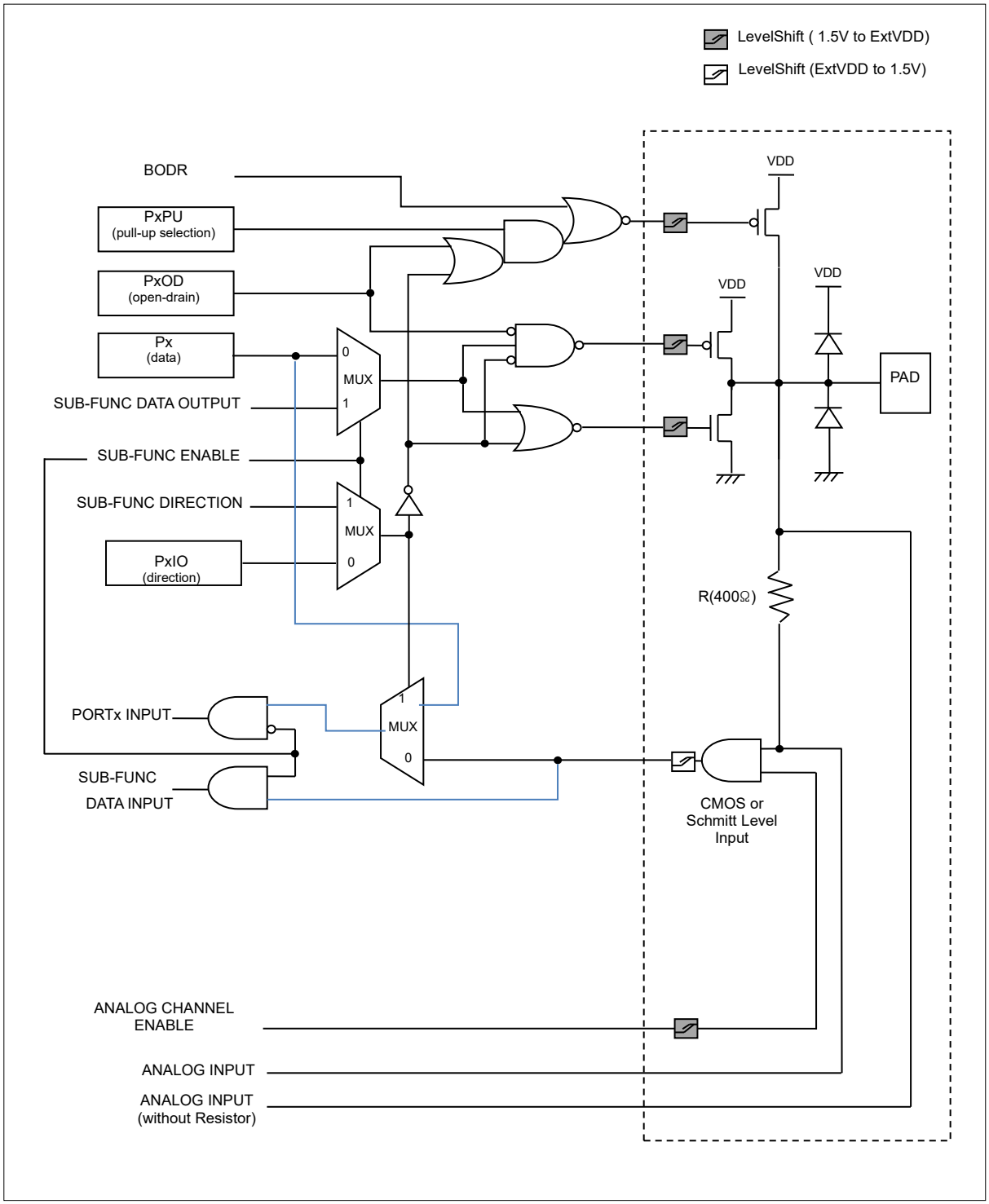


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

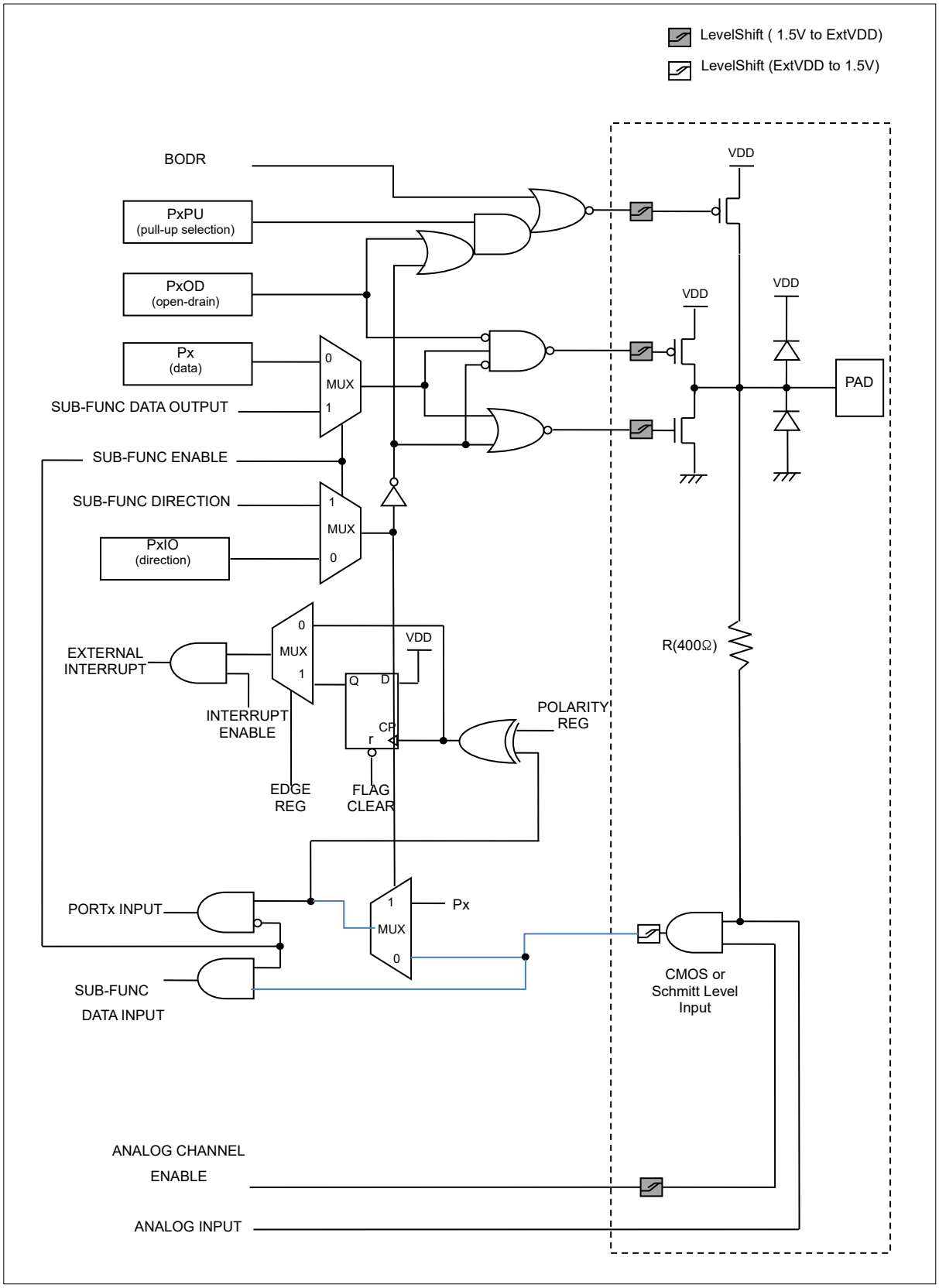


Figure 6.2 I/O with external interrupt function

6.3 External Interrupt I/O Port with drive strength selection

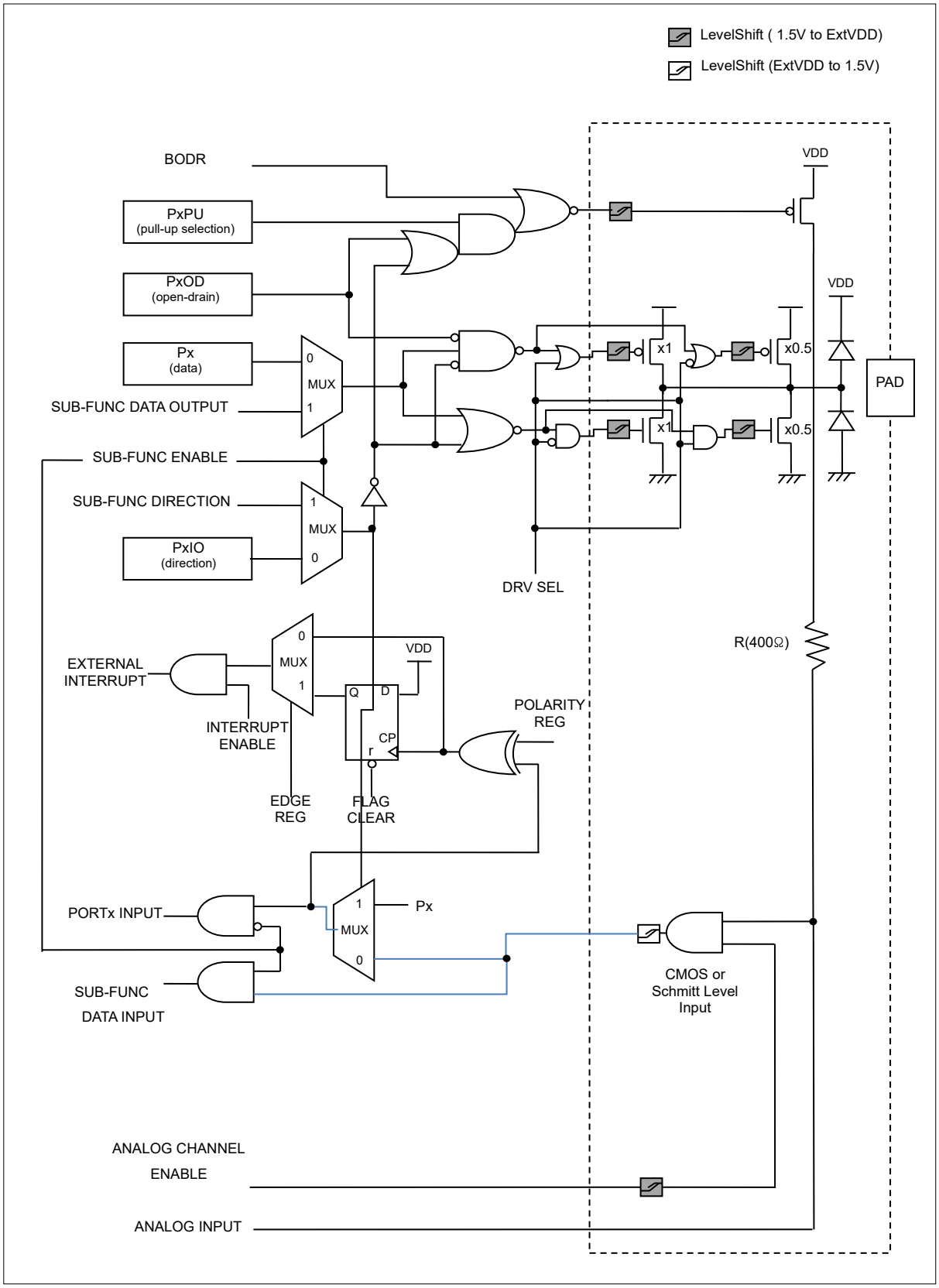


Figure 6.3 I/O with external interrupt function & selectable drive strength

6.4 REM OD Port

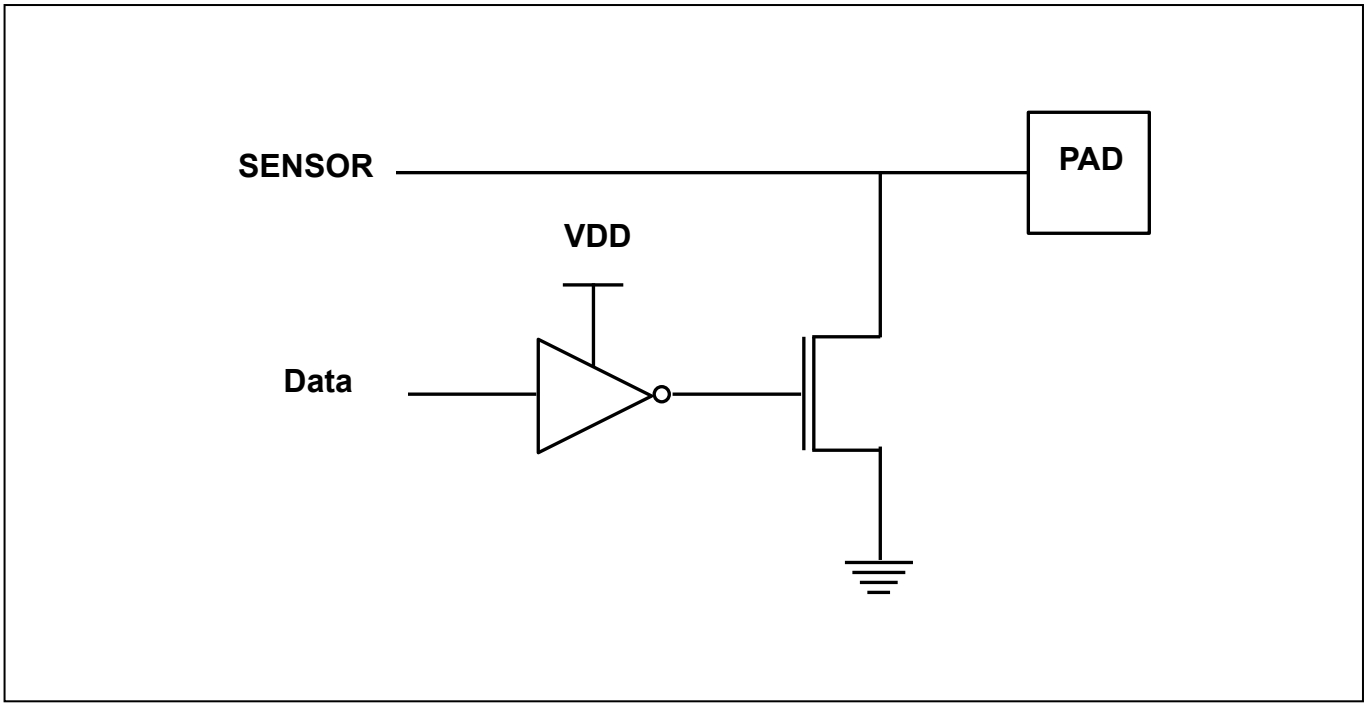


Figure 6.4 REM_OD Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3~+4.0	V
	VSS	-0.3~+0.3	V
Normal Voltage Pin	VI	-0.3~VDD+0.3	V
	VO	-0.3~VDD+0.3	V
	IOH	10	mA
	∑IOH	80	mA
	IOL	20	mA
	∑IOL	160	mA
Total Power Dissipation	PT	600	mW
Storage Temperature	TSTG	-45~+125	℃

Table 7.1 Absolute Maximum RatingsNOTE Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VDD	NOTE	1.71	-	3.6	V
	VDD_IR		1.71	-	3.6	V
Operating Temperature	T_{OPR}		-25	-	85	℃
Operating Frequency	F_{OPR}		1	-	12	MHz

Table 7.2 Recommended Operating Conditions

NOTE If you use a main clock oscillator, the voltage range depending on the frequency can vary.
See 7.18 Main Clock Oscillator Characteristics.

7.3 VOLTAGE DROPOUT CONVERTER (Core voltage regulator) CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Regulation Voltage		-	-	1.57	-	V

Table 7.3 Voltage Dropout Converter Characteristics

7.4 BROWN OUT DETECTOR(BOD) CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Detection Level	V_{BODR}	NOTE	1.51	1.60	1.67	V
	V_{BODI0}	NOTE	1.94	2.01	2.08	V
	V_{BODI1}	NOTE	2.15	2.25	2.35	V
	V_{BODI2}	NOTE	2.35	2.45	2.55	V
	-	-	-	-	-	-
	-	-	-	-	-	-
Startup time	t_{BODS}			30	50	us
Detection time	t_{BODD}			2		us
Operating Current	IDD	-	-	20	50	uA

Table 7.4 Brown out Detector Characteristics

NOTE V_{BODR} is a voltage level and BODR flag indicating it can generate internal reset due to voltage drop. When the external power drops below the V_{BODR} voltage level, the BOD detects the power condition and makes the device enter STOP-like mode called BOD mode. When the external power is restored, a BOD reset is generated according to pre-defined sequence and the device is initialized. $V_{BODI0/1/2}$ also indicates voltage levels and BODI0/1/2 are these flags. When the external power drops below the level indicated in above table, the associated flag is set to '1' and these values can be read through the BODSR register. These flags may be used to monitor the status of battery charging.

7.5 RAM Data Retention CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Data Retention Supply Voltage	V_{DR}		1.0			V
Data Retention Supply Current	I_{DR}	VDD=1.0V			20	uA

Table 7.5 RAM data retention Characteristics

7.6 FLASH CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Flash Read Supply Voltage	V_{READ}		1.71		3.6	V
Flash write Supply Voltage	V_{WRITE}	NOTE	1.71		3.6	V
Page Erase Time	t_{ERS}	1byte ~ 128bytes			2.5	ms
Page Program Time	t_{PGM}	1byte ~ 128bytes			2.5	ms
Program/Erase Cycle			10,000			cycles
Data Retention			10			years

Table 7.6 FLASH Characteristics

NOTE the recommended minimum voltage of FLASH write is V_{BODI0}. If FLASH is to be written, the VDD level has to be checked with V_{BODI0}.

7.7 Internal RC Oscillator CHARACTERISTICS

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
IRC Frequency	f_{IRC}				12		MHz
IRC Frequency Variability	f_{IRC_VAR}	VDD =1.71V~3.6V	T_A = +25˚C	-0.5	-	+0.5	% *note
			T_A = -20˚C ~ +70˚C	-1.0	-	+1.0	
			T_A = -25˚C ~ +85˚C	-2.0	-	+2.0	

Table 7.7 Internal RC Oscillator Characteristics

*note: It is possible to proceed with user trim

7.8 Internal RING Oscillator CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VDD		V_{BODR}	-	3.6	V
Frequency	f_{IRING}	-25~+85℃	0.5	1	1.5	MHz
Tolerance	$f_{RINGTOL}$	-25~+85℃	-50	-	+50	%

Table 7.8 Internal RING Oscillator Characteristics

7.9 Learning Amplifier CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
IR AMP Input Low Detection	I_{DL}	VDDEXT = 3.3V	1.5	-	-	uA
IR AMP Input High Detection	I_{DH}	VDDEXT = 3.3V	-	-	0.2	uA
IR AMP Learning Voltage Range	V_{LR}		2.4		3.6	V

Table 7.9 Learning Amplifier Characteristics

7.10 POWER-ON RESET CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
RESET Release Level		-	-	1.2	-	V

Table 7.10 Power-On Reset Characteristics

7.11 DC CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Low Voltage	VIL		0	-	0.2VDD	V
Input High Voltage	VIH		0.8VDD	-	VDD	V
Output Low Voltage of P0, P1, P2 and P3	VOL	VDD=3.0V, IOL=10mA	-	0.4	1.0	V
Output High Voltage of P0, P1, P2 and P3	VOH	VDD=3.0V, IOH=4mA	VDD-1.0	2.6	-	V
Output Low Voltage of REM_PP_OUT	VOL_REM_PP	VDD=3.3V, IOL=0.3mA	-	0.6	1.0	V
Output High Voltage of REM_PP_OUT	VOH_REM_PP	VDD=3.3V, IOH=8.5mA	VDD-1.0	2.9	-	V
Output Low Voltage of REM_OD_OUT	VOL_REM_OD	VDD=3.0V, IOL=210mA	-	0.4	1.0	V
Input High Leakage Current	IIH				1	uA
Input Low Leakage Current	IIL		-1			uA
Pull-Up Resistors	RPU	VDD=3.0V, V_{IN} = 0V	50	100	200	kΩ
Pull-Down Resistor	RPD	VDD=3.0V, V_{IN} = 3.0V	33	67	130	kΩ
Power Supply Current	IDD1	RUN Mode, f_{XIN}=12MHz@3.6V	0.4	2.5	4.0	mA
	IDD3 NOTE	STOP Mode @3.6V, 25 ºC	-	1	7	uA
		STOP Mode @3.6V, -20~ 70 ºC	-	1	15	uA
		STOP Mode @3.6V, -25~ 85 ºC	-	1	18	uA

Table 7.11 DC Characteristics

NOTE if chip is stop mode, BOD is disabled with chip.

7.12 AC Characteristics

Parameter	Symbol	PIN	MIN	TYP	MAX	Unit
Operating Frequency	fMCP	XIN	0	-	12	MHz
System Clock Cycle Time	tSYS	-	83	-		ns
Oscillation Stabilization Time (8MHz)	tMST1	XIN, XOUT	-	-	10	ms
External Clock “H” or “L” Pulse Width	tCPW	XIN	40	-	-	ns
External Clock Transition Time	tRCP,tFCP	XIN	-	-	10	ns
Interrupt Input Width	tIW	INT0~INT5	-	10	-	ns
RESETB Input Pulse “L” Width	tRST	RESETB	-	8	-	us

Table 7.12 AC Characteristics

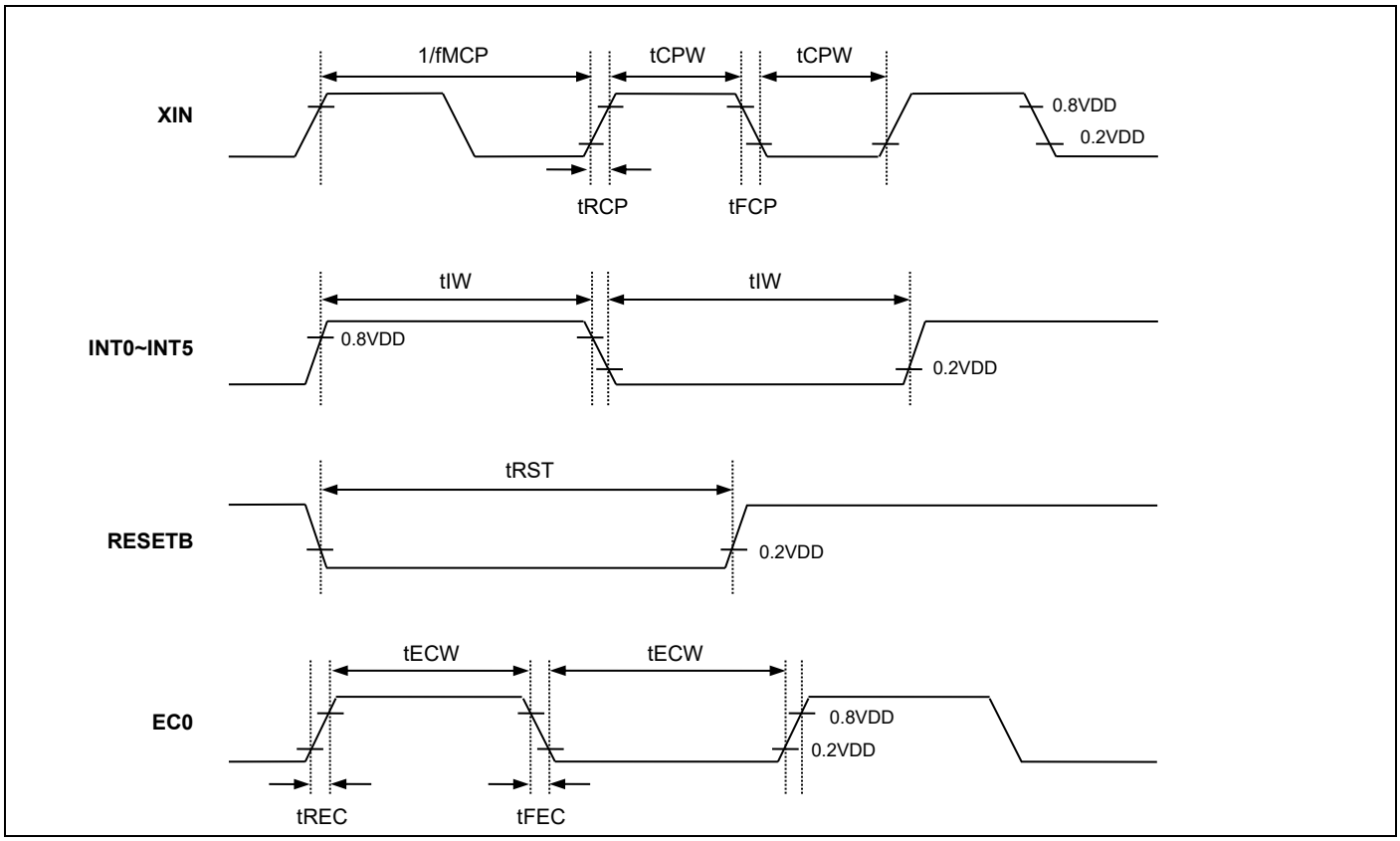


Figure 7.12 AC Timing

7.13 I2C CHARACTERISTICS

The following table and figure show the timing condition of SDA and SCL bus lines for I²C bus devices.

Parameter NOTE1	Symbol	STANDARD MODE		FAST MODE		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time after (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	us
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	us
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	us
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	us
Data setup time	$t_{SU;DAT}$	100	-	100	-	ns
Clock/data fall time	t_F	0	300	0	300	ns
Clock/data rise time	t_R	0	1000	0	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	us

Table 7.13 Timing characteristics of I2C

NOTE1 All timing is shown with respect to 20% VDD and 80% VDD.

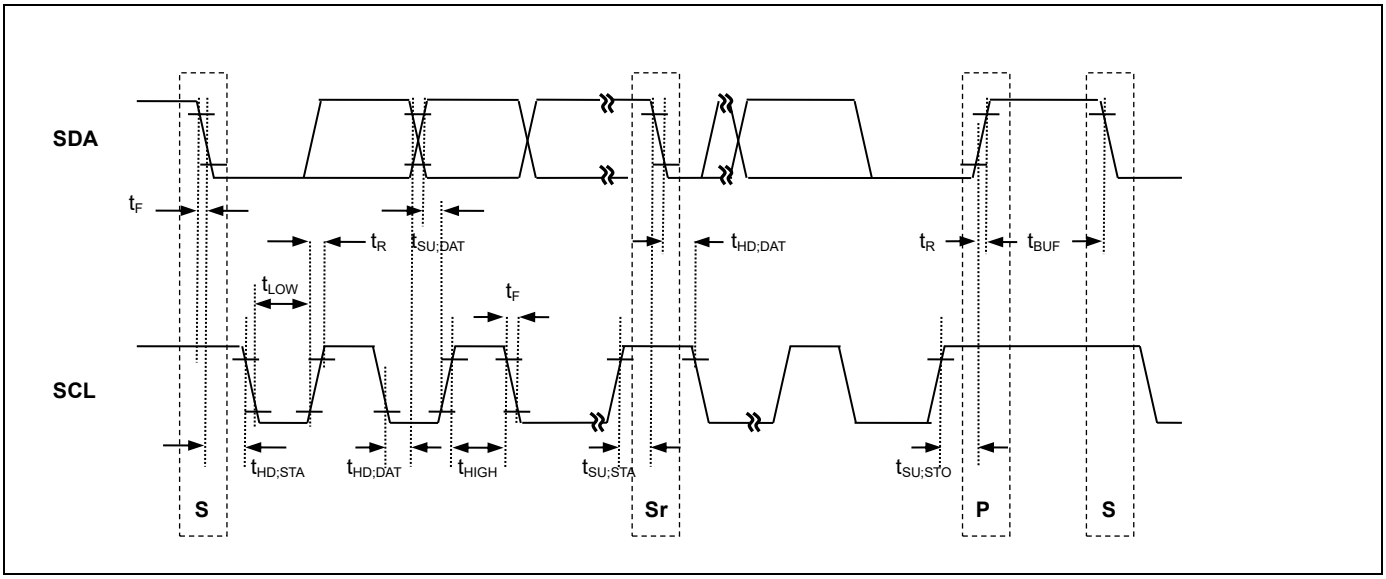


Figure 7.2 Timing diagram of I2C

7.14 USART Characteristics

The following table and figure show the timing condition of USART in SPI or Synchronous mode of operation. The USART is one of peripherals in A96R150.[NOTE1].

Parameter	Symbol[NOTE2]	MIN	MAX	Unit
System clock period(@12Mhz)	t_{SCLK}	83	1000	ns
Clock (XCK) period				
Master	t_{XCK}	2	1024	t_{SCLK}
Slave	t_{XCK}	4	-	
Lead time				
Master	t_{LEAD}		0.5	tXCK
Slave	t_{LEAD}	0.5		
Lag time				
Master	t_{LAG}		0.5	tXCK
Slave	t_{LAG}	0.5		
Data setup time (inputs)				
Master	t_{SIM}	30		ns
Slave	t_{SIS}	30		
Data hold time (inputs)				
Master	t_{HIM}	1		t_{SCLK}
Slave	t_{HIS}	1		
Data setup time (outputs)				
Master	t_{SOM}	30		ns
Slave	t_{SOS}	30		
Data hold time (outputs)				
Master	t_{HOM}	30		ns
Slave	t_{HOS}	30		
Disable time	t_{DIS}	1		t_{SCLK}

Table 7.14 Timing characteristics of USART in SYNC. or SPI mode of operations

[NOTE1] In synchronous mode, Lead and Lag time with respect to SS pin is ignored. And the case of UCPHA=0 is also applied to SPI mode only.

[NOTE2] All timing is shown with respect to 20% VDD and 80% VDD.

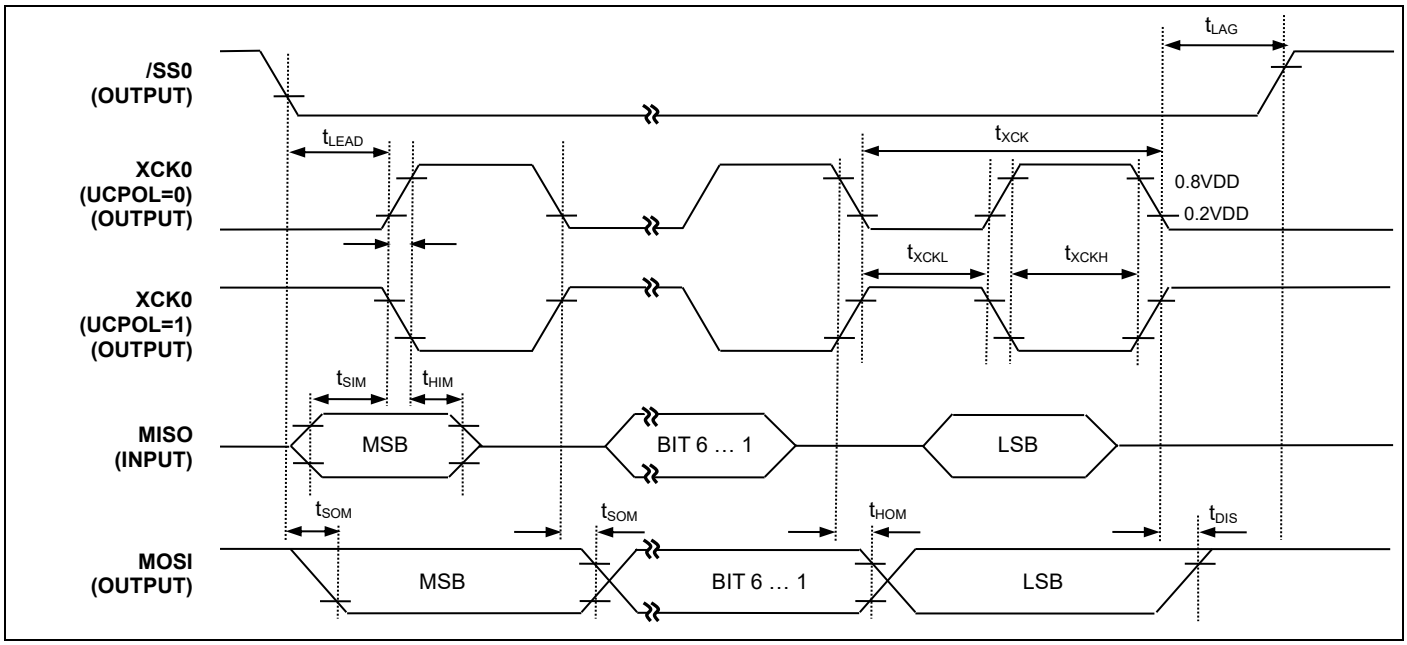


Figure 7.3 SPI master mode timing (UCPHA = 0, MSB first)

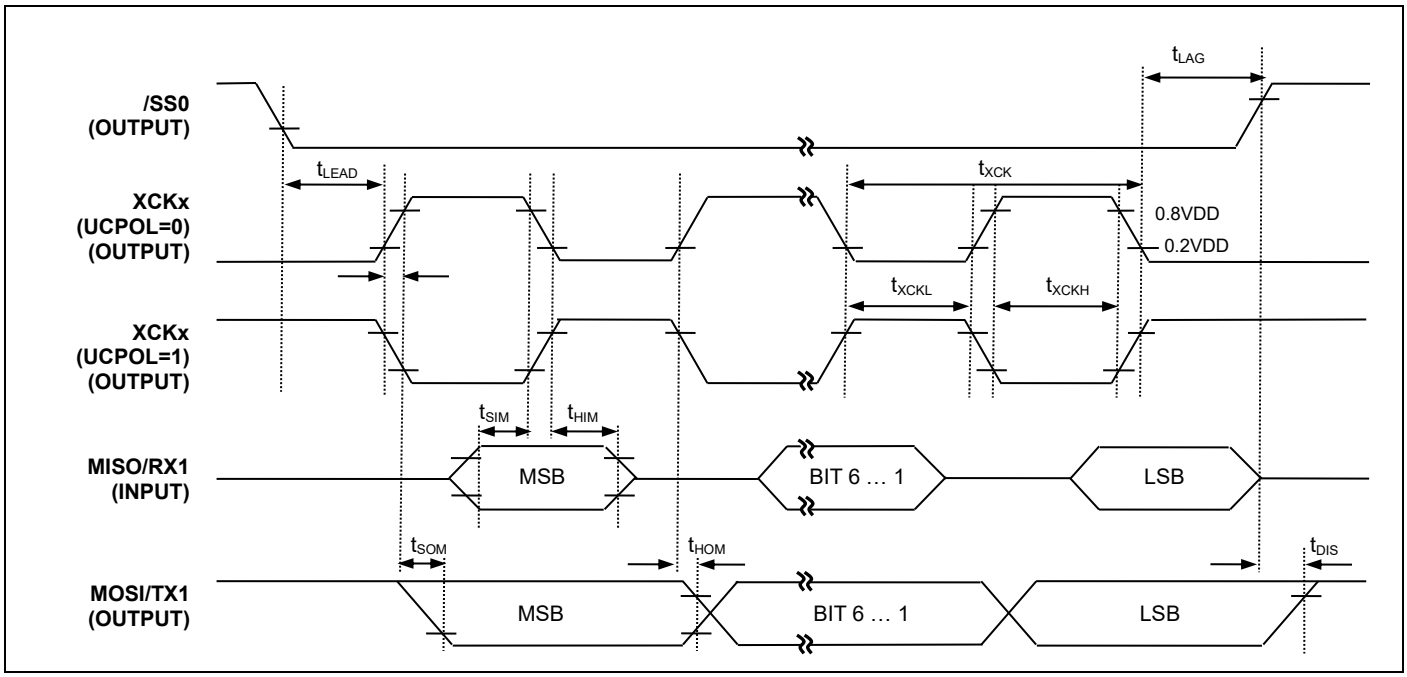


Figure 7.4 SPI / Synchronous master mode timing (UCPHA = 1, MSB first)

NOTE When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

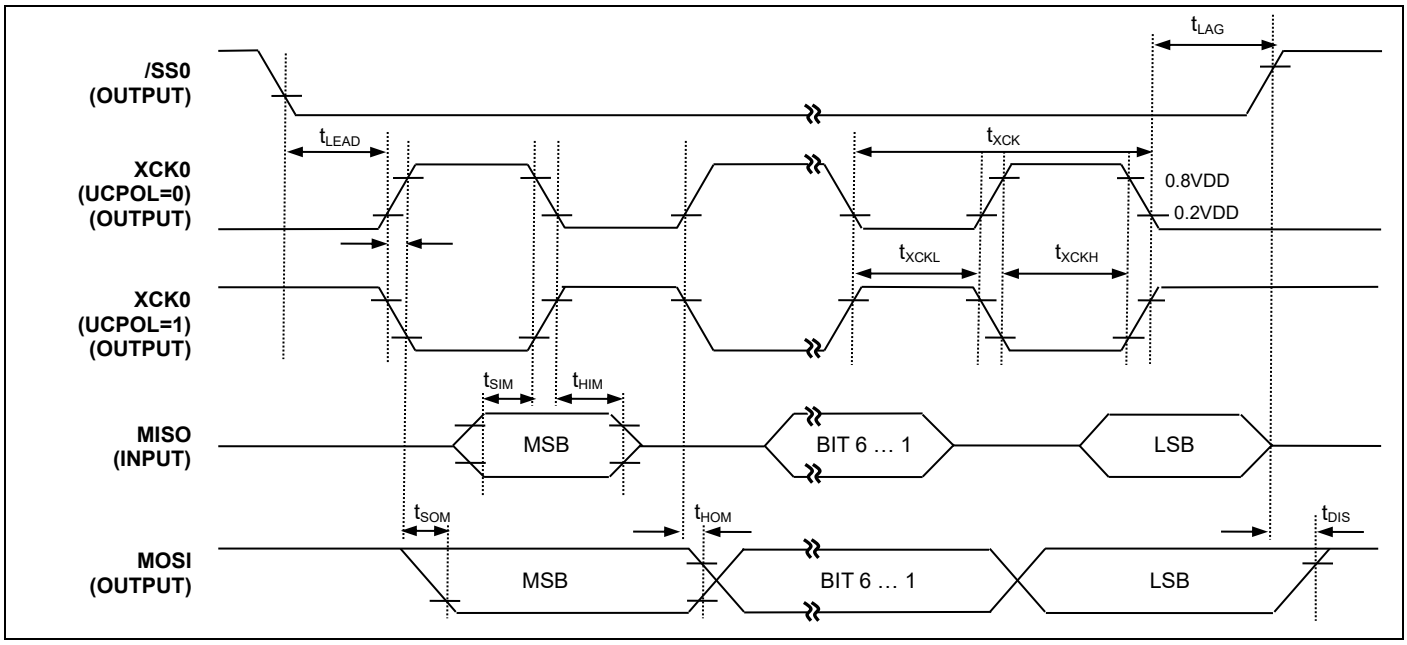


Figure 7.5 SPI slave mode timing (UCPHA = 0, MSB first)

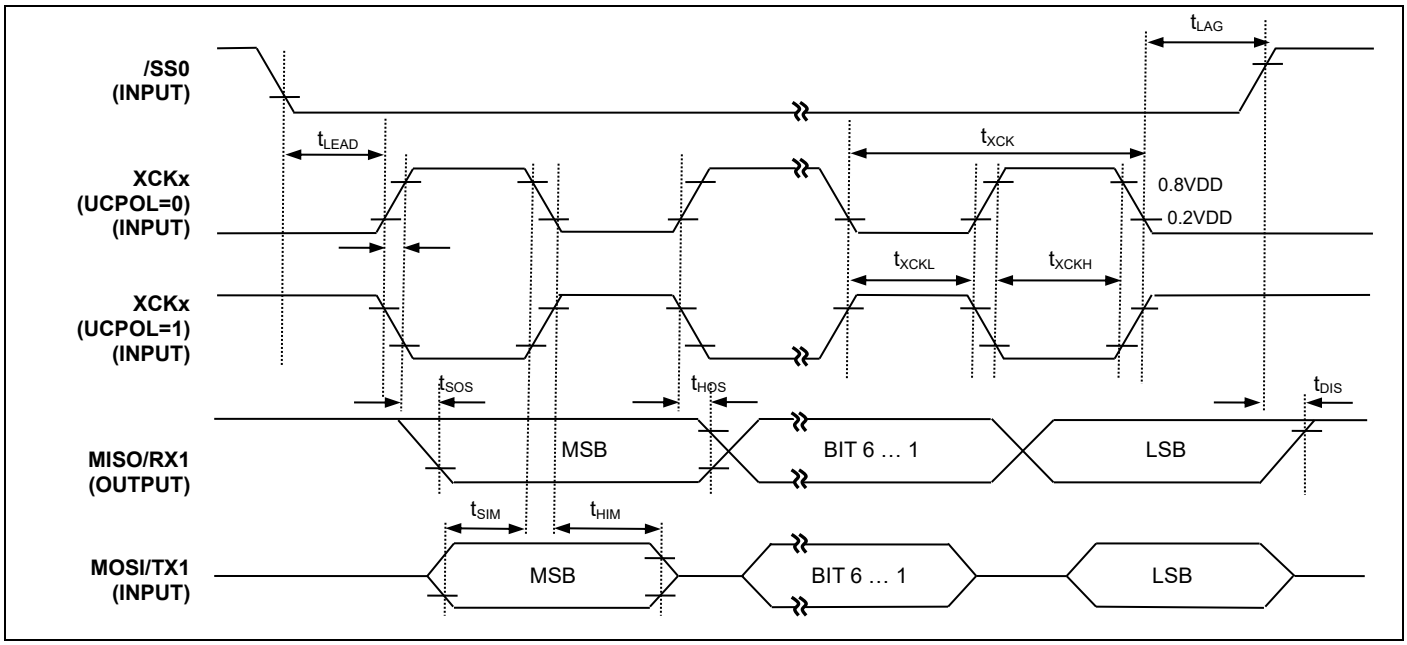


Figure 7.6 SPI / Synchronous slave mode timing (UCPHA = 1, MSB first)

NOTE1 When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

7.15 TYPICAL CHARACTERISTICS

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

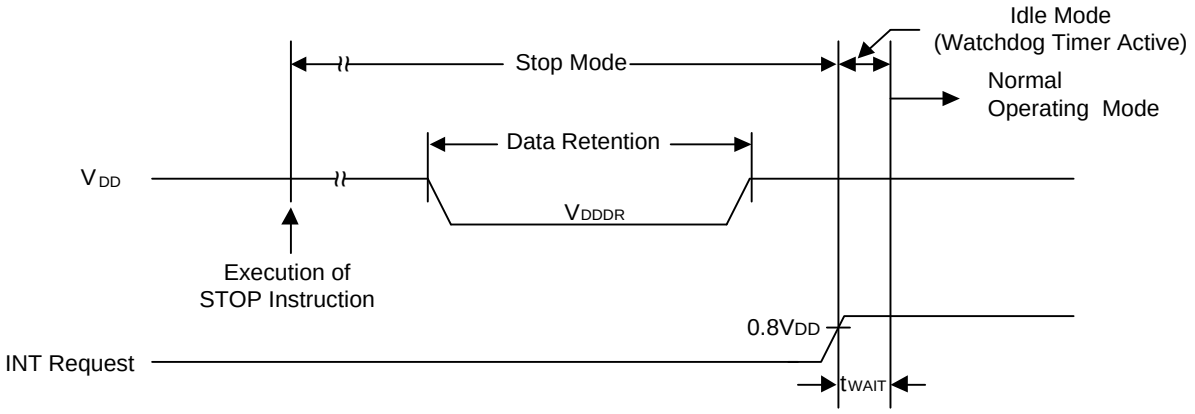
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

7.16 Data Retention Voltage in Stop Mode

(T_A = -25°C ~ +85°C, VDD = Vpor ~ 3.6V)

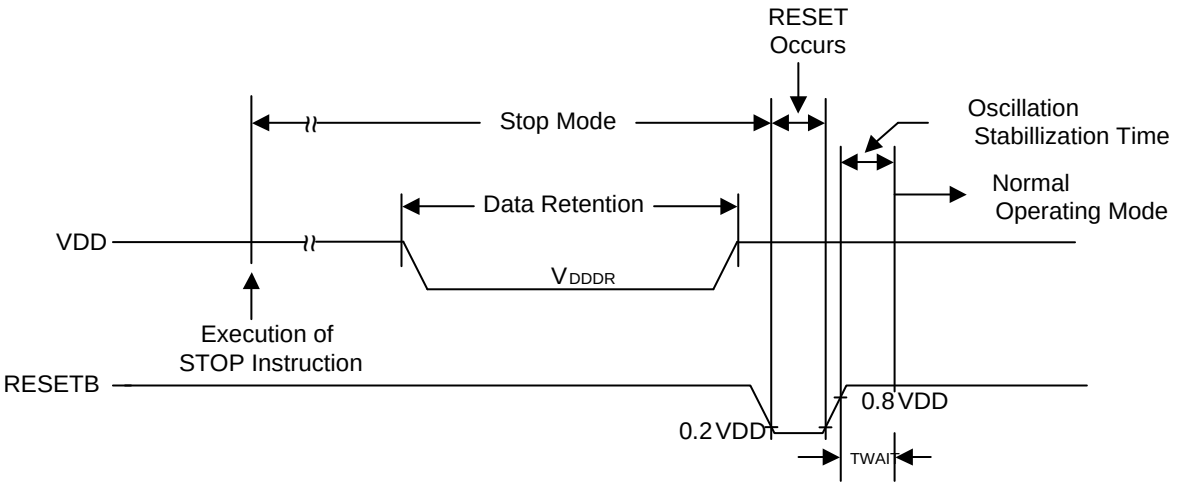
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	Vpor	–	Vmax	V
Data retention supply current	I_{DDDR}	V_{DDR} = 1.65V(T_A = 25°C), Stop mode	–	–	1	uA

Table 7.17 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.8 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 7.9 Stop Mode Release Timing when Initiated by RESETB

7.17 Input/output Capacitance

(T_A = -25°C ~ +85°C, VDD = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.19 Input/output Capacitance

7.18 Main Clock Oscillator Characteristics

(T_A = -25°C ~ +85°C, VDD = 1.71V ~ 3.6V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal Ceramic Oscillator External Clock	Main oscillation frequency Main oscillation frequency XIN input frequency	1.71V – 3.6V	1	–	4	MHz
Crystal Ceramic Oscillator External Clock	Main oscillation frequency Main oscillation frequency XIN input frequency	2.00V – 3.6V	8	8	8	MHz
Crystal Ceramic Oscillator External Clock	Main oscillation frequency Main oscillation frequency XIN input frequency	2.5V – 3.6V	12	12	12	MHz

Table 7.20 Main Clock Oscillator Characteristics

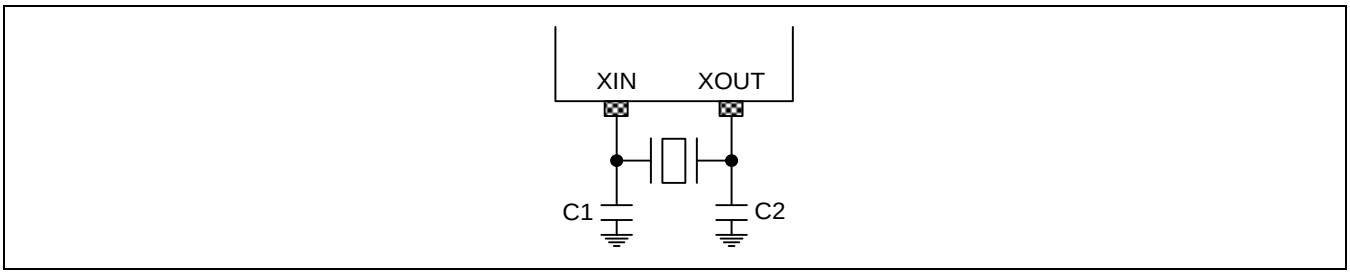


Figure7.10 Crystal/Ceramic Oscillator

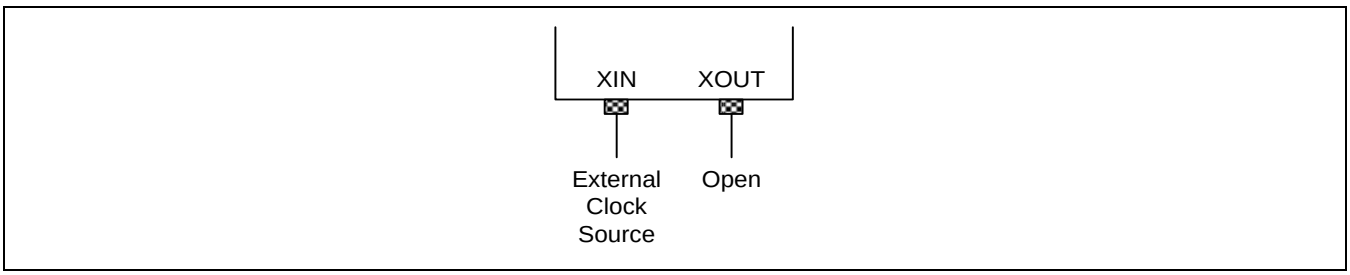


Figure 7.11 External Clock

7.19 Main Oscillation Stabilization Characteristics

(T_A = -25°C ~ +85°C, VDD = 1.71V ~ 3.6V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 4MHz, VDD = 1.71V ~ 3.6V,	–	–	15	ms
	fx > 1MHz, VDD = 1.71V, T_A=-25°C			60	
Ceramic	-	–	–	10	ms
External Clock	f_{XIN} = 1 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

Table 7.21 Main Oscillation Stabilization Characteristics

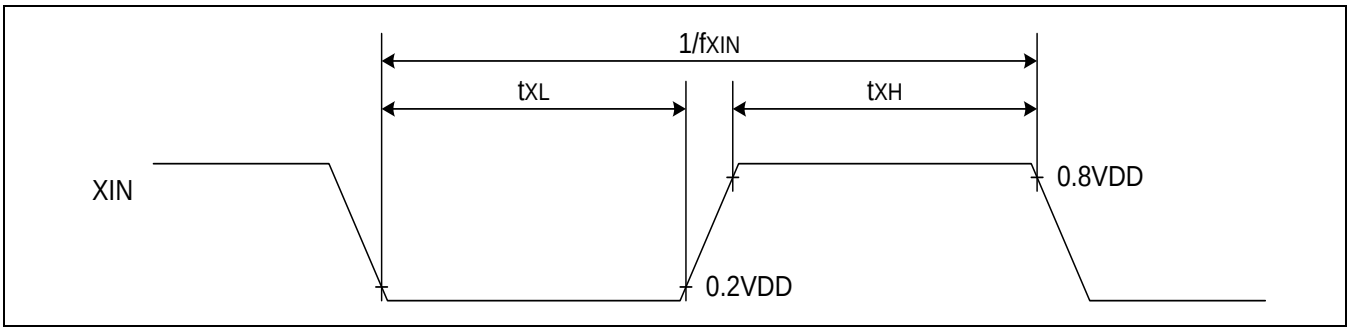


Figure 7.12 Clock Timing Measurements at XIN

7.20 Operating Voltage Range

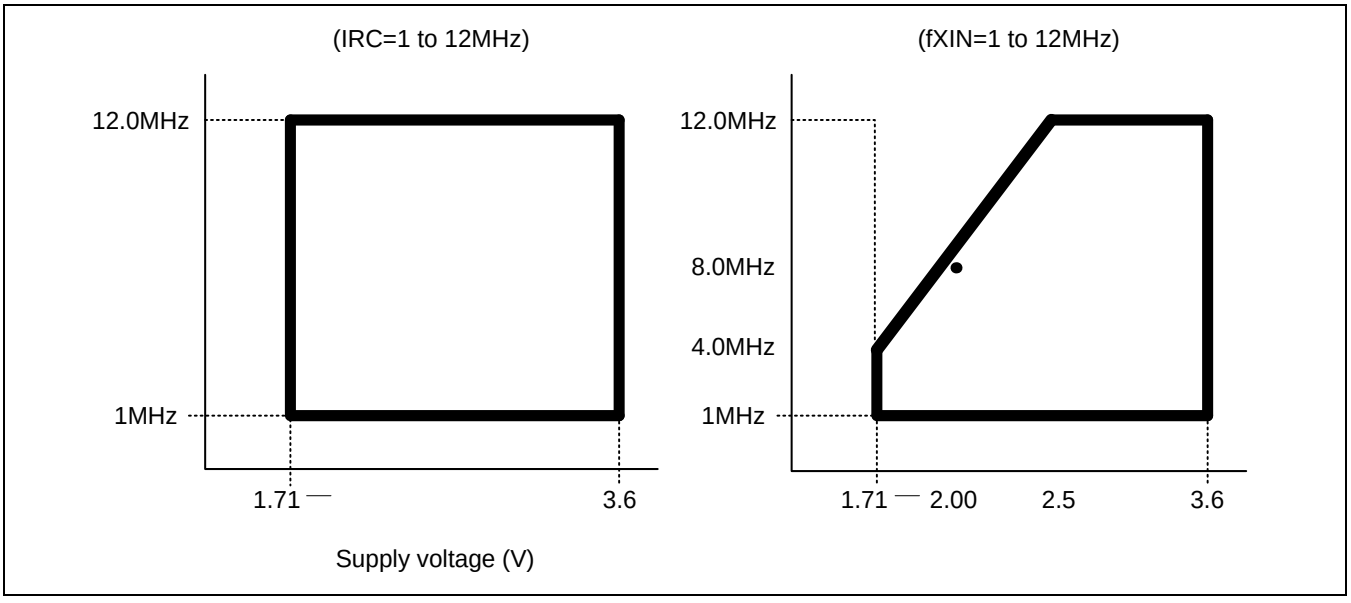


Figure 7.13 Operating Voltage Range

7.21 REM_PP_OUT PORT CHARACTERISTICS

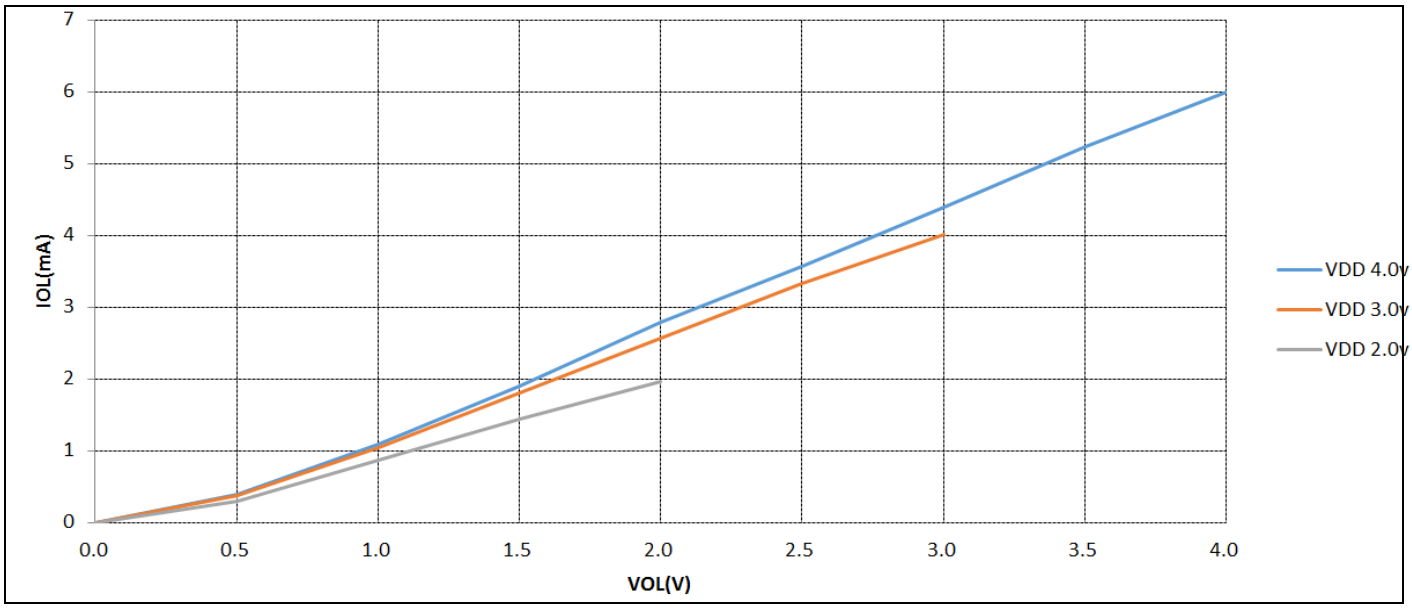


Figure 7.14 IOL vs VOL for REM_PP_OUT

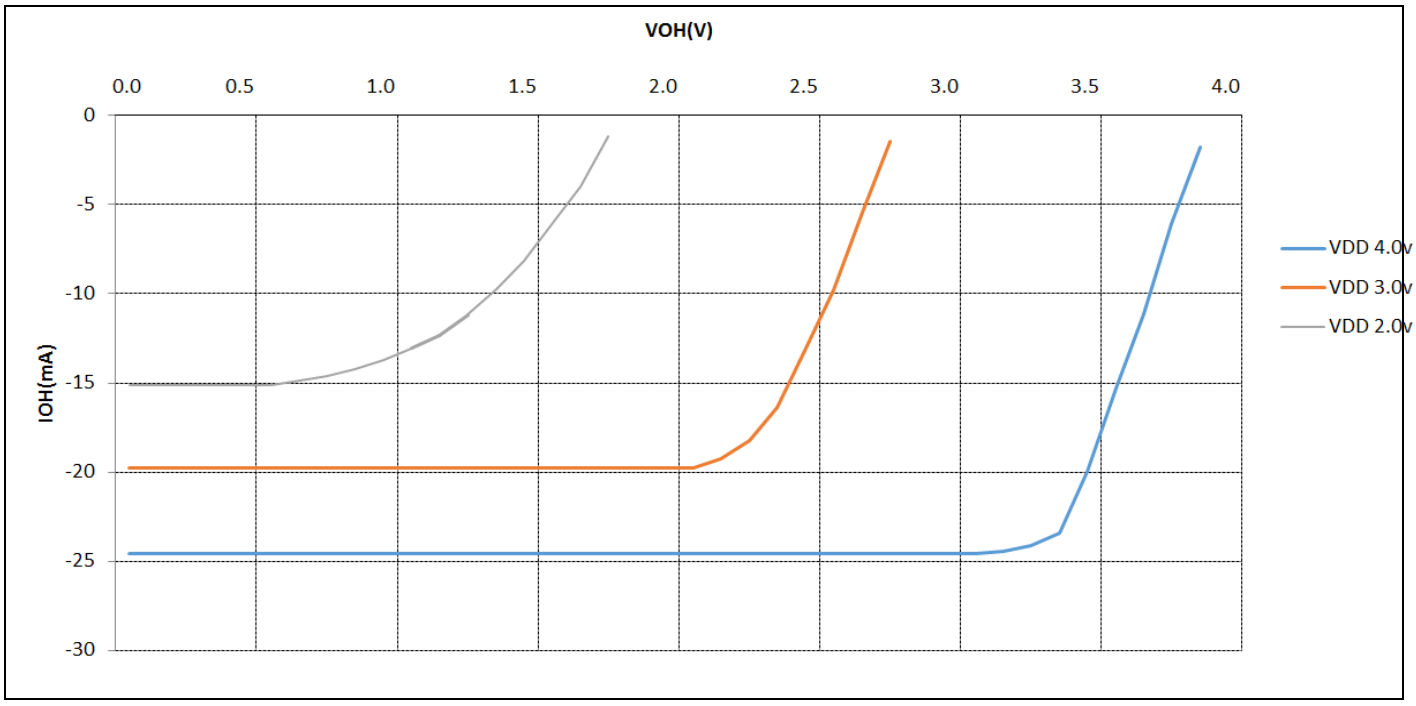


Figure 7.15 IOH vs VOH for REM_PP_OUT

7.22 REM_OD_OUT PORT CHARACTERISTICS

The characteristics of REM_OD_OUT are related with VDD_IR, not VDD.

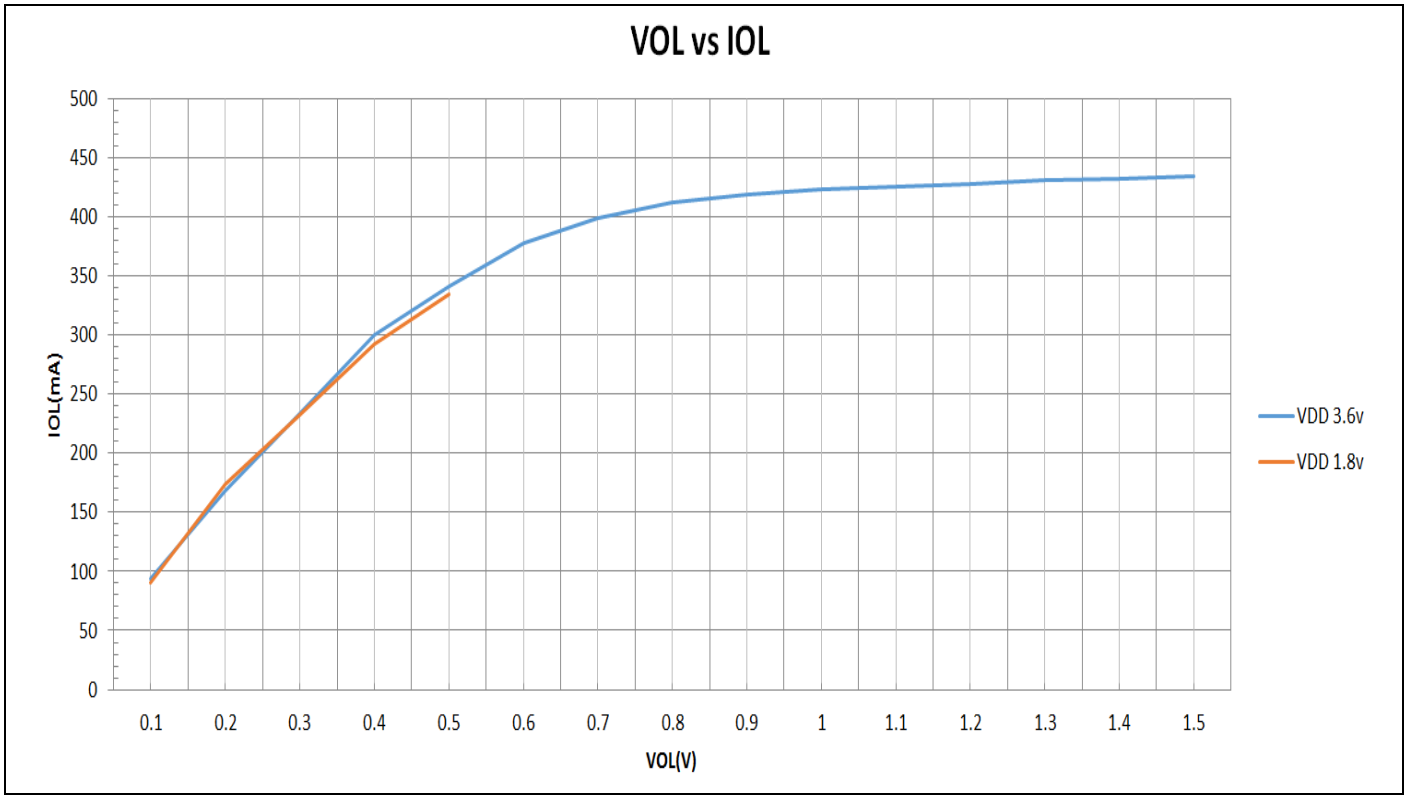


Figure 7.16 IOL vs IOH for REM_OD_OUT

The characteristics of REM_PP_OUT are related with VDD, not VDD_IR.

APPENDIX

Instruction Table

The instruction length of M8051W can be 1, 2, or 3 bytes as listed in the following table. It takes 1, 2, or 4 cycles for the CPU to execute an instruction. The cycle is composed of two internal clock periods.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54

ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90

MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20

JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠ 0	2	2	70
CJNE A,dir,rel	Compare A, direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A, immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

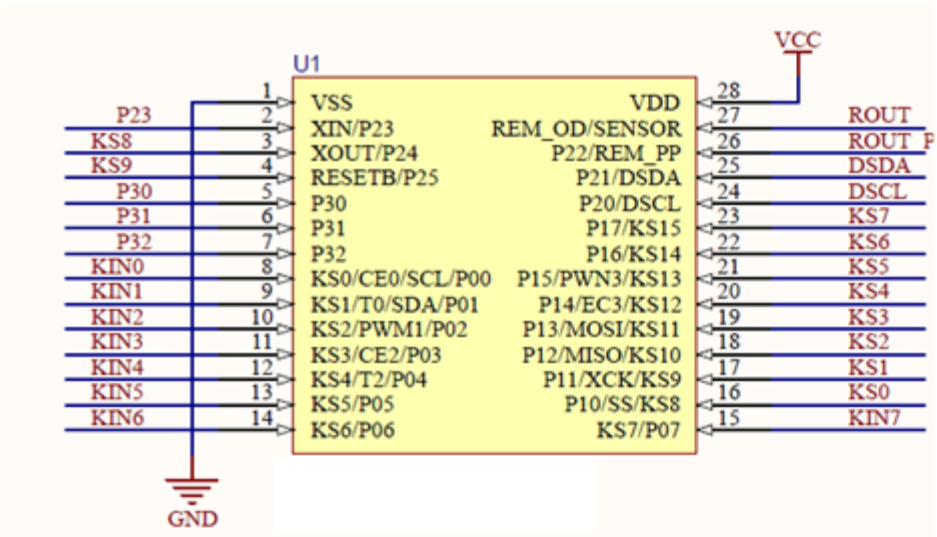
The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

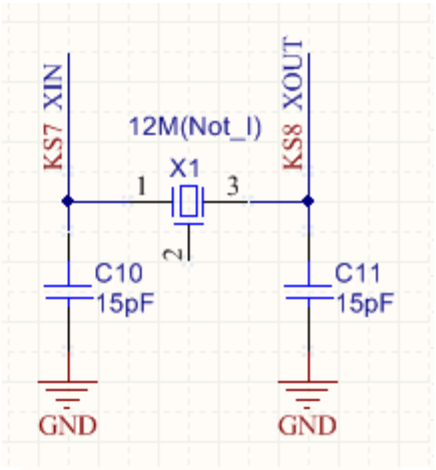
External OSC example schematic.

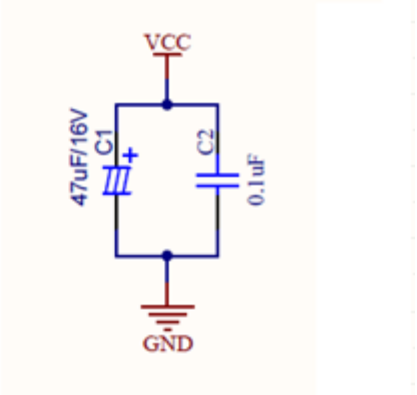
In fact, the parts are not necessarily worth the IRC must be used in order to obtain a satisfactory error rate. Use common parts

Demo Board Conditions are as follows.

- 12MHz oscillator : HC-49S(+- 20ppm)
- External Osc. Capacitor : ELEPARTS(C1608C0G120J50V) 12pF~15pF Tolerance +-0.25pF


U1
VCC
VSS
XIN/P23
XOUT/P24
RESETB/P25
P30
P31
P32
KS0/CE0/SCL/P00
KS1/T0/SDA/P01
KS2/PWM1/P02
KS3/CE2/P03
KS4/T2/P04
KS5/P05
KS6/P06
VDD
REM_OD/SENSOR
P22/REM_PP
P21/DSDA
P20/DSCL
P17/KS15
P16/KS14
P15/PWN3/KS13
P14/EC3/KS12
P13/MOSI/KS11
P12/MISO/KS10
P11/XCK/KS9
P10/SS/KS8
KS7/P07
P23
KS8
KS9
P30
P31
P32
KIN0
KIN1
KIN2
KIN3
KIN4
KIN5
KIN6
ROUT
ROUT_F
DSDA
DSCL
KS7
KS6
KS5
KS4
KS3
KS2
KS1
KS0
KIN7
GND


KS7 XIN
KS8 XOUT
12M(Not_I)
X1
1
2
3
C10
15pF
C11
15pF
GND
GND


VCC
47uF/16V
C1
C2
0.1uF
GND

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