A96G174/A96S174 Datasheet

16 MHz 8-bit A96G174/A96S174 Microcontroller
8 Kbyte Flash memory, 12-bit ADC, 3 Timers, USART, I2C, Window WDT

Datasheet Version 1.12

Feature

Core

- 8-bit CISC M8051 core
  (8051 Compatible, 2 clocks per cycle)

8 Kbytes On-Chip FLASH

- Endurance : 30,000 times
- In-System Programming (ISP)

256 bytes IRAM / 256 bytes XRAM

General Purpose I/O (GPIO)

Normal I/O : 18 Port (P0[7:0], P1[7:0], P2[7:0], P3[2:0])

Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Window Watch Dog Timer (WWDT) 8-bit × 1-ch
- 8-bit × 1-ch (T0), 16-bit × 2-ch (T1/T2)

Programmable Pulse Generation

- Pulse generation (by T1/T2)
- 8-bit PWM (by T0)
- 16-bit Complementary PWM (by T1)

USART

- 8-bit USART × 1-ch or 8-bit SPI × 1-ch
- Receiver Time Out(RTO)
- 0% Error Baud Rate

I2C

- 8-bit I2C × 1-ch

12-bit A/D Converter

- 15 Input channels,
- Internal BGR Typ. 1.20V

Power On Reset

- Reset release level (1.32V)

Low Voltage Reset

5 levels detect (1.61/1.77/2.13/2.46/3.56)

Low Voltage Indicator

3 levels detect (1.77/2.13/2.46/3.56V)

Interrupt Sources

- EINT0/1/2/PCI (4)
- Timer(0/1/2) (3)
- WDT (1), BIT (1)
- USART RX/TX (2), I2C (1)
- ADC (1), LVI (1)

Internal RC Oscillator

- HSIRC 32MHz ±1.5% (TA=0~ +50°C)
- HSIRC 32MHz ±2.0% (TA=-10~ +70°C)
- HSIRC 32MHz ±2.5% (TA=-40~ +85°C)
- HSIRC 32MHz ±5.0% (TA=-40~ +105°C)
- LSIRC 128kHz ±20% (TA= -40~ +85°C)
- LSIRC 128kHz ±30% (TA= -40~ +105°C)

Power Down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- 1.8V~ 5.5V (@0.5 ~ 16.0MHz with HSI RC-OSC)

Minimum Instruction Execution Time

- 125ns (@16MHz main clock)

Operating temperature

- –40 ~ +85℃, –40 ~ +105℃

Package Type

- 20 TSSOP / SOP / QFN, 16 SOPN
- Pb-free package

Product selection table

Table 1. Device Summary

Part Number	Flash	XRAM	IRAM	Timer	PWM	Peripheral	ADC 12-bit	GPIO	Package	Temperature Range
A96G174FR	8KB	256 bytes	256 bytes	3	3	USART, I2C	15	18	20 TSSOP	-40°C~+85°C
A96S174FR	8KB	256 bytes	256 bytes				14	18	20 TSSOP	
A96G174FD	8KB	256 bytes	256 bytes				15	18	20 SOP	

A96G174/A96S174
Datasheet

16 MHz 8-bit A96G174/A96S174 Microcontroller
8 Kbyte Flash memory, 12-bit ADC, 3 Timers, USART, I2C, Window WDT

A96G174FU	8KB	256 bytes	256 bytes				15	18	20 QFN	
A96S174FU	8KB	256 bytes	256 bytes				14	18	20 QFN	
A96G174AE	8KB	256 bytes	256 bytes				13	14	16 SOPN	
A96G174FR2*	8KB	256 bytes	256 bytes	3	3	USART, I2C	15	18	20 TSSOP	-40°C~+105°C
A96S174FR2*	8KB	256 bytes	256 bytes				14	18	20 TSSOP	
A96G174FD2*	8KB	256 bytes	256 bytes				15	18	20 SOP	
A96G174FU2*	8KB	256 bytes	256 bytes				15	18	20 QFN	
A96S174FU2*	8KB	256 bytes	256 bytes				14	18	20 QFN	
A96G174AE2*	8KB	256 bytes	256 bytes				13	14	16 SOPN	

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

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1 Description

A96G174/A96S174 is an advanced CMOS 8-bit microcontroller with 8Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A96G174/A96S174 and peripheral counts are introduced.

Table 2. A96G174/A96S174 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	8-bit CISC core (M8051, 2 clocks per cycle)
	Interrupt	Up to 14 peripheral interrupts supported. • EINT0 to 2, PCI (4) • Timer (0/1/2) (3) • WDT (1) • BIT (1) • USART Rx/Tx (2) • I2C (1) • ADC (1) • LVI (1)
Memory	ROM (FLASH) capacity	• 8Kbytes FLASH with self-read and write capability • In-system programming (ISP) • Endurance: 30,000times
	IRAM	256Bytes
	XRAM	256Bytes
Programmable pulse generation		• Pulse generation (by T1/T2) • 8-bit PWM (by T0) • 16-bit Complementary PWM (by T1, Dead time)
Minimum instruction execution time		• 125ns (@ 16MHz main clock) • 61us (@ 32.768kHz sub clock)
Power down mode		• STOP mode • IDLE mode
General Purpose I/O (GPIO)		• Normal I/O: 18ports

Table 2. A96G174/A96S174 Device Features and Peripheral Counts (continued)

Peripherals		Description
Reset	Power on reset	• Reset release level: 1.32V
	Low voltage reset	• 5 levels detect • 1.61/1.77/2.13/2.46/3.56V
Low voltage indicator		• 3 levels detect • 1.77/2.13/2.46/3.56V
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Window Watch Dog Timer (WWDT) 8-bit x 1-ch. • 8-bit x 1-ch (T0), 16-bit x 2-ch (T1/T2)
Communication function	USART	• 8-bit USART x 1-ch or 8-bit SPI x 1-ch • Receiver timer out (RTO) • 0% error baud rate
	I2C	• Compatible with I2C bus standard • Up to 400kHz
12-bit A/D converter		• 15 input channels
Internal RC oscillator		• HSIRC 32MHz ±1.5% (T_A= 0~ +50°C) • HSIRC 32MHz ±2.0% (T_A=-10~ +70°C) • HSIRC 32MHz ±2.5% (T_A=-40~ +85°C) • HSIRC 32MHz ±5.0% (T_A=-40~ +105°C) • LSIRC 128kHz ±20% (TA= -40~ +85°C) • LSIRC 128kHz ±30% (TA= -40~ +105°C)
Operating voltage and frequency		• 1.8V to 5.5V @ 32.768kHz with crystal • 1.8V to 5.5V @ 0.5MHz to 16.0MHz with internal RC
Operating temperature		• -40℃ to +85, -40℃ to +105℃
Package		• Pb-free packages • 20 SOP / TSSOP / QFN • 16 SOPN

1.2 A96G174/A96S174 block diagram

In this section, A96G174/A96S174 device with peripherals is described in a block diagram.

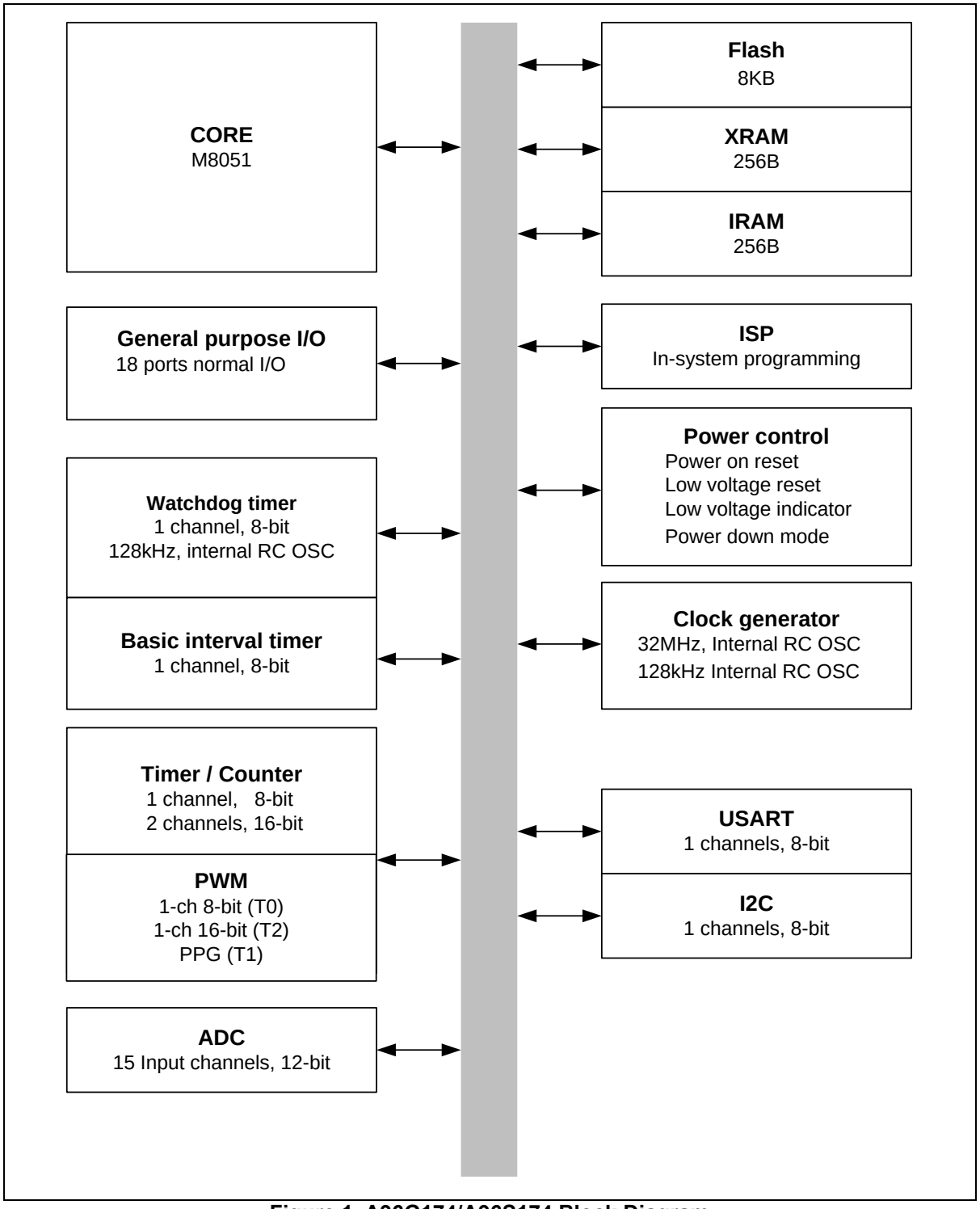
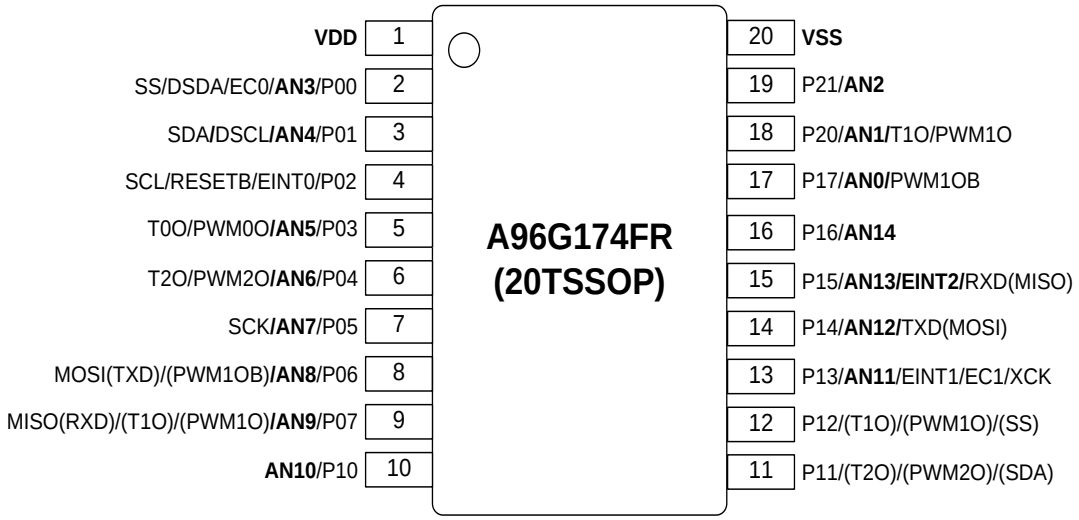


Figure 1. A96G174/A96S174 Block Diagram

2 Pinouts and pin description

Pinouts and pin descriptions of A96G174/A96S174 device are introduce in the following sections.

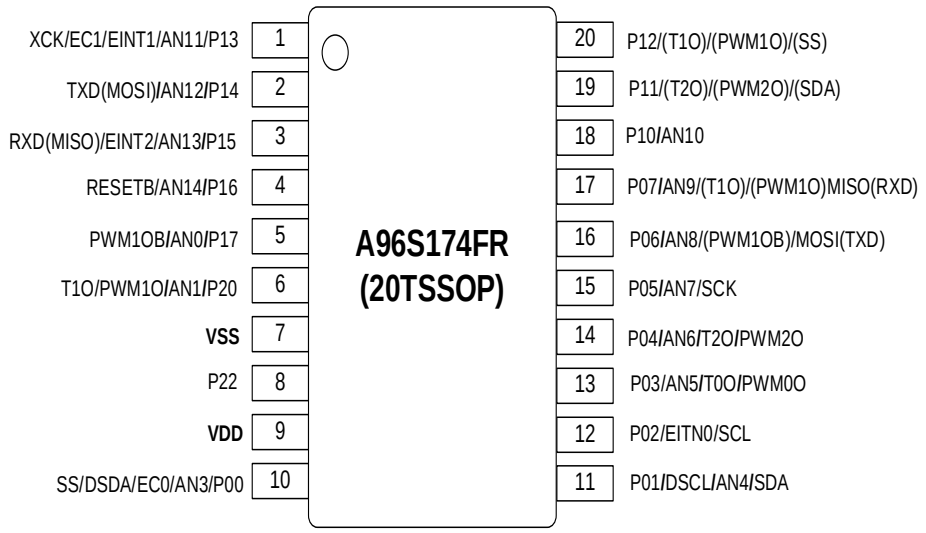
2.1 Pinouts



NOTES:

1. Programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P22 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 20-pin package is used.

Figure 2. A96G174 20TSSOP Pin Assignment

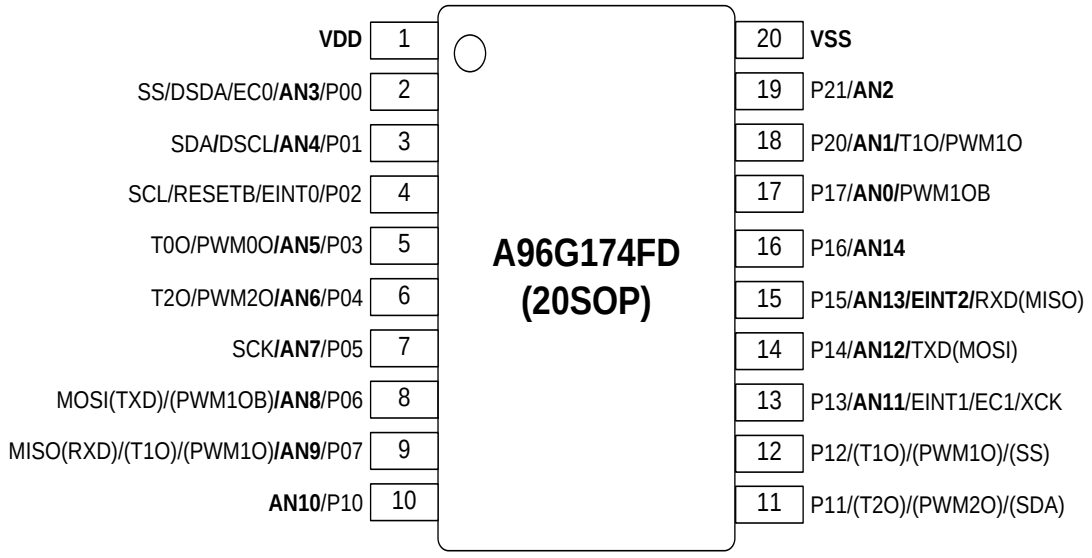


NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 20-pin package is used.

3.

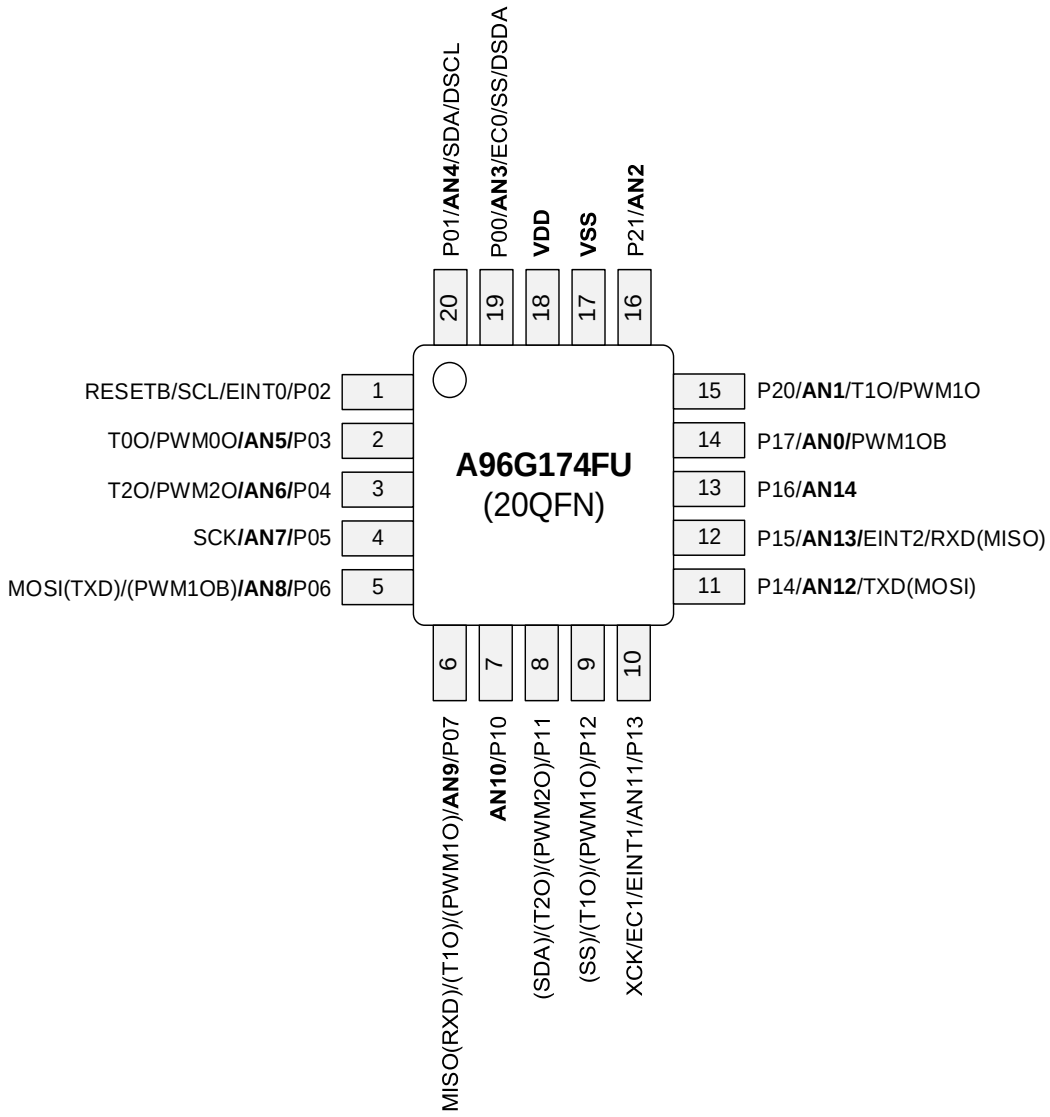
Figure 3. A96S174 20TSSOP pin assignment



NOTES:
1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P22 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 20-pin package is used.

3.

Figure 4. A96G174 20SOP Pin Assignment

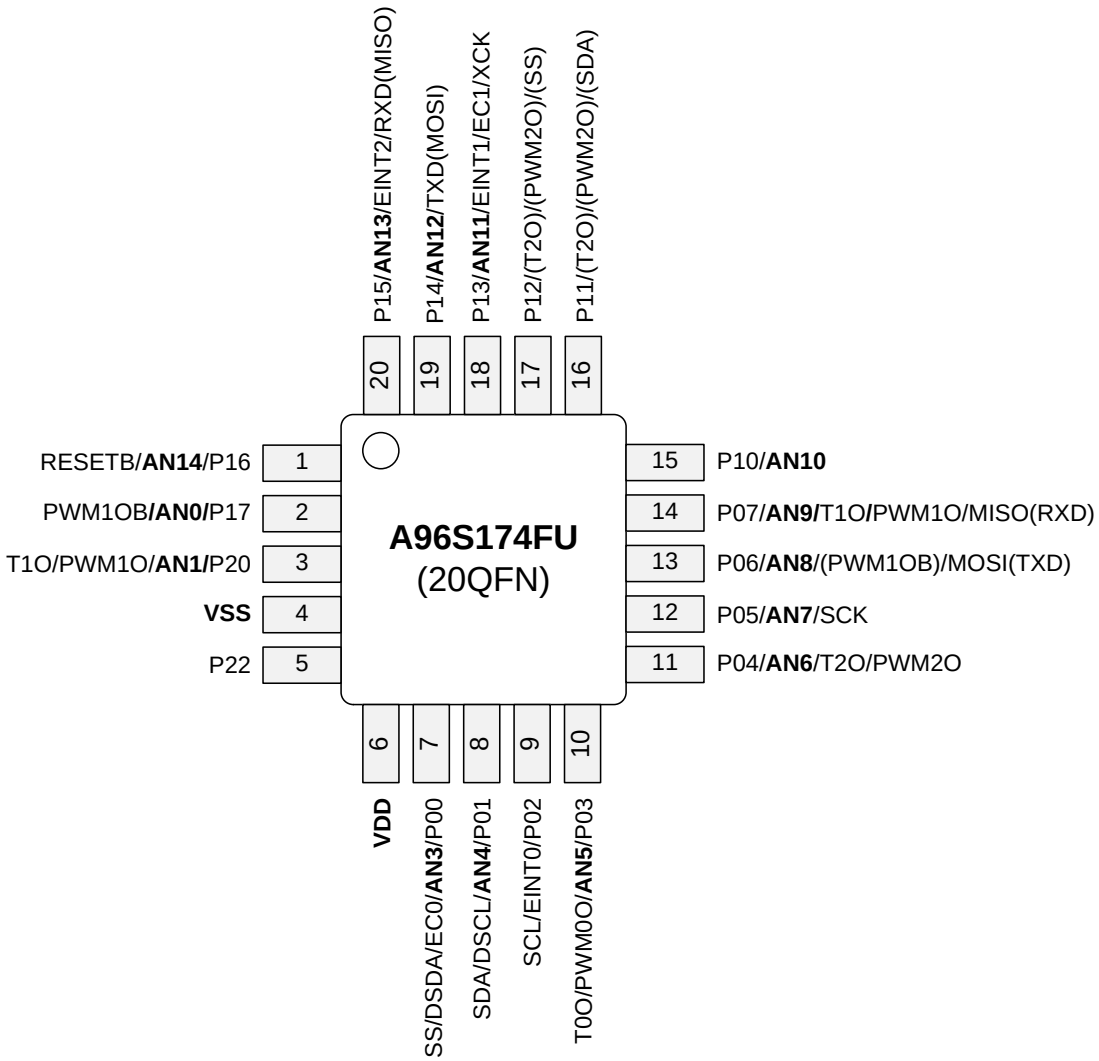


NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P22 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 20-pin package is used.

3.

Figure 5. A96G174 20QFN Pin Assignment

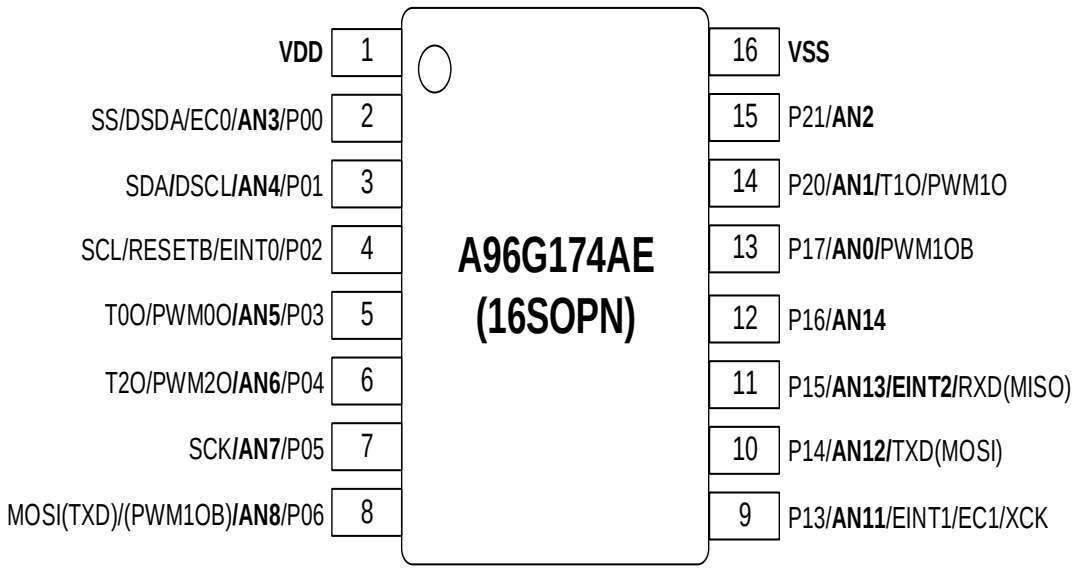


NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA.
2. The P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 20-pin package is used.

3.

Figure 6. A96S174 20QFN Pin Assignment



NOTE: The programmer (E-PGM+, E-Gang4/6) uses P0[1:0] pin as DSCL, DSDA

Figure 7. A94G174 16SOPN Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

Pin no.			PIN Name	I/O[2]	Description	Remark
20TSSOP	20QFN	16SOPN				
2(10) [1]	19(7)[1]	2	P00*	IOUS	Port 0 bit 0 Input/output	
			AN3	IA	ADC input ch-3	
			EC0	I	Timer 0(Event Capture) input	
			DSDA	IO	OCD debugger data input/output	Pull-up
			SS	IO	USART slave select signal	
3(11)	20(8)	3	P01*	IOUS	Port 0 bit 1 Input/output	
			AN4	IA	ADC input ch-4	
			DSCL	I	OCD debugger clock	Pull-up
			SDA	IO	I2C data signal	
4(12)	1(9)	4	P02*	IOUS	Port 0 bit 2 Input/output	
			RESETB	IU	A96G174 only, Reset pin	Pull-up
			EINT0	I	External interrupt input ch-0	
			SCL	IO	I2C clock signal	
5(13)	2(10)	5	P03*	IOUS	Port 0 bit 3 Input/output	
			AN5	IA	ADC input ch-5	
			T0O	O	Timer 0 interval output	
			PWM0O	O	Timer 0 PWM output	
6(14)	3(11)	6	P04*	IOUS	Port 0 bit 4 Input/output	
			AN6	IA	ADC input ch-6	
			T2O	O	Timer 2 interval output	
			PWM2O	O	Timer 2 PWM output	
7(15)	4(12)	7	P05*	IOUS	Port 0 bit 5 Input/output	
			AN7	IA	ADC input ch-7	
			SCK	IO	USART external clock input/output	
8(16)	5(13)	8	P06*	IOUS	Port 0 bit 6 Input/output	
			AN8	IA	ADC input ch-8	
			MOSI (TXD)	IO	USART data transmit /SPI MOSI	
			PWM1OB	O	Timer 1 PWM complementary output	
9(17)	6(14)	-	P07*	IOUS	Port 0 bit 7 Input/output	
			AN9	IA	ADC input ch-9	
			MISO (RXD)	IO	USART data receive /SPI MISO	

Table 3. Normal Pin Description (continued)

Pin no.			PIN Name	I/O[2]	Description	Remark
20TSSOP	20QFN	16SOPN				
9(17)	6(14)	-	T1O	O	Timer 1 interval output	
			PWM1O	O	Timer 1 PWM output	
10(18)	7(15)	-	P10*	IOUS	Port 1 bit 0 Input/output	
			AN10	IA	ADC input ch-10	
11(19)	8(16)	-	P11*	IOUS	Port 1 bit 1 Input/output	
			T2O	O	Timer 2 interval output	
			PWM2O	O	Timer 2 PWM output	

			SDA	IO	I2C data signal	
12(20)	9(17)	-	P12*	IOUS	Port 1 bit 2 Input/output	
			T1O	O	Timer 1 interval output	
			PWM1O	O	Timer 1 PWM output	
			SS	IO	USART slave select signal	
13(1)	10(18)	9	P13*	IOUS	Port 1 bit 3 Input/output	
			AN11	IA	ADC input ch-11	
			EINT1	I	External interrupt input ch-1	
			EC1	I	Timer 1(Event Capture) input	
			XCK	IO	USART clock signal	
14(2)	11(19)	10	P14*	IOUS	Port 1 bit 4 Input/output	
			AN12	IA	ADC input ch-12	
			TXD (MOSI)	IO	USART data transmit /SPI MOSI	
15(3)	12(20)	11	P15*	IOUS	Port 1 bit 5 Input/output	
			AN13	IA	ADC input ch-13	
			EINT2	I	External interrupt input ch-2	
			RXD (MISO)	IO	USART data receive /SPI MISO	
16(4)	13(1)	12	P16*	IOUS	Port 1 bit 6 Input/output	
			AN14	IA	ADC input ch-14	
			RESETB	IU	A96S174 only, Reset pin	
17(5)	14(2)	13	P17*	IOUS	Port 1 bit 7 Input/output	
			AN0	IA	ADC input ch-0	
			PWM1OB	O	Timer 1 PWM Complementary Output	

Table 3. Normal Pin Description (continued)

Pin no.			PIN Name	I/O(2)	Description	Remark
20TSSOP	20QFN	16SOPN				
20(6)	15(3)	14	P20*	IOUS	Port 2 bit 0 Input/output	
			AN1	IA	ADC input ch-1	
			T1O	O	Timer 1 interval output	
			PWM1O	O	Timer 1 PWM output	
21(-)	16(-)	15	P21*	IOUS	Port 2 bit 1 Input/output	
			AN2	IA	ADC input ch-2	
-(8)	-(5)	-	P22 I/O*	IOUS	Port 2 bit 2 Input/output	
1(9)	18(6)	1	VDD	P	VDD	
20(7)	17(4)	16	VSS	P	VSS	

NOTE:

1. (1) It is applied to A96S174.
2. (2) I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
3. (3) The * means ‘Selected pin function after reset condition

3 Port structures

In this chapter, two port structures are introduced in Figure 8 & Figure 9 regarding general purpose I/O port and external interrupt I/O port respectively.

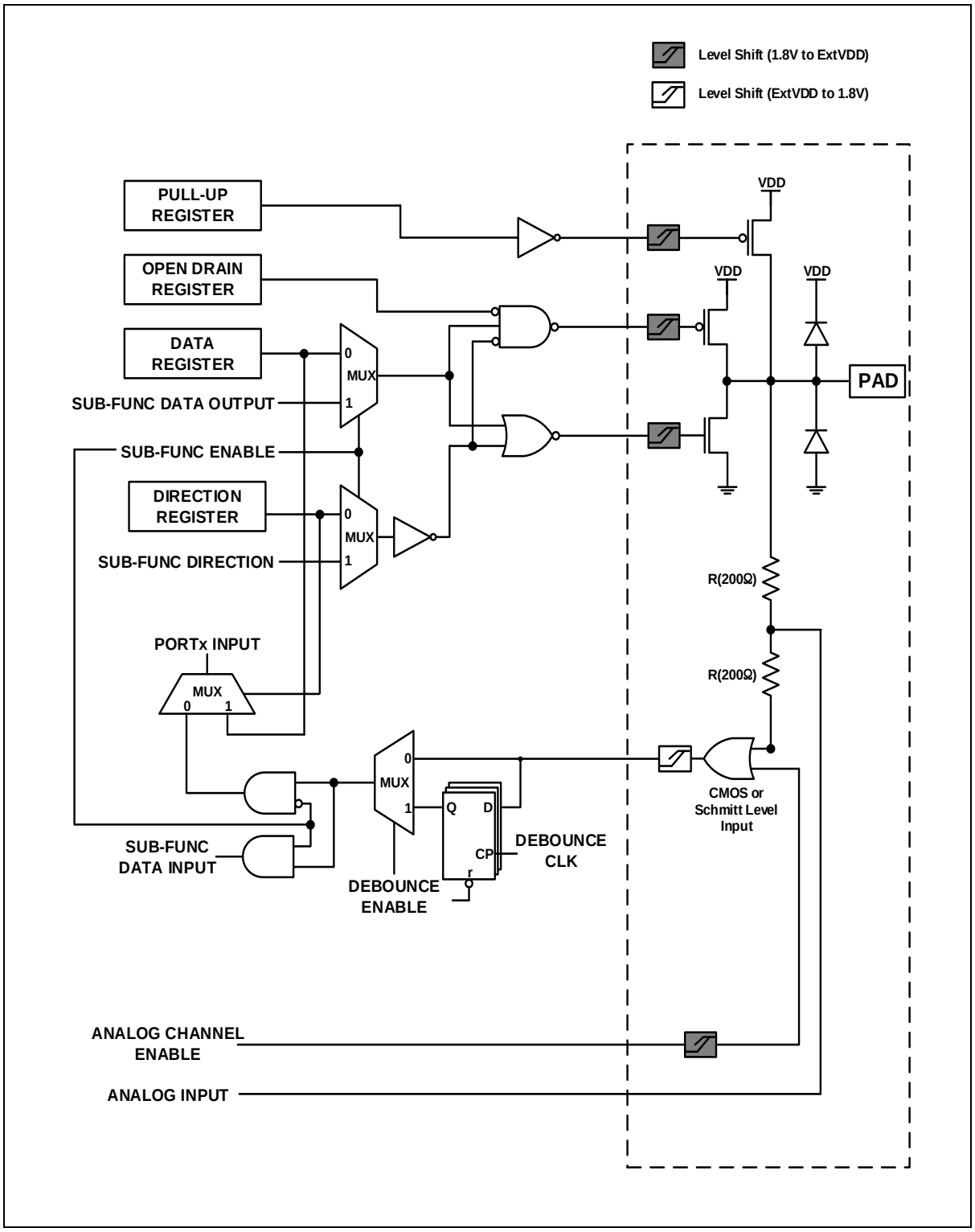


Figure 8. General Purpose I/O Port

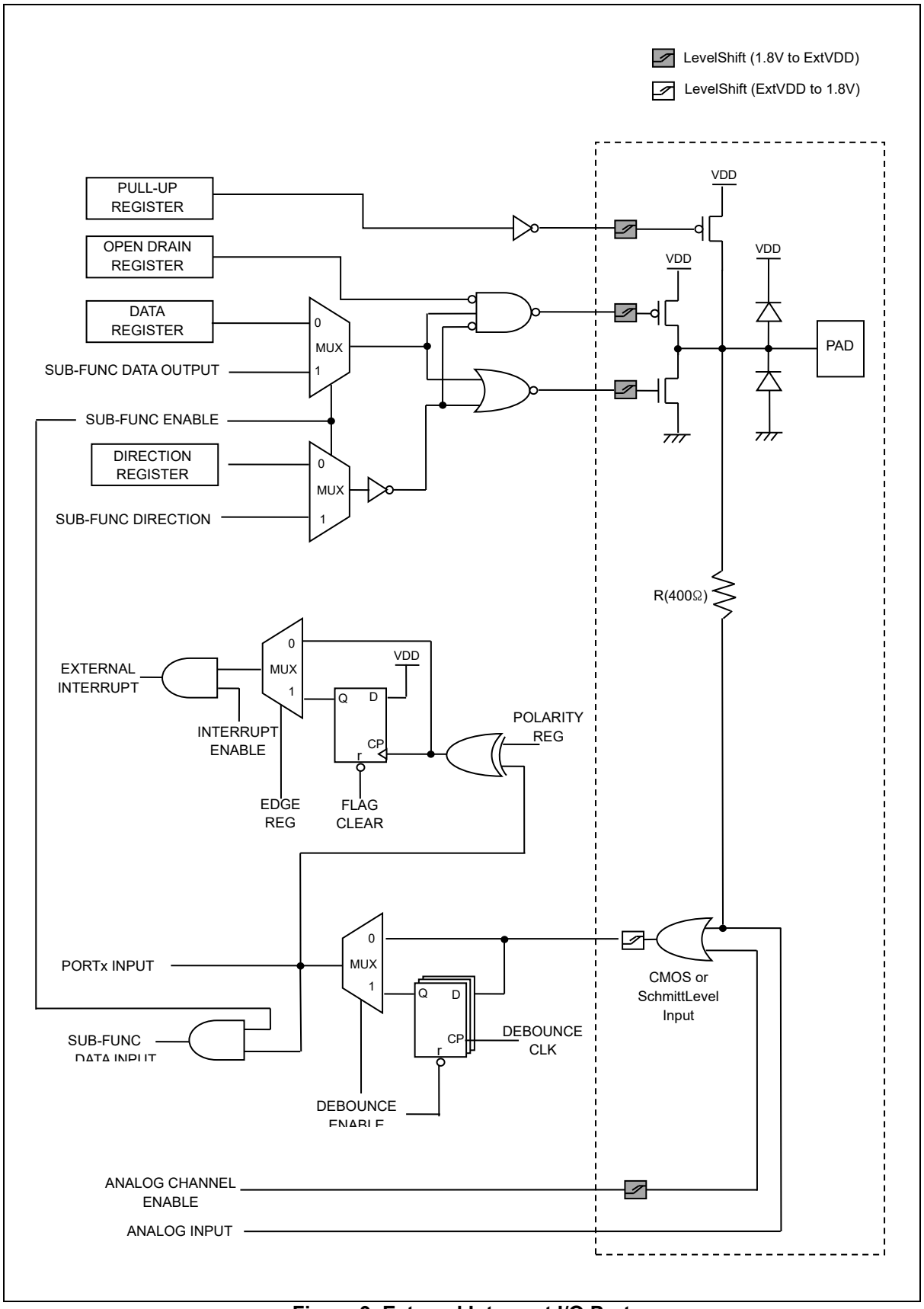


Figure 9. External Interrupt I/O Port

4 Central Processing Unit(CPU)

Central Processing Unit (CPU) of A96G174/A96S174 is based on Mentor Graphics M8051EW core, which offers improved code efficiency and high performance.

4.1 Architecture and registers

Figure 10 shows a block diagram of the M8051EW architecture. As shown in the figure, the M8051EW supports both Program Memory and External Data Memory. In addition, it features a Debug Mode in which it can be driven through a dedicated debug interface.

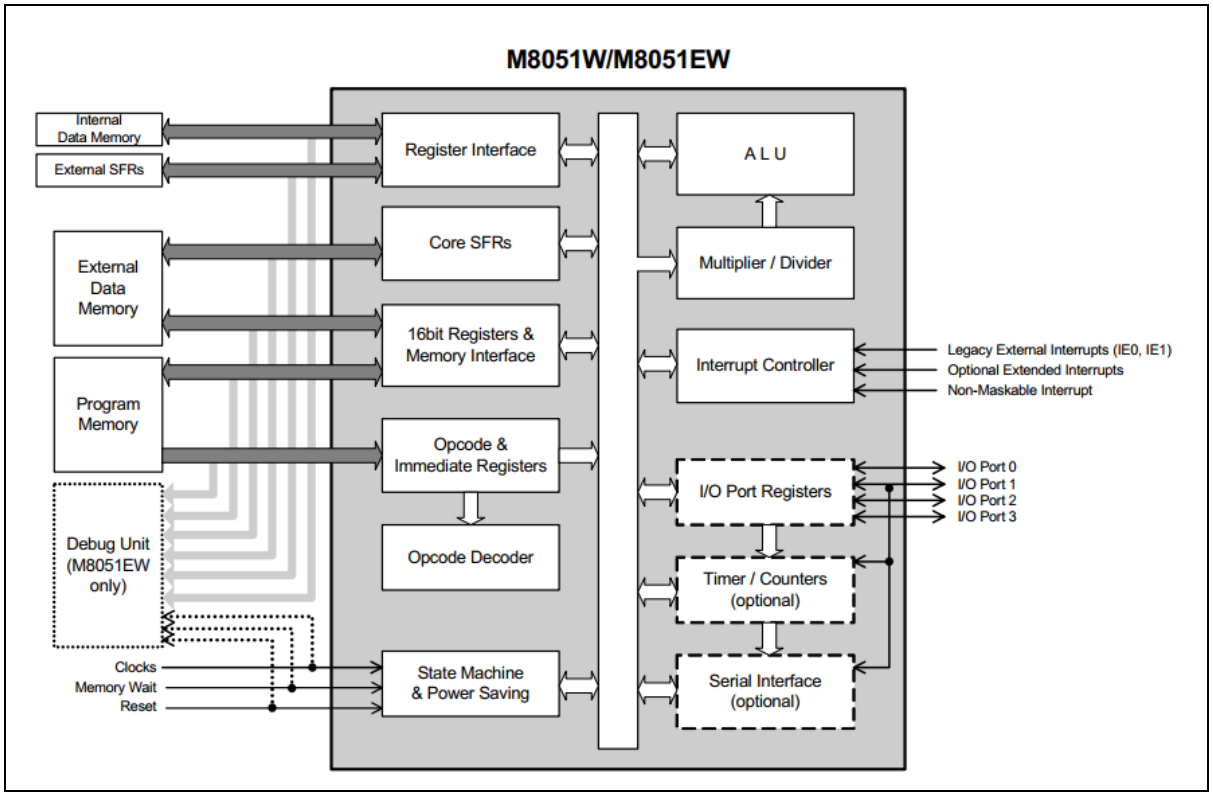


Figure 10 M8051EW Architecture

Main features of the M8051EW are listed below:

- Two clocks per machine cycle architecture:
- Debug support (OCD and OCD II):
- Separate program and external data memory interfaces or a single multiplexed interface
- Support for synchronous and asynchronous Program, External Data and Internal Data Memory
- Wait states support for slow Program and External Data Memory

- 16-bit Data Memory address is generated through the Data Pointer register(DPTR register).
- 16-bit program counter is capable of addressing up to Flash size in Each device
- A single data pointer, two memory-mapped data pointers, or 2 banked data pointers
- Support for 2 or 4 level of priority scheme – Up to 24 maskable Interrupt sources
- External Special Function Register (SFR) are memory mapped into Direct Memory at the addresses between 80 hex and FF hex

4.2 Addressing

The M8051EW supports six types of addressing modes as listed below:

1. Direct addressing mode: In this mode, the operand is specified by the 8-bit address field. Only internal data and SFRs can be accessed using this mode.
2. Indirect addressing mode: In this mode, the operand is specified by addresses contained in a register. Two registers (R0 and R1) from the current bank or the Data Pointer may be used for addressing in this mode. Both internal and external Data Memory may be indirectly addressed.
3. Register addressing mode: In this mode, the operand is specified by the top 3 bits of the opcode, which selects one of the current bank of registers. Four banks of registers are available. The current bank is selected by the 3rd and 4th bits of the PSW.
4. Register specific addressing mode: In this mode, some instructions only operate on specific registers. This is defined by the opcode. In particular many accumulator operations and some stack pointer operations are defined in this manner.
5. Immediate DATA mode: In this mode, Instructions which use Immediate Data are 2 or more bytes long and the Immediate operand is stored in Program Memory as part of the instruction.

   Example) `MOV A, #100`

   It loads the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.
6. Indexed addressing mode: In this mode, only Program Memory can be addressed. It is intended for simple implementation of look-up tables. A 16-bit base register (either the PC or the DPTR) is combined with an offset stored in the accumulator to access data in Program Memory.

4.3 Instruction set

An instruction is a single operation of a processor that is defined by the instruction set. The M8051EW uses the instruction set of 8051 that is broadly classified into five functional categories:

1. Arithmetic instructions
2. Logical instructions
3. Data transfer instructions
4. Boolean instructions
5. Branching instructions

Major features of the instruction set are listed below. If you need detailed information about the instruction table, please refer to **Appendix** or **Instruction table**:

- Instructions are either 1, 2 or 3 bytes long as listed in the ‘Bytes’.
- Each instruction takes either 1, 2 or 4 machine cycles to execute. 1 machine cycle comprises 2 CCLK clock cycles.
- An M8051EW-specific instruction “`MOVC @(DPTR++), A`” is provided to enable software to be downloaded into Program Memory where it is implemented as RAM. This instruction can also be used subsequently to modify contents of the Program Memory RAM.
- Arithmetic Instruction
- Logical Instruction
- Internal data memory
- External data memory
- Unconditional Jumps
- Subroutine calls and returns
- Conditional Jumps
- Boolean Instructions
- Flag

5 Memory organization

A96G174/A96S174 addresses two separate memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the Data Memory more rapidly. 16-bit Data Memory address is generated through the DPTR register.

A96G174/A96S174 provides on-chip 8Kbytes of the ISP type flash program memory, which readable and writable. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 256bytes.

5.1 Program memory

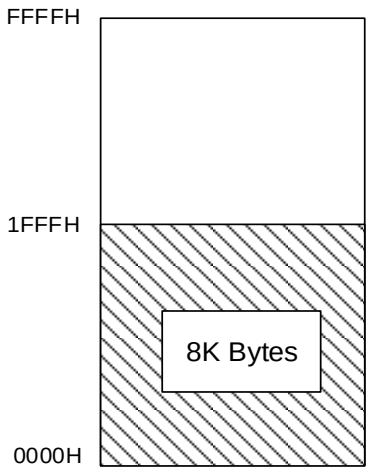
A 16-bit program counter is capable of addressing up to 64Kbytes, and A96G174/A96S174 has just 8Kbytes program memory space.

Figure 11 shows a map of the lower part of the program memory.

After reset, CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in the program memory. An interrupt causes the CPU to jump to the corresponding location, where it commences execution of the service routine.

An external interrupt 11, for example, is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within an interval of 8-bytes.

Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.



NOTE: The 8Kbytes includes the Interrupt Vector Region.

Figure 11. Program Memory Map

5.2 Data memory

Internal data memory space is divided into three blocks, which are generally referred to as lower 128bytes, upper 128bytes, and SFR space. Internal data memory addresses are always one byte wide, which implies an address space of 256bytes. In fact, the addressing modes for the internal data memory can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space, while indirect addresses higher than 7FH access a different memory space. Thus as shown in Figure 12, the upper 128bytes and SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 13. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes of RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

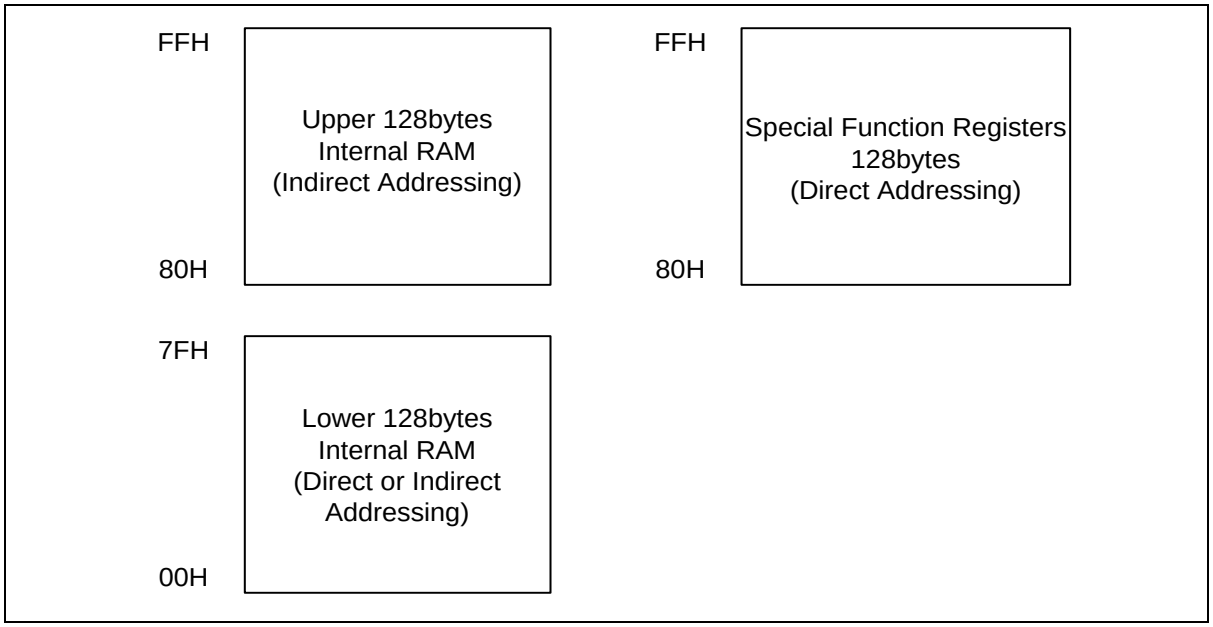


Figure 12. Data Memory Map

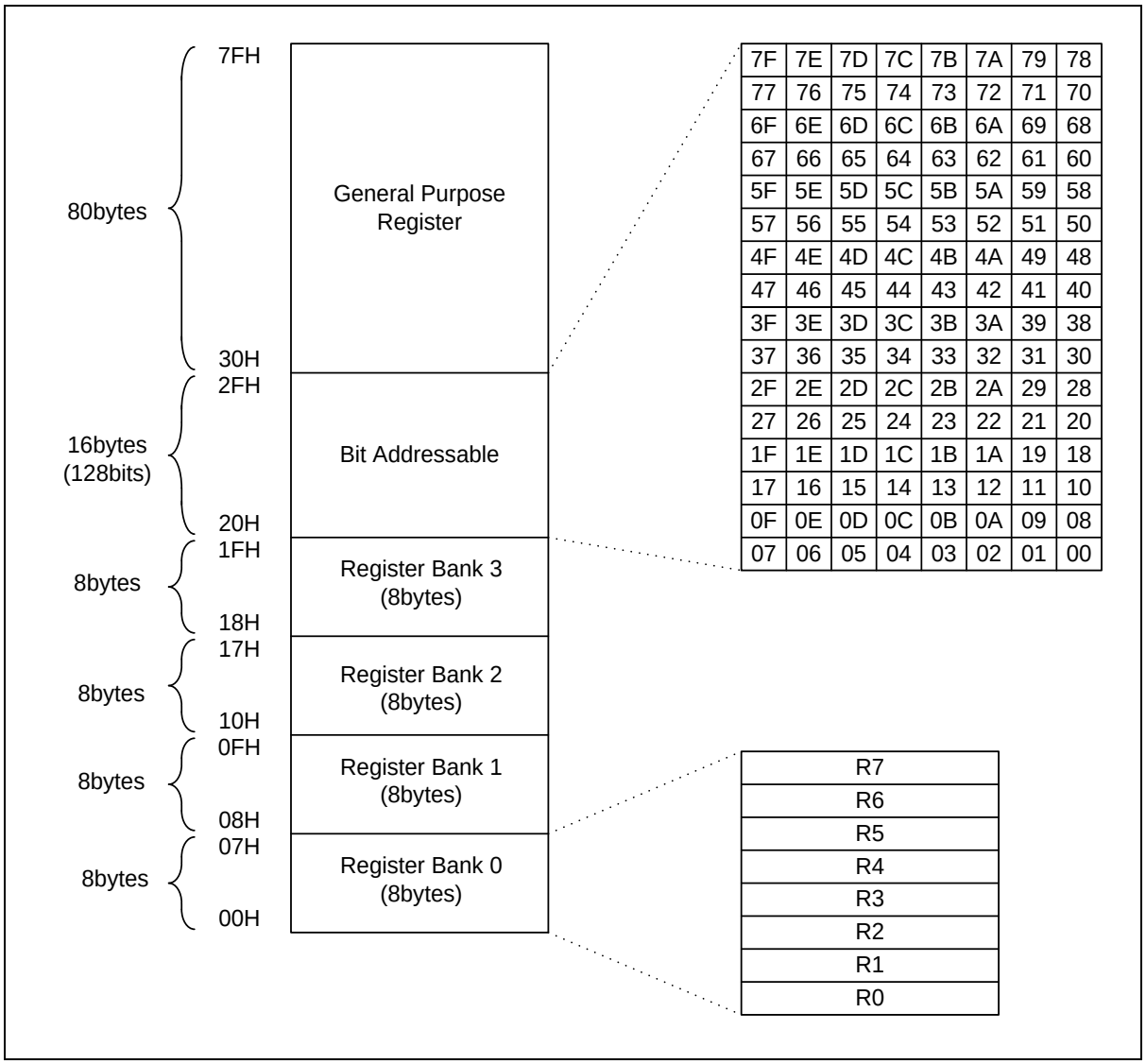


Figure 13. Lower 128bytes of RAM

5.3 External data memory

A96G174/A96S174 has 256bytes of XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

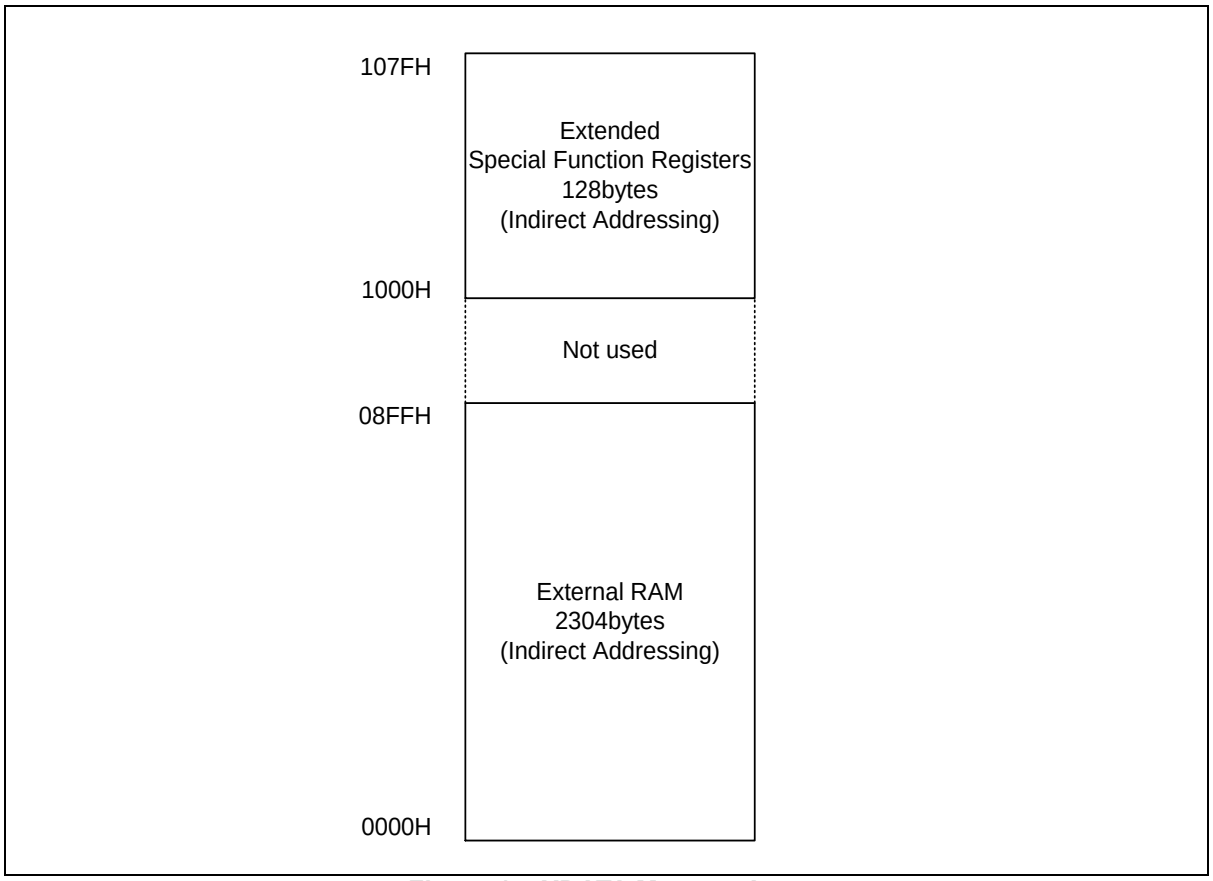


Figure 14. XDATA Memory Area

5.4 SFR map

5.4.1 SFR map summary

Table 4. SFR Map Summary

–	Reserved
	M8051 compatible

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	–	–	UBAUD	UDATA	–	
0F0H	B							
0E8H	RSTFR	I2CSAR	I2CSAR1					
0E0H	ACC	I2CMR	I2CSR	I2CSCLLR	I2CSCLHR	I2CSDAHR	I2CDR	–
0D8H	LVRCR	T1CDRL	T1CDRH	T1DDRL	T1DDRH	–	P0DB	P1DB
0D0H	PSW		P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSR	–
0C8H	OSCCR		–	UCTRL1	UCTRL2	UCTRL3	–	USTAT
0C0H	EIFLAG		T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H		P1IO	T0CR	T0CNT	T0DR/ T0CDR	–	–	–
0A8H	IE	IE1	IE2	–	P0PU	P1PU	P2PU	
0A0H		P0IO	EO	–	EIPOL	–	–	–
98H	–	–	–	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	PCI1	–	–	
88H	P1	–	SCCR	BITCR	BITCNT	WDTCR	WDTIDR	
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTE: 00H/8H, these registers are bit-addressable.

Table 5. XSFR Map Summary

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
1078H	–	–	–	–	–	–	–	–
1070H	–	–	–	–	–	–	–	–
1068H	–	–	–	–	–	–	–	–
1060H	–	–	–	–	–	–	–	–
1058H	–	–	–	–	–	–	–	–
1050H	–	–	–	–	–	–	–	–
1048H	–	–	–	–	–	–	–	–
1040H	–	–	–	–	–	–	–	–
1038H	–	–	–	–	–	–	–	–
1030H	–	–	–	–	–	–	–	–
1028H	FEARH	FEARM	FEARL	FEDR	FETR	–	–	–
1020H	FEMR	FECR	FESR	FETCR	FEARM1	FEARL1	–	–
1018H	UCTRL4	FPCR	RTOCH	RTOCL	–	–	–	–
1010H	WDTC	WDTSR	WDTCNTH	WDTCNTL	–	–	–	–
1008H	–	–	–	–	–	–	–	–
1000H	–	–	–	–	–	–	–	–

5.4.2 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	1	0	0	0	1	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	0	0	1	1	1
8EH	Watch Dog Timer Identification Register	WDTIDR	W	0	0	0	0	0	0	0	0
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	P4 Open-drain Selection Register	P4OD	R/W	0	0	0	0	0	0	0	0
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	0	0	0	0	0	0	1
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	0	0	0	0	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	–	–	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0
BBH	Timer 1 Counter High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1
D9H	Timer 1 C Data Low Register	T1CDRL	R/W	1	1	1	1	1	1	1	1
DAH	Timer 1 C Data High Register	T1CDRH	R/W	1	1	1	1	1	1	1	1
DBH	Timer 1 D Data Low Register	T1DDRL	R/W	1	1	1	1	1	1	1	1
DCH	Timer 1 D Data High Register	T1DDRH	R/W	1	1	1	1	1	1	1	1

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	0	0	0	0	0	0	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	0	1	0	1	0	0	0
CBH	USART Control Register 1	UCTRL1	R/W	0	0	0	0	0	0	0	0
CCH	USART Control Register 2	UCTRL2	R/W	0	0	0	0	0	0	0	0
CDH	USART Control Register 3	UCTRL3	R/W	0	0	0	0	–	0	0	0
CFH	USART Status Register	USTAT	R/W	1	0	0	0	0	0	0	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D2H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
D3H	P0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
D5H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
D6H	P2 Function Selection Register	P2FSR	R/W	–	–	–	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	–	–	–	0	0	0	0	0
DFH	P1/P5 De-bounce Enable Register	P15DB	R/W	–	–	0	0	0	0	0	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	I2C Mode Control Register	I2CMR	R/W	0	0	0	0	0	0	0	0
E2H	I2C Status Register	I2CSR	R	0	0	0	0	0	0	0	0
E3H	SCL Low Period Register	I2CSCLLR	R/W	0	0	1	1	1	1	1	1
E4H	SCL High Period Register	I2CSCLHR	R/W	0	0	1	1	1	1	1	1
E5H	SDA Hold Time Register	I2CSDAHR	R/W	0	0	0	0	0	0	0	1
E6H	I2C Data Register	I2CDR	R/W	1	1	1	1	1	1	1	1
E9H	I2C Slave Address Register	I2CSAR	R/W	0	0	0	0	0	0	0	0
EAH	I2C Slave Address Register 1	I2CSAR1	R/W	0	0	0	0	0	0	0	0
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
FCH	USART Baud Rate Generation Register	UBAUD	R/W	1	1	1	1	1	1	1	1
FDH	USART Data Register	UDATA	R/W	0	0	0	0	0	0	0	0

Table 7. XSFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1010H	Watch Dog Timer Clear Register	WDTC	R/W	0	0	0	0	0	0	0	0
1011H	Watch Dog Timer Status Register	WDTSR	R/W	0	0	0	0	0	0	0	0
1012H	Watch Dog Timer Count H Register	WDTCNTH	R	0	0	0	0	0	0	0	0
1013H	Watch Dog Timer Count L Register	WDTCNTL	R	0	0	0	0	0	0	0	0
1018H	USART Control Register 4	UCTRL4	R/W	–	–	–	0	0	0	0	0
1019H	USART Floating Point Counter	FPCR	R/W	0	0	0	0	0	0	0	0
101AH	Receiver Time Out Counter High Register	RTOCH	R	0	0	0	0	0	0	0	0
101BH	Receiver Time Out Counter Low Register	RTOCL	R	0	0	0	0	0	0	0	0
1020H	Flash Mode Register	FEMR	R/W	0	–	0	0	0	0	0	0
1021H	Flash Control Register	FECR	R/W	0	–	0	0	0	0	1	1
1022H	Flash Status Register	FESR	R/W	1	–	–	–	0	0	0	0
1023H	Flash Time Control Register	FETCR	R/W	0	0	0	0	0	0	0	0
1024H	Flash Address Middle Register 1	FEARM1	R/W	0	0	0	0	0	0	0	0
1025H	Flash Address Low Register 1	FEARL1	R/W	0	0	0	0	0	0	0	0
1028H	Flash Address High Register	FEARH	R/W	0	0	0	0	0	0	0	0
1029H	Flash Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
102AH	Flash Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0

6 I/O ports

A96G174/A96S174 has 3 groups of I/O ports (P0 ~ P2). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. P0 includes a function that can generate interrupt signals according to state of a pin.

6.1 P0 port

6.1.1 P0 port description

P0 is an 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

6.2 P1 port

6.2.1 P1 port description

P1 is an 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P1DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

6.3 P2 port

6.3.1 P2 port description

P2 is an 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) andP2 open-drain selection register (P2OD).Refer to the port function selection registers for the P2 function selection.

7 Interrupt controller

A96G174/A96S174 supports up to 14 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. In addition, they have four levels of priority assigned to themselves.

A non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources, and is not controllable by software.

Interrupt controller of A96G174/A96S174 has following features:

- Request receive from the 14 interrupt sources
- 2 groups of priority
- 4 levels of priority
- Multi Interrupt possibility
- A request of higher priority level is served first, when multiple requests of different priority levels are received simultaneously.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency of 3 to 9 machine cycles in single interrupt system

A non-maskable interrupt is always enabled, while maskable interrupts are enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The A96G174/A96S174 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Figure 15 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

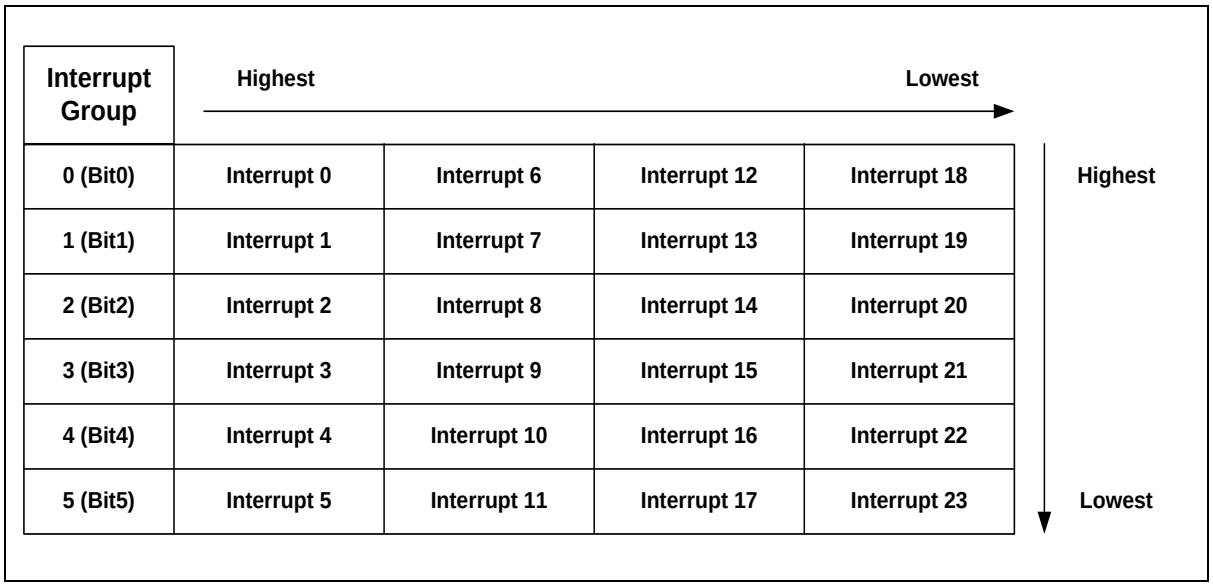
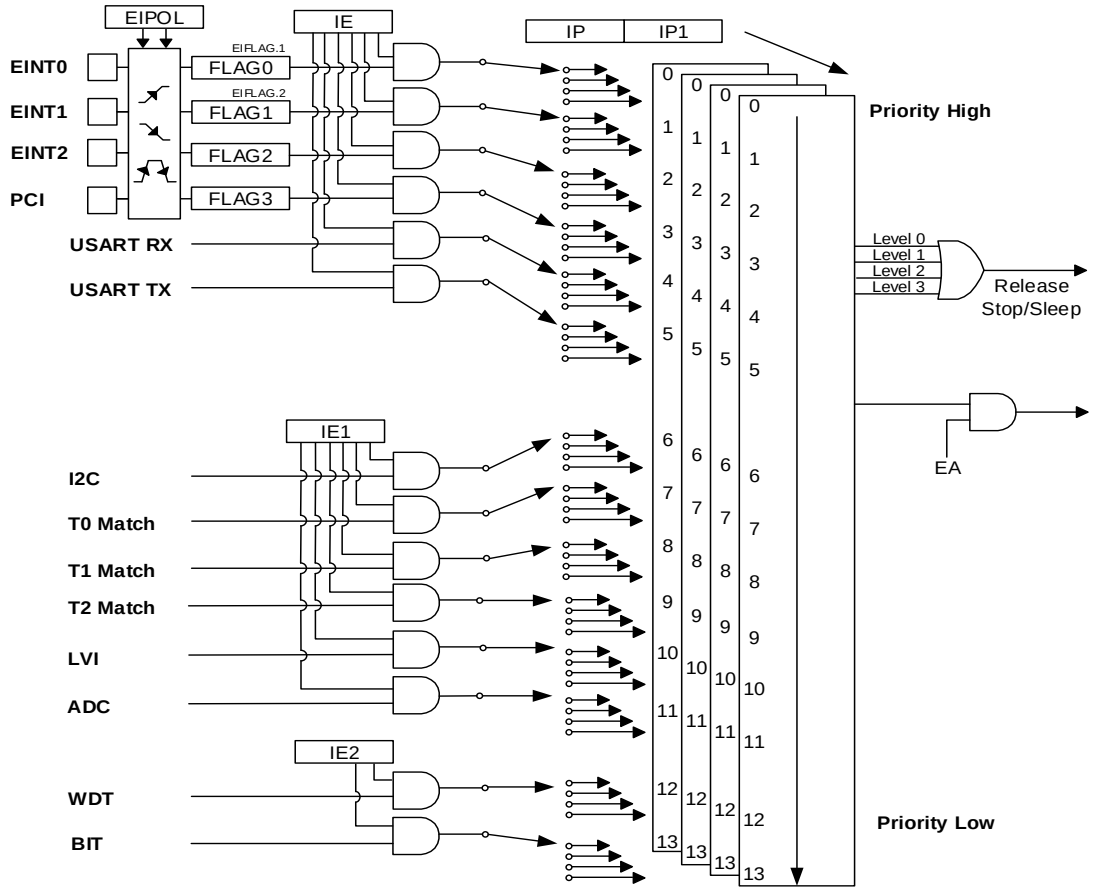


Figure 15. Interrupt Group Priority Level

7.1 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

Figure 16. Interrupt Controller Block Diagram

7.2 Interrupt vector table

Interrupt controller of A96G174/A96S174 supports 14 interrupt sources as shown in Table 8. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 8. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt enable bit	Priority	Mask	Vector address
Hardware Reset	RESETB	-	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
External Interrupt 2	INT2	IE.2	3	Maskable	0013H
PCI Interrupt	INT3	IE.3	4	Maskable	001BH
USART Rx Interrupt	INT4	IE.4	5	Maskable	0023H
USART Tx Interrupt	INT5	IE.5	6	Maskable	002BH
I2C Interrupt	INT6	IE1.0	7	Maskable	0033H
T0 Match Interrupt	INT7	IE1.1	8	Maskable	003BH
T1 Match Interrupt	INT8	IE1.2	9	Maskable	0043H
T2 Match Interrupt	INT9	IE1.3	10	Maskable	004BH
LVI Interrupt	INT10	IE1.4	11	Maskable	0053H
ADC Interrupt	INT11	IE1.5	12	Maskable	005BH
WDT Interrupt	INT12	IE2.0	13	Maskable	0063H
BIT Interrupt	INT13	IE2.1	14	Maskable	006BH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

8 Clock generator

As shown in Figure 17, a clock generator produces basic clock pulses which provide a system clock for CPU and peripheral hardware.

Default system clock is 16MHz INT-RC Oscillator. To stabilize the system internally, 128kHz LOW INT-RC oscillator on POR is recommended.

Oscillators in the clock generator are introduced in the followings:

- Calibrated high internal RC oscillator (32MHz)
  - HSIRC OSC/2 (16MHz, default system clock)
  - HSIRC OSC/4 (8MHz)
  - HSIRC OSC/8 (4MHz)
  - HSIRC OSC/16 (2MHz)
  - HSIRC OSC/32 (1MHz)
  - HSIRC OSC/64 (0.5MHz)
- Internal LSIRC oscillator (128kHz)

8.1 Clock generator block diagram

In this section, a clock generator of A96G174/A96S174 is described in a block diagram.

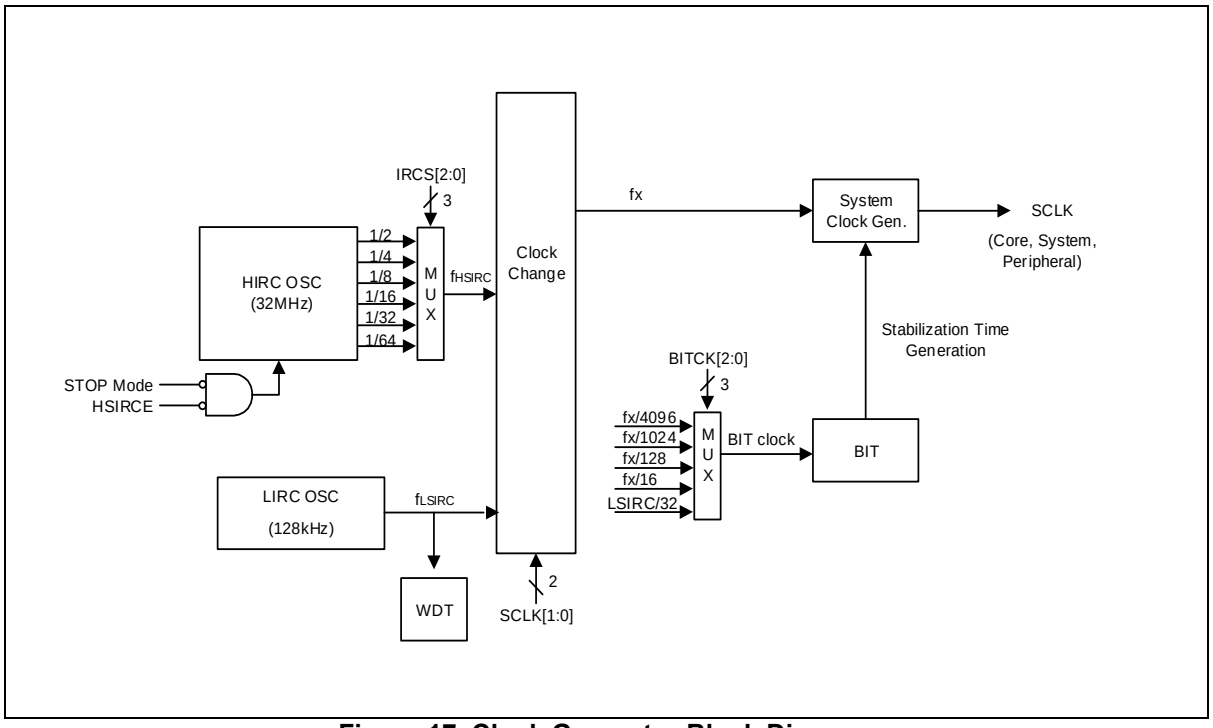


Figure 17. Clock Generator Block Diagram

9 Basic interval timer

A96G174/A96S174 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting, and provides a basic interval timer interrupt (BITIFR).

BIT of A96G174/A96S174 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

9.1 BIT block diagram

In this section, basic interval timer of A96G174/A96S174 is described in a block diagram.

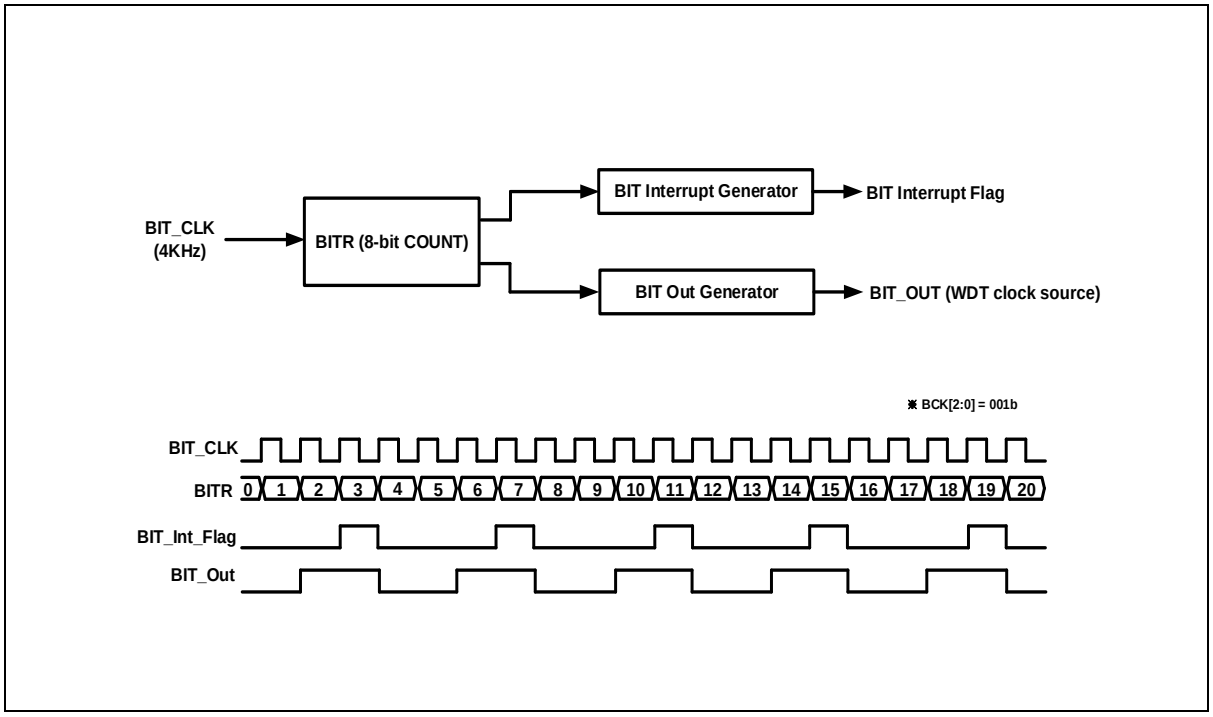


Figure 18. Basic Interval Timer Block Diagram

10 Watchdog timer

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. When 75% of the overflow time is reached, a watchdog interrupt can be generated. The overflow time of the watchdog timer can select by WDTOVF[2:0] of WDTCR. If an overflow occurs, an internal reset is generated. The WDTRC operation in the STOP/IDLE mode differs as follows depending on the setting value of WDTPDON. If WDTPDON = 0, the WDTRC operation stop in the STOP/IDLE mode and if WDTPDON = 1, the WDTRC operation in the STOP/IDLE mode. The watchdog timer operate on the 4kHz, based on clock 128kHz Ring oscillator clock.

Watchdog reset is occurred in the following cases:

- When the watchdog timer counter overflows
- When the data except “96H” is written to the WDTC register
- When the data “96H” is written to the WDTC register during a window close period

10.1 WDT block diagram

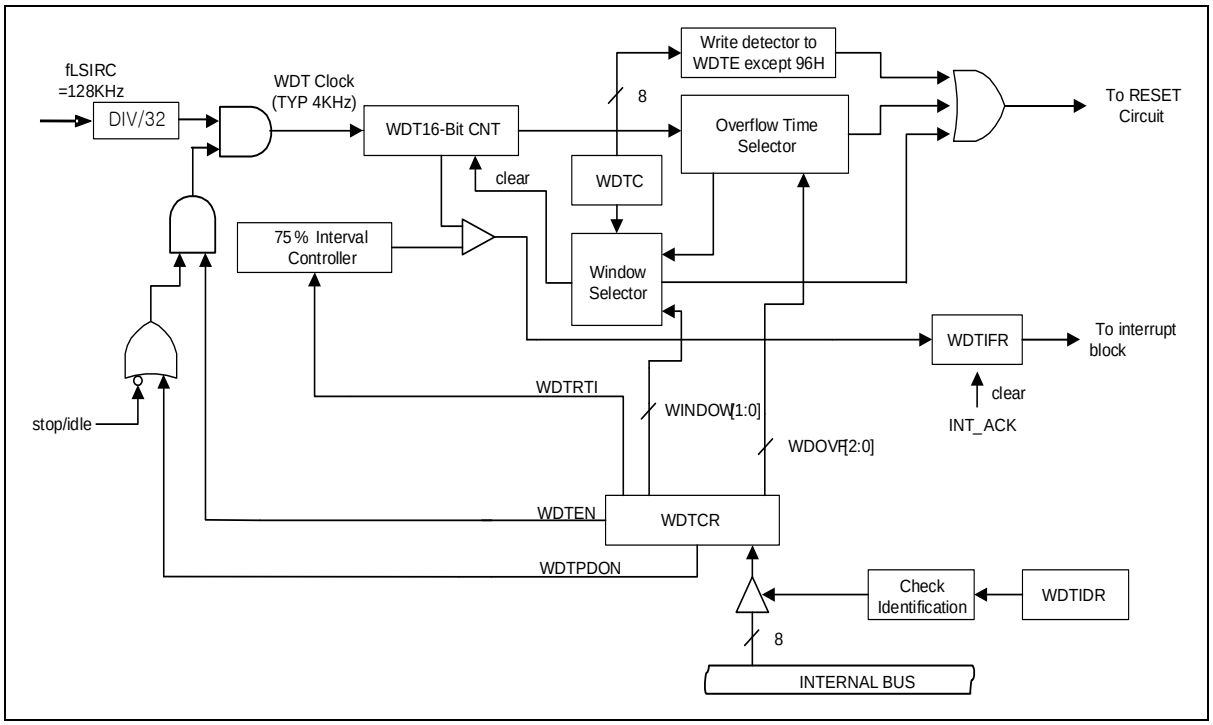


Figure 19. Watch Dog Timer Block Diagram

11 Timer 0/1/2

11.1 Timer 0

An 8-bit timer 0 consists of a multiplexer, a timer 0 counter register, a timer 0 data register, a timer 0 capture data register and a timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

Timer 0 operates in one of three modes introduced in the followings:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

Timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by clock selection bits T0CK[2:0].

- TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048 and EC0

In capture mode, data is captured into input capture data register (T0CDR) by EINT10. In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. In addition, timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 9. Timer 0 Operating Mode

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

11.1.1 Timer 0 block diagram

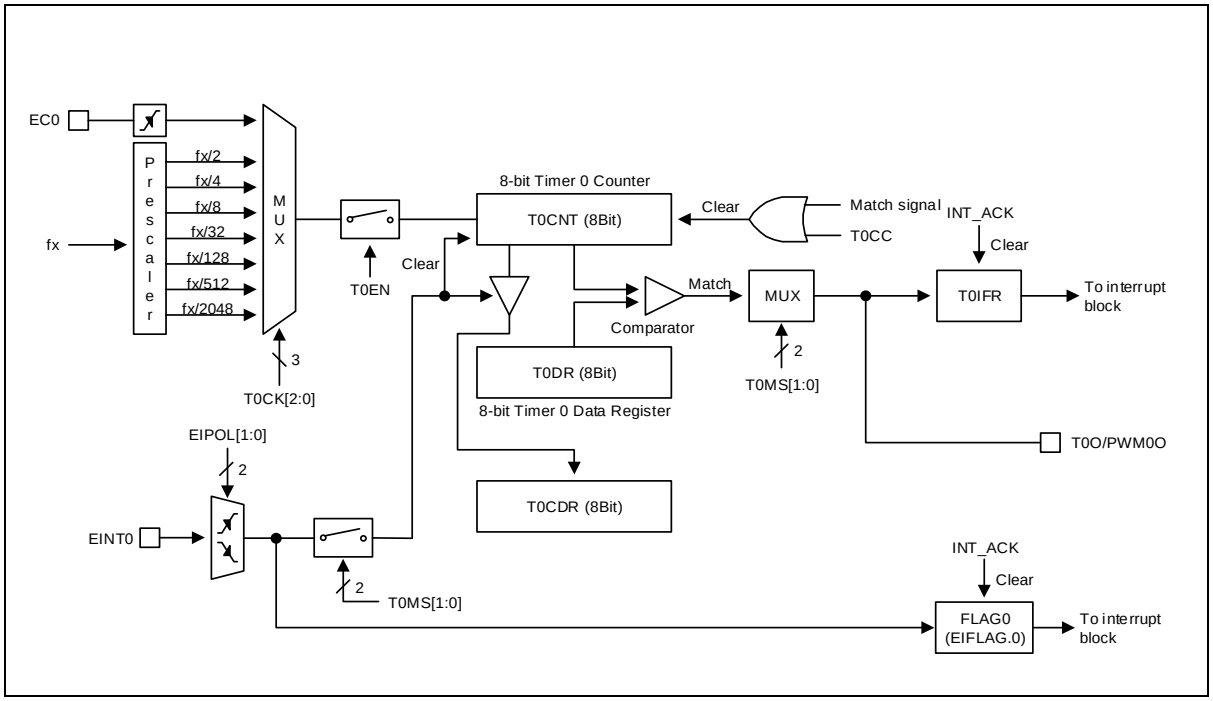


Figure 20. 8-bit Timer 0 Block Diagram

11.2 Timer 1

A 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL, T1DRH, T1DRL).

Timer 1 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock source: fX/1, 2, 4, 8, 64, 2048, HFO and EC1

In capture mode, the data is captured into input capture data register (T1BDRH/T1BDRL) by EINT11. Timer 1 results in the comparison between counter and data register through T1O port in timer/counter mode. In addition, Timer 1 outputs PWM waveform through PWM1Oport in the PPG mode.

Table 10. TIMER 1 Operating Modes

T1EN	P1FSRL[5:4]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

11.2.1 16-bit timer 1 block diagram

In this section, a 16-bit timer 1 is described in a block diagram.

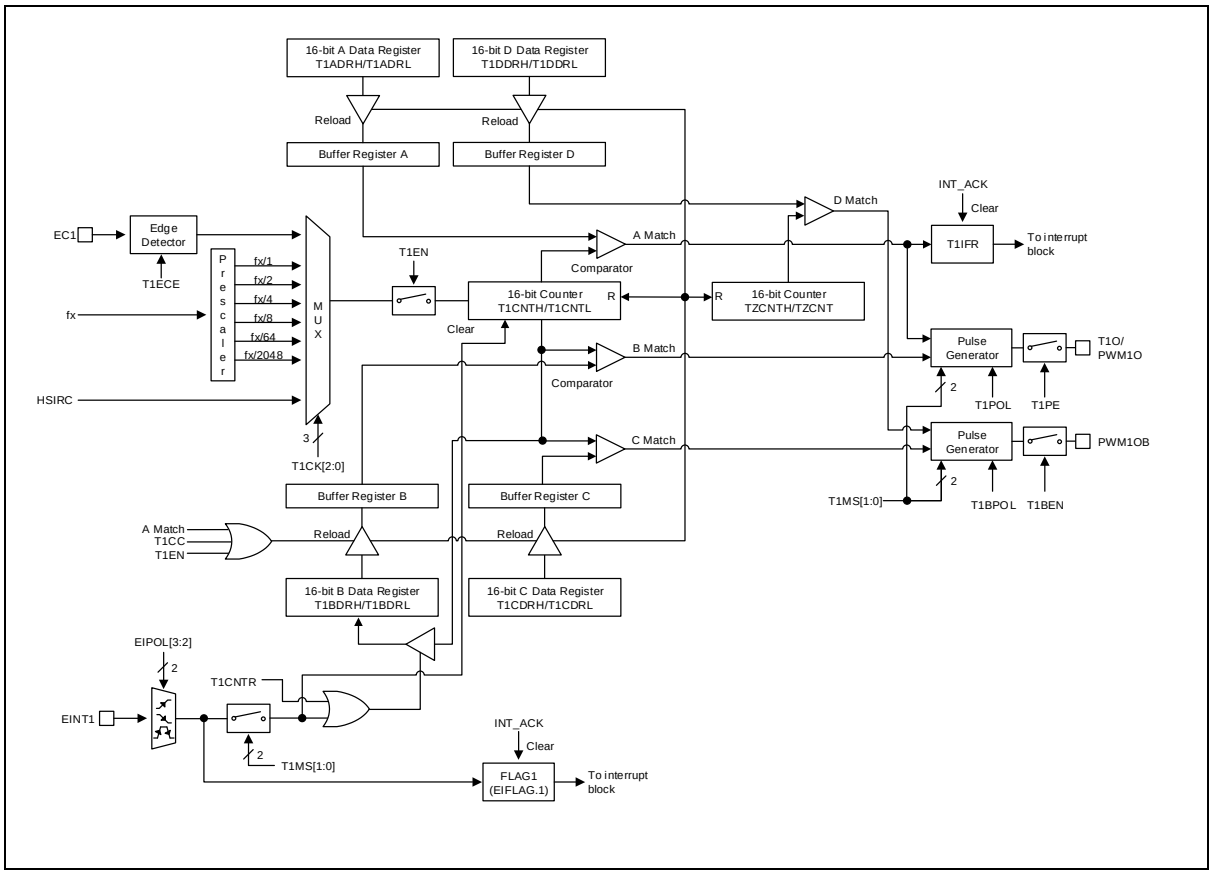


Figure 21. 16-bit Timer 1 Block Diagram

11.3 Timer 2

A 16-bit timer 2 consists of a multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

Timer 2 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be a divided clock of a system clock which is selected from prescaler output and T1 A Match (timer 1 A match signal). The clock source is selected by a clock selection logic, controlled by clock selection bits (T2CK[2:0]).

- TIMER 2 clock source: fX/1, fX/2, fX/4,fX/8,fX/32, fX/128, fX/512 and T1 A Match

In capture mode, data is captured into input capture data registers (T2BDRH/T2BDRL) by EINT12. In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. In addition, the timer 2 outputs PWM waveform to PWM2O port in the PPG mode.

Table 11. TIMER 2 Operating Modes

T2EN	P1FSRL[3:2]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode

1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

11.3.1 16-bit timer 2 block diagram

In this section, a 16-bit timer 2 is described in a block diagram.

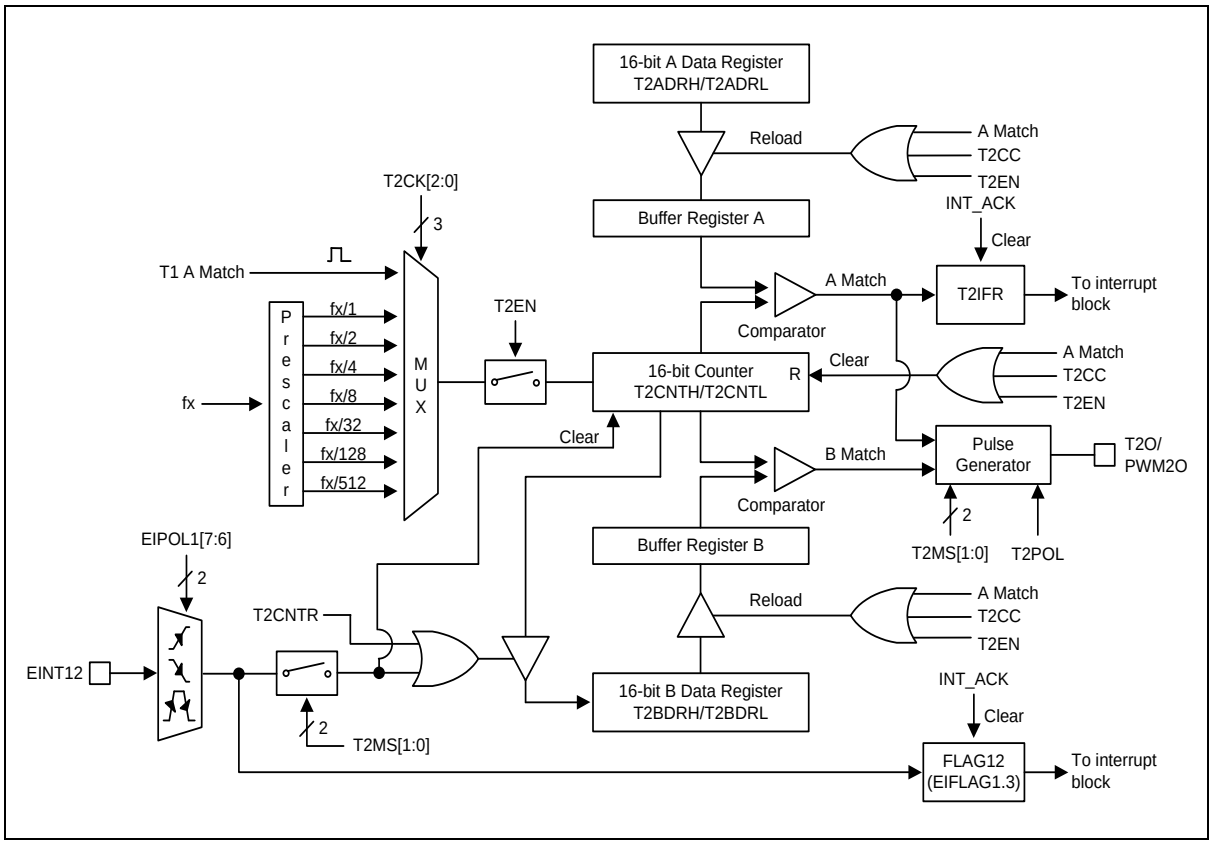


Figure 22. 16-bit Timer 2 Block Diagram

12 12-bit ADC

Analog-to-digital converter (ADC) of A96G174/A96S174 allows conversion of an analog input signal to corresponding 12-bit digital value. This A/D module has eight analog inputs. Output of the multiplexer becomes input into the converter which generates the result through successive approximation.

The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL).

ADSEL[3:0] bits are used to select channels to be converted. To execute A/D conversion, TRIG[2:0] bits should be set to ‘xxx’. Registers ADCDRH and ADCDRL contain the result of A/D conversion. When the conversion is completed, the result is loaded into ADCDRH and ADCDRL, A/D conversion status bit AFLAG is set to ‘1’, and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as ‘0’.

12.1 Block diagram

In this section, the 12-bit ADC is described in a block diagram, and an analog input pin and a power pin with capacitors respectively are introduced.

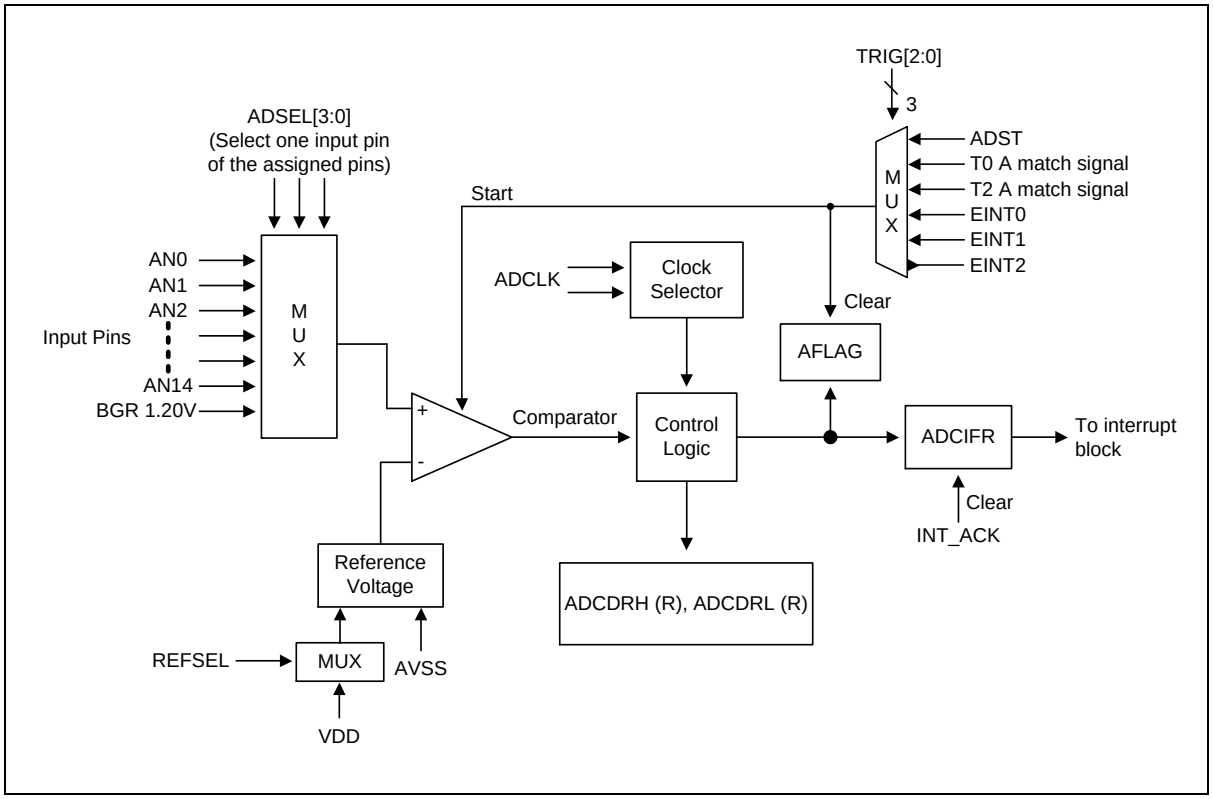


Figure 23. 12-bit ADC Block Diagram

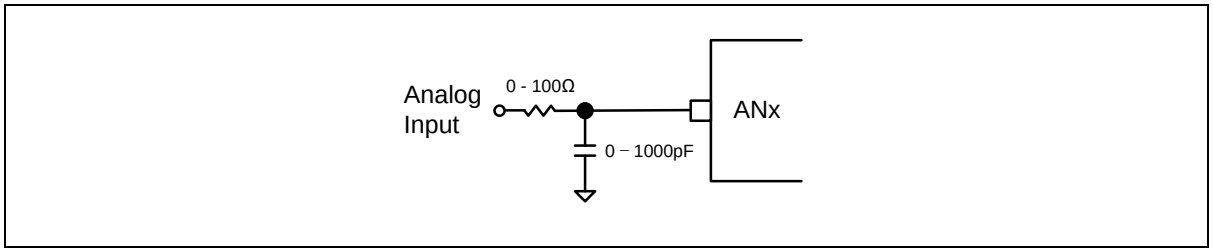


Figure 24. A/D Analog Input Pin with a Capacitor

13 I2C

The I²C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below. Asynchronous mode (UART)

- Compatible with I²C bus standard
- Multi-master operation
- Up to 400kHz data transfer speed
- 7 bit address
- Support 2 slave addresses
- Both master and slave operation
- Bus busy detection

13.1 Block diagram

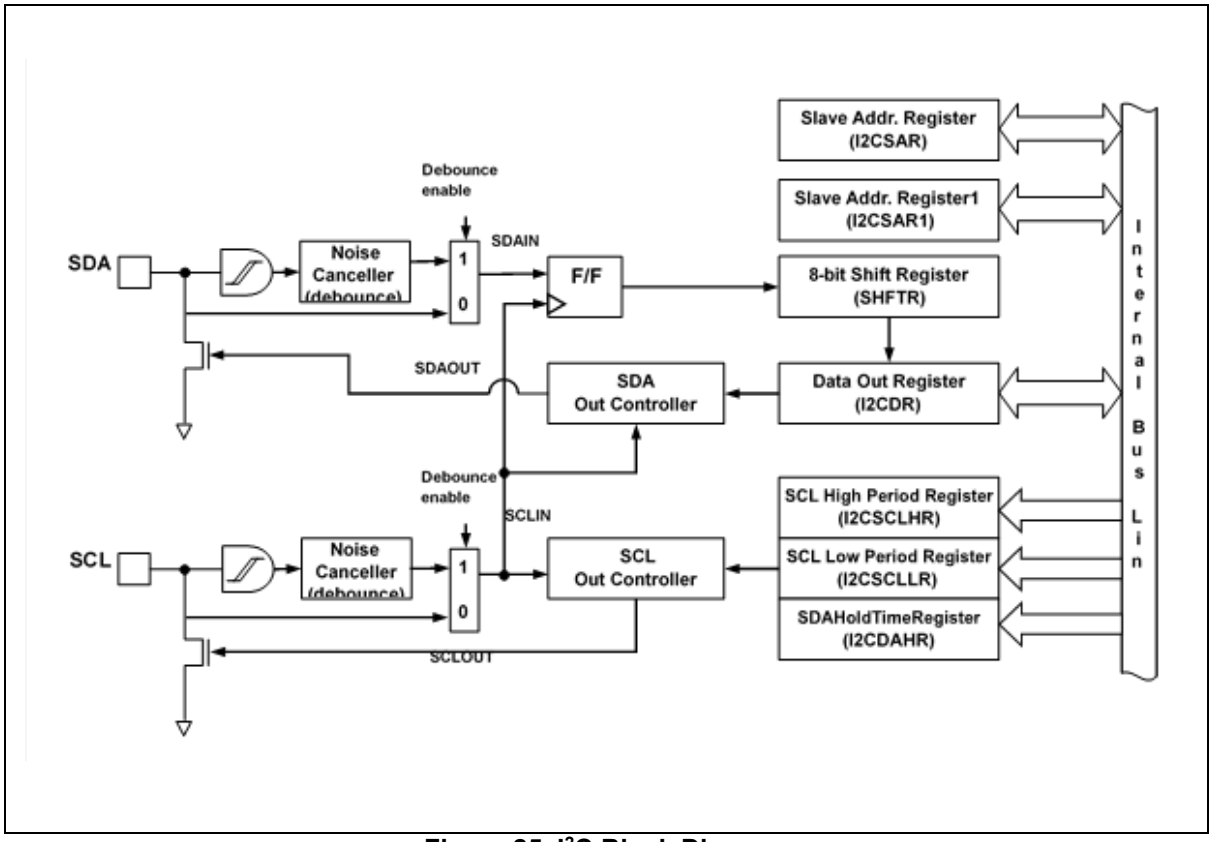


Figure 25. I²C Block Diagram

14 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. USART of A96G174/A96S174 features the followings:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

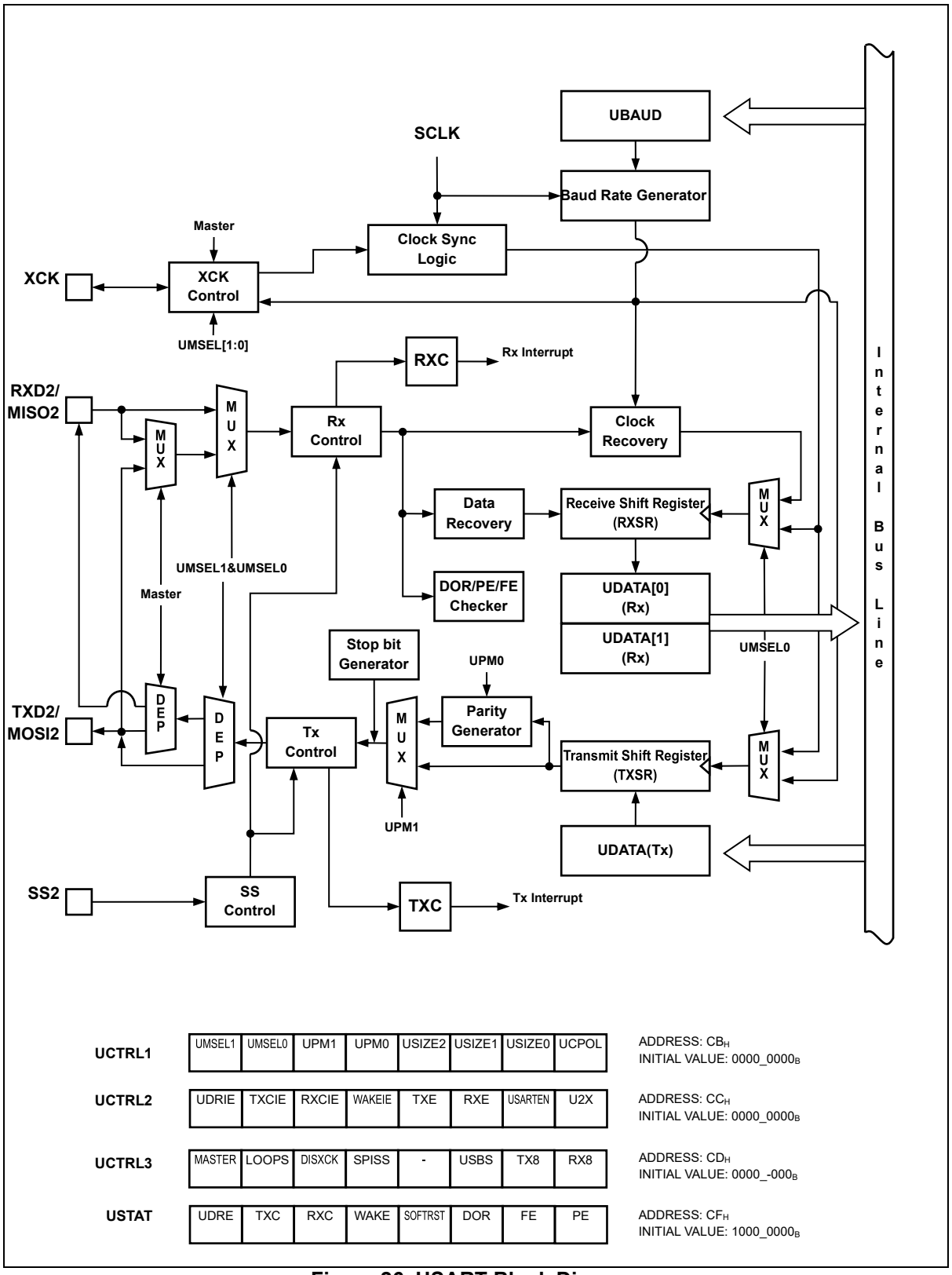
USART has three main parts such as a Clock Generator, Transmitter and Receiver.

Clock Generation logic consists of a synchronization logic for external clock input used by synchronous or SPI slave operation, and a baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

Receiver is the most complex part of the USART module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, the Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATA) and control logic. The Receiver supports the same frame formats as the Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

14.1 Block diagram



UCTRL1	UMSEL1	UMSEL0	UPM1	UPM0	USIZE2	USIZE1	USIZE0	UCPOL	ADDRESS: CB_H INITIAL VALUE: 0000_0000_B
UCTRL2	UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	USARTEN	U2X	ADDRESS: CC_H INITIAL VALUE: 0000_0000_B
UCTRL3	MASTER	LOOPS	DISXCK	SPISS	-	USBS	TX8	RX8	ADDRESS: CD_H INITIAL VALUE: 0000_-000_B
USTAT	UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE	ADDRESS: CF_H INITIAL VALUE: 1000_0000_B

Figure 26. USART Block Diagram

15 Power down operation

A96G174/A96S174 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. A96G174/A96S174 provides three kinds of power saving functions such as Main-IDLE mode, Sub-IDLE mode and STOP mode. During one of these three modes, program will be stopped.

15.1 Peripheral operation in IDLE/ STOP mode

Table 12 shows operation status of each peripheral in IDLE mode and STOP mode.

Table 12. Peripheral Operation Status during Power-down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU operations are disabled.	ALL CPU operations are disabled.
RAM	Retains.	Retains.
Basic Interval Timer	Operates continuously.	Stops (can be operated with WDTRC OSC).
Watch Dog Timer	Operates continuously.	Stops (can be operated with WDTRC OSC).
Timer0~2	Operates continuously.	Halts (only when the event counter mode is enabled, timer operates normally).
ADC	Operates continuously.	Stops.
Internal OSC (32MHz)	Oscillates.	Stops when the system clock (fx) is fHSIRC.
WDTRC OSC (128kHz)	Can be operated with setting value.	Can be operated programmable.
I/O Port	Retains.	Retains.
Control Register	Retains.	Retains.
Address Data Bus	Retains.	Retains.
Release Method	By RESET All Interrupts	By RESET Timer Interrupt (EC0, EC1, EC3) External Interrupt USART by RX, WT (sub clock), WDT USI0/1 by RX, I2C(Slave mode)

16 Reset

Table 13 shows hardware setting values of main peripherals.

Table 13. Hardware Setting Values in Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

A96G174/A96S174 has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

16.1 Reset block diagram

In this section, reset unit is described in a block diagram.

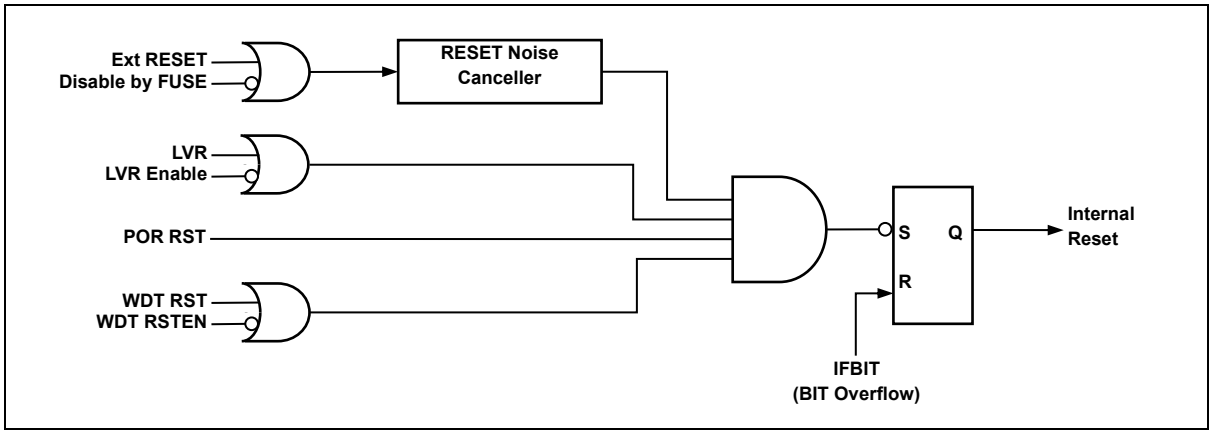


Figure 27. Reset Block Diagram

17 Memory programming

A96G174/A96S174 has flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

Flash of A96G174/A96S174 features the followings:

- Flash Size : 8Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 30,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

17.1 Memory map

17.1.1 Flash memory map

Program memory uses 8K bytes of flash memory. It is read by byte and written by byte or page. One page is 32-bytes

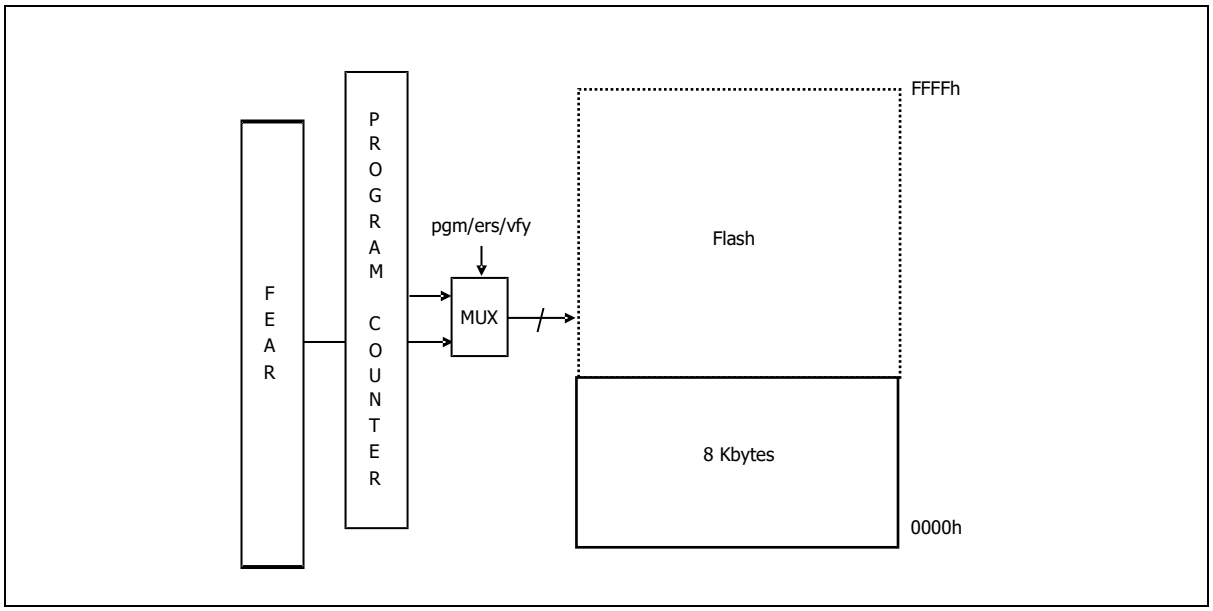


Figure 28. Flash Memory Map

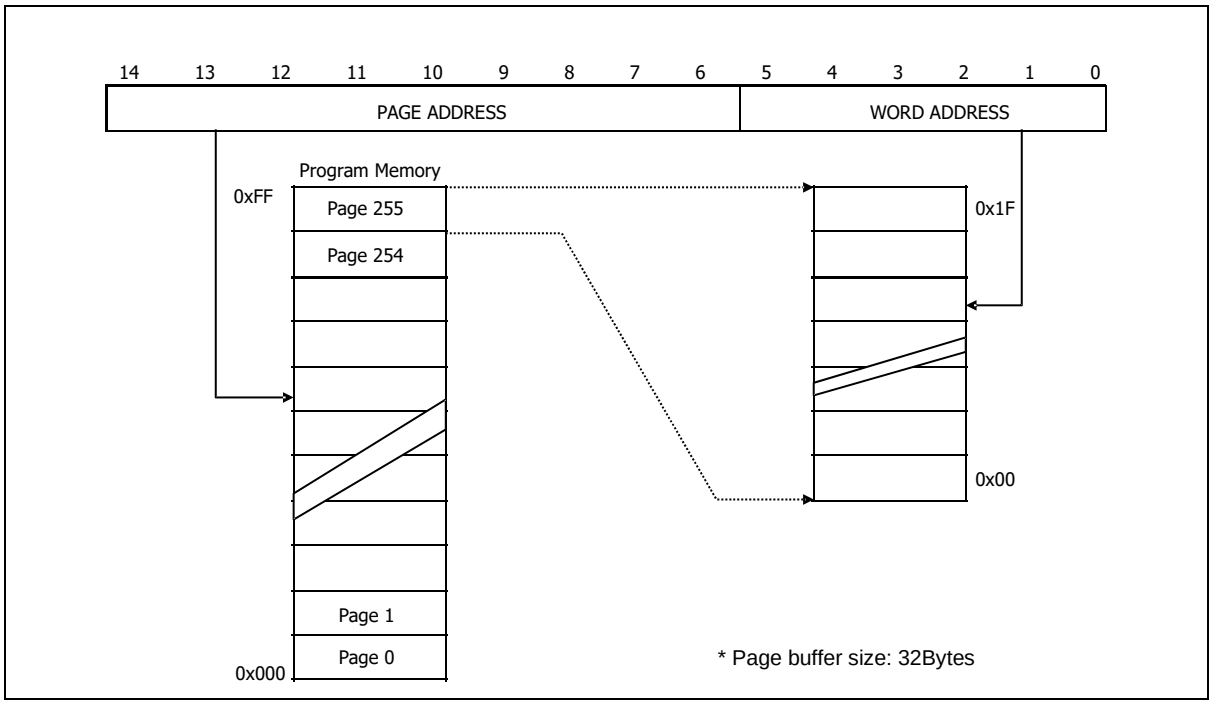


Figure 29. Address Configuration of Flash Memory

18 Electrical characteristics

18.1 Absolute maximum ratings

Table 14. Absolute Maximum Ratings

Parameter	Symbol	Rating NOTE2	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	80	mA	Maximum current (I_{OL} per I/O pin)
	$\sum I_{OL}$	100	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

NOTE:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The measured value for the parameters and conditions listed were confirmed by simulation.

18.2 Recommended operating conditions

Table 15. Recommended Operating Conditions

(T_A=-40°C ~ 85°C or T_A=-40°C ~ 105°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 0.5 ~16MHz	Internal RC	1.8	–	5.5	V
Operating Temperature	T_{OPR}	VDD=1.8~5.5V		-40	–	85	°C
				-40	–	105	

18.3 A/D converter characteristics

Table 16. A/D Converter Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Integral Linear Error	ILE	AVDD = 5.0V MCLK = 8MHz		–	±4	±8	LSB
Differential Linearity Error	DLE			–	±1	±2	
Offset Error of Top	EOT			–	±4	±8	
Offset Error of Bottom	EOB			–	±2	±4	
Conversion Time	t_{CON}	12-bit resolution, 8MHz		7.5	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	VDD	V
Analog Input Leakage Current	I_{AN}	VDDREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC} NOTE6	Enable	VDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

NOTES:

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (VDD).
3. When VDD is lower than 2.2V, the ADC resolution will get worse.
4. If VDD is less than or equal to 2.2V, the resolution degrades by 1-bit whenever VDD drops 0.1V. (@ADCLK = 0.5MHz, under 2.2V, resolution has no test.)
5. ADCLK must be less than 0.5MHz. Furthermore, if ADCLK is less than 0.125MHz, it can be improved INL characteristic.
6. The measured value for the parameters and conditions listed were confirmed by simulation.

Table 17. Recommended ADC Resolution

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

VDD [V]	Resolution	Conditions
2.6	12-bit / Upper 12-bit	ADCLK ≤ 0.5MHz
2.5	12-bit / Upper 12-bit	
2.4	12-bit / Upper 12-bit	
2.3	12-bit / Upper 12-bit	
2.2	11-bit / Upper 11-bit	
2.1	10-bit / Upper 10-bit	
2.0	9-bit / Upper 9-bit	
1.9	8-bit / Upper 8-bit	
1.8	7-bit / Upper 7-bit	

NOTE: Guaranteed by design.

18.4 BGR Characteristics

Table 18. BGR Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
BGR Reference Voltage	V_{BGR}	T_A=+25°C	1.164	1.200	1.236	V
		T_A=-40°C ~ 85°C	1.146	1.200	1.254	
		T_A=-40°C ~ 105°C	1.140	1.200	1.260	

18.5 Power on reset characteristics

Table 19. Power-on Reset Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR} NOTE	–	–	1.32	–	V
VDD Voltage Rising Time	t_R NOTE	–	0.05	–	50.0	V/ms
Minimum Pulse Width	t_{LW} NOTE	–	100	–	–	us
POR Current	I_{POR} NOTE	–	–	0.2	–	uA

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

18.6 Low voltage reset and low voltage indicator characteristics

Table 20. LVR and LVI Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels. But LVI can select other levels except 1.61V because the minimum operating voltage is 1.8V. V_{LVR}/V_{LVI} can be measured when voltage drops (falling level).		–	1.61	1.75	V
				1.63	1.77	1.91	
				1.96	2.13	2.30	
				2.26	2.46	2.66	
				3.28	3.56	3.84	
Hysteresis	△V	–		–	20	180	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

NOTE: Guaranteed by design.

18.7 High internal RC oscillator characteristics

Table 21. High Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 1.8 – 5.5V		–	32	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -10°C to +70°C				±2.0	
		T_A = -40°C to +85°C				±2.5	
		T_A = -40°C to +105°C				±5.0	
Clock Duty Ratio	TOD NOTE2	–		40	50	60	%
Stabilization Time	T_{HFS} NOTE2	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

NOTE:

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.
2. The measured value for the parameters and conditions listed were confirmed by simulation.

18.8 Low internal RC oscillator characteristics

Table 22. Internal WDTRC Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{LSIRC}	T_A=-40°C ~ +85°C	102	128	154	kHz
		T_A=-40°C ~ +105°C	90	128	166	
Stabilization Time	T_{LSIRC} NOTE	–	–	–	1	ms
LSIRC Current	I_{LSIRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

18.9 DC characteristics

Table 23. DC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0, P1,P5, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1,P5, RESETB		–	–	0.3VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.2VDD	V
Output High Voltage	V_{OH1}	VDD=4.5V, I_{OH}=-8.57mA, All output ports;		VDD-1.0	–	–	V
	V_{OH2}	VDD=4.5V, I_{OH}= -19 mA, All output ports;		VDD-2.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 10mA; All output ports except V_{OL2}		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
Supply Current	I_{DD1} (RUN)	f_{XIN}= 16MHz, VDD= 5V		0.7	2	4.0	mA
		f_{XIN}= 128kHz, VDD= 3V		–	0.2	-	
	I_{DD2} (IDLE)	f_{XIN}= 16MHz, VDD= 5V		0.5	1.5	3.0	mA
		f_{XIN}= 128kHz, VDD= 3V		–	0.15	-	
		f_{HSIRC}= 16MHz, VDD= 5V		0.5	-	3.0	
	I_{DD3} (STOP)	STOP @ WDT off & LVR off, VDD= 5.5V, T_A= 25°C		–	2	7	uA
		STOP@ WDT off & LVR off, VDD= 3V, T_A= 25°C		–	1.5	–	
		STOP @ WDT on, VDD= 1.8V, T_A= 25°C		–	2	–	
		STOP @ WDT on, VDD= 5.5V, T_A= 25°C		–	3	22	

NOTES:

3. Where the f_{HSIRC} and f_{LSIRC} are an internal RC oscillator, and the fx is the selected system clock.
4. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
5. All supply current items include the current of the power-on reset (POR) block.

18.10 AC characteristics

Table 24. AC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RSL} NOTE	Input, VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{INTH} NOTE, t_{INTL} NOTE	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	tECWH NOTE, tECWL NOTE	ECn, VDD = 5V (n= 0, 1, 3)	200	–	–	
External Counter Transition Time	tREC NOTE, tFEC NOTE	ECn, VDD = 5V (n= 0, 1, 3)	20	–	–	

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

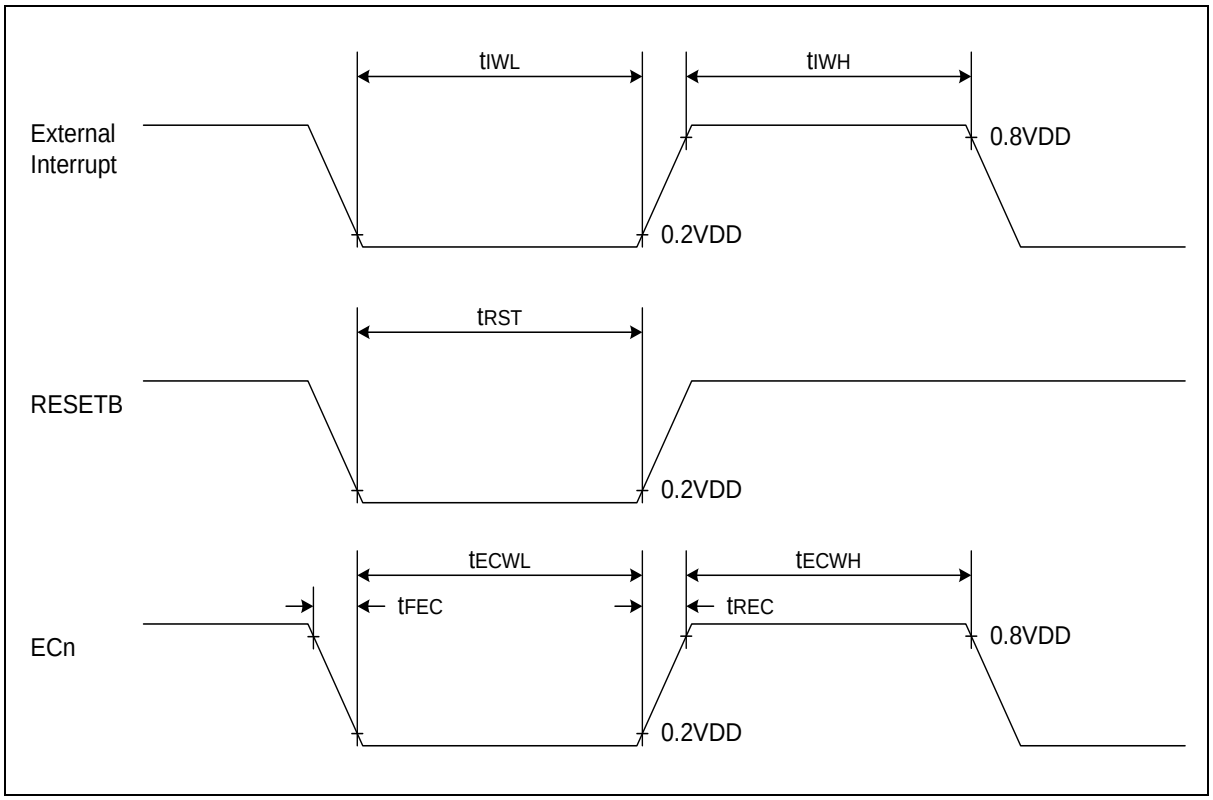


Figure 30. AC Timing

18.11 USART characteristics

The following table and figures show USART timing condition in SPI or Synchronous mode operation.

Table 25. USART Timing Characteristics in SYNC. or SPI Mode Operations

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter		Symbol	MIN	MAX	Unit
System clock period(0.5MHz~16MHz)		t_{SCLK}	62.5	2000	ns
Clock (XCK) period		t_{XCK}	4 x t_{SCLK}	1028 x t_{SCLK}	ns
Clock (XCK) high time		t_{XCKH}	2 x t_{SCLK}	514 x t_{SCLK}	ns
Clock (XCK) low time		t_{XCKL}	2 x t_{SCLK}	514 x t_{SCLK}	ns
Lead time	Master Slave	t_{LEAD} t_{LEAD}	0.5 x t_{XCK} 2 x t_{SCLK}	0.5 x t_{XCK} –	ns
Lag time	Master Slave	t_{LAG} t_{LAG}	0.5 x t_{XCK} 2 x t_{SCLK}	0.5 x t_{XCK} –	ns
Data setup time (inputs)	Master Slave	t_{SIM} t_{SIS}	2 x t_{SCLK} 2 x t_{SCLK}	2 x t_{SCLK} 2 x t_{SCLK}	ns
Data hold time (inputs)	Master Slave	t_{HIM} t_{HIS}	10 10	– –	ns
Data setup time (outputs)	Master Slave	t_{SOM} t_{SOS}	2 x t_{SCLK} 2 x t_{SCLK}	2 x t_{SCLK} 2 x t_{SCLK}	ns
Data hold time (outputs)	Master Slave	t_{HOM} t_{HOS}	-10 -10	– –	ns
Disable time		t_{DIS}	1 x t_{SCLK}	2 x t_{SCLK}	ns

NOTE:

1. In synchronous mode, Lead and Lag time for SS pin is ignored. And the case of “UCPHA=0” is also only applied to SPI mode
2. All timing is shown between 20% VDD and 80% VDD.

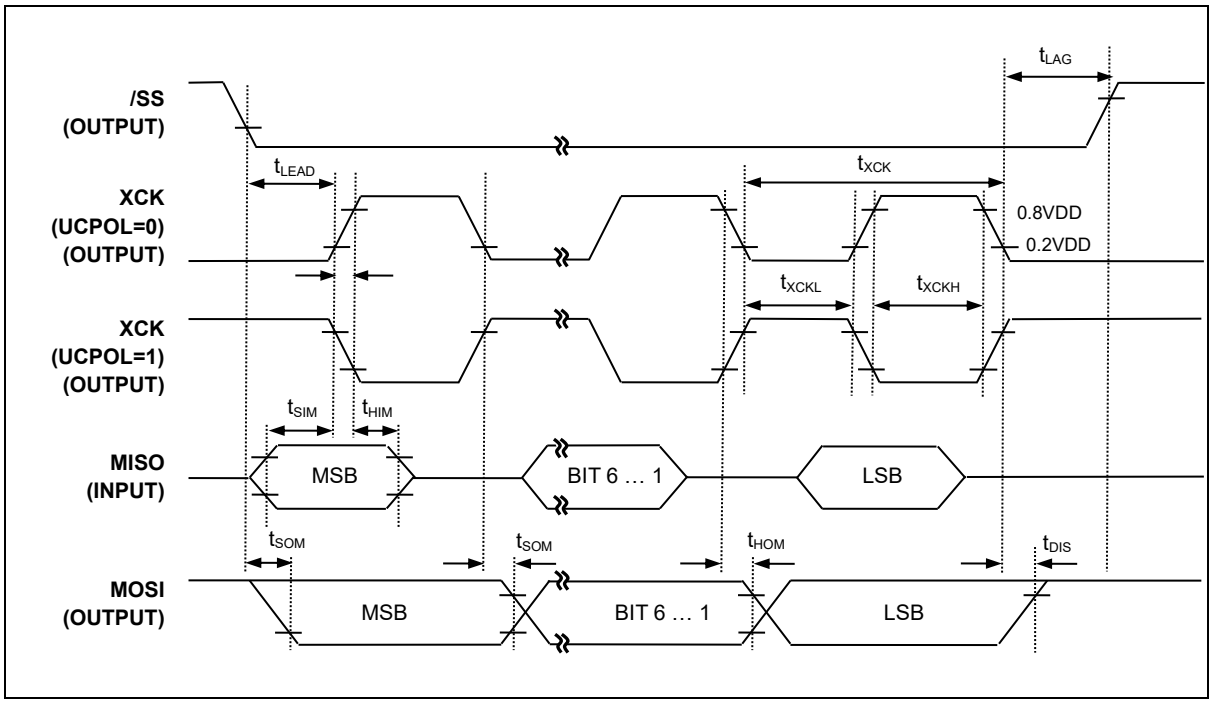
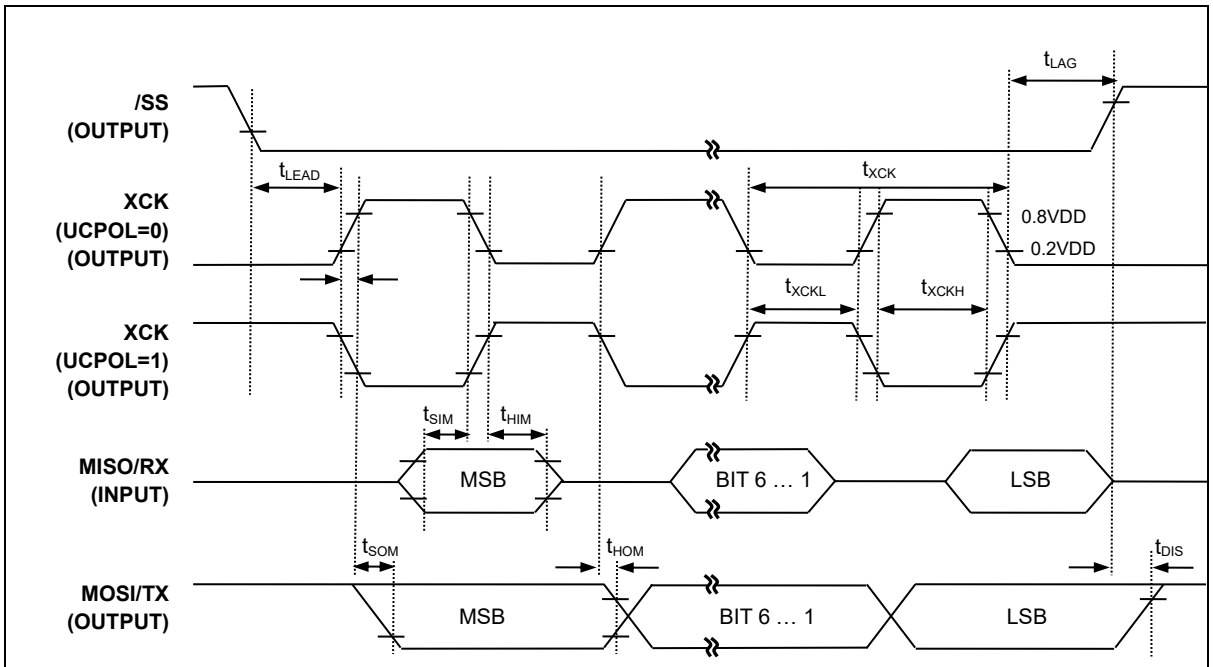


Figure 31. SPI master mode timing (UCPHA = 0, MSB first)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 32. SPI/Synchronous master mode timing (UCPHA = 1, MSB first)

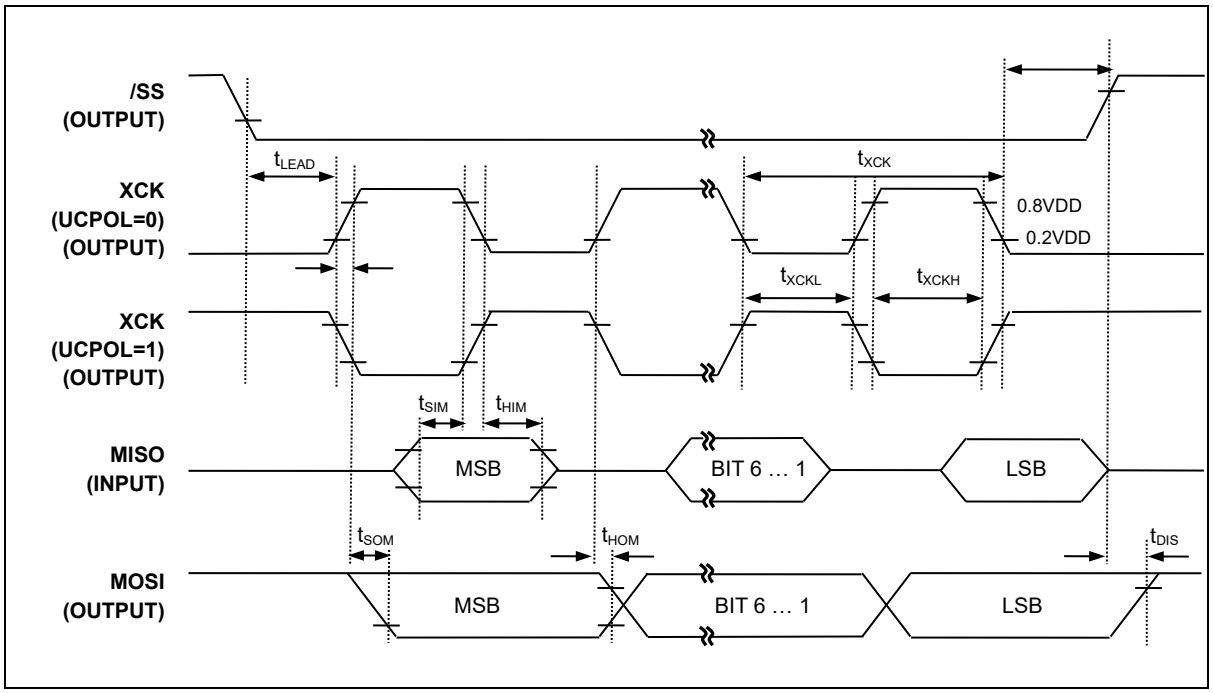
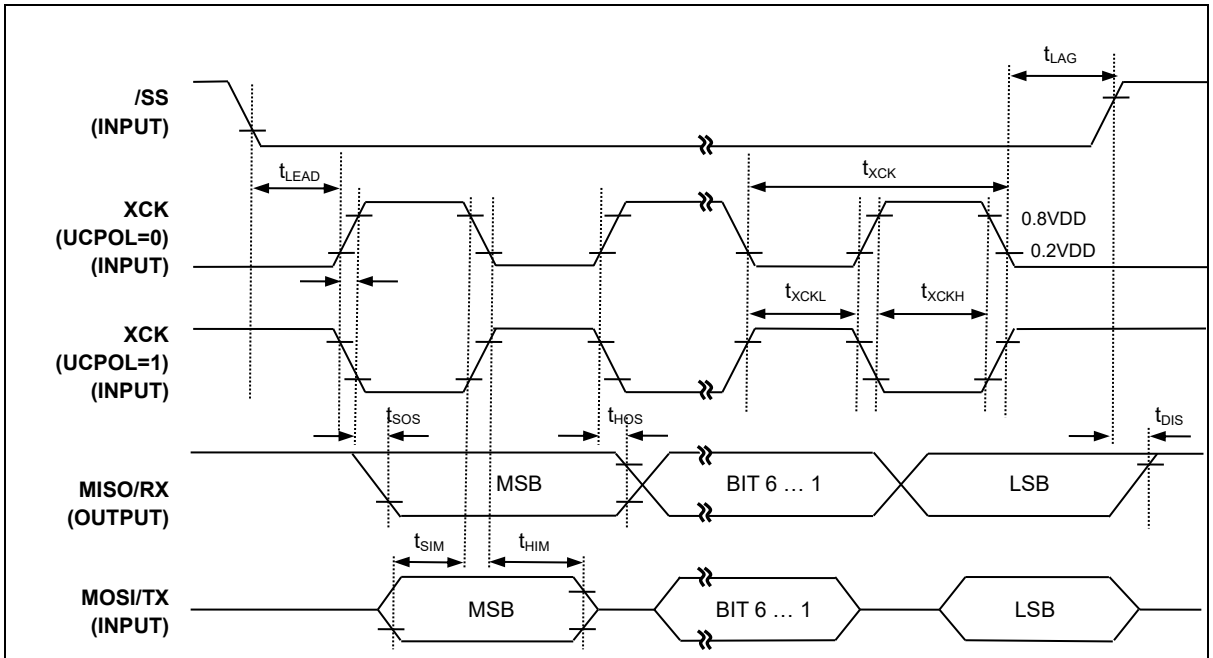


Figure 33 SPI slave mode timing (UCPHA = 0, MSB first)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 34 SPI/Synchronous slave mode timing (UCPHA = 1, MSB first)

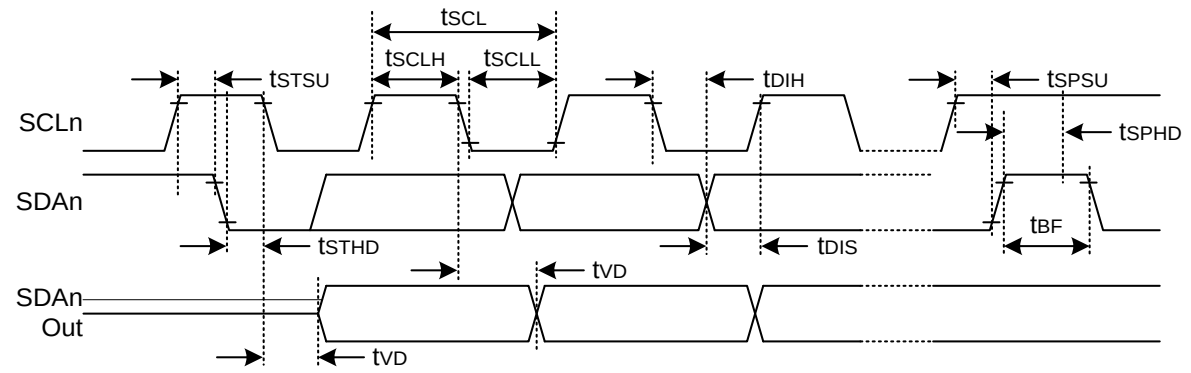
18.12 I2C characteristics

Table 26. I2C Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	tSCL[NOTE]	0	100	0	400	kHz
Clock High Pulse Width	tSCLH[NOTE]	4.0	–	0.6	–	us
Clock Low Pulse Width	tSCLL[NOTE]	4.7	–	1.3	–	
Bus Free Time	tBF[NOTE]	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU[NOTE]	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD[NOTE]	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU[NOTE]	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD[NOTE]	4.0	–	0.6	–	
Output Valid from Clock	tVD[NOTE]	0	–	0	–	
Data Input Hold Time	tDIH[NOTE]	0	–	0	1.0	
Data Input Setup Time	tDIS[NOTE]	250	–	100	–	ns

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.



NOTE: n= 0, and 1

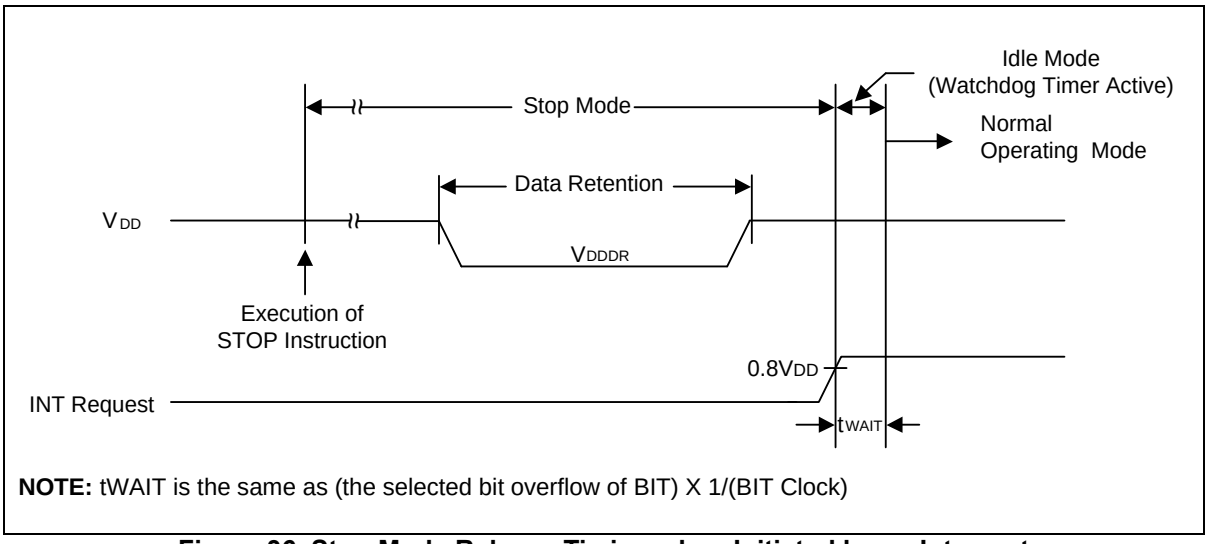
Figure 35. I2C Timing

18.13 Data retention voltage in stop mode

Table 27. Data Retention Voltage in Stop Mode

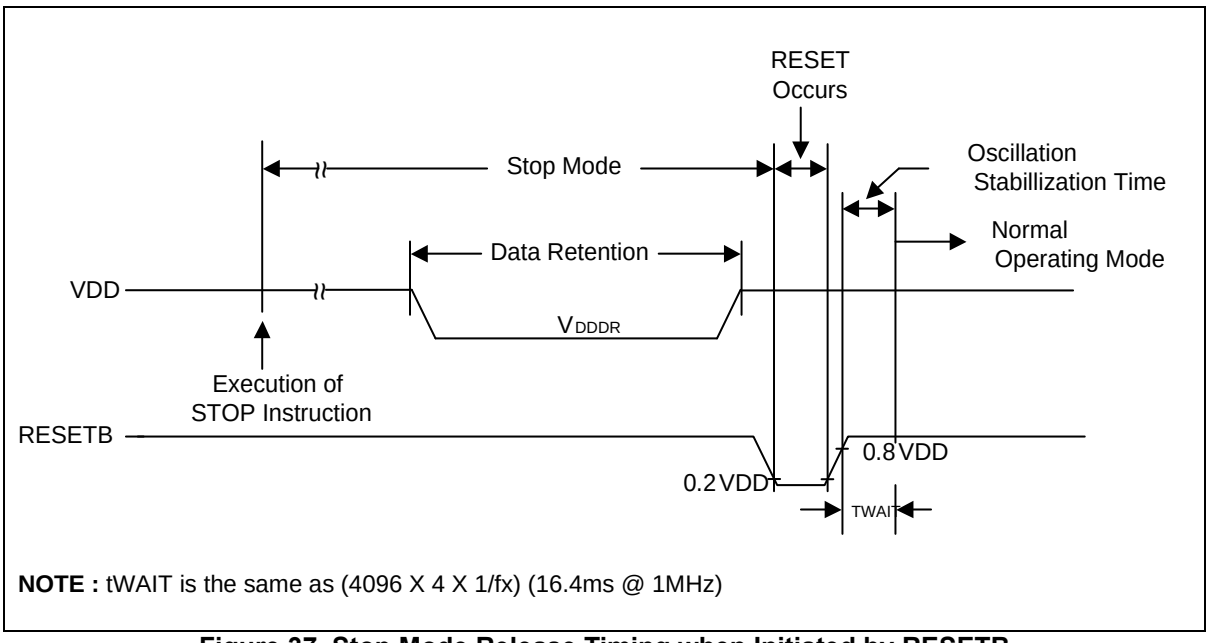
(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 36. Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 37. Stop Mode Release Timing when Initiated by RESETB

18.14 Internal flash ROM characteristics

Table 28. Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM} NOTE2	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE} NOTE2	–	–	–	30,000	times

NOTE:

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC for system clock).
2. The measured value for the parameters and conditions listed were confirmed by simulation.

18.15 Recommended circuit and layout

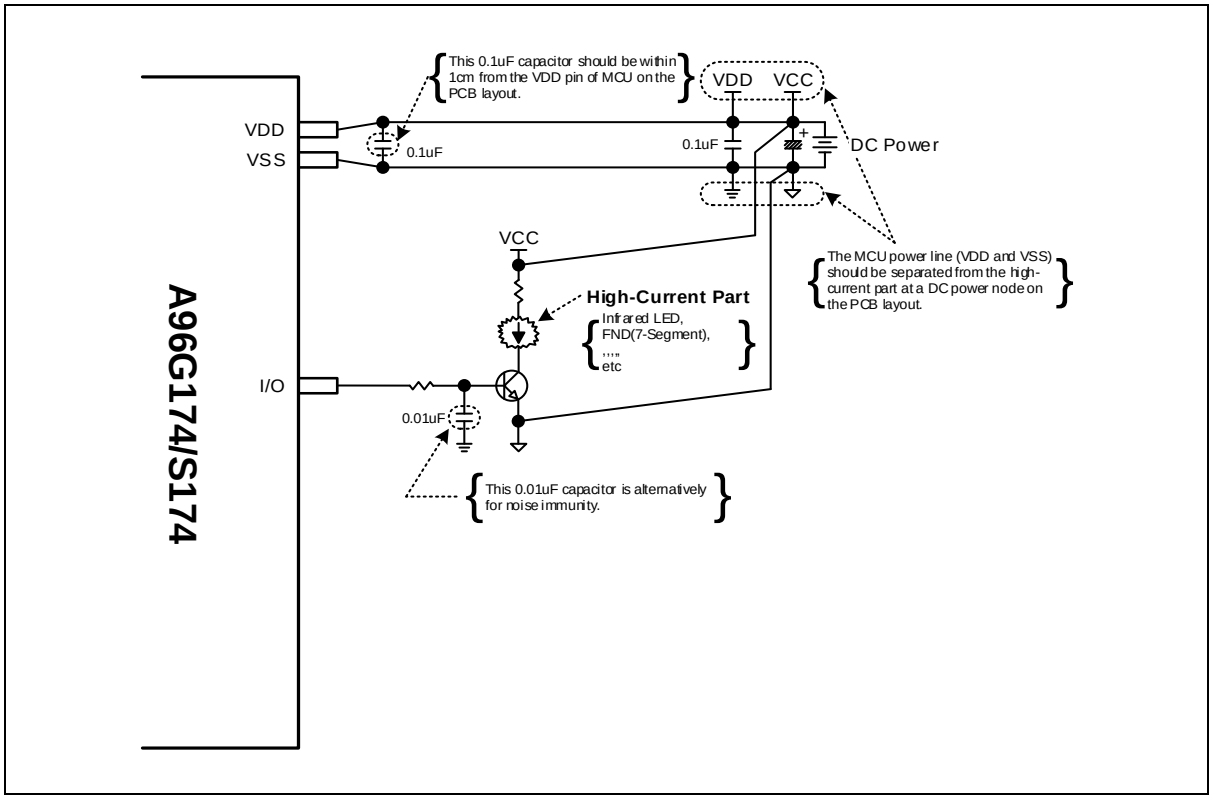


Figure 38. Recommended Voltage Range

Table 29. Reset Pin Component Values

Item	Component	Value
Pull-up/down resistor	R1	10KΩ
Filter capacitor	C1	Typ. 100nF (0.1uF, example)

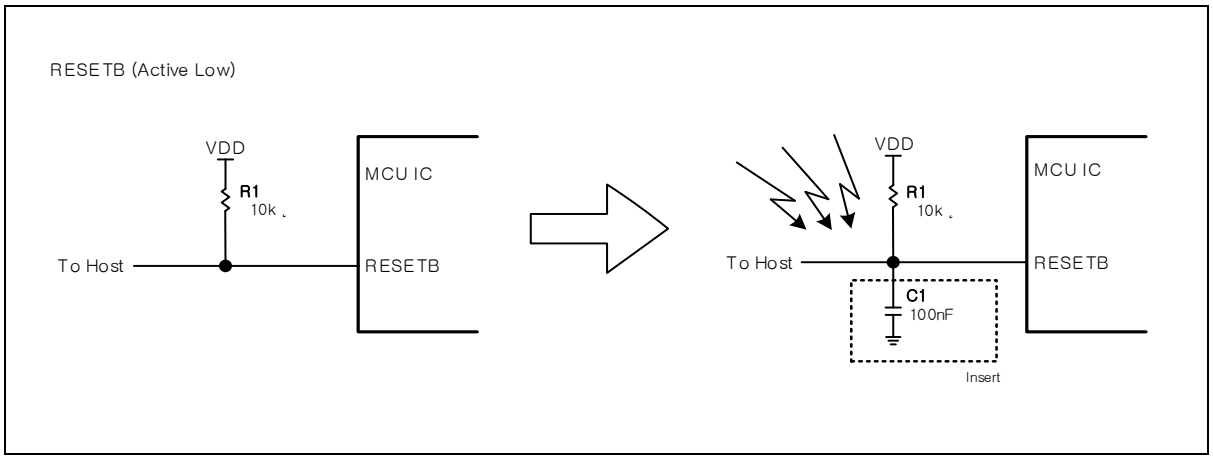


Figure 39. Filters used on a Reset Pin Diagram

19 Development tools

This chapter introduces a wide range of development tools for microcontrollers. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire developer ecosystem of the customers.

19.1 Compiler

ABOV semiconductor does not provide any compiler for the A96G174/A96S174. Regarding the compilers, it is recommended to consult with your compiler provider.

Since A96G174/A96S174 has the Mentor 8051 as a core, and ROM is smaller than 64Kbytes in size, a developer can use any standard 8051 compiler from other providers.

19.2 Core and debug tool information

ABOV's microcontroller uses OCD (On-Chip Debugger) interface for debugging, which is ABOV's own interface. The OCD not only monitors and controls the core, but also supports the read and write operations of external memory and devices. In addition, it supports memory monitoring and break functions.

Debug interfaces such as OCD interfaces enable microcontrollers to write to internal programmable memory, allowing them to support ISP (In-System Program) that makes possible to write as a single chip or as an embedded chip in the system. Table 30 provides information of the core and debug emulation interface.

Table 30. Information of Core and Debug Emulation Interfaces

	Description	Remark
Device Name	A9xXxxx	
Series	94/ 95/ 96/ 97 series	
Core	M8051/ CM8051	
Extended Stack Pointer	Yes/ no	94, 97 series only
Debug Interface	OCD 1/ OCD 2	
Number of Break Point	4/ 8	
Real-time Monitoring	Yes/ no	OCD 2 only
Run Flag Port	Yes/ no	OCD 2 option

NOTE:

1. The A96G174/A96S174 has the 96 series core and OCD 1 interface.
2. The A96G174/A96S174 can be operated with OCD II dongle too, because the OCD II dongle includes all of OCD1 functions.
3. The 95 series core is the old version of 96 series core.

19.2.1 Feature of 94/96/97 series core

ABOV's 8-bit microcontroller contains the M8051/CM8051 core that is an improved version of the 8051. The M8051/CM8051 core is compatible with the 8051, and reduces time of operation cycles. It makes development easier by providing the OCD debug function.

ABOV's 8-bit microcontroller has a core of the 94-series, 96-series, or 97-series that is basically compatible with the 8051 series at the instruction set level. The cores in each series use different Debug Interfaces, as shown in Table 31.

Table 31. Core and Debug Interface by Series

	Core	**Debug Interface**
96 Series	M8051	OCD 1
97 Series	M8051	OCD 2
94 Series	CM8051	OCD 2

Features of each series are compared in Table 32.

Table 32. Feature Comparison Chart By Series and Cores

	96 Series	**97 Series**	**94 Series**
CPU Core	M8051	M8051	CM8051
Cycle Compatible with MCS51	1/6	1/6	No
OCD Function	OCD 1	OCD 2	OCD 2
Program BUS	8-bit		
Data Bus	8-bit IRAM/ XRAM separated		8-bit single SRAM
EA Auto Clear NOTE1	Yes	Yes	Yes
EA=0, Idle/ Stope Mode Wake up	Yes	Yes	Yes
Interrupt Priority NOTE2	6 group x 4 level	Interrupt x 4 level	Interrupt x 2 level
Nested Interrupt Priority	4 level	4 level	Interrupt x 2 level (max. 4 times)
SFR BUS (read/ write)	Two ports	Two ports	Single port
Stack Extension	X	O	O
Register	SRAM		
Register Bank	4		
CPU/ Flash Clock Ratio	x 1		

Table 32. Feature Comparison Chart By Series and Cores (continued)

	96 Series	97 Series	94 Series
Pipeline	No	No	2-stage (IF + ID/ EX)
DHRY Stone Score (I8051: 1.00)	6.0	6.0	8.4
Average Instruction Set Exe. Cycle Compare with i8051	x 6.0	x 6.0	x 6.4
Power Consumption/ DHRY (@synthesis)	52.27uA/ MHz	52.27uA/ MHz	30.19 uA/ MHz

NOTE:

1. EA means that All Interrupt Enable bit or Disable bit (Standard 8051).
2. Group: When a programmer selects a specific interrupt (e.g. Interrupt1),
   Whole interrupts: 0, 6, 12, and 18 have higher priorities.
3. The A96G174/A96S174 has the 96 series core and OCD 1 interface.
4. The A96G174/A96S174 can be operated with the OCD II dongle too, because the OCD II dongle includes all functions of the OCD1.

ABOV's 8-bit microcontroller maintains binary compatibility with 8051 cores; however, the cores and series have differences in performances, core functionalities, and debug interfaces.

You can see the differences between each series in the following sections.

19.2.2 OCD type of 94/96/97 series core

Cores of the 96-series use the OCD 1 for debug interfaces, while cores of the 94-series and 97-series use the OCD 2 for debug interfaces. The OCD 1 and OCD 2 use the same method on the Hardware, however, the protocols are incompatible with each other.

In the OCD 2, it is able to measure the emulation time through the “Run Flag” pin.

Table 33. OCD Type of Each Series

	96-Series	97-Series	94-Series	Remark
OCD type	OCD 1	OCD 2	OCD 2	

In Table 34, debug interfaces of the OCD 1 and OCD 2 are compared.

Table 34. Comparison of OCD 1 and OCD 2

	Value	Description
OCD 1	Break point MAX.8	PC break only
OCD 2	Break point MAX.12	With RAM break • Code, XDATA, IDATA • 1/8/16/32bit compare
	Real-time monitoring	Code, XDATA, IDATA
	Frequency output	Examine CPU frequency
	Run Flag port	Option for run time measurement

96 Series – OCD 1

The 96 series supports basic operation of debug interfaces such as Run, Stop, Step, Break point, register reading/ writing, Memory reading/ writing, and SFR reading/ writing..

94 Series and 97 Series – OCD 2

The 94 series and 97 series support the features listed below, as well as the features of the OCD 1 (however, their protocol is incompatible with the OCD1):

- RTM support: CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- Run Flag support: Emulation Time can be measured in OCD mode (using the Run Flag port).
- RAM Break support: IDATA, SFR, and XDATA break are added.

19.2.3 Interrupt priority of 94/96/97 series core

In the M8051, users can set interrupt priorities by group. The 96-series microcontroller with the basic M8051 core only supports interrupt priorities in group units. In the 94-series or 97-series microcontroller, users set interrupt priorities to have more functionalities than existing features, and can set individual priority for each interrupt source.

Table 35. Interrupt Priorities in Groups and Levels

Series	96-Series	97-Series	94-Series	Remark
Interrupt Priority	6 Grouped 4 Level	Fully 4 Level	Fully 4 Level	**96 Series:** IP/IP (Interrupt Priority Register) **94, 97 Series:** IPxL/IPxH (Interrupt Priority Register)

96 Series

- The priority by group is available only with IP/IP1 settings.
  - With the IP/IP1 settings, users can set the interrupt priorities in group units.
  - The interrupt priority in group units (4 interrupts in a group) can be changed to the level between 0 and 3 according to the value of the IP/IP1.

94, 97 Series

- The individual interrupt priority can be set by setting IPxL/IPxH (x = 0 to x = 3).
- The individual interrupt priority can be changed to the level between 0 and 3 according to value of the IPxL/IPxH (x = 0 to x = 3).

19.2.4 Extended stack pointer of 94/96/97 series core

The M8051 uses IRAM area for Stack Pointer. However, 94-series and 97-series microcontrollers use both IRAM area and XRAM area for the Stack Pointer by configuring additional registers.

The XSP and XSPCR registers are involved in this functionality as described below:

- By configuring the XSP/XSPCR register, you can use the XRAM area for the Stack Pointer.
  - The XSPCR decides whether to use XRAM for the Stack Pointer.
    - If XSPCR = ′0′, the IRAM is available for the Stack Pointer.
    - If XSPCR = ′1′, the XRAM is available for the Stack Pointer.
  - The XSP decides a position of XRAM Stack Pointer.
    - This is valid only if XSPCR=′1′.

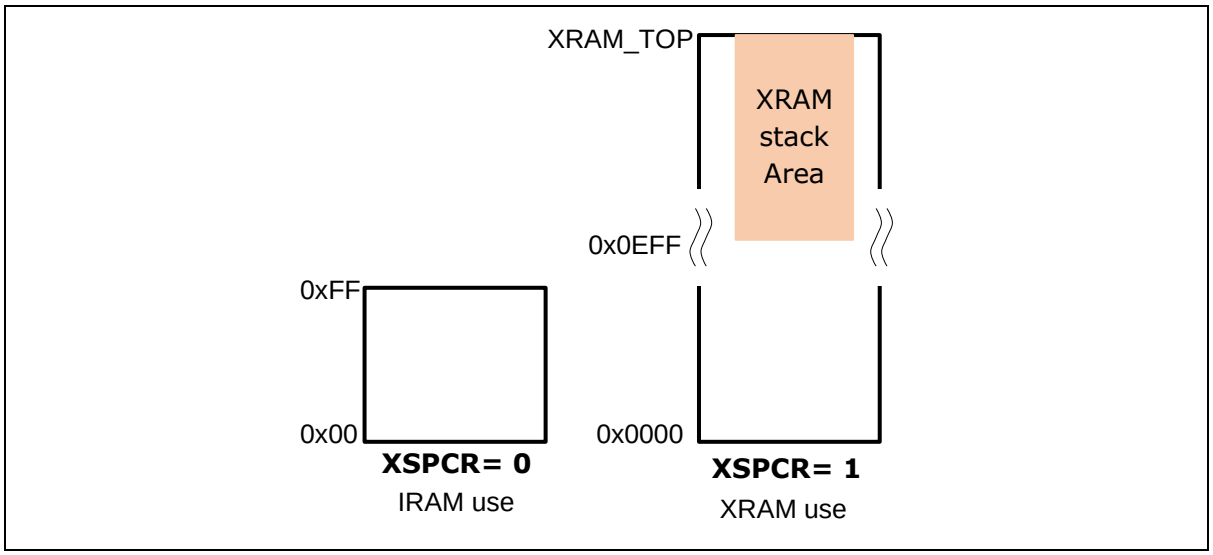


Figure 40. Configuration of the Extended Stack Pointer

STACK_POINTER = {XSP[7:0],SP[7:0]} = XRAM_TOP – STACK_SIZE

Ex) If only 256bytes of XRAM will be used for stack,

- XRAM_TOP = 4K(0x0FFF)
- STACK_SIZE = 256byte(0x0100)
- XSPCR= 1, XSP= 0x0E
- SP=0xFF setting
- Stack Pointer Position = 0x0FFF - 0x0100= 0x0EFF

19.3 OCD (On-chip debugger) emulator and debugger

Microcontrollers with 8051 cores have an OCD (On-Chip Debugger), a debug emulation block. The OCD is connected to a target microcontroller using two lines such as DSCL and DSDA. The DSCL is used for clock signal and the DSDA is used for bi-directional data.

The two lines work for the core management and control by doing register management and execution, step execution, break point and watch functions. In addition, they control and monitor the internal memory and the device by reading and writing.

Table 36. Debug Feature by Series

Series name	96-series	97-series	94-series
OCD function	OCD 1	OCD 2	OCD 2
Max. number of breakpoints	8	8	4
Saving stack in XRAM	No	Yes	Yes
Real time monitoring	No	Yes	Yes
Run flag support	No	Yes	Yes

The OCD 2 applied to the 94-series and 97-series provides the RTM (Real Time Monitoring) function that monitors internal memory and I/O status without stopping the debugging. In addition, the OCD 2 provides the breakpoint function (RAM Break Function) for the IDATA, SFR, and XDATA.

The following functions have been extended from the OCD 2:

- Emulation Time can be measured in OCD mode (using the Run Flag port)
- CODE, XDATA, and IDATA are updated during the Run Time (Real Time Monitoring available).
- IDATA, SFR, and XDATA break are added (RAM Break support).

Figure 41 shows the standard 10-pin connector of OCD 1 and OCD 2.

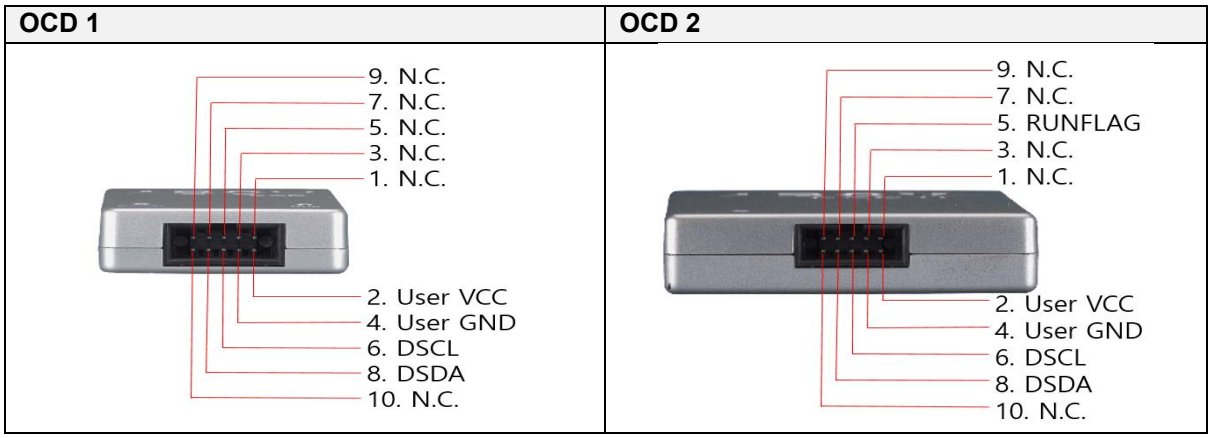


Figure 41. OCD 1 and OCD 2 Connector Pin Diagram

Table 37 introduces pins used for the OCD 1 and OCD 2.

Table 37. OCD 1 and OCD 2 Pin Description

Pin name	Microcontroller function in Debug Mode	
	I/O	**Description**
DSCL	I	Serial clock pin. Input only pin.
DSDA	I/O	• Serial data pin. • Output port when reading and input port when programming. • IT can be assigned as input/push-pull output port.
VDD,VSS	__	Logic power supply pin.

The OCD emulator supports ABOV's 8051 series MCU emulation. The OCD uses two wires that are interfaces between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means that the OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista (32-bit). If you want to see more details, please visit ABOV's website (www.abovsemi.com), and download debugger S/W and OCD debugger manuals.

- Connection:
  - DSCL (A96G174/A96S174 P01 port)
  - DSDA (A96G174/A96S174 P00 port)

Figure 42 shows pinouts of OCD connector.

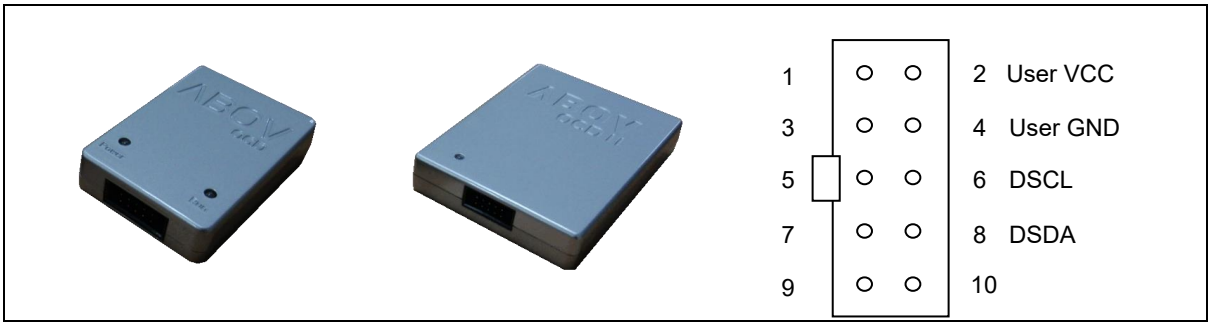


Figure 42. Debugger (OCD1/OCD2) and Pinouts

19.3.1 On-chip debug system

A96G174/A96S174 supports On-chip debug (OCD) system. We recommend developing and debugging program with A96G1xx series. The OCD system of the A96G174/A96S174 can be used for programming the non-volatile memories and on-chip debugging.

In this section, you can find detailed descriptions for programming via the OCD interface. Table 38 introduces features of the OCD.

Table 38. OCD Features

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

Figure 43 shows a block diagram of the OCD interface and the On-chip Debug system.

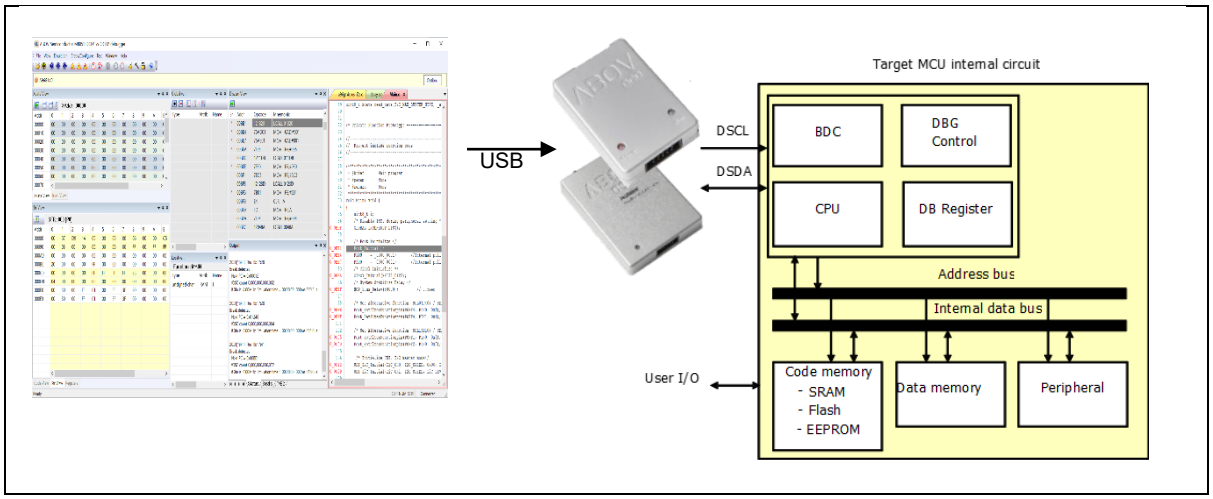


Figure 43. On-Chip Debugging System in Block Diagram

19.3.2 Entering debug mode

While communicating through the OCD, you can enter the microcontroller into DEBUG mode by applying power to it. This means that the microcontroller enters DEBUG mode when you place specific signals to the DSCL and DSDA at the moment of initialization when the microcontroller is powered on. This requires that you can control power of the microcontroller (VCC or VDD) and need to be careful to place capacitive loads such as large capacity condensers on a power pin.

Please remember that the microcontroller can enter DEBUG mode only when power is applied, and it cannot enter DEBUG mode once the OCD is run.

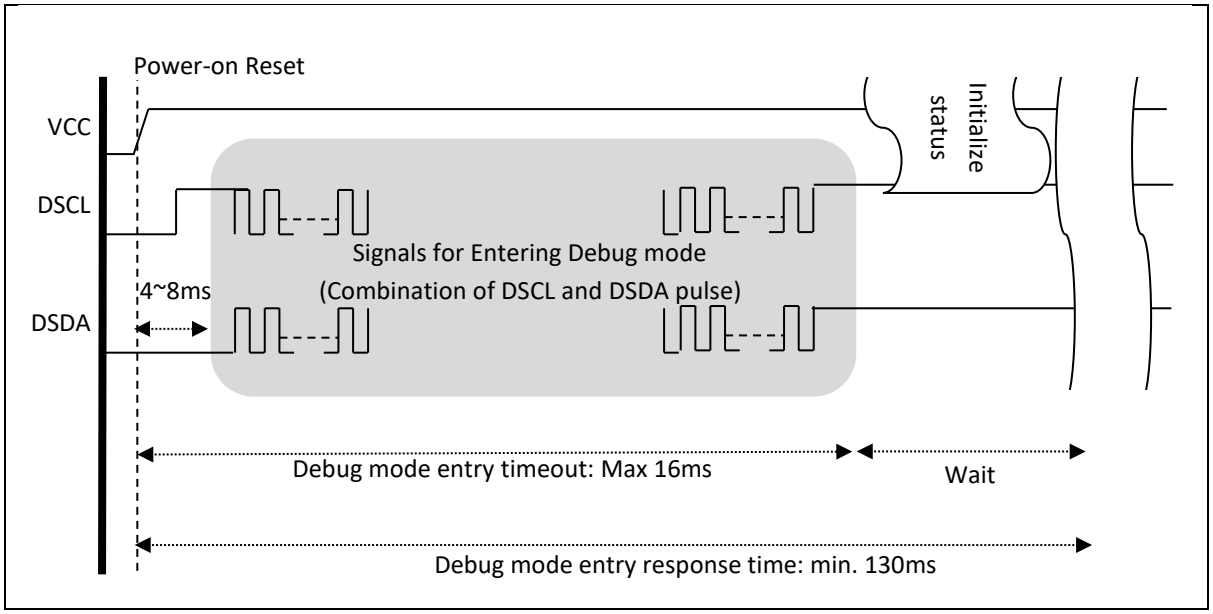


Figure 44. Timing Diagram of Debug Mode Entry

19.3.1 Two-wire communication protocol

For the OCD interface, the semi-duplex communication protocol is used through separate two wires, the DSCL and DSDA. The DSCL is used for serial clock signal and the DSDA is used for bi-directional serial address and data.

A unit packet of transmission data is 10-bit long and consists of a byte of data, 1-bit of parity, and 1-bit of acknowledge. A parity check bit and a receive acknowledge bit are transmitted to guarantee stability of the data communication. A communication packet includes a start bit and an end bit to indicate the start and end of the communication.

More detailed information of this communication protocol is listed below:

Basic transmission packet

- A 10-bit packet transmission using two-pin interface.
- A packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of ′1′ for 8-bit data in transmitter.
- Receiver generates acknowledge bit as ′0′ when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is ′1′ at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits a command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start and stop conditions notify start and stop of the background debugger command respectively.

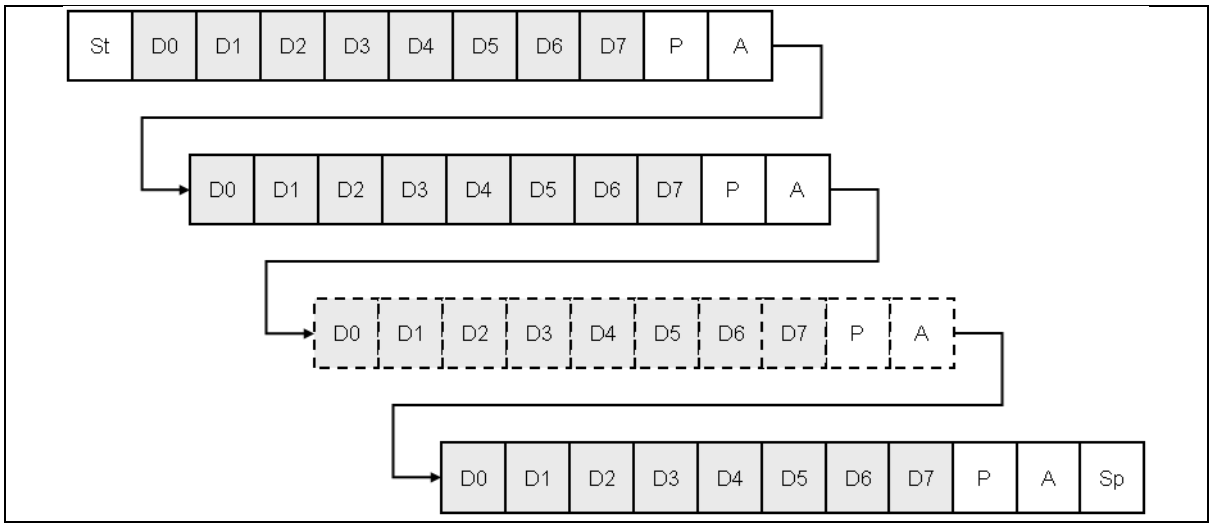


Figure 45. 10-bit Transmission Packet

Packet transmission timing

Figure 46 shows a timing diagram of a packet transmission using the OCD communication protocol.

A start bit in the figure means start of a packet and is valid when the DSDA falls from 'H' to 'L' while External Host maintains the DSCL to 'H'. After the valid start bit, communication data is transferred and received between a Host and a microcontroller.

An end bit means end of the data transmission and is valid when the DSDA changes from 'L' to 'H' while a Debugger maintains the DSCL to 'H'. Next, the microcontroller places the bus in a wait state and processes the received data.

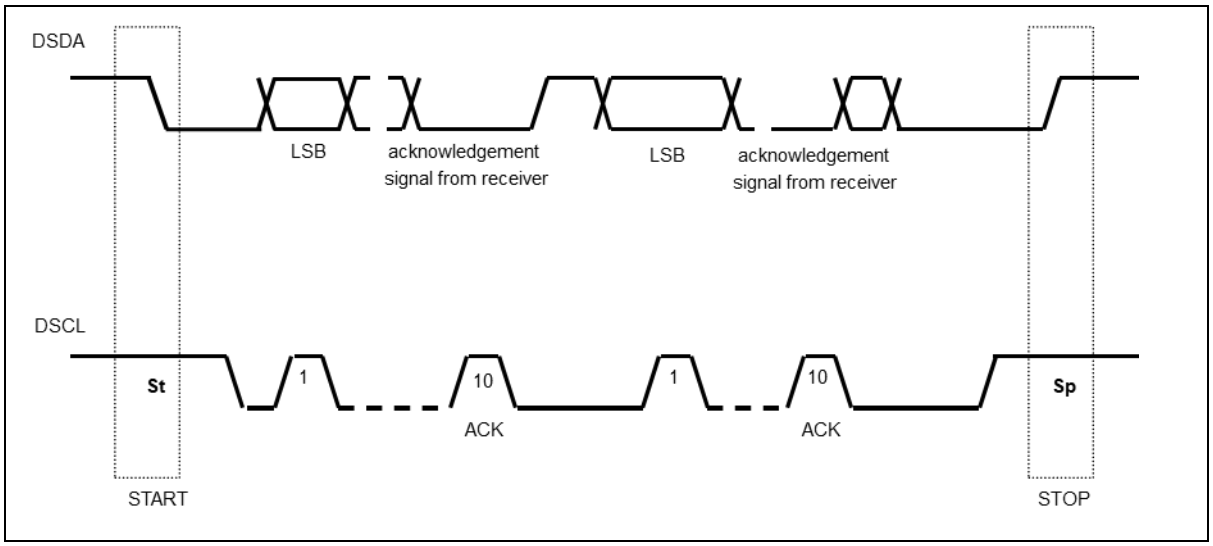


Figure 46. Data Transfer on OCD

Figure 47 shows a timing diagram of each bit based on state of the DSCL clock and the DSDA data. Similar to I2C signal, the DSDA data is allowed to change when the DSCL is 'L'. If the data changes when the DSCL is 'H', the change means 'START' or 'STOP'.

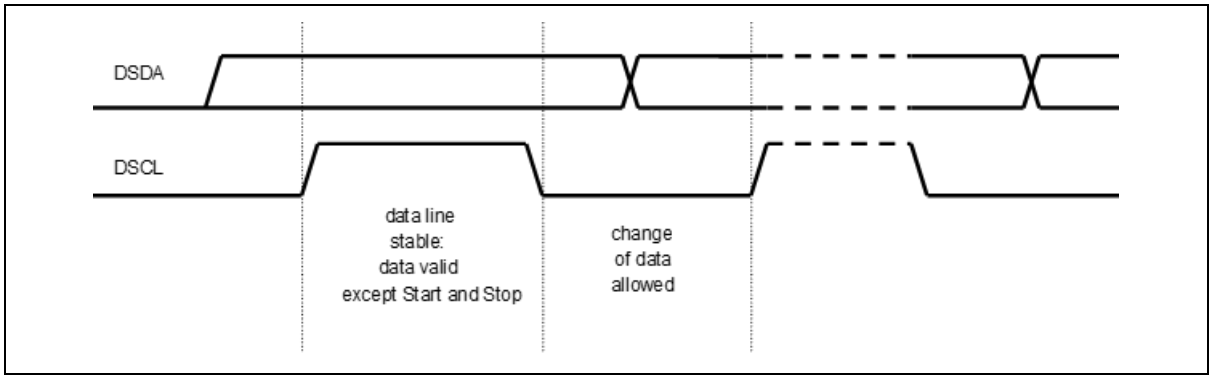


Figure 47. Bit Transfer on Serial Bus

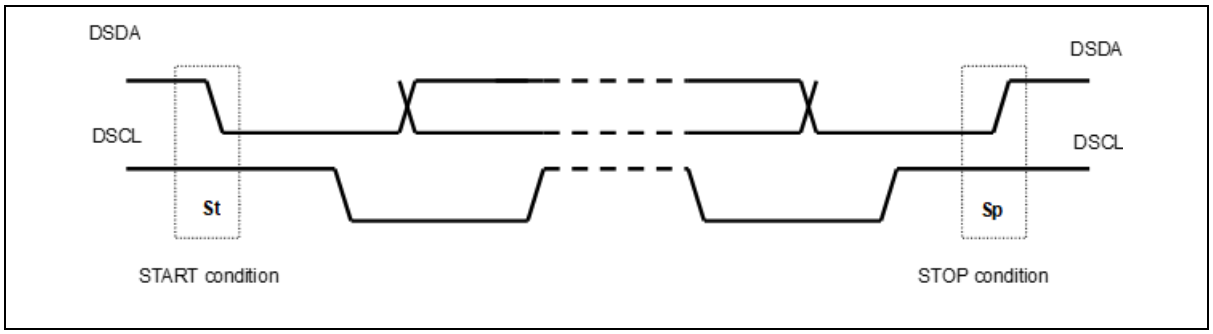


Figure 48. Start and Stop Condition

During the OCD communication, each data byte is transferred in accompany with a parity bit. When data is transferred in succession, a receiver returns the acknowledge bit to inform that it received.

As shown in Figure 49, when transferring data, a receiver outputs the DSDA to ‘L’ to inform the normal reception of data. If a receiver outputs DSDA to ‘H’, it means error reception of data.

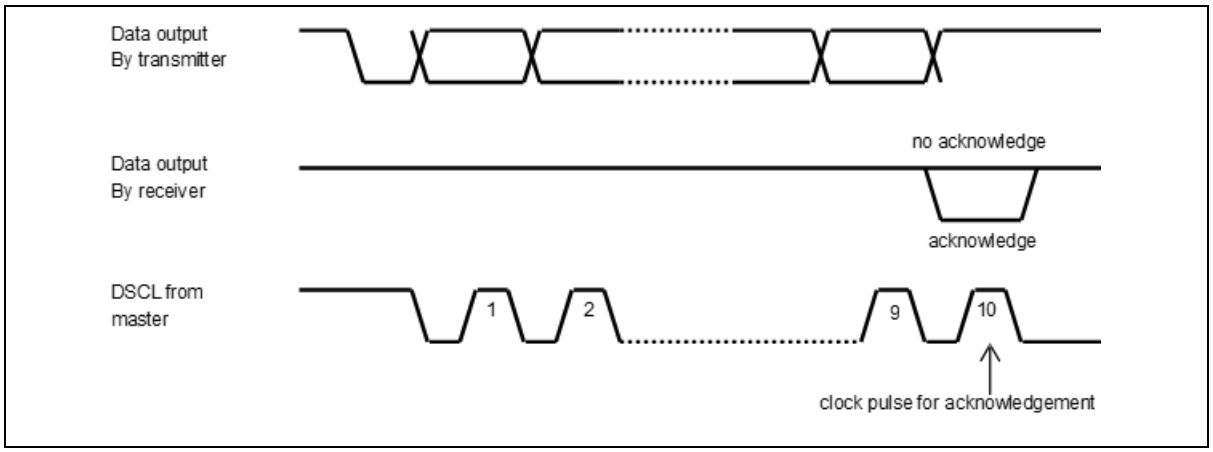


Figure 49. Acknowledge on Serial Bus

While the Host Debugger executes data communications, if a microcontroller needs communication delay or process delay, it can request communication delay to the Host Debugger.

Figure 50 shows timing diagrams where a microcontroller requests communication delay to the Host Debugger. If the microcontroller requests timing delay of the DSCL signal that the Host Debugger outputs, the microcontroller maintains the DSCL signal to ‘L’ to delay the clock change although the Host Debugger changes the DSCL to ‘H’.

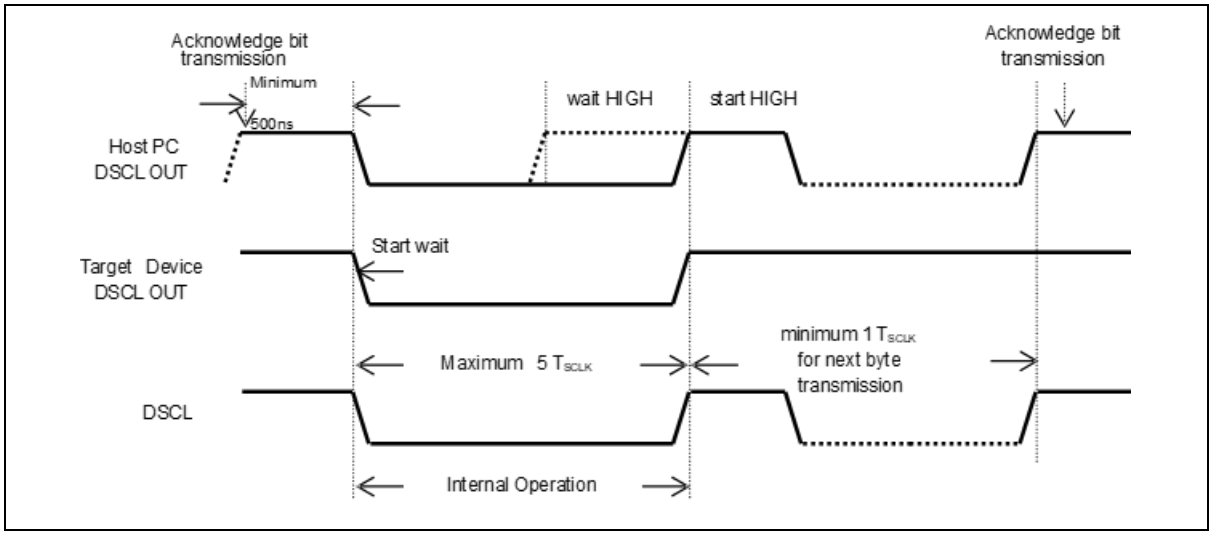


Figure 50. Clock Synchronization during Wait Procedure

19.4 Programmers

19.4.1 E-PGM+

E-PGM+ USB is a single programmer. You can program A96G174/A96S174 directly using the E-PGM+.

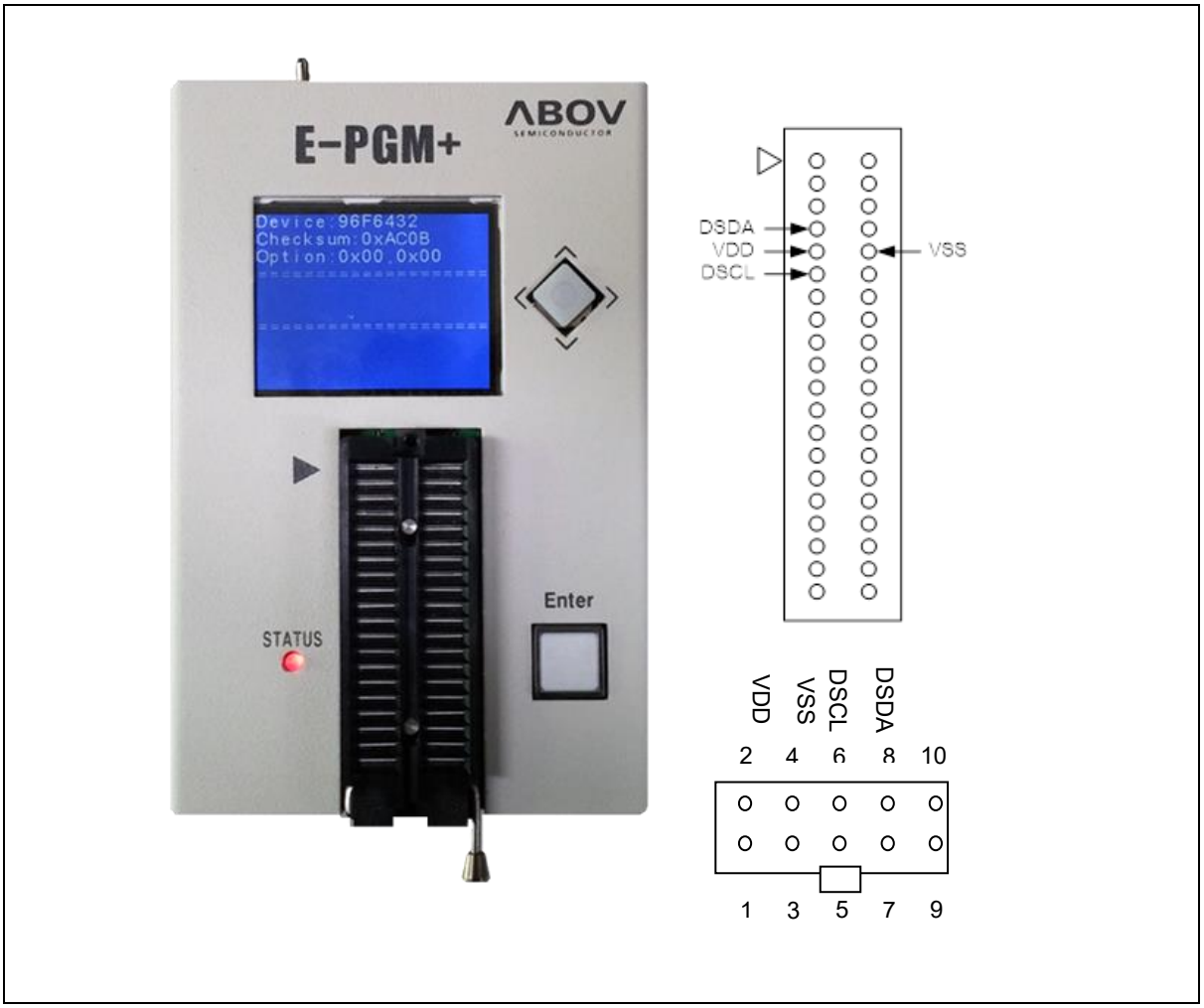


Figure 51. E-PGM+ (Single Writer) and Pinouts

19.4.2 OCD emulator

OCD emulator allows users to write code on the device too, since OCD debugger supports In System Programming (ISP). It doesn't require additional H/W, except developer's target system.

19.4.3 Gang programmer

E-Gang4 and E-Gang6 allow users to program multiple devices simultaneously. They can be run not only in PC controlled mode but also in standalone mode without the PC control.

USB interface is available, and it is easy to connect to the handler.

Figure 52. E-Gang4 and E-Gang6 (for Mass Production)

19.5 Flash programming

Program memory for A96G174/A96S174 is a Flash type. This Flash ROM is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. For detailed information about the Flash memory programming, please refer to **17. Memory programming.**

Table 39 introduces each pin and corresponding I/O status.

Table 39. Pins for Flash Programming

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

19.5.1 On-board programming

Microcontrollers need only four signal lines including VDD and VSS pins, to program the Flash ROM using serial protocol. Therefore, on-board programming is possible if the programming signal lines are considered at the time the PCB of application board is designed.

19.6 Connection of transmission

OCD's two-wire communication interfaces use the Open-Drain Method (Wire-AND Bi-Directional I/O).

Normally, it is recommended to place a resister greater than 4.7kΩ for the DSCL and DSDA respectively. The capacitive load is recommended to be less than 100pF. Outside these ranges, because the communication may not be accomplished, the connection to Debug mode is not guaranteed.

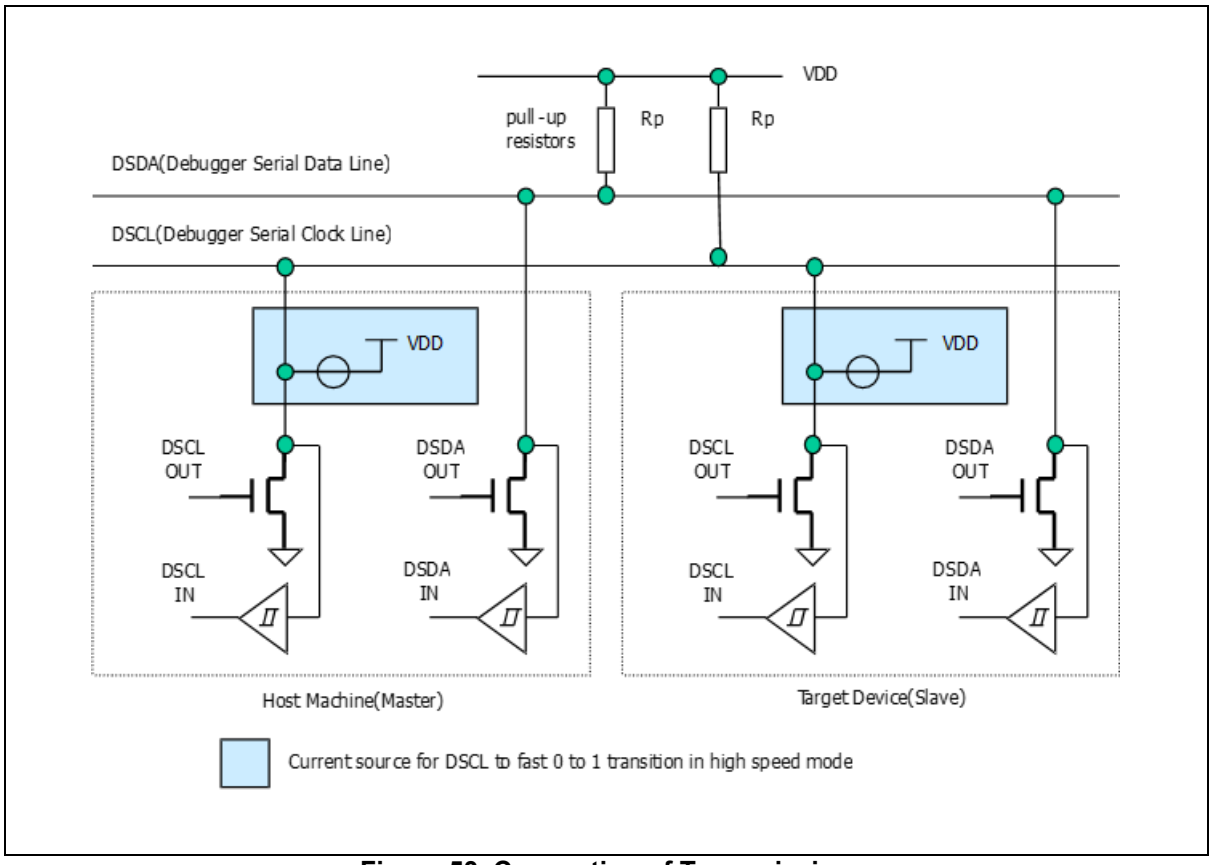


Figure 53. Connection of Transmission

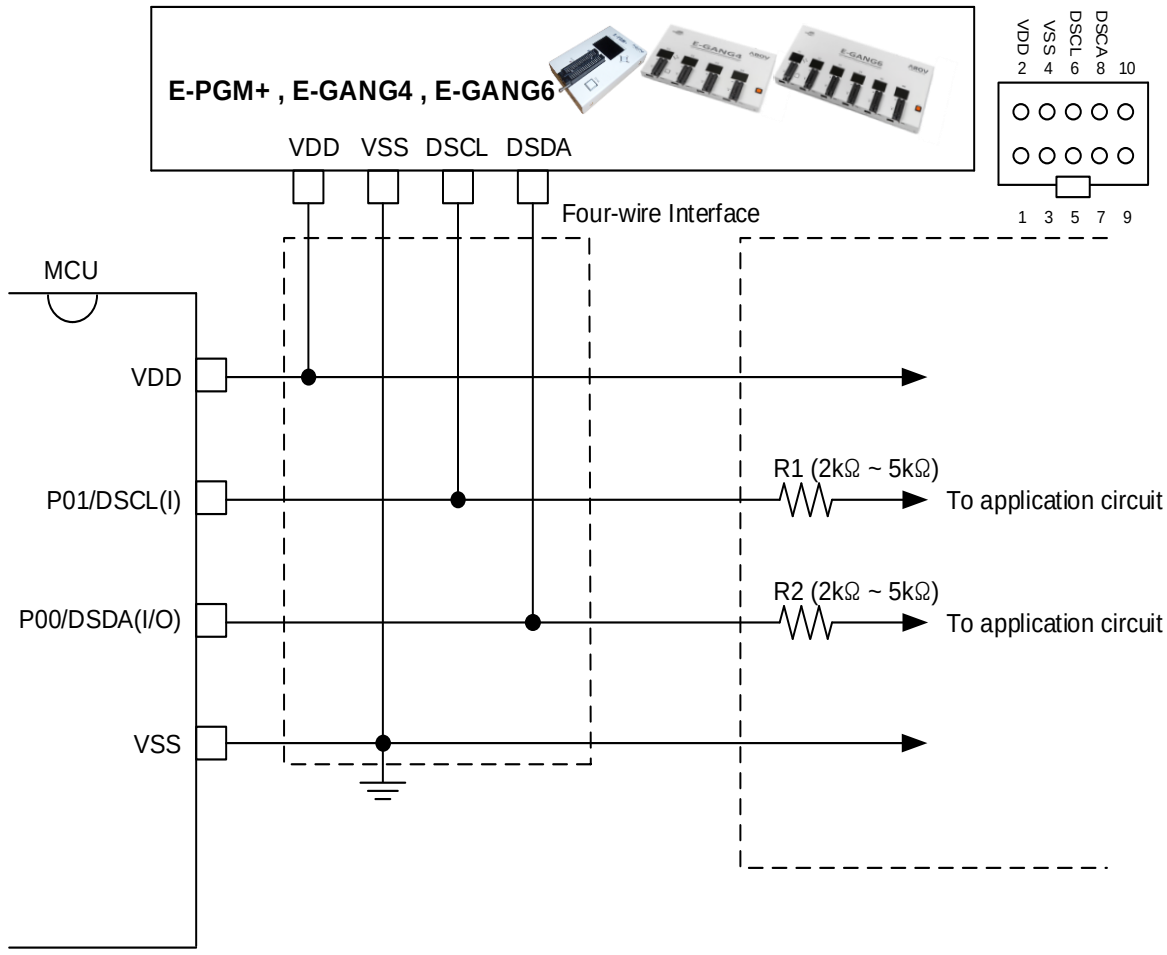
19.7 Circuit design guide

To program Flash memory, programming tools require 4 signal lines, DSCL, DSDA, VDD, and VSS. When designing a PCB circuit, you should consider these 4 signal lines for on-board programming. In addition, you need to be careful when designing the related circuit of these signal pins, because rising/falling timing of the DSCL and DSDA is very important for proper programming.

When you use the OCD pins exclusively or share them with other functions, it needs to be careful, too.

Figure 54 shows an example circuit where the OCD pins (DSCL and DSDA) are shared with other functions. They must be connected when debugging or executing In System Program (ISP).

Normally, the OCD pins are connected to outside to execute the predefined functions. Even when they are connected for debugging or executing ISP directly, the OCD pins are shared with other functions by using resistors as shown in Figure 54. By doing this, the OCD pins process the normal external signals and execute the OCD functions first when they are shared.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high-speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 54. PCB Design Guide for On-Board Programming

20 Package information

This chapter provides A96G174/A96S174 package information.

20.1 20 TSSOP package information

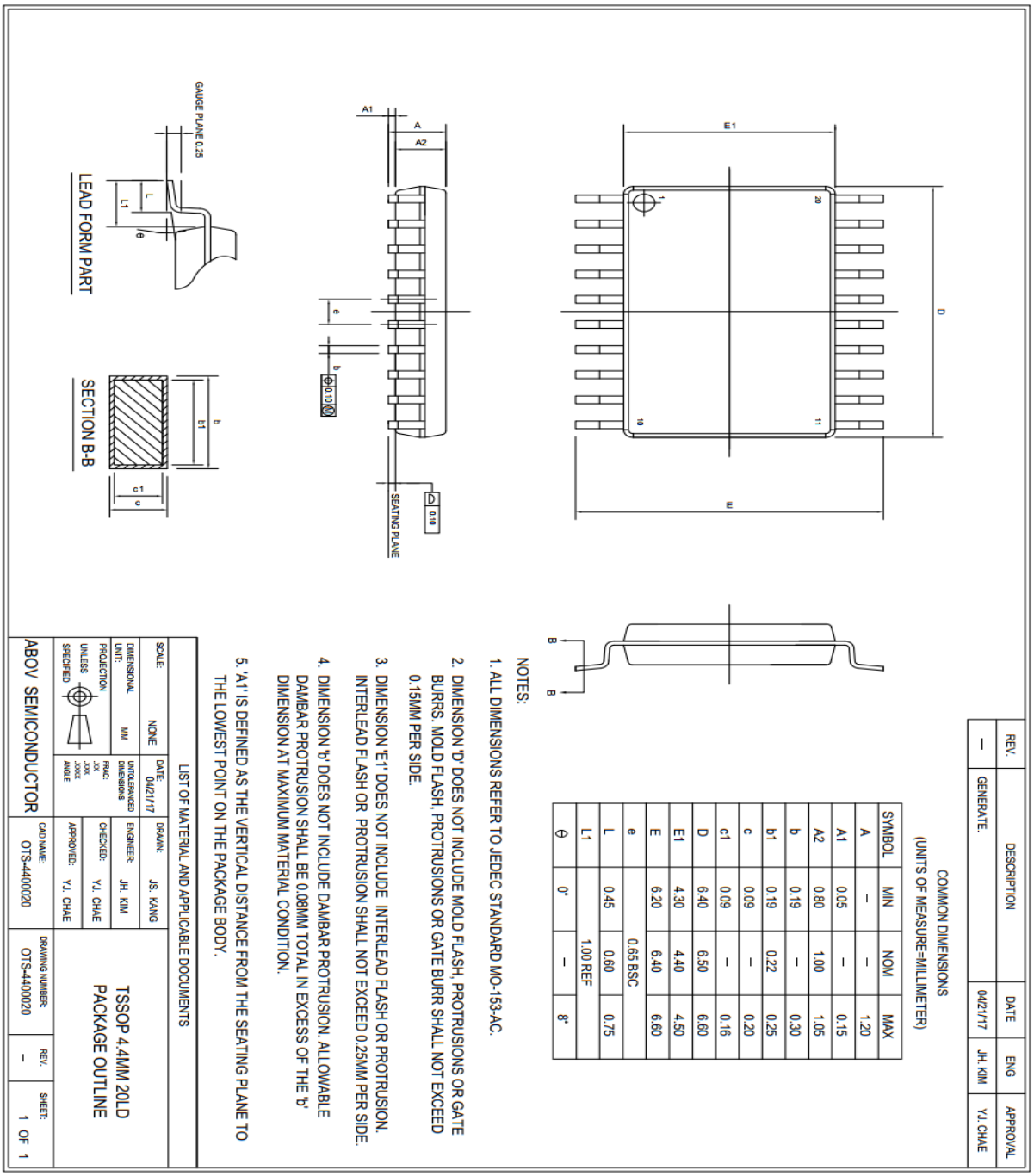


Figure 55. 20 TSSOP Package Outline

20.2 20 SOP package information

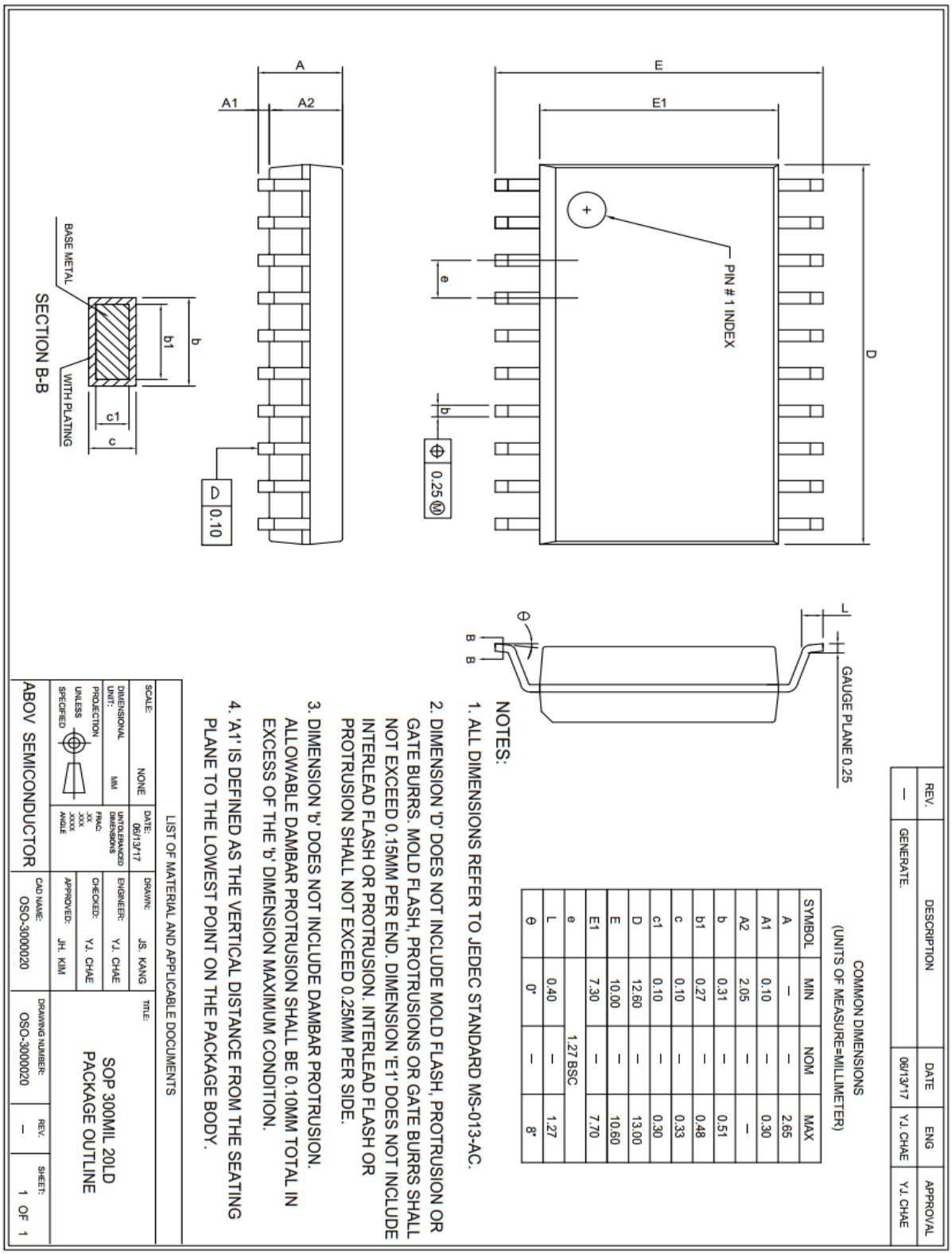


Figure 56. 20 SOP Package Outline

20.3 20 QFN package information

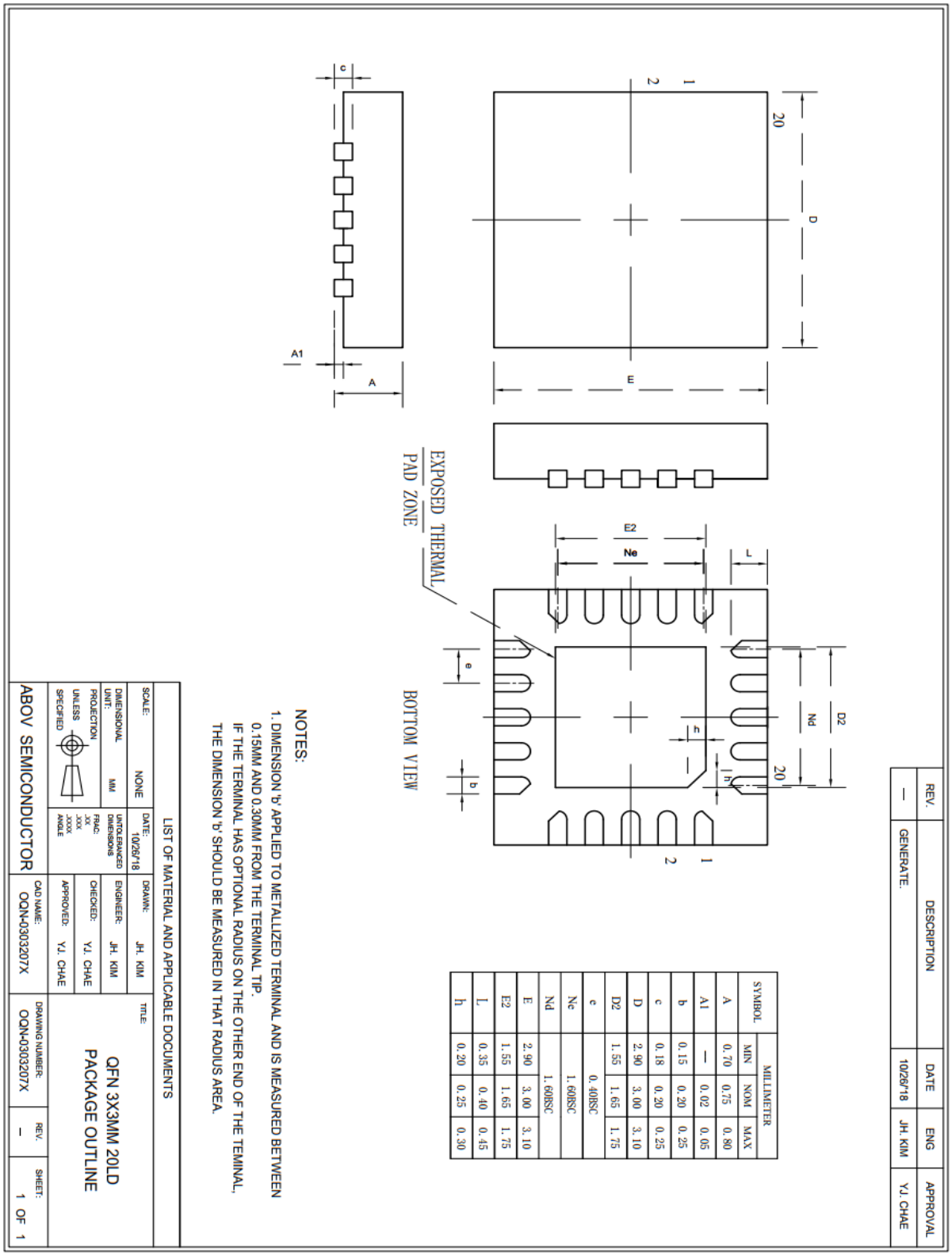


Figure 57. 20 QFN Package Outline

20.4 16 SOPN package information

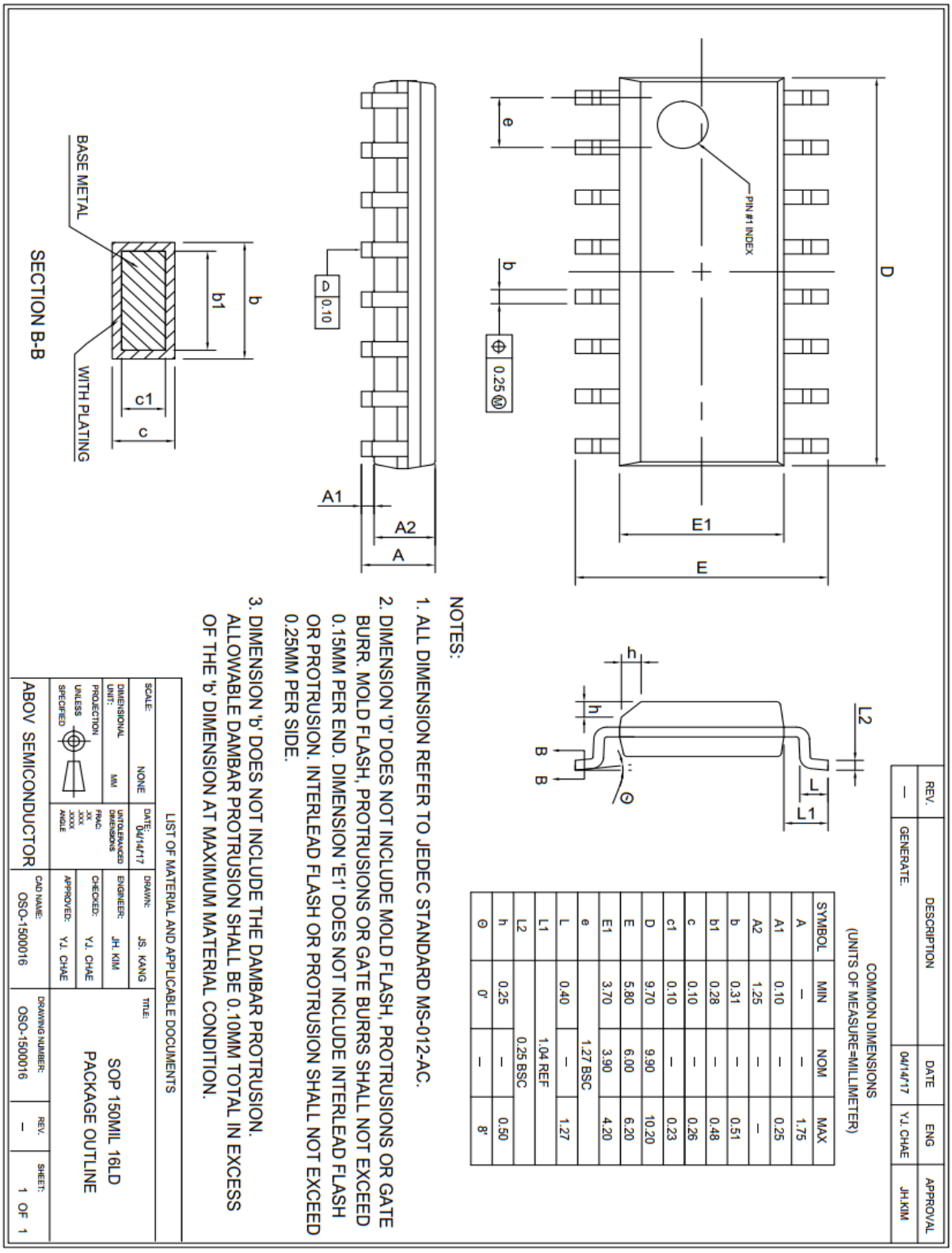


Figure 58. 16 SOPN Package Outline

21 Ordering information

Table 40. A96G174/A96S174 Device Ordering Information

Device name	FLASH	XRAM	IRAM	ADC	I/O	Package	Temperature Range
A96G174FR	8K bytes	256 bytes	256 bytes	15inputs	18	20 TSSOP	-40°C~ +85°C
A96S174FR				14inputs			
A96G174FD*				15inputs		20 SOP	
A96G174FU*				15inputs		20 QFN	
A96S174FU*				14inputs			
A96G174AE				13inputs	14	16 SOPN	
A96G174FR2	8K bytes	256 bytes	256 bytes	15inputs	18	20 TSSOP	-40°C~ +105°C
A96S174FR2				14inputs			
A96G174FD2*				15inputs		20 SOP	
A96G174FU2*				15inputs		20 QFN	
A96S174FU2*				14inputs			
A96G174AE2				13inputs	14	16 SOPN	

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

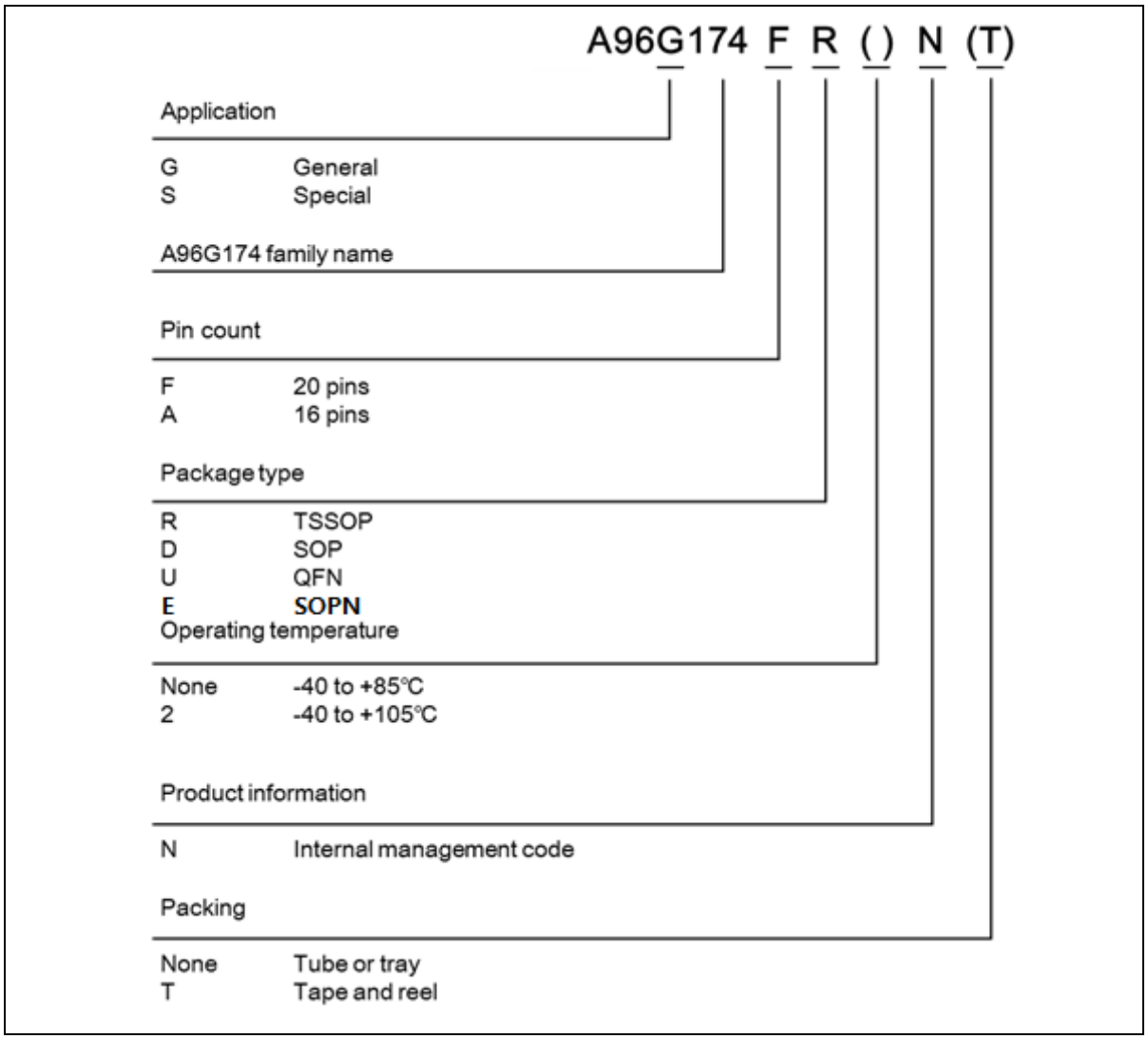


Figure 59. A96G174/A96S174 Device Numbering Nomenclature

Appendix

Instruction table

Instructions are either1, 2 or 3bytes long as listed in the ‘Bytes’ column below. Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

Table 41. Instruction Table

Arithmetic				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 41. Instruction Table (continued)

Logical				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 41. Instruction Table (continued)

Data transfer				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 41. Instruction Table (continued)

Boolean				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 41. Instruction Table (continued)

Miscellaneous				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00
Additional instructions (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, entries such as E8-EF indicate continuous blocks of hex opcodes used for 8 different registers. Register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as '11→F1' (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

CJNE instructions use abbreviation of #d for immediate data; other instructions use #data as an abbreviation.

Revision history

Date	Revision	Description
2019.12.10	1.00	First creation
2020.02.04	1.01	Added the disclaimer and modified the distributor.
2020.04.02	1.02	Revise “Ordering information”
2020.04.06	1.03	Revise “Device Numbering Nomenclature”
2020.05.22	1.04	Revise “Low voltage reset and low voltage indicator characteristics”
2020.06.08	1.05	Deleted AVREF at Figure 23. 12-bit ADC Block Diagram. Deleted Figure 58. A/D Power (AVREF) Pin with a Capacitor. Changed the maximum analog input voltage to VDD at Table 16. A/D Converter Characteristics. Updated Basic Timer Block Diagram at Figure 18. Added the description of V_{LVD}/V_{LVI} at Table 20. LVR and LVI Characteristics. Extended maximum operating temperature up to 105°C as well as 85°C.
2020.07.20	1.06	Enhanced the minimum ADC operation voltage to 2.2V at Table 16. A/D Converter Characteristics. Deleted Analog Reference Voltage item at Table 16. A/D Converter Characteristics. Added the note of “Guaranteed by design” at Table 17. Recommended ADC Resolution. Enhanced the tolerance of High-Speed Internal RC within “-40°C to +85°C” to ±2.5% at Table 21. High Internal RC Oscillator Characteristics. Corrected the conditions of Supply Current at Table 23. DC Characteristics. Updated the table and figures for USART characteristics in 17 Electrical characteristics. Corrected the minimum A/D Conversion time to 7.5us at Table 16. A/D Converter Characteristics.
2020.08.31	1.07	Advanced Flash Endurance times from 10,000 to 30,000.
2020.09.28	1.08	Updated the initial value in Table 6. SFR Map. Added the description of REMAP bit of FESR in 17.1.2 Register description. Added the example of reapplying the configure bytes by user program in 17.6 Configure option. Updated a typo in Table 19. Power on Reset Characteristics, Figure 82. Fast VDD Rising Time and Figure 83 Internal RESET Release Timing On Power Up.
2021.04.26	1.09	Changed the figures of Package Outline Drawing in 19 Package Information. Updated High Speed Internal RC Oscillator Tolerance at Table 21.High Internal RC Oscillator Characteristics. Corrected the frequency unit from KHz to kHz.
2022.04.01	1.10	Updated the Table 18. BGR Characteristics
2022.04.12	1.11	Added 4 Central processing unit. Marked simulation data in 18 Electrical characteristics. Added Figure 39. Filters used on a Reset Pin Diagram and Table 29 Reset Pin Component Values on page 73. Updated 19. Development tools chapter. Updated the pictures of development tool at 19 Development tools. Deleted the table of Input/Output Capacitance in Electrical Characteristics.

		Updated Package Outline Drawing to 20. Package information.
2022.10.20	1.12	Revised the font of this document Fixed the typing error of P12 at Figure 3. A96S174 20TSSOP pin assignment.

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
http://www.abovsemi.com/

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
http://www.abovsemi.com/

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr