32-bit Cortex-M3 based Programmable Motor Controller

AC33M8128
AC33M8128L
AC33M6128L

DATA SHEET

Version 1.2.2

2017.10.9.

Revision History:

Date	By	Version	Description
2015/12/15	SJ Park	0.9	File created
2016/01/07	SJ Park, MJ Kim	1.0	Clock configure procedure was modified.
2016/02/11	SJ Park	1.1	Modified IOL/IOH, VOL/VOH spec in DC characteristic.
2016/11/04	RS Park	1.2.0	Version renewal
2017/07/24	JH Oh	1.2.1	Package Dimension was corrected
2017/10/09	DH Shin	1.2.2	Modified Operation Frequency of PLL. (80MHz → 72MHz)

CHAPTER 1. OVERVIEW

1.1 INTRODUCTION

AC33M8128 is special purpose microcontroller for motor application. This microcontroller brings high-performance 32-bit computing to low cost system solution.

AC33M8128 provides 3-phase PWM generator units which are suitable to inverter motor drive system. Built-in two channels of 3-phase PWM generators control two inverter motors simultaneously.

Three 12-bit high speed ADC units with 16-channel analog multiplexed inputs support to get feedback information from motor. It can control up to two inverter motors or one inverter motor and PFC (Power Factor Correction) function simultaneously.

On-chip four operational AMPs and four analog comparators help to measure analog input signals. The Op-Amp can amplify input signal to proper signal range and transfer it to ADC input channel. The comparator monitors external signals and helps to makes internal emergency signal

Powerful and various external serial interface engines help to communicate with on-board sensors and devices.

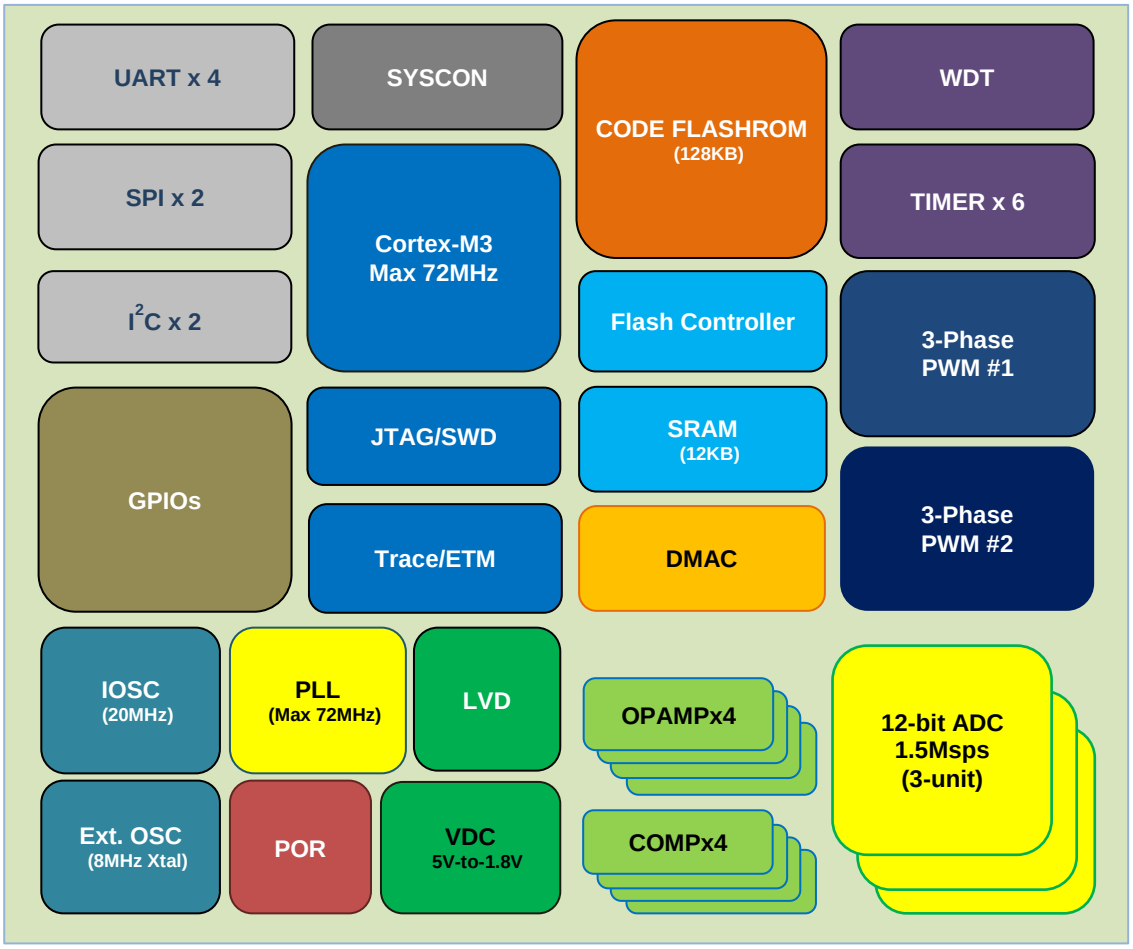

Figure 1.1. Block Diagram

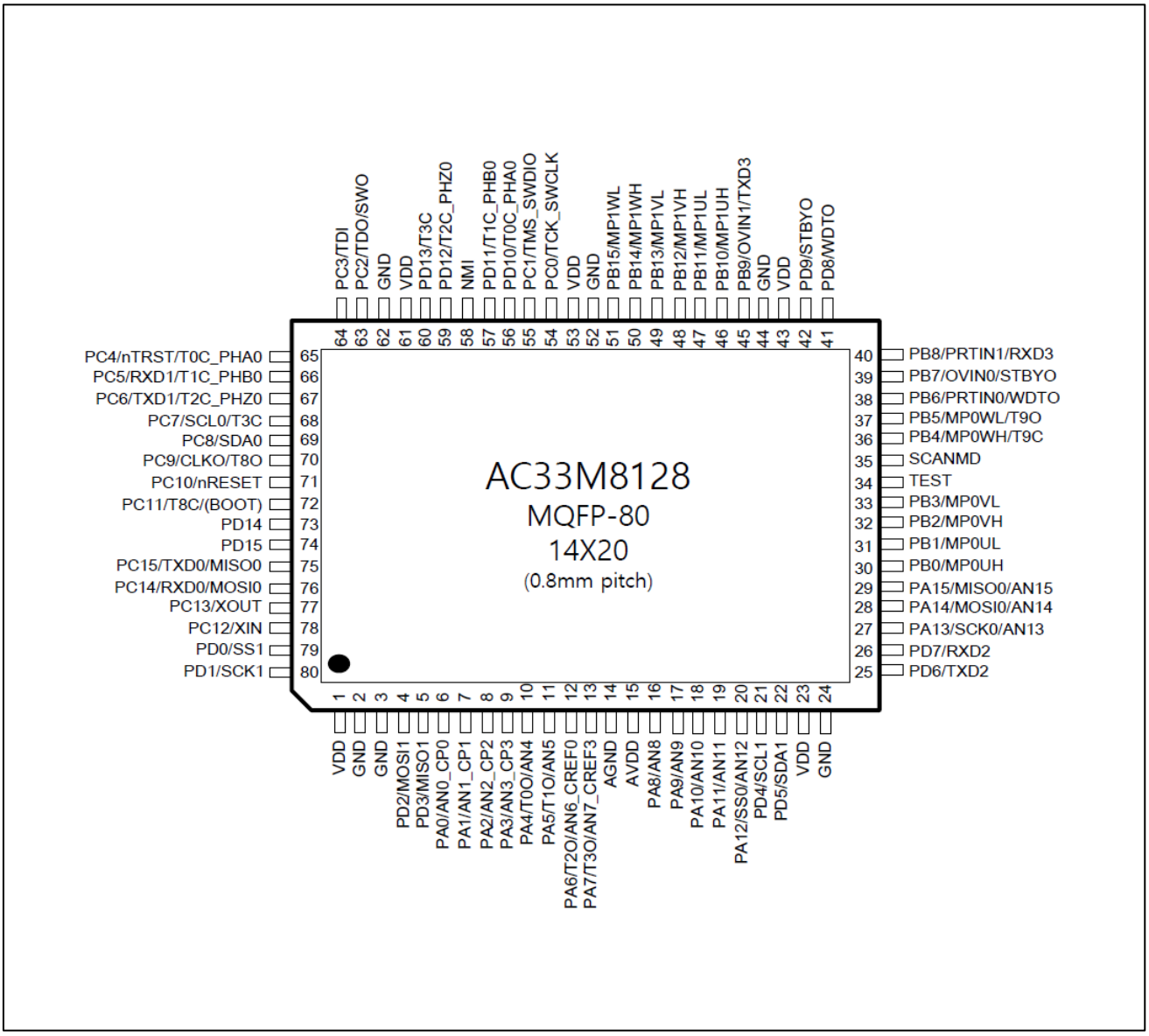

Figure 1.2. Pin layout (MQFP-80)

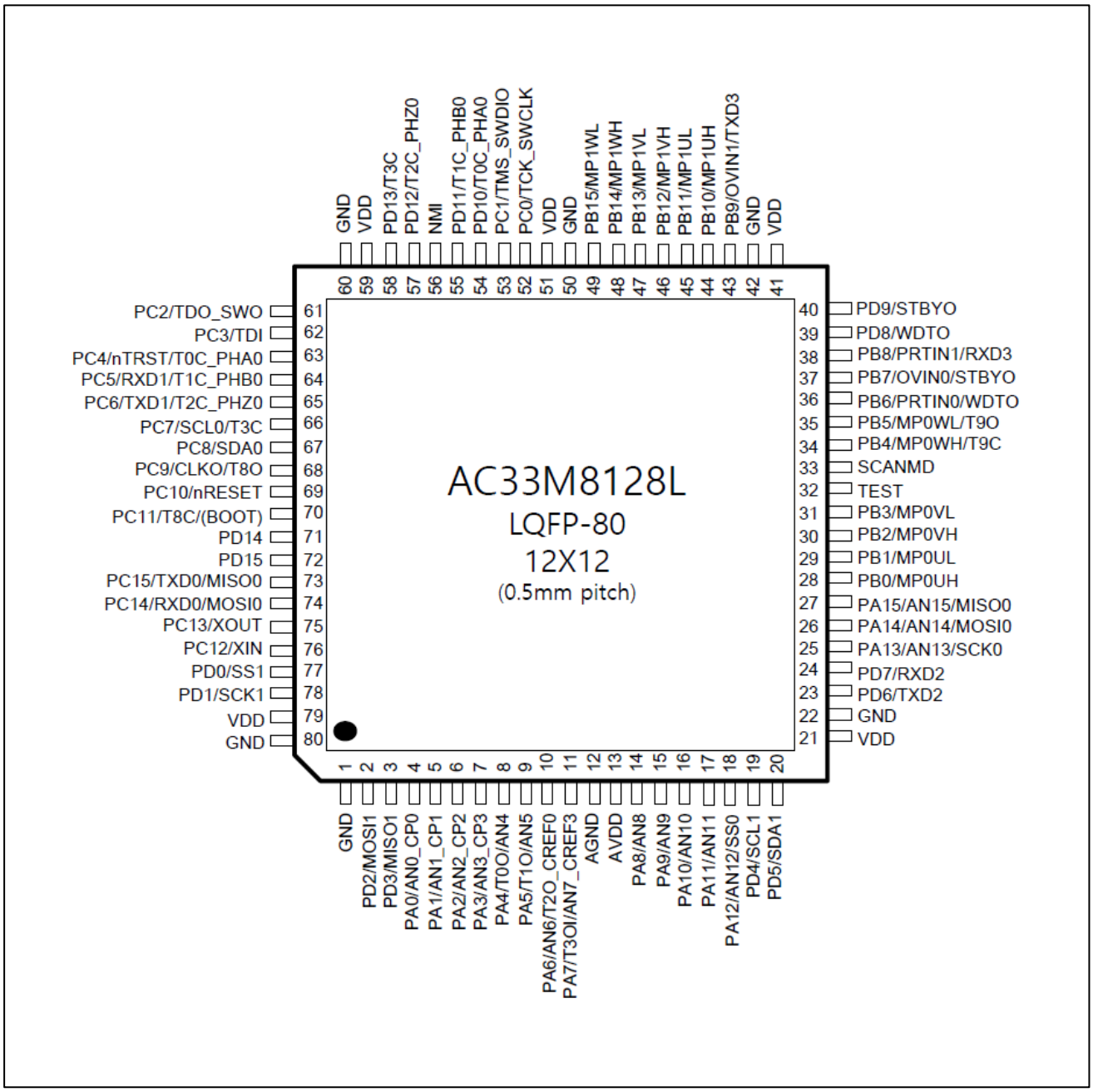

Figure 1.3. Pin layout (LQFP-80)

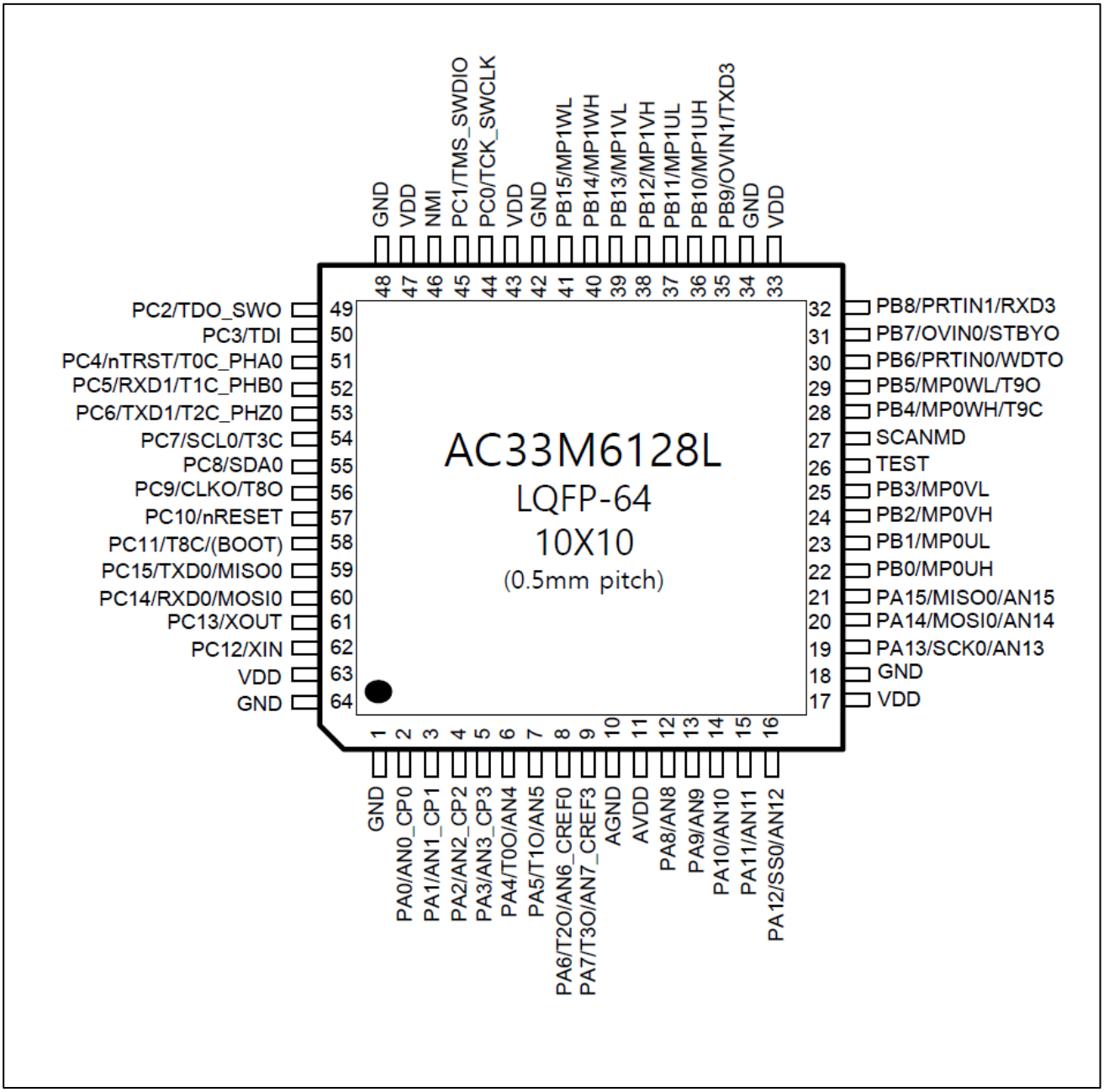

Figure 1.4. Pin layout (LQFP-64)

1.2 Product Features

Product features of AC33M8128 are as below:

- High Performance Low-power Cortex-M3 Core
- 128KB Code Flash Memory with Cache function
- 12KB SRAM
- 3-Phase Motor PWM with ADC triggering function
  - 2 Channels
- 1.5Msps high-speed ADC with burst conversion function
  - 2 or 3 units with 16 channel input
- Built-in PGA(Programmable Gain Amplifier) for ADC inputs
  - 4 Channels
    - 3 Channels for 3 shunt resistor configuration
    - 1 Channel for 1 shunt resistor configuration
- Built-in Analog Comparator
  - 4 channels
    - 3 channels for 3 shunt resistor configuration
    - 1 channel for 1 shunt resistor configuration
- System Fail-Safe function by Clock Monitoring
- XTAL OSC Fail monitoring
- Precision Internal Oscillator Clock (20MHz ±3%)
- Watchdog Timer
- Six General Purpose Timers
- Quadrature Encoder Counter
- External communication ports: 4 UARTs, 2 I^2Cs, 2 SPIs
- High current driving port for UART photo couplers
- Debug and Emergency stop function
- Real-time Monitoring function support for more effective development
- JTAG and SWD in-circuit debugger
- Various Memory size and Package options
  - MQFP-80, LQFP-80, LQFP-64
- Industrial grade operating temperature (-40 ~ +85℃)

Table1.1. Device type

Part Number	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O PORT	PKG
AC33M8128	128KB	12KB	4	2	2	2	3-unit 16 ch	64	MQFP-80
AC33M8128L			4	2	2	2		68	LQFP-80
AC33M6128L			2	2	1	2		48	LQFP-64

1.3 ARCHITECTURE

1.3.1 Block Diagram

AC33M8128 Block diagram.

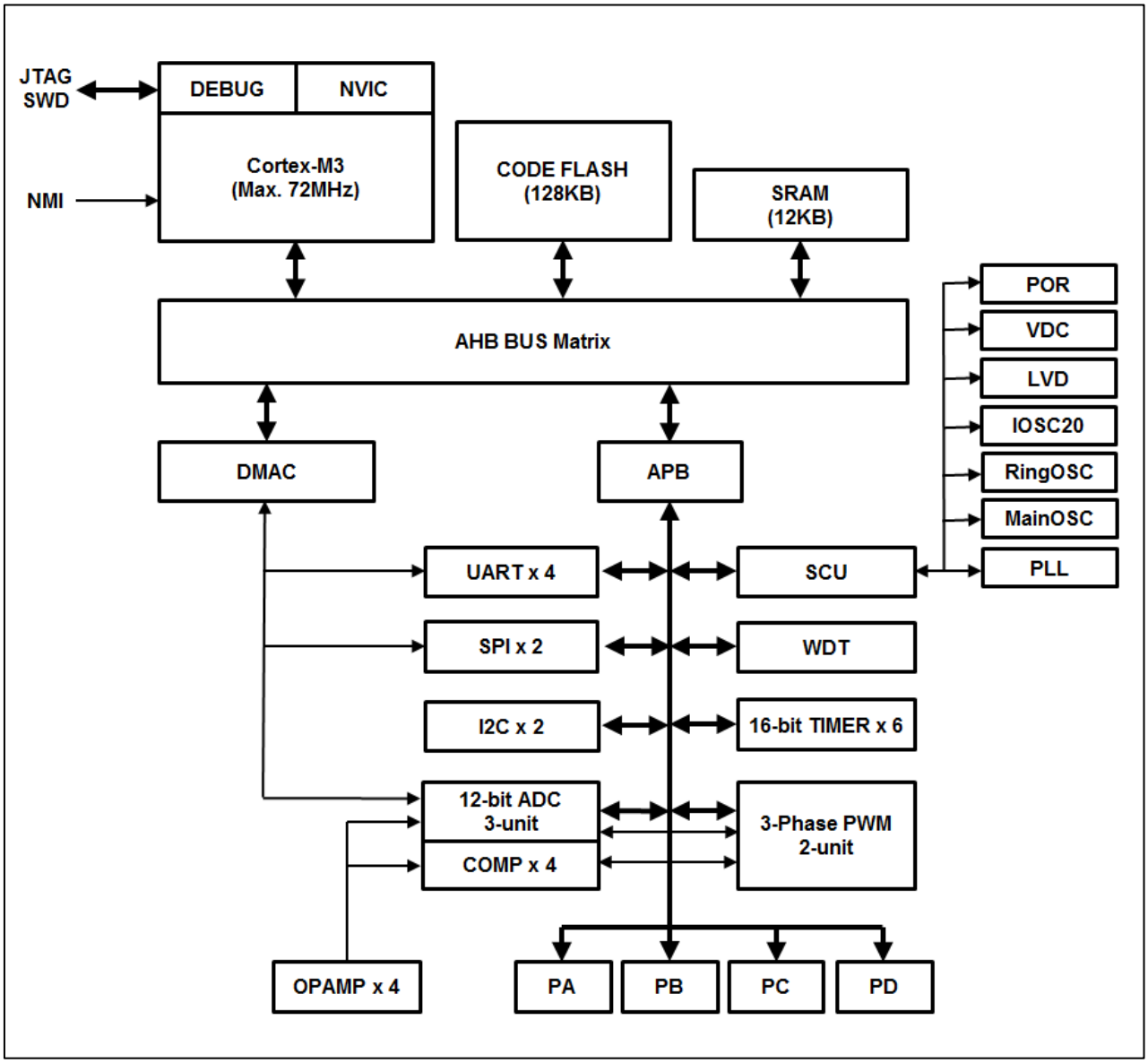

Figure1.5. Internal Block Diagram

1.3.2 Functional Description

The following section provides an overview of the features of AC33M8128 microcontroller.

ARM Cortex-M3

ARM powered Cortex-M3 Core based on v7M architecture which is optimized for small size and low power system.

On core system timer (SYSTICK) provides a simple 24 bit timer easy to manage the system operation

Thumb-compatible Thumb-2 only instruction set processor core makes code high-density.

Hardware division and single-cycle multiplication is present

Integrated Nested Vectored Interrupt Controller (NVIC) providing deterministic interrupt handling.

Full feature of debug solution is provided – JTAG and SWD, FPB, DWT, ITM and TPIU.

Max 72MHz operating frequency with zero wait execution

Nested Vector-Interrupt Controller (NVIC)

The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M3 core is included which handles all the internal and external exceptions. When interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of interrupt service routine.

The vector is fetched in parallel to the state saving, which enables efficient interrupt entry.

The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoring.

128KB Internal Code Flash Memory

The AC33M8128 provides internal 128KB code flash memory and its controller. This is enough to program motor algorithm and general control the system. Self-programming is available and ISP and JTAG programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory.

12KB 0-wait Internal SRAM

On chip 12KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

Boot Logic

The smart boot logic supports the flash programming. The AC33M8128 can be entered by external boot pin and UART and SPI programming are available in boot mode. UART0 or SPI0 is used in boot mode communication.

System Control Unit (SCU)

The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (INTOSC, VDC and LVD)

32-bit Watchdog Timer (WDT)

The watchdog timer performs system monitoring function. It will generate internal reset or interrupt to notice abnormal status of the system.

Multi-purpose 16bit Timer

Six-channel 16-bit general purpose timers supports below functions.

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

PWM Generator

3-phase PWM generator 2 channels are implemented. 16 bit up/down counter with prescaler supports both of triangular and saw tooth waveform.

The PWM generate internal ADC trigger signal to measure the signal on time.

Dead time insertion and emergency stop functionality help that the chip and system are under safety conditions.

Serial Peripheral Interface (SPI)

Synchronous serial communication is provided with SPI block. The AC33M8128 has 2 channel SPI modules. It has DMA function supported by DMA controller. Transfer data moved to/from memory area without CPU operation.

Boot mode will use this SPI block to download flash program.

Inter-Integrated Circuit Interface (I^2C)

The AC33M8128 has 2 channel I^2C block and it support up to 400KHz I^2C communication. The master and the slave mode supported.

Universal Asynchronous Receiver/Transmitter (UART)

The AC33M8128 has 4 channels UART block. For accurate baud rate control, the fractional baud rate generator is provided.

It has DMA function supported by DMA controller. Transfer data moved to/from memory area without CPU operation.

General PORT I/Os

16 bits PA, PB, PC, PD ports are available and provide multiple functionality

- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Pull-up/Open-drain
- On chip Debounce Filter

12-bit Analog-to-Digital Converter (ADC)

3 built-in ADCs can convert analog signal up to 1usec conversion rate. 16-channel analog mux and OP-AMP provides various combinations from external analog signals.

Operational Amplifier (OPAMP)

4 built-in OPAMPs amplify analog signals up to x8.74 gain.

Analog Comparator (COMP)

4 built-in analog comparators.

1.4 Pin Description

Below pin configuration is temporary one and 16 pins are reserved for power/ground pair and dedicated pins. The configuration including pin ordering will be changed in the future.

Table1.2. Pin Description

Pin No			Pin Name	Type	Description	Remark
MQFP80	LQFP80	LQFP64				
1	79	63	VDD	P	VDD	
2	80	64	GND	P	Ground	
3	1	1	GND	P	Ground	
4	2	-	PD2	IOUS	PORT D Bit 2 Input/Output	
			MOSI1	I/O	SPI Channel 1 Master Out / Slave In	
5	3	-	PD3*	IOUS	PORT D Bit 3 Input/Output	
			MISOI1	I/O	SPI Channel 1 Master In / Slave Out	
6	4	2	PA0*	IOUS	PORT A Bit 0 Input/Output	
			AN0	IA	Analog Input 0	
			COMP0	IA	Comparator 0 Input	
7	5	3	PA1*	IOUS	PORT A Bit 1 Input/Output	
			AN1	IA	Analog Input1	
			COMP1	IA	Comparator 1 Input	
8	6	4	PA2*	IOUS	PORT A Bit 2 Input/Output	
			AN2	IA	Analog Input 2	
			COMP2	IA	Comparator 2 Input	
9	7	5	PA3*	IOUS	PORT A Bit 3 Input/Output	
			AN3	IA	Analog Input 3	
			COMP3	IA	Comparator 3 Input	
10	8	6	PA4*	IOUS	PORT A Bit 4 Input/Output	
			T0O	Output	Timer 0 Output	
			AN4	IA	Analog Input 4	
11	9	7	PA5*	IOUS	PORT A Bit 5 Input/Output	
			T1O	Output	Timer 1 Output	
			AN5	IA	Analog Input 5	
12	10	8	PA6*	IOUS	PORT A Bit 6 Input/Output	
			T2O	Output	Timer 2 Output	
			AN6	IA	Analog Input 6	
			CREF0	IA	Comparator 0 Reference Input	
13	11	9	PA7*	IOUS	PORT A Bit 7 Input/Output	
			TRACED3	Output	ETM Trace Data 3	
			T3O	Output	Timer 3 Output	
			AN7	IA	Analog Input 7	
			CREF3	IA	Comparator 3 Reference Input	
14	12	10	AGND	P	Analog Ground	
15	13	11	AVDD	P	Analog VDD	
16	14	12	PA8*	IOUS	PORT A Bit 8 Input/Output	
			TRACECLK	Output	ETM Trace Clock	
			AD0O	Output	ADC0 Start Signal	
			AN8	IA	Analog Input 8	
17	15	13	PA9*	IOUS	PORT A Bit 9 Input/Output	
			TRACED0	Output	ETM Trace Data 0	
			AD1O	Output	ADC1 Start Signal	
			AN9	IA	Analog Input 9	

18	16	14	PA10*	IOUS	PORT A Bit 10 Input/Output	
			TRACED1	Output	ETM Trace Data 1	
			AD2O	Output	ADC2 Start Signal	
			AN10	IA	Analog Input 10	
19	17	15	PA11*	IOUS	PORT A Bit 11 Input/Output	
			TRACED2	Output	ETM Trace Data 2	
			AN11	IA	Analog Input 11	
20	18	16	PA12*	IOUS	PORT A Bit 12 Input/Output	
			SS0	I/O	SPI0 Slave Select signal	
			AD2I	Input	ADC2 Start Input signal	
			AN12	IA	Analog Input 12	
21	19	-	PD4	IOUS	PORT D Bit 4 Input/Output	
			SCL1	Output	I²C Channel 1 SCL In/Out	
22	20	-	PD5	IOUS	PORT D Bit 5 Input/Ouput	
			SDA1	Output	I²C Channel 1 SDA In/Out	
23	21	17	VDD	P	VDD	
24	22	18	GND	P	Ground	
25	23	-	PD6*	IOUS	PORT D Bit 6 Input/Ouput	
			TXD2	Output	UART Channel 2 TxD Input	
			AD0I	Input	ADC0 Start Input signal	
26	24	-	PD7*	IOUS	PORT D Bit 7 Input/Ouput	
			RXD2	Input	UART Channel 2 RxD Input	
			AD1I	Input	ADC1 Start Input signal	
27	25	19	PA13*	IOUS	PORT A Bit 13 Input/Output	
			SCK0	I/O	SPI0 Data Clock Input/Output	
			AN13	IA	Analog Input 13	
28	26	20	PA14*	IOUS	PORT A Bit 14 Input/Output	
			MOSI0	I/O	SPI0 Master-Output/Slave-Input Data signal	
			AN14	IA	Analog Input 14	
29	27	21	PA15*	IOUS	PORT A Bit 15 Input/Output	
			MISO0	I/O	SPI0 Master-Input/Slave-Output Data signal	
			AN15	IA	Analog Input 15	
30	28	22	PB0	IOUS	PORT B Bit 0 Input/Output	
			PWM0H0	Output	PWM0 H0 Output	
31	29	23	PB1	IOUS	PORT B Bit 1 Input/Output	
			PWM0L0	Output	PWM0 L0 Output	
32	30	24	PB2	IOUS	PORT B Bit 0 Input/Output	
			PWM0H1	Output	PWM0 H1 Output	
33	31	25	PB3	IOUS	PORT B Bit 1 Input/Output	
			PWM0L1	Output	PWM0 L1 Output	
34	32	26	TEST	Input	Test-mode Input (Always tied 'L')	Pull-down
35	33	27	SCANMD	Input	Scan-mode Input (Always tied 'L')	Pull-down
36	34	28	PB4	IOUS	PORT B Bit 4 Input/Output	
			PWM0H2	Output	PWM0 H2 Output	
			T9C	I/O	Timer 9 Clock/Capture Input	
37	35	29	PB5	IOUS	PORT B Bit 5 Input/Output	
			PWM0L2	Output	PWM0 L2 Output	
			T9O	I/O	Timer 9 Output	
38	36	30	PB6	IOUS	PORT B Bit 6 Input/Output	
			PRTIN0	Input	PWM0 Protection Input signal 0	
			WDTO	Output	WDT Output	
39	37	31	PB7	IOUS	PORT B Bit 7 Input/Output	
			OVIN0	Input	PWM0 Over-voltage put signal 1	

			STBYO	Output	Power-down mode indication signal	
40	38	32	PB8	IOUS	PORT B Bit 8 Input/Output	
			PRTIN1	Input	PWM1 Protection Input signal 0	
			RXD3	Input	UART3 RXD Input	
41	39	-	PD8	IOUS	PORT D Bit 8 Input/Output	
			WDTO	Output	WDT Output	
42	30	-	PD9	IOUS	PORT D Bit 9 Input/Output	
			STBYO	Output	Power-down mode indication signal	
43	41	33	VDD	P	VDD	
44	42	34	GND	P	Ground	
45	43	35	PB9	IOUS	PORT B Bit 9 Input/Output	
			OVIN1	Input	PWM1 Over-voltage Input signal 1	
			TXD3	Output	UART3 TXD Output	
46	44	36	PB10	IOUS	PORT B Bit 10 Input/Output	
			PWM1H0	Output	PWM Channel 1 Phase 0 H-side Output	
47	45	37	PB11	IOUS	PORT B Bit 11 Input/Output	
			PWM1L0	Output	PWM Channel 1 Phase 0 L-side Output	
48	46	38	PB12	IOUS	PORT B Bit 12 Input/Output	
			PWM1H1	Output	PWM Channel 1 Phase 1 H-side Output	
49	47	39	PB13	IOUS	PORT B Bit 13 Input/Output	
			PWM1L1	Output	PWM Channel 1 Phase 1 L-side Output	
50	48	40	PB14	IOUS	PORT B Bit 14 Input/Output	
			PWM1H2	Output	PWM Channel 1 Phase 2 H-side Output	
51	49	41	PB15	IOUS	PORT B Bit 15 Input/Output	
			PWM1L2	Output	PWM Channel 1 Phase 2 L-side Output	
52	50	42	GND	P	Ground	
53	51	43	VDD	P	VDD	
54	52	44	PC0	IOUS	PORT C Bit 0 Input/Output	
			TCK/SWCK	Input	JTAG TCK, SWD Clock Input	
55	53	45	PC1	IOUS	PORT C Bit 1 Input/Output	
			TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
56	54	-	PD10	IOUS	PORT D Bit 10 Input/Output	
			AD0SOC	Output	ADC0 Start-of-Conversion	
			T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
57	55	-	PD11	IOUS	PORT D Bit 10 Input/Output	
			AD0EOC	Output	ADC0 End-of-Conversion	
			T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
58	56	46	NMI	Input	Non-maskable Interrupt Input	
59	57	-	PD12	IOUS	PORT D Bit 12 Input/Output	
			AD1SOC	Output	ADC1 Start-of-Conversion	
			T2C/PHZ0	Input	Timer 2 Clock/Capture/Phase-Z Input	
60	58	-	PD13	IOUS	PORT D Bit 13 Input/Output	
			AD1EOC	Output	ADC1 End-of-Conversion	
			T3C	Input	Timer 3 Clock/Capture Input	
61	59	47	VDD	P	VDD	
62	60	48	GND	P	Ground	
63	61	49	PC2	IOUS	PORT C Bit 2 Input/Output	
			TDO/SWO	Output	JTAG TDO, SWO Output	
64	62	50	PC3	IOUS	PORT C Bit 3 Input/Output	
			TDI	Input	JTAG TDI Input	
65	63	51	PC4	IOUS	PORT C Bit 4Input/Output	
			nTRST	Input	JTAG nTRST Input	
			T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	

66	64	52	PC5	IOUS	PORT C Bit 5Input/Output	
			RXD1	Input	UART1 RXD Input	
			T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
67	65	53	PC6	IOUS	PORT C Bit 6Input/Output	
			TXD1	Output	UART1 TXD Output	
			T2C/PHZ	Input	Timer 2 Clock/Capture/Phase-Z Input	
68	66	54	PC7	IOUS	PORT C Bit 7Input/Output	
			SCL0	Output	I²C Channel 0 SCL In/Out	
			T3C	Input	Timer 3 Clock/Capture input	
69	67	55	PC8	IOUS	PORT C Bit 8 Input/Output	
			SDA0	Output	I²C Channel 0 SDA In/Out	
70	68	56	PC9	IOUS	PORT C Bit 9 Input/Output	
			CLKO	Output	System Clock Output	
			T8O	Output	Timer 8 Output	
71	69	57	PC10	IOUS	PORT C Bit 10 Input/Output	
			nRESET	Input	External Reset Input	Pull-up
72	70	58	PC11	IOUS	PORT C Bit 11 Input/Output	
			BOOT	Input	Boot mode Selection Input	
			T8C	Input	Timer 8 Clock/Capture Input	
73	71	-	PD14	IOUS	PORT D Bit 14 Input/Output	
			AD2SOC	Output	ADC2 Start-of-Conversion Output signal	
74	72	-	TD15	IOUS	PORT D Bit 15 Input/Output	
			AD2EOC	Output	ADC2 Start-of-Conversion Output signal	
75	73	59	PC15	IOUS	PORT C Bit 14 Input/Output	
			TXD0	Output	UART0 TXD Output	
			MISO0	I/O	SPI0 Master-Input/Slave-Output	
76	74	60	PC14	IOUS	PORT C Bit 14 Input/Output	
			RXD0	Input	UART0 RXD Input	
			MOSI0	I/O	SPI0 Master-Output/Slave-Input	
			VMARGIN	OA	Not used. (test purpose)	
77	75	61	PC13	IOUS	PORT C Bit 13 Input/Output	
			XOUT	OA	External Crystal Oscillator Output	
78	76	62	PC12	IOUS	PORT C Bit 12 Input/Output	
			XIN	IA	External Crystal Oscillator Input	
79	77	-	PD0	IOUS	PORT D Bit 0 Input/Output	
			SS1	I/O	SPI1 Slave Select	
80	78	-	PD1	IOUS	PORT D Bit 1 Input/Output	
			SCK1	I/O	SPI1 Clock Input/Output	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

1.5 Memory Map

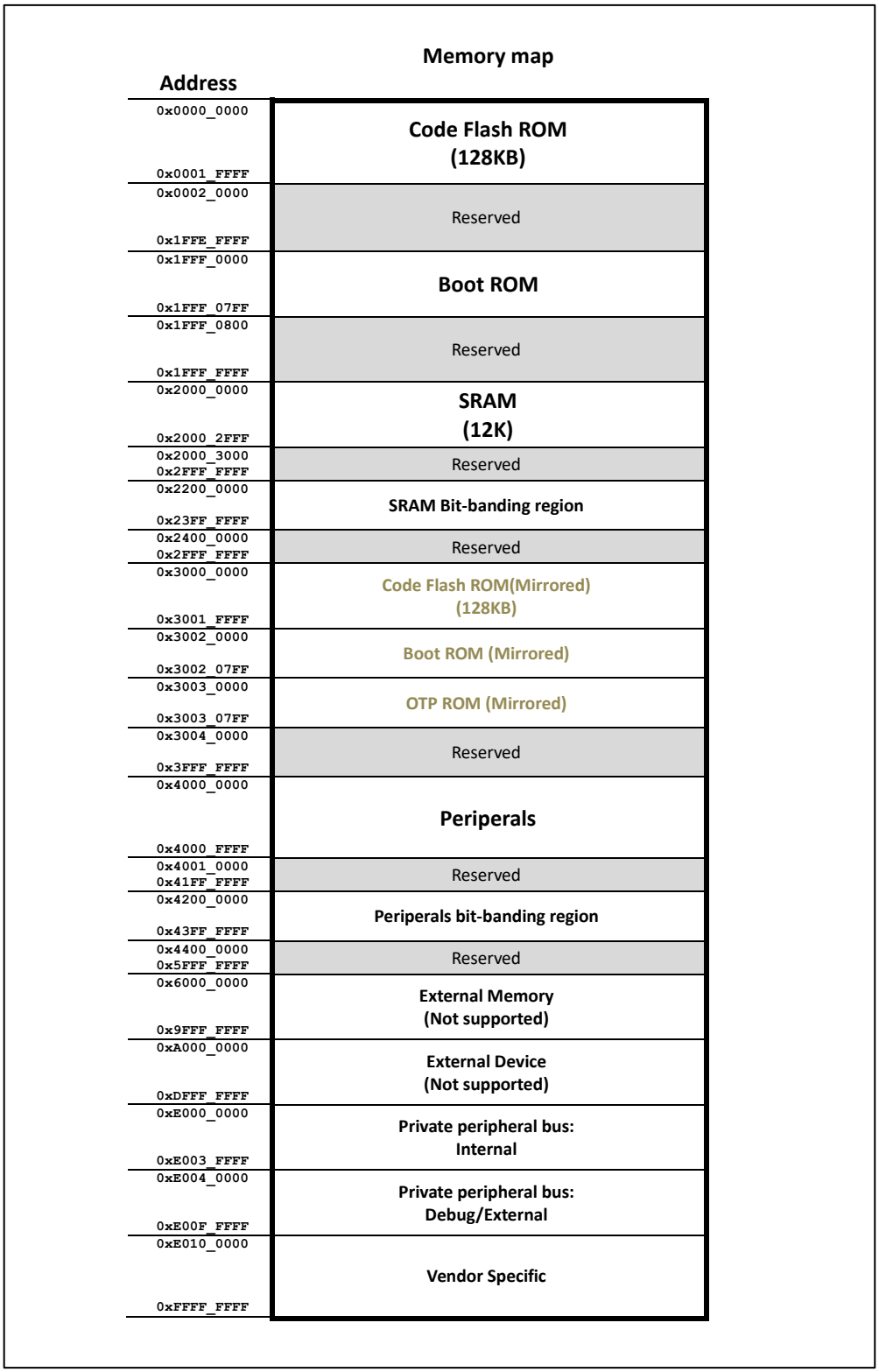

Figure1.6. Main Memory MAP

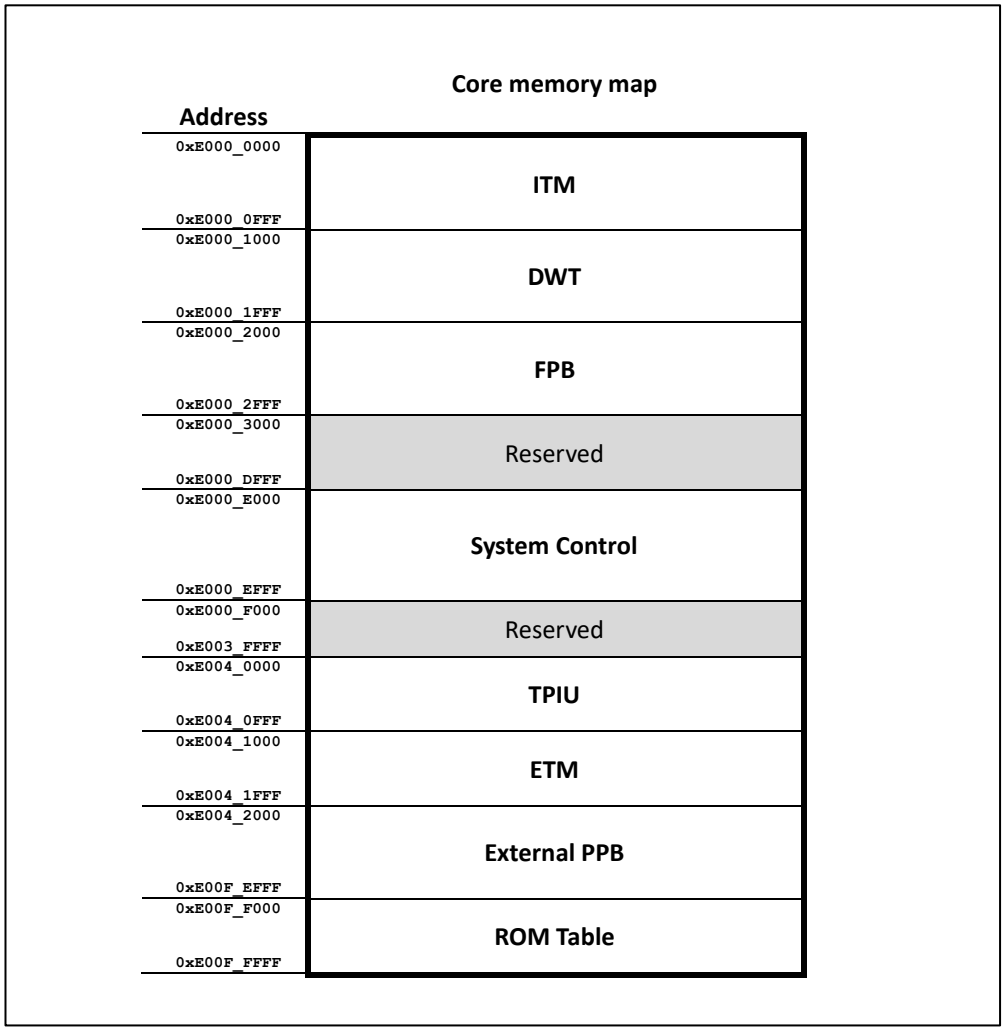

Figure1.7. Cortex-M3 Private Memory Map

Address	Peripheral map
0x4000_0000	SCU
0x4000_0100	FMC
0x4000_0200	WDT
0x4000_0300	Reserved
0x4000_0400	DMAC(15)
0x4000_0500	Reserved
0x4000_1000	PCU
0x4000_2000	GPIO(A,B,C,D)
0x4000_3000	TIMER(6)
0x4000_4000	MPWM0
0x4000_5000	MPWM1
0x4000_6000	Reserved
0x4000_8000	UART0
0x4000_8100	UART1
0x4000_8200	UART2
0x4000_8300	UART3
0x4000_8600	Reserved
0x4000_9000	SPI0
0x4000_9100	SPI1
0x4000_9200	Reserved
0x4000_A000	I^2C0
0x4000_A100	I^2C1
0x4000_A200	Reserved
0z4000_B000	ADC0
0x4000_B100	ADC1
0x4000_B200	ADC2
0x4000_B300	AFE
0x4000_B400 0x4000_FFFF	Reserved

Figure1.8. Peripheral Memory Map

CHAPTER 2. CPU

2.1 Cortex-M3 Core

CPU core is supported from the ARM Cortex-M3 processor which provides a high-performance, low-cost platform.

Document DDI337 from ARM provides detail information of Cortex-M3.

2.2 Interrupt Controller

Table2.1. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MPU Fault Handler
-11	0x0000_0014	BUS Fault Handler
-10	0x0000_0018	Usage Fault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVDDETECT
1	0x0000_0044	SCLKFAIL
2	0x0000_0048	XOSCFAIL
3	0x0000_004C	WDT
4	0x0000_0050	Reserved
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	Reserved
10	0x0000_0068	
11	0x0000_006C	
12	0x0000_0070	
13	0x0000_0074	TIMER8
14	0x0000_0078	TIMER9
15	0x0000_007C	Reserved
16	0x0000_0080	GPIOAE
17	0x0000_0084	GPIOAO
18	0x0000_0088	GPIOBE
19	0x0000_008C	GPIOBO
20	0x0000_0090	GPIOCE
21	0x0000_0094	GPIOCO
22	0x0000_0098	Reserved
23	0x0000_009C	GPIODO

24	0x0000_00A0	MPWM0
25	0x0000_00A4	MPWM0PROT
26	0x0000_00A8	MPWM0OVV
27	0x0000_00AC	MPWM1
28	0x0000_00B0	MPWM1PROT
29	0x0000_00B4	MPWM1OVV
30	0x0000_00B8	Reserved
31	0x0000_00BC	
32	0x0000_00C0	SPI0
33	0x0000_00C4	SPI1
34	0x0000_00C8	Reserved
35	0x0000_00CC	
36	0x0000_00D0	I2C0
37	0x0000_00D4	I2C1
38	0x0000_00D8	UART0
39	0x0000_00DC	UART1
40	0x0000_00E0	UART2
41	0x0000_00E4	UART3
42	0x0000_00E8	Reserved
43	0x0000_00EC	ADC0
44	0x0000_00F0	ADC1
45	0x0000_00F4	ADC2
46	0x0000_00F8	COMP0
47	0x0000_00FC	COMP1
48	0x0000_0100	COMP2
49	0x0000_0104	COMP3
50	0x0000_0108	Reserved
51	0x0000_010C	
52	0x0000_0110	
53	0x0000_0114	
54	0x0000_0118	
55	0x0000_011C	
56	0x0000_0120	
57	0x0000_0124	
58	0x0000_0128	
59	0x0000_012C	
60	0x0000_0130	
61	0x0000_0134	
62	0x0000_0138	
63	0x0000_013C	

CHAPTER 3. Boot Mode

3.1 Boot Mode Pins

AC33M8128 has boot mode option to program internal flash memory.

Boot mode can be entered by setting BOOT pin to ‘L’ at reset timing. (Normal state is ‘H’)

The boot mode supports UART boot and SPI boot.

UART boot uses UART0 port, and SPI boot uses SPI0.

The pins for boot mode are listed as following:

Table3.1. Boot mode pin list

Block	Pin Name	Dir	Description
SYSTEM	**nRESET/PC10**	I	Reset Input signal
	BOOT/PC11	I	‘0’ to enter Boot mode
UART0	**RXD0/PC14**	I	UART Boot Receive Data
	TXD0/PC15	O	UART Boot Transmit Data
SPI0	**SS0/PA12**	I	SPI Boot Slave Select
	SCK0/PA13	I	SPI Boot Clock Input
	MOSI0/PA14	I	SPI Boot Data Input
	MISO0/PA15	O	SPI Boot Data Output

3.2 Boot Mode Connections

User can design target board using any of boot mode ports – UART or SPI.

Followings are sample connection diagrams of boot mode.

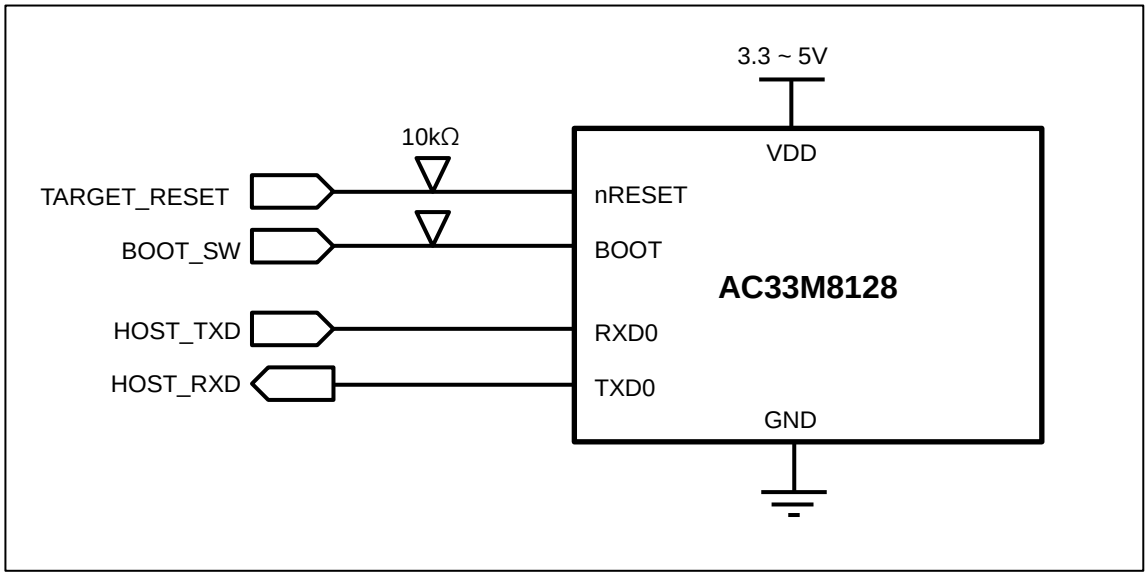

Figure3.1. Connection diagram of UART Boot

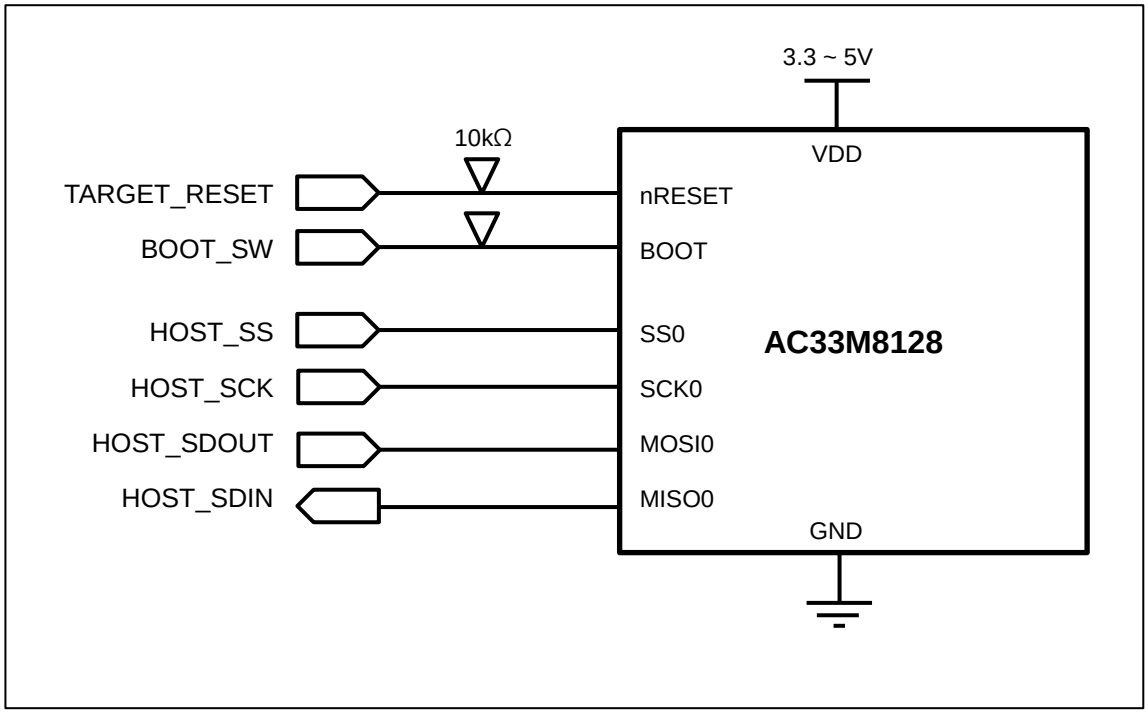

Figure3.2. Connection diagram of SPI Boot

CHAPTER 4. SYSTEM CONTROL UNIT (SCU)

4.1 OVERVIEW

The AC33M8128 has built-in intelligent power control block which manages system analog blocks and operating modes

Internal reset and clock signals are controlled by SCU block to maintain optimize system performance and power dissipation.

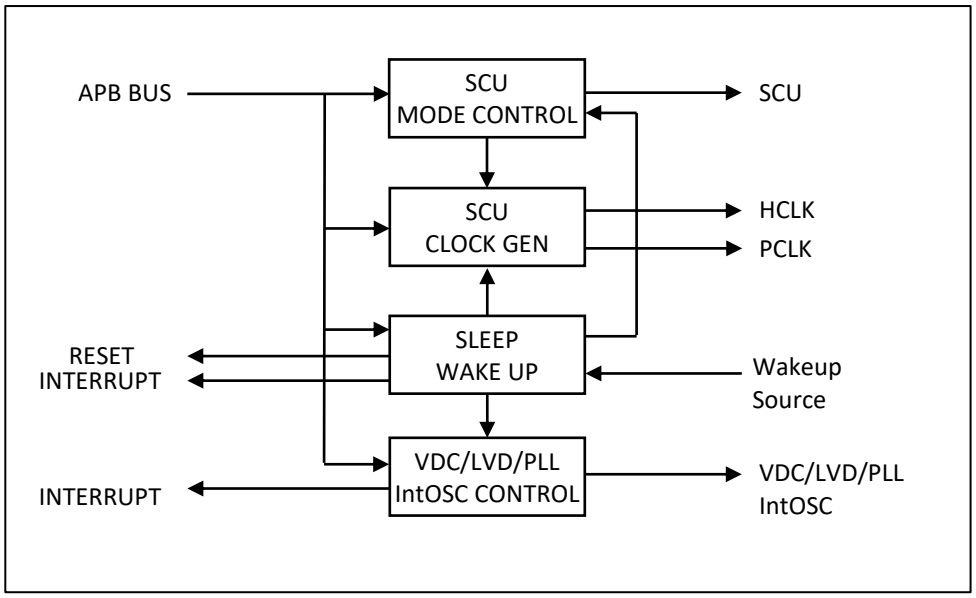

Figure4.1. SCU Block Diagram

4.2 CLOCK SYSTEM

AC33M8128 has two main operating clocks. One is HCLK which supplies the clock to CPU and AHB bus system. The other one is PCLK which supplies the clock to Peripheral systems.

User can control the clock system variation by software. Figure 4.2 shows the clock system of the chip. And Table 4.1 shows clock source descriptions.

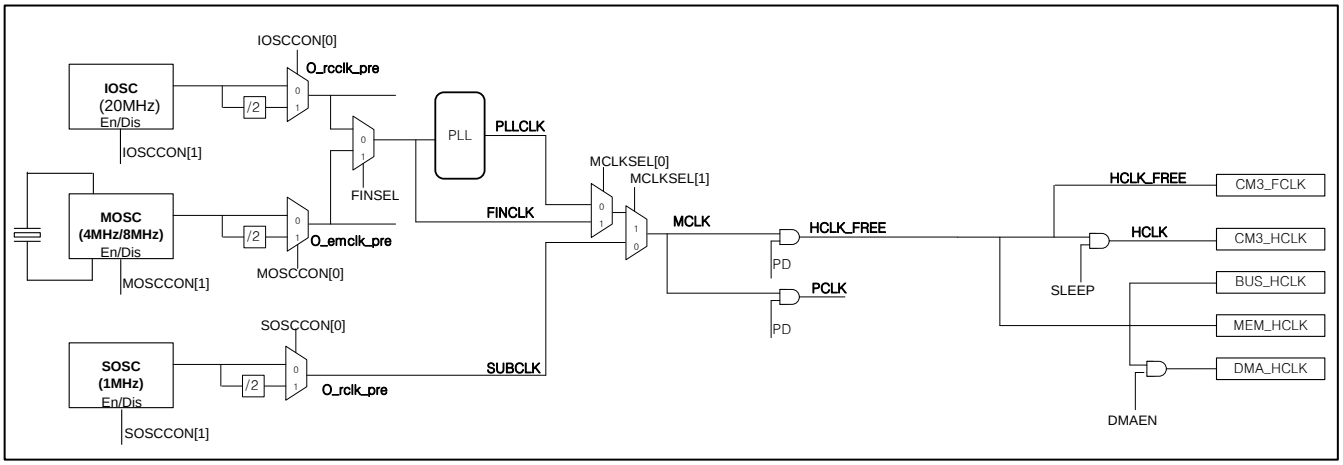

Figure 4.2. System clock configuration

All the mux to switch clock source have a glitch-free circuit in each. So clock can be switched without glitch risks.

Table4.1. Clock sources

Clock name	Frequency	Description
IOSC20	20MHz	Internal OSC
MainOSC	X-TAL(4MHz~8MHz)	External Crystal IOSC
PLL Clock	8MHz ~ 72MHz	On Chip PLL
ROSC	1MHz	Internal RING OSC

The PLL can synthesize PLLCLK clock up to 72MHz with FIN reference clock. It also has internal pre-divider and post-divider.

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M3 CPU requires 2 clocks related with HCLK clock. FCLK and HCLK. FCLK is free running clock and it is always running except power down mode. HCLK can be stopped in the idle mode.

4.2.2 Miscellaneous clock domain for Cortex-M3

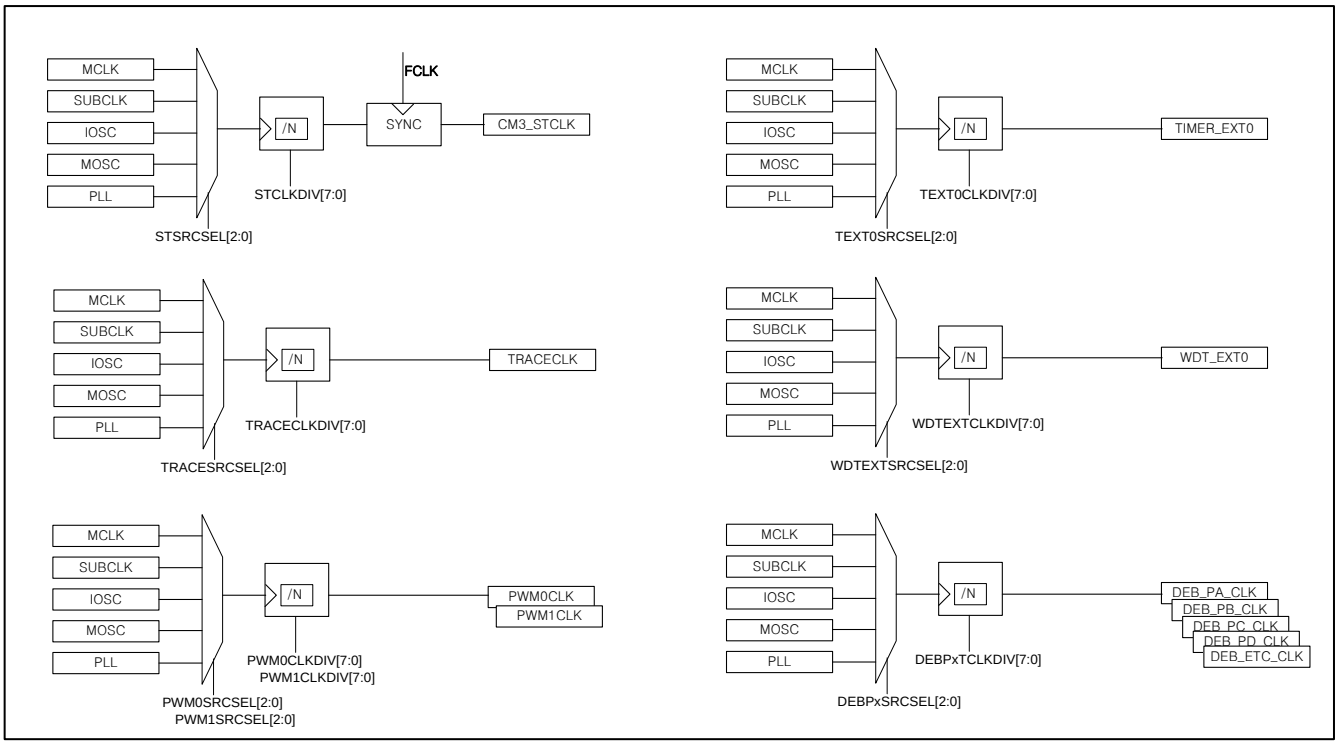

Figure 4.3. Miscellaneous clock configuration

4.2.3 PCLK clock domain

PCLK is master clock of all the peripherals. It can be stopped in powerdown mode. Each peripheral clocks generated by PCER register set.

4.2.4 Clock configuration procedure

After power up, the defulat system clock is feed by RINGOSC (1MHz) clock. RINGOSC is default enabled at power up sequence. The other clock sources will be enabled by user controls with the RINGOSC system clock.

MOSC clock can be enabled by CSCR register. Before enable MOSC block, the pin mux configuration should be set for XIN, XOUT function. PC12 and PC13 pins are shared with MOSC's XIN and XOUT function - PCCMR and PCCCR registers should be configured properly. After enabling the MOSC block, you must wait for more than 1msec time to ensure stable operation of crystal oscillation.

PLL clock can be enabled by PLLCON register. After enabling the PLL block, you must wait for pll lock flag. PLL output clock is stable, you can select MCLK for your system requirement. Before changing the system clock, flash access wait should be set to the maximum value. After the system clock is changed, you will need to set flash access wait that you want if necessary.

You can find an example flow chart to configure the system clock in Figure 4.4

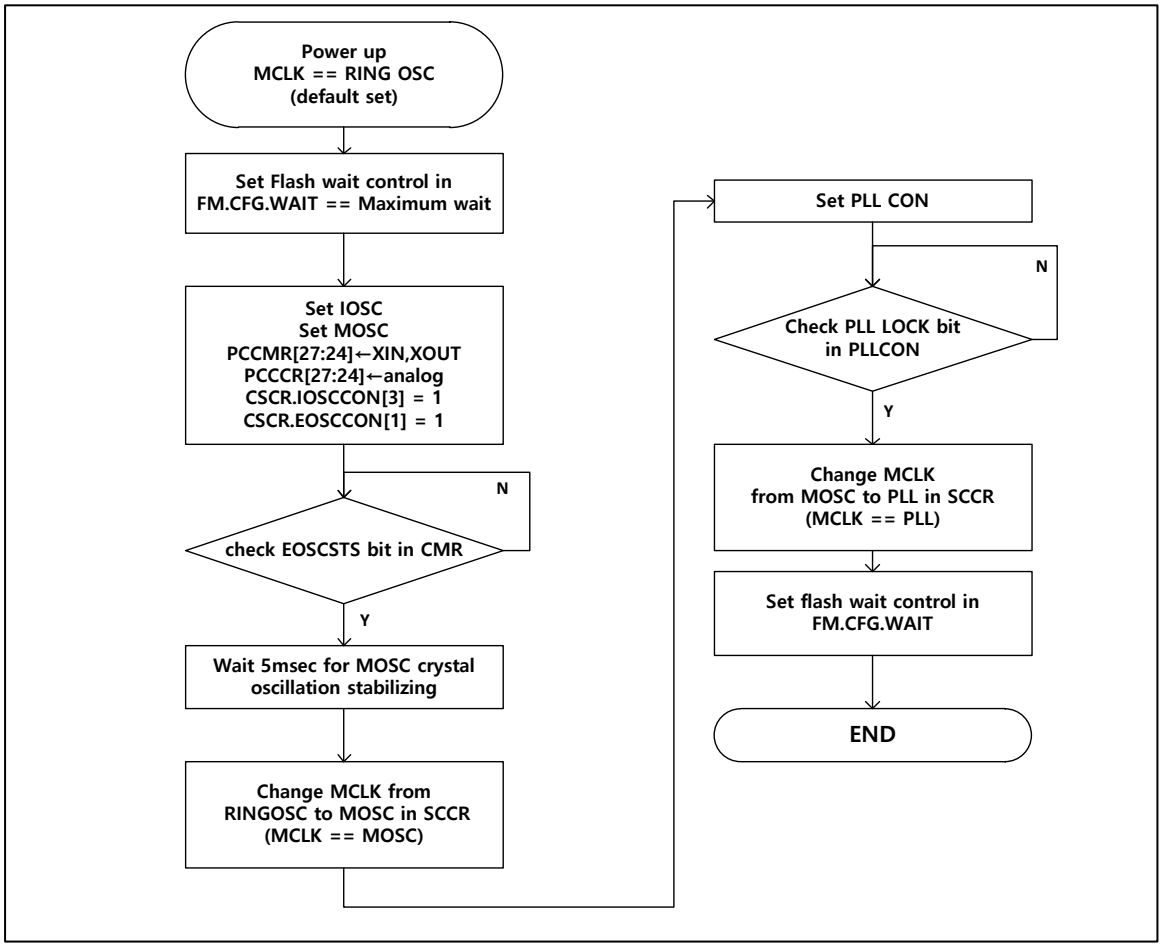

Figure 4.4. Clock configuration procedure

4.3 RESET

AC33M8128 has two system reset. One is the cold reset by POR which is effective during power up or down sequence. The other reset is the warm reset which is generated by several reset sources. The reset event make the chip to turn initial state.

The cold reset has only one reset source which is POR.

The warm reset has several reset sources as below

- nRESET pin
- WDT reset
- LVD reset
- MCLK Fail reset
- MOSC Fail reset
- S/W reset
- CPU request reset

4.3.1 The Cold Reset

The cold reset is important feature of the chip when power is up. This characteristic will globaly affect the system boot. Internal VDC is enabled when VDD power is turn on. Internal VDD level slope will follow by External VDD power slope. Internal PoR trigger level is 1.4V of internal VDC voltage out level. At this time, boot operation is started. The ringosc clock is enabled and counts 4msec time for internal VDC level stabilizing. In this time, external VDD voltage level should be over than initial LVD level (2.3V). After 4msec counting , the CPU reset is released and start the operation.

The figure 4.5 shows power up sequence and internal reset waveform.

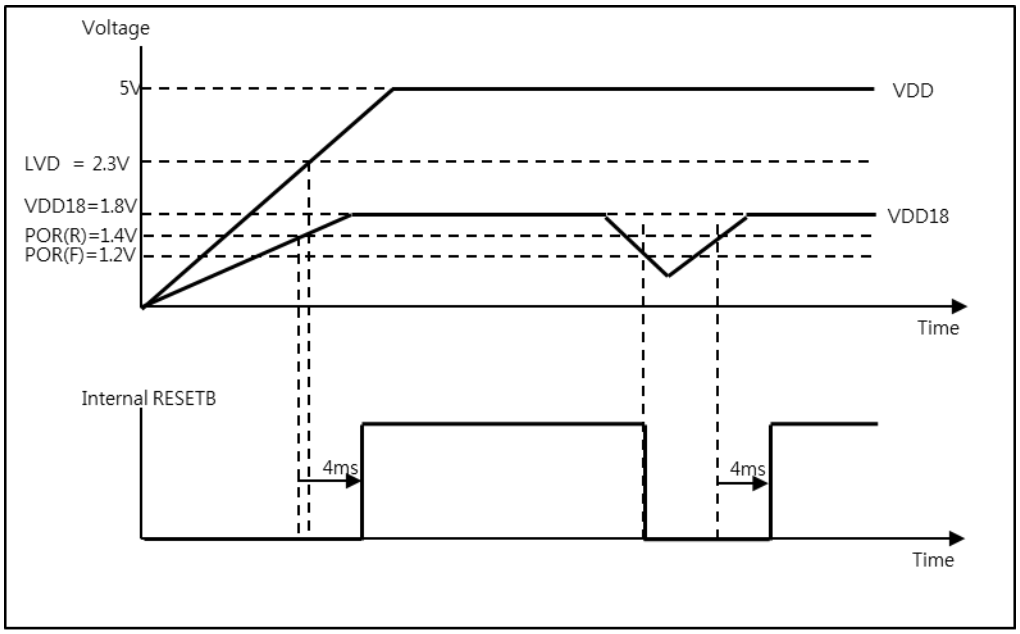

Figure 4.5. Power-up POR sequence

RSSR register shows the POR reset status. The last reset is come from POR, RSSR.PORST is set to “1”. After power up, this bit is always “1”. If abonormal internal voltage drop is occurred during normal operation, the system will be reset and this bit also set to “1”.

When the cold reset applied, all the chip returns to initial state.

4.3.2 The Warm Reset

The warm reset event has several reset sources and some parts of chip returns to itinial state when warm reset codition is occurred.

The wram reset source is controlled by RSER register and the status is appeared in RSSR register. The reset for each peripheral blocks is controlled by PRER register. The reset can be masked independently.

The CM3_SYSRESETn signal resets the processor excluding debug logics in the processor.

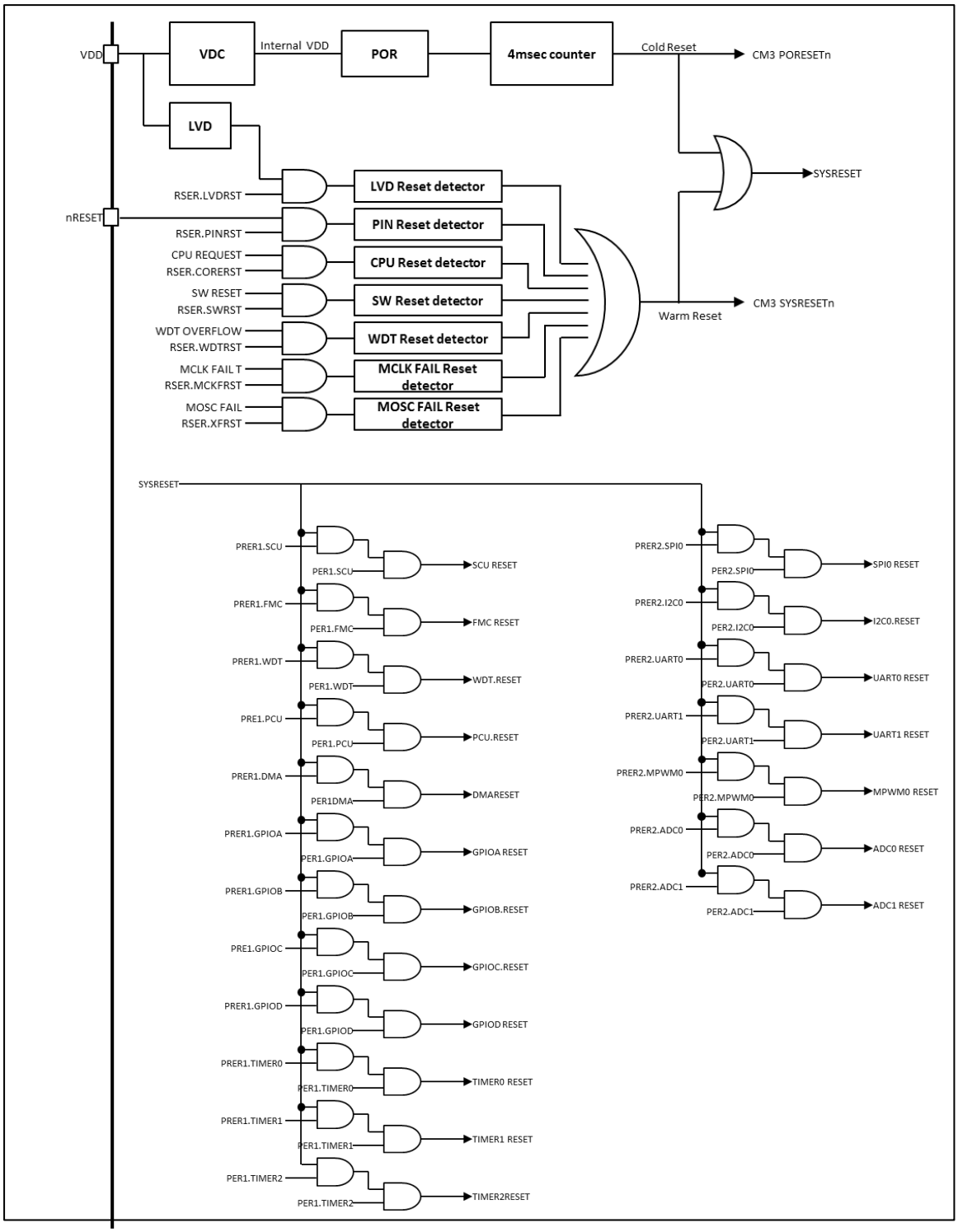

Figure 4.6. Reset configuration

4.4 OPERATION MODE

The INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals.

Figure 4.5 shows the operation mode transition diagram.

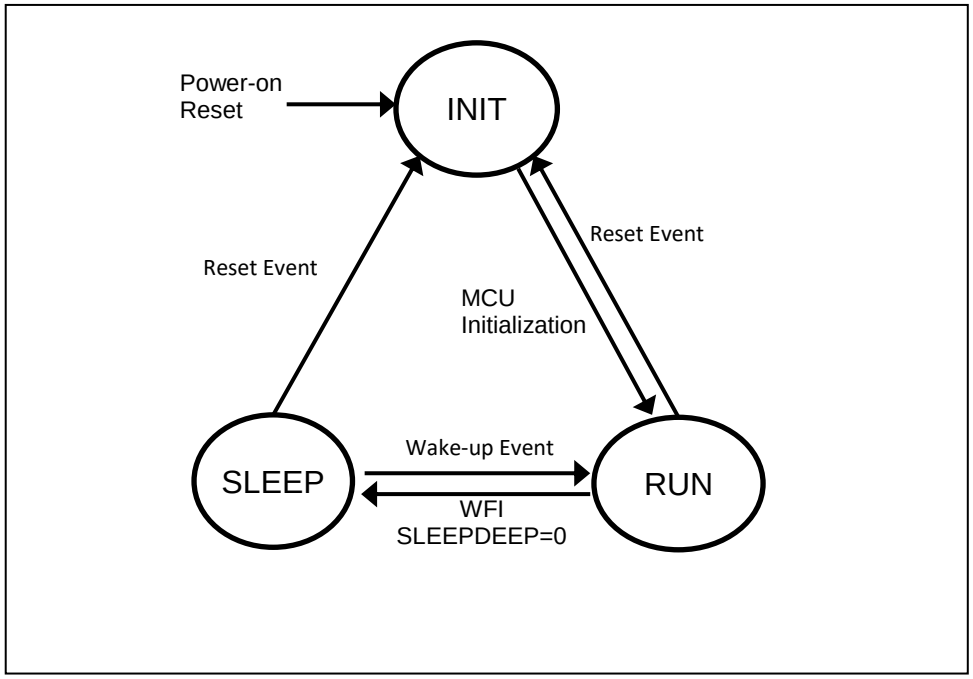

Figure4.7. Operating Mode

4.4.1 RUN Mode

This mode is to operate the CPU core and the peripheral hardware by using the high-speed clock. After reset followed by INIT state, it is entered into RUN mode.

4.4.2 SLEEP Mode

Only the CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.

4.5 PIN DESCRIPTION

Table4.2. SCU and PLL pins

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
STBYO	O	Stand-by Output Signal
CLKO	O	Clock Output Monitoring Signal

CHAPTER 5. PORT CONTROL UNIT (PCU)

5.1 OVERVIEW

PCU(Port Control Unit) controls the external I/Os as below

- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up register control and open drain control

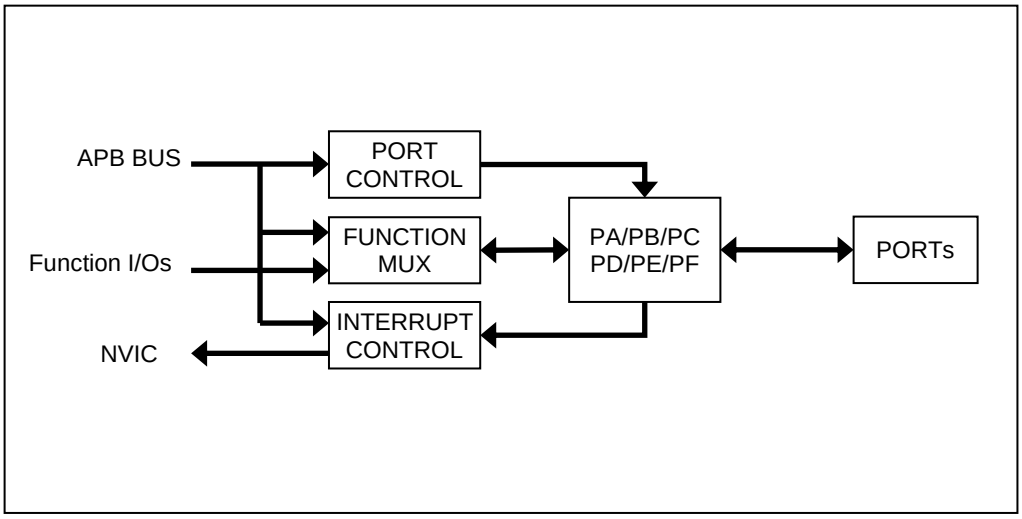

Figure5.1. Block Diagram

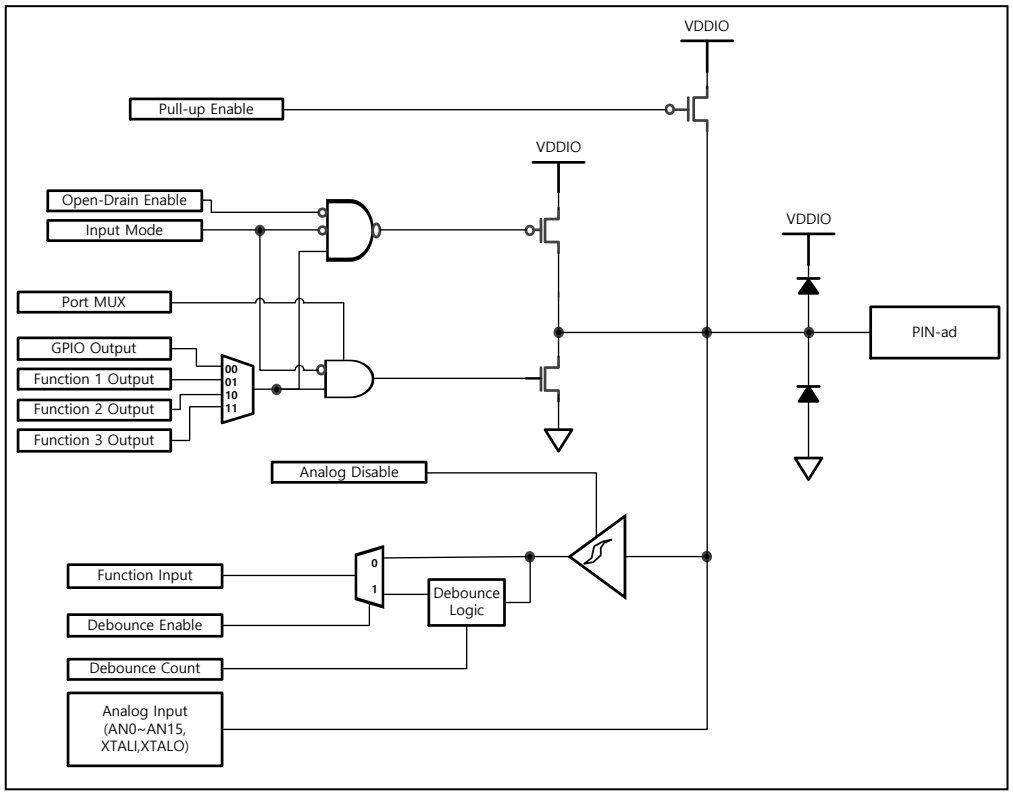

Figure5.2. I/O Port Block Diagram (ADC and External Oscillator pins)

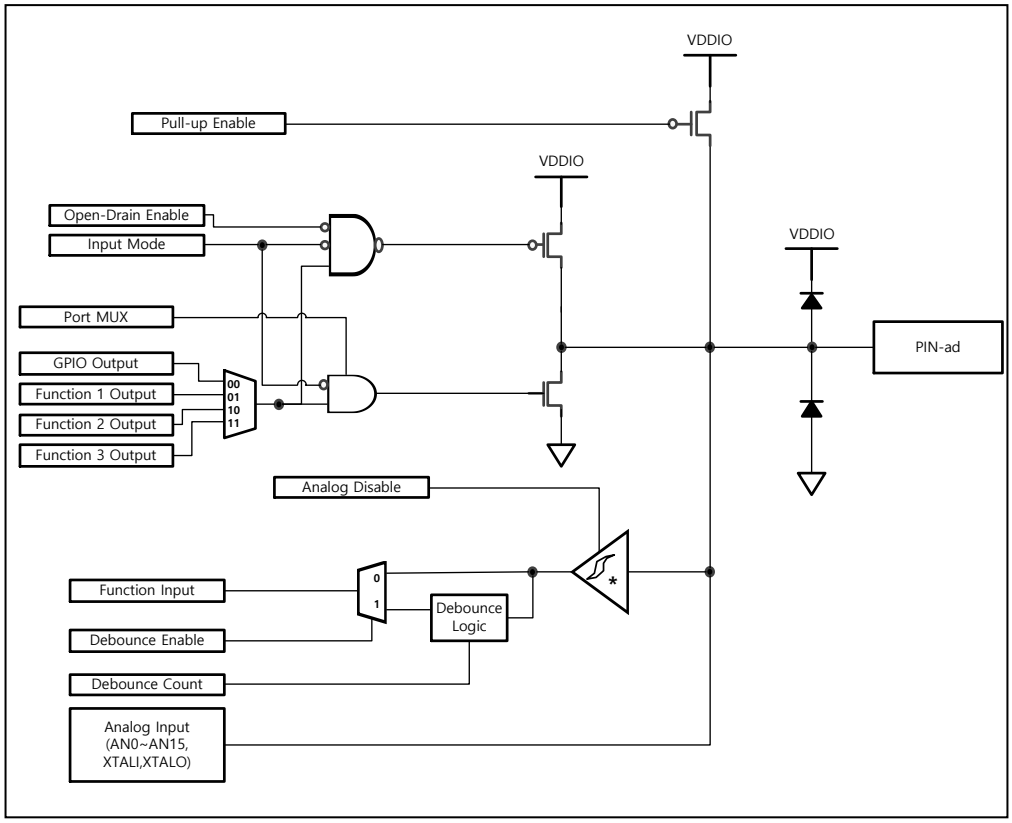

Figure5.3. I/O Port Block Diagram (General I/O pins)

5.2 Pin Multiplexing

GPIO pins have alternative function pins. Below table shows pin multiplexing information.

Table 5.1. GPIO Alternative function

PORT		FUNCTION			
		00	01	10	11
PA	0	**PA0***			AIN0/COMP0
	1	**PA1***			AIN1/COMP1
	2	**PA2***			AIN2/COMP2
	3	**PA3***			AIN3/COMP3
	4	**PA4***		T0O	AIN4
	5	**PA5***		T1O	AIN5
	6	**PA6***		T2O	AIN6/CREF0
	7	**PA7***	TRACED3	T3O	AIN7/CREF3
	8	**PA8***	TRACECLK	AD0O	AIN8
	9	**PA9***	TRACED0	AD1O	AIN9
	10	**PA10***	TRACED1	AD2O	AIN10
	11	**PA11***	TRACED2		AIN11
	12	**PA12***	SS0	AD2I	AIN12
	13	**PA13***	SCK0		AIN13
	14	**PA14***	MOSI0		AIN14
	15	**PA15***	MISO0		AIN15
PB	0	**PB0***	PWM0H0		
	1	**PB1***	PWM0L0		
	2	**PB2***	PWM0H1		
	3	**PB3***	PWM0L1		
	4	**PB4***	PWM0H2	T9C	
	5	**PB5***	PWM0L2	T9O	
	6	**PB6***	PRTIN0	WDTO[2]	
	7	**PB7***	OVIN0	STBYO[2]	
	8	**PB8***	PRTIN1	RXD3	
	9	**PB9***	OVIN1	TXD3	
	10	**PB10***	PWM1H0		
	11	**PB11***	PWM1L0		
	12	**PB12***	PWM1H1		
	13	**PB13***	PWM1L1		
	14	**PB14***	PWM1H2		
	15	**PB15***	PWM1L2		

(*) mark indicates default pin setting.
[2] mark indicates secondary port

Table5.2. GPIO Alternative function

PORT		FUNCTION			
		00	01	10	11
PC	0	PC0	**TCK/SWCLK***		
	1	PC1	**TMS/SWDIO***		
	2	PC2	**TDO/SWO***		
	3	PC3	**TDI***		
	4	PC4	**nTRST***	T0C/PHA(2)	
	5	**PC5***	RXD1	T1C/PHB(2)	
	6	**PC6***	TXD1	T2C/PHZ(2)	
	7	**PC7***	SCL0	T3C	
	8	**PC8***	SDA0		
	9	**PC9***	CLKO	T8O	
	10	PC10	**nRESET***		
	11	**PC11/BOOT***		T8C	
	12	**PC12***	XIN		
	13	**PC13***	XOUT		
	14	**PC14***	RXD0	MISO0(2)	
	15	**PC15***	TXD0	MOSI0(2)	
PD	0	**PD0***	SS1		
	1	**PD1***	SCK1		
	2	**PD2***	MOSI1		
	3	**PD3***	MISO1		
	4	**PD4***	SCL1		
	5	**PD5***	SDA1		
	6	**PD6***	TXD2	AD0I	
	7	**PD7***	RXD2	AD1I	
	8	**PD8***		WDTO	
	9	**PD9***		STBO	
	10	**PD10***	AD0SOC	T0C/PHA	
	11	**PD11***	AD0EOC	T1C/PHB	
	12	**PD12***	AD1SOC	T2C/PHZ	
	13	**PD13***	AD1EOC	T3C	
	14	**PD14***	AD2SOC		
	15	**PD15***	AD2EOC		

(*) mark indicates default pin setting.
(2) mark indicates secondary port

CHAPTER 6. GENERAL PURPOSE I/O (GPIO)

6.1 OVERVIEW

Most of pins except dedicated function pins can be used general I/O ports. General input/output ports are controlled by GPIO block.

- Output signal level (H/L) select
- Input signal level
- Output Set/Clear pin as writing '1'

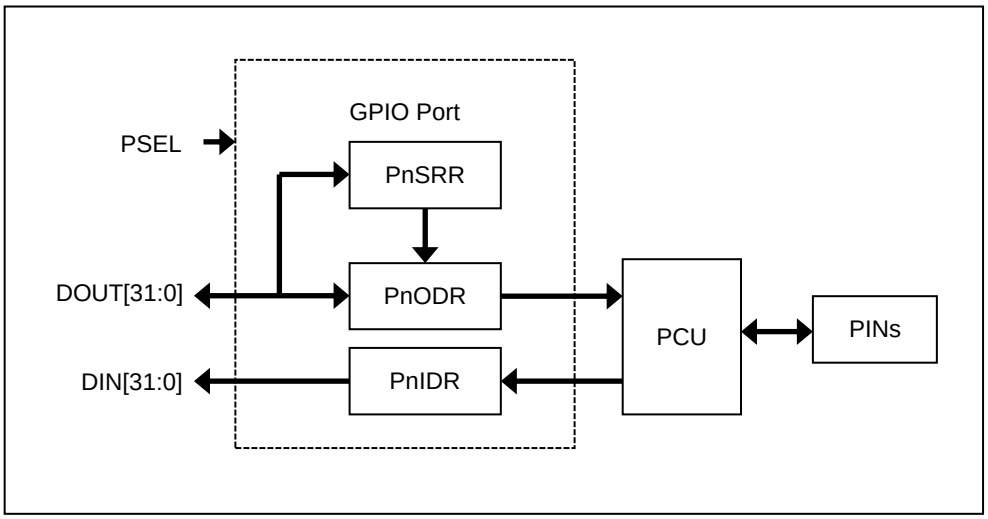

Figure6.1. Block diagram

6.2 Pin description

Table 6.1. External signal

PIN NAME	TYPE	DESCRIPTION
PA	IO	PA0 - PA15
PB	IO	PB0 - PB15
PC	IO	PC0 - PC15
PD	IO	PD0 - PD15

CHAPTER 7. FLASH MEMORY CONTROLLER

7.1 Flash Memory Controller Introduction

Flash Memory Controller is an internal flash memory interface controller.

- 128KB Flash code memory
- 32-bit read data bus width
- Code cache block for fast access mode
- 128-byte page size
- Support page erase and sector erase
- 128-byte unit program

Table7.1. Internal flash specification

Item	Decription
Size	128KB
Start Address	0x0000_0000
End Address	0x0001_FFFF
Page Size	128-byte
Total Page Count	1,024 pages
PGM Unit	128-byte
Erase Unit	128-byte

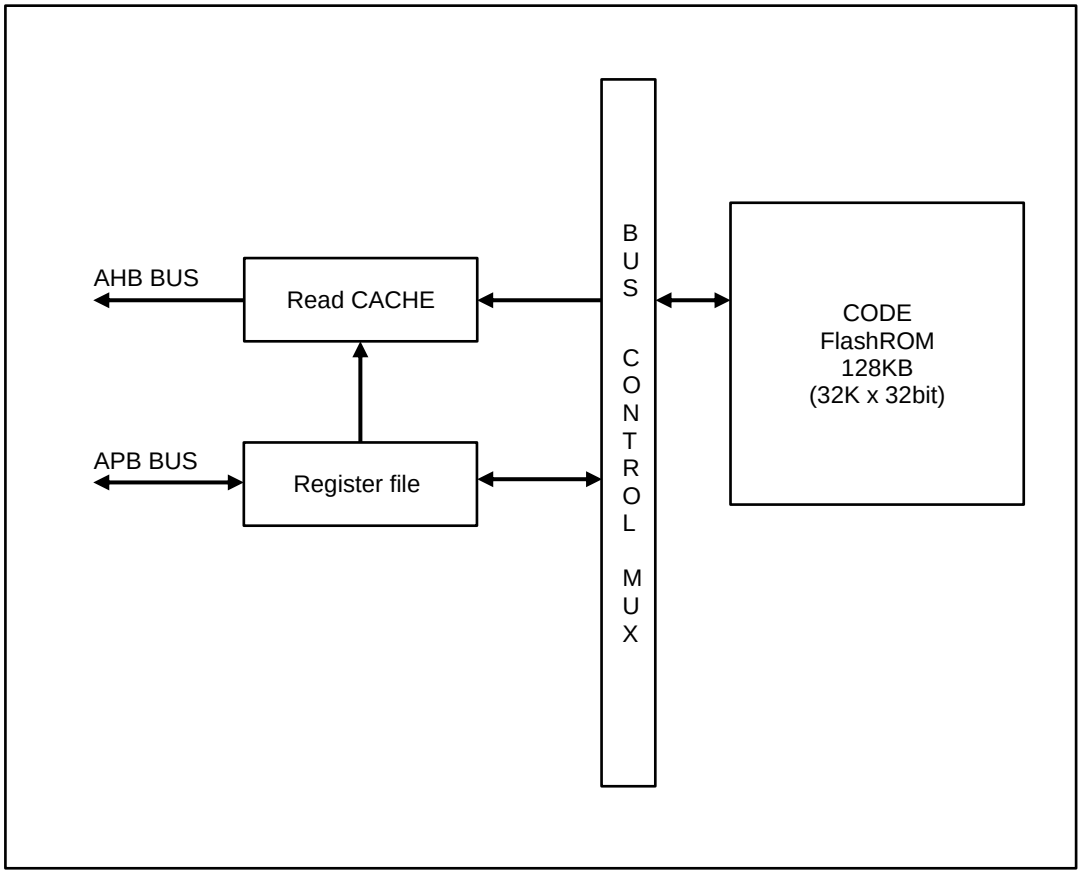

Figure7.1. Block Diagram

CHAPTER 8. INTERNAL SRAM

8.1 OVERVIEW

The AC33MX128 has a block of 0-wait on-chip SRAM. The size of SRAM is 12KB.

The SRAM base address is 0x2000_0000

The SRAM memory area usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/pgm operation.

This device does not support memory remap starategy. So jump and return is required to perform the code in SRAM memory area

CHAPTER 9. DIRECT MEMORY ACCESS CONTROLLER (DMAC)

9.1 DMAC Introduction

DMA is direct memory access controller

- 15 Channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through peripheral interrupt

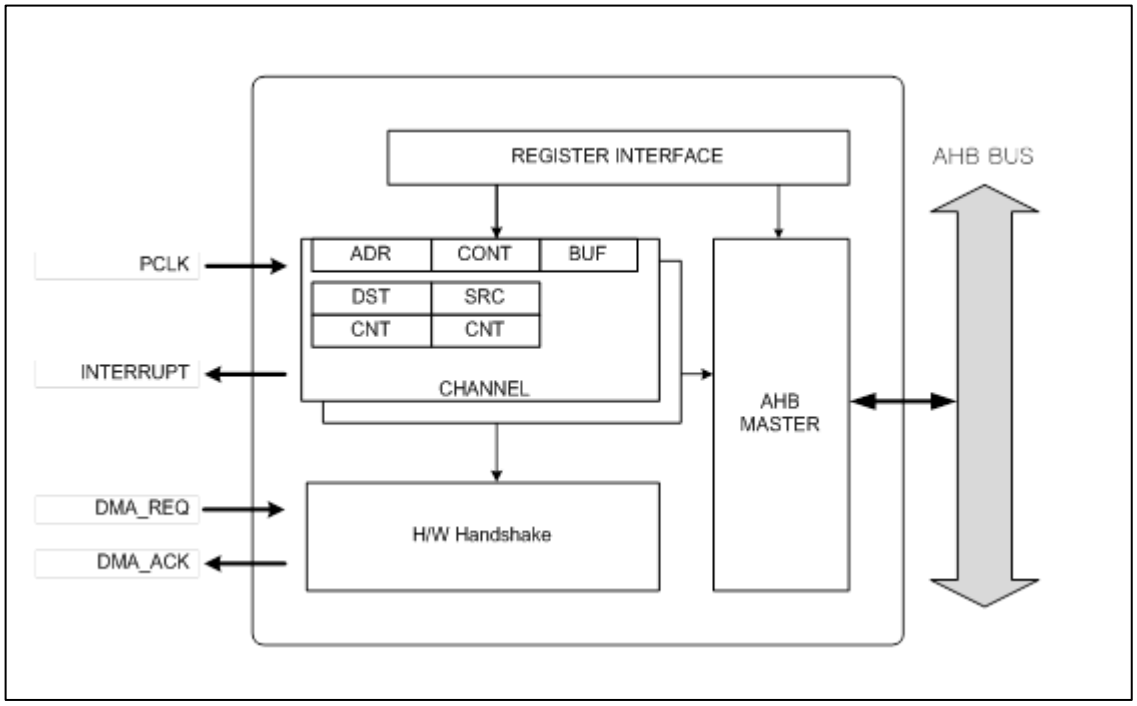

Figure9.1. Block Diagram

CHAPTER 10. WATCH-DOG TIMER (WDT)

10.1 OVERVIEW

The Watchdog timer can monitor the system and generate an interrupt or a reset. It has 32-bit down-counter.

- 32bit down counter (WDTCVR)
- Select reset or periodic interrupt
- Count clock selection
- Dedicated pre-scaler
- Watchdog overflow output signal

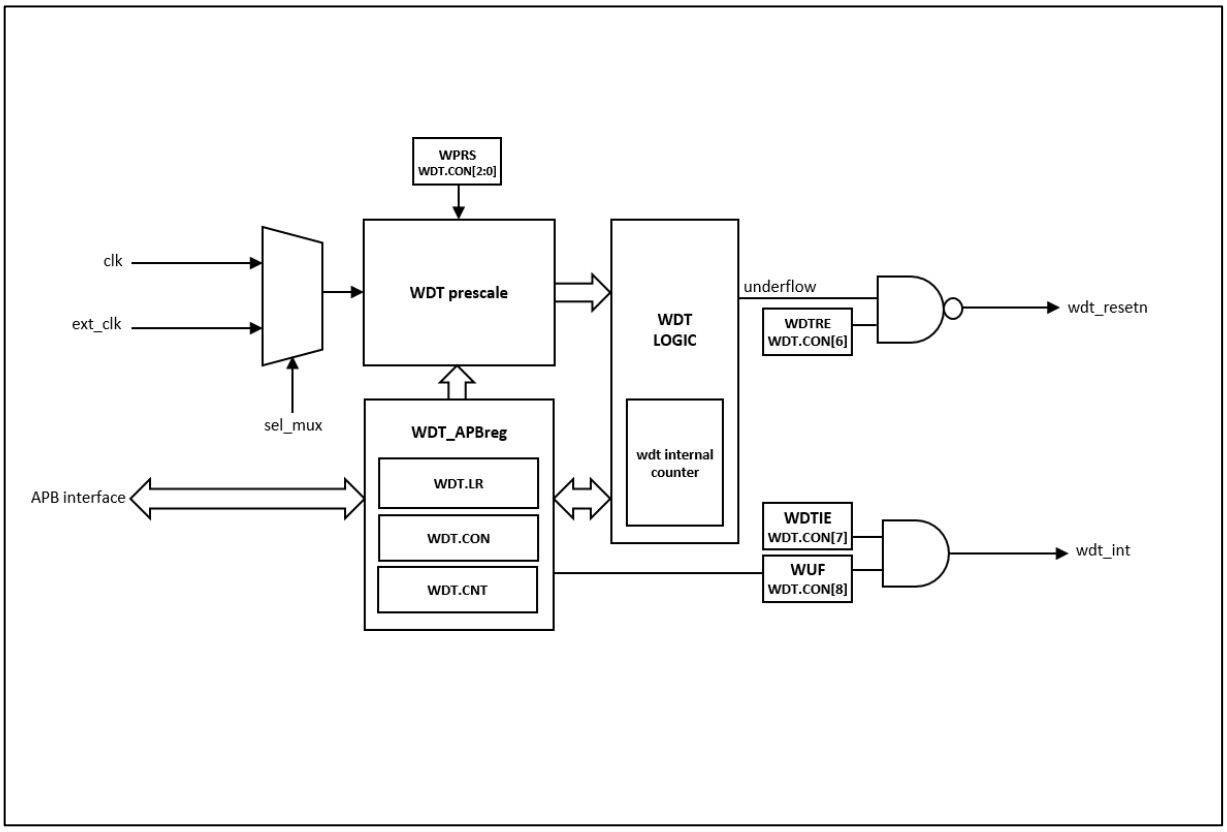

Figure10.1. Block diagram

CHAPTER 11. 16-BIT TIMER

11.1 OVERVIEW

The timer block is consisted with 6 channels of 16 bit General purpose timers. They can support periodic timer, PWM pulse, one-shot timer and capture mode.

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 10-bit prescaler

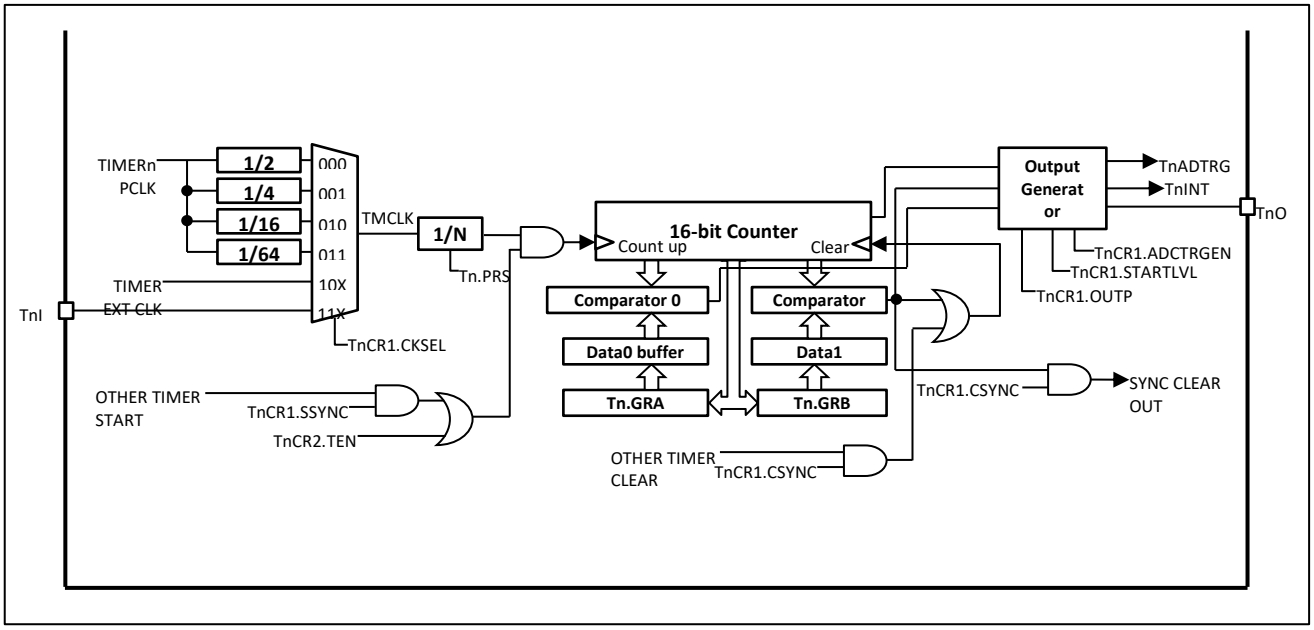

Figure11.1. Block diagram

11.2 Pin description

Table11.1. External pin

PIN NAME	TYPE	DESCRIPTION
TnC	I	External clock / capture input
TnO	O	Timer output

CHAPTER 12. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

12.1 OVERVIEW

4-Channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. Dedicated DMA support to data transfer between memory buffer and transmit or receive buffer of UART block.

UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK/2, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel

- Compatible with 16450
- Support DMA transfer
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication
  - 5-, 6-, 7- or 8- bit data transfer
  - Even, odd, or no-parity bit insertion and detection
  - 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register
- Loop-back control

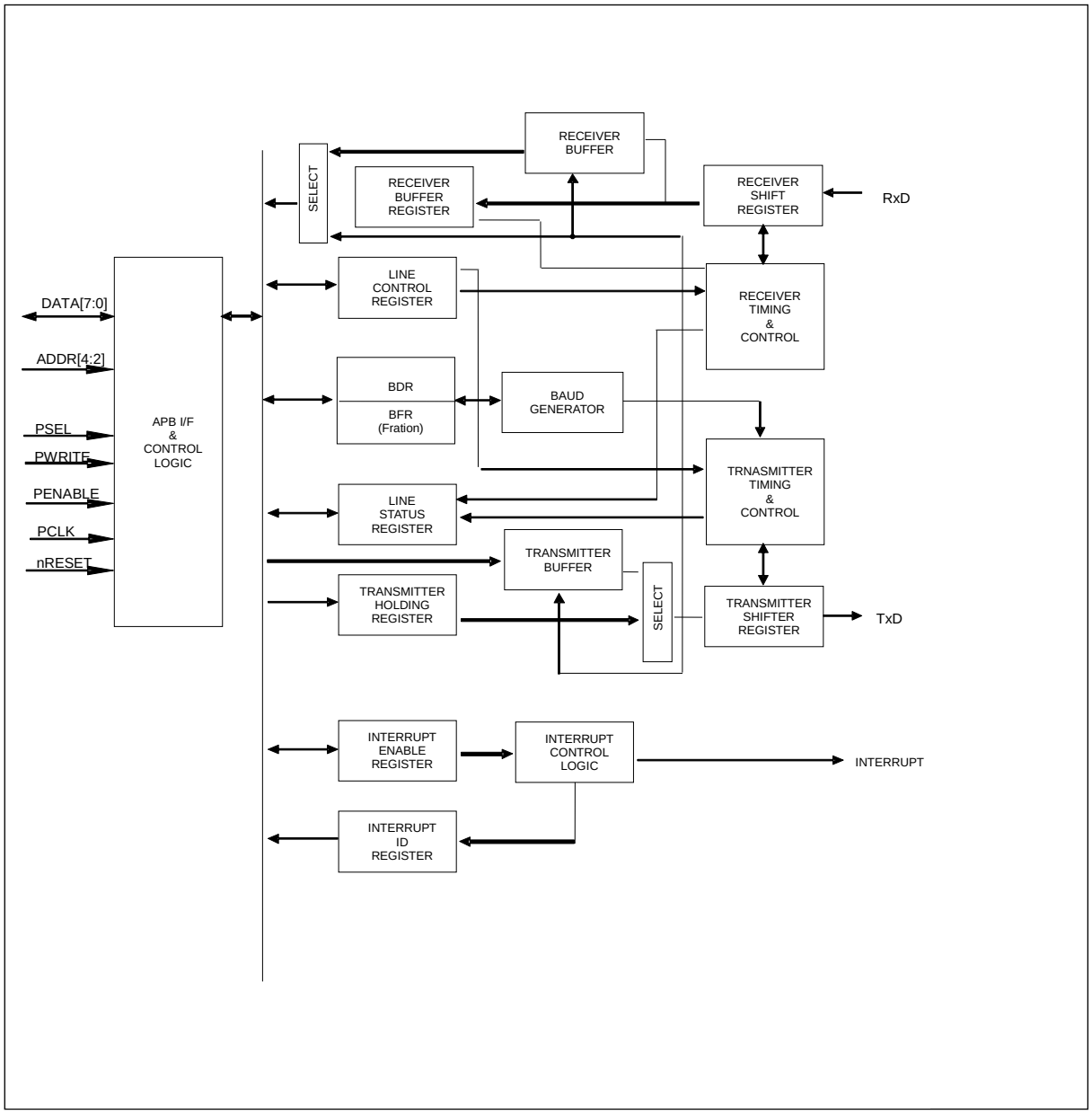

Figure 12.1. Block diagram

12.2 Pin description

Table 12.1. External signal

PIN NAME	TYPE	DESCRIPTION
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input
TXD2	O	UART Channel 2 transmit output
RXD2	I	UART Channel 2 receive input
TXD3	O	UART Channel 3 transmit output
RXD3	I	UART Channel 3 receive input

CHAPTER 13. SERIAL PERIPHERAL INTERFACE (SPI)

13.1 OVERVIEW

2-Channel serial Interface are provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. 4 signals will be used for SPI communication – SS, SCK, MOSI, and MISO.

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8,9,16,17-bit wide transmit/receive register.
- 8,9,16,17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

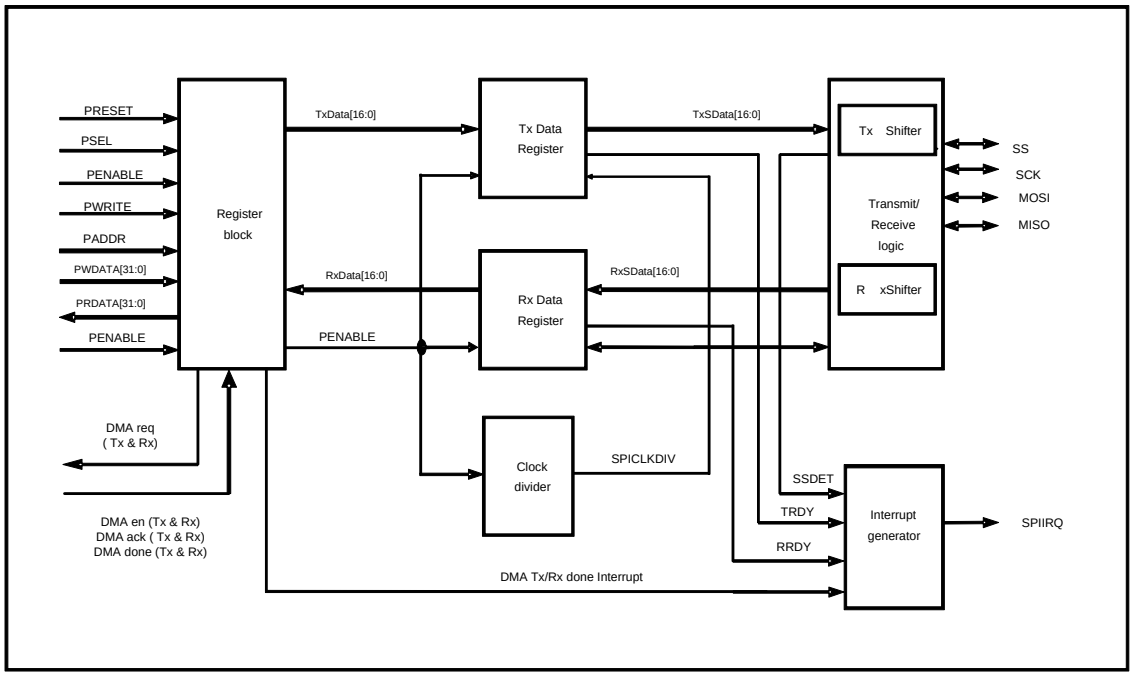

Figure 13.1. SPI block diagram

13.2 PIN DESCRIPTION

Table13.1. External Pins

PIN NAME	TYPE	DESCRIPTION
SS0	I/O	SPI0 Slave select (Master output, Slave input)
SCK0	I/O	SPI0 Serial clock (Master output, Slave input)
MOSI0	I/O	SPI0 Serial data (Master output, Slave input)
MISO0	I/O	SPI0 Serial data (Master input, Slave output)
SS1	I/O	SPI1 Slave select (Master output, Slave input)
SCK1	I/O	SPI1 Serial clock (Master output, Slave input)
MOSI1	I/O	SPI1 Serial data (Master output, Slave input)
MISO1	I/O	SPI1 Serial data (Master input, Slave output)

CHAPTER 14. I²C Interface

14.1 OVERVIEW

I²C(Inter-Integrated Circuit) bus serves as an interface between the microcontroller and the serial I²C bus. It provides two wires, serial bus interface to a large number of popular devices and allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

- Master and slave operation
- Programmable communication speed
- Multi-master bus configuration
- 7-bit addressing mode
- Standard data rate of 100/400 kbps
- STOP signal generation and detection
- START signal generation
- ACK bit generation and detection

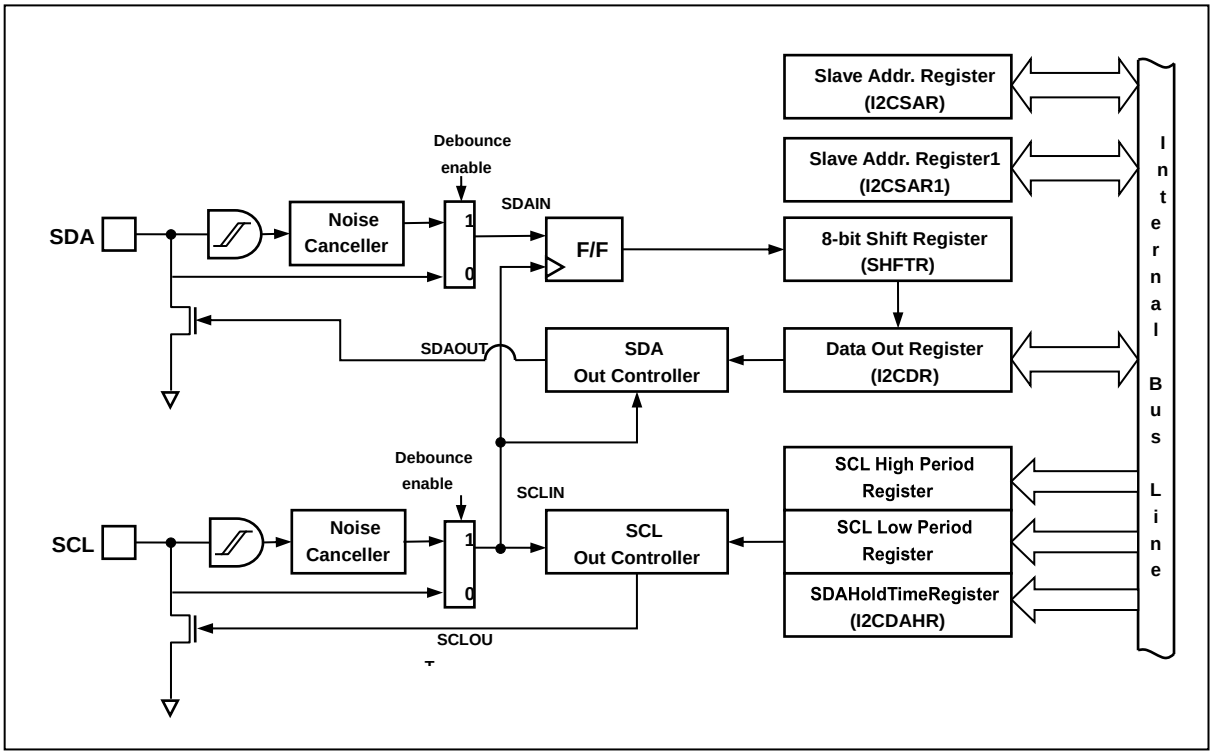

Figure14.1 I²C Block diagram

14.2 PIN DESCRIPTION

Table14.1 I²C interface external pins

PIN NAME	TYPE	DESCRIPTION
SCL0	I/O	I²C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I²C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I²C channel 1 Serial clock bus line (open-drain)
SDA1	I/O	I²C channel 1 Serial data bus line (open-drain)

CHAPTER 15. MOTOR PULSE-WIDTH-MODULATOR (MPWM)

15.1 MPWM Introduction

MPWM is Programmable Motor controller

- 6-Channel outputs for motor control
- Dead- time zone support
- Protection event and over voltage event handling
- Six ADC trigger outputs
- Interval interrupt mode (period interrupt only)
- Up-down count mode

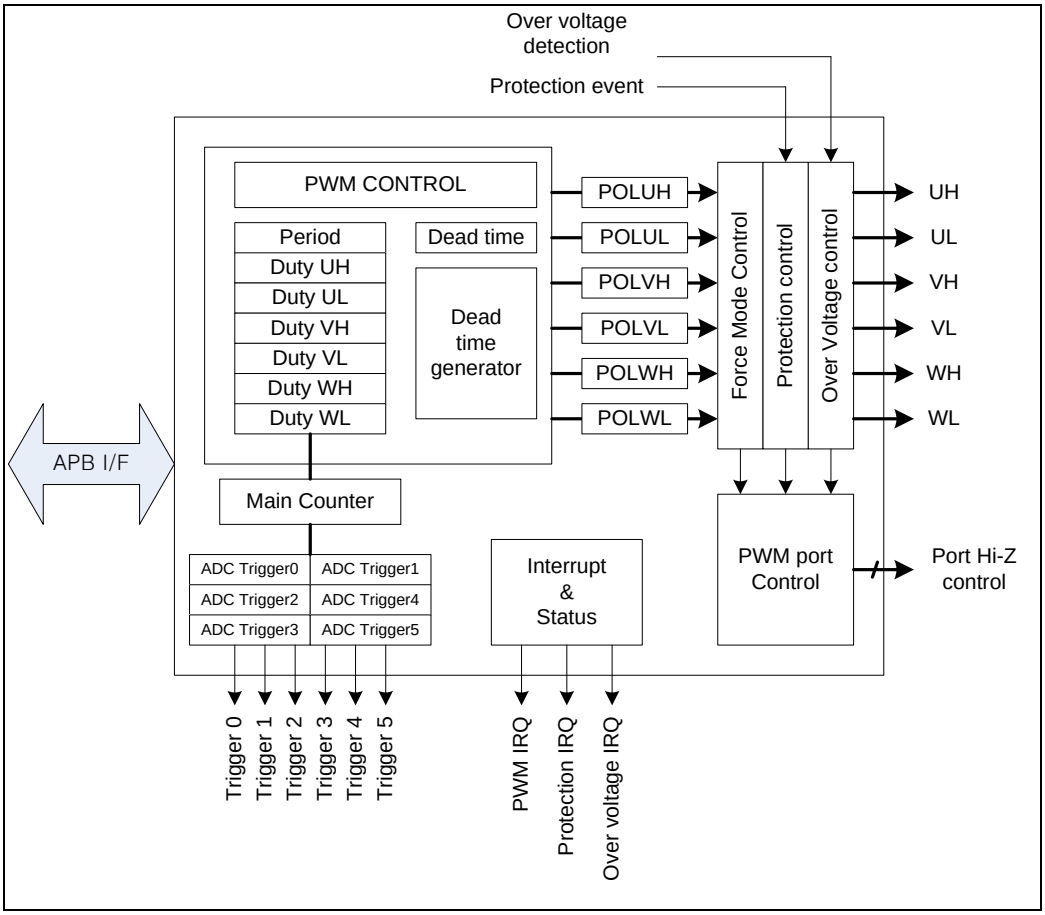

Figure15.1. Block Diagram

15.2 Pin description

Table15.1. External Signals

PIN NAME	TYPE	DESCRIPTION
MP0UH	O	MPWM 0 Phase-U H-side output
MP0UL	O	MPWM 0 Phase-U L-side output
MP0VH	O	MPWM 0 Phase-V H-side output
MP0VL	O	MPWM 0 Phase-V L-side output
MP0WH	O	MPWM 0 Phase-W H-side output
MP0WL	O	MPWM 0 Phase-W L-side output
MP1UH	O	MPWM 1 Phase-U H-side output
MP1UL	O	MPWM 1 Phase-U L-side output
MP1VH	O	MPWM 1 Phase-V H-side output
MP1VL	O	MPWM 1 Phase-V L-side output
MP1WH	O	MPWM 1 Phase-W H-side output
MP1WL	O	MPWM 1 Phase-W L-side output
PRTIN0	I	MPWM 0 Protection Input 0
OVIN0	I	MPWM 0 Over-voltage Input 1
PRTIN1	I	MPWM 1 Protection Input 0
OVIN1	I	MPWM 1 Over-voltage Input 1

CHAPTER 16. 12-BIT A/D CONVERTER

16.1 12-bit ADC Introduction

ADC block consists of 3 independent ADC units.

- 16 Channels of analog inputs
- Single and Continuous conversion mode
- Up to 8 times burst conversion support
- External pin trigger support
- 4 internal trigger sources support (PWMs, timers)
- Adjustable sample & hold time

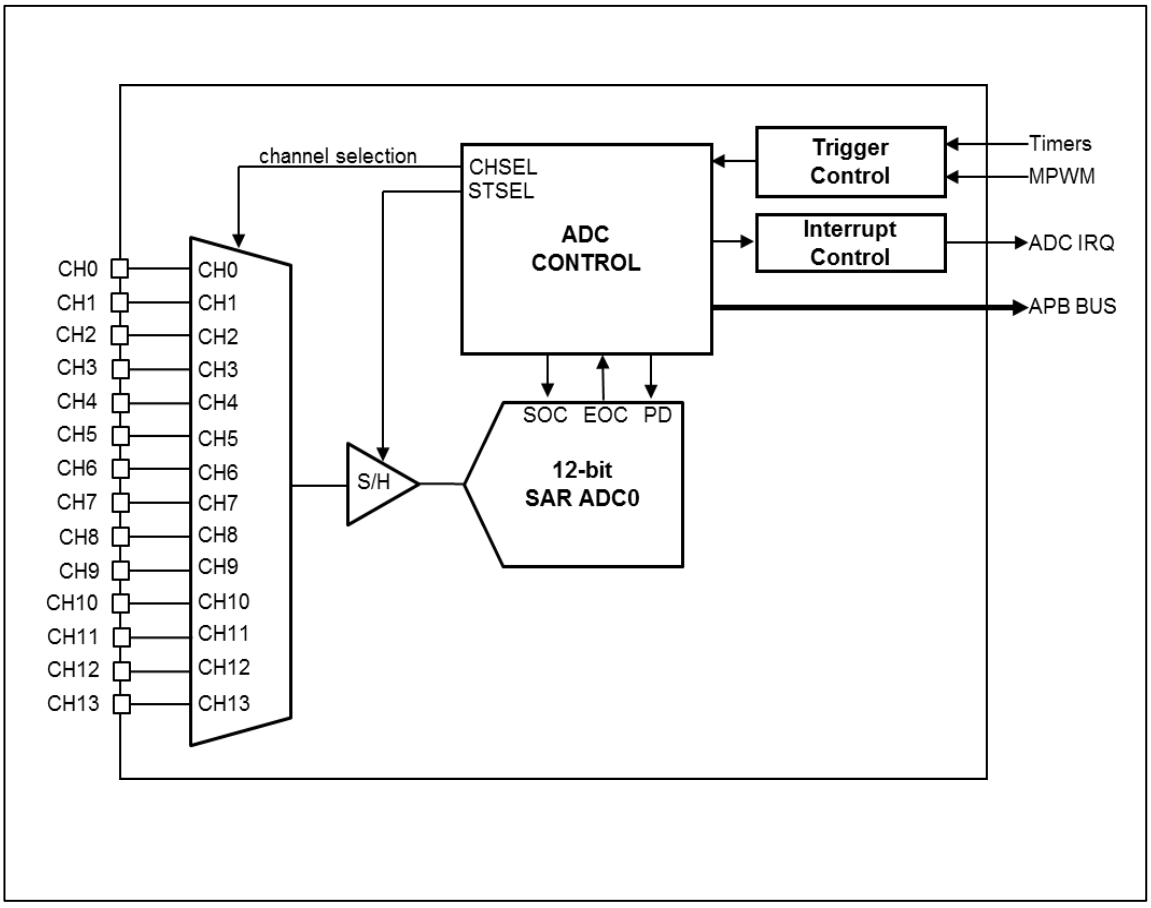

Figure16.1. Block Diagram

16.2 Pin description

Table16.1. External Signal

PIN NAME	TYPE	DESCRIPTION
AVDD	P	Analog Power(3.0V~VDD)
AVSS	P	Analog GND
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14
AN15	A	ADC Input 15

CHAPTER 17. ANALOG FRONT END (AFE)

17.1 Analog Front-end Control Introduction

AFE(Analog Front End) is OPAMPs and comparators interface controller

- 4 OPAMPs
- 4 Comparators
- OPAMP output can be connected with ADC or comparator
- Internal BGR reference for comparator
- Comparator output de-bounce function
- Level and edge interrupt mode support for comparator

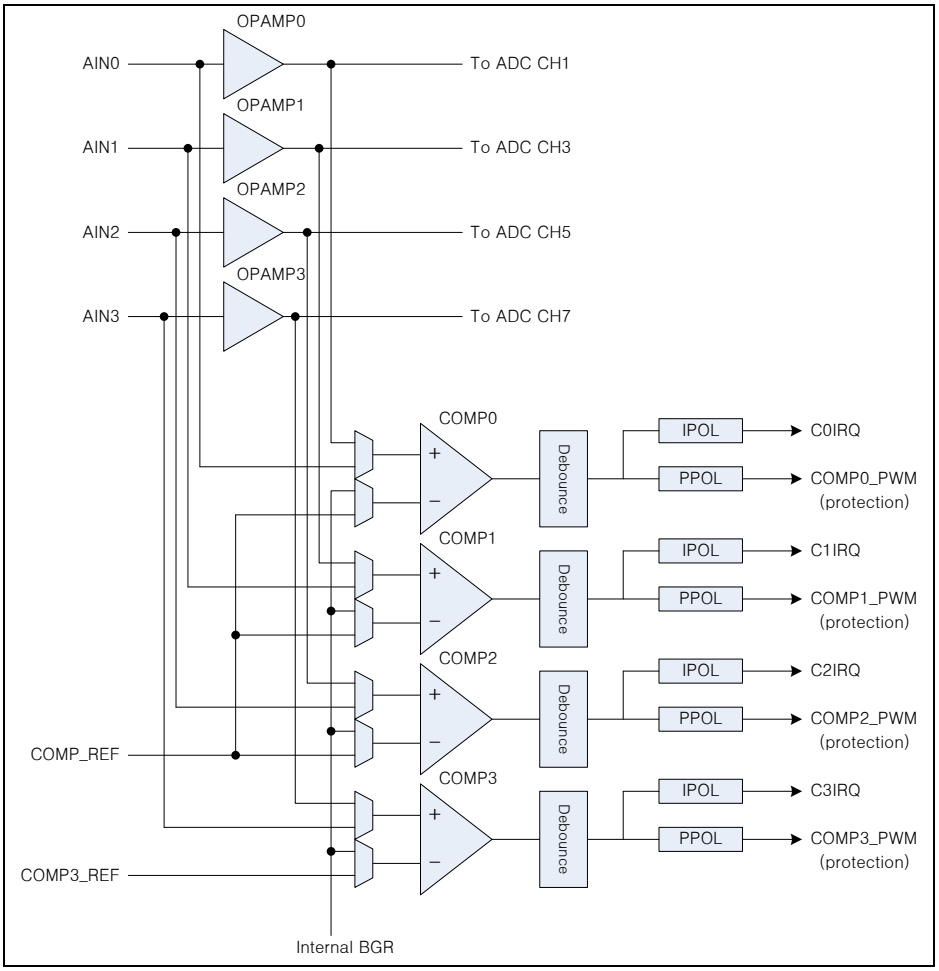

Figure17.1. Block Diagram

17.2 Pin description

Table17.1. External Signal

PIN NAME	TYPE	DESCRIPTION
AVDD	P	Analog Power (3.0V~VDD)
AVSS	P	Analog GND
CP0	A	Comparator Input 0
CP1	A	Comparator Input 1
CP2	A	Comparator Input 2
CP3	A	Comparator Input 3
CREF0	A	Comparator Reference Input 0
CREF3	A	Comparator Reference Input 3

CHAPTER 18. Electrical Characteristic

18.1 DC Characteristics

18.1.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions..

Table18.1. Absolute maximum rating

Parameter		Symbol	min	max	unit
Power Supply (VDD)		V_{DD}	-0.5	+6	V
Analog Power Supply (AVDD)		AV_{DD}	-0.5	+6	V
Input High Voltage			-	V_{DD}+0.5	V
Input Low Voltage			V_{SS}–0.5	-	V
Output Low Current per pin		I_{OL}	-	20	mA
Output Low Current Total	80-pin	$\sum I_{OL}$	-	100	mA
	64-pin	$\sum I_{OL}$	-	80	
Output High Current per pin		I_{OH}	-	-10	mA
Output High Current Total	80-pin	$\sum I_{OH}$	-	100	mA
	64-pin	$\sum I_{OH}$	-	80	
Input Main Clock Range			0.4	10	MHz
Operating Frequency			-	72	MHz
Storage Temperature		T_{ST}	-55	+125	℃
Operating Temperature		T_{OP}	-40	+85	℃

18.1.2 DC Characteristics

Table 18.2 Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Supply Voltage	VDD		3.0		5.5	V
Supply Voltage	AV_{DD}		3.0	5.0	5.5	V
Operating Frequency	f	OSC_{MAIN}	4		8	MHz
		OSC_{INT}		20		MHz
		PLL	4		72	MHz
Operating Temperature	T_{OP}	T_{OP}	-40		+85	℃

Table 18.3 DC Electrical Characteristics (VDD = +5V, Ta = 25 ℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Input Low Voltage	V_{IL}	Schmitt input	-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}	Schmitt input	$0.8V_{DD}$	-	-	V
Output Low Voltage	V_{OL1}	I_{OL} = 10mA All output ports except V_{OL2}	-	-	V_{SS} +1.0	V
	V_{OL2}	I_{OL} = 3mA PA0-PA6,PB6-PB7, PC4,PC7,PC8,PC10-PC13,PD0-PD3, PD10,PD11,PD14, PD15	-	-	V_{SS} +1.0	V
Output High Voltage	V_{OH1}	I_{OH} = -3mA All output ports except V_{OH2}	V_{DD} –1.0	-	-	V
	V_{OH2}	I_{OH} = -1.2mA PA0-PA6,PB6-PB7, PC4,PC7,PC8,PC10-PC13,PD0-PD3, PD10,PD11,PD14, PD15	V_{DD} –1.0	-	-	V
Input High Leakage	I_{IH}				4	µA
Input Low Leakage	I_{IL}		-4			µA
Pull-up Resister	R_{PU}	R_{MAX}:V_{DD}=3.0V R_{MIN}:V_{DD}=5V	30	-	70	kΩ

18.1.3 Current Consumption

Table18.4 Current consumption in each mode (Temperature: +25℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Normal Operation	$I_{DD\ NORM}$	OSC_{RING} =RUN IOSC20=RUN OSC_{MAIN} =8MHz HCLK=72MHz	-	35	-	mA
Sleep Mode	$I_{DD\ SLEEP}$	OSC_{RING} =RUN IOSC20=RUN OSC_{MAIN} =STOP HCLK =RUN	-	3	-	mA

18.1.4 POR Electrical Characteristics

Table18.5 POR Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	VDD18		1.6	1.8	2.0	V
Operating Current	IDD_{PoR}	Typ. <6uA If always on	-	60	-	nA
POR Set Level	VR_{PoR}	VDD rising (slow)	1.3	1.4	1.55	V
POR Reset Level	VF_{PoR}	VDD falling (slow)	1.1	1.2	1.4	V

18.1.5 LVD Electrical Characteristics

Table18.6 LVD Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD18}		1.7		5	V
Operating Current	I_{DD}	Typ. <6μA If always on	-	1	-	mA
LVD Set Level 0	V_{RISING}	V_{DD} rising (slow)	1.6	1.8	2.0	V
LVD Set Level 1	$V_{FALLING}$	V_{DD} rising (slow)	2.0	2.2	2.5	V
LVD Set Level 2	V_{DD18}	V_{DD} rising (slow)	2.5	2.7	3.0	V
LVD Set Level 3	I_{DD}	V_{DD} rising (slow)	3.9	4.3	4.6	V

18.1.6 VDC Electrical Characteristics

Table18.7VDC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD}		3.0	-	5.5	V
VDC Output Voltage	V_{OUT}	@RUN	1.62	1.8	1.98	V
		@STOP	1.4	1.8	2.0	V
Regulation Current	I_{OUT}				100	mA
Drop-out Voltage	V_{DROP}	VDDVDC=3.0V IOUT=100mA	-	-	200	mV
Current Consumption	$I_{DD\ NORM}$	@RUN	-	100	150	μA
	$I_{DD\ STOP}$	@STOP	-	1	2	μA

18.1.7 External OSC Characteristics

Table18.8External OSC Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ	Max	unit
Operating Voltage	V_{DD}		3.0	-	5.5	V
IDD	I_{DD}	@4MHz/5V	-	240		μA
Frequency	f_{osc}		4	8	10	MHz
Output Voltage	V_{OUT}		1.2	2.4	-	V
Load Capacitance	C_L		5	22	35	pF

18.1.8 Internal RC OSC Characteristics

Table 18.9 Internal RC OSC Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ	Max	unit
Operating Voltage	V_{DD}		3.0		5.5	V
IDD	I_{OSC}	@20MHz	-	240		μA
Frequency	f_{IOSC}			20		MHz

18.1.9 PLL Electrical Characteristics

Table18.10PLL Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD}		3.0		5.5	V
Output Frequency	f_{OUT}		4		72	MHz
Operating Current	I_{DD}	@72MHz		1.3		mA
Duty	f_{DUTY}		40	-	60	%
P-P Jitter	JITTER	@Lock			500	Ps
VCO	VCO		30		72	MHz
Input Frequency	f_{IN}		4		8	MHz
Locking time	t_{LOCK}				1	ms

18.1.10 ADC Electrical Characteristics

Table 18.11ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AV_{DD}		3.0	5	5.5	V
Reference Voltage	AV_{REF}		3.0	5	5.5	V
Resolution				12		Bit
Operating Current	AI_{DD}				2.8	mA
Analog Input Range			0		AVDD	V
Conversion Rate				-	1.6	Msps
Operating Frequency	f_{ACLK}				25	MHz
DC Accuracy	INL			±2.5		LSB
	DNL			±1.0		LSB
Offset Error				±1.5		LSB
Full Scale Error				±1.5		LSB
SNDR	SNDR			68		dB
THD				-70		dB

18.1.11 OP-Amp Electrical Characteristics

Table 18.12 ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AV_{DD}		3.0	5	5.5	V
Operating Current	AI_{DD}				2.2	mA
Analog Input Range			0		AV_{DD}-1.4	V
Slew Rate		@ C_L = 20pF		15		V/ µs
Gain Error		Gain=2.19~4.37	-3		+3	%
		Gain=5.0~8.74	-4		+4	%
Common Mode Rejection Ratio			50	70		dB
Power Supply Rejection Ratio			40	70		dB
Gain Bandwidth		@C_L=20pF		16		MHz
Open Loop Voltage Gain				100		dB
Open Loop Phase Margin		@C_L=20pF		45		°
Closed Loop Phase Margin				70		°
Turn On time	t_{ON}			2		µs
Gain			2.19		8.74	

18.1.12 Comparator Electrical Characteristics

Table 18.13 Comparator Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AV_{DD}		3.0	5	5.5	V
Analog Input Range	V_{IN}		AV_{SS}		AV_{DD}	V
Reference Input Range	V_{REF}		0.9		AV_{DD}-0.2	V
Input Offset Voltage			-4		+4	%
Response Time					1	µs

CHAPTER 19. Package

19.1 MQFP-80 Package dimension

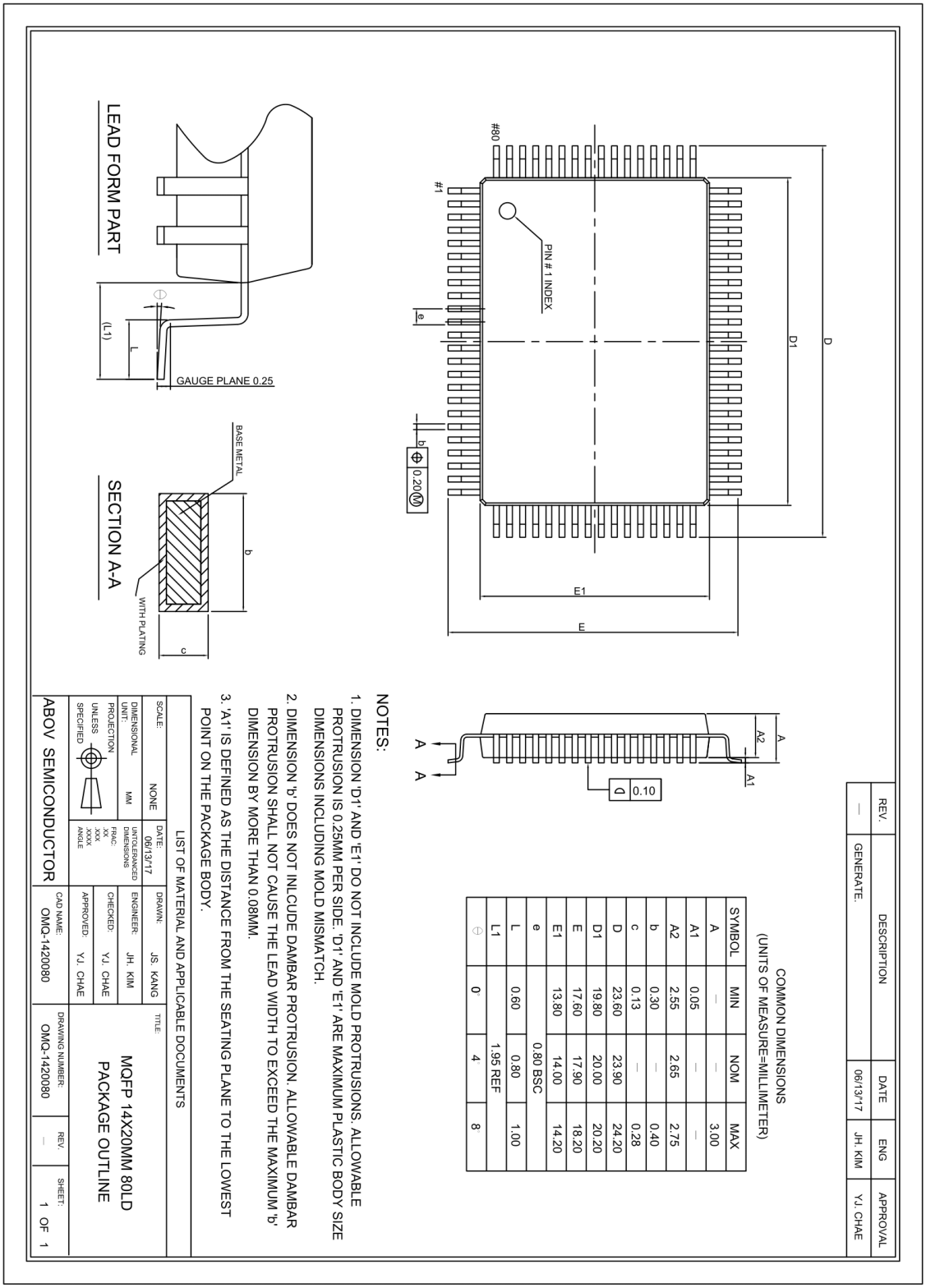

Figure 19.1. Package dimension (MQFP-80 14X20)

19.2 LQFP-80 Package dimension

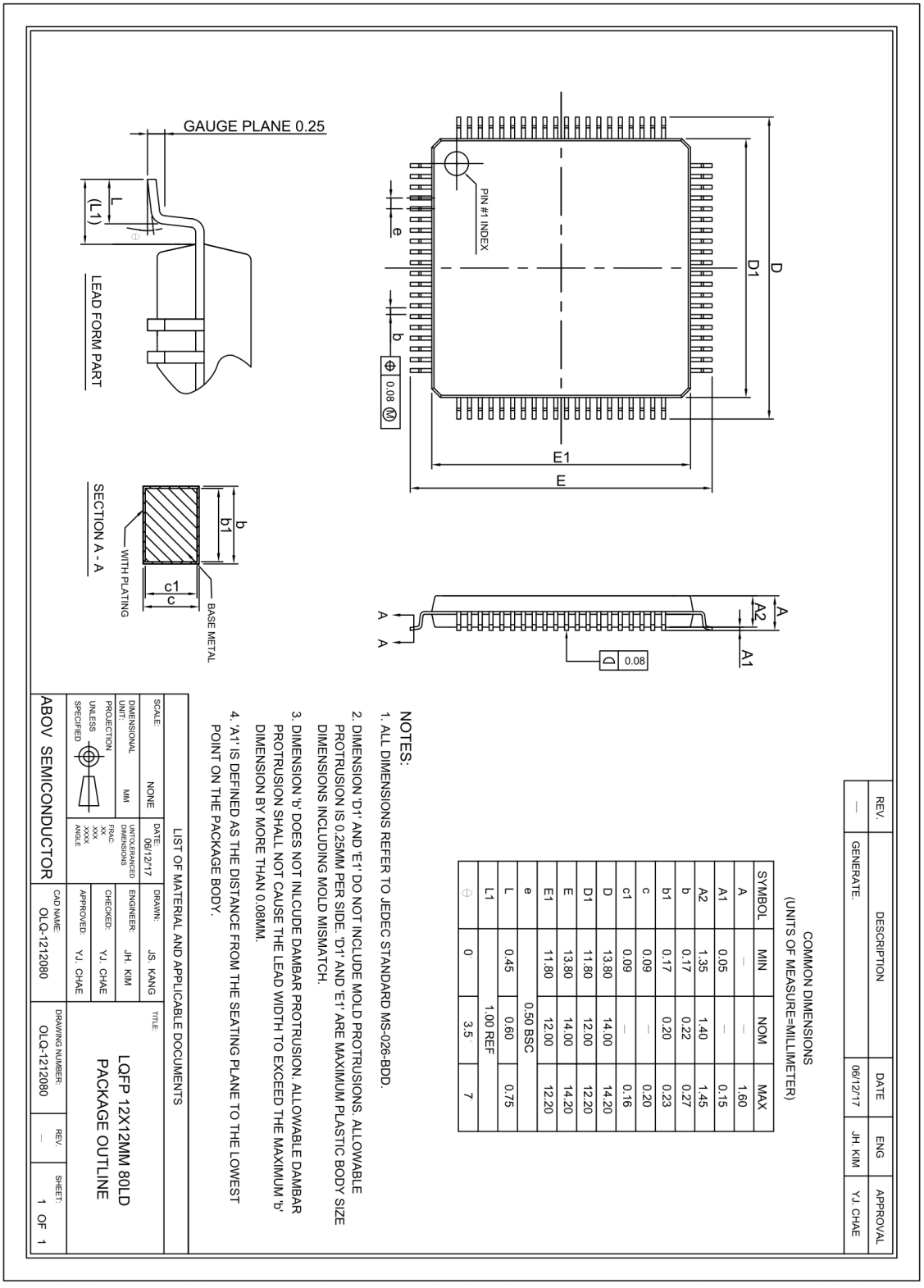

Figure 19.2. Package dimension (LQFP-80 12X12)

19.3 LQFP-64 Package dimension

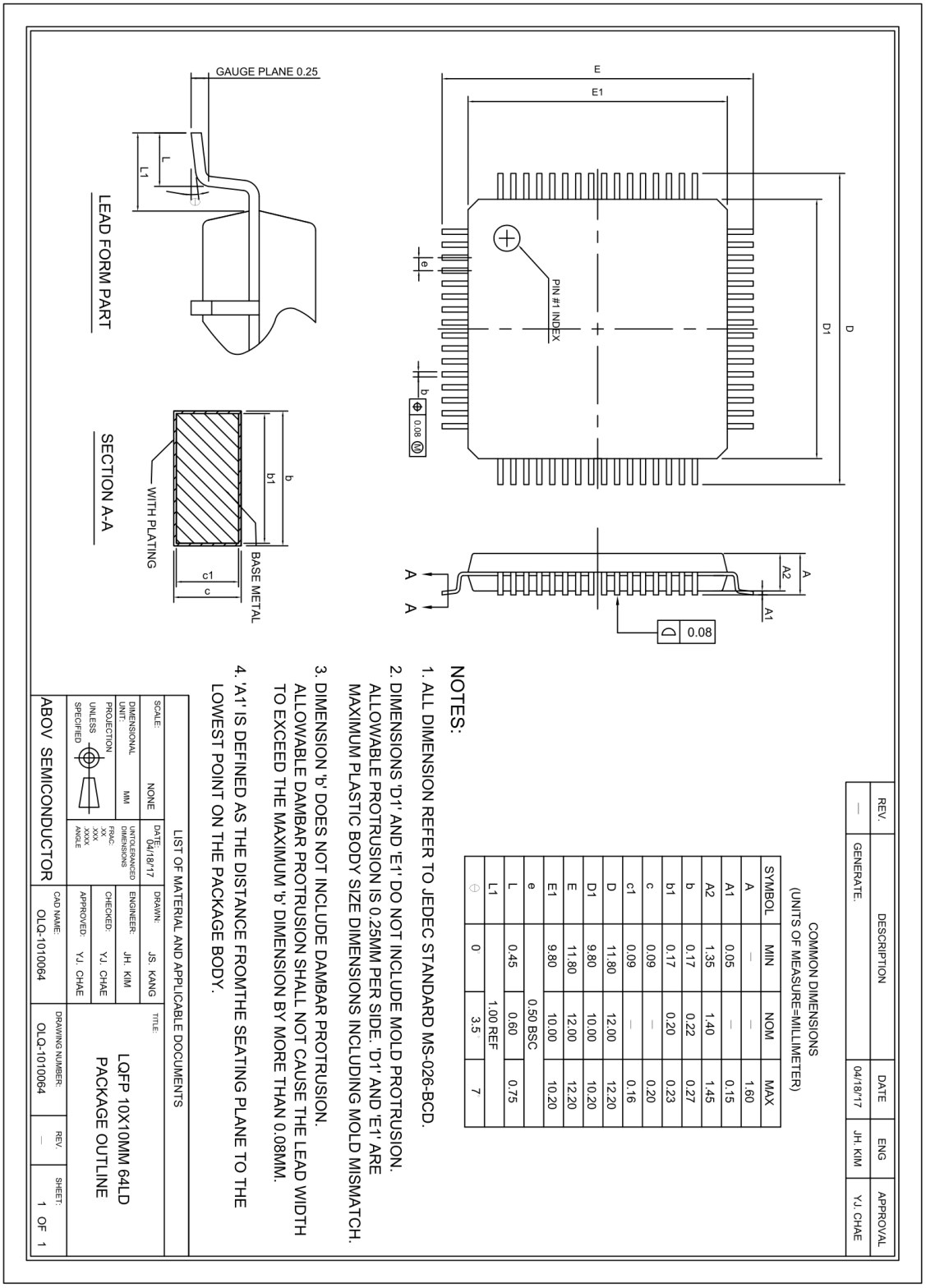

Figure 19.3. Package dimension (LQFP-64 10X10)