Capacitive 8-channel Touch Sensor

Main features

8-channel Capacitive Touch Sensor with Auto Sensitivity Calibration

GPIO Control

- Default 1-pin GPIO Control Support (OUT1)
- Max. 9-pin GPIO Control Support (with the not used touch channel pin)

Selectable Output Operation

- Single Key Output (Single Key Result Mode, Noise Mode)
- Multi Key Output

Independently Adjustable in 8-step Sensitivity

Adjustable Response Time and Interrupt Level by the Control Register

I2C Serial Interface

IDLE Mode to Save the Power Consumption

- Touch Wake-up : 30uA @300ms

Operating Voltage

- 2.7V ~ 5.5V

Operating Conditions

- -40°C to 85°C temperature range

Package

- 16 QFN (AT3108U)
- 16 SOPN (AT3108E)

Application

- Touch Key Application

AT3108

User's Manual

V 1.2

Revised 14 January, 2020

Revision history

Version	Date	Revision list
1.0	2017.02.15	First Release
1.1	2018.04.03	Two registers' description is added : START_THD(0x00), STEP_THD(0x01).
1.2	2020.01.14	RELEASE_INT_DELAY register is added.

Version 1.2

Published by Sensor Solution team

Additional information of this manual may be served by ABOV Semiconductor offices in Korea or distributors.

ABOV Semiconductor reserves the right to make changes to any information here in at any time without notice.

The information, diagrams and other data in this manual are correct and reliable;
However, ABOV Semiconductor is in no way responsible for any violations of patents or other rights of the third party generated by the use of this manual.

1. Overview

1.1 General Feature

- **8-channel Capacitive Sensor with Auto Sensitivity Calibration**
- **GPIO Control**
- **Selectable Output Operation**
  - **Single Key Output / Multi-Key Output Mode**
- **Independently Adjustable in 8-step Sensitivity**
- **Adjustable Response Time and Interrupt Level by the Control Registers**
- **I2C Serial Interface**
- **IDLE Mode to Save the Power Consumption**
  - **Touch Wake up : 30uA @ 300ms**
- **Operating Voltage**
  - **2.7V ~ 5.5V**
- **Operating Temperature : -40℃ ~ +85℃**

Device name	Touch CH	Package
AT3108U	8CH	16 QFN
AT3108E	8CH	16 SOPN

2. Pin Description

PKG		NAME	Function	Shared with
16QFN	16SOPN			
2	4	RESETB	System Reset (Low Reset)	-
3	5	CS4	Capactive Sensing Channel 4	GPIO4
4	6	CS5	Capactive Sensing Channel 5	GPIO5
5	7	CS6	Capactive Sensing Channel 6	GPIO6
6	8	CS7	Capactive Sensing Channel 7	GPIO7
7	9	CS0	Capactive Sensing Channel 0	GPIO0
8	10	CS1	Capactive Sensing Channel 1	GPIO1
9	11	CS2	Capactive Sensing Channel 2	GPIO2
10	12	CS3	Capactive Sensing Channel 3	GPIO3
11	13	OUT1	Digital Output Pin 1	-
13	15	INT	Interrupt Output	-
12	14	I2C_EN	I2C Enable (Low Enable; Open-drain) (0 : Enable / 1 : Disable)	-
14	16	VSS	Supply Ground	-
15	1	VDDEXT	Power (2.7V to 5.5V)	
16	2	SDA	I2C Data (Open-drain)	-
1	3	SCL	I2C Clock (Open-drain)	-

3. Pin Assignment

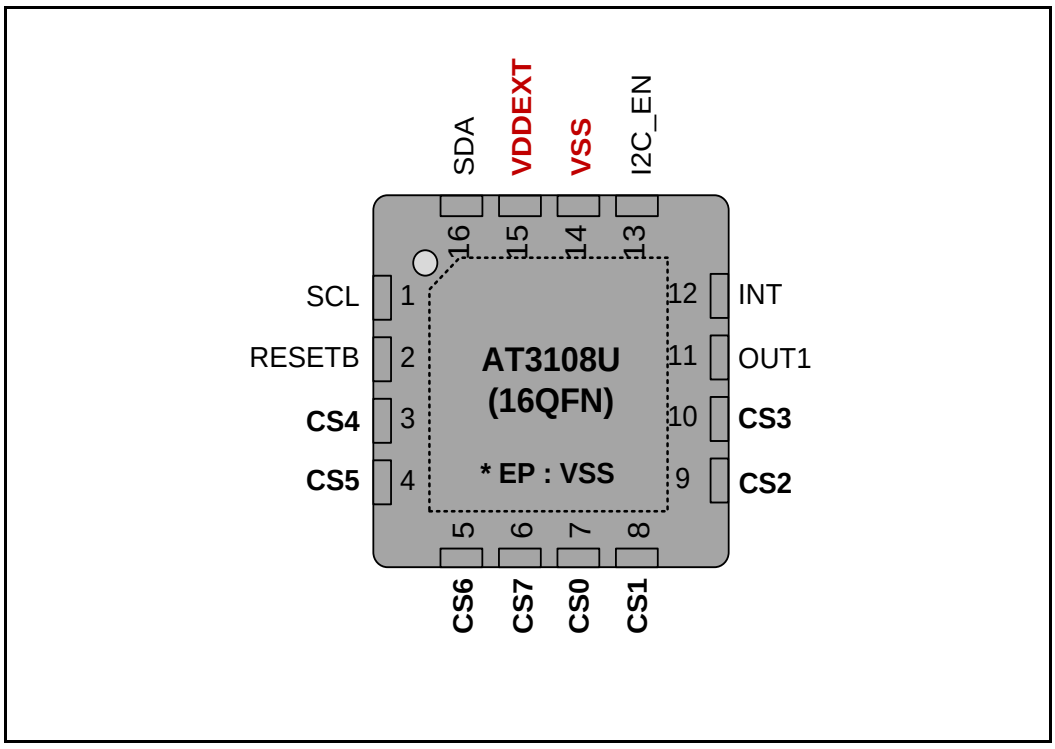


Figure 1 16-QFN Pin Assignment

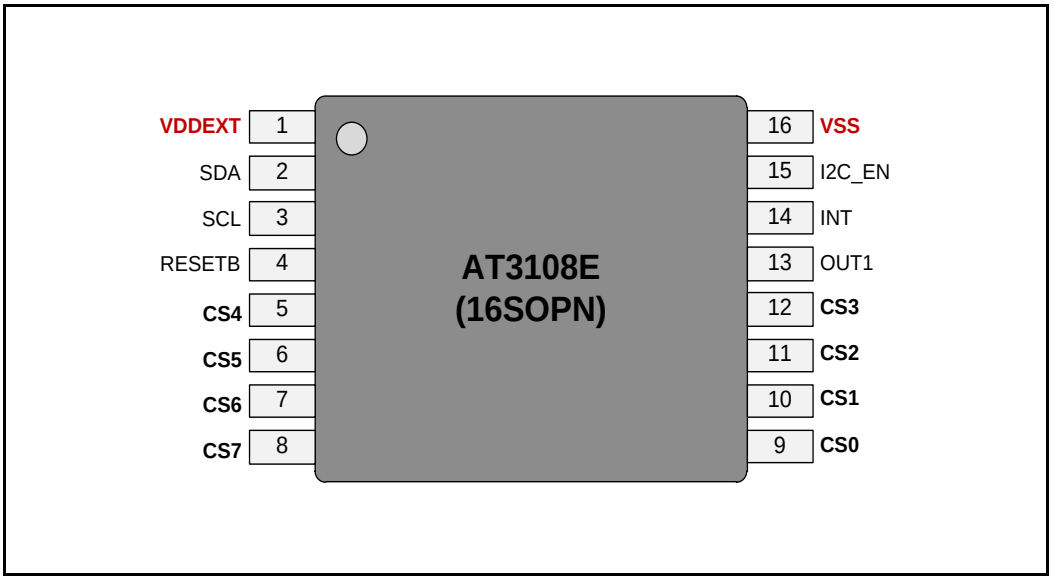
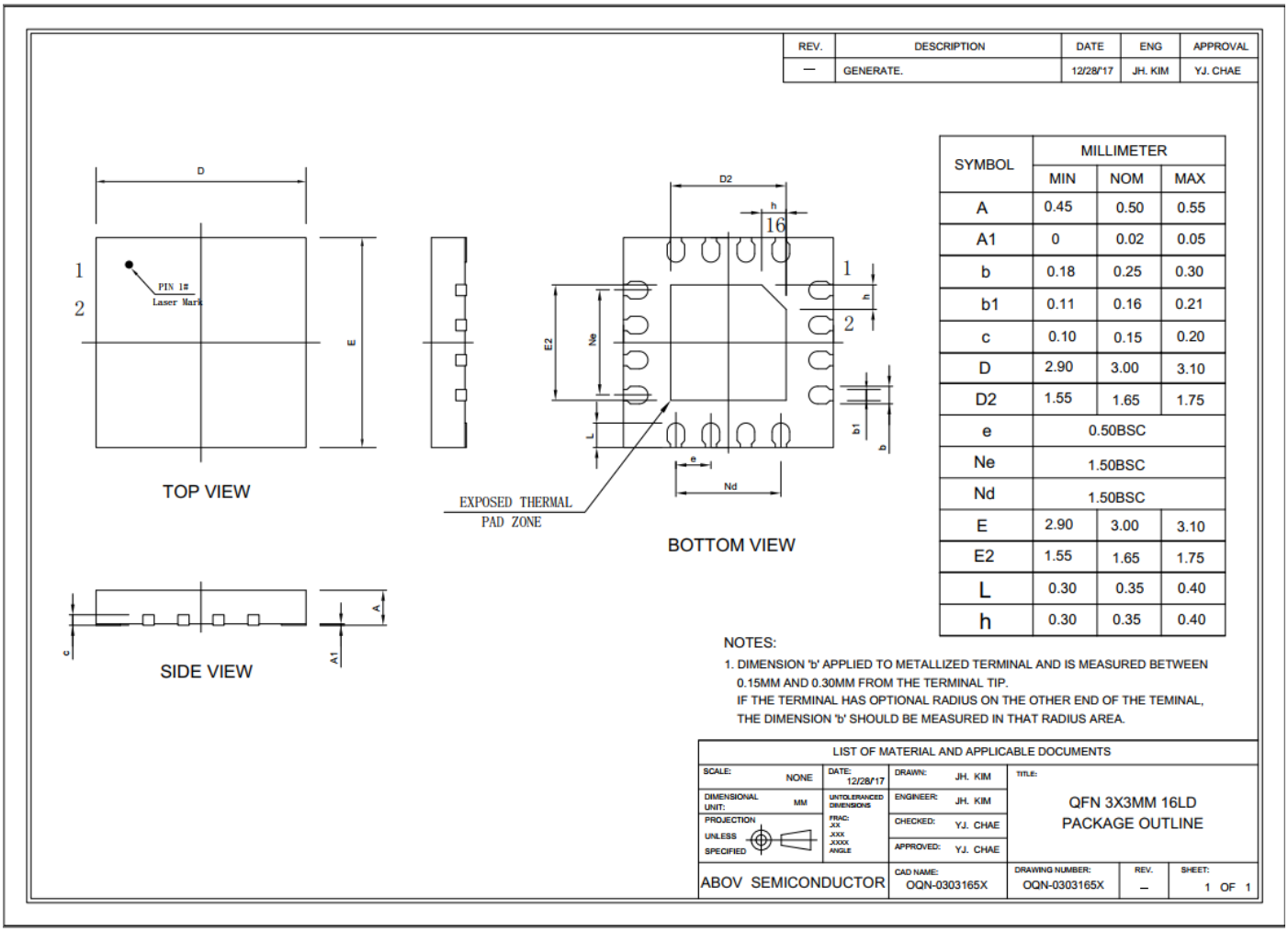


Figure 2 16-SOPN Pin Assignment

4. Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.11	0.16	0.21
c	0.10	0.15	0.20
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.30	0.35	0.40
h	0.30	0.35	0.40

Figure 3 16-pin QFN Package

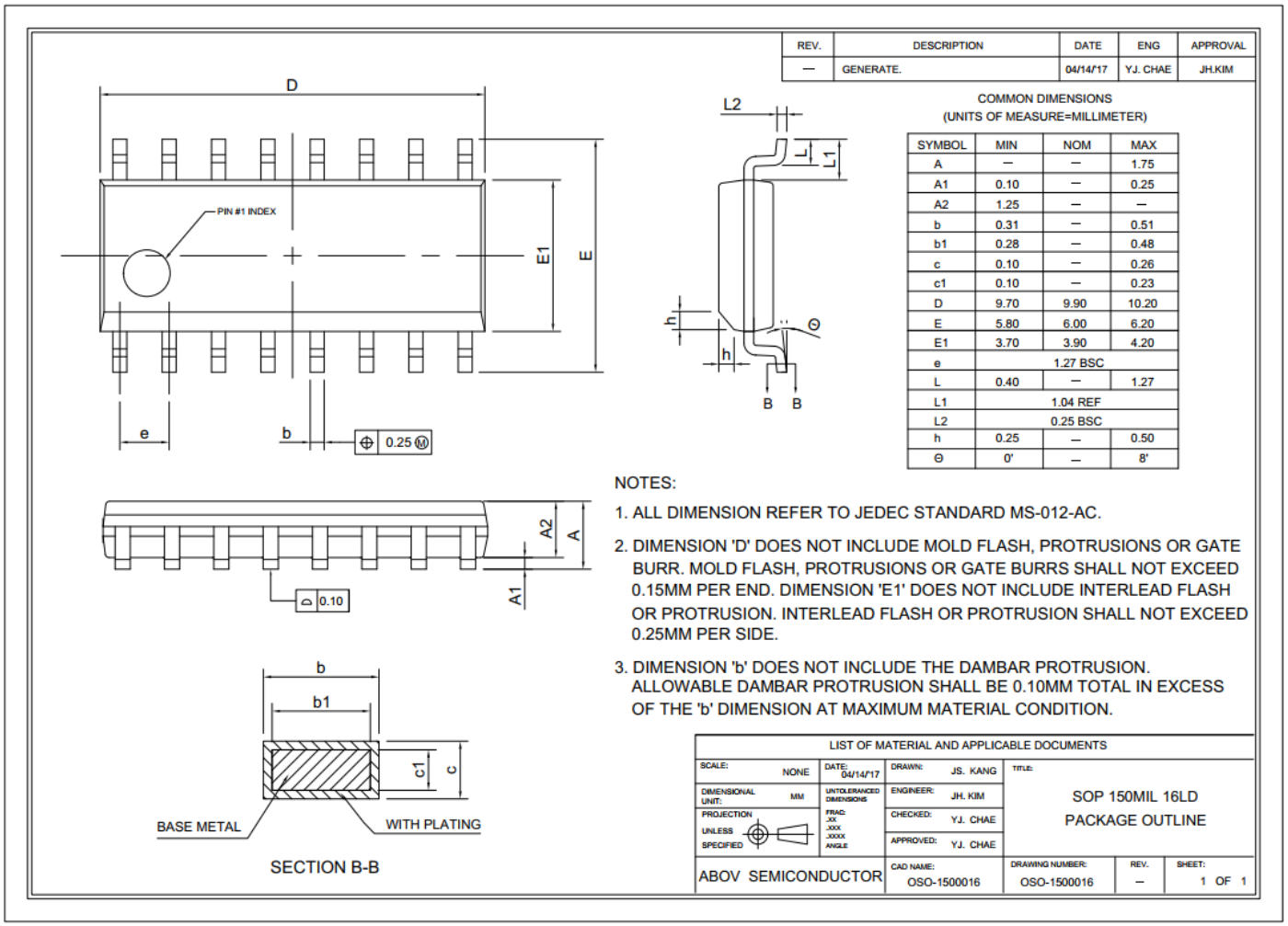


Figure 4 16-pin SOPN Package

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3~+6.5	V
	VSS	-0.3~+0.3	V
Normal Voltage Pin	VI	-0.3~VDD+0.3	V
	VO	-0.3~VDD+0.3	V
	IOH	10	mA
	∑IOH	80	mA
	IOL	20	mA
	∑IOL	160	mA
Total Power Dissipation	PT	600	mW
Storage Temperature	TSTG	-65 ~ +150	℃

Note) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 ESD Characteristics

Table 5-2 ESD Characteristics

Mode	Polarity	Max.	Reference
H.B.M	Pos. / Neg.	2,000V	VDD
		2,000V	VSS
		2,000V	P to P
M.M	Pos. / Neg.	200V	VDD
		200V	VSS
		200V	P to P
C.D.M	Pos. / Neg.	1,000V	DIRECT
		1,000V	

5.3 Latch-up Characteristics

Table 5-3 Latch-up Characteristics

Mode	Polarity	Max.	Test Step
Current (I – Mode)	Positive	200mA	25mA
	Negative	200mA	25mA
VDD-VSS (Over Voltage)	Positive	8.25V	-

5.4 Recommended Operating Conditions

Table 5-4 Recommended Operation Conditions

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VDD	Touch Sensing Operation	2.7	-	5.5	V
Operating Temperature	TOPR	VDD=2.7~5.5V	-40	-	85	℃

5.5 Power-On-Reset Characteristics

Table 5-5 Recommended Operation Conditions

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage			VSS	-	5.5	V
Operating Temperature			-40	-	+85	℃
VDD Rise Rate	VRR		0.05	-	50	V/ms

6. I²C Interface

6.1 I²C Bit Transfer (Data Validity)

The data on the SDA line must be stable during HIGH period of the clock, SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

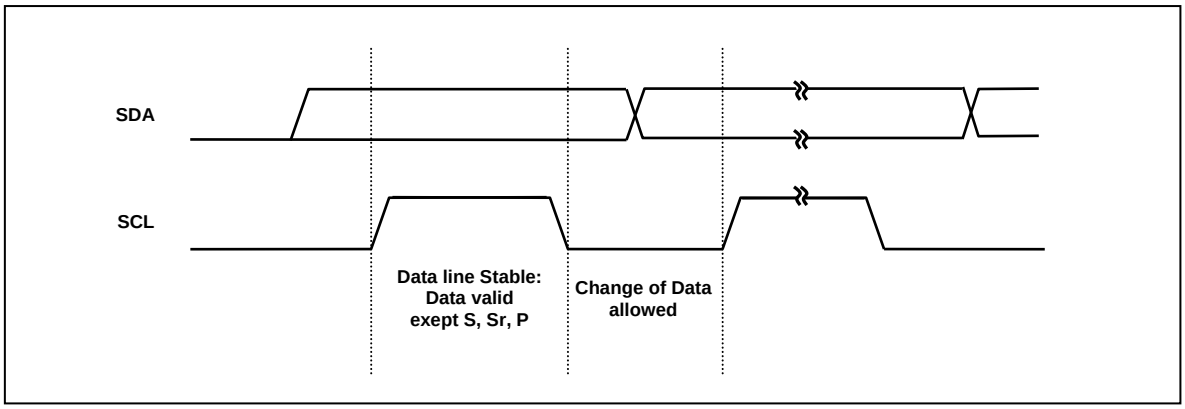


Figure 5 Bit Transfer on the I²C-Bus

6.2 Start / Repeated Start / Stop

One master can issue a START (S) condition to notice other devices connected to the SCL, SDA lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

A high to low transition on the SDA line while SCL is high defines a START (S) condition.

A low to high transition on the SDA line while SCL is high defines a STOP (P) condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

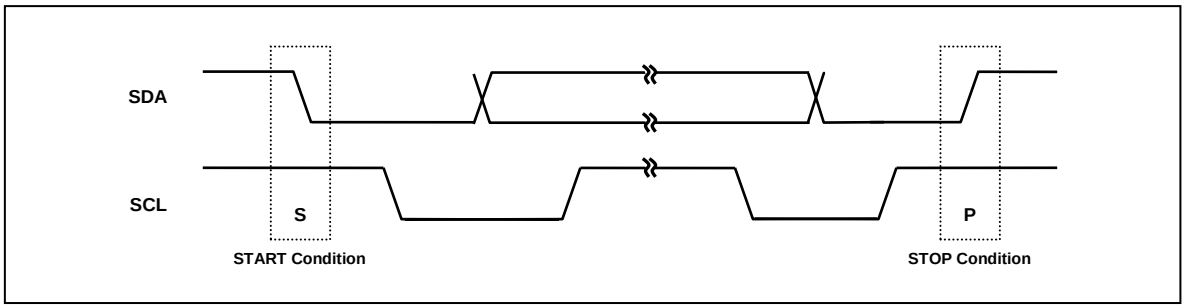


Figure 6 START and STOP Condition

6.3 Data Transfer

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can

hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

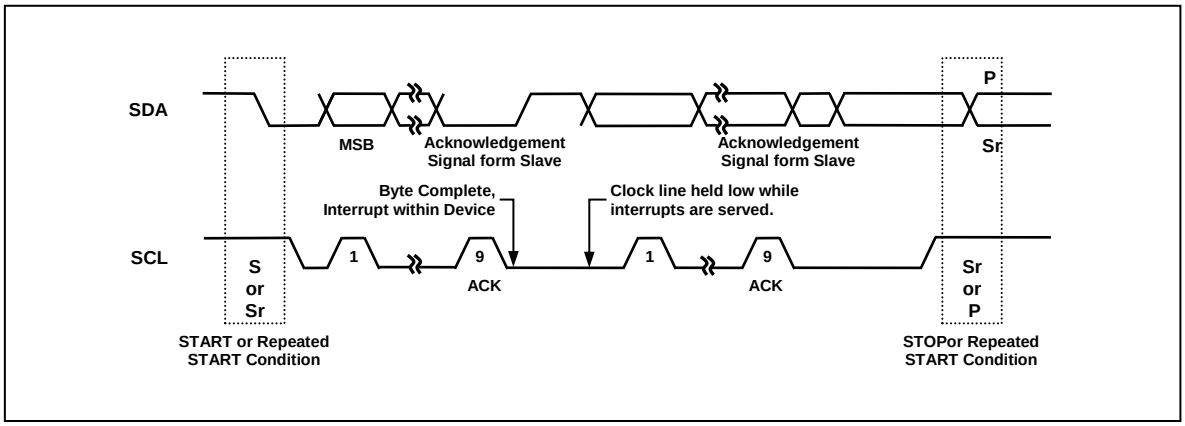


Figure 7 Data Transfer on the I²C-Bus

6.4 Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

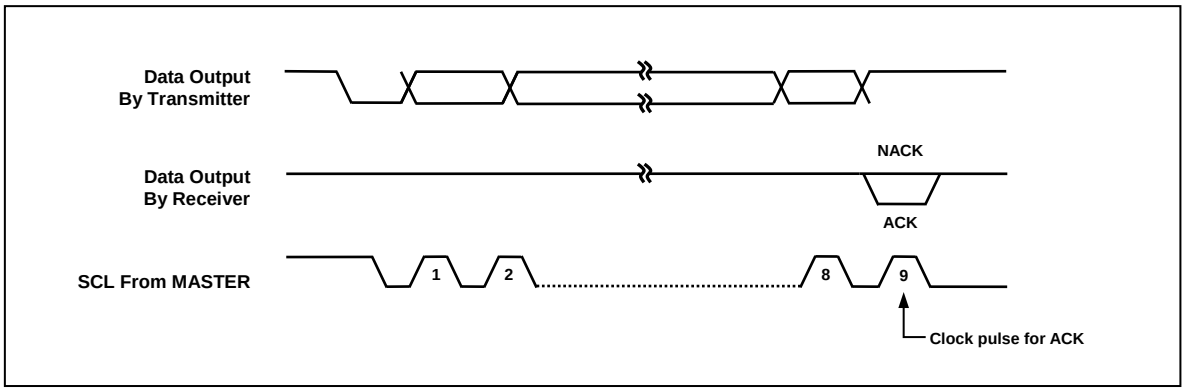


Figure 8 Acknowledge on the I²C-Bus

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

6.5 Synchronization / Arbitration

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and it will hold the SCL line in that state until the clock HIGH state is reached. However the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. In this way, a synchronized

SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition. Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output state because the level on the bus doesn't correspond to its own level. Arbitration continues for many bits until a winning master gets the ownership of I^2C bus. Its first stage is comparison of the address bits.

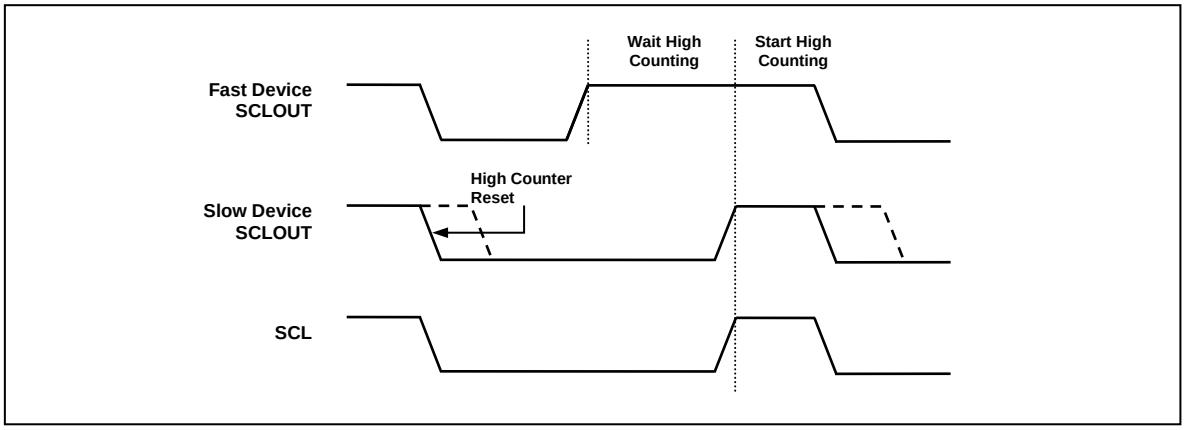


Figure 9 Clock Synchronization during Arbitration Procedure

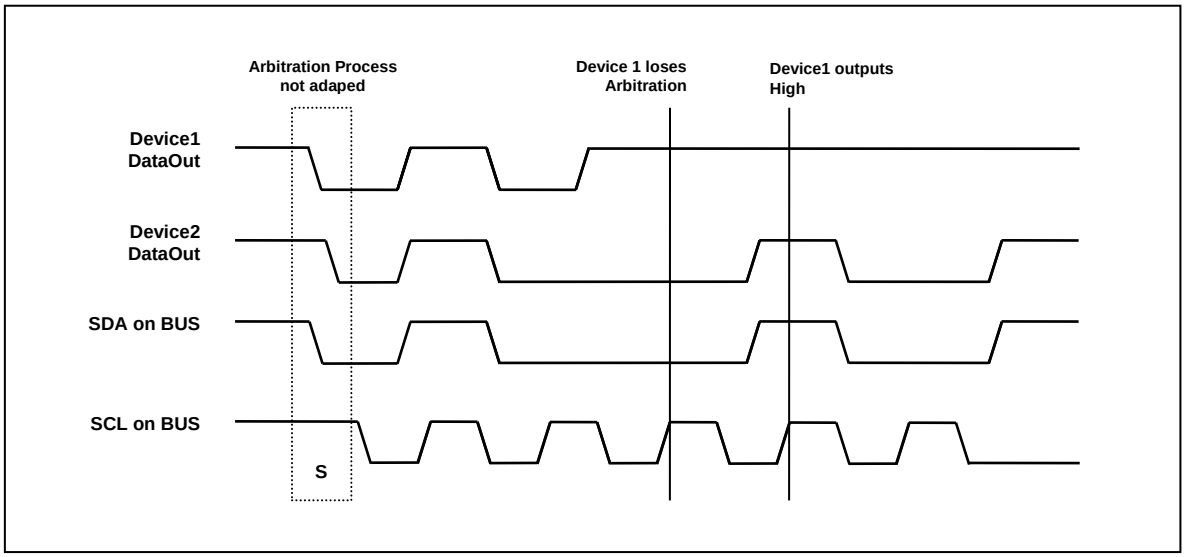


Figure 10 Arbitration Procedure of Two Masters

6.6 First Byte

6.6.1 Slave Address

The slave address of the AT3108 Chip is 0xF0 (F0h).

6.6.2 R/W (Read or Write)

The direction of data, read or write, is decided by the 1-bit value behind of the address 7-bit data.

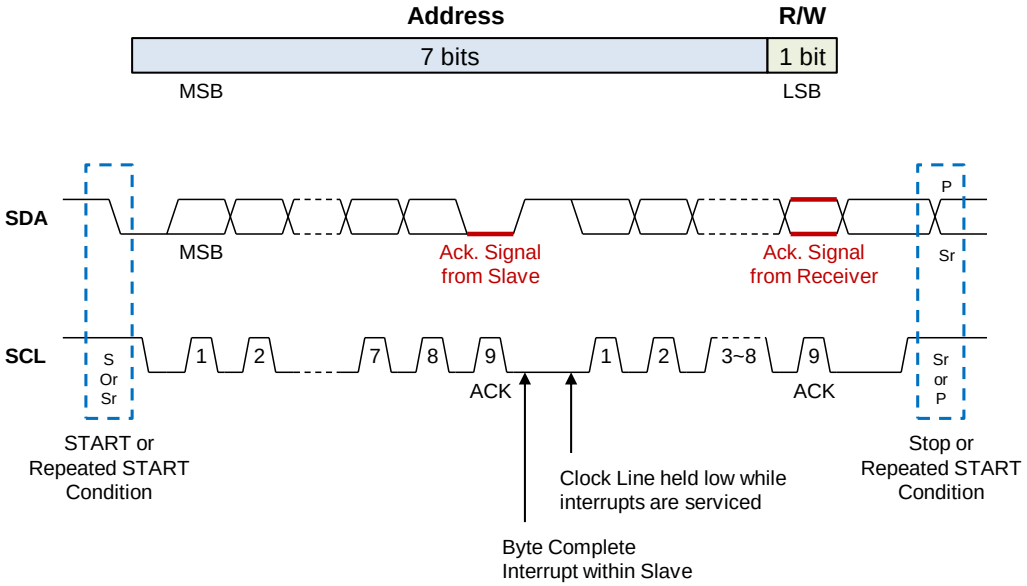


Figure 11 First Byte (Slave Address and R/W)

6.7 I²C Write and Read Operations

The figures as below represents the I2C write and read operation

Write the register 0x02 to 0x03 with 2-byte data 0x33 and 0x22.

START	Device Address 0xF0	ACK	Register Address 0x02	ACK	Write Data 0x33	ACK	Write Data 0x22	ACK	STOP

Read the register 0x02 to 0x03.

START	Device Address 0xF0	ACK	Register Address 0x02	ACK	STOP

START	Device Address **0xF1**	ACK	Read Data 0x33	ACK	Read Data 0x22	ACK	STOP

From Master to Slave

From Slave to Master

.

7. Register List

7.1 I2C Register Map

Register Name	Addr. (HEX)	Register Function and Description							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
START_THD	00h	START_THD[7:0]							
STEP_THD	01h	STEP_THD[7:0]							
SENSITIVITY1	02h	Reserved	Ch1[2:0]			Reserved	Ch0[2:0]		
SENSITIVITY2	03h	Reserved	Ch3[2:0]			Reserved	Ch2[2:0]		
SENSITIVITY3	04h	Reserved	Ch5[2:0]			Reserved	Ch4[2:0]		
SENSITIVITY4	05h	Reserved	Ch7[2:0]			Reserved	Ch6[2:0]		
CTRL1	06h	MS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CTRL2	07h	Reserved	Reserved	Reserved	Reserved	SRST	SLEEP	Reserved	Reserved
REF_RST	08h	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
CH_HOLD	09h	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
OUTPUT1	0Ah	OUT3[1:0]		OUT2[1:0]		OUT1[1:0]		OUT0[1:0]	
OUTPUT2	0Bh	OUT7[1:0]		OUT6[1:0]		OUT5[1:0]		OUT4[1:0]	
GPIO_CTRL1	0Ch	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
GPIO_CTRL2	0Dh-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OUT1
STATE_CHECK	0Eh	STATE_CHECK[7:0]							
PMOD	1Dh	Reserved	Reserved	Reserved	Reserved	Reserved	PMOD[2:0]		
HOLD_TIME	1Eh	HOLD_TIME[7:0]							
OPTION_FUNC	1Fh	Reserved	Reserved	Reserved	MKN	FASTT	MKEY	RHOLD	KHOLD
HW_SUM_CNT	20h	HW_SUM_CNT[7:0]							
STOP_DELAY	23h	STOP_DELAY[7:0]							
STOP_WAKEL	24h	STOP_WAKEL[7:0]							
STOP_WAKECL	25h	STOP_WAKECL[7:0]							
CHATTER_NUM	26h	CHATTER_NUM[7:0]							
RELEASE_INT_DELAY	27h	RELEASE_INT_DELAY[7:0]							
SAVE_FS	2Ah	SAVE_FS[7:0]							
RECAL	FEh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECAL

7.2 Registers Description

7.2.1 Senitivity Control Register

START_THD (Start Threshold Control Register)

Address : 00h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
START_THD	00h	START_THD[7:0]							

Description

The default(initial) value for this register is 0x14 (Decimal number 20). User can set the start value of threshold.

Bit Name	Default	Function
START_THD [7:0]	0x14	0x00 : 0 0x01 : 1 … 0x13 : 19 0x14 : 20 (Default) … 0xFF : 255

STEP_THD (Step Threshold Control Register)

Address : 01h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STEP_THD	01h	STEP_THD[7:0]							

Description

The default(initial) value for this register is 0x14 (Decimal number 20). User can set the step value of threshold. The real threshold level value is calculated as 'start value(20) + step value(20) * sensitivity register's setting.'

Bit Name	Default	Function
STEP_THD [7:0]	0x14	0x00 : 0 0x01 : 1 … 0x13 : 19 0x14 : 20 (Default) … 0xFF : 255

SENSITIVIY1 (Channel 0 and 1 Sensitivity Control 1 Register)

Address : 02h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SENSITIVITY1	02h	Reserved	Ch1[2:0]			Reserved	Ch0[2:0]		

Description

The default(initial) value for this register is 0x33. The sensitivy of channel 0 and 1 are adjustable by the register SENSITIVY1. User can adjust the sensitivity with Chx[2:0] values.

The real threshold (initial setting) is 80 from 'start value(20) + step value(20) * sensitivity level (3).'
If START_THD = 0x64 (100), STEP_THD = 0x0A (10), SENSITIVITY = 0x05 (5), the calculated threshold is 150 from 100 + (10 * 5).

When user modifies the value of START_THD or STEP_THD register, please change the sensitivity register value again. Because the touch sensor reloads the value of START_THD and STEP_THD registers after the sensitivity register's value is changed.

Bit Name	Default	Function
Chx0[2:0]	011	Sensitivity Level Selection 000 : High (Thick Cover) 100 : 001 : 101 : 010 : 110 : 011 : Normal (Default) 111 : Low (Thin cover)

SENSITIVIY2 (Channel 2 and 3 Sensitivity Control 2 Register)

Address : 03h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SENSITIVITY2	03h	Reserved	Ch3[2:0]			Reserved	Ch2[2:0]		

Description

The default(initial) value for this register is 0x33. The sensitivy of channel 2 and 3 are adjustable by the register SENSITIVY2. User can adjust the sensitivity with Chx[2:0] values.

Bit Name	Default	Function
Chx0[2:0]	011	Sensitivity Level Selection 000 : High (Thick Cover) 100 : 001 : 101 : 010 : 110 : 011 : Normal (Default) 111 : Low (Thin cover)

SENSITIVIY3 (Channel 4 and 5 Sensitivity Control 3 Register)

Address : 04h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SENSITIVITY3	04h	Reserved	Ch5[2:0]			Reserved	Ch4[2:0]		

Description

The default(initial) value for this register is 0x33. The sensitivy of channel 4 and 5 are adjustable by the register SENSITIVY3. User can adjust the sensitivity with Chx[2:0] values.

Bit Name	Default	Function
Chx0[2:0]	011	Sensitivity Level Selection 000 : High (Thick Cover) 100 : 001 : 101 : 010 : 110 : 011 : Normal (Default) 111 : Low (Thin cover)

SENSITIVIY4 (Channel 6 and 7 Sensitivity Control 4 Register)

Address : 05h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SENSITIVITY4	05h	Reserved	Ch7[2:0]			Reserved	Ch6[2:0]		

Description

The default(initial) value for this register is 0x33. The sensitivy of channel 6 and 7 are adjustable by the register SENSITIVY4. User can adjust the sensitivity with Chx[2:0] values.

Bit Name	Default	Function
Chx0[2:0]	011	Sensitivity Level Selection 000 : High (Thick Cover) 100 : 001 : 101 : 010 : 110 : 011 : Normal (Default) 111 : Low (Thin cover)

7.2.2 General Control Register

CTRL1 (General Control 1 Register)

Address : 06h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRL1	06h	MS	Reserved						

Description

The default(initial) value for this register is 0x80. If the MS bis is clear and if the sleep mode is enabled (SLEEP bit at CTRL2), the sensing function can be operated with SLEEP mode (SNAP). If the MS bis is set, the sensing function will be operated alone without SLEEP mode.

Bit Name	Default	Function
MS	80h	Mode Selection 0 : Auto alternative (fast/slow) mode 1 : Fast mode

CTRL2 (General Control 2 Register)

Address : 07h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRL2	07h	Reserved				SRST	SLEEP	Reserved	

Description

The default(initial) value for this register is 0x00. All the digitial part and I2C part except of the analog part are reset when SRST bit is set. If he sleep mode is enabled, SLEEP bit is set, the current consumption can be getting very low. But the report time (response) time will be more longer than normal operation (Sleep mode disable).

Bit Name	Default	Function
SRST	0	Software Reset 0 : Software Reset Disable 1 : Software Reset Enable
SLEEP	0	Sleep Mode Enable 0 : Sleep Mode Disable 1 : Sleep Mode Enable

7.2.3 Channel Reference Reset Control Register

REF_RST (Channel Reference Reset Control 1 Register)

Address : 08h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REF_RST1	08h	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Description

The default(initial) value for this register is 0x00. The reference value of each channel will be renewing when chx is set.

Bit Name	Default	Function
Chx	0	0 : Reference Reset Disable 1 : Reference Reset Enable

7.2.4 Channel Sensing Hold Control Register

CH_HOLD (Hold Control 1 Register for Channel 0 ~ 7)

Address : 09h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH_HOLD1	09h	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Description

The default(initial) value for this register is 0x00. The operation of each channel is indepently available to control. When Chx bit is set, the operation of the sensing will be hold.

Bit Name	Default	Function
Chx	0	0 : Operation Enable (Sensing) 1 : Operation Hold (No Sensing)

7.2.5 Channel Sensing Hold Control Register

OUTPUT1 (Output Data 1 Register for Channel 0 ~ 3)

Address : 0Ah

Type : R (Read Only)

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUTPUT1	0Ah	OUT3[1:0]		OUT2[1:0]		OUT1[1:0]		OUT0[1:0]	

Description

The OUTx[1:0] data is the each channel's sensing result.

Bit Name	Default	Function
OUT3[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)
OUT2[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)
OUT1[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)
OUT0[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)

OUTPUT2 (Output Data 1 Register for Channel 4 ~ 7)

Address : 0Bh

Type : R (Read Only)

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUTPUT2	0Bh	OUT7[1:0]		OUT6[1:0]		OUT5[1:0]		OUT4[1:0]	

Description

The OUTx[1:0] data is the each channel's sensing result.

Bit Name	Default	Function
OUT3[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)
OUT2[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)
OUT1[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)
OUT0[1:0]	00	00 : No Output (Not Touched) 01 : Reserved 10 : Reserved 11 : High Output (Touched)

7.2.6 GPIO Control Register

GPIO_CTRL1 (GPIO Control & Data 1 Register for Channel 0 ~ 7)

Address : 0Ch

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GPIO_CTRL1	0Ch	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Description

The default(initial) value for this register is 0x00. If the some channel is in hold mode (refer to CH_HOLD1), this channel can output in digital output (high or low). But if the channel is in sensing mode, this channel cannot output.

Bit Name	Default	Function
Chx	0	0 : Low Level 1 : High Level

GPIO_CTRL2 (GPIO Control & Data 2 Register for LED 1 pin)

Address : 0Dh

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GPIO_CTRL2	0Dh	Reserved							OUT1

Description

The default(initial) value for this register is 0x01. If the some channel is in hold mode (refer to CH_HOLD), this channel can output in digital output (high or low). But if the channel is in sensing mode, this channel cannot output.

Bit Name	Default	Function
OUT1	1	0 : Low Level 1 : High Level

7.2.7 Function Control Register

STATE_CHECK (Chip Reset State Check Register)

Address : 0Eh

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATE_CHECK	0Eh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Description

The default(initial) value for this register is 0x00, and user can write the arbitrary value at this register. Then user reads this value for this register. If the read value doesn't equal to 0x00, this device was restarted (or reset).

Bit Name	Default	Function
Bitx	0x00	0x00 : Initial Value after reset (Default) Arbitray value except of 0x00 : User value

PMOD (IDLE Mode Duty Time Register)

Address : 1Dh

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PMOD	1Dh	Reserved					PMOD[2:0]		

Description

The default(initial) value for this register is 0x02. User can set the duty time of the IDLE mode with 8 steps. The device in the IDLE mode check the touch detection (once) every the duty time (ex : 300ms).

The total duty time for IDLE mode equals 100ms + (100ms * step value).

Bit Name	Default	Function
PMOD[2:0]	0x02	0x00 : 100ms 0x01 : 200ms 0x02 : 300ms (Default) 0x03 : 400ms 0x04 : 500ms 0x05 : 600ms 0x06 : 700ms 0x07 : 800ms

HOLD_TIME (Touch Key Hold Time Register)

Address : 1Eh

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HOLD_TIME	1Eh	HOLD_TIME[7:0]							

Description

The default(initial) value for this register is 0x0C. User can set the hold time for touch key pressed with 255 steps. If the touch key dectecting (pressed) time is greater than the hold time, the touch key is released and re-initialized.

The total hold time for touch key equals (1 second * step value).

Bit Name	Default	Function
HLOD_TIME [7:0]	0x0C	0x00 : 0s 0x01 : 1s 0x02 : 2s … 0x0B : 11s 0x0C : 12s (Default) 0x0D : 13s 0x0E : 14s … 0xFE : 254s 0xFF : 255s

OPTION_FUNC (Function Option Selection Register)

Address : 1Fh

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPTION_FUNC	1Fh	Reserved			MKN	FASTT	MKEY	RHOLD	KHOLD

Description

The default(initial) value for this register is 0x09. User can set the hold time enable for touched state or reverse touched state. And user can set the multi-key mode, fast baseline tracking, and multi-key noise mode.

Bit Name	Default	Function
KHOLD	1	Hold Time Enable Bit for Touched State 0 : Disable 1 : Enable (Default) Refer to the description of the HOLD_TIME Register. If this bit is 1 (Default) and the hold time for touched state is greater than the user hold time(HOLD_TIME register), the touch key is released and re-initialized.
RHOLD	0	Hold Time Enable Bit for Reverse Touched State 0 : Disable (Default) 1 : Enable We recommend that this option is set to 0 (Disable). If this bit is 1 (Enable) and the reversed touched time by the external noise is more than 200ms (fixed reverse hold time), the touch key is released and re-initialized.
MKEY	0	Multi-Key Mode Bit 0 : Single-key Mode (Default) 1 : Multi-key Mode
FASTT	1	Fast Baseline Tracking Option Bit 0 : 1 second 1 : 200ms (Default)
MKN	0	Multi Key Noise Bit 0 : Single Key Result Mode (Default) Return Single Key Result from the Multi-key (Default) 1 : Noise Mode Not Touched State (They're considered as the noise) If the multi-key state is occurred in single key mode, the result will be single key from these multi-key or not touched with this bit setting.

HW_SUM_CNT (Haredware Sum Count Register)

Address : 20h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HW_SUM_CNT	20h	HW_SUM_CNT[7:0]							

Description

The default(initial) value for this register is 0x02 (2 times). To increase the DIFF (Difference or Delta) value, user can user can set the hardware sum count. But because the sensing time is slower, the response time will be slower too and the power (current) consumption will be more increased.

Bit Name	Default	Function
HW_SUM_CNT [7:0]	0x01	Accumulated Count for Touch Sensing

STOP_DELAY (IDLE Mode Start Delay Time Register)

Address : 23h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STOP_DELAY	23h	STOP_DELAY[7:0]							

Description

The default(initial) value for this register is 0x03. User can set the delay time for starting the IDLE Mode. When the device starts the entrance to the IDLE mode in the ACTIVE mode, After the delay time was passed, the device will be in the IDLE mode.

The total delay time for starting the IDLE mode equals (500ms + 500ms * step value).

Bit Name	Default	Function
STOP_DELAY [7:0]	0x03	0x00 : 0.5s 0x01 : 1s 0x02 : 1.5s 0x03 : 2s (Default) 0x04 : 2.5s 0x05 : 3s … 0xFE : 127.5s 0xFF : 128s

STOP_WAKEL (IDLE Mode Wakeup Level Control Register)

Address : 24h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STOP_WAKEL	24h	STOP_WAKEL[7:0]							

Description

The default(initial) value for this register is 0x0A. User can set the wakeup level for the IDLE mode. The recommend value is 100% of threshold as the default value.

First, the device checks which the touch difference value is greater than the wakeup check level (ex: 50% from STOP_WAKECL) twice times in a row. If the check level detection event is occurred, then the device checks that the touch difference value is greater that the wakeup level (ex: 100% from STOP_WAKEL). If the level detection is occurred, the device will be wakeup from IDLE mode.

The total wakeup level for the IDLE mode equals (10% of the threshold * step value).

Bit Name	Default	Function
STOP_WAKEL [7:0]	0x0A	0x00 : 0% 0x01 : 10% … 0x09 : 90% 0x0A : 100% (Default) 0x0B : 110% … 0xFF : 2,550%s

STOP_WAKECL (IDLE Mode Wakeup Check Level Control Register)

Address : 25h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STOP_WAKECL	25h	STOP_WAKECL[7:0]							

Description

The default(initial) value for this register is 0x05. User can set the wakeup check level for the IDLE mode. The recommend value is 50% of threshold as the default value. In more detail information, please refer to the STOP_WALEL register.

The total wakeup check level for the IDLE mode equals (10% of the threshold * step value).

Bit Name	Default	Function
STOP_WAKECL [7:0]	0x05	0x00 : 0% 0x01 : 10% … 0x05 : 50% (Default) 0x06 : 60% … 0xFF : 2,550%s

CHATTER_NUM (Chattering Number Register)

Address : 26h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHATTER_NUM	26h	STOP_WAKEL[7:0]							

Description

The default(initial) value for this register is 0x02. User can set the chattering number for the touch key state. The recommend value is 2 times (0x02). The same key has to detect more than the chattering number in a row.

Bit Name	Default	Function
CHATTER_NUM [7:0]	0x02	0x00 : None 0x01 : 1 Time 0x02 : 2 Times (Default) 0x03 : 3 Times … 0xFF : 255 Times

RELEASE_INT_DELAY (Release Interrupt Delay Time Register)

Address : 27h

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RELEASE_INT_DELAY	27h	RELEASE_INT_DELAY[7:0]							

Description

The default(initial) value for this register is 0x14. User can set the delay time for interrupt output at release event. When the releaseevent is occurred, the interrupt output pin will be low pulse after delay time (default : 20ms). The total delay time for interrupt output at release event equals (1ms * step value; Max. 255ms).

Note : This register setting data can not be saved by SAVE_FS register. It means that host should always send the setting of this register each power on or reset.

Bit Name	Default	Function
RELEASE_INT_DELAY [7:0]	0x14	0x00 : 0ms 0x01 : 1ms 0x02 : 2ms … 0x14 : 20ms (Default) 0x15 : 21ms … 0xFE : 254ms 0xFF : 255ms

SAVE_FS (Save at FLASH Memory Control Register)

Address : 2Ah

Type : R/W

Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SAVE_FS	2Ah	SAVE_FS[7:0]							

Description

The default(initial) value for this register is 0x00. When user write the value 0xAA to the SAVE_FS register. the current setting for touch sensing is written to the FLASH memory. If the device is reset by hardware, the device will read the setting at the FLASH memory.

Bit Name	Default	Function
SAVE_FS [7:0]	0x00	0x00 : None (Default) 0xAA : Save the Current Touch Setting to the FLASH. 0x5A : Save the H/W Calibration Setting to the FLASH

RECAL (Recalibration Control Register)

Address : FEh

Type : W (Write Only)

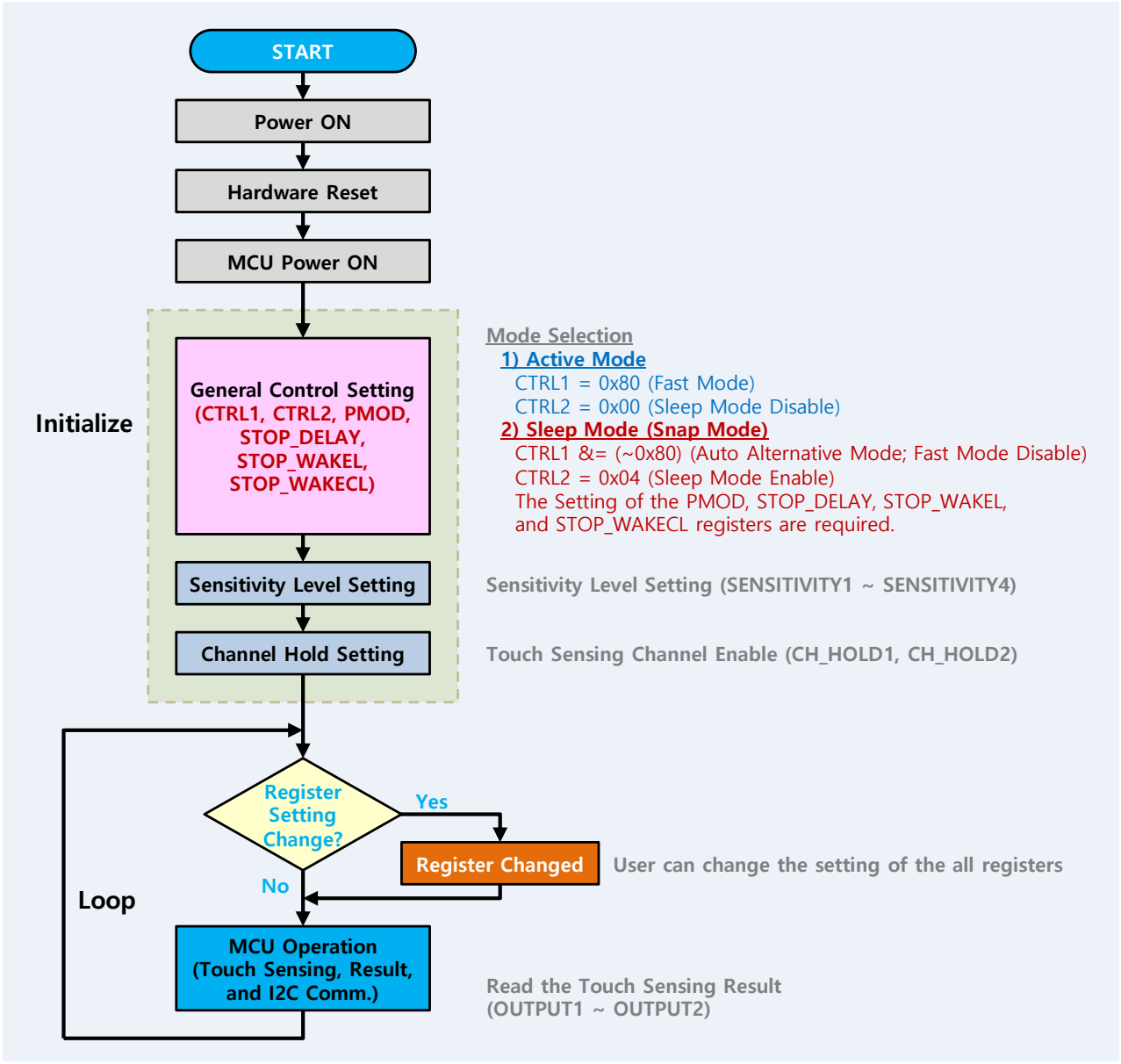
Register Name	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RECAL	FEh	Reserved							RECAL

Description

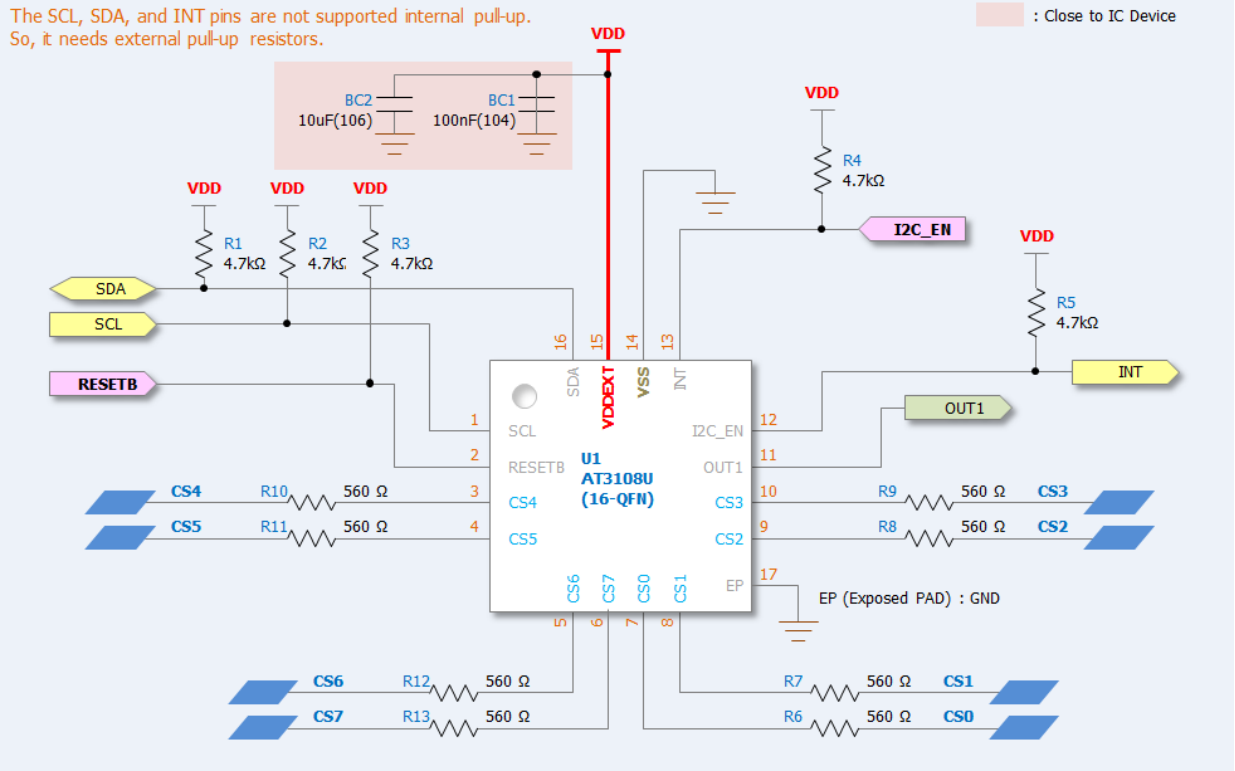
The default(initial) value for this register is 0x00. User can run the recalibration for the Touch Sensing.

Bit Name	Default	Function
RECAL	0	0 : None (Default) 1 : Run the Re-calibration for the Touch Sensing

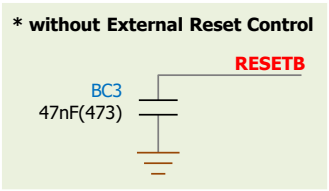
8. Recommended Flow (Example)



9. Recommended Circuit Design



1) The threse three pins (SDA, SCL, and I2C_EN) are open-drain output. Then, these pins needs pull-up resistors. But if the host has already pull-up resistors, these pull-up resistors at slave don't be needed.
2) The output pin is needed, OUT1(#11).
3) The I2C_EN pin have to low before START condition starts for I2C communication.
4) When the digital input level of the RESETB pin is low, hardware reset will be run(Active Low) .
If the external reset control is not needed, please connect the capacitor (47nF) for stable operation.



5) The recommended value of channel resistor is 560 Ohms (can use 1k Ohm).
In PCB layout design, channel resistor have to place besides the touch sensor device.
6) The bypass capacitors (Decoupling) have to place besides the touch sensor device too.

10. Ordering Information

Device Nomenclature