ABOV SEMICONDUCTOR
16 SEGMENT X 12 GRID VFD DRIVER WITH KEYSCAN

MC3401A
MC3411A

Data Sheet (Ver. 1.10)

Version 1.10

Published by
FAE Team

REVISION HISTORY

VERSION 1.10 (2013. 02. 28) This book.
Internal pull-down resistors for SGn and GRn are enhanced in size, width and contact number.
(Typ. 50 kΩ → 70 kΩ)

VERSION 1.0 (2011. 09. 08)
The first Edition

NOTE:

QFN Type Package has a bonding pad at the bottom. Bonding pad exists outside. This is to improve heat radiating for IC. Also this is connected to substrate. Generally Substrate is connected to lowest voltage of IC. Lowest level is VEE.
Therefore, Do not connect to VSS. Also You don’t need to connect to anywhere or if you want to connect, you must connect to VEE.

DESCRIPTION

MC3401A/3411A is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/12 duty factor. Sixteen segment output lines, 4 grid output lines, 8 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer.
Serial data is fed to MC3401A/3411A via a three-line serial interface.
MC3401A is housed in a 44-pin LQFP
MC3411A is housed in a 48-pin QFN

FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (16 x 2 matrix)
- Multiple Display Modes: (16 segments, 12 digits to 24 segments, 4 digits)
- 8-Step Dimming Circuitry
- LED Ports Provide (4 channels, 20mA max.)
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 44-pin LQFP(MC3401A), 48-pin QFN(MC3411A)

APPLICATION

- Microcomputer Peripheral Devices
- Digital Audio/Video system : CD/MD/VCD/DVD players
- Car audio
- VCR
- Electric scale meter
- P.O.S.
- Electronic equipment with instructional display

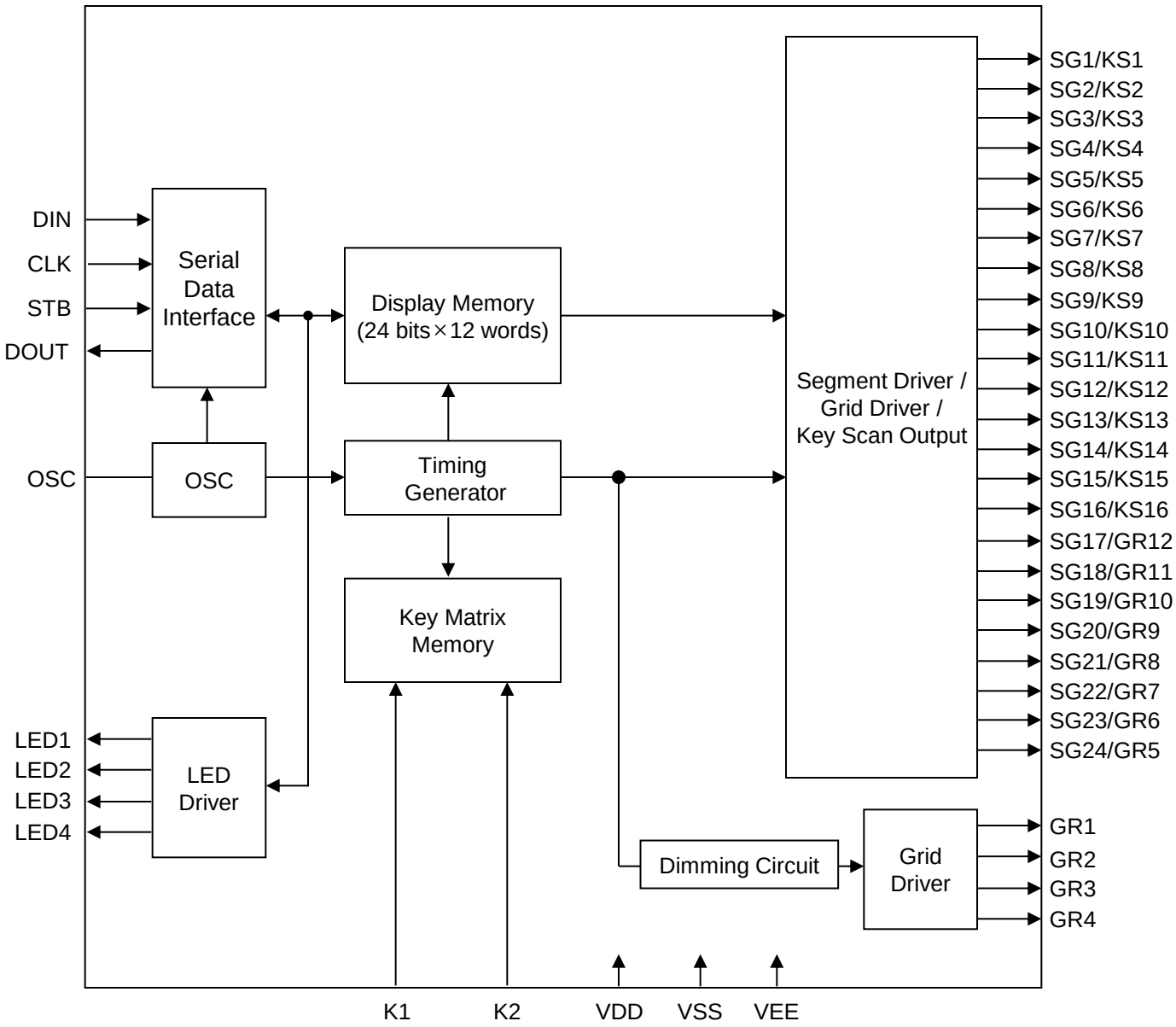
ORDERING INFORMATION

Device name	Segment	Grid	Key Scanning	PKG TYPE
MC3401AL	24 Segments	12 Grid	16 x 2 matrix	44LQFP
MC3411AU	24 Segments	12 Grid	16 x 2 matrix	48QFN

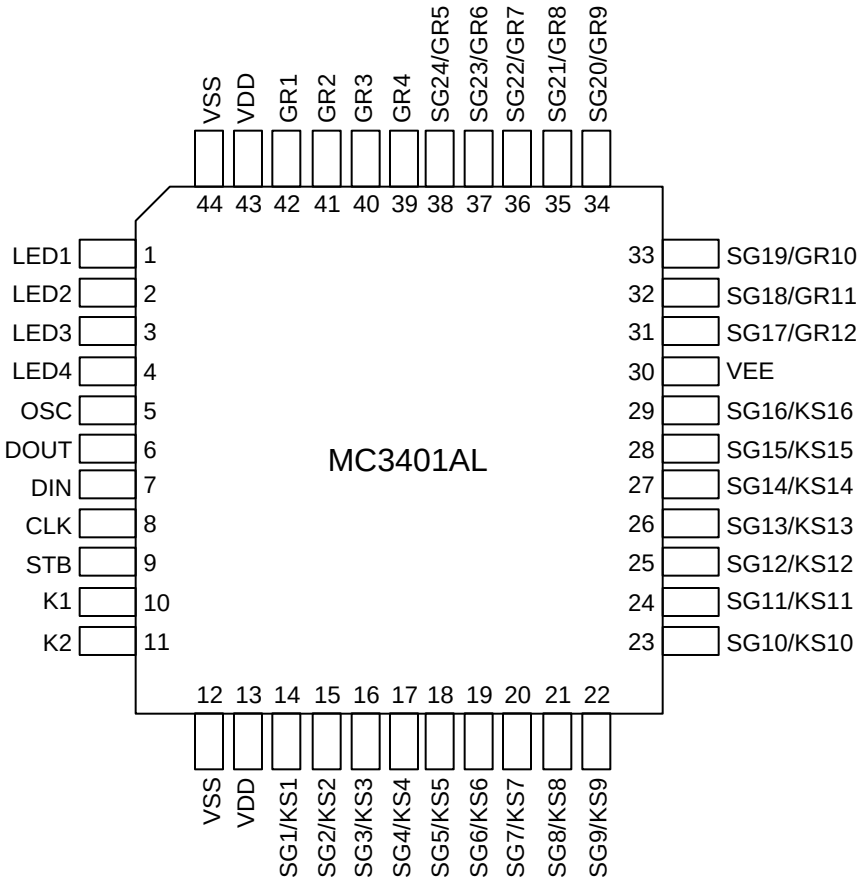
PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION	PIN No. (MC3401A)	PIN No. (MC3411A)
LED1 to LED4	O	LED Output Pin	1 to 4	1 to 4
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation Frequency.	5	5
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit)	6	7
DIN (Schmitt Trigger)	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	7	8
CLK (Schmitt Trigger)	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge of the shift clock	8	9
STB (Schmitt Trigger)	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is “HIGH”, CLK is ignored.	9	10
K1 to K2	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	10, 11	11, 12
VSS	-	Logic Ground Pin	12, 44	13, 48
VDD	-	Logic Power Pin	13, 43	14, 47
SG1/KS1 to SG16/KS16	O	High-Voltage Segment Output Pins Also acts as the Key Source.	14 to 29	15 to 32
VEE	-	Pull-Down Level	30	33
SG17/GR12 to SG24/GR5	O	High-Voltage Segment/Grid Output Pins	31 to 38	34 to 41
GR4 to GR1	O	High-Voltage Grid Output Pins	39 to 42	43 to 46

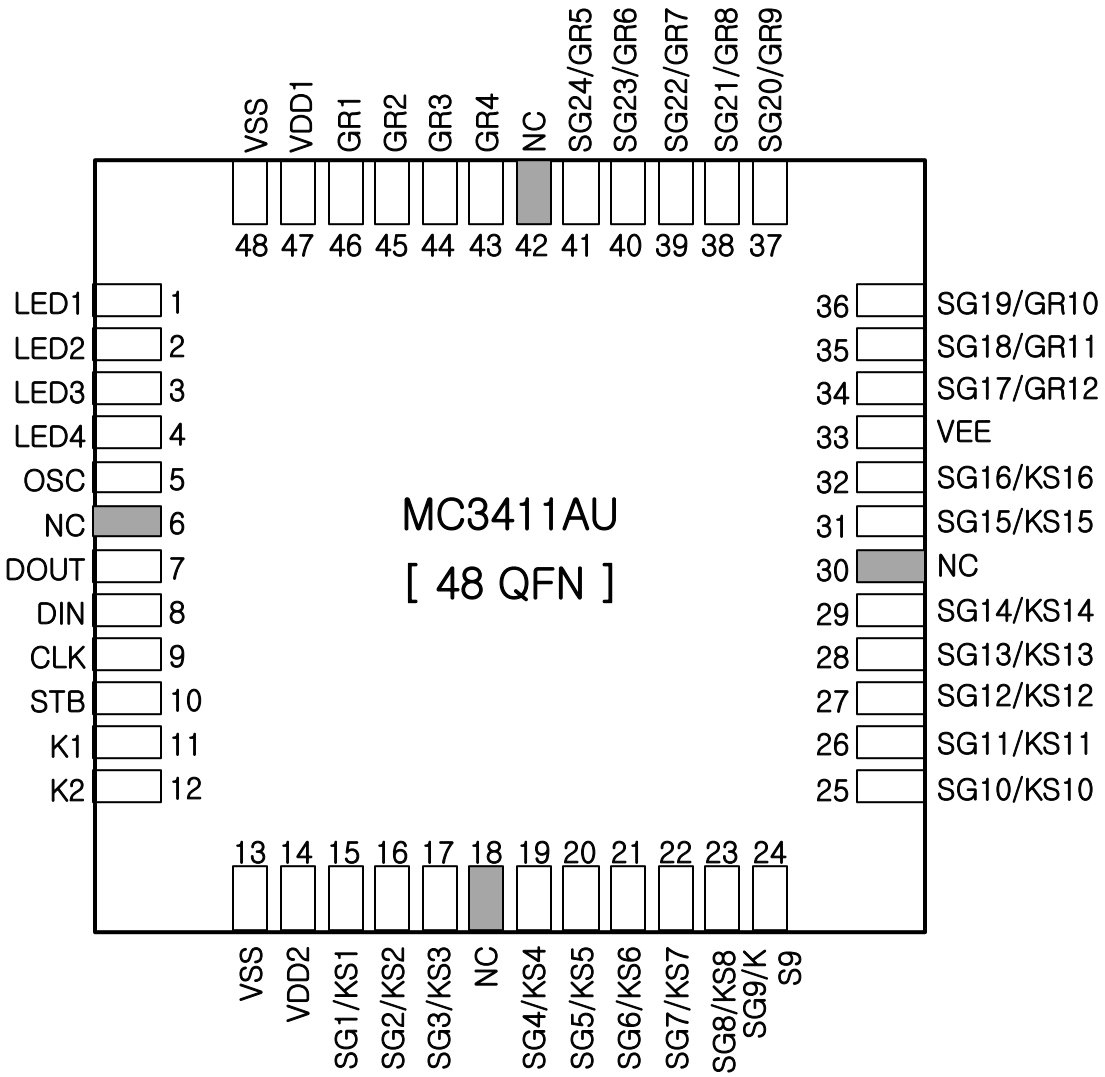
BLOCK DIAGRAM



PIN CONFIGURATION



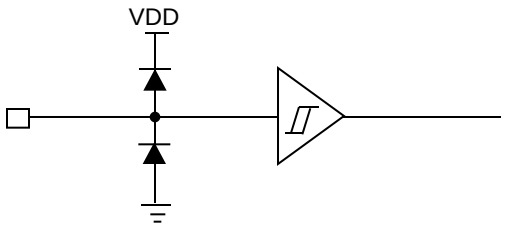
PIN CONFIGURATION



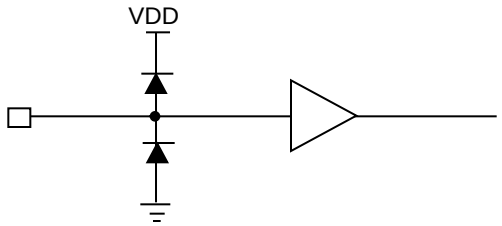
VDD1 : Grid Power
VDD2 : Logic Power
NC: No connect

INPUT/OUTPUT PINS SCHEMATIC DIAGRAM

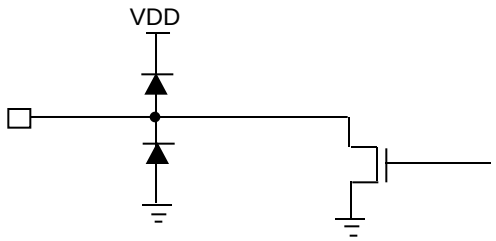
Input pins : CLK,STB,DIN



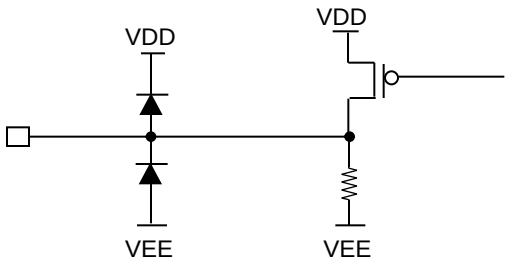
Input pins : K1,K2



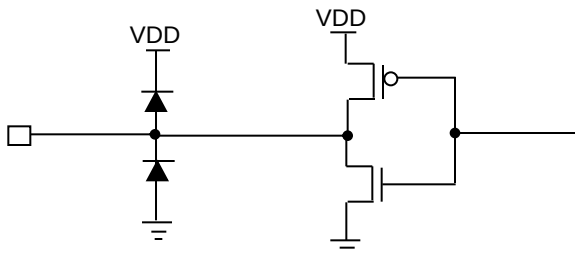
Output pin : DOUT



Output pins : SGn, GRn



Output pins : LED1 to LED4



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
Driver Supply Voltage	VEE	VDD+0.3 to VDD-40	V
Logic Input Voltage	VI	-0.3 to VDD+0.3	V
VFD Driver Output Voltage	VO	VEE-0.3 to VDD+0.3	V
LED Driver Output Voltage	IOLED	±20	mA
VFD Drive Output Current	IOVFD	-40 (Grid) -15 (Segment)	mA
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 to +150	℃
VDD (MC3401A)	-	Logic Power Pin	13, 43
VDD (MC3411A)	-	Logic Power Pin	14, 47

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta= 25℃, GND=0V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	3.0	5	5.5	V
High-Level Input Voltage	VIH	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V
Driver Supply Voltage	VEE	VDD-35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOHLED	IOHLED = -12mA LED1 to LED4	VDD-1	-	-	V
Low-Level Output Voltage	VOLLED	IOLLED = +15mA LED1 to LED4	-	-	1	V
Low-Level Output Voltage	VOLDOUT	IOLDOUT = 4mA DOUT	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD – 2V SG1/KS1 to SG16/KS16	-3	-	-	mA
High-Level Output Current	IOHGR	VO = VDD – 2V GR1 to GR8, SG17/GR12 to SG24/GR5	-15	-	-	mA
Oscillation Frequency	fosc	R=82KΩ	350	500	650	KHz
Schmitt-Trigger Transfer Voltage (+)	VT+	VDD = 5V DIN, CLK, STB	2.7	3	3.3	V
Schmitt-Trigger Transfer Voltage (-)	VT-	VDD = 5V DIN, CLK, STB	0.7	1.0	1.3	V
Hysteresis Voltage	Vhys	VDD = 5V DIN, CLK, STB	1.4	2.0	-	V
Input Current	II	VI = VDD or VSS	-	-	±1	uA
Dynamic Current Consumption	IDDdyn	Under no load Display Off	-	-	5	mA

Note : The frequency value is for MC3401A/3411A test condition : fosc = 224/T (see page 13 for detailed data)

ELECTRICAL CHARACTERISTICS

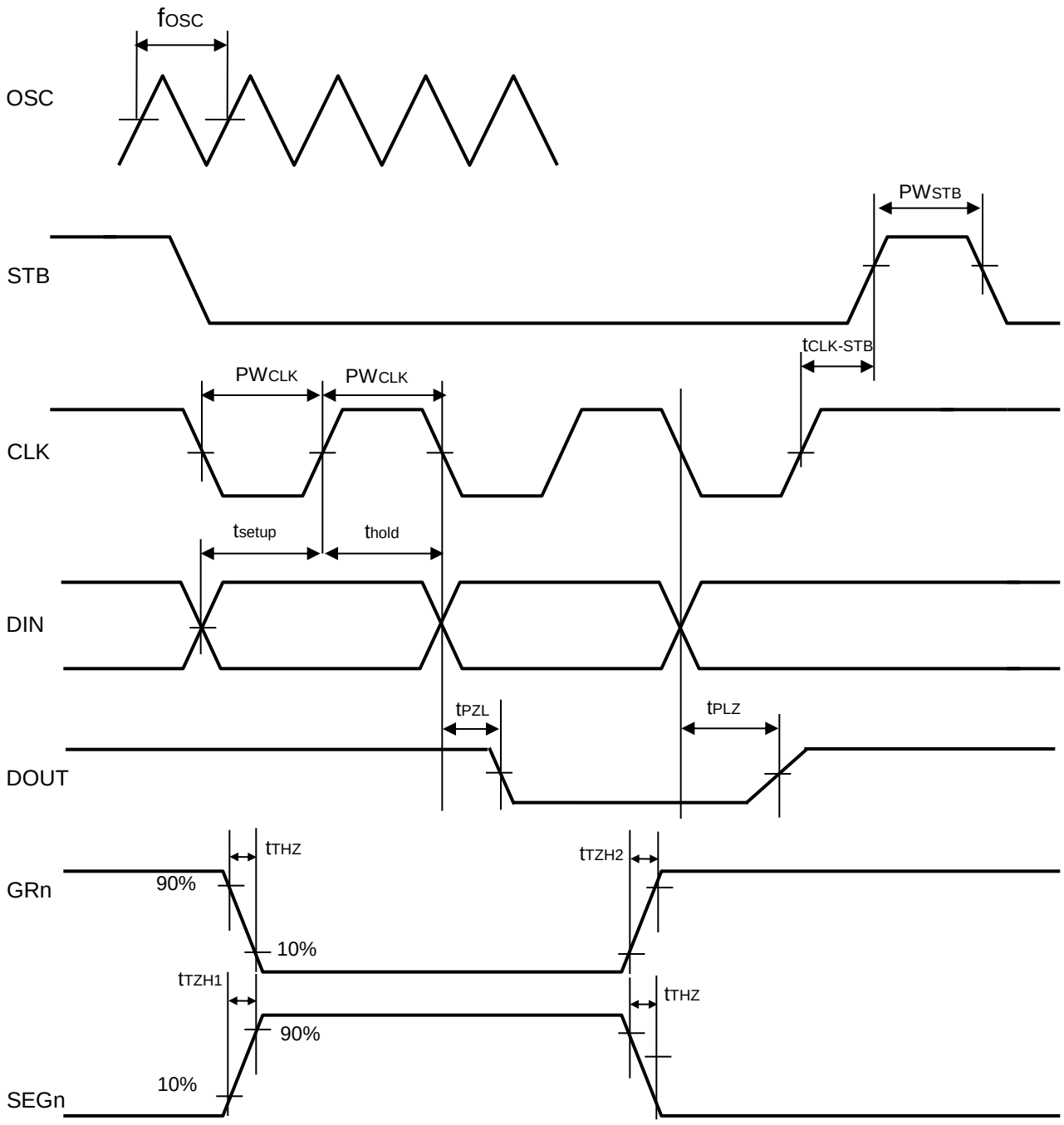
(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOHLED	IOHLED = -6mA LED1 to LED4	VDD-1	-	-	V
Low-Level Output Voltage	VOLLED	IOLLED = +15mA LED1 to LED4	-	-	1	V
Low-Level Output Voltage	VOLDOUT	IOLDOUT = 4mA DOUT	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD – 2V SG1/KS1 to SG16/KS16	-1.5	-	-	V
High-Level Output Current	IOHGR	VO = VDD – 2V GR1 to GR8, SG17/GR12 to SG24/GR5	-6	-	-	mA
Oscillation Frequency	fosc	R=82KΩ	350	500	650	KHz
Schmitt-Trigger Transfer Voltage (+)	VT+	VDD = 5V DIN, CLK, STB	1.8	2.0	2.2	V
Schmitt-Trigger Transfer Voltage (-)	VT-	VDD = 5V DIN, CLK, STB	0.2	0.4	0.6	V
Hysteresis Voltage	Vhys	VDD = 5V DIN, CLK, STB	1.0	1.6	-	V
Input Current	II	VI = VDD or VSS	-	-	±1	uA
Dynamic Current Consumption	IDDdyn	Under no load Display Off	-	-	3	mA

Note : The frequency value is for MC3401A/3411A test condition : fosc = 224/T (see page 13 for detailed data)

SWITCHING CHARACTERISTIC WAVEFORM

MC3401A/3411A Switching Characteristics Waveform is given below.



PW $_{CLK}$ (Clock Pulse Width) ≥400ns
t setup (Data Setup Time) ≥ 100ns
t $_{CLK-STB}$ (Clock - Strobe Time) ≥ 1㎲
t $_{TZH2}$ (Grid Rise Time) ≤ 0.5㎲ (VDD=5V)
t $_{TZH2}$ (Grid Rise Time) ≤ 1.2㎲ (VDD=3.3V)
t $_{TZH1}$ (Segment Rise Time) < 2.0㎲ (VDD=5V)
t $_{TZH1}$ (Segment Rise Time) < 4.0㎲ (VDD=3.3V)

PW$_{STB}$ (Strobe Pulse Width) ≥ 1㎲
thold (Data Hold Time) ≥ 100ns
t $_{THZ}$ (Fall Time) ≤ 150㎲
t $_{PZL}$ (Propagation Delay Time) ≤ 100ns
t $_{PLZ}$ (Propagation Delay Time) ≤ 400ns (VDD=5V)
t $_{PLZ}$ (Propagation Delay Time) ≤ 400ns (VDD=3.3V)
fosc = Oscillation Frequency

FUNCTIONAL DESCRIPTION

COMMANDS

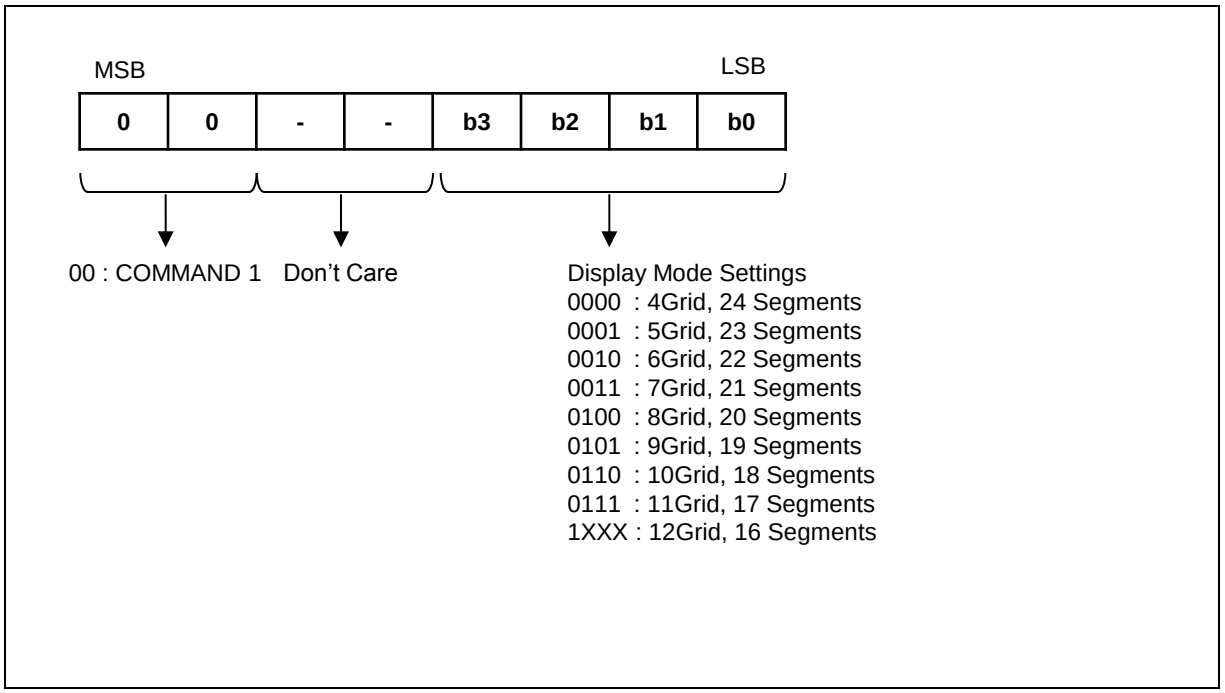
Commands determine the display mode and status of MC3401A/3411A. A command is the first byte (b0 to b7) inputted to MC3401A/3411A via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1 : DISPLAY MODE SETTING COMMAND

MC3401A/3411A provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to MC3401A/3411A via the DIN Pin when STB is “LOW”. However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to1/12 duty, 16 to 24 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 12-digit, 16-segment modes is selected.



Display Mode and RAM Address

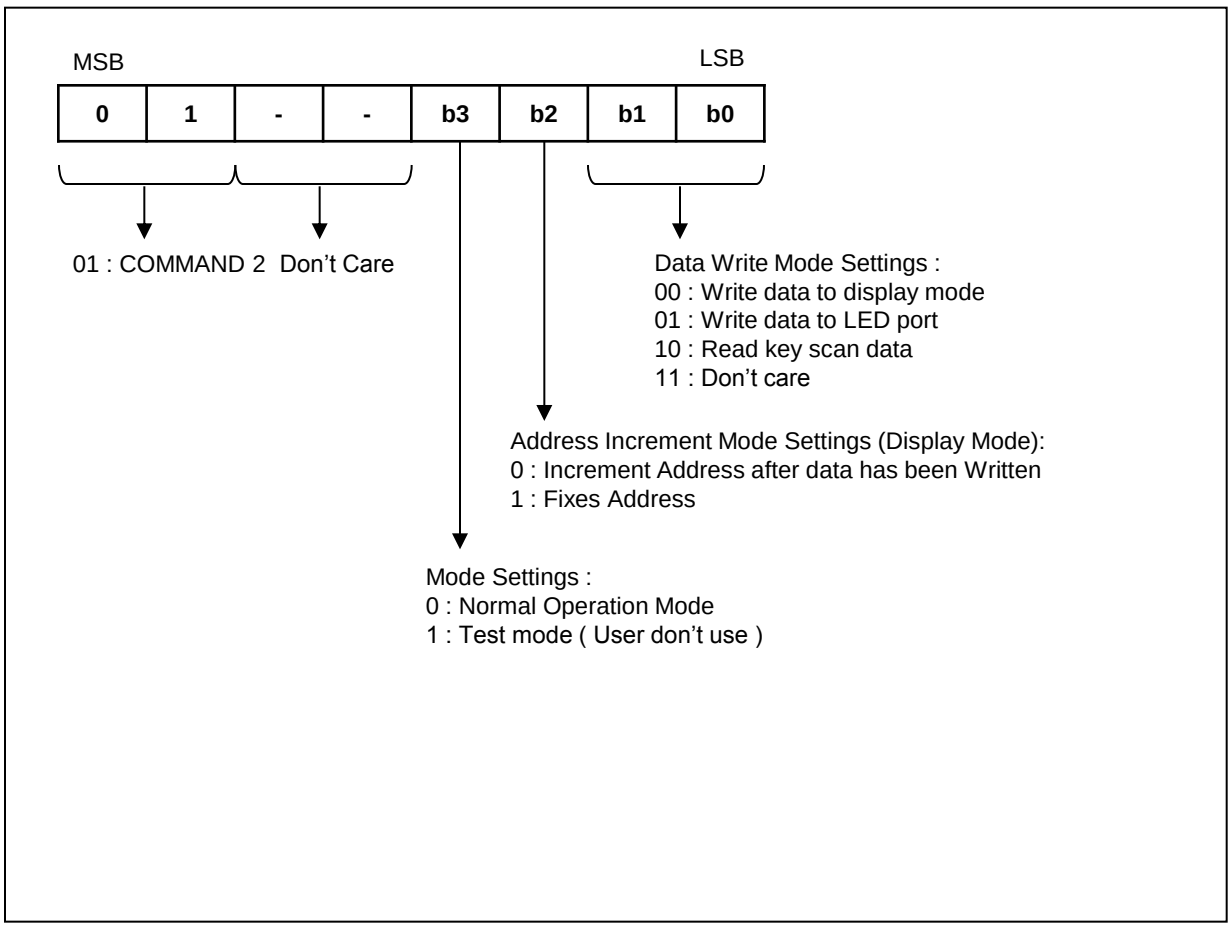
Data transmitted from an external device to MC3401A/3411A via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of MC3401A/3411A are given below in 8bits unit.

SG1 SG4	SG5 SG8	SG9 SG12	SG13 SG16	SG1 7 SG20	SG21 SG24	
$00H_L$	$00H_U$	$01H_L$	$01H_U$	$02H_L$	$02H_U$	DIG1
$03H_L$	$03H_U$	$04H_L$	$04H_U$	$05H_L$	$05H_U$	DIG2
$06H_L$	$06H_U$	$07H_L$	$07H_U$	$08H_L$	$08H_U$	DIG3
$09H_L$	$09H_U$	$0AH_L$	$0AH_U$	$0BH_L$	$0BH_U$	DIG4
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$	$0EH_L$	$0EH_U$	DIG5
$0FH_L$	$0FH_U$	$10H_L$	$10H_U$	$11H_L$	$11H_U$	DIG6
$12H_L$	$12H_U$	$13H_L$	$13H_U$	$14H_L$	$14H_U$	DIG7
$15H_L$	$15H_U$	$16H_L$	$16H_U$	$17H_L$	$17H_U$	DIG8
$18H_L$	$18H_U$	$19H_L$	$19H_U$	$1AH_L$	$1AH_U$	DIG9
$1BH_L$	$1BH_U$	$1CH_L$	$1CH_U$	$1DH_L$	$1DH_U$	DIG10
$1EH_L$	$1EH_U$	$1FH_L$	$1FH_U$	$20H_L$	$20H_U$	DIG11
$21H_L$	$21H_U$	$22H_L$	$22H_U$	$23H_L$	$23H_U$	DIG12

COMMAND 2 : DATA SETTING COMMAND

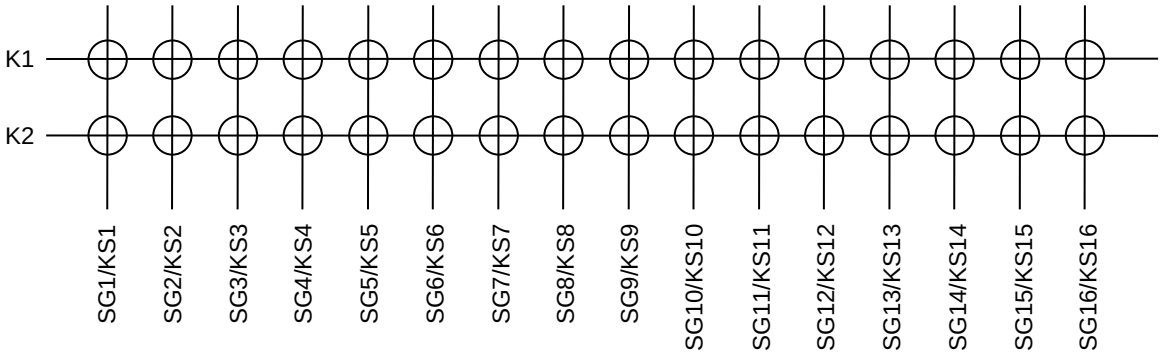
The Data Setting Commands executes the Data Write or Data Read Modes for MC3401A/3411A.
The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of “0”.



MC3401A/3411A Key Matrix & Key Input Data Storage RAM

MC3401A/3411A key matrix consists of 16×2 array as shown bellows.



Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG16, b7) has been read, the least significant bit of the next data (SG1, b0) is read.

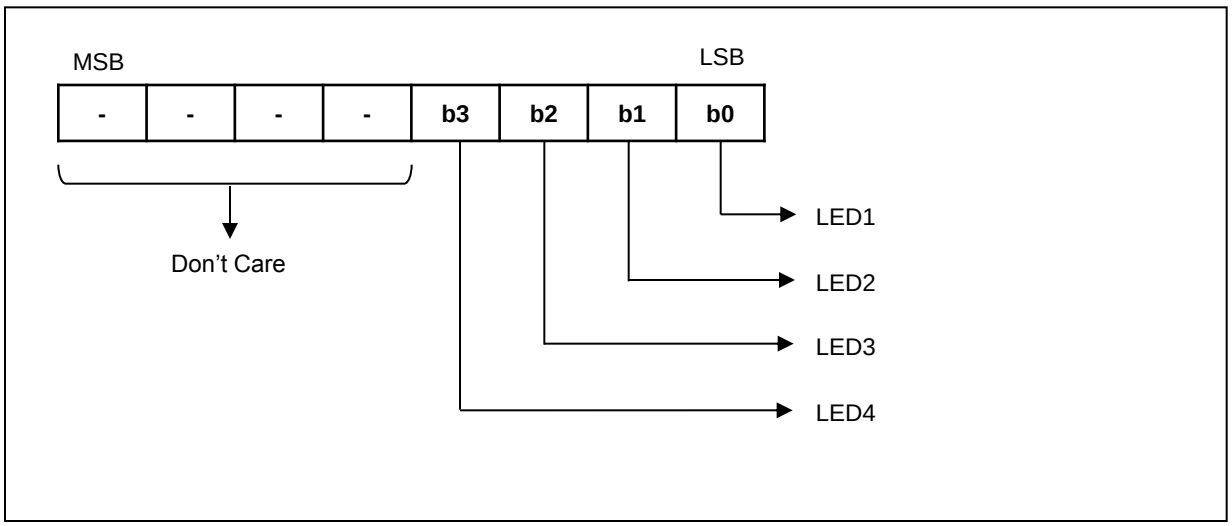
K1 …… K2	K1 …… K2	K1 …… K2	K1 …… K2
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10	SG11/KS11	SG12/KS12
SG13/KS13	SG14/KS14	SG15/KS15	SG16/KS16
b0 …… b1	b2 …… b3	b4 …… b5	b6 …… b7

Reading Sequence

LED Display

MC3401A/3411A provides 4 LED Display Terminals, namely LED1 to LED4. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal – b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 4 LED display terminals, bits 5 to 8 (b4 ~ b7) are not used and therefore ignored. This means that b4 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

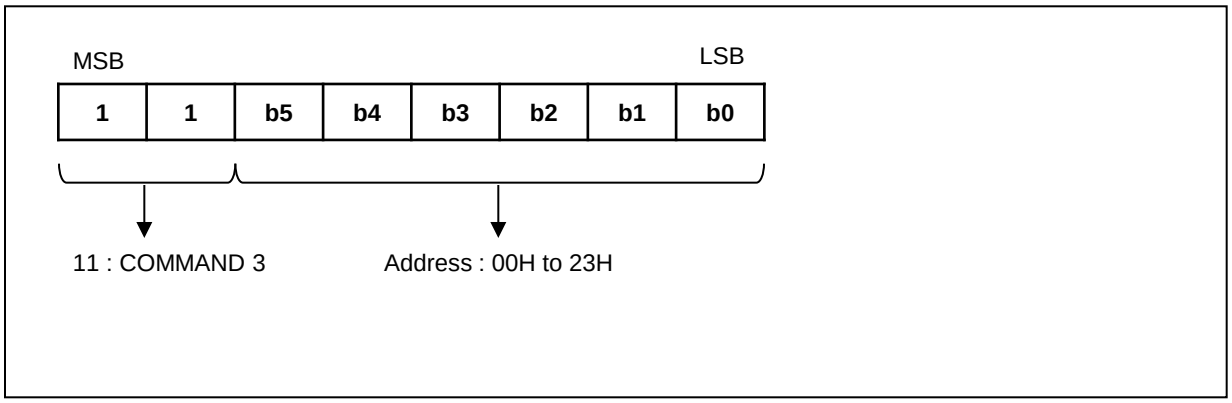
When a bit (b0 ~ b3) in the LED Port is “1”, the corresponding LED is OFF. Conversely, when the bit is “0”, the LED Display is turned ON. For example, Bit 1 (as designated by b0) has the value of “1”, then this means that LED1 is OFF. **It must be noted that when power is turned ON, bit 1 to bit 4 (b0 to b3) are given the value of “0” (all LEDs are turned ON). Please** refer to the diagrams below.



COMMAND 3 : ADDRESS SETTING COMMAND

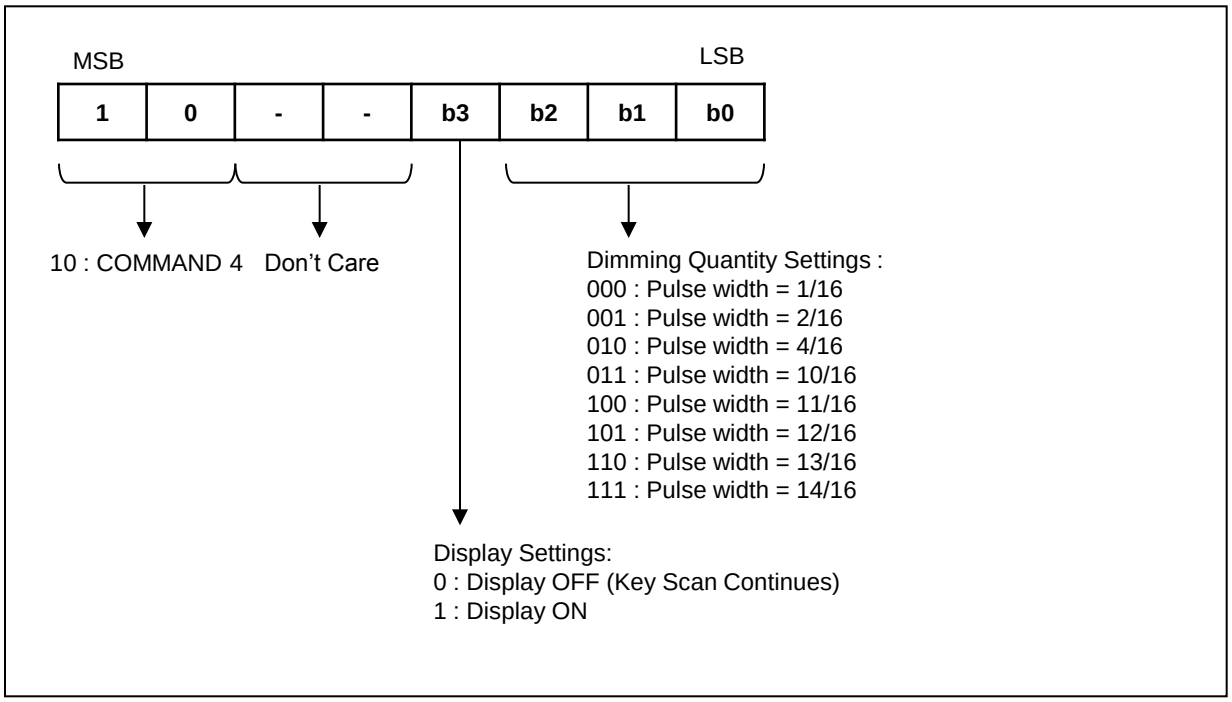
The display memory is addressed by Address Setting Command. The valid address range is “00H” to 23H”. If the address is set to 24H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



COMMAND 4 : DISPLAY CONTROL COMMANDS

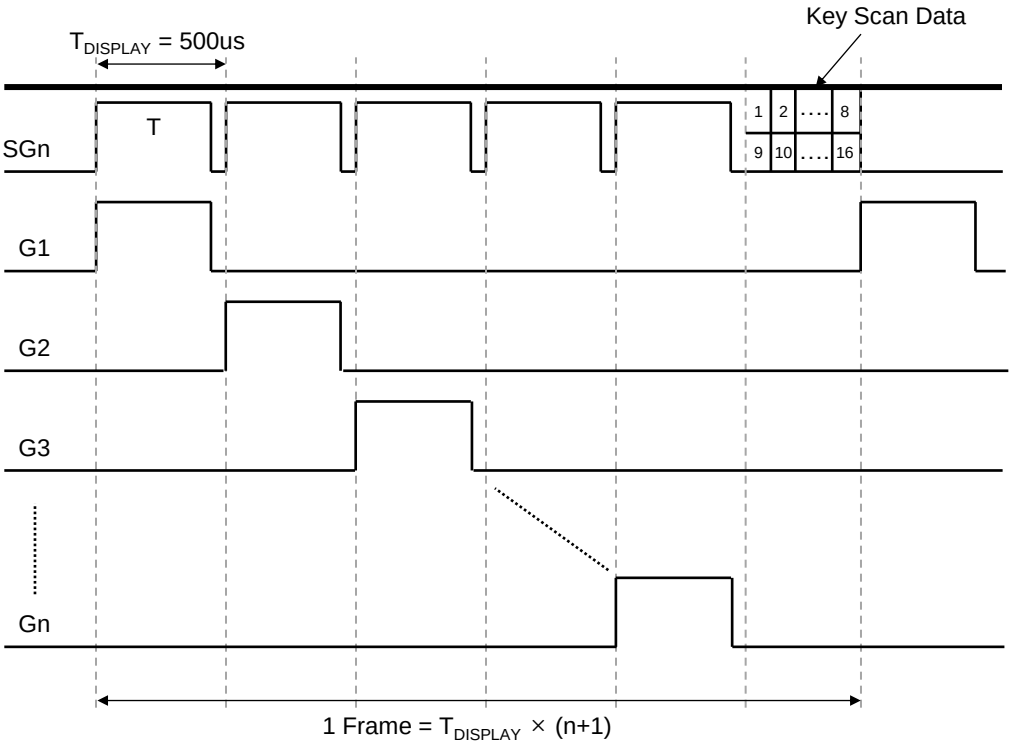
The Display Control Commands are used to turn ON or OFF a display. It is also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the display is turned OFF (the key scanning is stopped).



SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 16 x 2 matrix is stored in the RAM.

Internal Operating Frequency (fosc) = 224/T

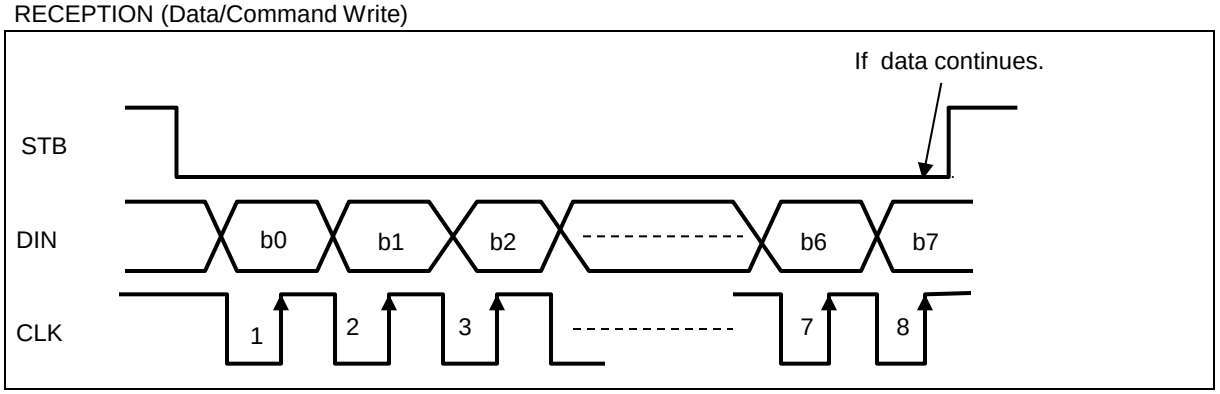


Note : T is the width of segment only

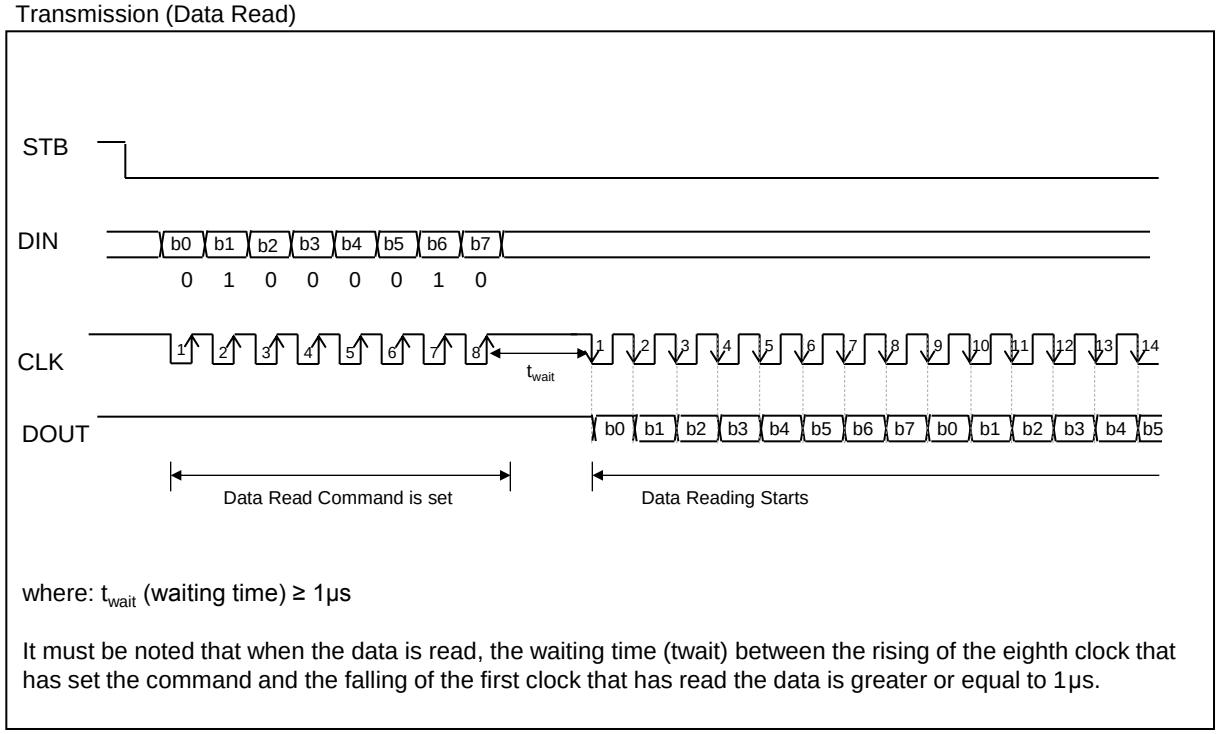
SERIAL COMMUMICATION FORMAT

The following diagram shows the MC3401A/3411A serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1KΩ to10KΩ) must be connected to DOUT.

RECEPTION (Data/Command Write)



Transmission (Data Read)

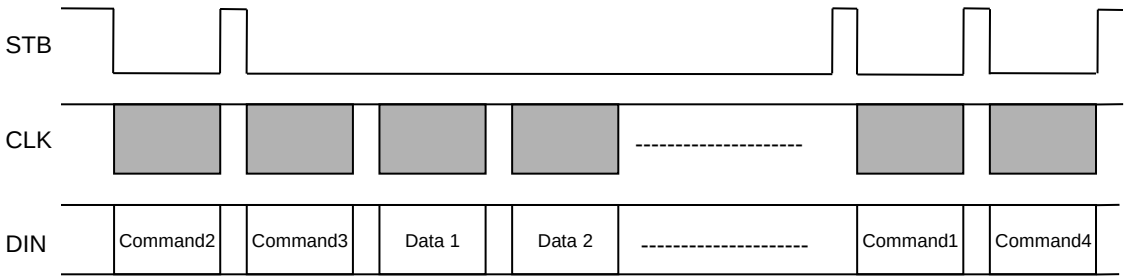


where: t_{wait} (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

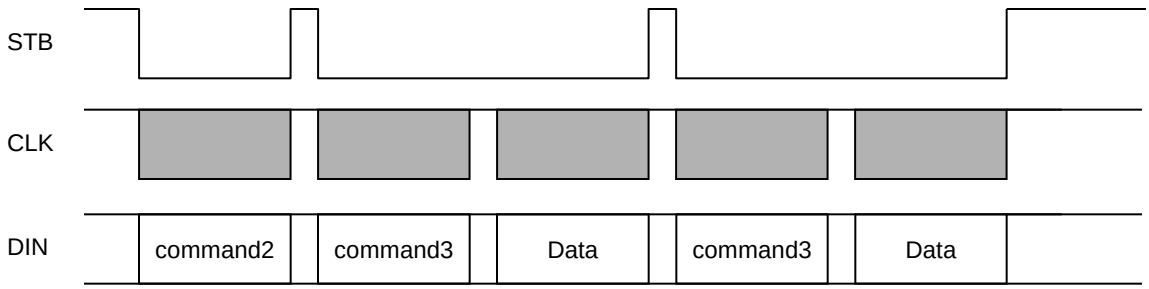
SERIAL COMMUNICATION EXAMPLES

Serial communication timing diagram for initialization setting.



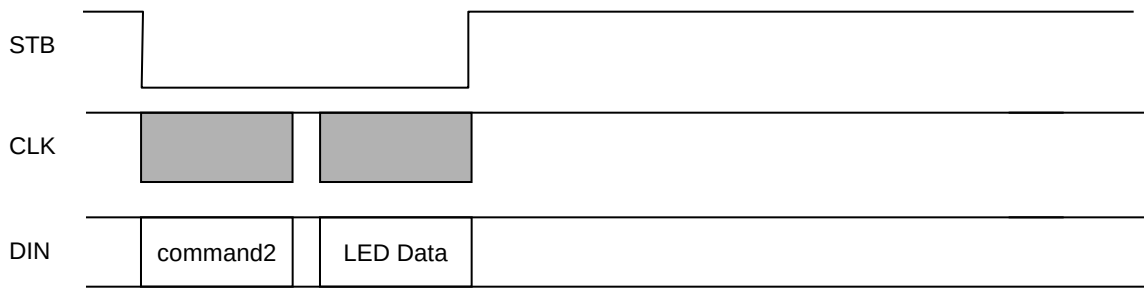
Where : Command 1 : Display Mode Setting
Command 2 : Data Setting Command
Command 3 : Address Setting Command
Data 1 to n : Transfer Display Data (36 Bytes max.)
Command 4 : Display Control Command

Transmission diagram for new Data on specific addresses.



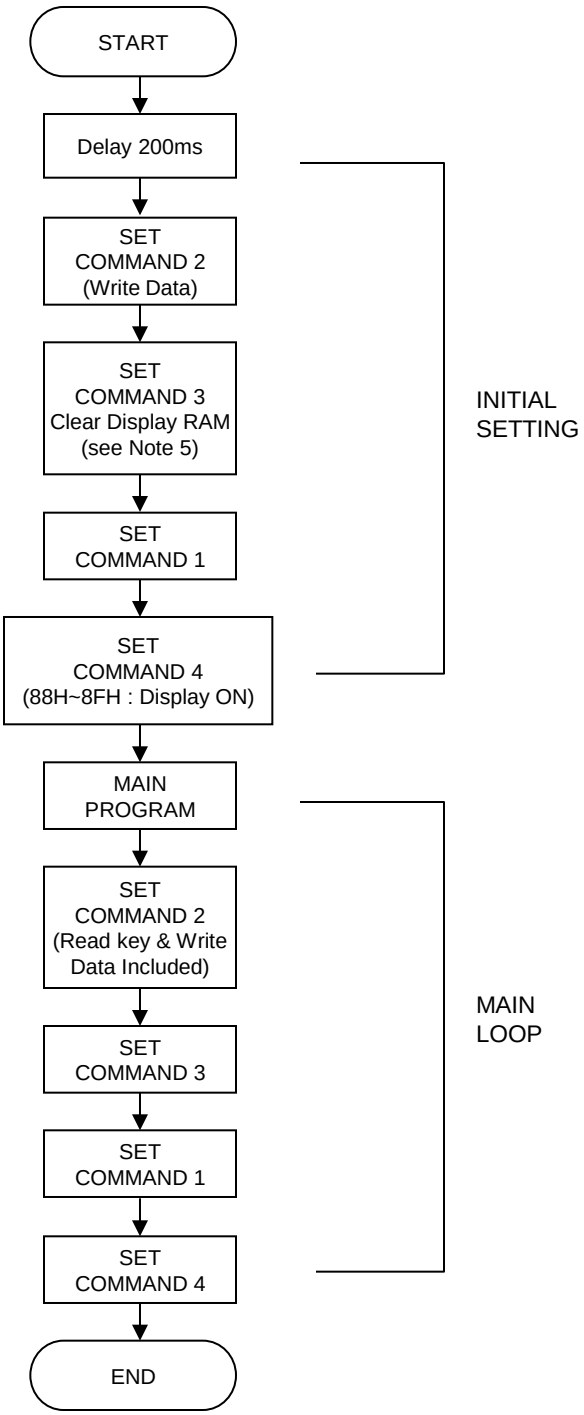
Where : Command 2 -- Data Setting Command
Command 3 -- Address Setting Command
Data -- Display Data

Transmission diagram for LED Data setting diagram.



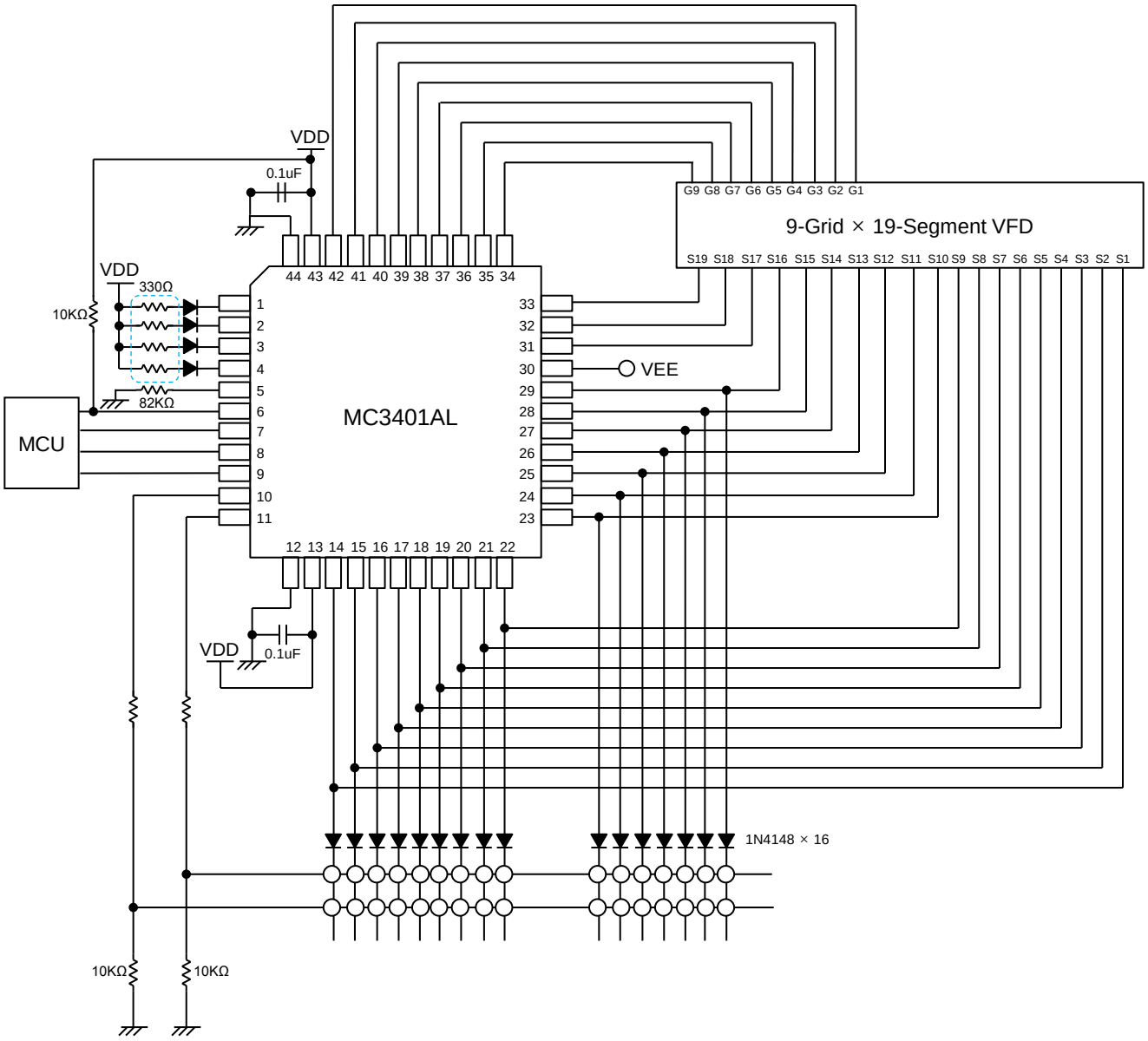
Where : Command 2 -- Data Setting Command
LED Data – 4 LED(LED1 to LED4) Display Data
(bit value 0: LED is turned ON, bit value 1: LED is turned OFF)

RECOMMENDED SOFTWARE PROGRAMMING FLOW CHART



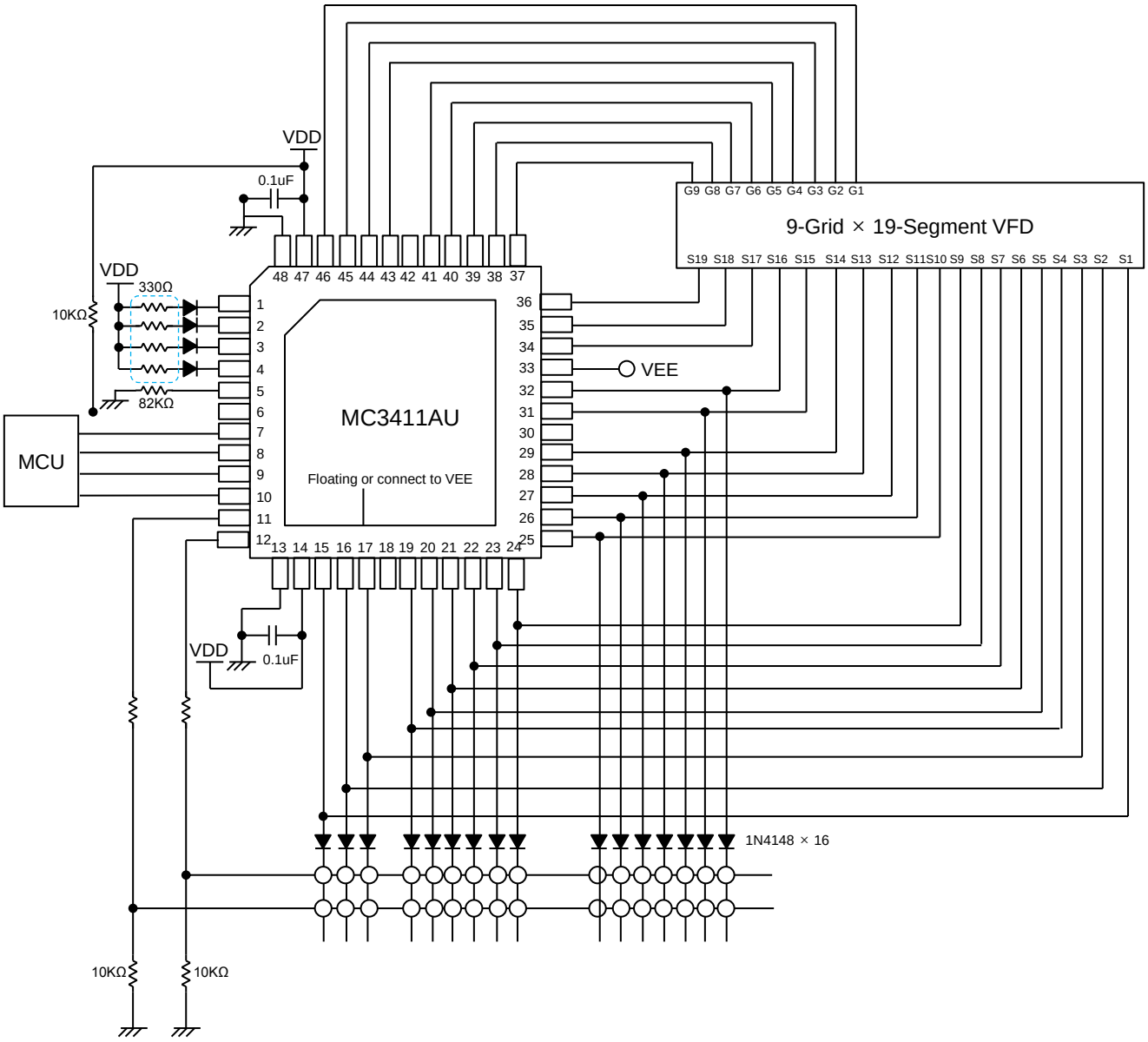
- Note : 1. Command 1 : Display Mode Setting
  2. Command 2 : Data Setting Commands
  3. Command 3 : Address Setting Commands
  4. Command 4 : Display Control Commands
  5. When IC power is applied for the first time, the contents of the Display RAM are not defined : thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

APPLICATION CIRCUIT



Note : The capacitor (0.1μF) connected between the GND and the VDD pins must be located as close as possible to the MC3401A chip.

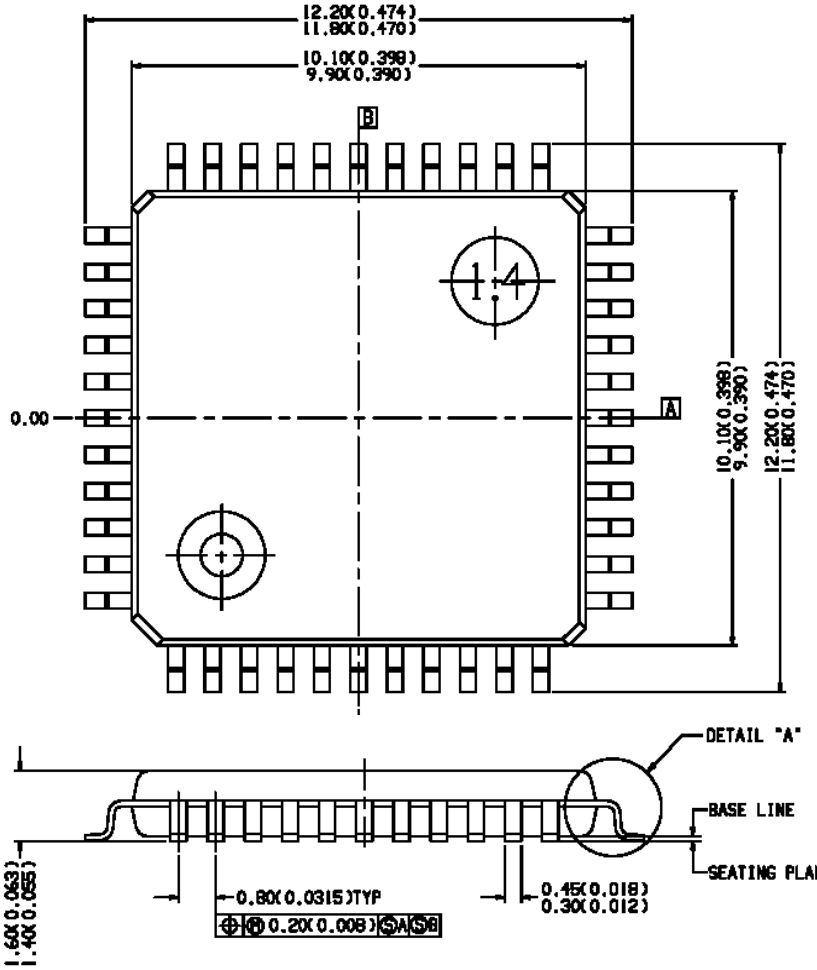
APPLICATION CIRCUIT



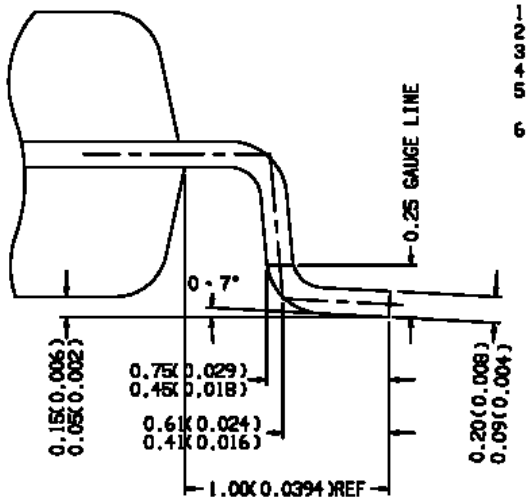
Note : The capacitor (0.1μF) connected between the GND and the VDD pins must be located as close as possible to the MC3411A chip.

PACKAGE INFORMATION

MC3401AL 44-PIN LQFP



NOTE
1) LEAD FRAME : C7025
2) LEAD FINISH : SOLDER PLATED.
3) BACK EJECTOR PIN MARKED "KOREA".
4) BOTH PACKAGE LENGTH AND WIDTH DO NOT INCLUDE FLASH.
5) FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.10(0.004) MM.
6) CONTROLLING DIMENSION : MM(INCHES)



DETAIL "A" (40/1)

PACKAGE INFORMATION

MC3411AU 48QFN