

ABOV SEMICONDUCTOR
24 SEGMENT X 16 GRID VFD DRIVER WITH KEYSKAN

MC3501A

Data Sheet (Ver. 1.00)



Version 1.00

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FAE Team

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REVISION HISTORY

VERSION 1.00 (2013. 06. 18) This Book

The first edition.

Internal pull-down resistors for SGn and GRn are enhanced in size, width and contact number.

(Typ. 50 k Ω \rightarrow 70 k Ω)

DESCRIPTION

MC3501A are Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52 plastic LQFP. 24 segment output lines, 16 grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to MC3501A via a three-line serial interface.

FEATURES

- CMOS Technology
- Low Power Consumption
- Wide operating voltage $V_{DD}=2.7V\sim 5.5V$
- Key Scanning (16 x 2 matrix)
- Display Modes : (24 segments, 8digits to 24 segments, 16 digits)
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors needed for driver outputs
- Available in 52-pin LQFP.

Device name	MC3501A
Package Type	52 LQFP
Power	VDD : 2EA, VSS : 2EA, VEE : 1EA
Port I/O	I : 6EA , O : 1EA
FIP Output	40 EA

APPLICATION

- Microcomputer Peripheral Devices
- Digital Audio/Video system : CD/MD/VCD/DVD players
- Car Audio
- VCR
- Electric scale meter
- P.O.S.
- Electronic equipment with instructional display

ORDERING INFORMATION

Device name	Segment	Grid	Key Scanning	Package Type
MC3501AL	24 Segments	16 Grid	16 x 2 matrix	52 LQFP

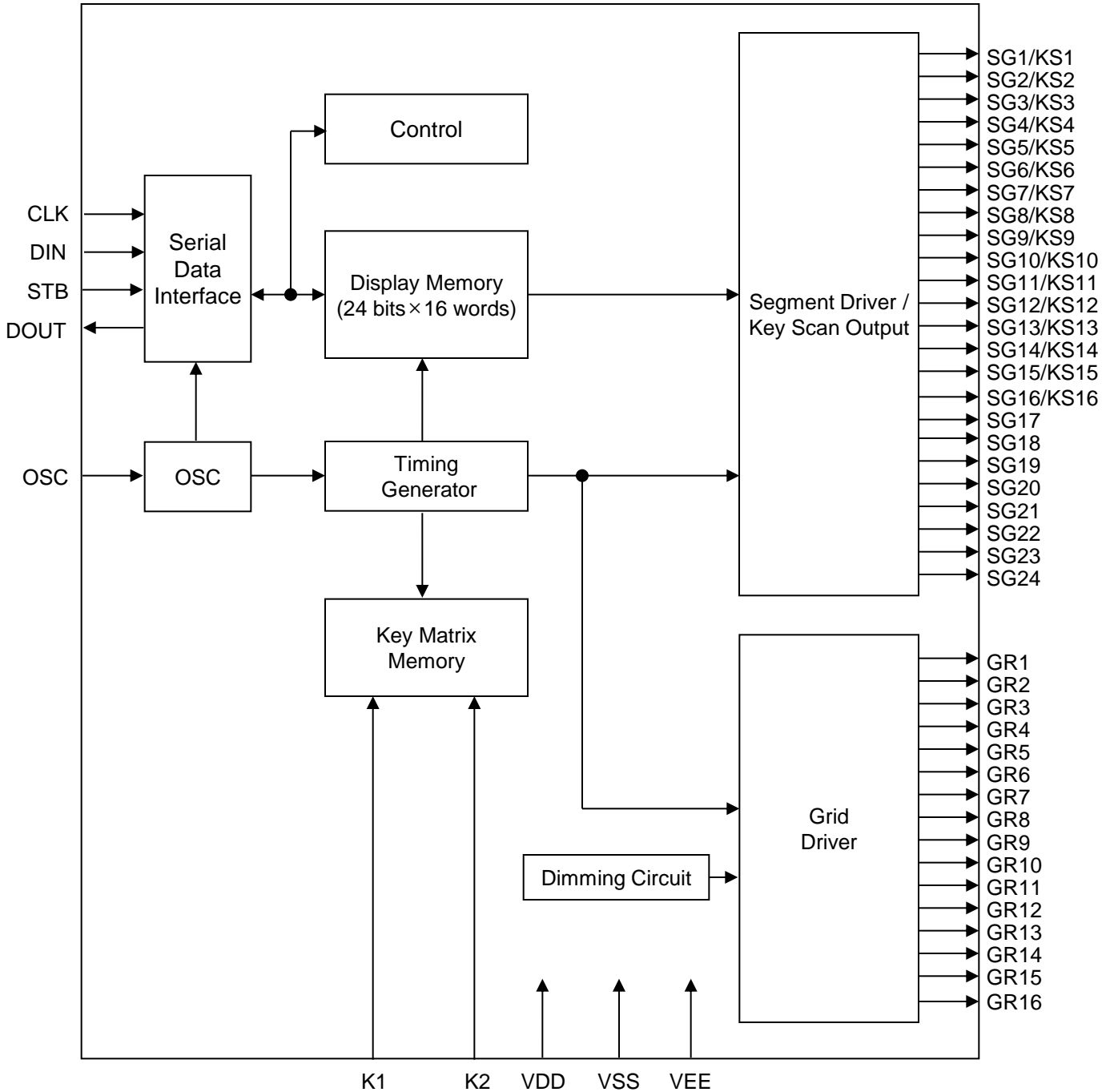
PIN DESCRIPTION

MC3501A

PIN NAME	I/O	DESCRIPTION	PIN No.
CLK (Schmitt Trigger)	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge of the shift clock	1
DIN (Schmitt Trigger)	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	2
STB (Schmitt Trigger)	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is "HIGH", CLK is ignored.	3
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock. (starting from the lower bit) Enable push-pull type output via setting b5,b4 of command 4.	4
K1 to K2	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	5,6
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation Frequency.	7
VSS	-	Logic Ground Pin	8,52
VDD	-	Logic Power Pin	9,51
SG1/KS1 to SG16/KS16	O	High-Voltage Segment Output Pins Also acts as the Key Source.	10 to 25
SG17 to SG24	O	High-Voltage Segment Output Pins	26 to 33
GR1 to GR16	O	High-Voltage Grid Output Pins	34 to 49
VEE	-	Pull-Down Level	50

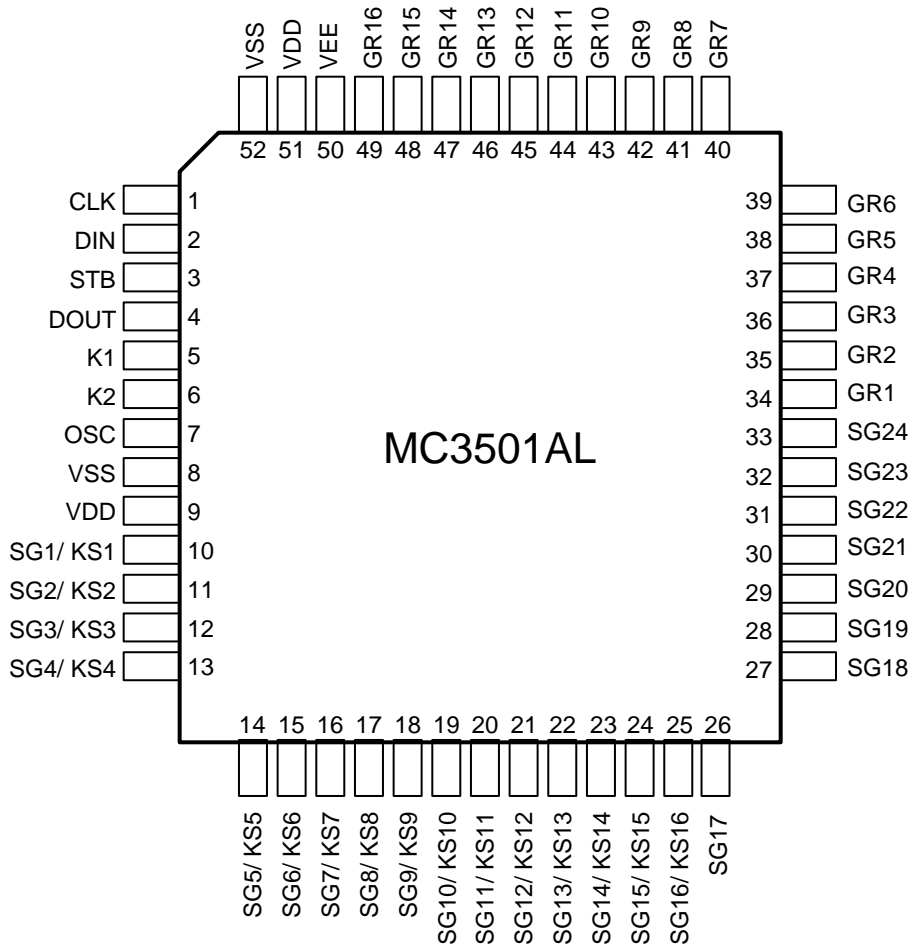
BLOCK DIAGRAM

MC3501A



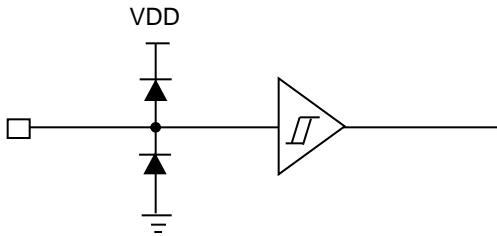
PIN CONFIGURATION

MC3501A

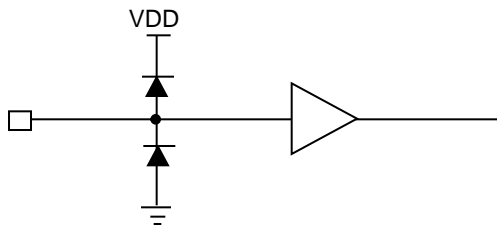


INPUT/OUTPUT PINS SCHEMATIC DIAGRAM

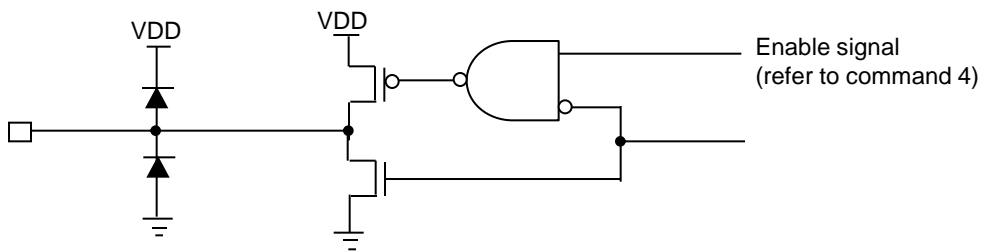
Input pins : CLK,STB, DIN



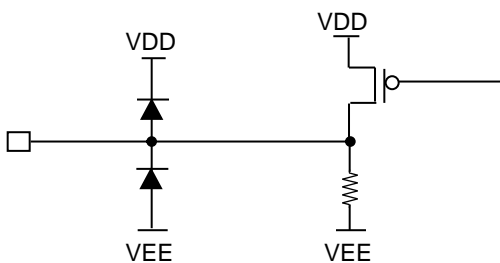
Input pins : K1,K2



Output pin : DOUT



Output pins : SGn, GRn



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25 °C, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
Driver Supply Voltage	VEE	VDD+0.3 to VDD-45	V
Logic Input Voltage	VI	-0.3 to VDD+0.3	V
VFD Driver Output Voltage	VO	VEE-0.3 to VDD+0.3	V
VFD Drive Output Current	IOVFD	-40 (Grid) -15 (Segment)	mA
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta= 25 °C, GND=0V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	2.7	5	5.5	V
High-Level Input Voltage (VDD=5V)	VIH	0.75VDD	-	VDD	V
Low-Level Input Voltage (VDD=5V)	VIL	0	-	0.2VDD	V
High-Level Input Voltage (VDD=3.3V)	VIH	0.8VDD	-	VDD	V
Low-Level Input Voltage (VDD=3.3V)	VIL	0	-	0.2VDD	V
Driver Supply Voltage	VEE	VDD-35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	IOLDOUT = 4mA DOUT, DIO	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD – 2V SG1/KS1 to SG16/KS16, SG17 to SG24	-3	-	-	mA
High-Level Output Current	IOHGR	VO = VDD – 2V GR1 to GR16	-15	-	-	mA
High-Level Input Voltage	VIH	-	0.75VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	0	-	0.2VDD	V
Input Current	II	VI = VDD or VSS	-	-	±1	µA
Dynamic Current Consumption	IDDdyn	Under no load Display Off	-	-	5	mA

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	IOLDOUT = 4mA DOUT, DIO	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD – 2V SG1/KS1 to SG16/KS16, SG17 to SG24	-1.5	-	-	mA
High-Level Output Current	IOHGR	VO = VDD – 2V GR1 to GR16	-6	-	-	mA
High-Level Input Voltage	VIH	-	0.8VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	0	-	0.2VDD	V
Input Current	II	VI = VDD or VSS	-	-	±1	µA
Dynamic Current Consumption	IDDdyn	Under no load Display Off	-	-	3	mA

SWITCHING CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Grid rise time	tGLH	CL = 300pF	-	-	0.5	us
Segment rise time	tSLH		-	-	2.0	us
Grid fall time	tGHL		-	-	150	us
Segment fall time	tSHL		-	-	150	us
Oscillation frequency	fOSC	R=82KΩ	250	350	450	KHz

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Grid rise time	tTZH2	CL = 300pF	-	-	1.2	us
Segment rise time	tTZH1		-	-	4.0	us
Grid fall time	tGHL		-	-	150	us
Segment fall time	tSHL		-	-	150	us
Oscillation frequency	fOSC	R=82KΩ	250	350	450	KHz

TIMING CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25°C)

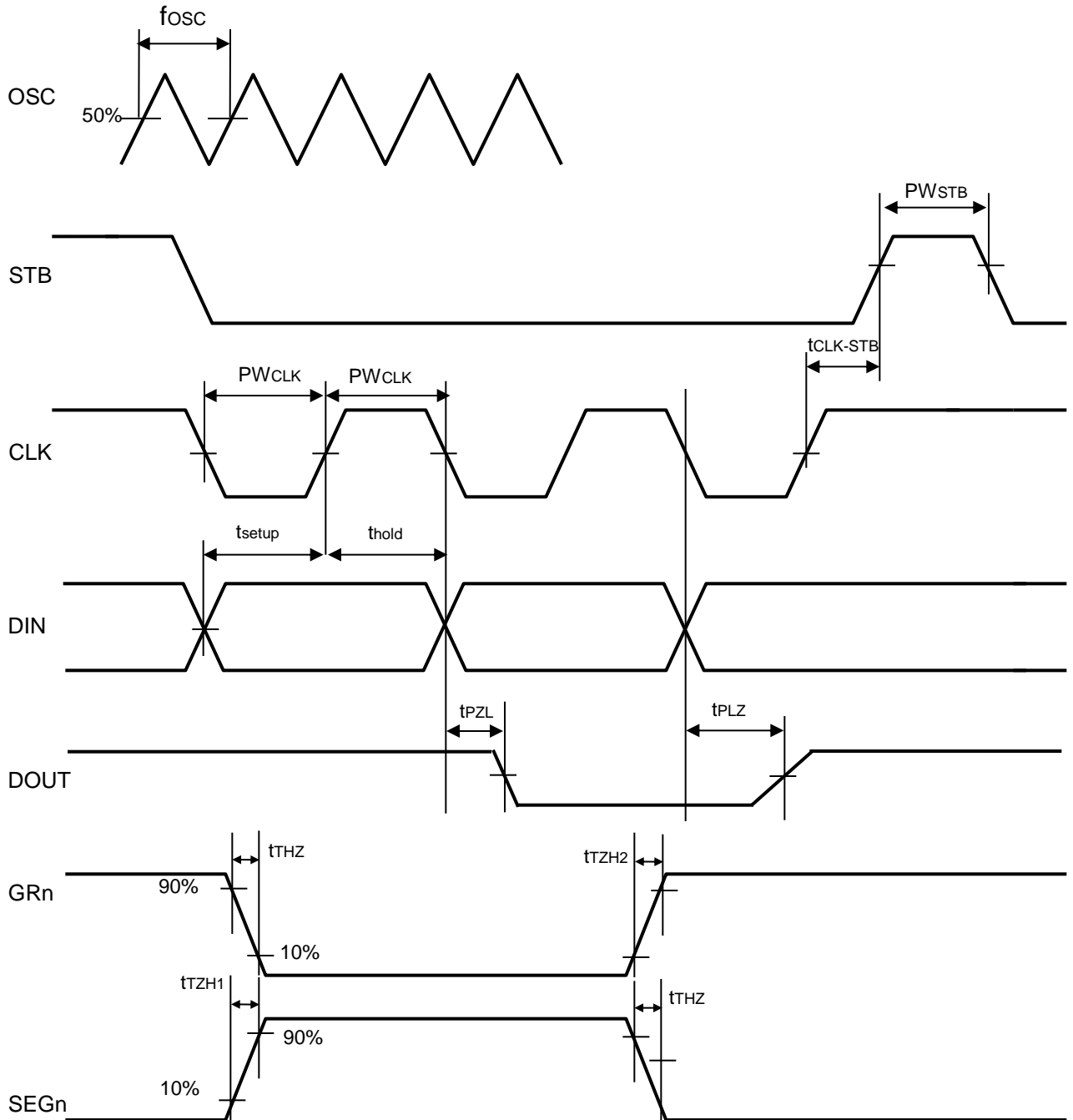
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK		400			ns
Strobe pulse width	PWSTB		1000			ns
Data setup time	tsetup		100			ns
Data hold time	thold		100			ns
Clock-strobe time	tCLK-STB	CLK ↑ → STB ↑	1000			ns
Propagation delay time	tPZL	RL=10KΩ, CL=15pF			100	ns
	tPLZ				400	ns

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK		400			ns
Strobe pulse width	PWSTB		1000			ns
Data setup time	tsetup		100			ns
Data hold time	thold		100			ns
Clock-strobe time	tCLK-STB	CLK ↑ → STB ↑	1000			ns
Propagation delay time	tPZL	RL=10KΩ, CL=15pF			100	ns
	tPLZ				600	ns

SWITCHING CHARACTERISTIC WAVEFORM

MC3501A Switching Characteristics Waveform is given below.



FUNCTIONAL DESCRIPTION

COMMANDS

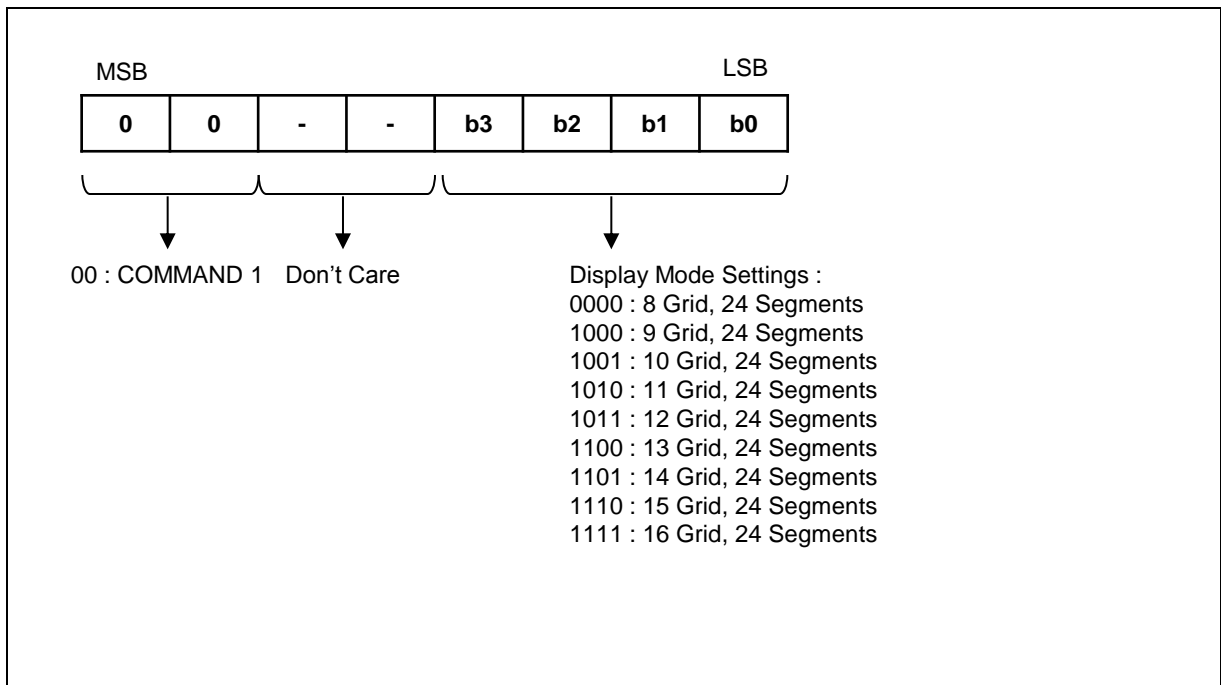
Commands determine the display mode and status of MC3501A. A command is the first byte (b0 to b7) inputted to MC3501A via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. If for some reason the STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1 : DISPLAY MODE SETTING COMMAND

MC3501A provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to MC3501A via the DIN Pin when STB is "LOW". However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/8 to 1/16 duty, 24 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command "ON" must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned "ON", the 16-digit, 24-segment modes is selected.



Display Mode and RAM Address

Data transmitted from an external device to MC3501A via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of MC3501A are given below in 8bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	SG13	SG16	SG17	SG20	SG21	SG24	
00H _L	00H _U		01H _L		01H _U		02H _L		02H _U			DIG1
03H _L	03H _U		04H _L		04H _U		05H _L		05H _U			DIG2
06H _L	06H _U		07H _L		07H _U		08H _L		08H _U			DIG3
09H _L	09H _U		0AH _L		0AH _U		0BH _L		0BH _U			DIG4
0CH _L	0CH _U		0DH _L		0DH _U		0EH _L		0EH _U			DIG5
0FH _L	0FH _U		10H _L		10H _U		11H _L		11H _U			DIG6
12H _L	12H _U		13H _L		13H _U		14H _L		14H _U			DIG7
15H _L	15H _U		16H _L		16H _U		17H _L		17H _U			DIG8
18H _L	18H _U		19H _L		19H _U		1AH _L		1AH _U			DIG9
1BH _L	1BH _U		1CH _L		1CH _U		1DH _L		1DH _U			DIG10
1EH _L	1EH _U		1FH _L		1FH _U		20H _L		20H _U			DIG11
21H _L	21H _U		22H _L		22H _U		23H _L		23H _U			DIG12
24H _L	24H _U		25H _L		25H _U		26H _L		26H _U			DIG13
27H _L	27H _U		28H _L		28H _U		29H _L		29H _U			DIG14
2AH _L	2AH _U		2BH _L		2BH _U		2CH _L		2CH _U			DIG15
2DH _L	2DH _U		2EH _L		2EH _U		2FH _L		2FH _U			DIG16

b0 b3 b4 b7

xxH _L	xxH _U
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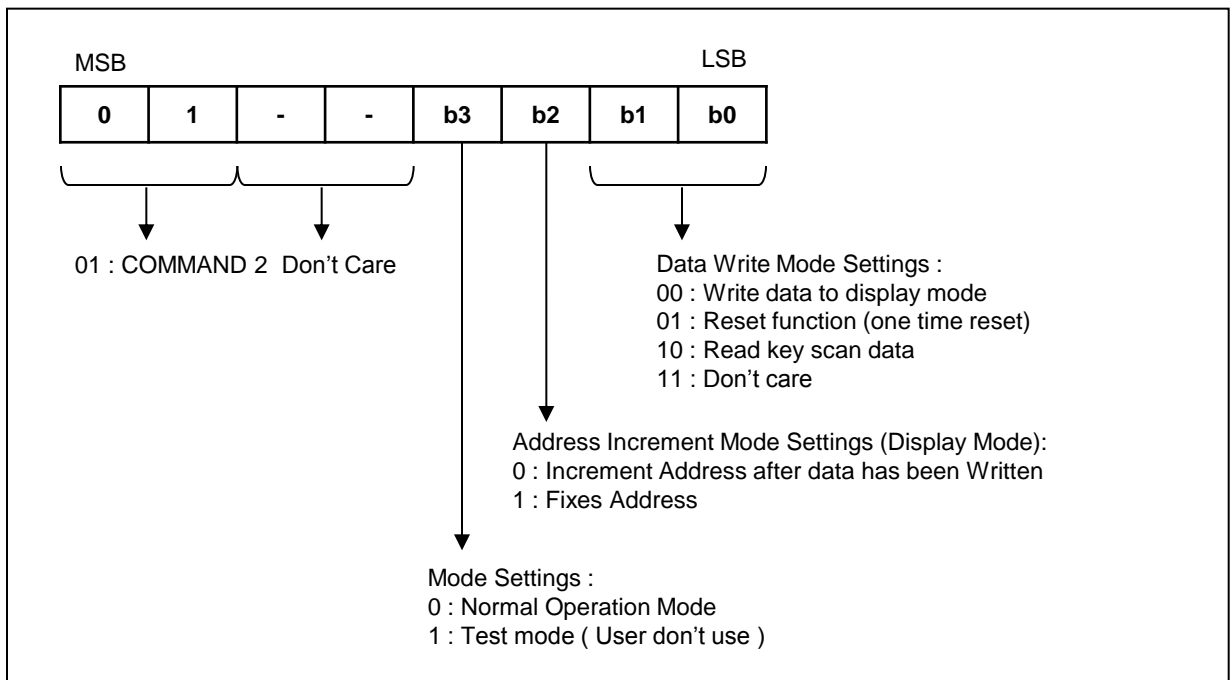
Lower 4bits

Higher 4bits

COMMAND 2 : DATA SETTING COMMAND

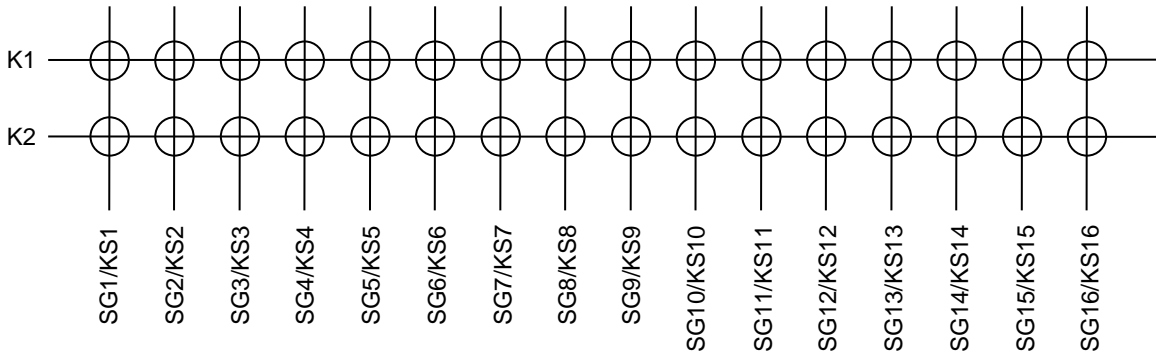
The Data Setting Commands executes the Data Write or Data Read Modes for MC3501A. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of "0".

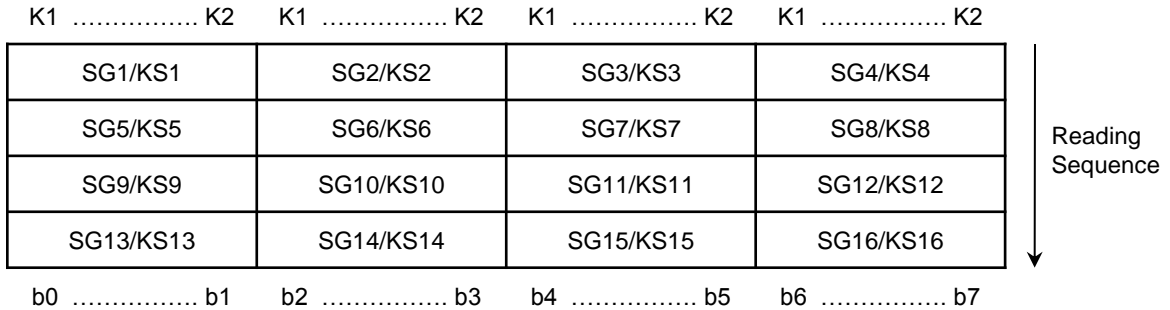


MC3501A Key Matrix & Key Input Data Storage RAM

MC3501A key matrix consists of 16×2 array as shown belows.



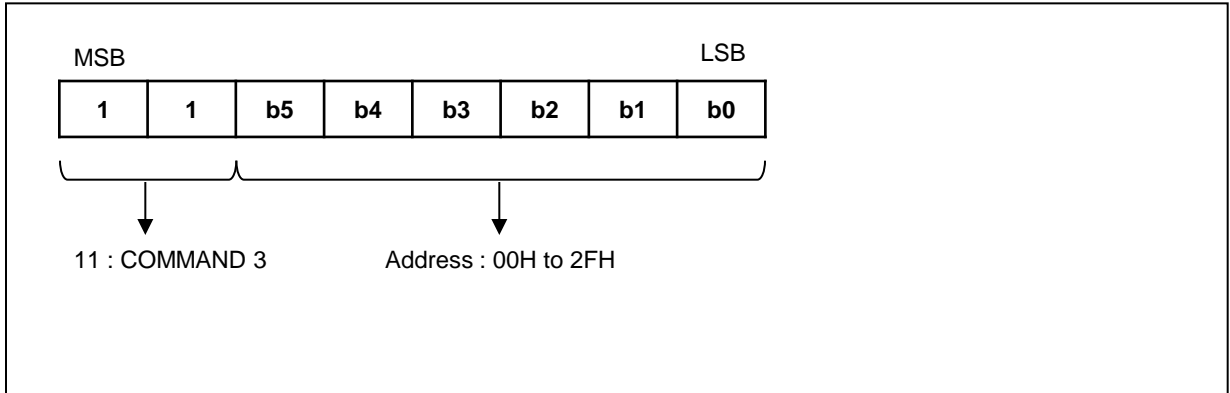
Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG1, b0) has been read, the least significant bit of the next data (SG16, b7) is read.



COMMAND 3 : ADDRESS SETTING COMMAND

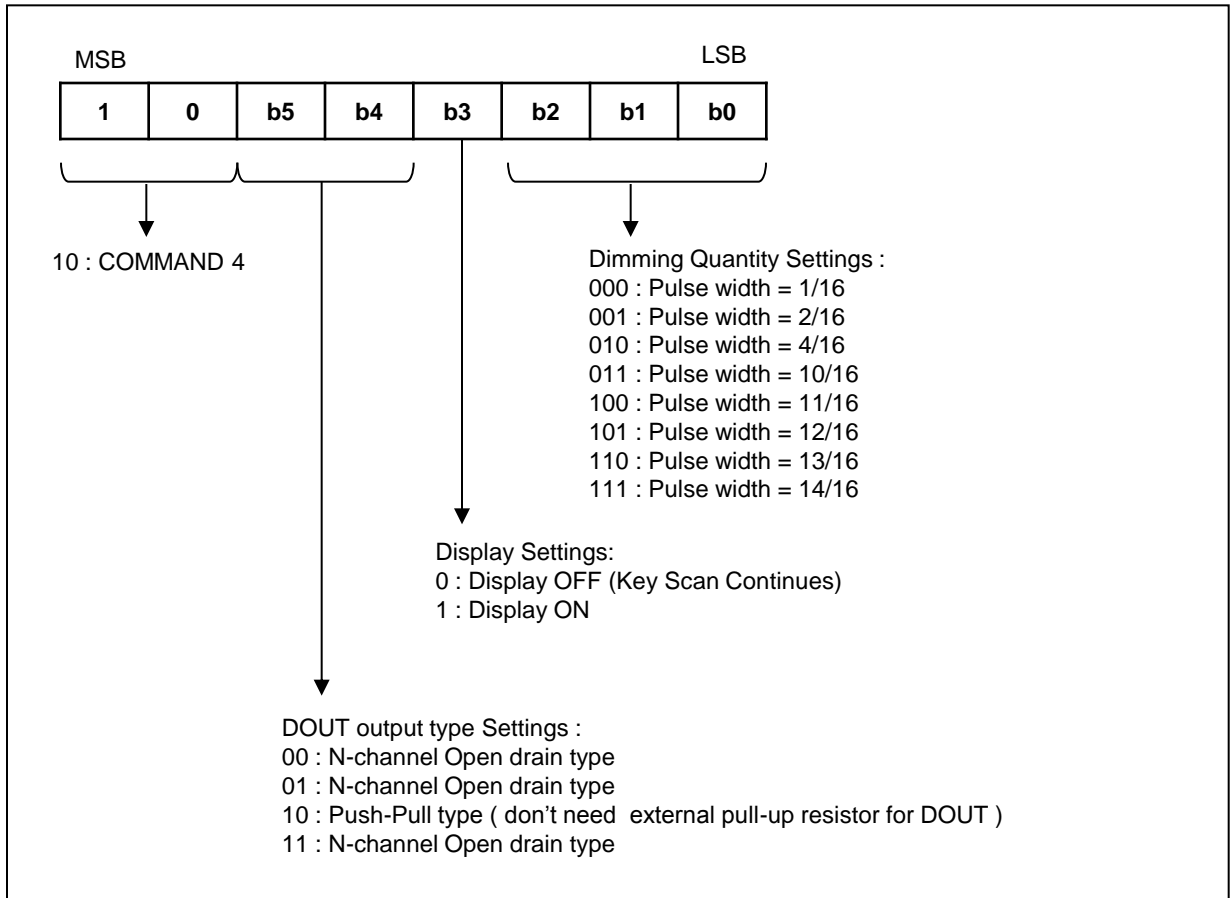
The display memory is addressed by Address Setting Command. The valid address range is "00H" to 2FH". If the address is set to 30H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at "00H".

Please refer to the diagram below.



COMMAND 4 : DISPLAY CONTROL COMMANDS

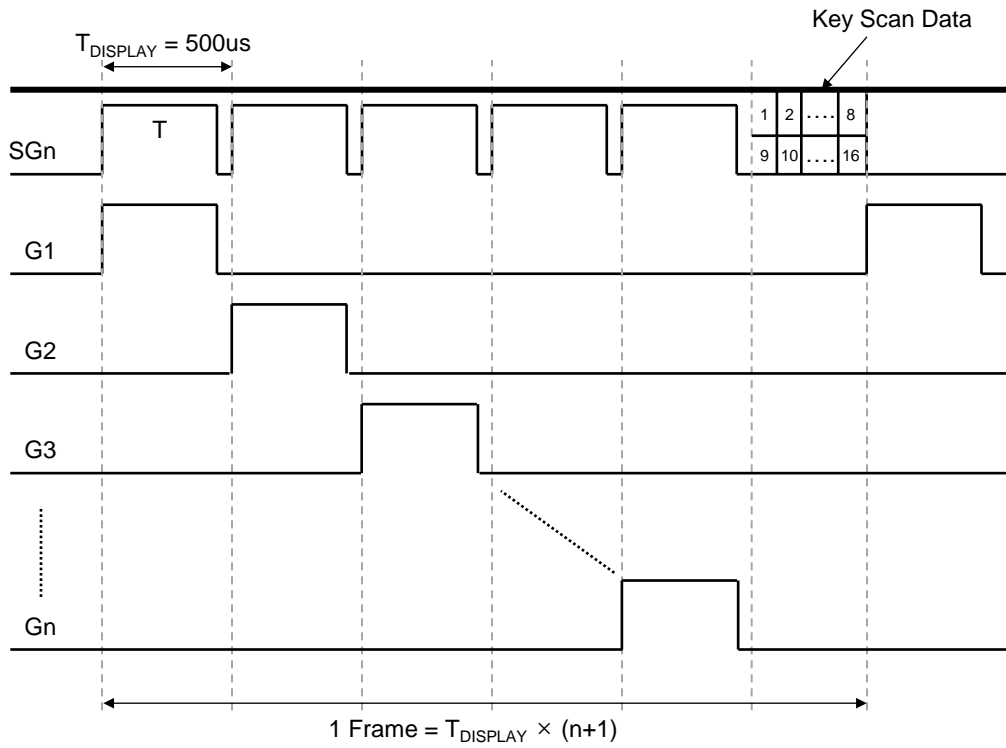
The Display Control Commands are used to turn ON or OFF a display. It is also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the display is turned OFF (the key scanning is stopped) and DOUT is selected N-channel Open drain type.



SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 16 x 2 matrix is stored in the RAM.

Operating Frequency (f_{osc}) = $224/T$

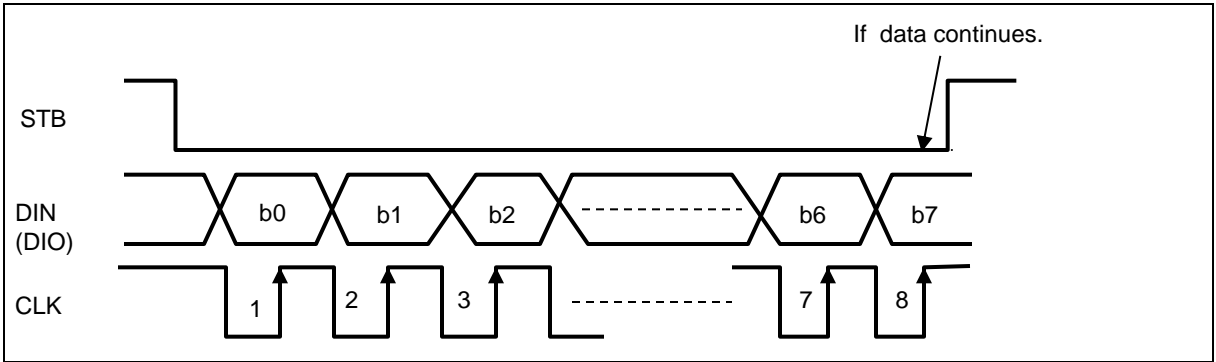


Note : T is the width of segment only

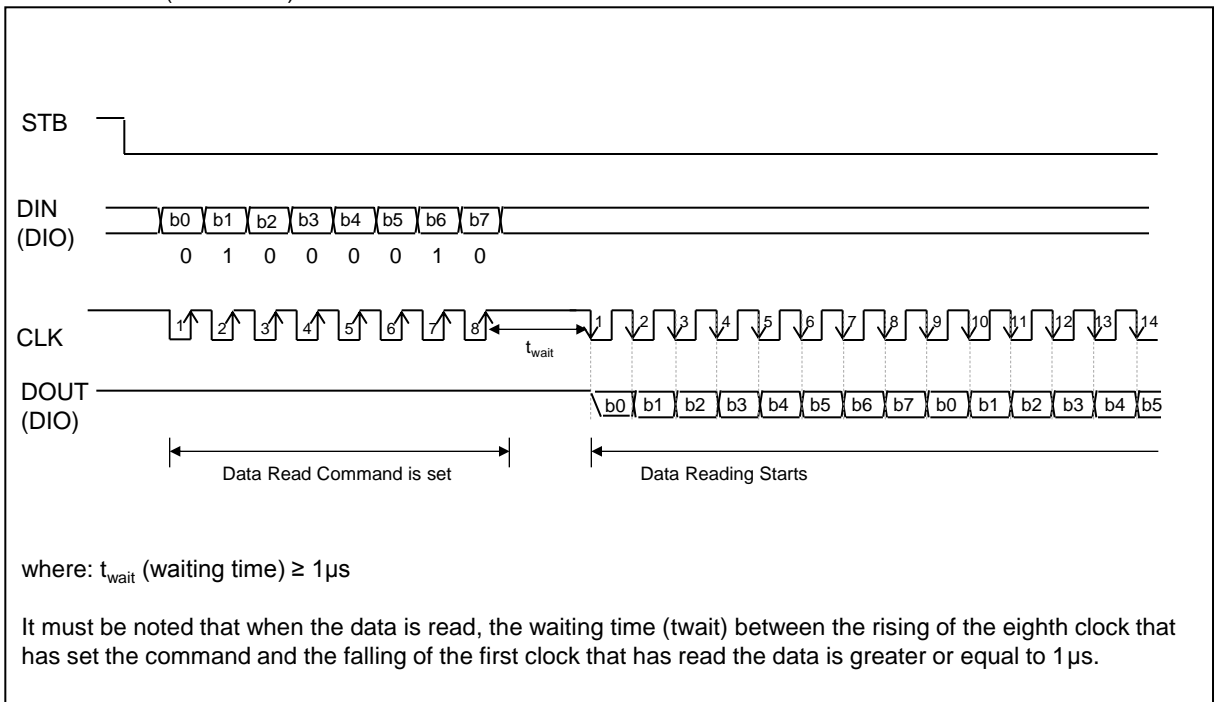
SERIAL COMMUNICATION FORMAT

The following diagram shows the MC3501A serial communication format. The DOUT Pin is selected output type (N-channel open-drain type or Push-pull type) via command 4. If DOUT is selected open-drain type output, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DOUT.

RECEPTION (Data/Command Write)

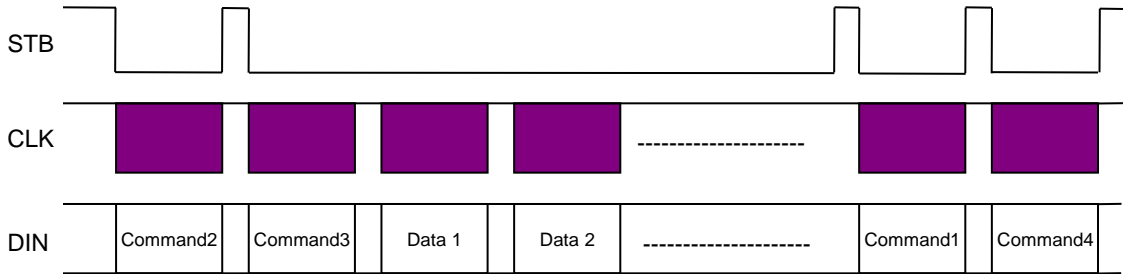


Transmission (Data Read)



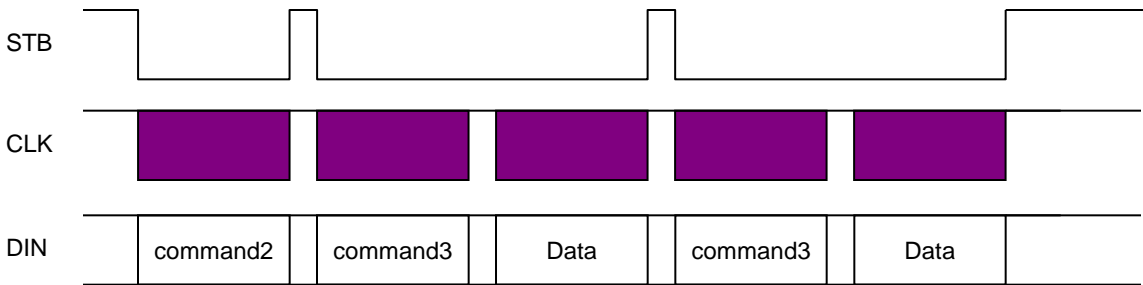
SERIAL COMMUNICATION EXAMPLES

Serial communication timing diagram for initialization setting.



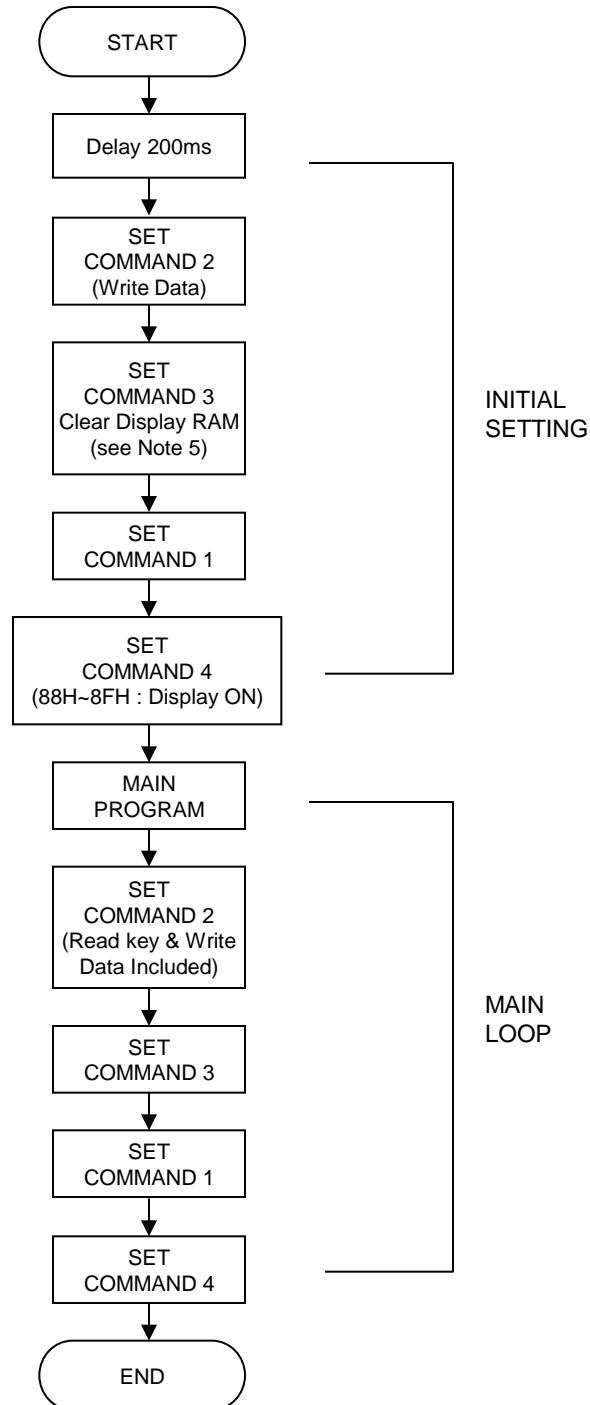
Where : Command 1 : Display Mode Setting
 Command 2 : Data Setting Command
 Command 3 : Address Setting Command
 Data 1 to n : Transfer Display Data (36 Bytes max.)
 Command 4 : Display Control Command

Memory updating timing diagram.



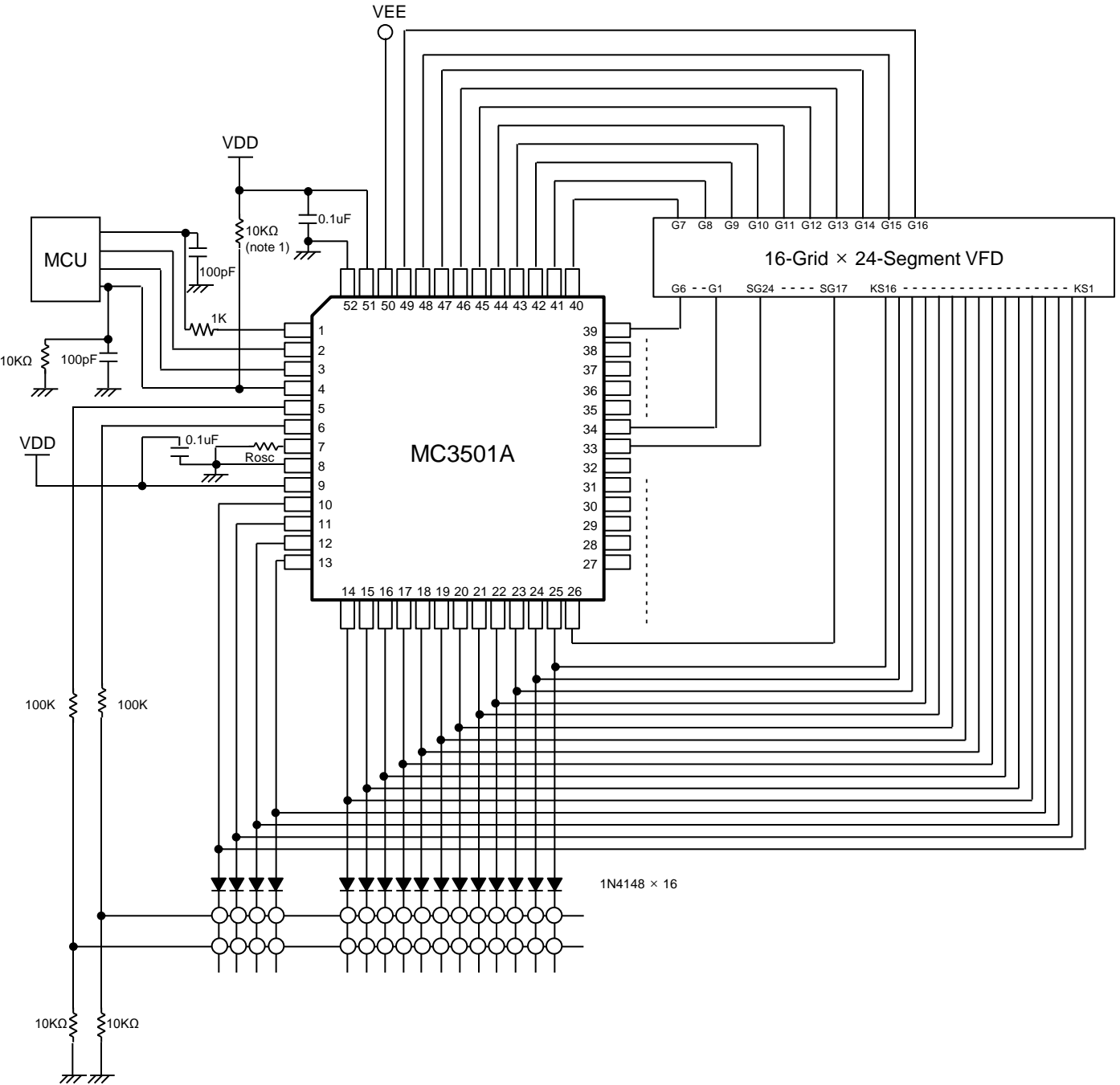
Where : Command 2 -- Data Setting Command
 Command 3 -- Address Setting Command
 Data -- Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOW CHART



- **Note** : 1. Command 1 : Display Mode Setting
- 2. Command 2 : Data Setting Commands
- 3. Command 3 : Address Setting Commands
- 4. Command 4 : Display Control Commands
- 5. When IC power is applied for the first time, the contents of the Display RAM are not defined : thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

APPLICATION CIRCUIT



(note 1) don't need external pull-up resistor for DOUT (refer to COMMAND 4 on page 20)
 - in this case, VDD have to be same level or higher than power of MCU

PACKAGE INFORMATION

52-PIN LQFP

