# CMOS single-chip 8-bit MCU with 12-bit ADC

## Main features

**8-bit Microcontroller with high performance CM8051-S CPU**

**Basic MCU Function**
- 2 Kbytes Flash Code Memory
- Code Area Protection
- 256 bytes SRAM Data Memory

**Built-in Analog Function**
- Power-On Reset and Brown-out Detect Reset
- Internal 32 MHz RC Oscillator (±1.5%@25℃)

**Peripheral features**
- 12-bit Analog to Digital Converter

**I/O and packages**
- Up to 14 programmable I/O lines with 16pin package
- Package types 16SOP, 16QFN, 10SSOP, 8SOP

**Operating conditions**
- -40°C to 85°C temperature range
- -40°C to 105°C temperature range

**Application**
- Battery charge & discharge control
- Small home appliance

# MC94F1202A

## Data Sheet

**V 1.18**

**Nov 25, 2022**

# Revision history

| Version | Date | Revision list |
|---|---|---|
| 1.0 | 2016.03.03 | Initial preliminary version |
| 1.1 | 2016.04.29 | Change Version Start V1.0<br>Change BOD to LVI (Name Change)<br>Updated Table format and contents in 7 Electrical Characteristics.<br>Updated MCU Stabillzation time.<br>Add 7.10 Operating Voltage Range and 7.11 Typical Characteristics. |
| 1.2 | 2016.05.02 | Fixed the errors of the figure 2.1. ( [P7:0] -> [P6:0] , 10 Page)<br>Updated Table 7.1 Absolute maximum ratings. (16 Page)<br>Updated Table 7.3 Analog ADC Voltage (16 Page)<br>Fixed Table 7.8 DC Characteristics (IDD2 Max 5mA -> 4mA, 17 Page)<br>11.5.4 ADC Zero offset delete.<br>Add 10-SSOP Package. (1.1 Description, 3 Pin Assignment, 4 Package Dimension)<br>Table of Contents fixed. (99 Page) |
| 1.3 | 2016.05.19 | Fixed Value. (RSFR Initial / Default Value, 75-76 Page)<br>Add NOTE for OCD reset state. (RSFR, 76 Page)<br>Updated Table 15.2.<br>Fixed Flash Control Register ADDRESS. |
| 1.4 | 2016.06.15 | Fixed Value. (POR level 1.4V -> 1.1V, Page 73-74).<br>Delete unused Register. (DPL1,DPH1, Page 26) |
| 1.5 | 2016.06.24 | Fixed the errors of table 15.4 Security policy using lock-bits.<br>Updated description of FESR register. |
| 1.6 | 2017.03.08 | Fixed the errors of address of 15.4.1.2 Enable program mode. |
| 1.7 | 2017.10.10 | Fixed the errors of the 1.2 Features.<br>Fixed the errors of the Figure3.1.<br>Fixed the errors of the IE(Interrupt Enable Register). (T1 <-> T0, 43 Page)<br>Add maximum allowable current of 7.1 Absolute Maximum Ratings |
| 1.8 | 2017.10.24 | Added description of PUSH SP, POP SP, DA incompatible instruction. (17.APPENDIX A) |
| 1.9 | 2017.11.06 | Added description of PWM Duty related error.<br>Updated Table 7.3 Analog ADC Voltage |
| 1.10 | 2017.11.10 | Removed the maximum allowable current ($I_{IK}$) in chapter 7.1 Absolute Maximum Ratings<br>Added the maximum allowable voltage ($V_{IK}$) in chapter 7.1 Absolute Maximum Ratings<br>Added the Figure describing $V_{IK}$ in chapter 7.1 Absolute Maximum Ratings |
| 1.11 | 2017.12.21 | Revised this book.<br>Add Device Nomenclature.<br>Add OCD Interface circuit |
| 1.12 | 2017.12.28 | Added the recommended operating conditions for $f_X$= 1, 4, 8MHz and +5~+35°C in chapter 7.2 Recommended Operating conditions.<br>Added minimum voltage of LVR to 1.65V. |
| 1.13 | 2018.01.25 | Added table 7.4 for ADC characteristic under 2.7V in chapter 7.3 A/D Converter Characteristics.<br>Updated Table 7.7 for Internal RC Oscillator characteristics in chapter 7.6.<br>Added 16 QFN package type. |
| 1.14 | 2018.09.18 | Added Chapter 1.3.3 OCD Port Operation.<br>Updated Figure 1.4 OCD Interface Circuit<br>Updated Chapter 7.4 Power-On Reset VDD Voltage Rising Time.<br>Added Chapter 7.12 Recommended Application Circuit. |
| 1.15 | 2019. 08. 09 | Updated Figure 1.4 OCD Interface Circuit.<br>Updated Figure 2.1 Block diagram of MC94F1202A.<br>Added Voltage Down Converter(BMR) Specification to Chapter 7.4<br>Assigned the internal reference voltage(BMR) to AN14 in Chapter 11.5.2<br>Added how to use the internal reference voltage(BMR) in Chapter 11.5.6 |
| 1.16 | 2019.10.23 | Extended maximum operating temperature up to 105°C as well as 85°C<br>Updated Ordering Information of MC94F1202A on page 4<br>Updated Device Nomenclature on page 5<br>Updated temperature condition in 7 Electrical Characteristics<br>Changed the name of Voltage Down Converter(BMR) to BMR Reference Voltage Characteristics in Chapter 7.4 |
| 1.17 | 2020.07.03 | Corrected the divided clock of Timer2 at Figure 11.10 on page 70. |
| 1.18 | 2022.11.25 | Revised the font of this document |

**Version 1.18**

**Published by FAE team**



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# 1 Overview

## 1.1. Description

The MC94F1202A is an advanced CMOS 8-bit microcontroller with 2 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 2 Kbytes of FLASH, 256 bytes of SRAM, 16-bit timer/counter/PWM, Watchdog timer with WDTOSC, 12-bit ADC, On-chip POR, LVI and LVR, Internal RC-Oscillator, Internal WDT-Oscillator and clock circuitry. The MC94F1202A also supports Power saving modes to reduce Power Consumption.

| Device Name | FLASH | IRAM | XRAM | ADC | I/O PORT | Package | Temperature Range |
|---|---|---|---|---|---|---|---|
| MC94F1202AMB | 2 Kbytes | 256 bytes | - | 14 inputs | 14 | 16-SOP | -40°C ~ +85°C |
| MC94F1202AUB | 2 Kbytes | 256 bytes | - | 14 inputs | 14 | 16-QFN | |
| MC94F1102ASB | 2 Kbytes | 256 bytes | - | 8 inputs | 8 | 10-SSOP | |
| MC94F1102AMB | 2 Kbytes | 256 bytes | - | 6 inputs | 6 | 8-SOP | |
| MC94F1202AMB2 | 2 Kbytes | 256 bytes | - | 14 inputs | 14 | 16-SOP | -40°C ~ +105°C |
| MC94F1202AUB2 | 2 Kbytes | 256 bytes | - | 14 inputs | 14 | 16-QFN | |
| MC94F1102ASB2 | 2 Kbytes | 256 bytes | - | 8 inputs | 8 | 10-SSOP | |
| MC94F1102AMB2 | 2 Kbytes | 256 bytes | - | 6 inputs | 6 | 8-SOP | |

**Table 1.1** Ordering Information of MC94F1202A

# Device Nomenclature

**MC94F1x02A M B 2 N (T)**

MC94F1x02A Family Name
- x=1 8/10 pin
- x=2 16 pin

Package Type
- M SOP
- S SSOP
- U QFN

RoHS
- B Halogen Free

Temperature
- none -40°C ~ 85°C
- 2 -40°C ~ 105°C

Bonding Wire
- none Au wire
- N Pd-Cu wire

Packing
- (T) Tape & Reel

## 1.2 Features

- **CPU**
  - CM8051-S (8051 Compatible, 1 clock per cycle)
- **2 Kbytes On-Chip FLASH**
  - Endurance : 10,000 times at room temperature
  - Retention : 10 years
  - Self-Writing (Code protect option)
- **256 bytes IRAM**
- **Input Output Ports**
  - GPIO 14
- **Timer/Counter**
  - 16-bit × 2-ch (Timer0, Timer1)
  - 8-bit × 1-ch (Timer2)
- **PWM (16-bit 2-ch, Using Timer0,1)**
- **Watch Dog Timer**
- **12-bit A/D Converter**
  - 14-Input channels
  - 1-channel for internal ref.
- **Interrupt Sources**
  - External Interrupts (3, with PCI)
  - Timer (3)
  - ADC (1)
  - WDT (1)
  - LVI (1)
- **On-Chip RC-Oscillator**
  - 32MHz Osillator (±1.5%@25°C)
  - 32MHz Osillator (±2.5%@-20°C~+60°C)
  - 32MHz Osillator (±3.0%@-40°C~+85°C)
  - 32MHz Osillator (±5.0%@-40°C~+105°C)
- **On-Chip WDT-Oscillator**
  - 8kHz (±50%) Oscillator
- **Power On Reset**
  - 1.1 V
- **Low Voltage Reset**
  - 1-Level (1.8 V)
- **Low Voltage Indicator**
  - 3-Level (2.1V, 2.5V, 3.5 V)
- **Minimum Instruction Execution Time**
  - 125ns (@8MHz, NOP Instruction)
- **Power Down Mode**
  - IDLE, STOP1, STOP2 mode
- **Operating Frequency**
  - 1 / 4 / 8 / 16MHz
- **Operating Voltage**
  - 2.2V ~ 5.5V
- **Operating Temperature**
  - -40°C ~ +85°C
  - -40°C ~ +105°C
- **Package Type**
  - 16-SOP, 16-QFN, 10-SSOP, 8-SOP
  - Pb free package

## 1.3 Development tools

### 1.3.1 Compiler

ABOV semiconductor does not provide any compiler for the MC94F1202A. But the CPU core of MC94F1202A is CM8051-S core, you can use all kinds of third party's standard 8051 compiler like Keil C Compiler, Open Source SDCC (Small Device C Compiler). These compilers' output debug information can be integrated with our OCD2 emulator and debugger. Refer to OCD1&OCD2 manual for more details.

### 1.3.2 OCD2 emulator and debugger

The OCD2 emulator supports ABOV Semiconductor’s 8051 series MCU emulation.

The OCD2 interface uses two wires interfacing between PC and MCU which is attached to user’s system. The OCD2 can read or change the value of MCU internal memory and I/O peripherals. And also the OCD2 controls MCU internal debugging logic, it means OCD2 controls emulation, step run, monitoring etc.

The OCD2 Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit), 7, 8, 8.1 operating system.

If you want to see more details, please refer OCD2 debugger manual. You can download debugger S/W and manual from our web-site.

### 1.3.3 OCD Port Operation

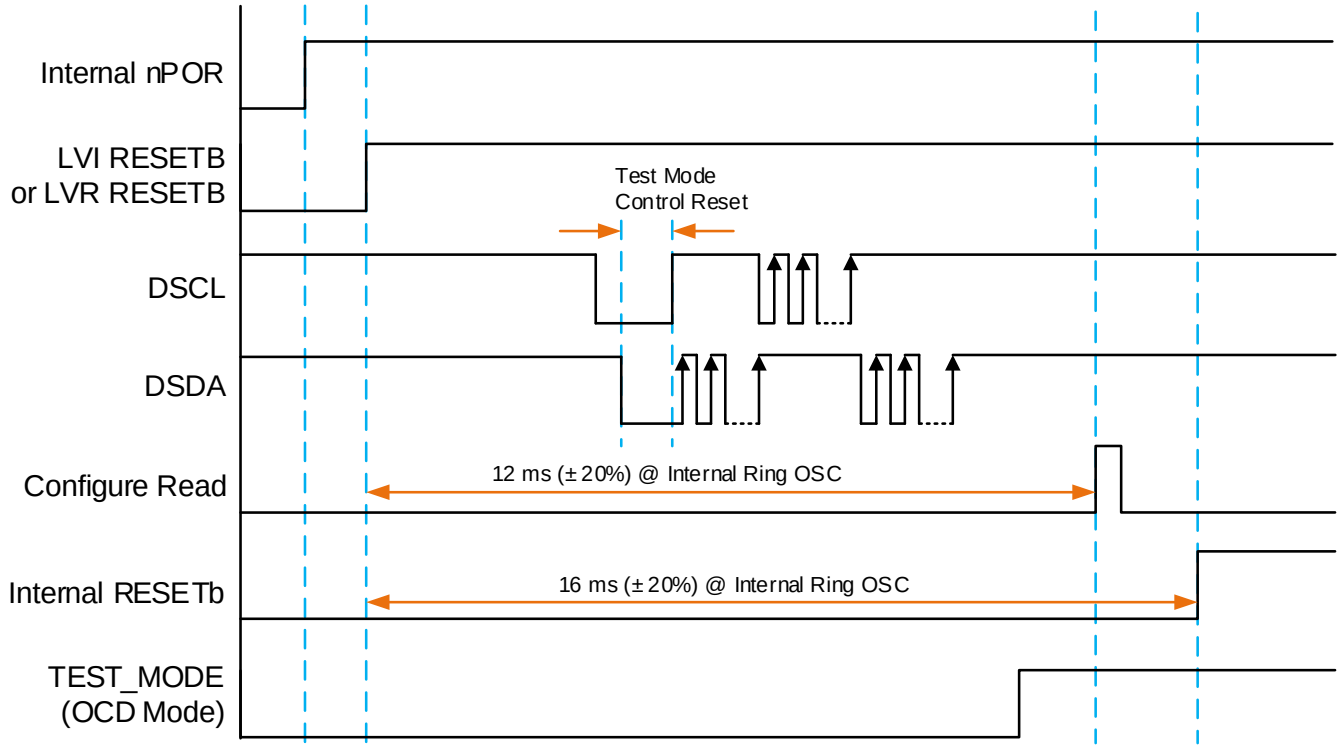



**Figure 1.1** OCD Mode Sequence

The OCD port is used for flash program writing and device debugging. The device has a section that determines whether to use it in that mode of POR. This is done when the internal reset is cleared and waiting to clear Configure Read and Internal Reset. If the internal reset is cleared and DSCL and DSDA wait for a period of time from internal pull-up 'high' to 'low', the internal controller for entering test mode is initialized. Then, when DSCA and DSCA appointed communication, the test mode is entered.

As described above, OCD port is a port for special purpose. Even if it is used as Normal GPIO in User Program, it is necessary to limit the state to prevent malfunction during POR. Therefore, it is recommended to connect Pull-up Resistor to the outside of OCD Port and to fix OCD Port input to VDD / GND at POR. If it is difficult to apply pull-up on the circuit, install at least 0.1uf bypass capacitor to prevent Floating state at POR. However, if you install a bypass cap, you can not use on board writing and OCD Debugger.

There are OCD2 mode connection.

- P01 (MC94F1202A DSCL pin)
- P00 (MC94F1202A DSDA pin)

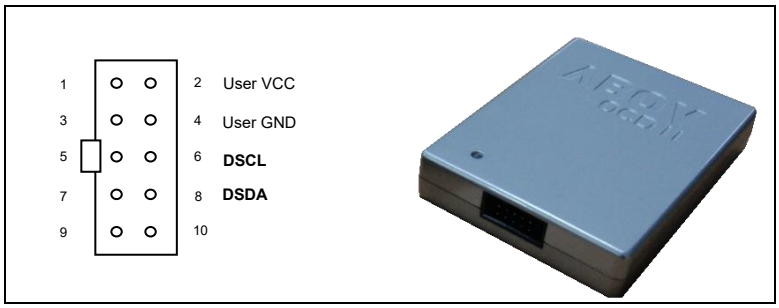



**Figure 1.2** On Chip Debugger 2 and Pin description (OCD2 mode)

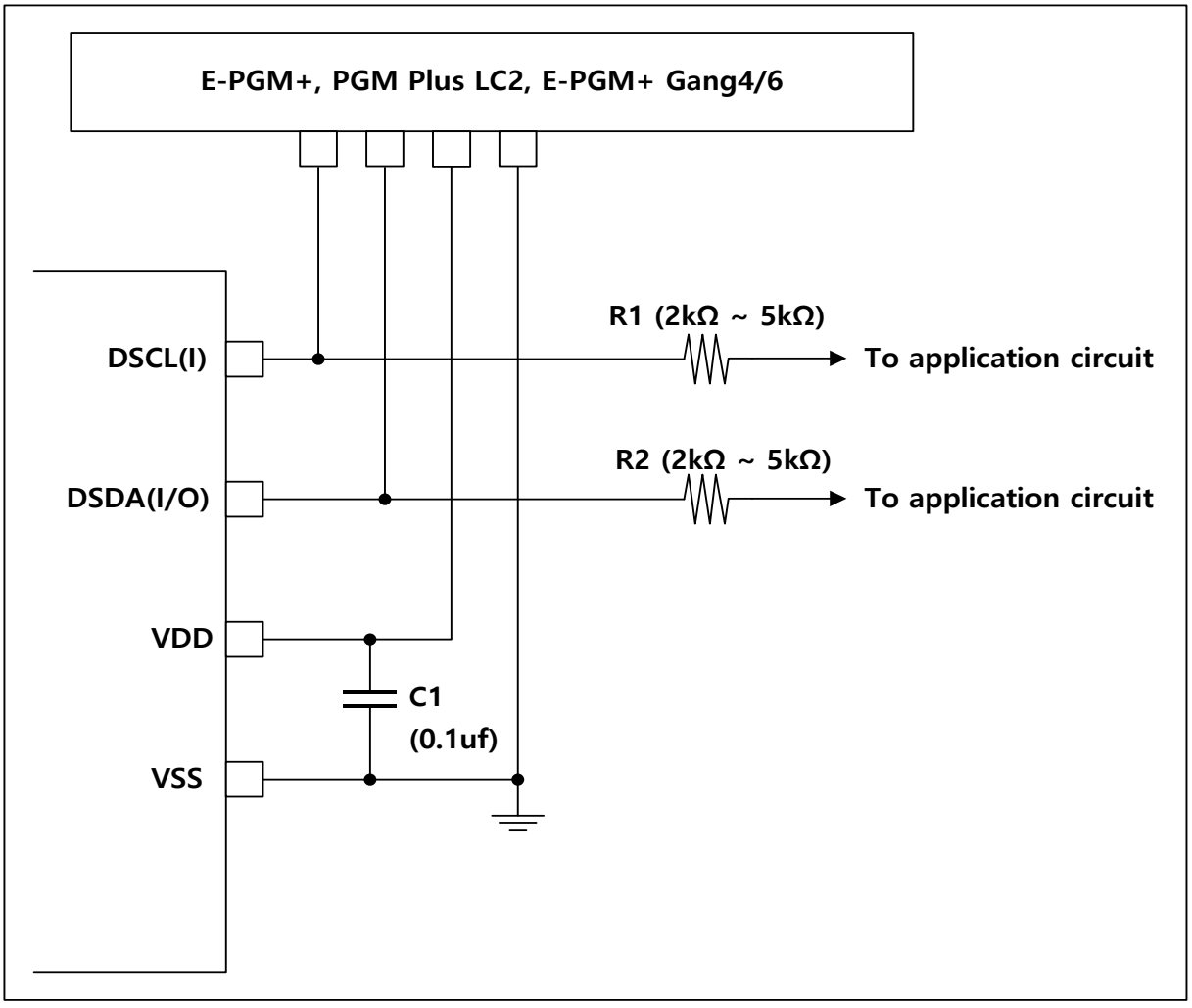



**Figure 1.3** OCD Interface Circuit

**NOTE)**

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1, R2 and C1 is recommended value. It varies with circuit of system.

**OCD2 (On Chip Debug) Emulator**

- MCU emulation control via 2pin OCD interface.
- 2pin interface : OCD2 clock & data.
- Higher interface speed than OCD dongle.
- Compact size.
- Cost effective emulator.
- Emulation & debugging on the target system directly.
- Real time emulation.
- PC interface : USB.

**Debugger**

- Operates with OCD2 emulator H/W.
- Integrated Development Environment (IDE).
  Support docking windows and menus.
- Support Free run, Step run, auto step run.
- Support Symbolic debugging.
- Support Source level debugging.

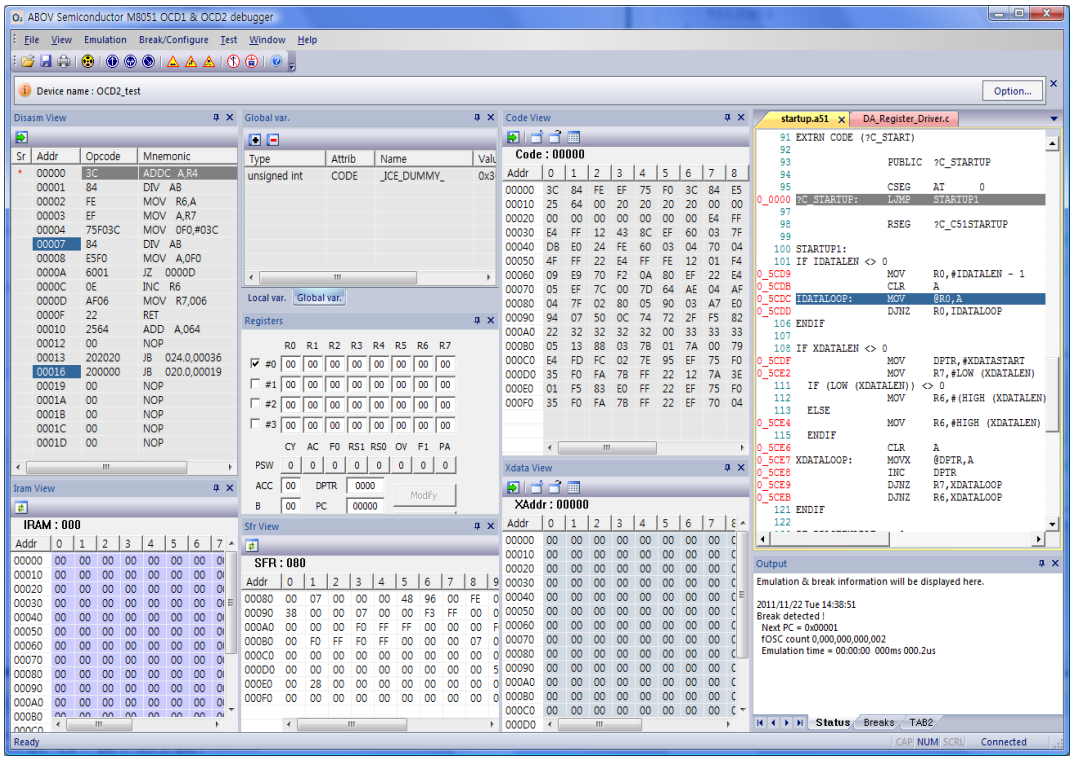



**Figure 1.4** OCD Debugger

### 1.3.4 Programmer

**E-PGM +**

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32-bit MCU @ 72MHz
- Buffer memory : 1MB

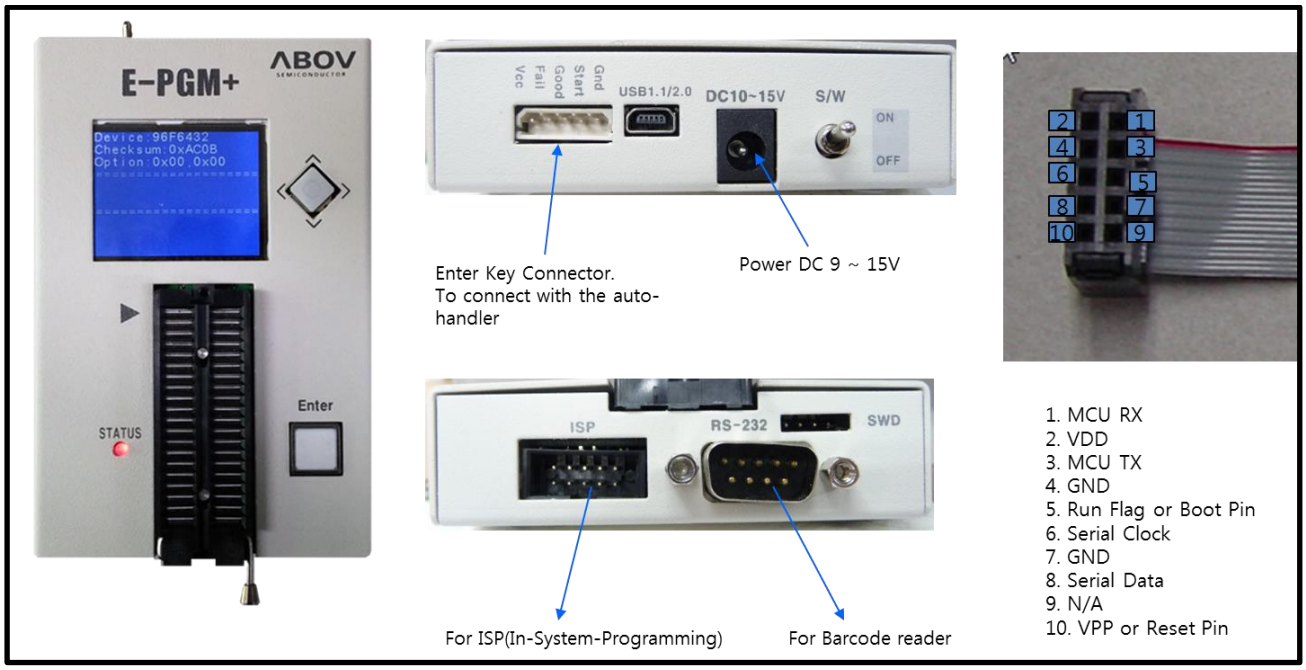



**Figure 1.5** E-PGM+ component and connector

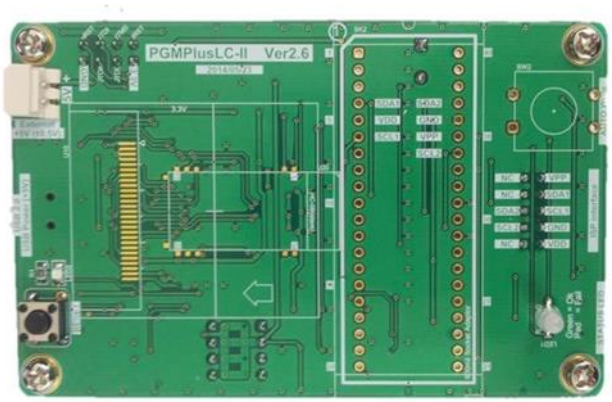
**PGMPlusLC** 2

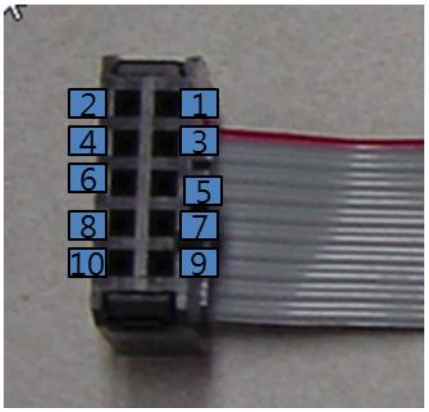
**Description**

PGMPlusLC2 is for ISP(In System Programming). It is used to write into the MCU Which is already mounted on target board using 10pin cable.

**Features**

- PGMplusLC2 is low cost writing Tool.
- USB interface is supported.
- Not need USB driver installation.
- Connect the external power adaptor(5V@2A).
- Supported high voltage Max 18V.
- PGMplusLC2 is based on PC environment.
- PGMplusLC2 is faster than PGMplusLC.
- Transmission speed is 64Kbyte/s




2. Vdd
4. GND
6. Serial Clock
8. Serial Data

**Figure 1.6** PGMplusLC Writer

**E-PGM+ Gang4/6**

- Product name : **E-PGM+ GANG 4**
- Dimension(x , y, h) : 33.5 x 22.5 x35mm
- Weight : 2.0kg
- Input Voltage : DC Adaptor 15V/2A
- Power Consumption :
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

- Product name : **E-PGM+ GANG 6**
- Dimension(x , y, h) : 148.2 x 22.5 x35mm
- Weight : 2.8kg
- Input Voltage : DC Adaptor 15V/2A
- Power Consumption :
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

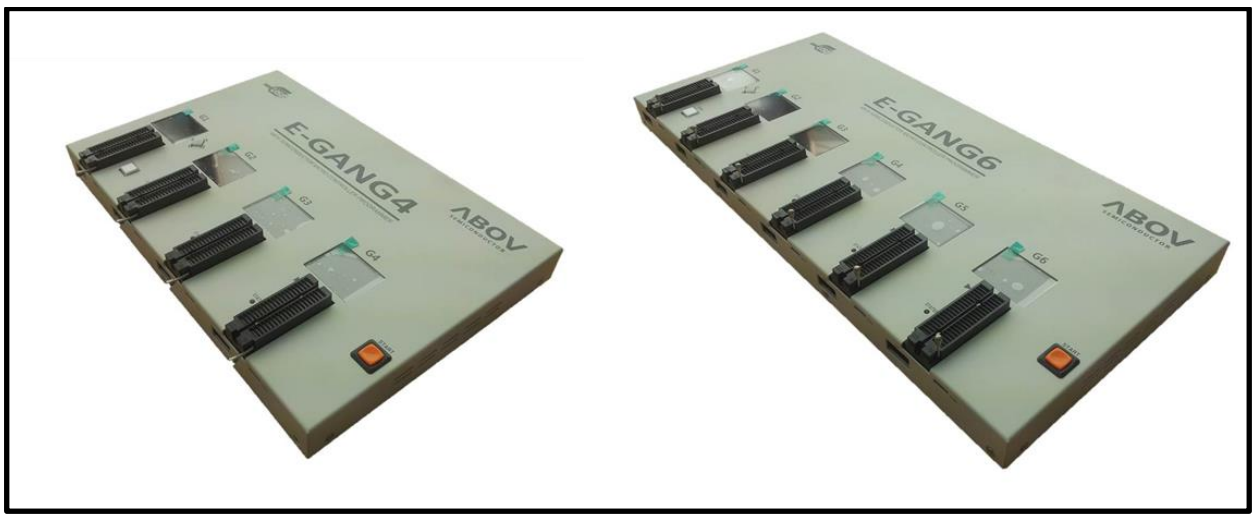



**Figure 1.7** Gang Programmer

# 2 Block diagram

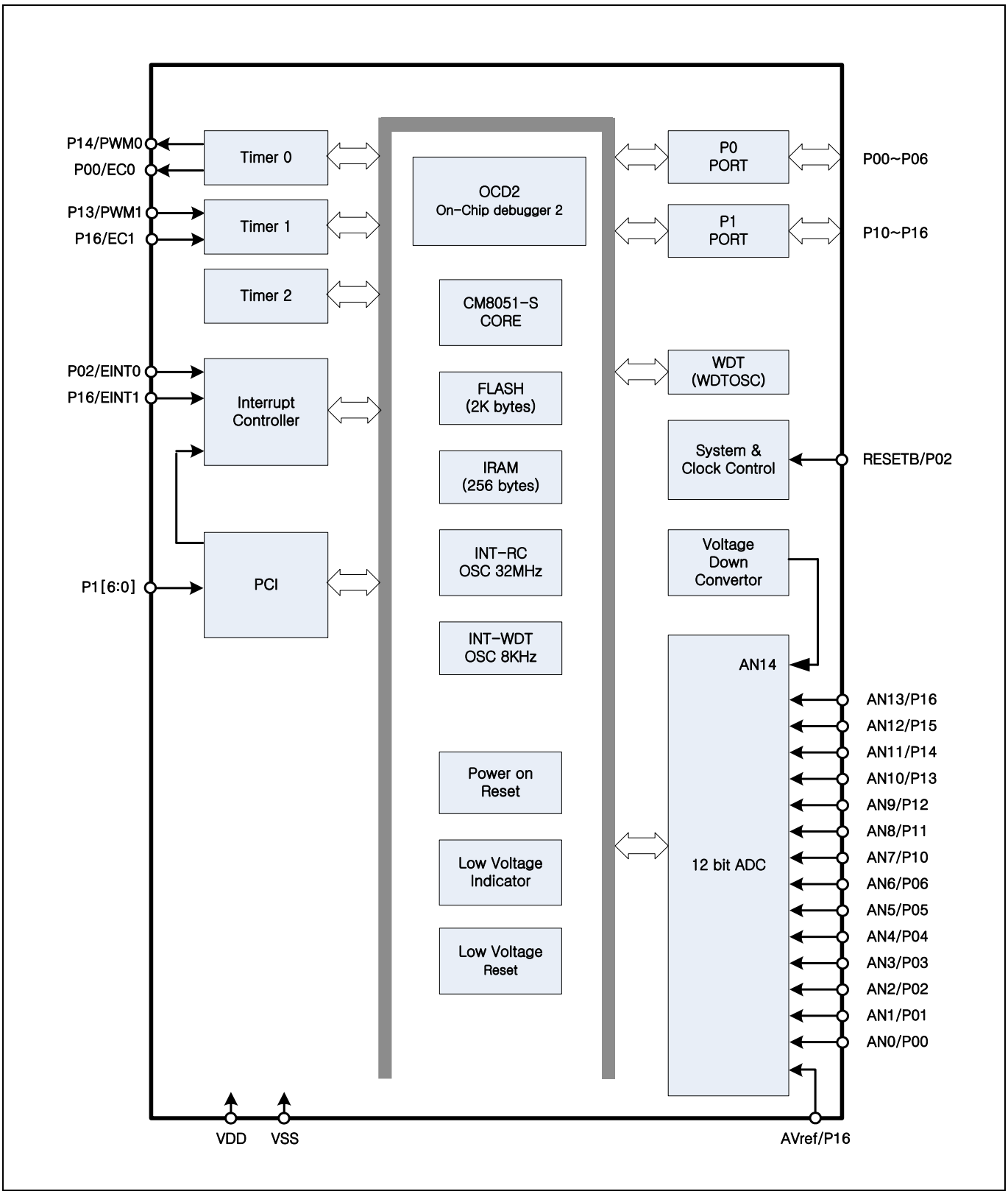



**Figure 2.1** Block diagram of MC94F1202A

# 3 Pin assignment

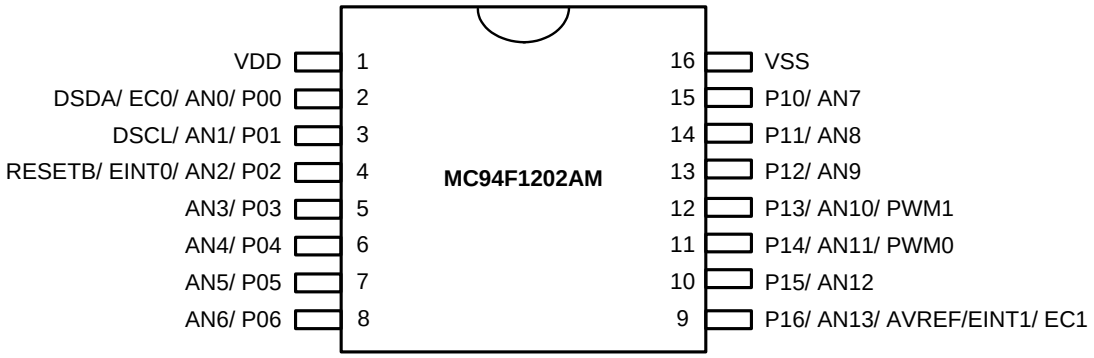



**Figure 3.1** MC94F1202AM 16 SOP pin assignment

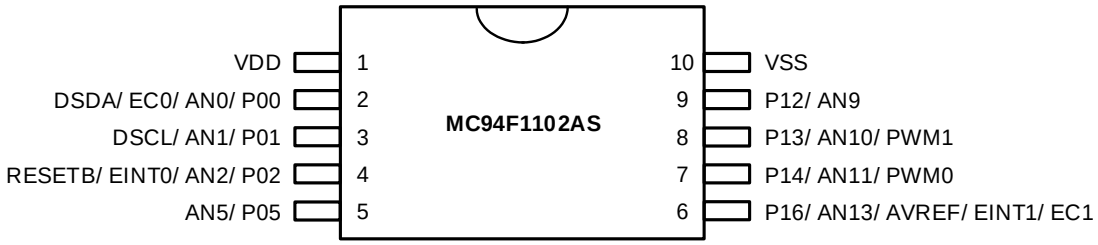



**Figure 3.2** MC94F1102AS 10 SSOP pin assignment

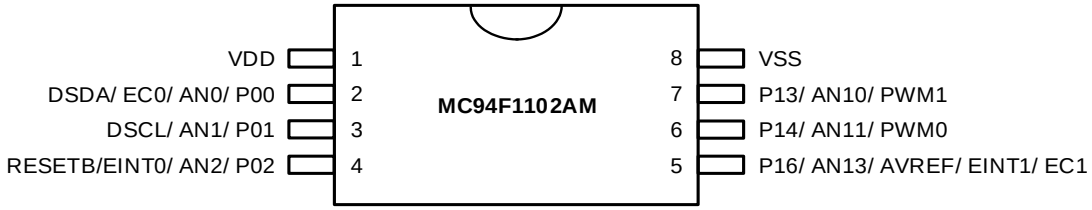



**Figure 3.3** MC94F1102AM 8 SOP pin assignment

**Note) When using 10-pin, 8-pin products, floating port should be set to input pull-up or output state in order to prevent current consumption.**

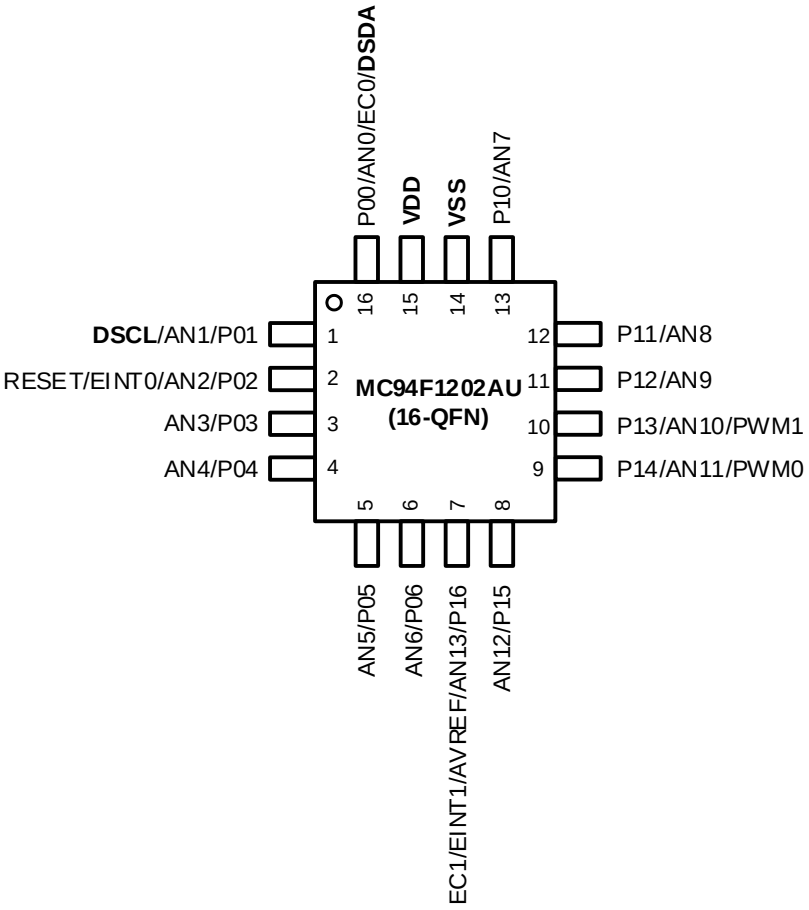



**Figure 3.4** MC94F1202AU 16 QFN pin assignment

# 4 Package Diagram

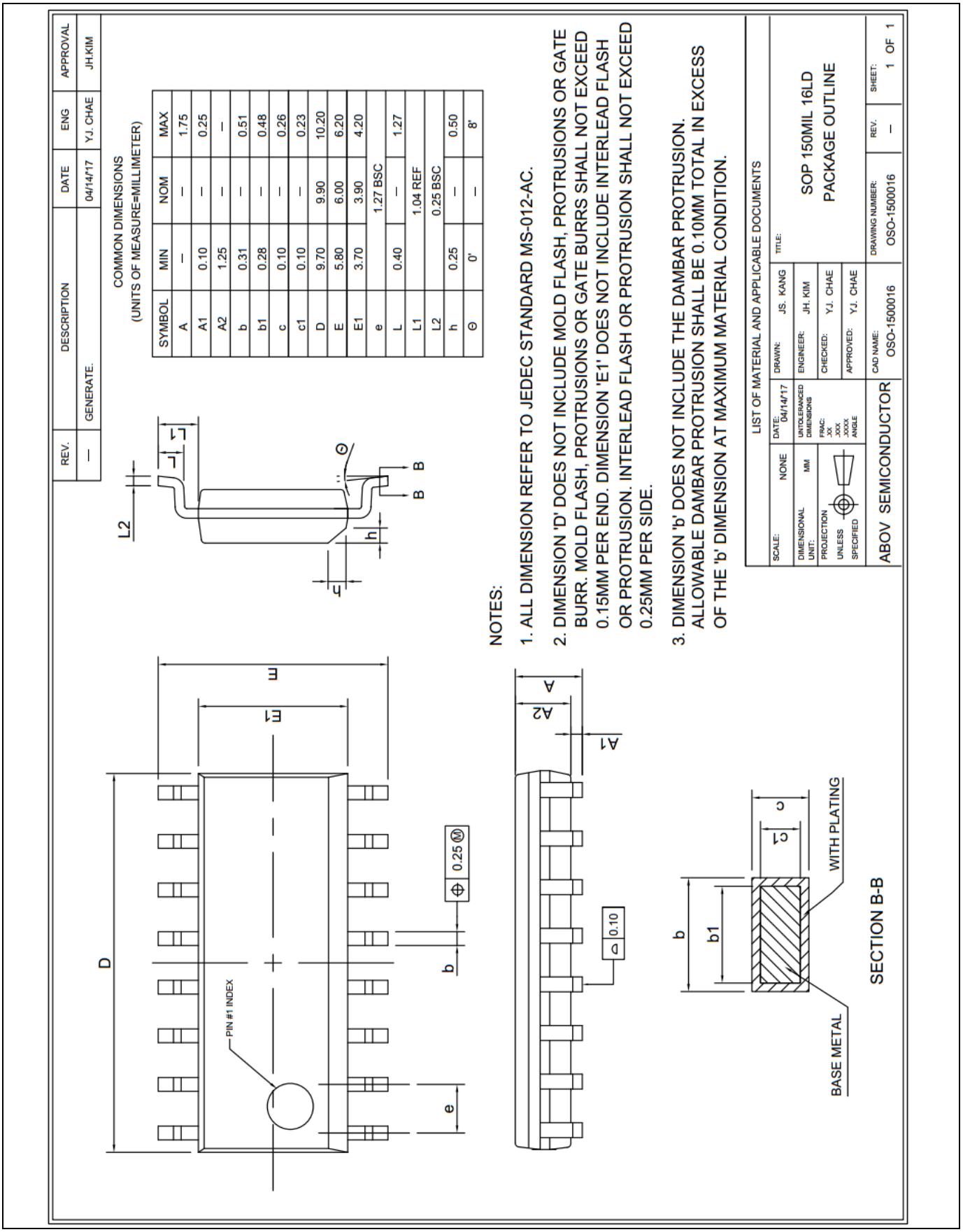



**Figure 4.1** 16-Pin SOP Package

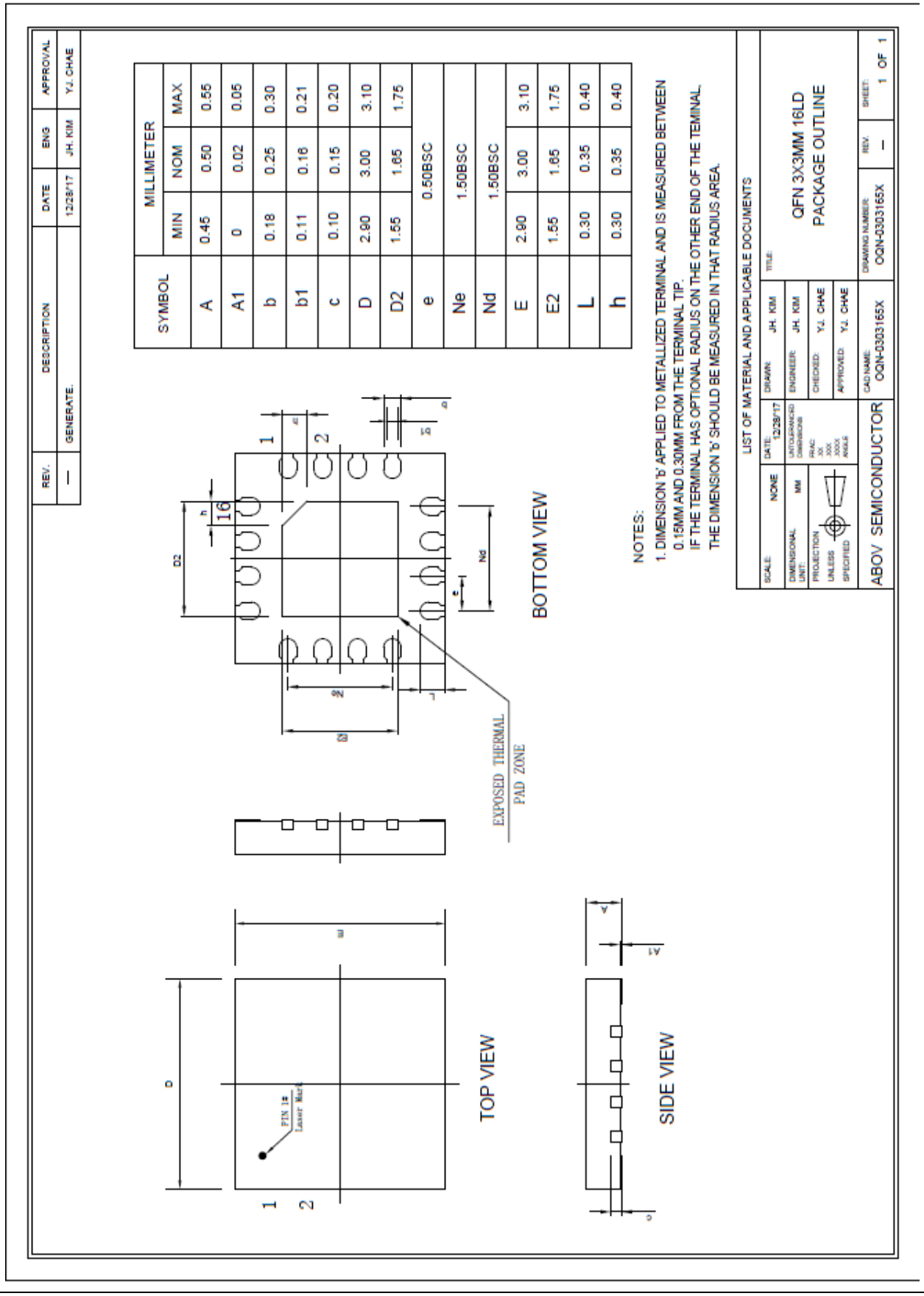



**Figure 4.2** 16-Pin QFN Package

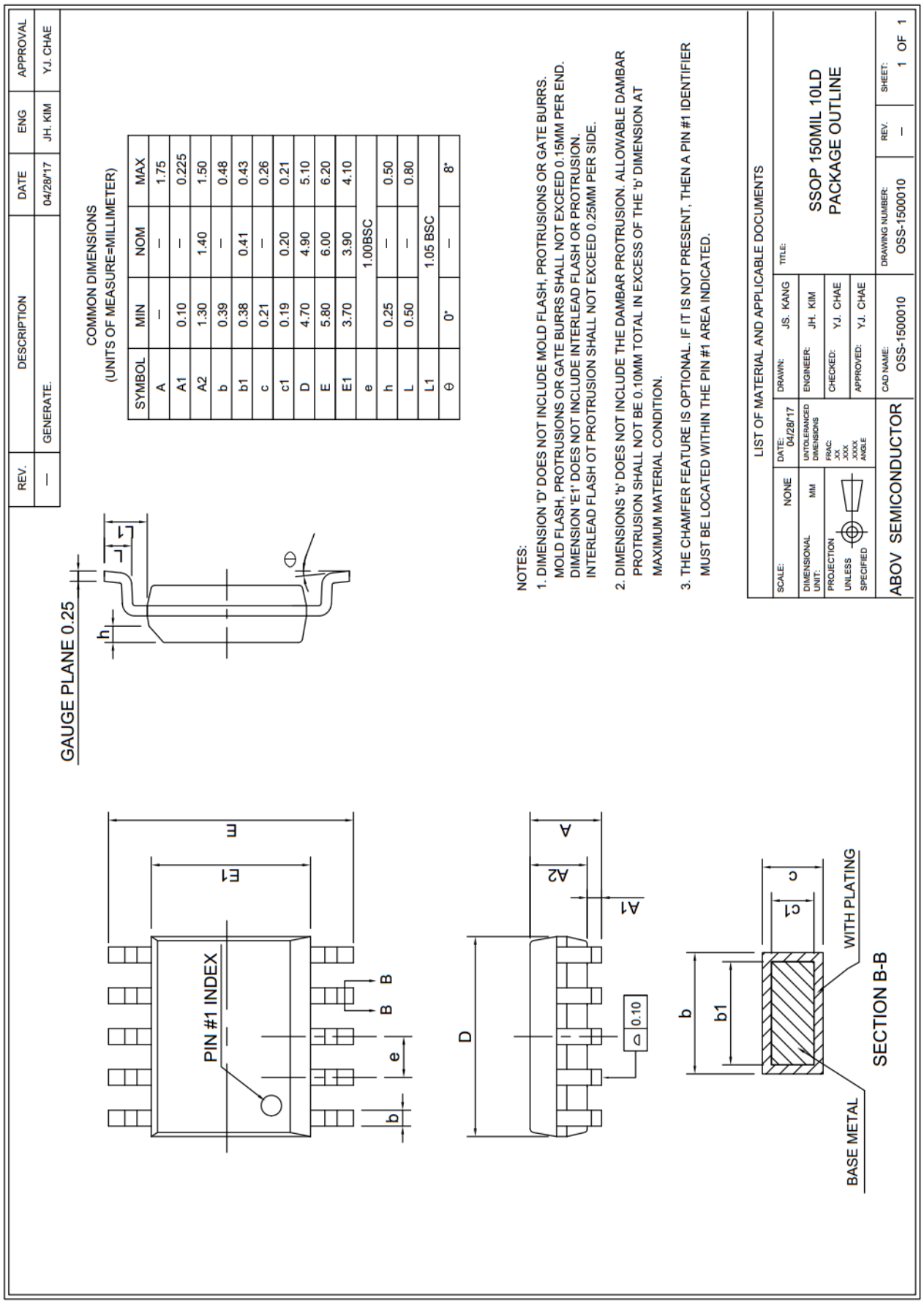



**Figure 4.3** 10-Pin SSOP Package

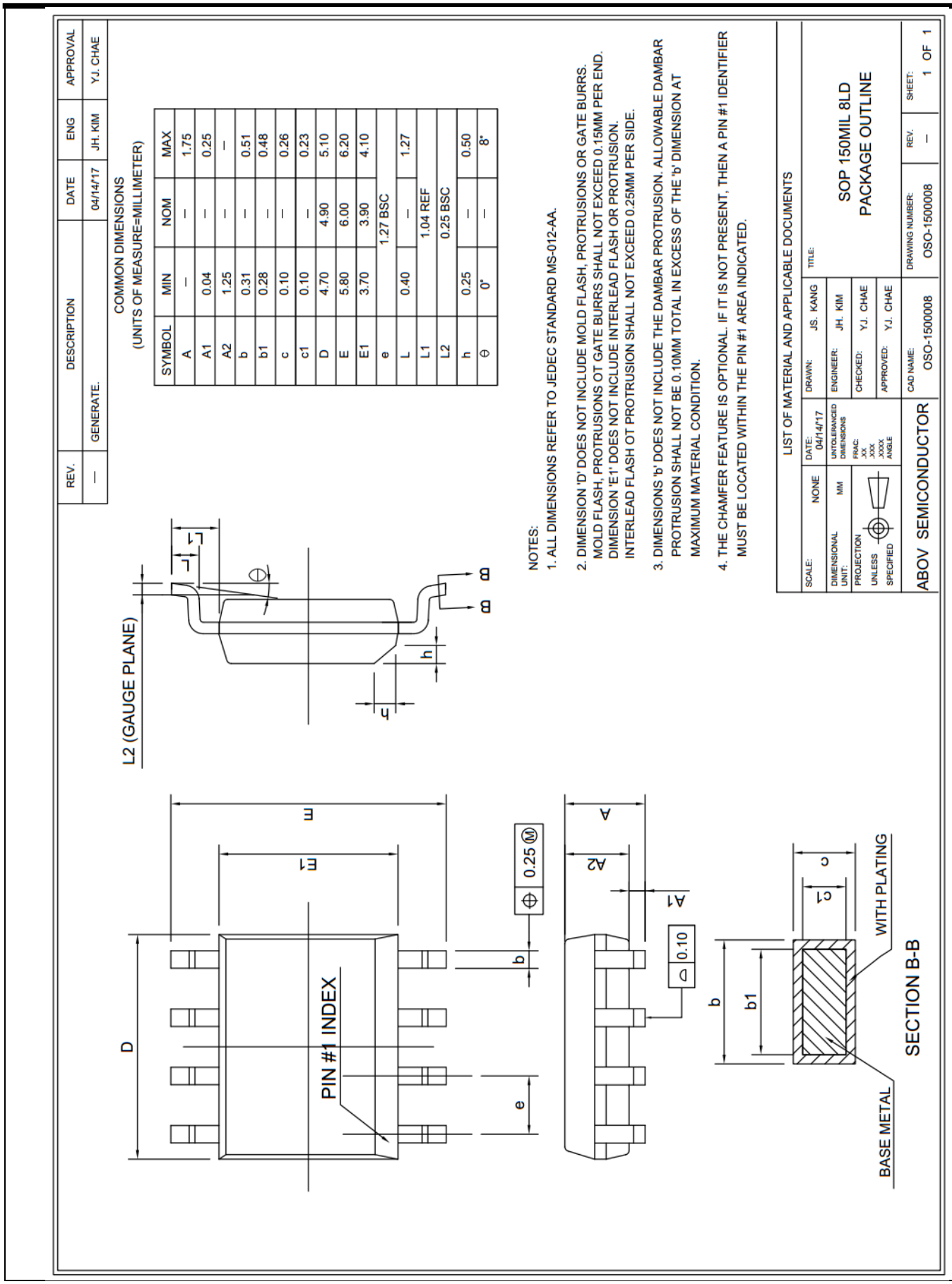



**Figure 4.4** 8-Pin SOP Package

# 5 Pin Description

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| P00 | I/O | **Port P0**<br><br>7-bit I/O Port<br>Can be set in input or output mode in 1-bit units<br>Internal pull-up register can be selected by software when this port is used as input port<br>Open Drain enable register can be selected by software when this port is used as output port | Input | AN0/ EC0/ DSDA |
| P01 | | | | AN1/ DSCL |
| P02 | | | | AN2/ EINT0/ RESETB |
| P03 | | | | AN3 |
| P04 | | | | AN4 |
| P05 | | | | AN5 |
| P06 | | | | AN6 |
| P10 | I/O | **Port P1**<br><br>7-bit I/O Port<br>Can be set in input or output mode in 1-bit units<br>Internal pull-up register can be selected by software when this port is used as input port<br>Open Drain enable register can be selected by software when this port is used as output port | Input | AN7 |
| P11 | | | | AN8 |
| P12 | | | | AN9 |
| P13 | | | | AN10/ PWM1 |
| P14 | | | | AN11/ PWM0 |
| P15 | | | | AN12 |
| P16 | | | | AN13/ AVREF/EINT1/ EC1 |
| VDD | | Power Supply | | |
| VSS | | System Ground | | |

**Table 5.1** Pin Description

# 6 Port Structure

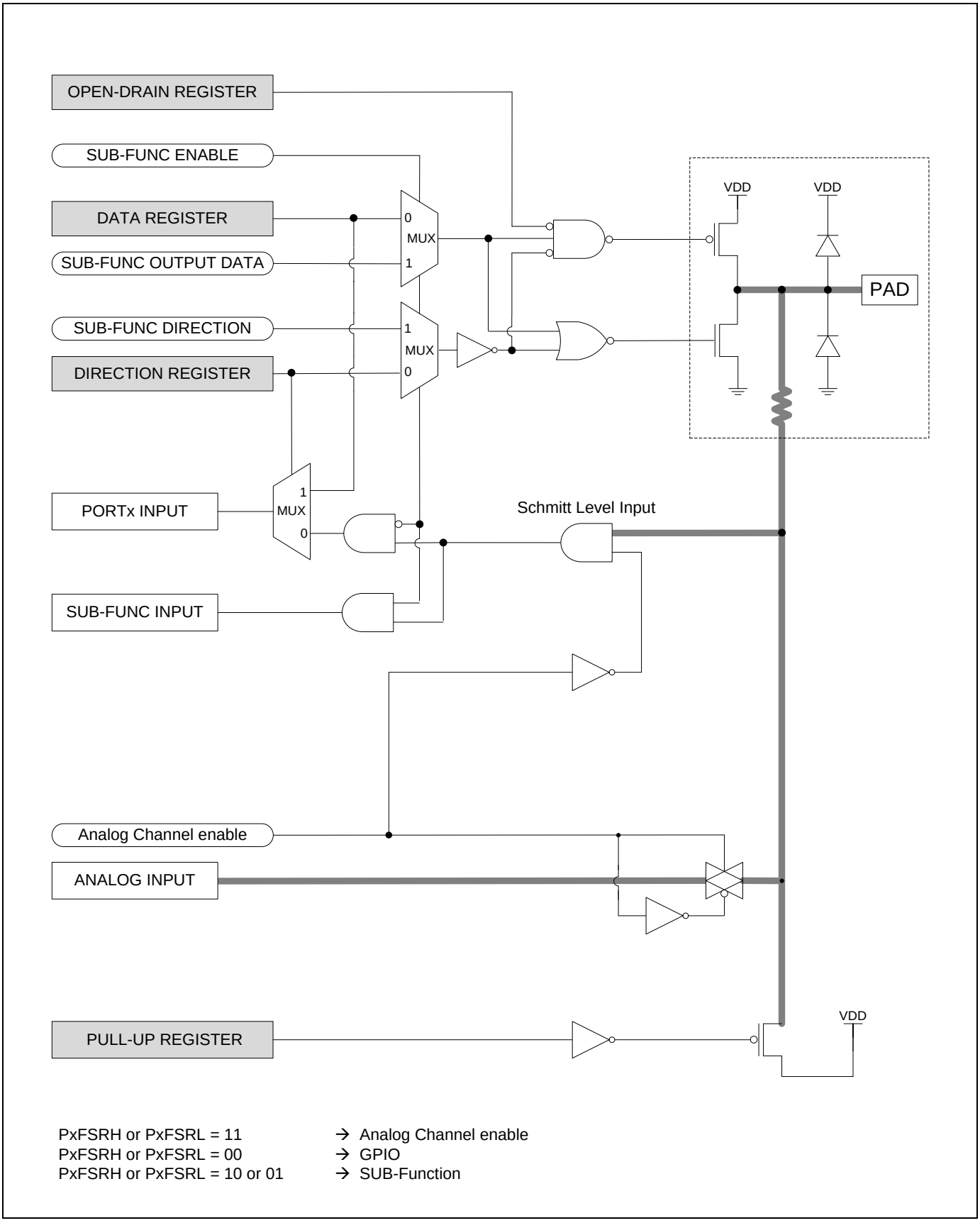



**Figure 6.1** Second Function I/O Por

# 7 Electrical Characteristics

## 7.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply Voltage | VDD | -0.3~+6.5 | V | – |
| Normal Voltage Pin | $V_I$ | -0.3~VDD+0.3 | V | Voltage on any pin with respect to VSS |
| | $V_O$ | -0.3~VDD+0.3 | V | |
| | $V_{IK}$ Note2) | $V_{IK}$ < 6.5 | V | $I_{IK}$ = 200uA |
| | | (VDD- $V_{IK}$) < 6.5 | V | $I_{IK}$ = -200uA |
| | $I_{OH}$ | -10 | mA | Maximum current output sourced by ($I_{OH}$ per I/O pin) |
| | $\sum I_{OH}$ | -80 | mA | Maximum current ($\sum I_{OH}$) |
| | $I_{OL}$ | 20 | mA | Maximum current sunk by ($I_{OL}$ per I/O pin) |
| | $\sum I_{OL}$ | 160 | mA | Maximum current ($\sum I_{OL}$) |
| Total Power Dissipation | $P_T$ | 600 | mW | – |
| Storage Temperature | $T_{STG}$ | -65~+150 | °C | – |

**Table 7.1** Absolute Maximum Ratings

**NOTE)**

1. **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

2. **$V_{IK}$ is instantaneous voltage like noise. (Burst, Impulse etc)**

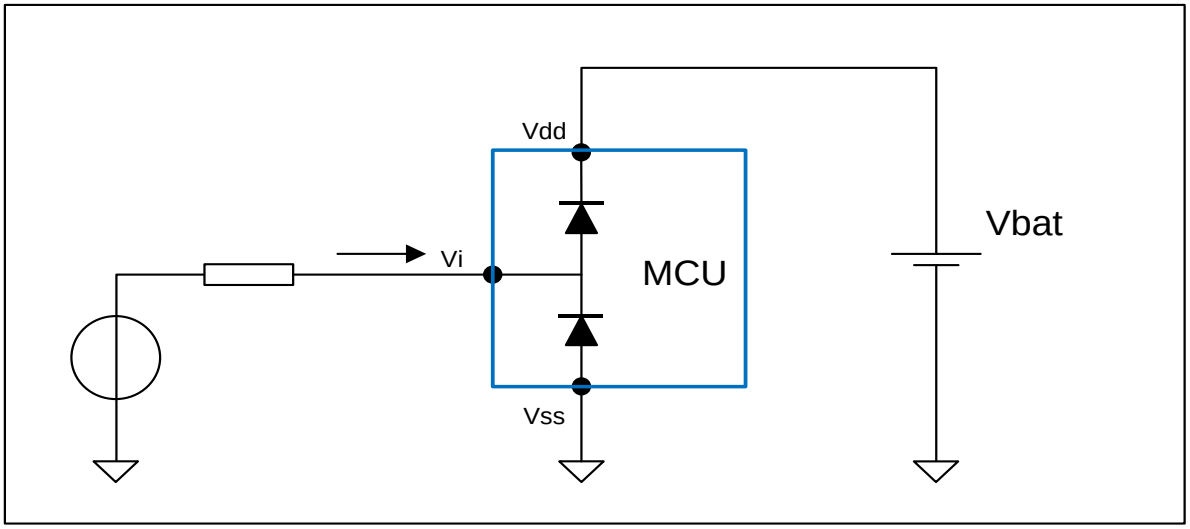



**Figure 7.1** Figure Describing $V_{IK}$

## 7.2 Recommended Operating Conditions

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Operating Voltage | VDD | $f_X$= 1, 4, 8, 16MHz | $T_{OPR}$(NOTE1) = -40~+85°C<br>$T_{OPR}$(NOTE1) = -40~+105°C | 2.2 | – | 5.5 | V |
| | | $f_X$= 1, 4, 8MHz | $T_{OPR}$ = +5~+35°C | $V_{LVR}$(NOTE2) | – | 5.5 | |

**Table 7.2** Recommended Operating Conditions

**NOTE1)** $T_{OPR}$ is the Operating Temperature.
**NOTE2)** $V_{LVR}$ is the reset release voltage by Low Voltage Reset. Refer to chapter 7.5 for Low Voltage Reset characteristics.

## 7.3 A/D Converter Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD= 2.2V ~ 5.5V, VSS=0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | – | AVREF=2.7V~5.5V | | –- | 12 | – | bit |
| Integral Non-Linearity | INL | Analog Reference Voltage = 2.7V ~ 5.5V<br>fx= 8MHz | | – | – | ±4 | LSB |
| Differential Non-Linearity | DNL | | | – | – | ±1 | |
| Zero Offset Error | ZOE | | | -3 | – | +7 | |
| Overall Accuracy | OA | | | – | – | ±3 | |
| Conversion Time | $t_{CONV}$ | AVREF = 4.0V ~ 5.5V | | 20 | – | – | us |
| | | AVREF = 3.0V ~ 5.5V | | 30 | – | – | |
| | | AVREF = 2.7V ~ 5.5V | | 60 | – | – | |
| Analog Input Voltage | $V_{AIN}$ | – | | VSS | – | VDD | V |
| Analog Reference Voltage | AVREF | 2.7V (NOTE1) | | 2.7 | – | – | V |
| Analog Input Leakage Current | $I_{AIN}$ | AVREF=5.12V | | – | – | 2 | uA |
| ADC Operating Current | $I_{ADC}$ | Enable | VDD=5.12V | – | 1 | 2 | mA |
| | | Disable | | – | – | 0.1 | uA |

**Table 7.3** A/D Converter Characteristics

**NOTE1)** When Analog Reference Voltage is lower than 2.7V, the ADC resolution is decrease.
**NOTE2)** ADC clock should be used below 3MHz. If the Analog Reference Voltage is low, the A/D clock speed should also be slow.
**NOTE3)** If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V.
(@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)
**NOTE4)** ADCLK must be less than 0.5MHz. If ADCLK is less than 0.125MHz, it can be improved INL characteristic.

| VDD = AVREF [V] | Resolution | Conditions |
|---|---|---|
| 2.6 | Upper 11-bit valid | ADCLK ≤ 0.5MHz, INL = ±6 [LSB] |
| 2.5 | Upper 10-bit valid | |
| 2.4 | Upper 9-bit valid | |
| 2.3 | Upper 8-bit valid | |
| 2.2 | Upper 7-bit valid | |
| 2.1 | Upper 6-bit valid | |
| 2.0 | Upper 5-bit valid | |
| 1.9 | Upper 4-bit valid | |
| 1.8 | Upper 3-bit valid | |

**Table 7.4** Recommended ADC Resolution

**NOTE5) Table 7.4 is not guaranteed to work at voltage below 2.7V and this table should be used for reference only.**

## 7.4 BMR Reference Voltage Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=2.2 ~ 5.5V, VSS=0V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| BMR Reference Voltage | $V_{BMR}$ | -40°C ~ +85°C<br>-40°C ~ +105°C | 1.205 | 1.295 | 1.385 | V |

## 7.5 Power-On Reset Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=2.2 ~ 5.5V, VSS=0V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| RESET Release Level | $V_{POR}$ | – | 0.9 | 1.1 | 1.3 | V |
| VDD Voltage Rising Time | $t_R$ | 0V to 2.0V | 0.05 | – | 5 | V/ms |
| POR Current | $I_{POR}$ | – | – | 0.1 | – | uA |

**Table 7.5** Power-On Reset Characteristics

## 7.6 Low Voltage Reset and Low Voltage Indicator Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=5.0V, VSS=0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Detection Level | $V_{LVR}$<br>$V_{LVI}$ | The LVR can select all levels but LVI can select other levels except 1.80V | | 1.65 | 1.80 | 1.95 | V |
| | | | | 1.6 | 2.1 | 2.6 | |
| | | | | 1.95 | 2.5 | 3.05 | |
| | | | | 2.9 | 3.5 | 4.1 | |
| Hysteresis | △V | – | | – | 50 | - | mV |
| Minimum Pulse Width | $t_{LW}$ | – | | - | 500 | – | us |
| LVR and LVI Current | $I_{BL}$ | LVR 1.80V | VDD=5V | – | 1 | - | uA |
| | | LVR/LVI except 1.80V | | – | - | 50 | |

**Table 7.6** LVR and LVI Characteristics

## 7.7 Internal RC Oscillator Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=2.2V ~ 5.5V, VSS=0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Frequency | $f_{IRC}$ | $V_{DD}$ = 2.2 ~ 5.5V | | – | 32 | – | MHz |
| Tolerance | – | $T_A$ = 25°C | With 0.1uF Bypass capacitor | – | – | ±1.5 | % |
| | | $T_A$ = -20°C to +60°C | | | | ±2.5 | |
| | | $T_A$ = -40°C to +85°C | | | | ±3.0 | |
| | | $T_A$ = -40°C to +105°C | | | | ±5.0 | |
| Stabilization Time | $T_{HFS}$ | – | | – | 1 | - | ms |
| IRC Current | $I_{IRC}$ | Enable | | – | 0.4 | – | mA |

**Table 7.7** Internal RC Oscillator Characteristics

**NOTE)** 0.1uF bypass capacitor should be connected to VDD and VSS.

## 7.8 Internal WDT Oscillator Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=2.2V ~ 5.5V, VSS=0V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Frequency | $f_{WDTRC}$ | – | 4 | 8 | 12 | kHz |
| Stabilization Time | $t_{WDTS}$ | – | – | 1 | - | ms |
| WDTRC Current | $I_{WDTRC}$ | Enable | – | 5 | – | uA |
| | | Disable | – | – | 0.1 | |

**Table 7.8** Internal WDT Oscillator Characteristics

## 7.9 DC Characteristics

($T_A$=-40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=2.2V ~ 5.5V, VSS=0V, $f_X$=8.0MHz)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH1}$ | P0, P1 | 0.8VDD | – | VDD | V |
| Input Low Voltage | $V_{IL1}$ | P0, P1 | – | – | 0.2VDD | V |
| Output High Voltage | $V_{OH1}$ | VDD=3.3V, $I_{OH}$=-5mA, All output ports | VDD-1.5 | – | – | V |
| | $V_{OH2}$ | VDD=5V, $I_{OH}$=-10mA, All output ports | VDD-1.5 | – | – | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$= 20mA,All output ports | – | – | 1.0 | V |
| Input High Leakage Current | $I_{IH}$ | All input ports | -1 | – | 1 | uA |
| Input Low Leakage Current | $I_{IL}$ | All input ports | -1 | – | 1 | uA |
| Pull-Up Resistor | $R_{PU1}$ | $V_I$=0V, $T_A$= 25°C All Input ports | 25 | 50 | 75 | kΩ |
| Power Supply Current | $I_{DD1}$ (RUN) | Run Mode, $f_X$=8MHz | - | 3 | 5 | mA |
| | $I_{IDD2}$ (IDLE) | IDLE Mode, $f_X$=8MHz | - | 2 | 4 | mA |
| | $I_{DD3}$ (STOP1) | STOP1 Mode, WDTRC Enable, LVR ON | - | 5 | 10 | uA |
| | $I_{DD4}$ (STOP2) | STOP2 Mode, WDTRC Disable, LVR ON | - | 2.5 | 5 | uA |
| | $I_{DD5}$ (STOPL) | STOP2 Mode, WDTRC Disable, LVR OFF | - | 1 | - | uA |

**Table 7.9** DC Characteristics

**NOTE)** STOP1: WDT only running, STOP2: All function disable.

## 7.10 AC Characteristics

($T_A$= -40°C ~ +85°C or $T_A$=-40°C ~ +105°C, VDD=2.2V ~ 5.5V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| RESETB input low width | $t_{RST}$ | Input, VDD=5V | - | 500 | – | us |
| Interrupt input high, low width | $t_{IWH}$, $t_{IWL}$ | All interrupt, VDD=5V | 125 | – | – | ns |
| External Counter Input High, Low Pulse Width | tECWH, tECWL | ECn, VDD=5V (n=0, 1) | 125 | – | – | ns |
| External Counter Transition Time | tREC, tFEC | ECn, VDD=5V (n=0, 1) | - | – | 20 | ns |

**Table 7.10** AC Characteristics

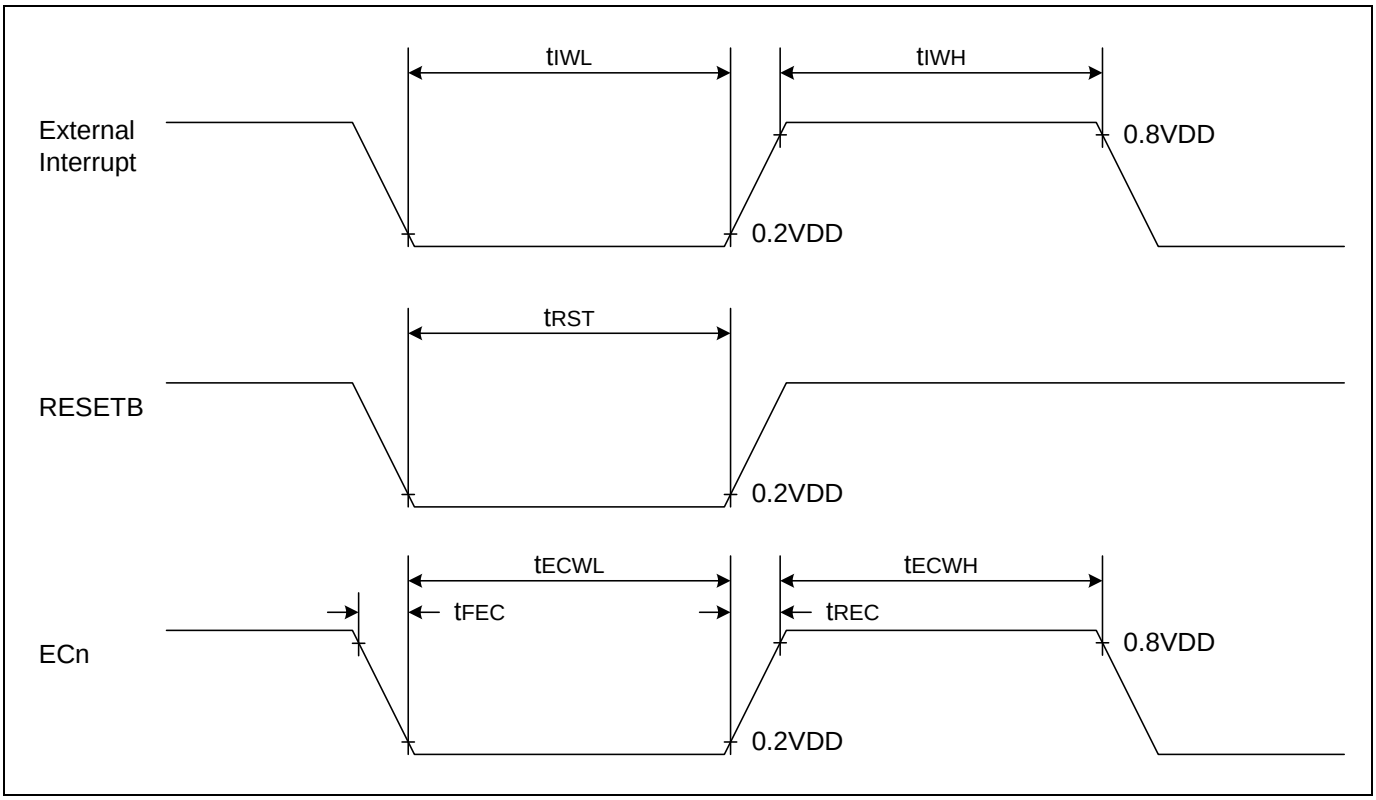



**Figure 7.2** AC Timing

## 7.11 Operating Voltage Range

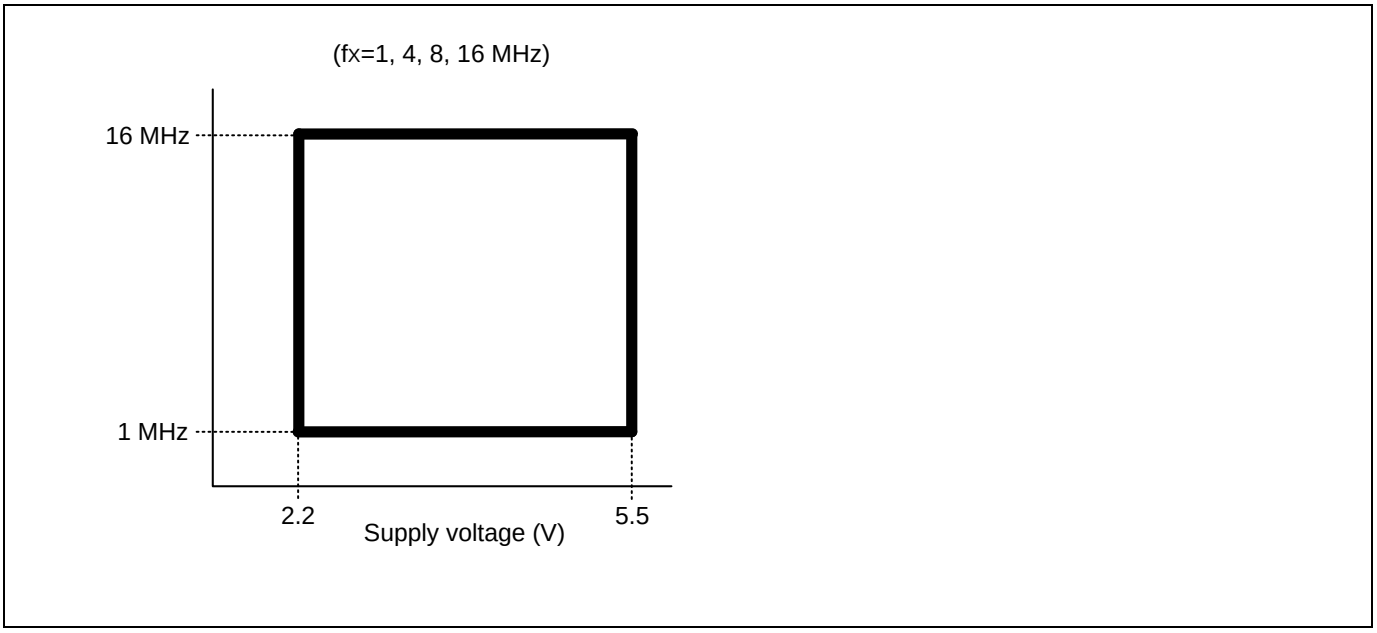



**Figure 7.3** Operating Voltage Range

## 7.12 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

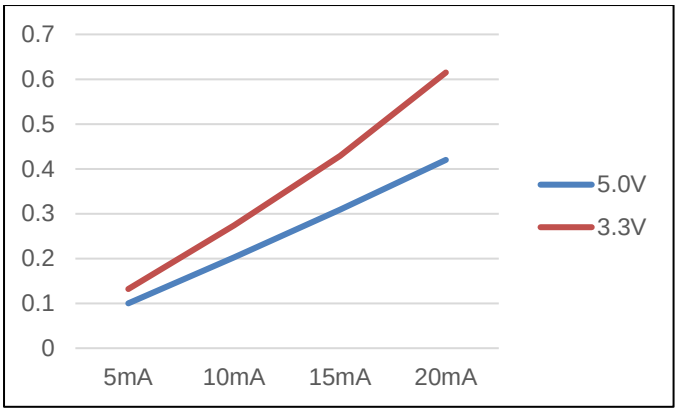



**Figure 7.4** Output Low Voltage ($V_{OL}$)

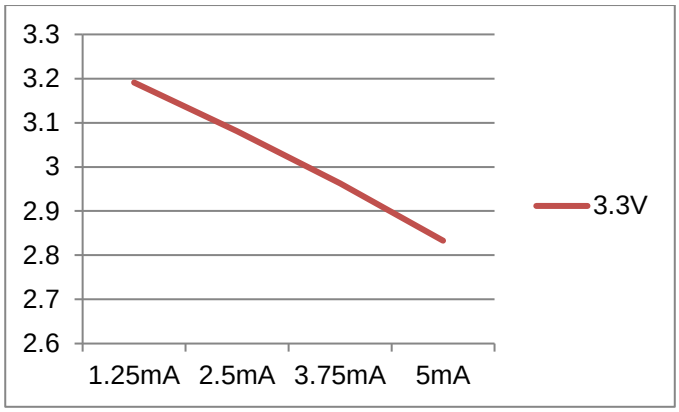



**Figure 7.5** Output High Voltage ($V_{OL1}$)

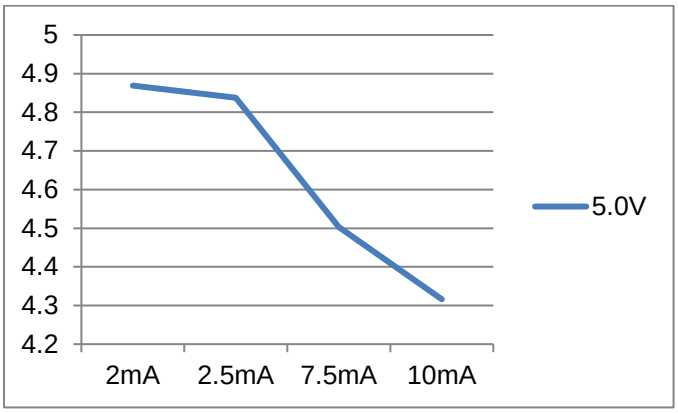



**Figure 7.6** Output High Voltage ($V_{OL2}$)

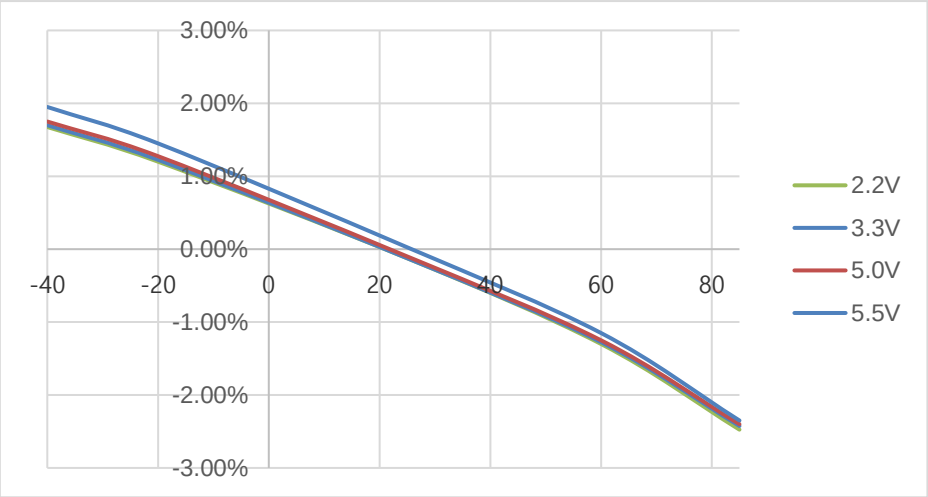



**Figure 7.7** IRC Tolerance

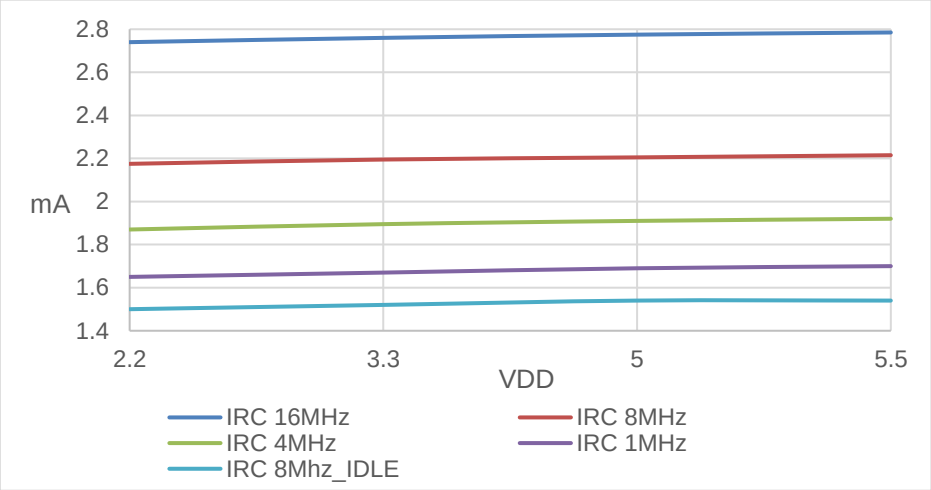



**Figure 7.8** Power Supply Current (RUN, IDLE)

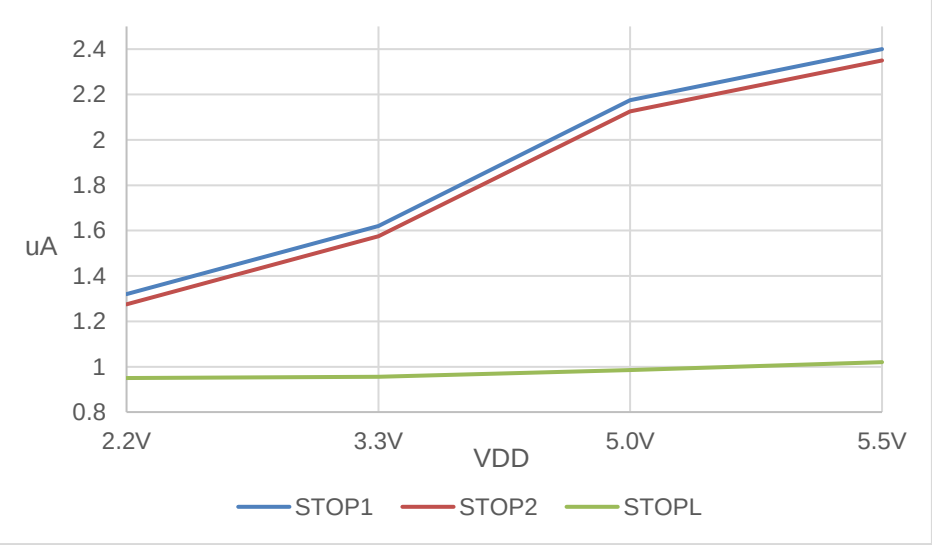



**Figure 7.9** Power Supply Current (STOP1, STOP2, STOPL)

## 7.13 Recommended Application Circuit

For the microprocessor and other devices in the system to function correctly, it is also necessary to monitor the supply voltage during operations. Voltage drops or glitches on the power supply lines, can cause unwanted changes in the internal registers, which can lead to instructions being incorrectly executed, incorrect output signals and errors in the operations results. If noise is applied to the VDD rising slope due to external factors during the POR, the microprocessor may malfunction because the microprocessor continues to operate and does not recognize that the voltage has fallen below the threshold due to the internal RC time constants. Therefore, VDD / GND requires a power capacitor for VDD drop and a decoupling capacitor for high frequency noise. Normally, electrolytic / tantalum capacitors of 10uf / 9V or more are recommended for power capacitors and multilayer ceramic capacitors of 0.1uF or more are recommended for decoupling capacitors. Decoupling capacitors should be placed as close as possible to the microprocessor.

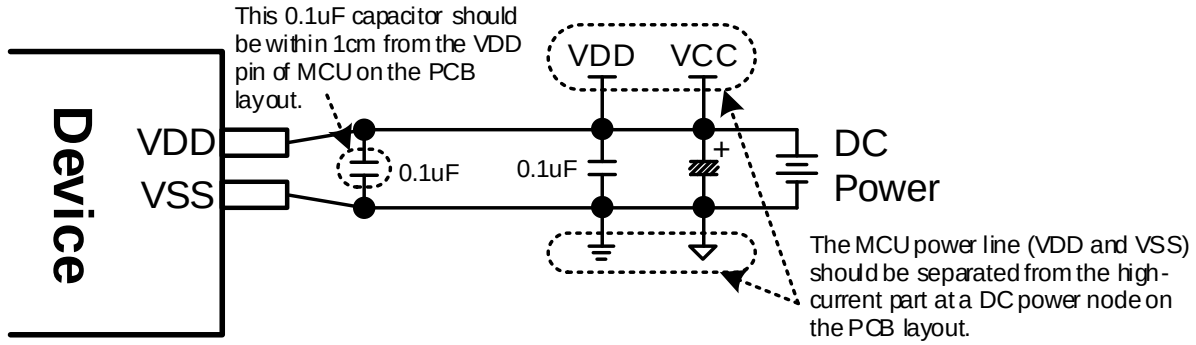



**Figure 7.10** Recommended Power Circuit part when using DC Power.

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