MC96F1206
Datasheet

CMOS single-chip 8-bit MCU with 12-bit ADC and LDO

Datasheet Version 1.22

Features

Core

- 8-bit CISC M8051 core
  (8051 Compatible, 2 clocks per cycle)

6 Kbytes On-Chip FLASH

- Endurance : 10,000 cycles
- In-System Programming (ISP)

256 bytes IRAM

General Purpose I/O (GPIO)

- Normal I/O: 18 Port (P0[7:0], P1[7:0], P2[2:0]

Timer/Counter/PWM

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watch Dog Timer (WDT) 8-bit × 1-ch
- PWM : T0/T1

12-bit A/D Converter

- 15 Input channels
- Internal 2.5V LDO reference(option)

16-bit CRC/Checksum Generator

Power On Reset

- Reset release level (1.1V)

Low Voltage Indicator

- 1 Level (1.75V)

Low Voltage Reset

3 levels detect (2.1V/2.5V/3.5V)

Interrupt Sources

- External Interrupts (3, with PCI)
- Timer(0/1) (2), WDT (1), BIT (1)
- ADC (1)

Internal RC Oscillator

- 32MHz ±5.0% (TA=-40~ +85°C)

Power Down Mode

- STOP1, STOP2, IDLE mode

Operating Voltage and Frequency

- 2.2V to 5.5V (@0.125ns to 16MHz with IRC)

Minimum Instruction Execution Time

- 125ns (@16MHz IRC)

Operating Temperature

- –40 ~ +85℃

Package Type

- 20 QFN/TSSOP, 16 SOPN
- Pb-free package

Product selection table

Table 1. Device Summary

Part number	Flash	iRAM	XRAM	Timer	ADC	I/O	Package
MC96F1206USBN	6KB	256B	-	2	15ch	18	20 QFN
MC96F1206RBN	6KB	256B	-	2	15ch	18	20TSSOP
MC96F1206MBN	6KB	256B	-	2	12ch	14	16 SOPN

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.

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1 Description

MC96F1206 is an advanced CMOS 8-bit microcontroller with 4 Kbytes of FLASH. This is a powerful microcontroller which provides low power consumption and cost effective solution to smoke detector applications.

Table 2 introduces features of MC96F1206 and peripheral counts. In addition, MC96F1206 supports power down modes to reduce power consumption.

1.1 Device overview

Table 2. MC96F1206 Device Features and Peripheral Counts

Peripheral \ Device		MC96F1206
CPU		8-bit CISC core (M8051, 2 clocks per cycle)
Flash		• 6 Kbytes with self r/w capability • On chip debug and ISP • Endurance: 10,000 cycles
iRAM		256 bytes
GPIO		• Normal I/Os • 18 ports: P0[7:0], P1[5:0], P2[2:0]
Timer/ counter		• BIT 8-bit x 1-ch • WDT 8-bit x 1-ch: 8 KHz internal RC oscillator for WDT • 16-bit x 2-ch (T0/T1)
PWM		16-bit 2-ch(T0/T1)
ADC		• 12-bit ADC, 15 input channels • 2.5V Internal reference
Reset	Power on reset	Reset release level (1.1V)
	Low voltage reset	3 level detect (2.1/ 2.5V/ 3.5V)

Peripheral \ Device	MC96F1206
Interrupt sources	• External interrupts: EINT0/1 (2) • PCI1 (1) • Timer : T0/ T1 (2) • WDT (1) • BIT (1) • ADC (1) • LVI (1)
Internal RC oscillator	• 32MHz ± 2.0% (T_A = 25℃) • 32MHz ± 5.0% (T_A = -40℃ to +85℃)
Power down mode	• STOP1,STOP2, IDLE
Operating voltage and frequency	• 2.2V to 5.5V • Voltage dropout converter included for core
Minimum instruction execution time	• 125ns @16MHz with IRC
Operating temperature	• -40℃ to +85℃
Package type	• 20QFN, 20TSSOP, 16SOPN Pb-free package

1.2 Block diagram

Figure 1 describes MC96F1206 in a block diagram.

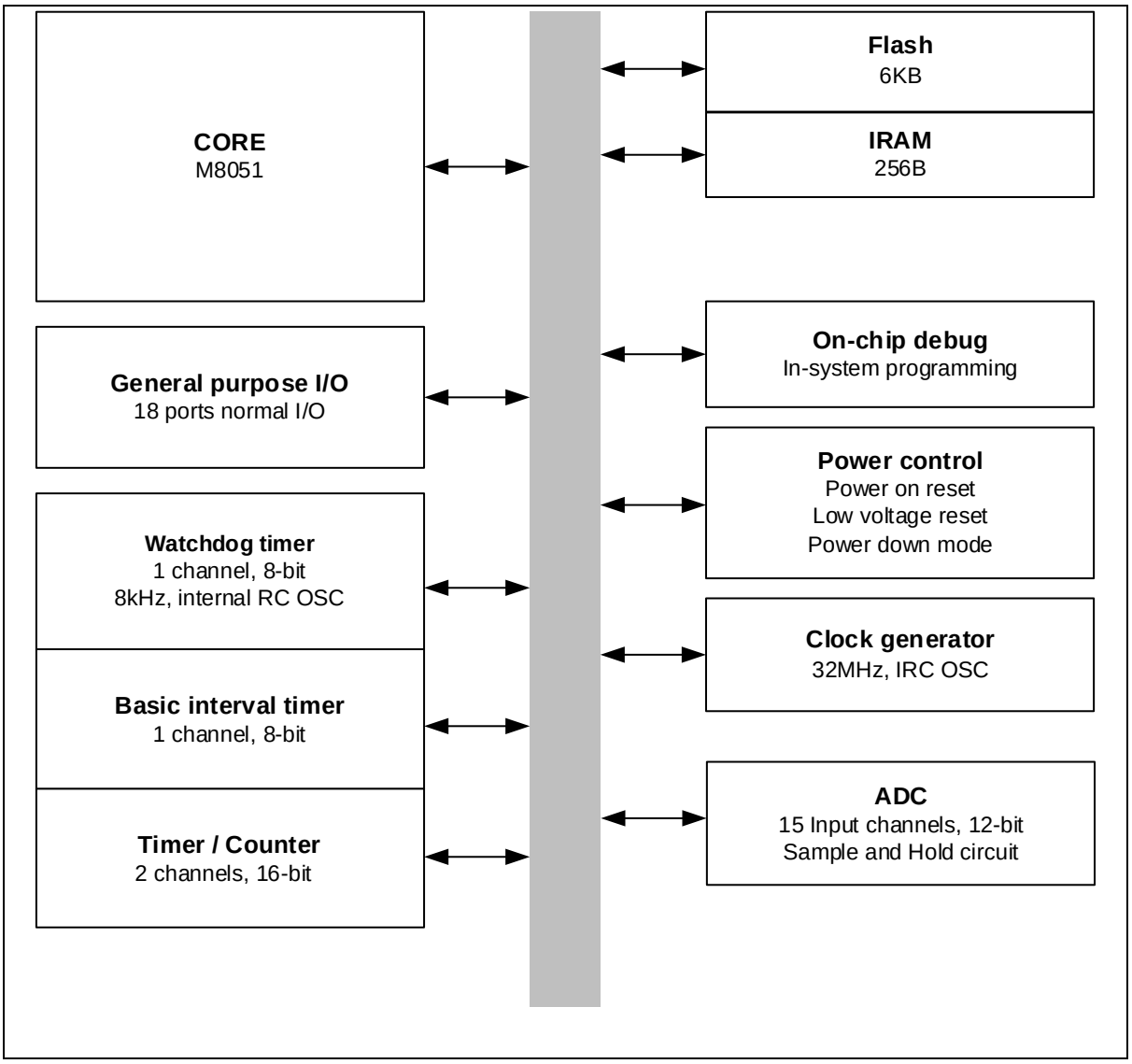


Figure 1. MC96F1206 Block Diagram

2 Pinouts and pin descriptions

In this chapter, MC96F1206 pinouts and pin descriptions are introduced.

2.1 Pinouts

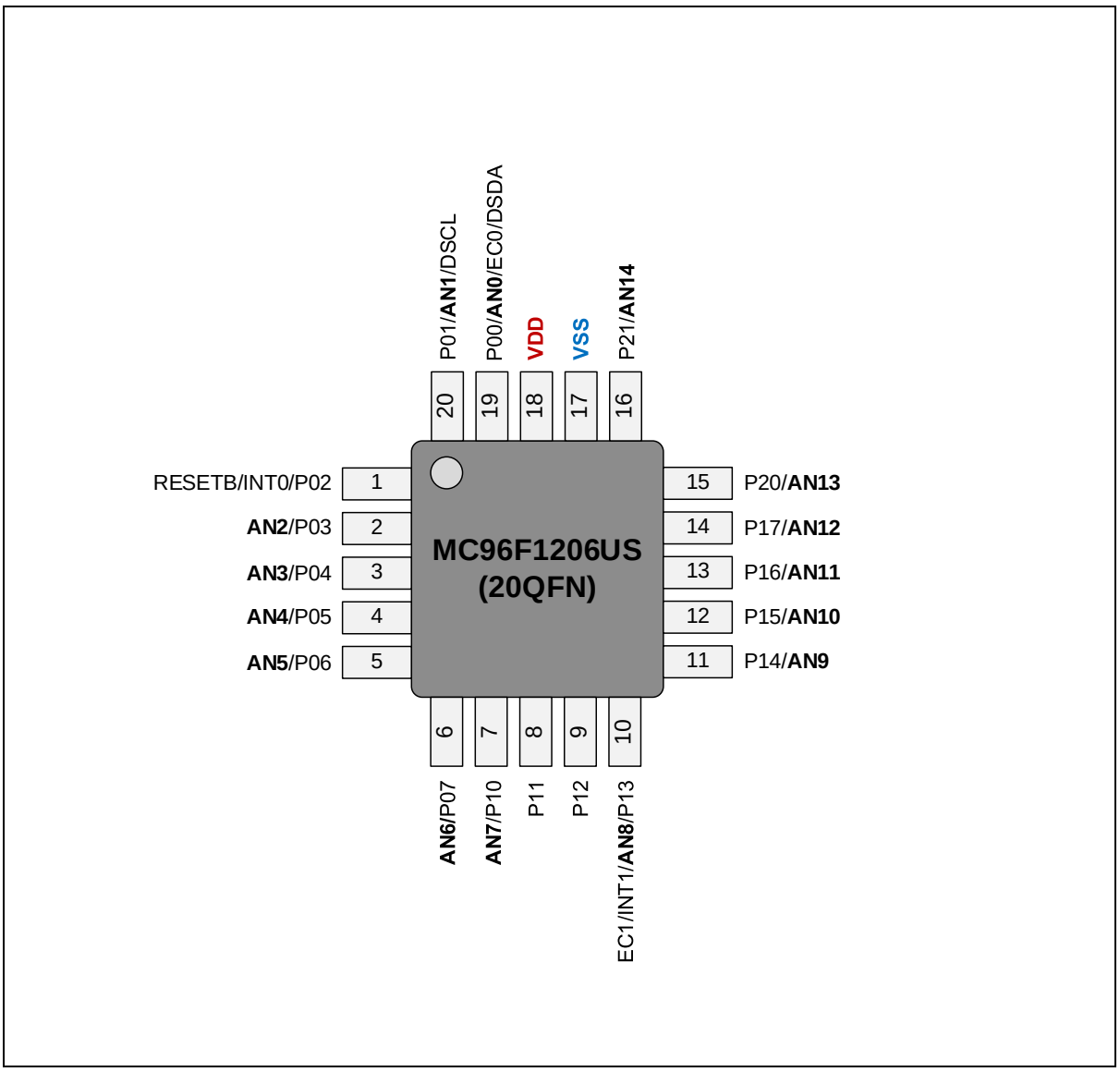


Figure 2. MC96F1206AEN 16 SOPN Pinouts

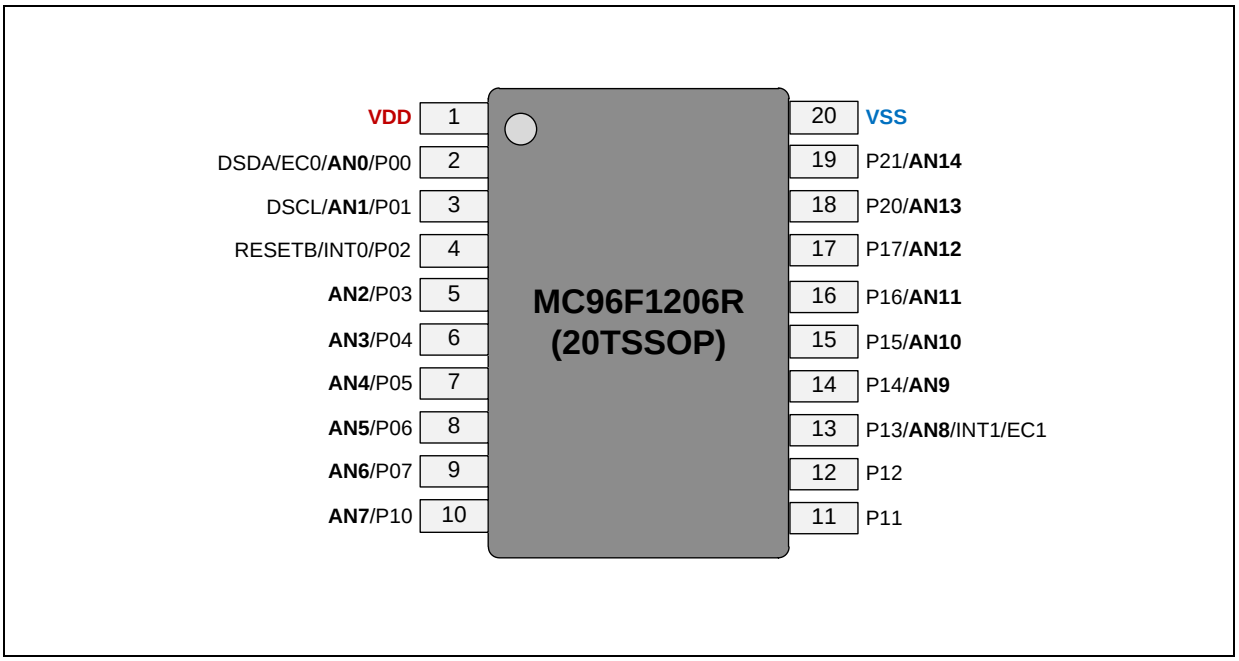


Figure 3. MC96F1206 20TSSOP assignment

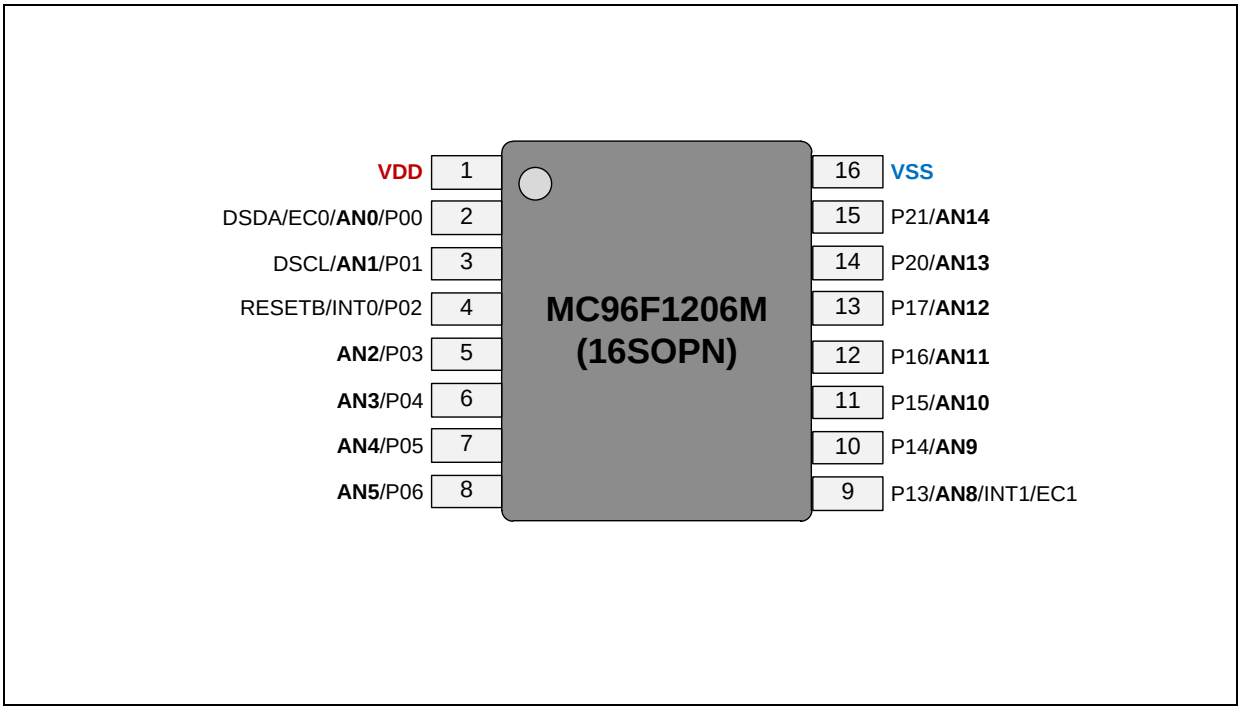


Figure 4. MC96F1206 16SOPN assignment

2.2 Pin description

Table 3. 16 SOPN Pin Description

Pin name	I/O	Function	@reset	Shared with
P00	I/O	Port P0 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN0/ EC0/ DSDA
P01				AN1/ DSCL
P02				INT0/ RESETB
P03				AN2
P04				AN3/ PWM0/ PWM1
P05				AN4/ PWM0/ PWM1
P06				AN5/ PWM0/ PWM1
P07				AN6/ PWM0/ PWM1
P10	I/O	Port P1 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN7
P11				
P12				
P13				AN8/ INT1 / EC1
P14				AN9/ PWM0/ PWM1
P15				AN10/ PWM0/ PWM1
P16				AN11/ PWM0/ PWM1
P17				AN12/ PWM0/ PWM1
P20	I/O	Port P2 2-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN13
P21				AN14
VDD		Power Supply		
VSS		System Ground		

Pin name	I/O	Function	@reset	Shared with
EINT0	I/O	External interrupt input and Timer 0 capture input	Input	P02/RESETB
EINT1	I/O	External interrupt input and Timer 1 capture input		P13/AN8/EC1
PWM0O	I/O	Timer 0 pulse output		P0[7:4], P1[7:4], PWM0
PWM1O	I/O	Timer 1 pulse output		P0[7:4], P1[7:4], PWM1
EC0	I/O	Timer 0 event count input		AN0/DSDA/P00
EC1	I/O	Timer 1 event count input		AN8/INT1/P13
AN0	I/O	A/D converter analog input channels	Input	P00/EC0/DSDA
AN1				P01/DSCL
AN2				P03
AN3				P04/PWM0/PWM1
AN4				P05/PWM0/PWM1
AN5				P06/PWM0/PWM1
AN6				P07/PWM0/PWM1
AN7				P10
AN8				P13/INT1/EC1
AN9				P14/PWM0/PWM1
AN10				P15/PWM0/PWM1
AN11				P16/PWM0/PWM1
AN12				P17/PWM0/PWM1
AN13				P20
AN14				P21

NOTES:

1. The P02/RESETB pin is configured by the “CONFIGURE OPTION”.
2. If the P00/DSDA and P01/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P00/DSDA and P01/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.

3 Port structures

3.1 GPIO port structure

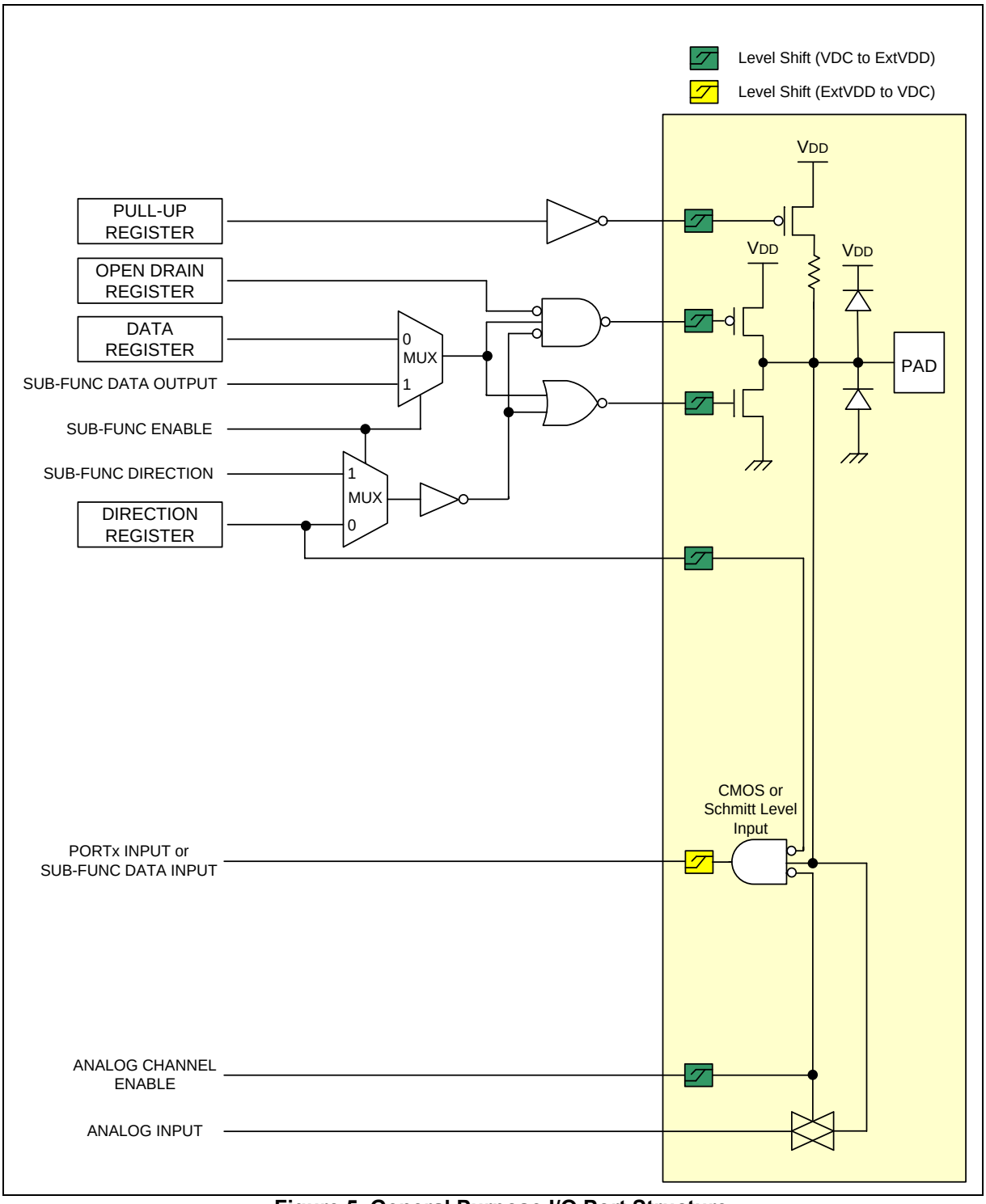


Figure 5. General Purpose I/O Port Structure

3.2 External interrupt I/O port structure

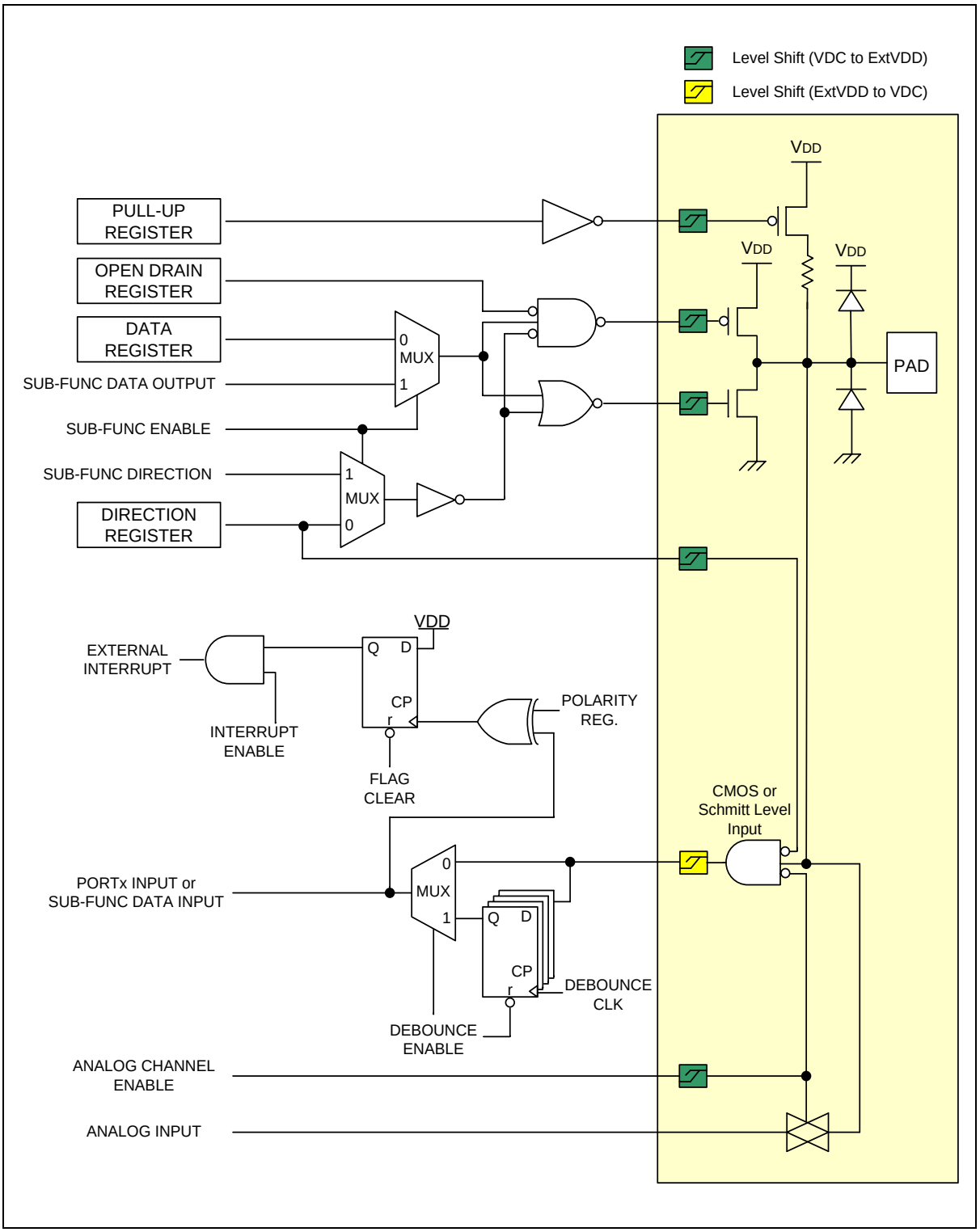


Figure 6. External Interrupt I/O Port Structure

4 Memory organization

MC96F1206 addresses two separate memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

MC96F1206 provides on-chip 6 Kbytes of the ISP type flash program memory, which is readable and writable. Internal data memory (iRAM) is 256 bytes and it includes the stack area.

4.1 Program memory

A 16-bit program counter is capable of addressing up to 64 Kbytes, but MC96F1206 has only 6 Kbytes program memory space. After reset, CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 1 is assigned to location 000BH. If the external interrupt 1 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8 byte interval.

A longer service routine can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use. Figure 8 shows a map of the lower part of the program memory.

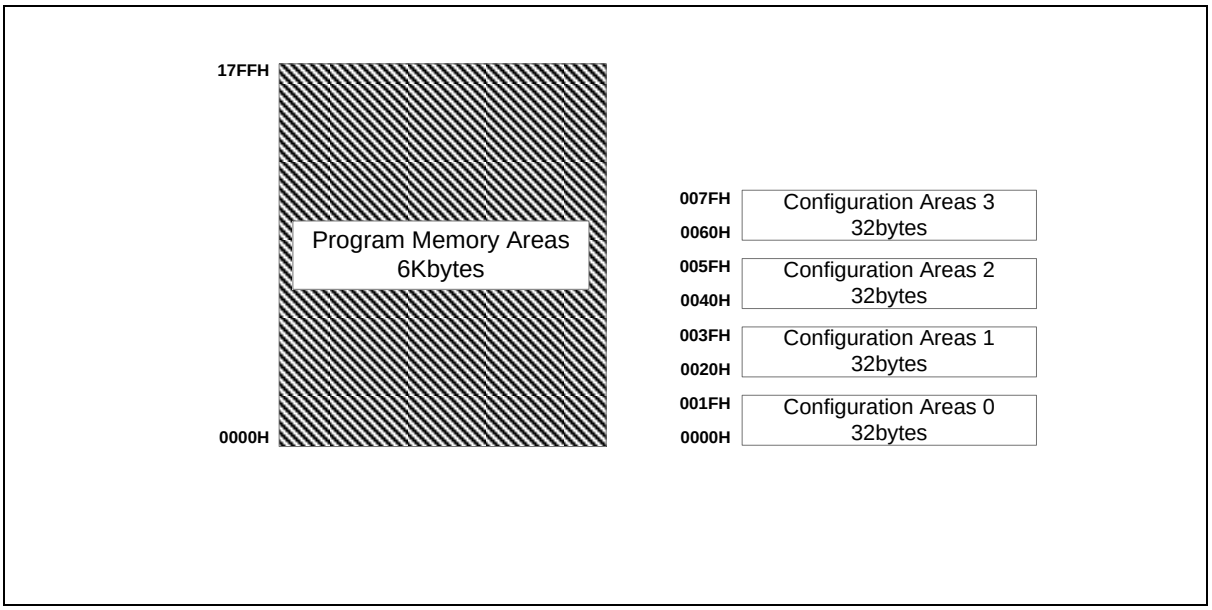


Figure 7. Program Memory

More detailed description of program memory is introduced in **chapter 14. Flash memory** later part in this document.

4.2 Internal data memory

Internal data memory is divided into three spaces as shown in figure 8. Those three spaces are generally called as,

- Lower 128 bytes
- Upper 128 bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256 bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. By means of this method, the upper 128 bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in figure 3.

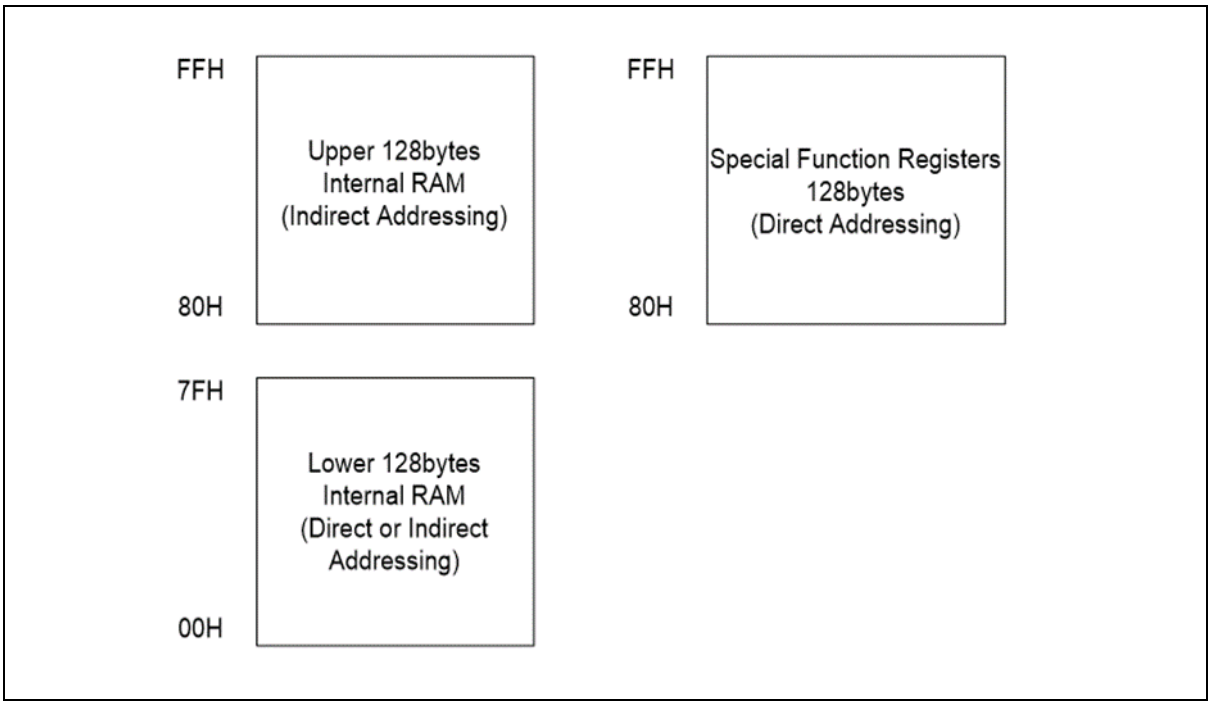


Figure 8. Internal Data Memory Map

The lower 128 bytes of RAM are present in all 8051 devices as mapped in figure 8. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128 bytes can be accessed by either direct or indirect addressing, while the upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

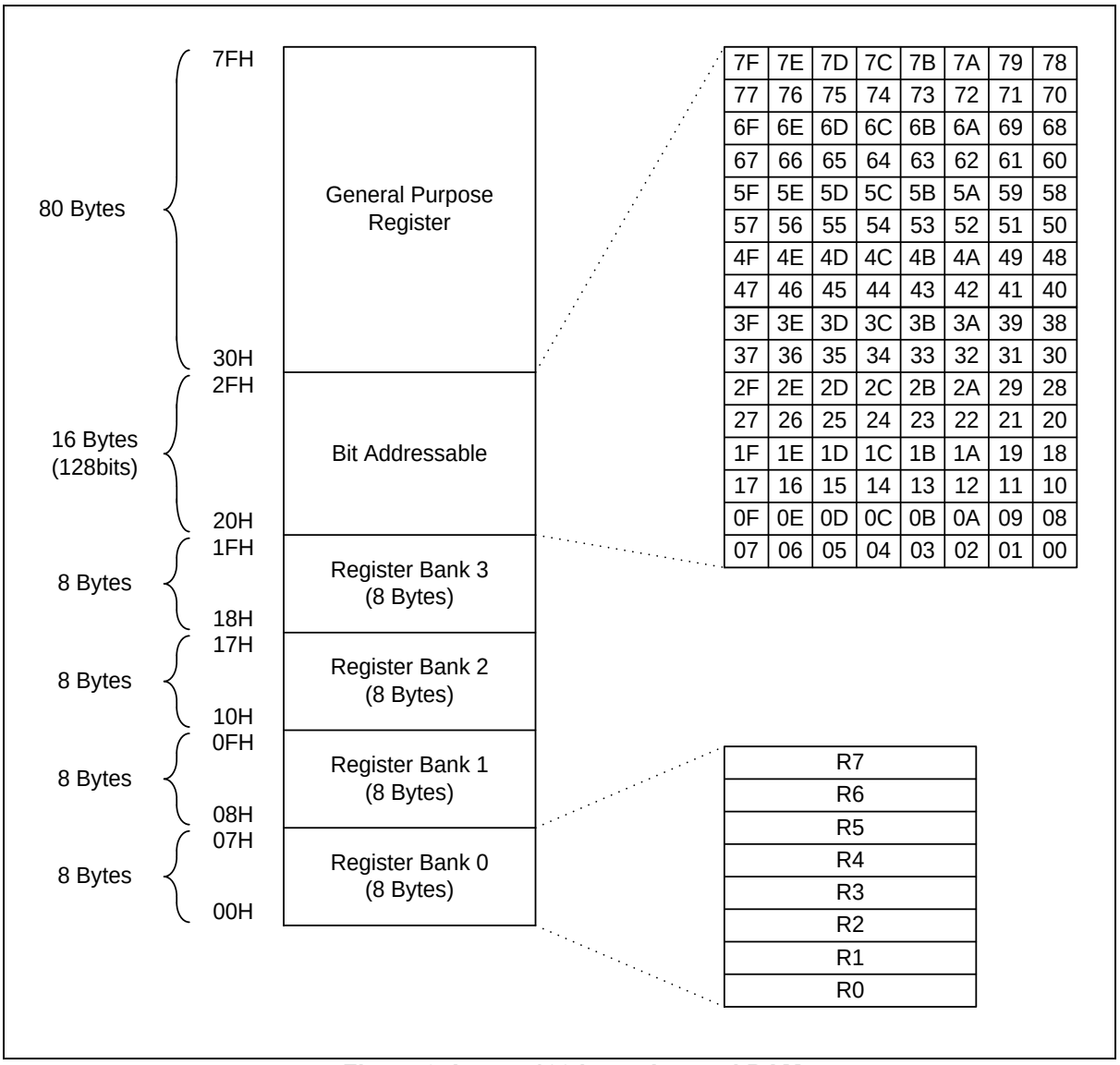


Figure 9. Lower 128 bytes Internal RAM

4.3 Extended SFR area

Extended SFR area has no relation with RAM nor FLASH. This area can be read or written to by using SFR in 8-bit unit but XSFR is not used in MC96F1206.

4.4 SFR map

In this section, information of SFR map and map summaries are introduced through tables 3 to 6.

4.4.1 SFR map summary

Table 4. SFR Map Summary

– Reserved M8051 compatible

	00H/8H[NOTE]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1							
0F0H	B		FEARL	FEARM	FEARH			
0E8H			FEMR	FECR	FESR	FETCR		
0E0H	ACC	P2PU						
0D8H		P1PU	PSR0		PSR2	PSR3	PSRPWM	
0D0H	PSW	P0PU						
0C8H								
0C0H		P2OD						
0B8H	IP	P1OD	T1CR	T1CR1	PWM1DRL C1R1L / T1L	PWM1DRH CDR1H / T1H	PWM1PRL T1DRL	PWM1PRH T1DRH
0B0H		P0OD	T0CR	T0CR1	PWM0DRL CDR0L / T0L	PWM0DRH CDR0H / T0H	PWM0PRL T0DRL	PWM0PRH T0DRH
0A8H	IE	IE1						
0A0H		LDOCR	EO	EIENAB	EIFLAG	EIEDGE	EIPOLA	EIBOTH
98H		P2IO						PCI1
90H	P2	P1IO			ADCM1	ADCM	ADCRL	ADCRH
88H	P1	P0IO	SCCR	BCCR	BITR	WDTMR	WDTR /WDTCR	LVIR
80H	P0	SP	DPL	DPH	DPL1	DPH1	RSFR	PCON

NOTE: Registers 00H/8H are bit-addressable.

4.4.2 SFR map

Table 5. SFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reset Source Flag Register	RSFR	R/W	1	1	0	0	0	1	-	-
87H	Power Control Register	PCON	R/W	–	–	–	–	–	–	0	0
88H	P1 Data Register	P1	R/W	–	–	0	0	0	0	0	0
89H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0

8AH	System and Clock Control Register	SCCR	R/W	0	0	0	0	0	–	–	0
8BH	BIT Clock Control Register	BCCR	R/W	0	R	R	0	0	1	1	0
8CH	Basic Interval Timer Register	BITR	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Mode Register	WDTMR	R/W	0	0	0	–	–	–	–	0
8EH	Watch Dog Timer Register	WDTR	W	1	1	1	1	1	1	1	1
8EH	Watch Dog Timer Counter Register: Read Case	WDTCR	R	X	X	X	X	X	X	X	X
8FH	LVI Control Register	LVIR	R/W	-	1	-	-	-	0	0	0
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
92H	Reserved	-	R/W	-							
93H	Reserved	-	R/W	-							
94H	A/D Converter Mode Register	ADCM1	R/W	1	0	0	1	-	1	0	0
95H	A/D Converter Mode Register	ADCM	R/W	1	0	0	0	1	1	1	1
96H	A/D Converter Result Low Register	ADCRL	R	X	X	X	X	X	X	X	X
97H	A/D Converter Result High Register	ADCRH	R	X	X	X	X	X	X	X	X
98H	Reserved	–	–	–							
99H	P2 Direction Register	P2IO	R/W	–	–	–	–	–	–	0	0
9AH	Reserved	–	–	–							
9BH	Reserved	–	–	–							
9CH	Reserved	–	–	–							
9DH	Reserved	–	–	–							
9EH	Reserved	–	–	–							
9FH	Reserved	–	–	–							
A0H	Reserved	–	–	–							
A1H	Reserved	–	–	–							
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	External Interrupt Enable Register	EIENAB	R/W	–	–	–	–	–	–	0	0
A4H	External Interrupt Flag Register	EIFLAG	R/W	–	–	–	–	–	0	0	0
A5H	External Interrupt Edge Register	EIEDGE	R/W	–	–	–	–	–	–	0	0
A6H	External Interrupt Polarity Register	EIPOLA	R/W	–	–	–	–	–	–	0	0
A7H	External Interrupt Both Edge Enable Register	EIBOTH	R/W	–	–	–	–	–	–	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	–	–	0	0	–	0
AAH	Reserved	–	–	–							
ABH	Reserved	–	–	–							
ACH	Reserved	–	–	–							
ADH	Reserved	–	–	–							

AEH	Reserved	–	–	–							
AFH	Reserved	–	–	–							
B0H	Reserved	–	–	–							
B1H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
B3H	Timer 0 Control Register1	T0CR1	R/W	–	0	0	0	0	0	0	0
B4H	PWM 0 Duty Register Low, Write Case	PWM0DRL	W	0	0	0	0	0	0	0	0
B4H	Timer 0 Register Low, Read Case	T0L	R	0	0	0	0	0	0	0	0
B4H	Capture 0 Data Register Low, Read Case	CDR0L	R	0	0	0	0	0	0	0	0
B5H	PWM0 Duty Register High, Write Case	PWM0DRH	W	0	0	0	0	0	0	0	0
B5H	Timer 0 Register High, Read Case	T0H	R	0	0	0	0	0	0	0	0
B5H	Capture 0 Data High Register, Read Case	CDR0H	R	0	0	0	0	0	0	0	0
B6H	PWM 0 Period Register Low, Write Case	PWM0PRL	W	0	0	0	0	0	0	0	0
B6H	Timer 0 Data Register Low, Write Case	T0DRL	W	0	0	0	0	0	0	0	0
B7H	PWM 0 Period Register Low, Write Case	PWM0PRH	W	0	0	0	0	0	0	0	0
B7H	Timer 0 Data Register High, Write Case	T0DRH	W	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
BBH	Timer 1 Control Register1	T1CR1	R/W	-	0	0	0	0	0	0	0
BCH	PWM 1 Duty Register Low, Write Case	PWM1DRL	W	0	0	0	0	0	0	0	0
BCH	Timer 1 Register Low, Read Case	T1L	R	0	0	0	0	0	0	0	0
BCH	Capture 1 Data Register Low, Read Case	CDR1L	R	0	0	0	0	0	0	0	0
BDH	PWM 1 Duty Register High, Write Case	PWM1DRH	W	0	0	0	0	0	0	0	0
BDH	Timer 0 Register High, Read Case	T1H	R	0	0	0	0	0	0	0	0
BDH	Capture 1 Data High Register, Read Case	CDR1H	R	0	0	0	0	0	0	0	0

BEH	PWM 1 Period Register Low, Write Case	PWM1PRL	W	0	0	0	0	0	0	0	0
BEH	Timer 1 Data Register Low, Write Case	T1DRL	W	0	0	0	0	0	0	0	0
BFH	PWM 1 Period Register Low, Write Case	PWM1PRH	W	0	0	0	0	0	0	0	0
BFH	Timer 1 Data Register High, Write Case	T1DRH	W	0	0	0	0	0	0	0	0
C0H	Reserved	–	–	–							
C1H		P2OD	R/W	–	–	–	–	–	–	0	0
C2H	Reserved	–	–	–							
C3H	Reserved	–	–	–							
C4H	Reserved	–	–	–							
C5H	Reserved	–	–	–							
C6H	Reserved	–	–	–							
C7H	Reserved	–	–	–							
C8H	Reserved	–	–	–							
C9H	Reserved	–	–	–							
CAH	Reserved	–	–	–							
CBH	Reserved	–	–	–							
CCH	Reserved	–	–	–							
CDH	Reserved	–	–	–							
CEH	Reserved	–	–	–							
CFH	Reserved	–	–	–							
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	Reserved	–	–	–							
D5H	Reserved	–	–	–							
D6H	Reserved	–	–	–							
D7H	Reserved	–	–	–							
D8H	Reserved	–	–	–							
D9H	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
DAH	Port Debounce selection register	PSR0	R/W	–	–	–	–	–	–	0	0
DBH	Reserved	–	–	–							
DCH	P0, P1, P2 Port Selection Register	PSR2	R/W	0	0	0	0	0	0	0	0
DDH	P1, P2 Port Selection Register	PSR3	R/W	–	0	0	0	0	0	0	0
DEH	PWM Port Selection Register	PSRPWM	R/W	–	0	0	0	–	0	0	0
DFH	Reserved	–	–	–							
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0

E1H	P2 Pull-up Resistor Selection Register	P2PU	R/W	–	–	–	–	–	–	0	0
E2H	Reserved	–	–	–							
E3H	Reserved	–	–	–							
E4H	Reserved	–	–	–							
E5H	Reserved	–	–	–							
E6H	Reserved	–	–	–							
E7H	Reserved	–	–	–							
E8H	Reserved	–	–	–							
E9H	Reserved	–	–	–							
EAH	Flash Mode Register	FEMR	R/W	0	–	0	0	0	0	0	0
EBH	Flash Control Register	FECR	R/W	0	–	0	0	0	0	0	0
ECH	Flash Status Register	FESR	R/W	R	0	–	–	0	R	R	R
EDH	Flash Time control Register	FETCR	R/W	0	0	0	0	0	0	0	0
EEH	Reserved	–	–	–							
EFH	Reserved	–	–	–							
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Reserved	–	–	–							
F2H	Flash address low Register	FEARL	W	0	0	0	0	–	–	–	–
F3H	Flash address middle Register	FEARM	W	0	0	0	0	0	0	0	0
F4H	Flash address High Register	FEARH	W	0	0	0	0	0	0	0	0
F5H	Reserved	–	–	–							
F6H	Reserved	–	–	–							
F7H	Reserved	–	–	–							
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Reserved	–	–	–							
FBH	Reserved	–	–	–							
FCH	Reserved	–	–	–							
FDH	Reserved	–	–	–							
FEH	Reserved	–	–	–							
FFH	Reserved	–	–	–							

4.4.3 8051 Compiler Compatible SFR map

ACC (Accumulator Register): E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ACC	Accumulator

B (B Register): F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

B	B Register

SP (Stack Pointer): 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 07H

SP	Stack Pointer

DPL (Data Pointer Register Low): 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL	Data Pointer Low

DPH (Data Pointer Register High): 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH	Data Pointer High

DPL1 (Data Pointer Register Low 1): 84H

7	6	5	4	3	2	1	0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL1	Data Pointer Low 1

DPH1 (Data Pointer Register High 1): 85H

7	6	5	4	3	2	1	0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH1	Data Pointer High 1

PSW (Program Status Word Register): D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

CY	Carry Flag
AC	Auxiliary Carry Flag
F0	General Purpose User-Definable Flag
RS1	Register Bank Select bit 1
RS0	Register Bank Select bit 0
OV	Overflow Flag
F1	User-Definable Flag
P	Parity Flag. Set/Cleared by hardware each instruction cycle to indicate an odd/even number of ‘1’ bits in the accumulator

EO (Extended Operation Register): A2H

7	6	5	4	3	2	1	0
–	–	–	TRAP_EN	–	DPSEL2	DPSEL1	DPSEL0
–	–	–	R/W	–	R/W	R/W	R/W

Initial value: 00H

TRAP_EN Select the Instruction **(Keep always ‘0’)**.
- 0 Select MOVC @(DPTR++), A
- 1 Select Software TRAP Instruction

DPSEL[2:0] Select Banked Data Pointer Register

DPSEL2	DPSEL1	SPSEL0	Description
0	0	0	DPTR0
0	0	1	DPTR1
Reserved			

5 I/O Ports

MC96F1206 has two groups of I/O ports, P0, P1 and P2. Each port can be easily configured as an input pin, an output, or an internal pull up and open-drain pin by software. The port configuration pursues to meet various system configurations and design requirements. P0, P1 and P2 have a function generating interrupts in accordance with a change of state of the pin.

5.1 Port P0

5.1.1 Port description of P0

As an 8-bit I/O port, P0 controls the following registers:

- P0 data register (P0)
- P0 direction register (P0IO)
- P0 pull-up resistor selection register (P0PU)
- P0 open-drain selection register (P0OD)

5.2 Port P1

5.2.1 Port description of P1

As a 8-bit I/O port, P1 controls the following registers:

- P1 data register (P1)
- P1 direction register (P1IO)
- P1 pull-up resistor selection register (P1PU)
- P1 open-drain selection register (P1OD)

5.3 Port P2

5.3.1 Port description of P2

As a 2-bit I/O port, P2 controls the following registers:

- P2 data register (P2)
- P2 direction register (P2IO)
- P2 pull-up resistor selection register (P2PU)
- P2 open-drain selection register (P2OD)

6 Interrupt controller

Up to 9 interrupt sources are available in the MC96F1206. Allowing software control, each interrupt source can be enabled by defining separate enable register bit associated with it. It can also have four levels of priority assigned. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources, and is not controllable by software.

The interrupt controller features the followings:

- Receives requests from 9 interrupt sources
- 6 group priority
- 4 priority levels
- Multi interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit
- Interrupt latency varies ranging from 5 to 8 machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupt enable registers (IE, IE1). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control. It must be set to '1' to enable interrupts as introduced in the followings:

- When EA is set to '0' ➔ all interrupts are disabled.
- When EA is set to '1' ➔ a particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

EA is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. MC96F1206 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of the four levels according to IP and IP1.

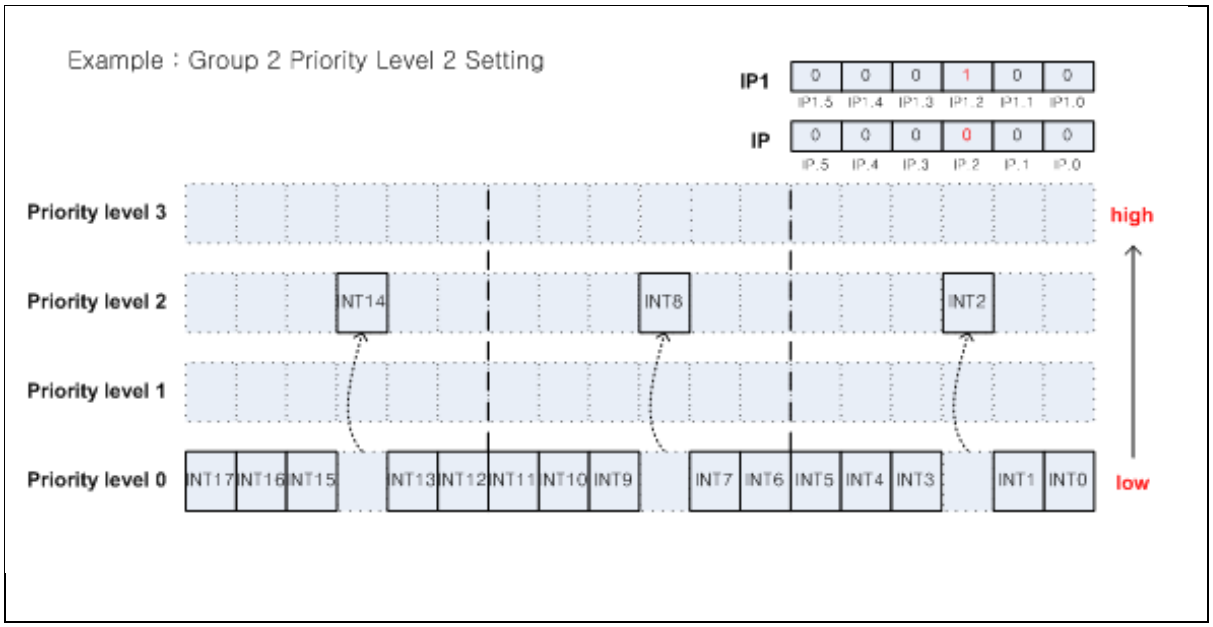


Figure 10. Interrupt Group Priority Level

Figure 10 introduces interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by 2 bits of Interrupt Priority (IP) registers: 1 bit from IP and another 1 bit from IP1.

Interrupt Service Routine serves an interrupt having higher priority first. If two requests of different priority levels are received simultaneously, the request with higher priority level is served prior to the lower one.

6.1 Interrupt controller block diagram

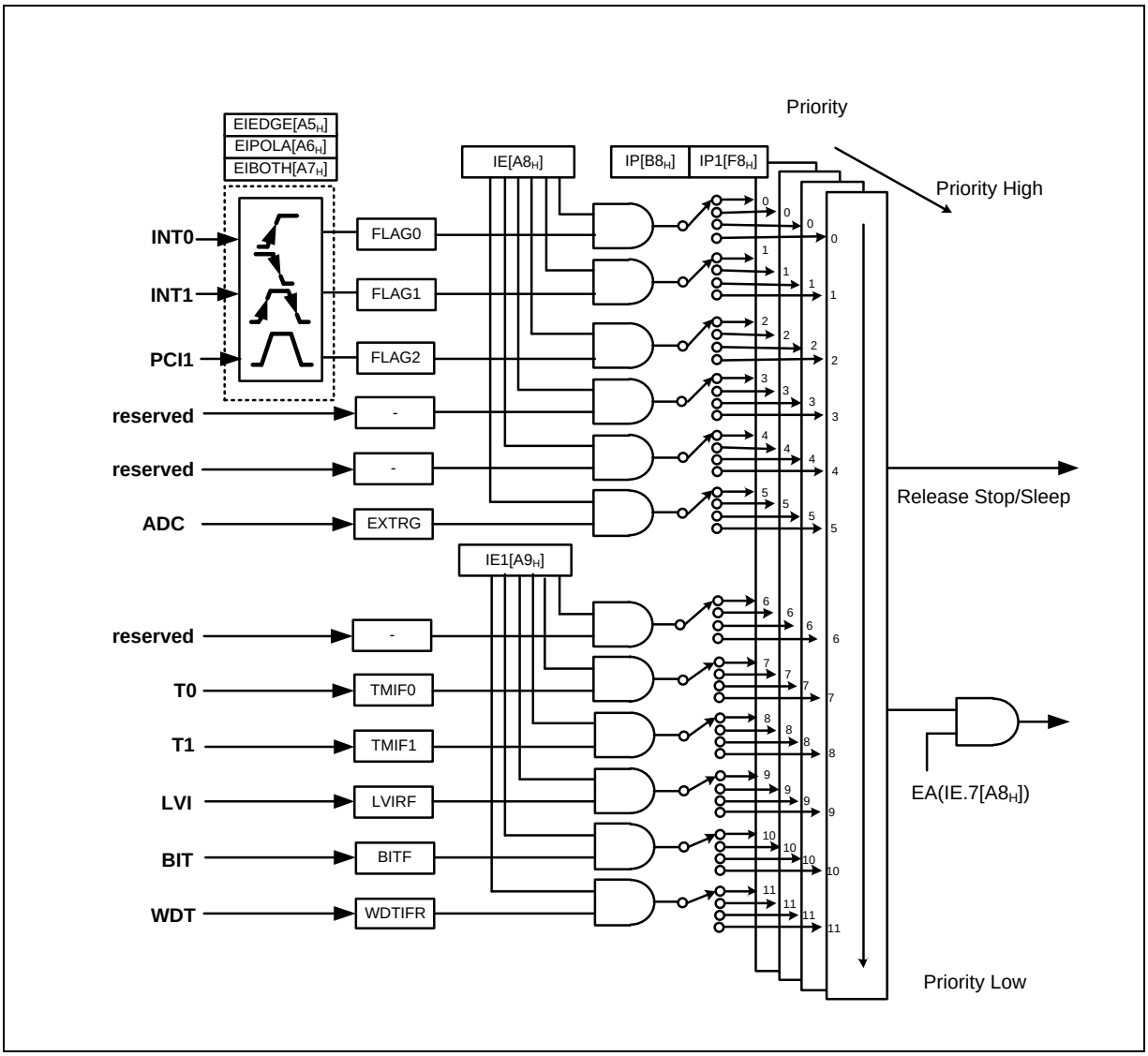


Figure 11. Interrupt Controller Block Diagram

6.2 Interrupt vector table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack, and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address.

Interrupt controller supports 9 interrupt sources and each interrupt source has a determined priority order as shown in table 6.

Table 6. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector address
Hardware Reset	RESETB	0	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
PCI	INT2	IE.2	3	Maskable	0013H
-	INT3	IE.3	4	Maskable	001BH
-	INT4	IE.4	5	Maskable	0023H
ADC	INT5	IE.5	6	Maskable	002BH
-	INT6	IE.6	7	Maskable	0033H
TIMER 0	INT7	IE1.1	8	Maskable	003BH
TIMER 1	INT8	IE1.2	9	Maskable	0043H
LVI	INT9	IE1.3	10	Maskable	004BH
BIT	INT10	IE1.4	11	Maskable	0053H
WDT	INT11	IE1.5	12	Maskable	005BH

.

7 Clock generator

The clock generator produces the basic clock pulses which provide the system clock to CPU and peripheral hardware. The internal RC-OSC is used as system clock and the default division rate is two.

- Calibrated Internal RC Oscillator (32MHz)

- . INTERNAL CLOCK(16MHz)/1 (16MHz)
- . INTERNAL CLOCK(16MHz)/2 (8MHz, Default system clock)
- . INTERNAL CLOCK(16MHz)/4 (4MHz)
- . INTERNAL CLOCK(16MHz)/16 (1MHz)

7.1 Block diagram

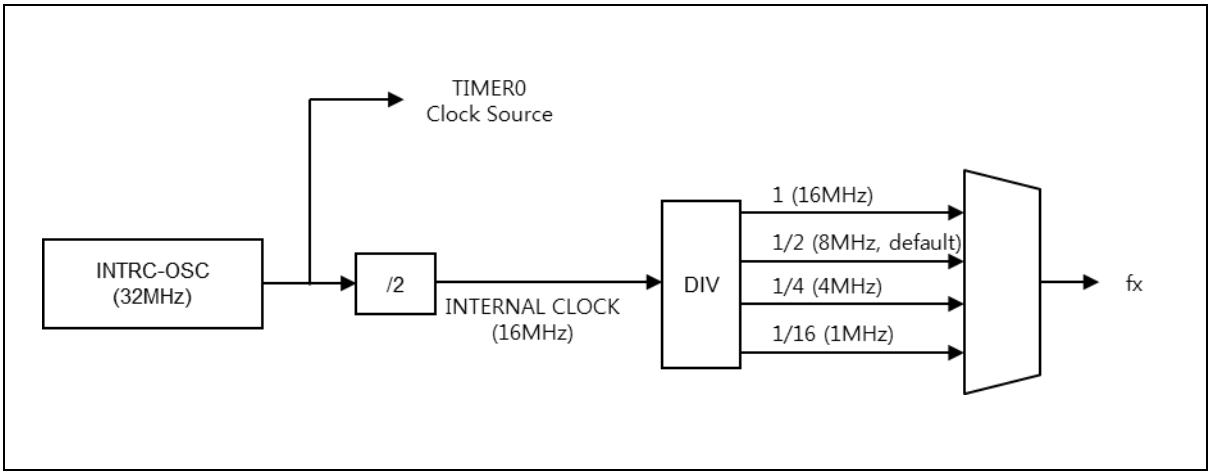


Figure 12. Clock Generator in Block Diagram

8 Basic interval timer

The MC96F1206 has one 8-bit Basic Interval Timer that is free-run and can't stop. Block diagram is shown in. In addition, the Basic Interval Timer generates the time base for watchdog timer counting. It also provides a Basic interval timer interrupt (BITF).

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As clock function, time interrupt occurrence

8.1 Block diagram

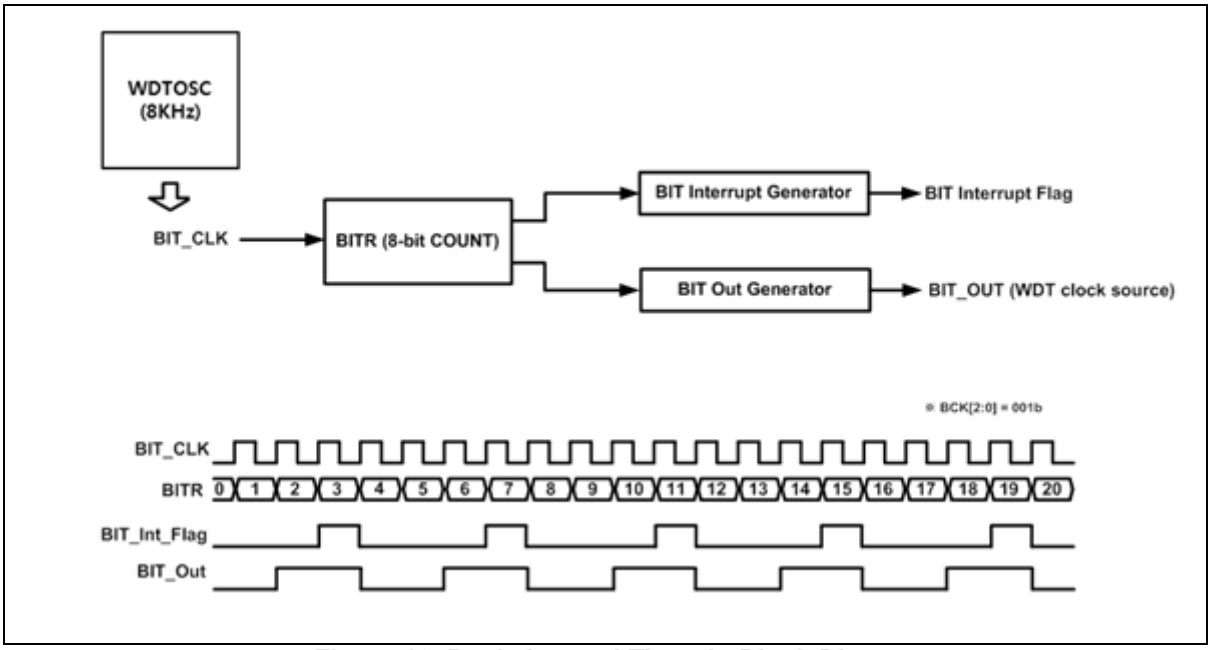


Figure 13. Basic Interval Timer in Block Diagram

9 Watchdog timer

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or the like, and resumes the CPU to the normal state. The watchdog timer signal for detecting malfunction can be selected either a reset CPU or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTMR[6] bit. If writing WDTMR[5] to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit has '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTR, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset the CPU in accordance with the bit WDTRSON.

The clock source of Watch Dog Timer is BIT overflow output. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTR set value. The equation is as below

9.1 Block diagram

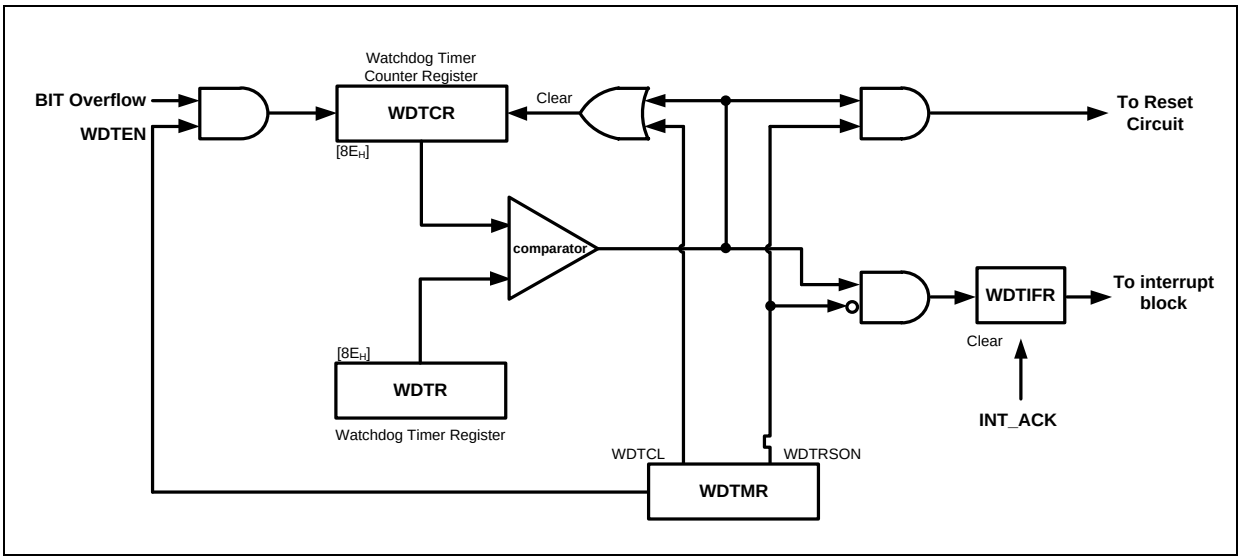


Figure 14. Watchdog Timer in Block Diagram

10 TIMER

The 16-bit timer x(0~1) consists of Multiplexer, Timer Data Register High/Low, Timer Register High/Low, Timer Mode Control Register, PWM Duty High/Low, PWM Period High/Low Register. It is able to use internal 16-bit timer/ counter without a port output function. The 16-bit timer x can be clocked by internal or external clock source (EC0, EC1). The divided clock of the main clock selected from prescaler output.

T32M in the T0CR1 register is select internal-RCOSC(32MHz) as Timer0 clock source.

10.1 16-bit timer/ counter mode

In the 16-bit Timer/Counter Mode, If the TxH + TxL value and the TxDRH + TxDRL value are matched, Tx/PWMx port outputs. The output is 50:50 of duty square wave, the frequency is following.

$$f_{COMP} = \frac{\text{Timer Clock Frequency}}{2 \times \text{Prescaler Value} \times (TxDR + 1)}$$

f_{COMP} is timer output frequency and TxDR is the 16 bits value of TxDRH and TxDRL.To export the compare output as Tx/PWMx, the Tx_PE bit in the TxCR1 register must set to '1'.The 16-bit Timer/Counter Mode is selected by control registers as shown in Figure 27. When TxH, TxL are read, TxL should be read first. Because when TxL is read TxH is captured to buffer, and when TxH is read captured value of TxH is read.

10.1 Block diagram

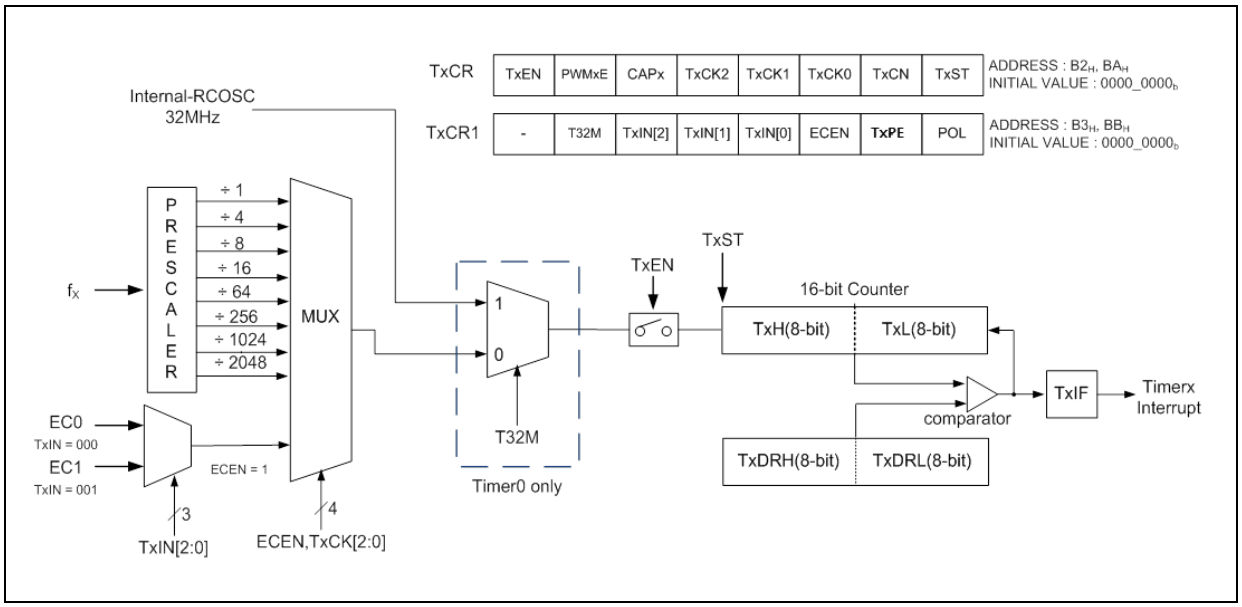


Figure 15. 16-bit Timer 0 in Block Diagram

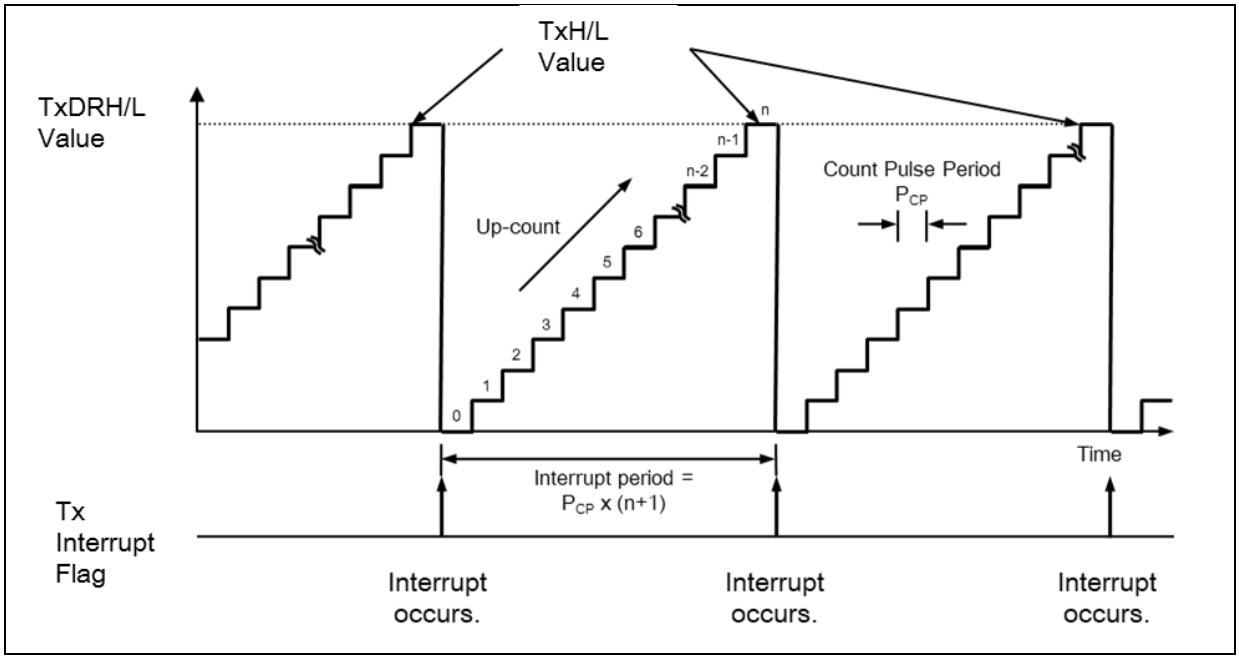


Figure 16. 16-bit Timer/ Counter 0/1 Interrupt Example

11 12-bit A/D Converter

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 12-bit digital value. The A/D module has tenth analog inputs. The output of the multiplex is the input into the converter, which generates the result via successive approximation. The A/D module has four registers which are the control register ADCM (A/D Converter Mode Register), ADCM1 (A/D Converter Mode Register 1) and A/D result register ADCHR (A/D Converter Result High Register) and ADCLR (A/D Converter Result Low Register). It is selected for the corresponding channel to be converted by setting ADSEL[3:0]. To executing A/D conversion, ADST bit sets to '1'. The register ADCHR and ADCLR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCHR and ADCLR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. For processing A/D conversion, AFLAG bit is read as '0'. If using STBY (power down) bit, the ADC is disabled. Also internal timer, external generating event, comparator, the trigger of timer1pwm and etc. can start ADC regardless of interrupt occurrence.

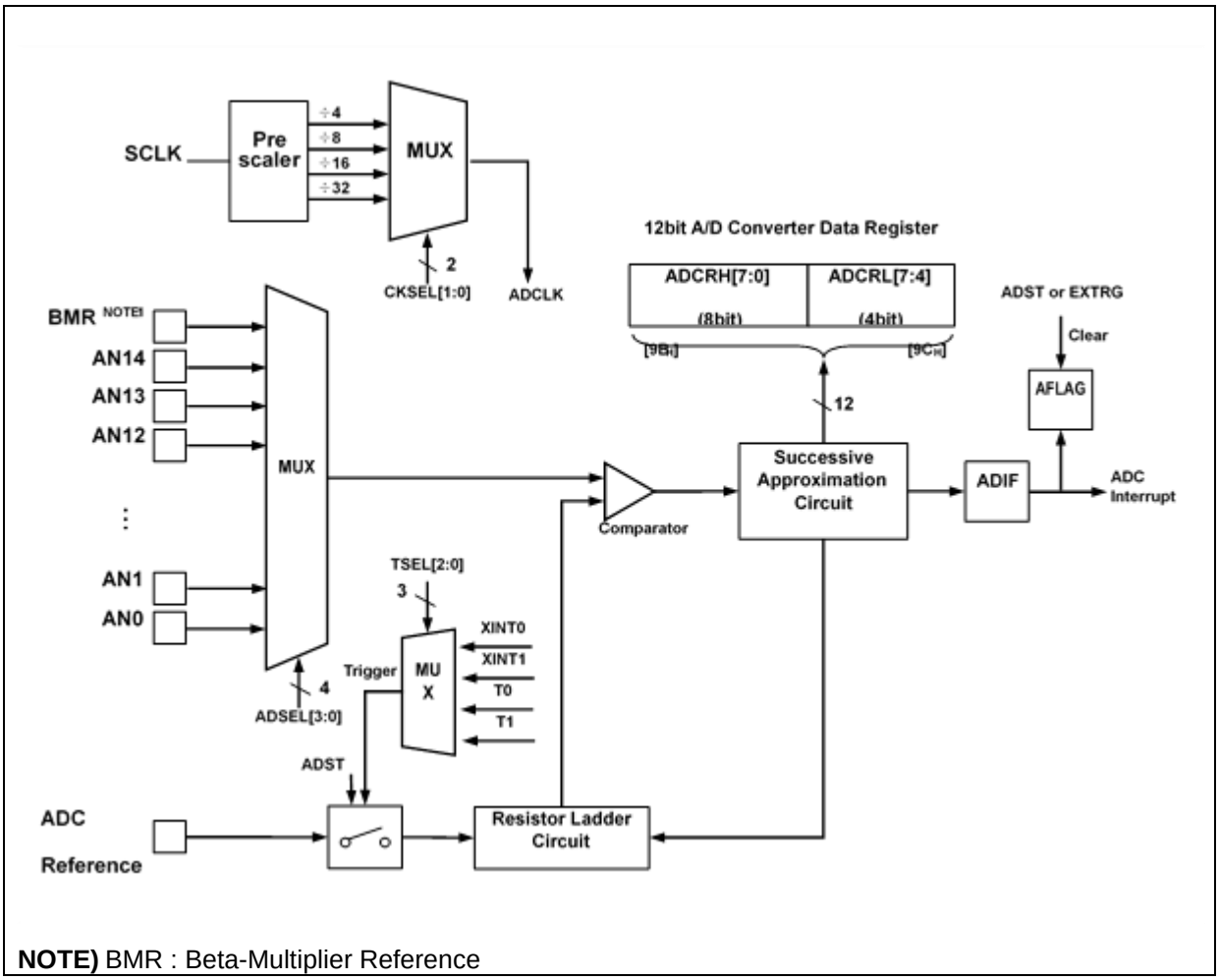
- ADC Conversion Time = ADCLK * 60 cycles

After STBY bit is reset (ADC power enable) and it is restarted, during some cycle, ADC conversion value may have an inaccurate value. When using ports as ADC input port, it is recommended to set corresponding PSR2, PSR3 registers to prevent current leakage or unexpected function, because analog value enters to digital circuit. ADC zero offset value is written to 1868h of option memory.

To read the zero offset value, refer to the assembly code below.

```
(Example)
char Zero_offset;                    // signed value
#pragma ASM
mov     A, #0                        ;
mov     DPTR, #1868h                 ; ADC Zero offset value is addressed at 0x1868
movc    A, @A+DPTR                   ; A = ADC zero offset value
#pragma ENDASM
Zero_offset = ACC;                   //
```

11.1 Block diagram



NOTE) BMR : Beta-Multiplier Reference

Figure 17. ADC Block Diagram

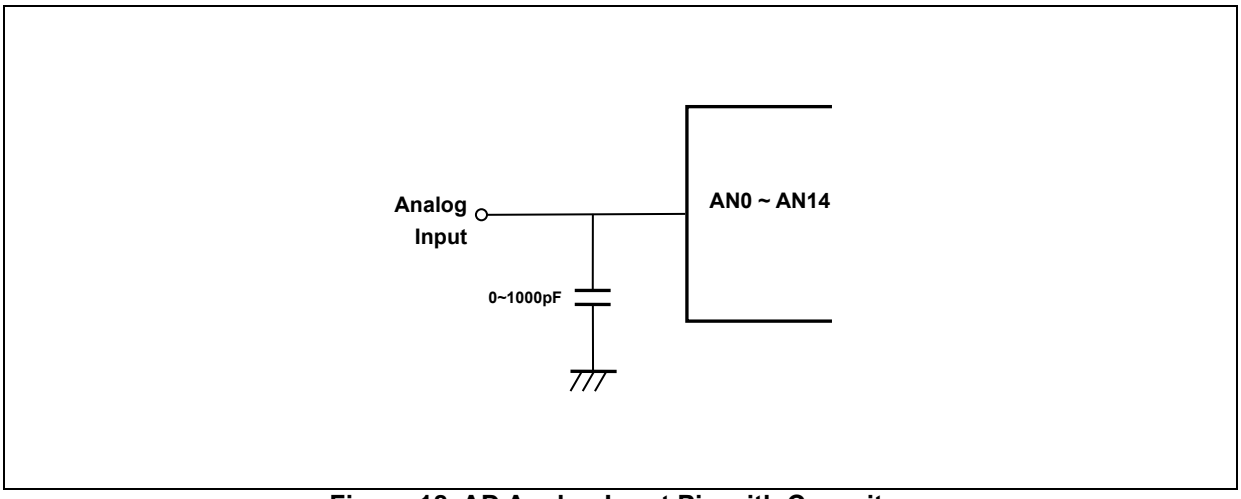


Figure 18. AD Analog Input Pin with Capacitor

12 Power down operation

The MC96F1206 has three power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, IDLE, STOP1 and STOP2 mode. In three modes, program is stopped.

12.1 Peripheral Operation in IDLE/STOP Mode

Peripheral's operations during IDLE/STOP mode is introduced in table 7.

Table 7. Peripheral Operation during Power-down Mode

Peripheral	IDLE Mode	STOP1 Mode STOP1 = '1'	STOP2 Mode STOP1 = '0'
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain	Retain
Watch Dog Timer	Operates Continuously	Operates Continuously	Stop
Timer	Operates Continuously	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)	Halted(Only when the Event Counter Mode is Enable, Timer operates Normally)
Internal OSC (32MHz)	Oscillation	Stop	Stop
Internal WDTOSC (8kHz)	Oscillation	Oscillation	Stop
I/O Port	Retain	Retain	Retain
Control Register	Retain	Retain	Retain
Address Data Bus	Retain	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, External Interrupt, WDT, LVI, TIMER(EC)	By RESET, External Interrupt, LVI, TIMER(EC)

13 Reset

The MC96F1206 has reset by external RESETB pin. The following is the hardware setting value.

Table 8. Reset Value and the Relevant On Chip Hardware

On Chip Hardware	Reset Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral clock	On
Control register	Refer to peripheral registers.
Low Voltage Indicator	Enable

The MC96F1206 has six types of reset generation procedures. The following is the reset sources.

- - External RESETB
- - Power ON RESET (POR)
- - WDT Overflow Reset (In the case of WDT_EN = '1')
- - LVR Reset
- - OCD Reset
- - LVI Reset (In the case of LVILS ≠ '000')

13.1 Reset block diagram

Figure 19 shows a reset block of MC96F1206.

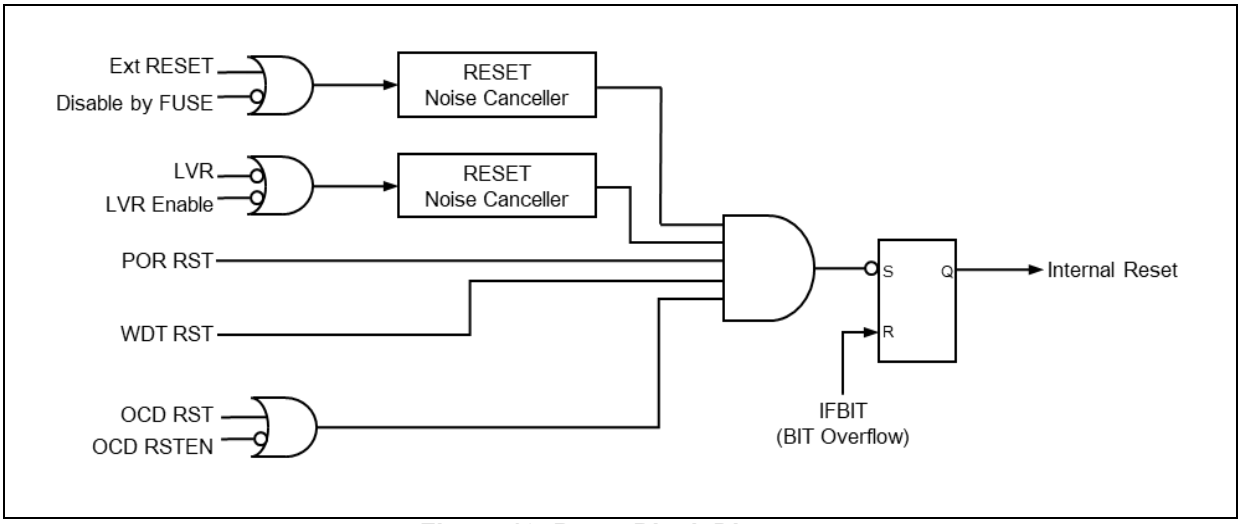


Figure 19. Reset Block Diagram

14 Flash memory

MC96F1206 incorporates flash memory inside. Program can be written, erased, and overwritten on the flash memory while it is mounted on a board. The flash memory can be read by 'MOVC' instruction and programmed in OCD, serial ISP mode or user program mode. Followings are features summary of flash memory.

- Flash Size : 6Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
-

14.1 Flash program ROM structure

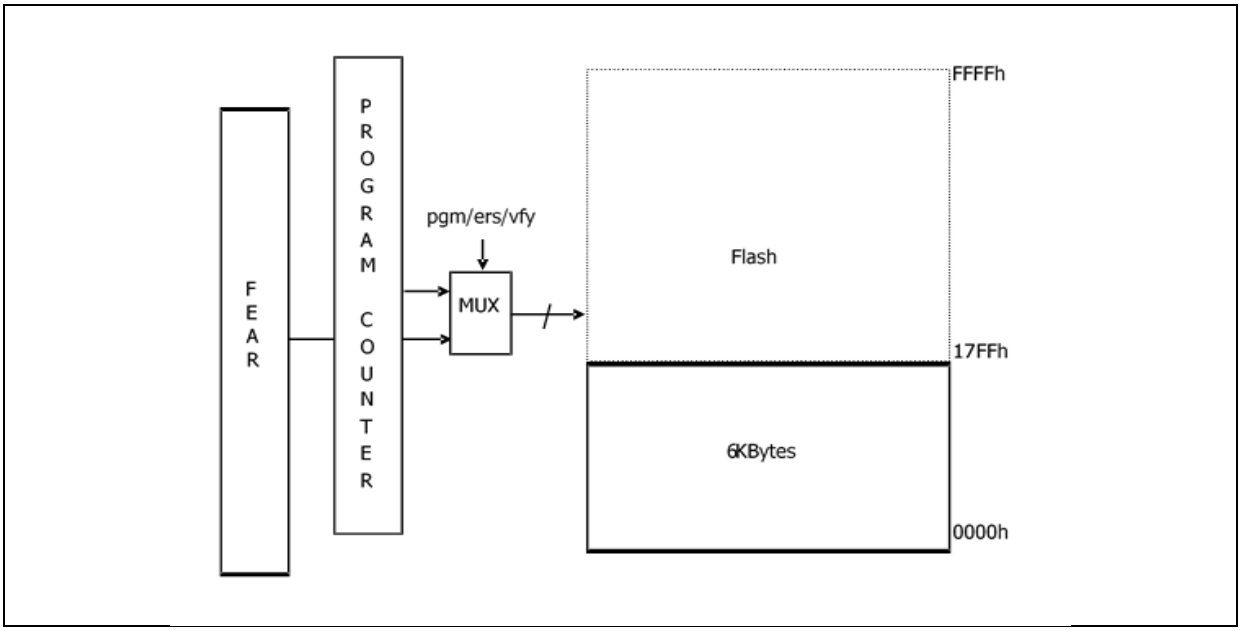


Figure 20. Flash Memory Map

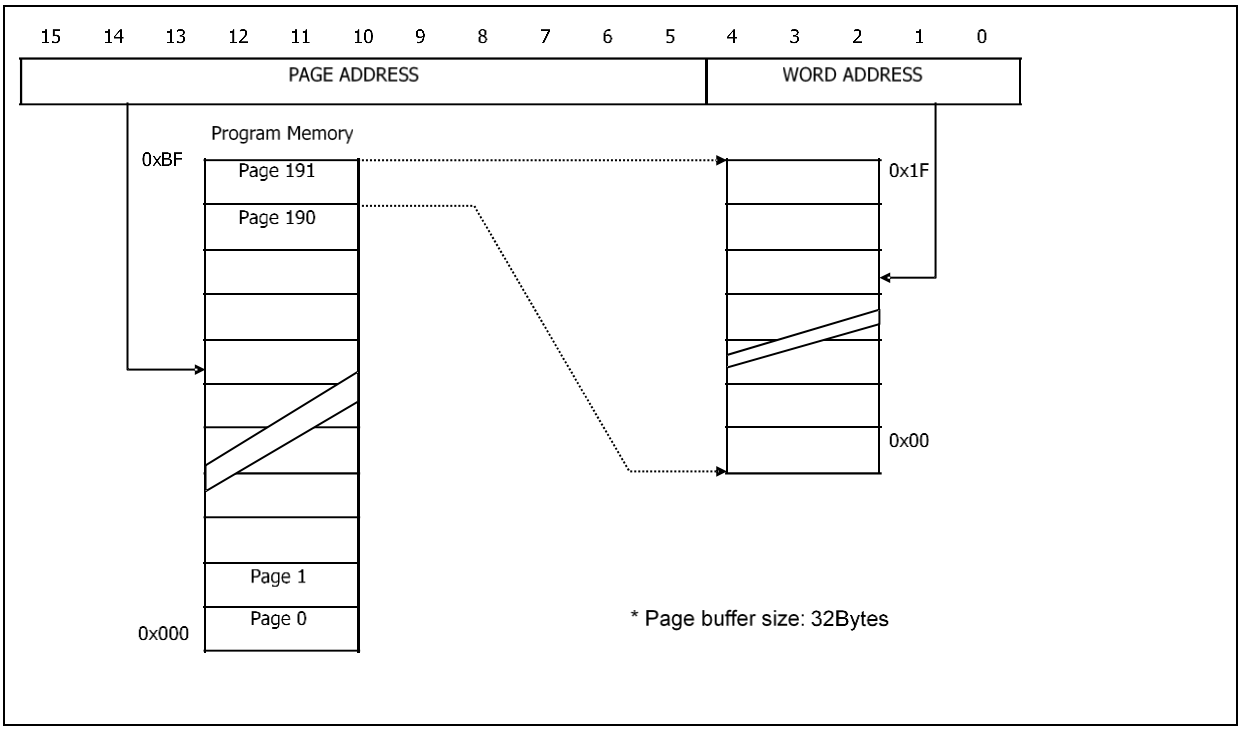


Figure 21. Address configuration of Flash memory

15 Electrical characteristics

15.1 Absolute maximum ratings

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	30	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	160	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	400	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Caution

Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

15.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Table 10. Recommended Operating Conditions

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X=1,4, 8, 16MHz	Internal RC	2.2	–	5.5	V
Operating Temperature	T_{OPR}	VDD=2.2~5.5V		-40	–	85	°C

15.3 A/D Converter Characteristics

(TA=-40℃ ~ +85℃, VDD= 2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Resolution	–	–	–-	12	–	bit
Integral Non-Linearity	INL	Analog Reference Voltage = 2.5V ~ 5.5V. fx= 8MHz	–	–	±4	LSB
Differential Non-Linearity	DNL		–	–	±1	
Zero Offset Error	ZOE		-3	–	+7	
Full Scale Error	FSE		–	–	±3	
Conversion Time	t_{CON}		–	60	–	Cycle
Analog Input Voltage	V_{AIN}	–	VSS	–	VDD	V
Analog Reference Voltage	VDDREF	NOTE	2.2	–	VDD	V
	LDOREF	–	-	2.5	-	
Analog Input Leakage Current	I_{AIN}	VDDREF=5.12V	–	–	2	uA
ADC Operating Current	I_{ADC}	Enable, VDD=5.12V	–	1	2	mA
		Disable, VDD=5.12V	–	–	0.1	uA

NOTE) When Analog Reference Voltage is lower than 2.5V, the ADC resolution is worse. ADC zero offset value (-3LSB ~ 7 LSB) is addressed at 0x1868 of option memory. (@ LDOREF)

15.4 Low Drop Out Characteristics

(T_A=-40°C ~ +85°C, VDD=2.7 ~ 5.5V, VSS=0V)

Table 11.Low Drop Out Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Current	I_{DD}	-	-	-	200	uA
Load Current	I_{LOAD}	-	-	1	-	mA
LDO Output Voltage	V_{LDO}	-40°C ~ 85°C	2.450	2.5	2.550	V
		25°C	2.475	2.5	2.525	V

15.5 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2 ~ 5.5V, VSS=0V)

Table 12.Power-On Reset Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	0.9	1.1	1.3	V
VDD Voltage Rising Time	t_R	0V to 2.0V	0.05	–	5	V/ms
POR Current	I_{POR}	–	–	0.1	–	uA

15.6 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=5.0V, VSS=0V)

Table 13.LVR and LVI Characteristics

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.80V		–	1.80	1.95	V
				1.6	2.1	2.6	
				2.0	2.5	3.0	
				3.0	3.5	4.0	
Hysteresis	△V	–		–	50	-	mV
Minimum Pulse Width	t_{LW}	–		-	500	–	us
LVR and LVI Current	IBL	LVR 1.80V	VDD=5V	–	1	-	uA
		LVR/LVI except 1.80V		–	-	50	

NOTE) LVR 1.80V is always ON.

15.7 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Table 14.Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.2 ~ 5.5V		–	32	–	MHz
Tolerance	–	T_A = 25°C	With 0.1uF Bypass capacitor	–	–	±2.0	%
		T_A = -40°C to +85°C		–	–	±5.0	
Stabilization Time	T_{HFS}	–		–	1	-	ms
IRC Current	I_{IRC}	Enable		–	0.4	–	mA
		Disable		–	–	0.1	uA

NOTE) 0.1uF bypass capacitor should be connected to VDD and VSS.

15.8 Internal WDT Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Table 15.Internal WDT Oscillator Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	4	8	12	kHz
Stabilization Time	t_{WDTS}	–	–	1	-	ms
WDTRC Current	I_{WDTRC}	Enable	–	5	–	uA
		Disable	–	–	0.1	

15.9 DC Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V, f_X=8.0MHz)

Table 16.DC Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
	V_{IH1}	P0, P1, P2	0.8VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1, P2	–	–	0.2VDD	V
Output High Voltage	V_{OH1}	VDD=3.3V, I_{OH}=-5mA, All output ports	VDD-1.5	–	–	V
	V_{OH2}	VDD=5V, I_{OH}=-10mA, All output ports	VDD-1.5	–	–	V
Output Low Voltage	V_{OL}	I_{OL}= 20mA,All output ports	–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports	-1	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	1	uA
Pull-Up Resistor	R_{PU1}	V_I=0V, T_A= 25°C All Input ports	25	50	100	kΩ
Supply Current	I_{DD1} (RUN)	Run Mode, f_X=8 MHz	-	3	5	mA
	I_{IDD2} (IDLE)	IDLE Mode, f_X=8 MHz	-	2	5	mA
	I_{DD3} (STOP1)	STOP1 Mode, WDTRC Enable	-	2	35	uA
	I_{DD4} (STOP2)	STOP2 Mode, WDTRC Disable	-	1.5	30	uA

NOTE) STOP1: WDT only running, STOP2: All function disable.

15.10 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Table 17.AC Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD=5V	-	500	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD=5V	125	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD=5V (n=0, 1)	125	–	–	ns
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD=5V (n=0, 1)	-	–	20	ns

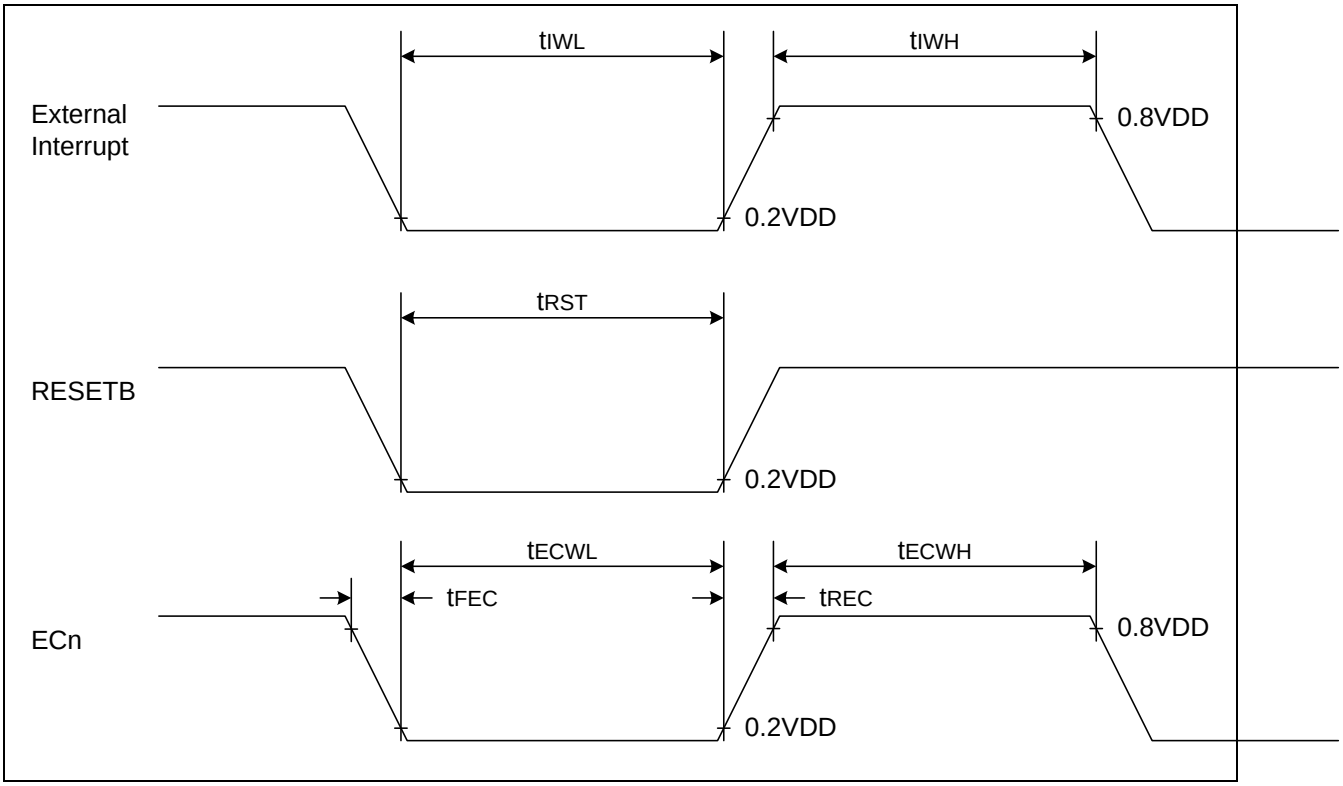


Figure 22. AC Timing

15.11 Operating Voltage Range

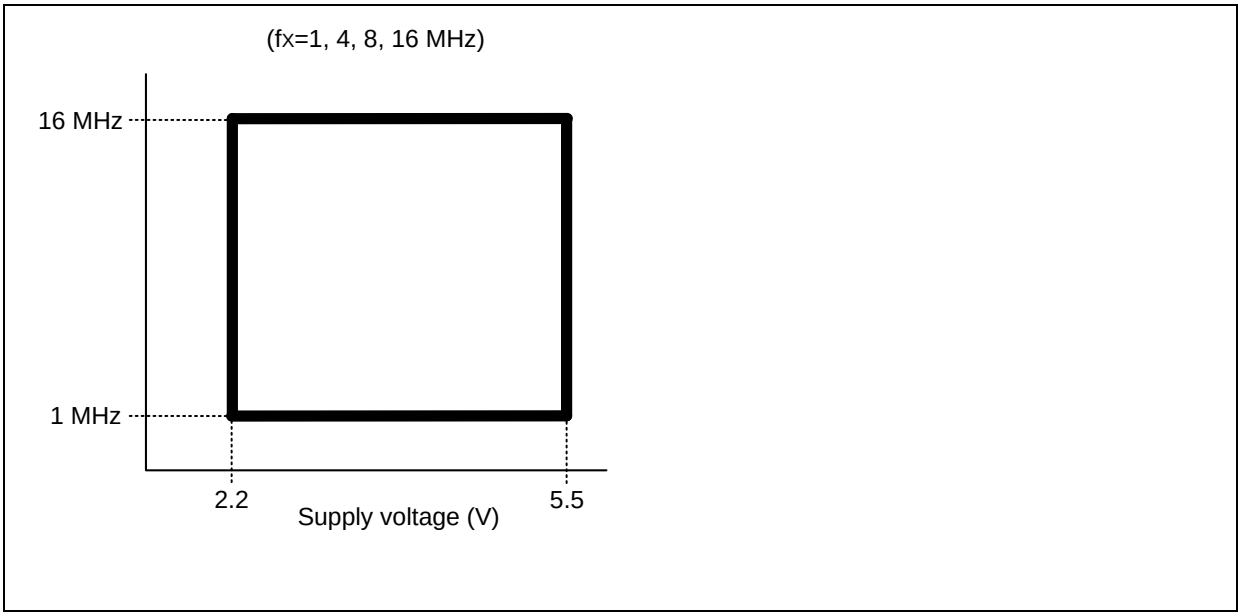


Figure 23.Operating Voltage Range

15.12 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

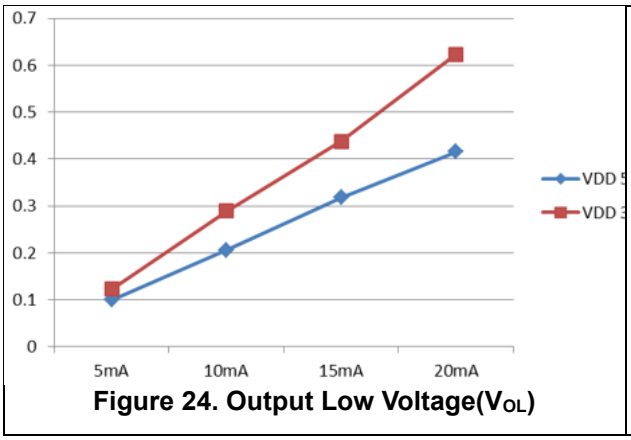


Figure 24. Output Low Voltage(V_{OL})

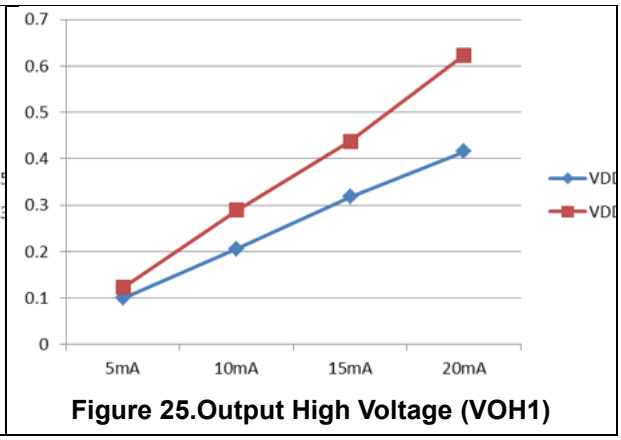


Figure 25.Output High Voltage (VOH1)

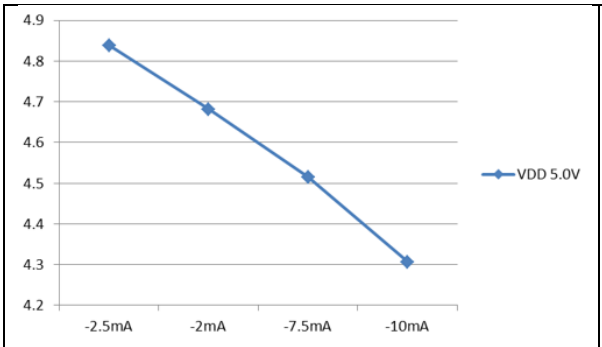


Figure 26.Output High Voltage (VOH2)

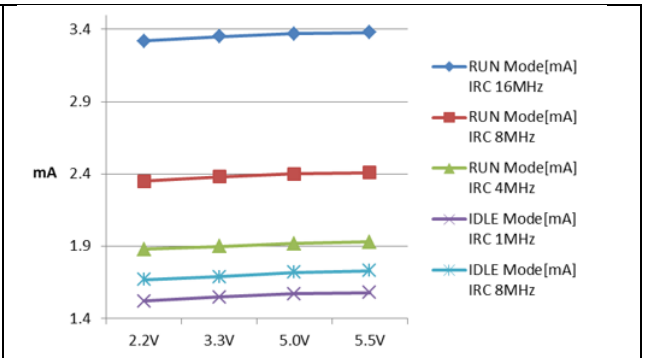


Figure 27.Power Supply Current (RUN, IDLE)

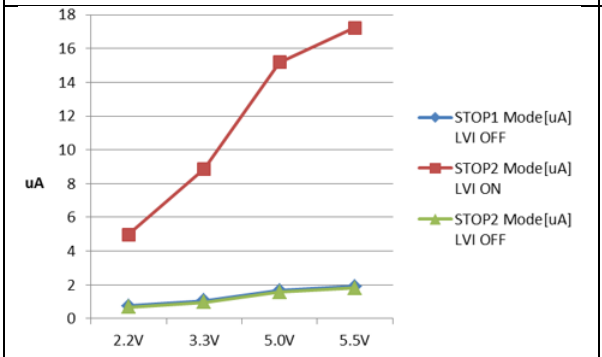


Figure 28.Power Supply Current (STOP1, STOP2)

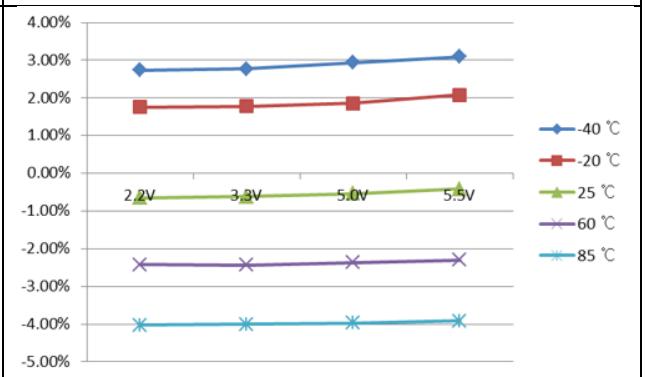


Figure 29.IRC Tolerance

15.13 Recommended Application Circuit

For the microprocessor and other devices in the system to function correctly, it is also necessary to monitor the supply voltage during operations. Voltage drops or glitches on the power supply lines, can cause unwanted changes in the internal registers, which can lead to instructions being incorrectly executed, incorrect output signals and errors in the operations results. If noise is applied to the VDD rising slope due to external factors during the POR, the microprocessor may malfunction because the microprocessor continues to operate and does not recognize that the voltage has fallen below the threshold due to the internal RC time constants. Therefore, VDD / GND requires a power capacitor for VDD drop and a decoupling capacitor for high frequency noise. Normally, electrolytic / tantalum capacitors of 10uf / 9V or more are recommended for power capacitors and multilayer ceramic capacitors of 0.1uF or more are recommended for decoupling capacitors. Decoupling capacitors should be placed as close as possible to the microprocessor.

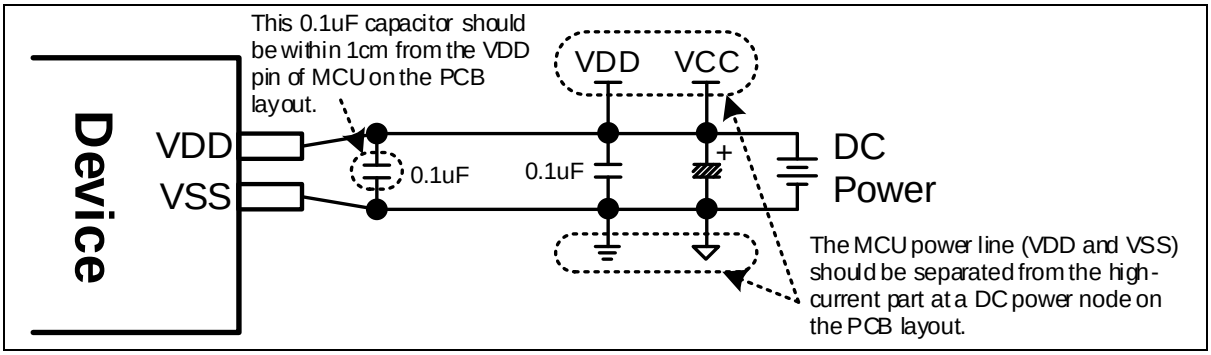


Figure 30. Recommended Power Circuit part when using DC Power.

16 Development tools

This chapter introduces wide range of development tools for MC96F1206. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

16.1 Compiler

ABOV semiconductor does not provide any compiler for MC96F1206. However, since MC96F1206 has Mentor 8051 as its CPU core, you can use all kinds of third party's standard 8051 compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Please visit our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

16.2 OCD (On-Chip Debugger) emulator and debugger

The OCD emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the OCD is provided in section **23.5 Circuit design guide** later part in this chapter. More detailed information about the OCD, please visit our website www.abovsemi.com and download the debugger S/W and documents.

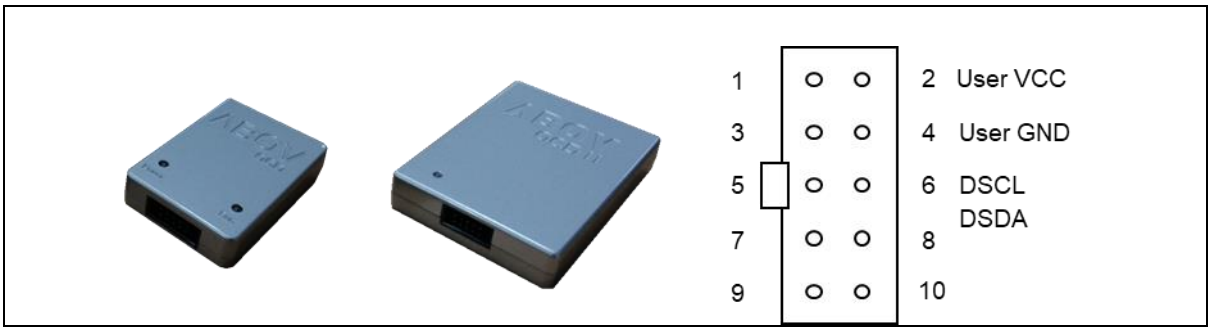


Figure 31. OCD and Pin Descriptions

Following is the OCD mode connections:

- DSCL (MC96F1206 P12 port)
- DSDA (MC96F1206 P13 port)

16.3 Programmer

E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32-bit MCU @ 72MHz
- Buffer memory : 1MB

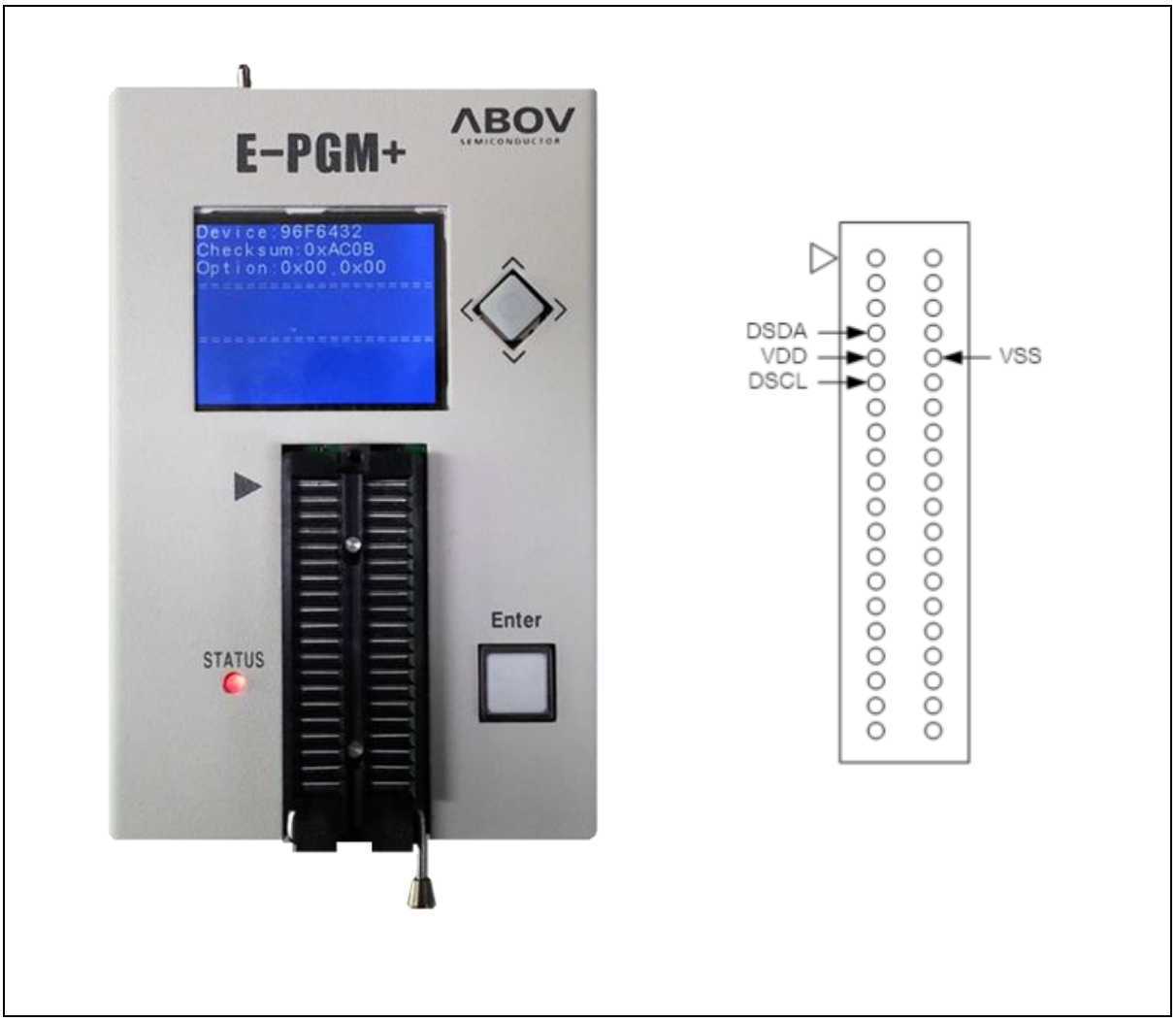


Figure 32. E-PGM+ (Single Writer) and Pin Descriptions

OCD emulator

OCD emulator allows a user to write code on the device too, since OCD debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Table 18. Specification of E-Gang4 and E-Gang6

Gang programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x35mm	148.2 x 22.5 x35mm
Weight	2.0kg	2.8kg
Input voltage	DC Adaptor 15V/2A	DC Adaptor 15V/2A
Operating temperature	-10 ~ 40℃	-10 ~ 40℃
Storage temperature	-30 ~ 80℃	-30 ~ 80℃
Water proof	No	No

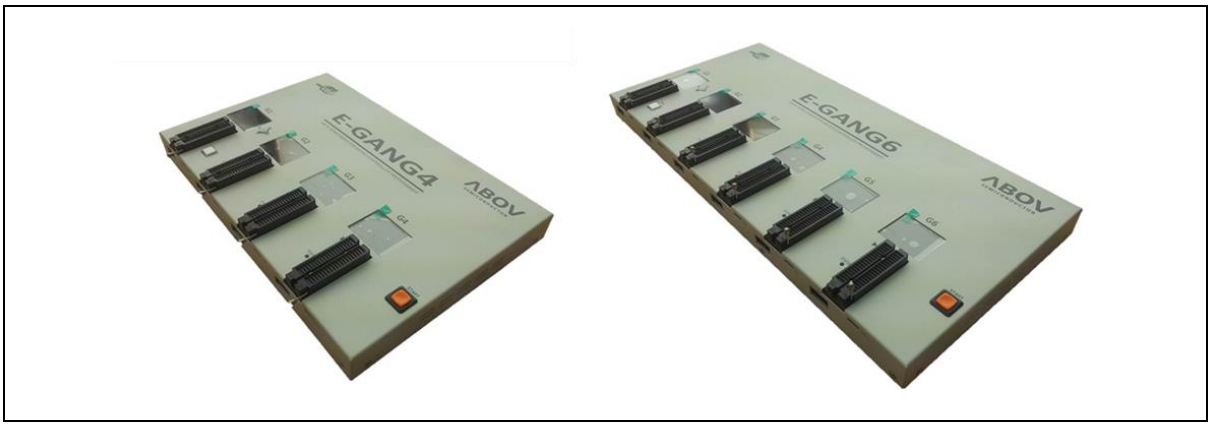


Figure 33. E-Gang4 and E-Gang6 (for Mass Production)

16.4 MTP programming

Program memory of MC96F1206 is an MTP Type. This flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. Table 31 introduces each pin and corresponding I/O status.

Table 19. Pins for MTP Programming

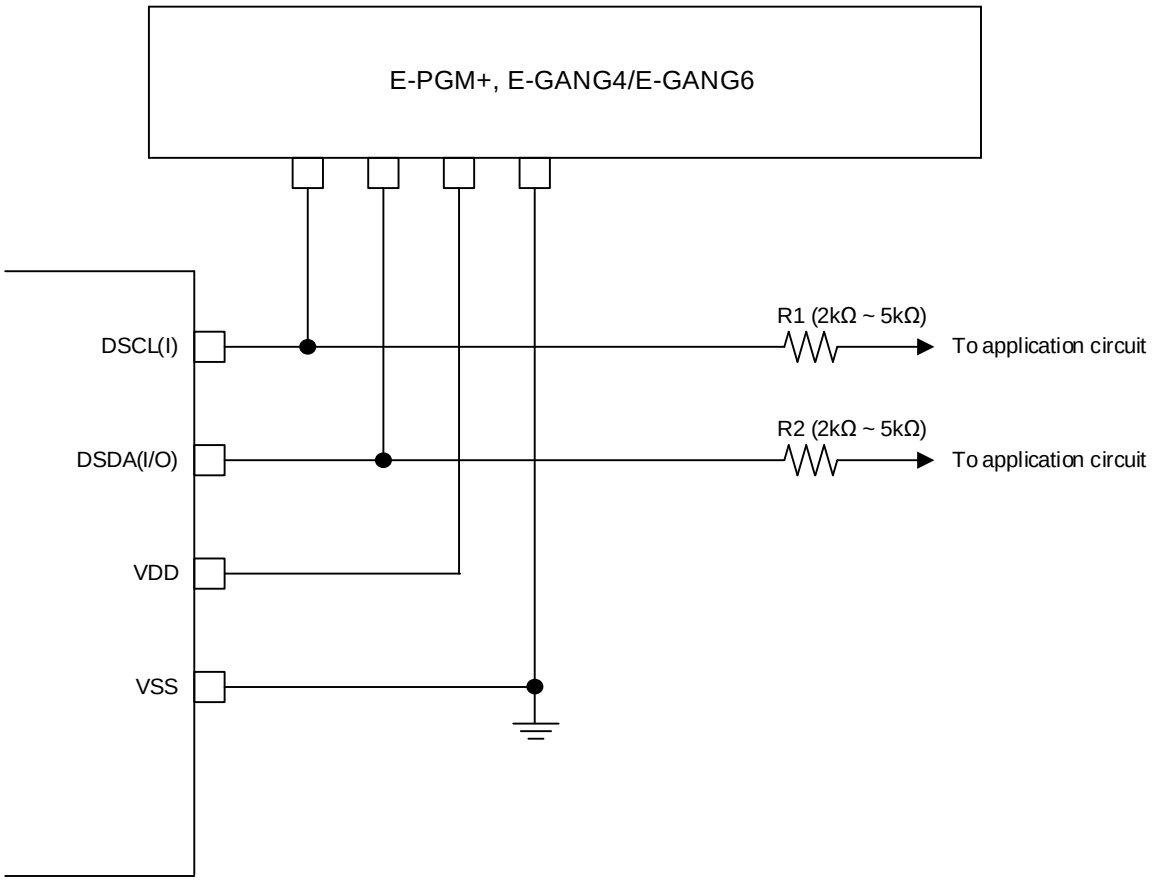
Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P12	I	Serial clock pin. Input only pin.
DSDA	P13	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

On-board programming

The MC96F1206 needs only four signal lines including VDD and VSS pins for programming flash with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

16.5 Circuit design guide

When programming flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. When you design a PCB circuit, you should consider the usage of these 4 signal lines for the on-board programming.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 34. PCB Design Guide for On-Board Programming

16.5.1 On-Chip Debug system

Detail descriptions for programming via the OCD interface can be found in the following figures. Table 32 introduces features of OCD and figure 45 shows a block diagram of the OCD interface and the On-chip Debug system.

Table 20. Features of OCD

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

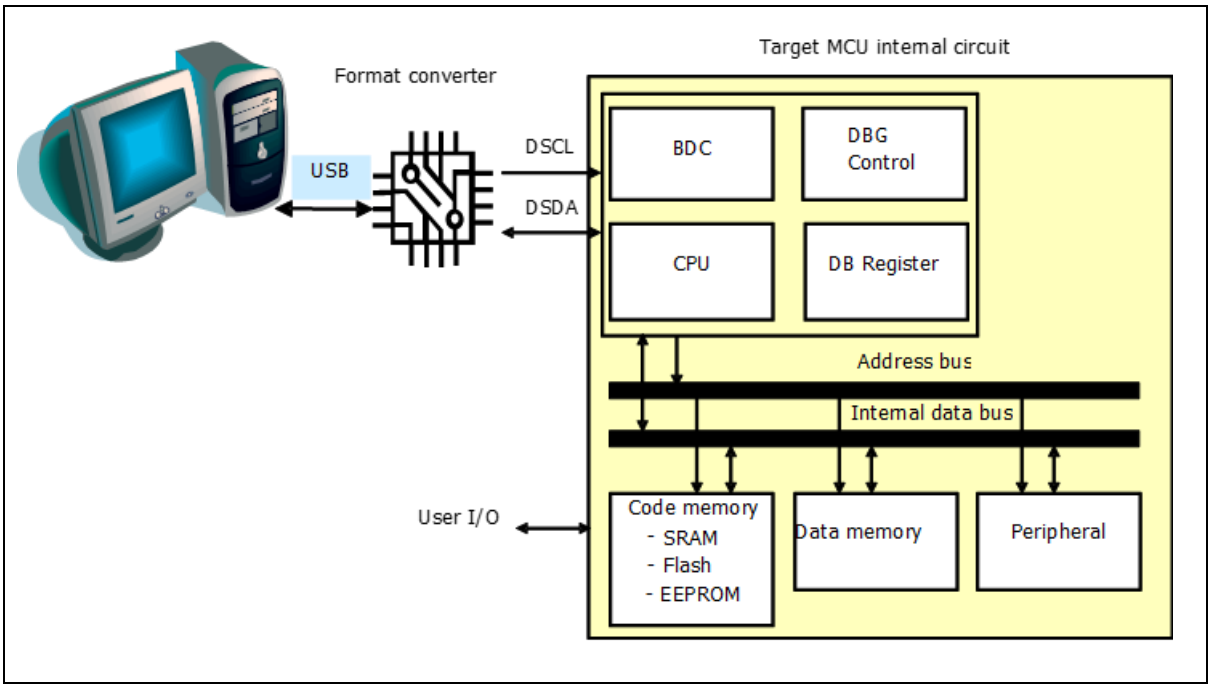


Figure 35. On-Chip Debugging System in Block Diagram

16.5.2 Two-pin external interface

Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

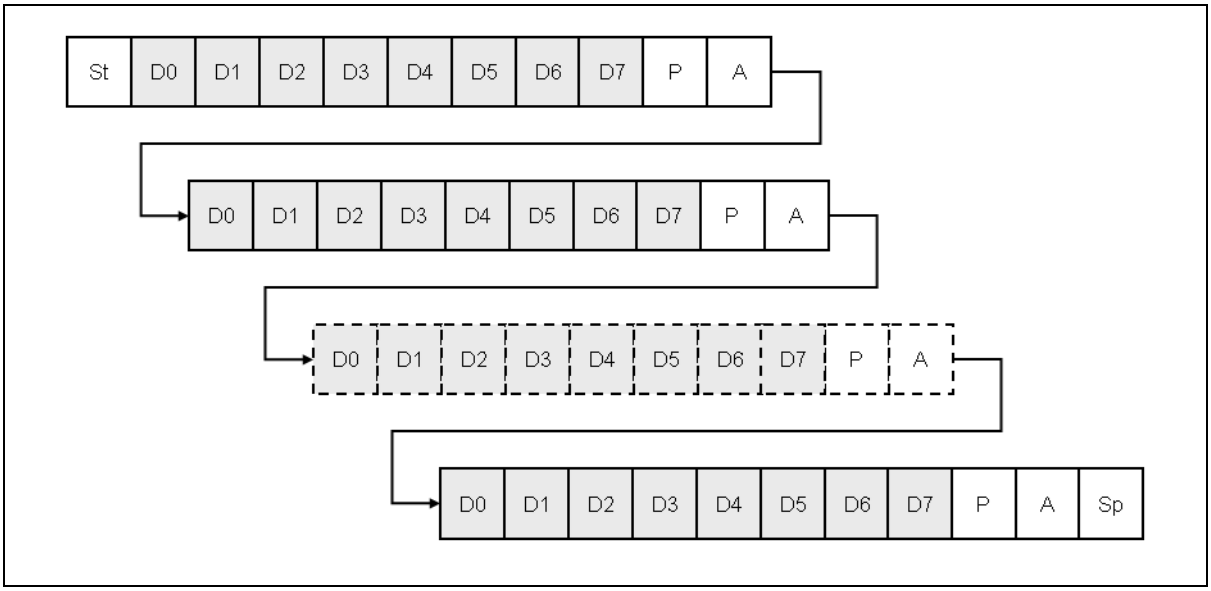


Figure 36. 10-bit Transmission Packet

Packet transmission timing

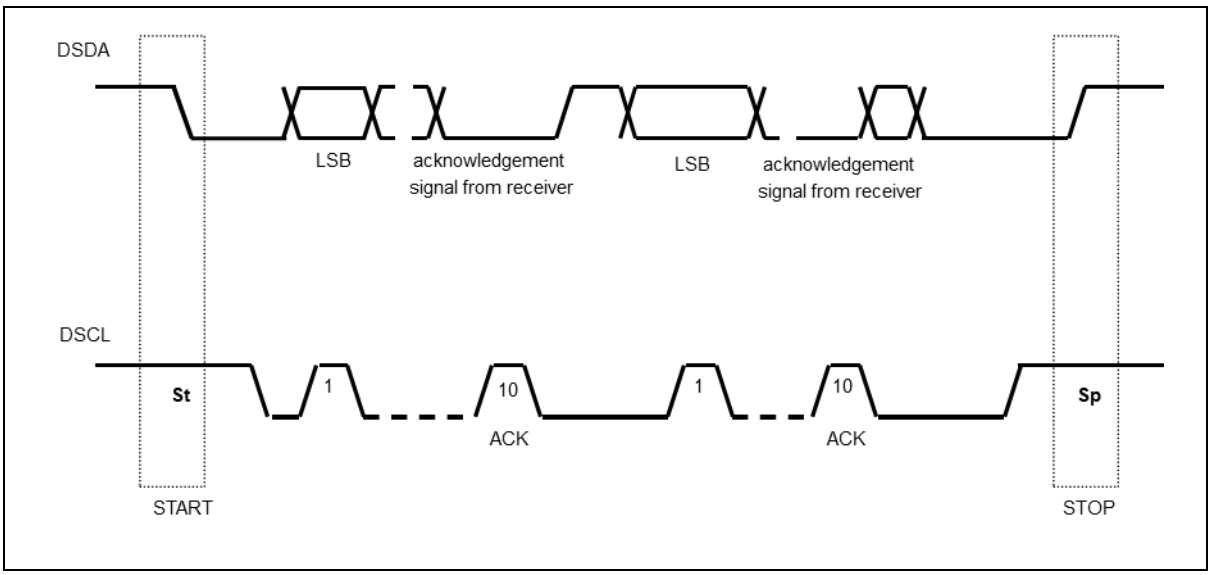


Figure 37. Data Transfer on Twin Bus

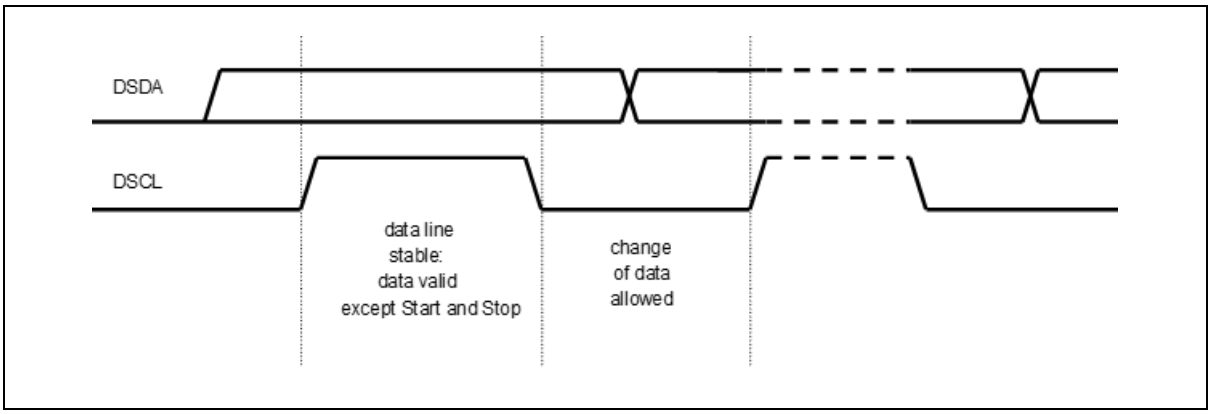


Figure 38. Bit Transfer on Serial Bus

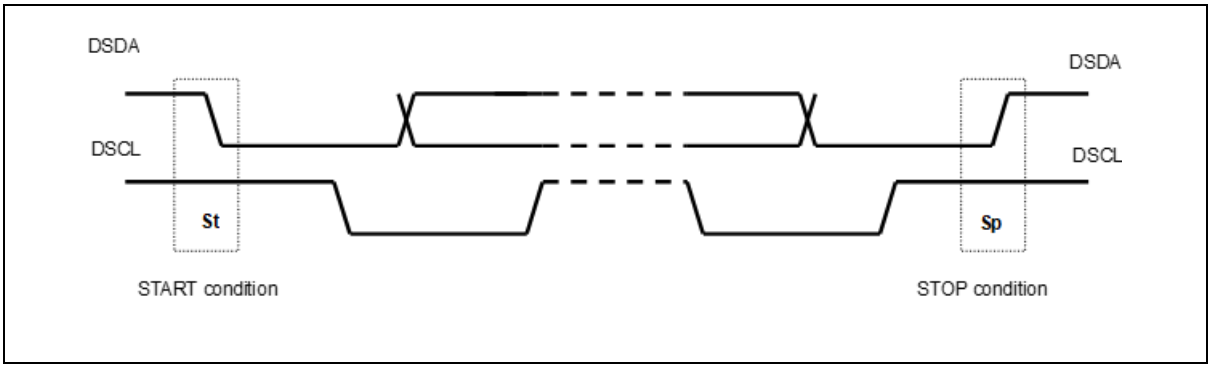


Figure 39. Start and Stop Condition

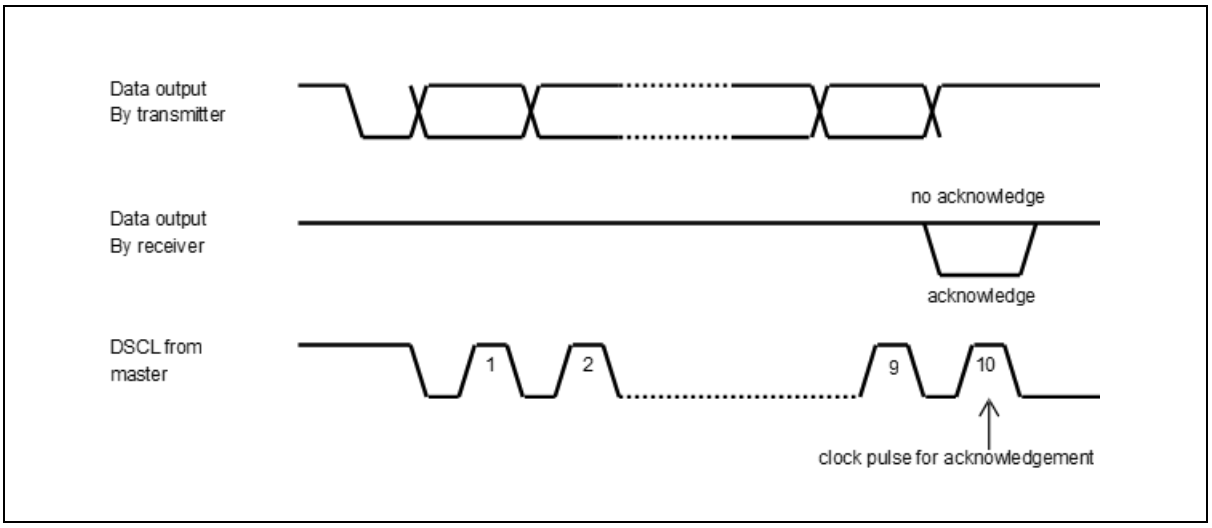


Figure 40. Acknowledge on Serial Bus

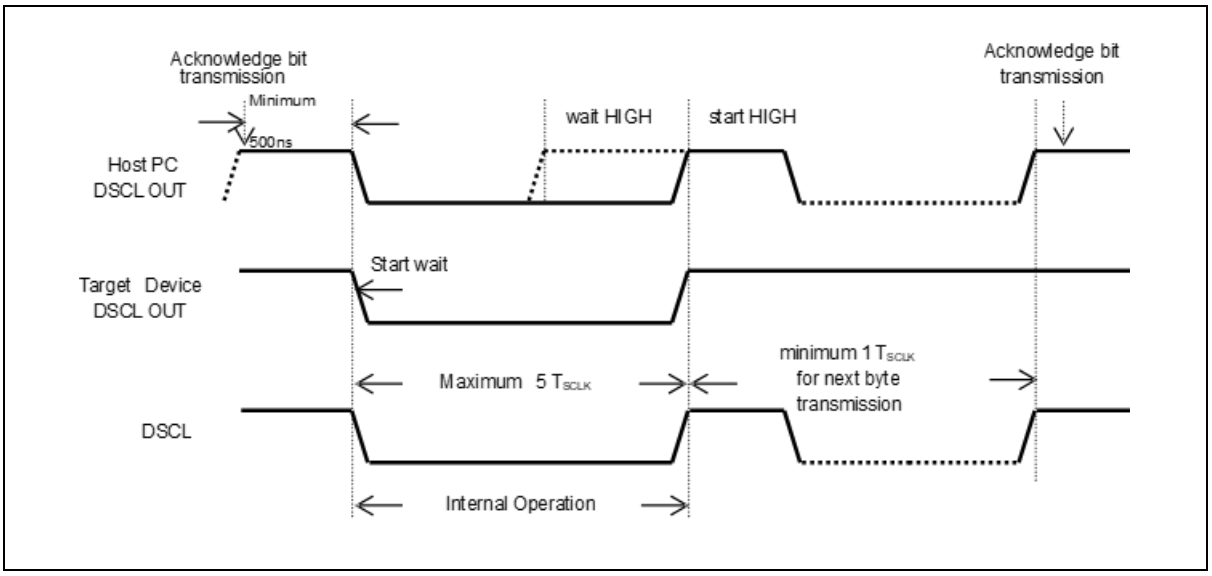


Figure 41. Clock Synchronization during Wait Procedure

16.5.3 Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

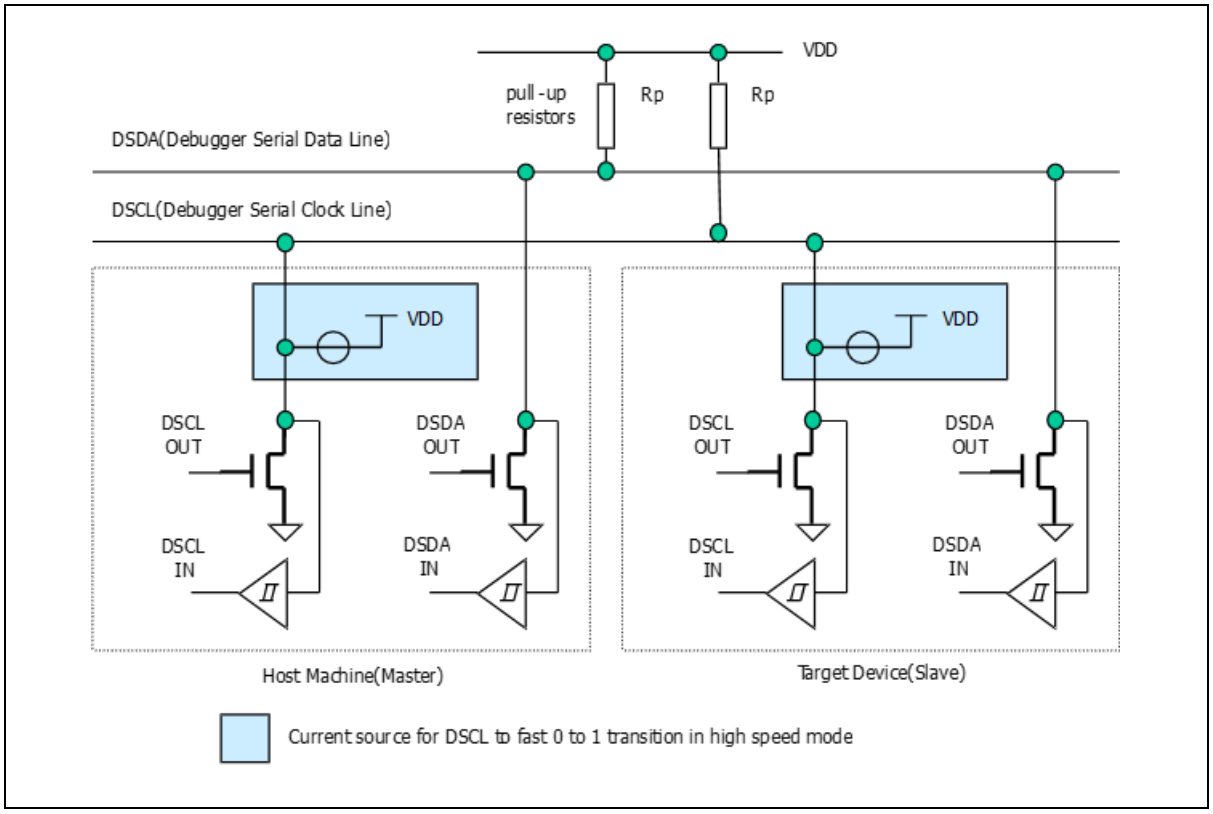


Figure 42. Connection of Transmission

17 Package information

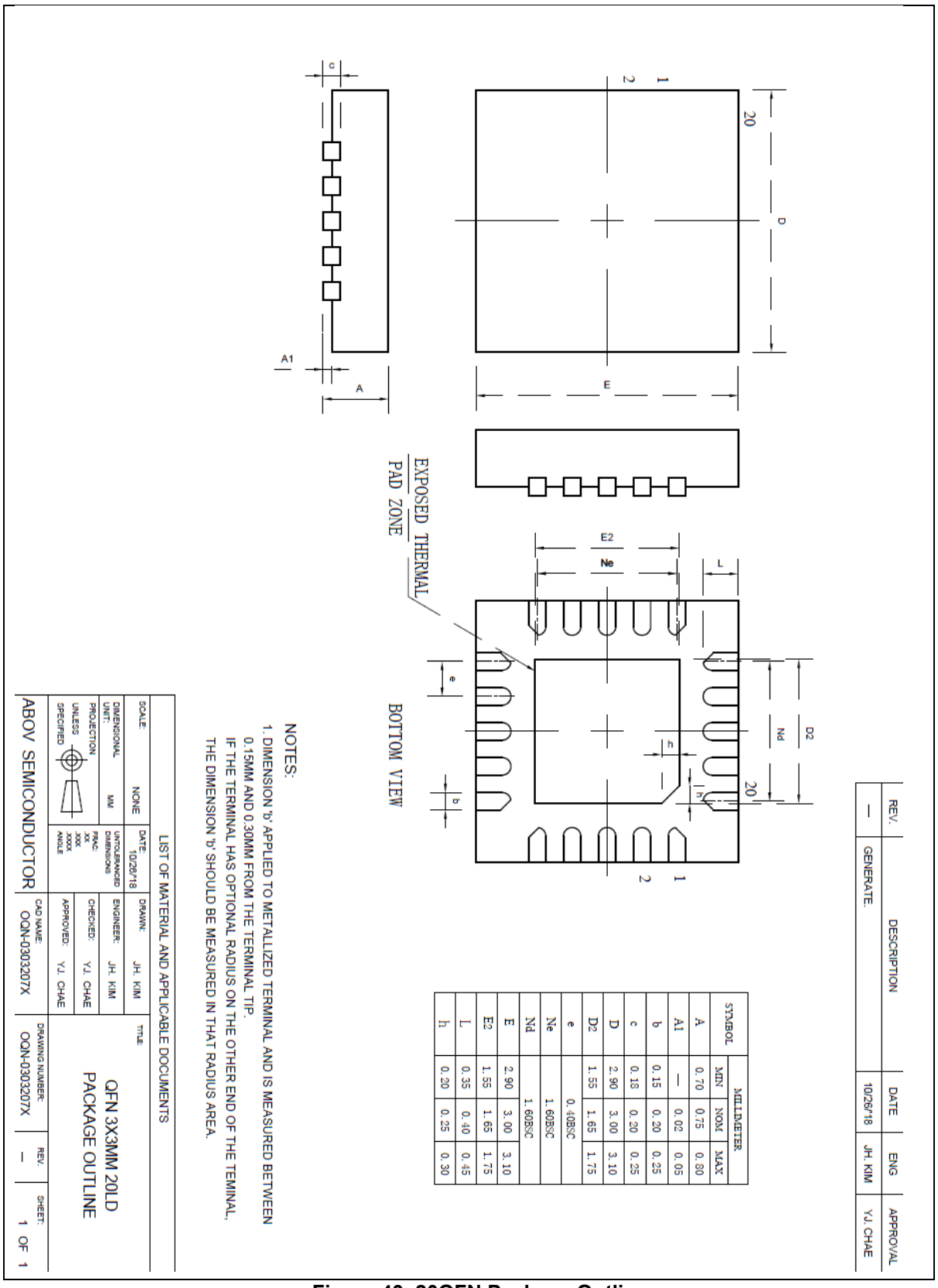


Figure 43. 20QFN Package Outline

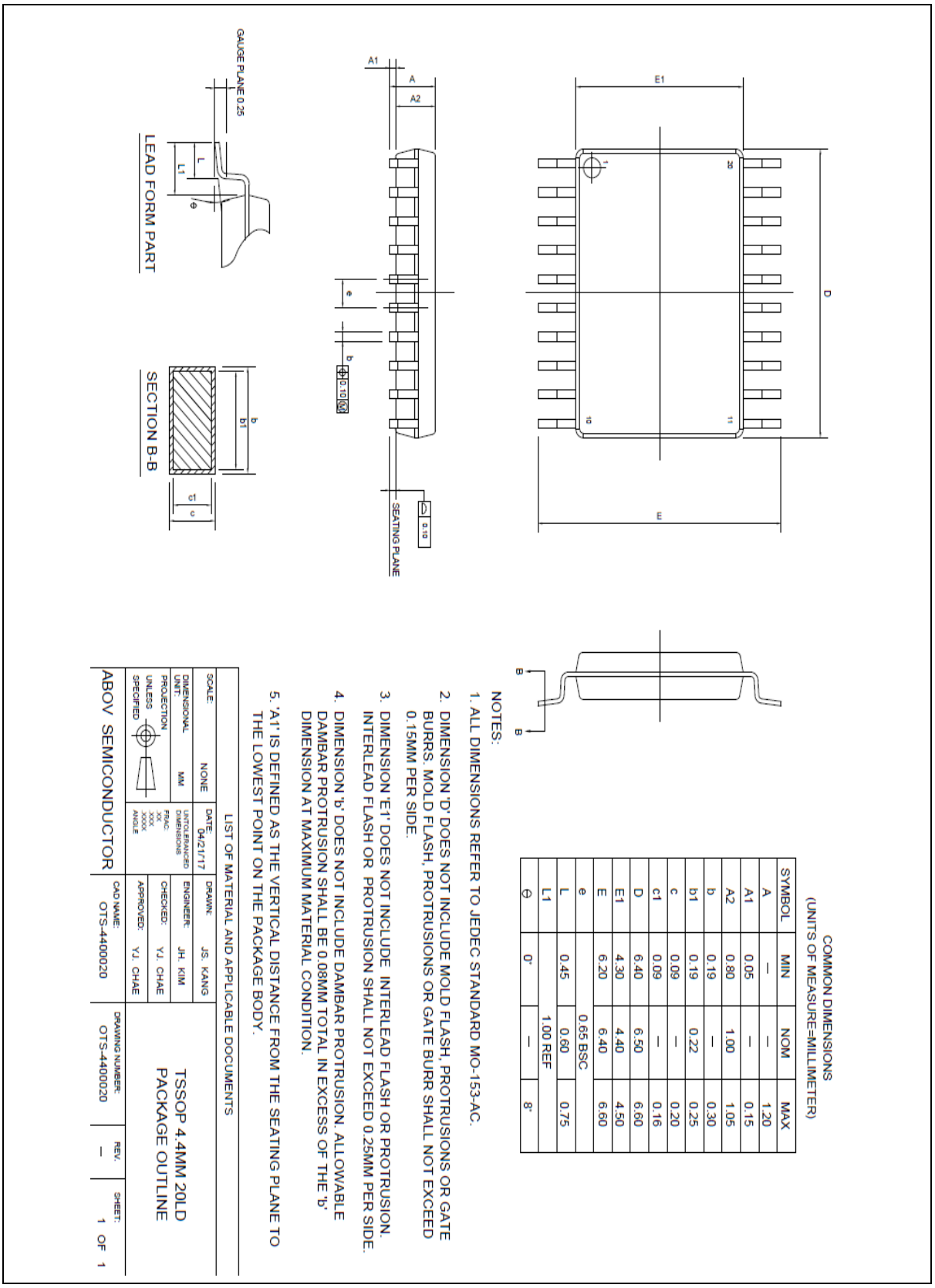
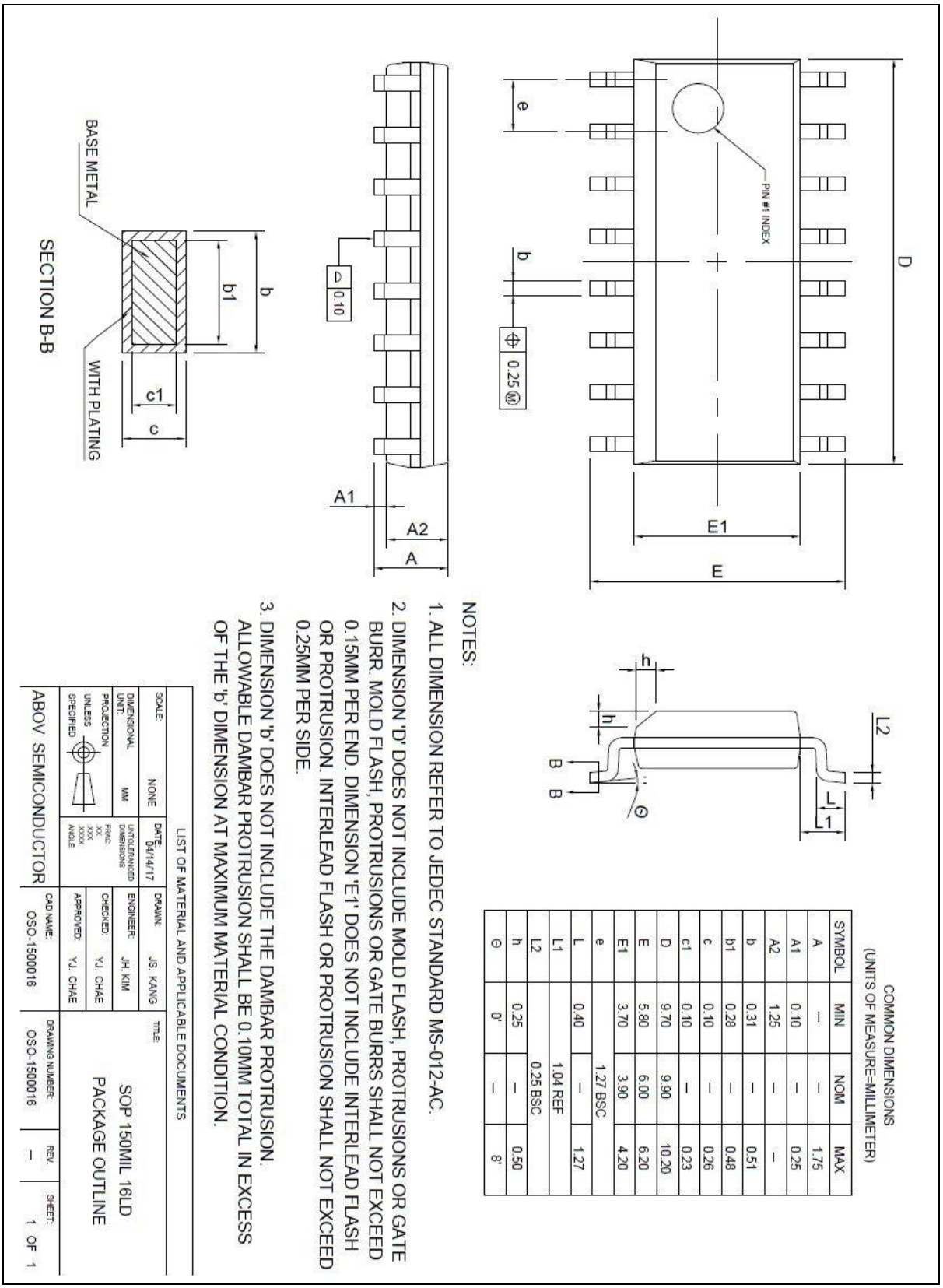


Figure 44. 20 TSSOP Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
b1	0.28	–	0.48
c	0.10	–	0.26
c1	0.10	–	0.23
D	9.70	9.90	10.20
E	5.80	6.00	6.20
E1	3.70	3.90	4.20
e		1.27 BSC	
L	0.40	–	1.27
L1		1.04 REF	
L2		0.25 BSC	
h	0.25	–	0.50
θ	0°	–	8°

NOTES:

1. ALL DIMENSION REFER TO JEDEC STANDARD MS-012-AC.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. DIMENSION 'b' DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

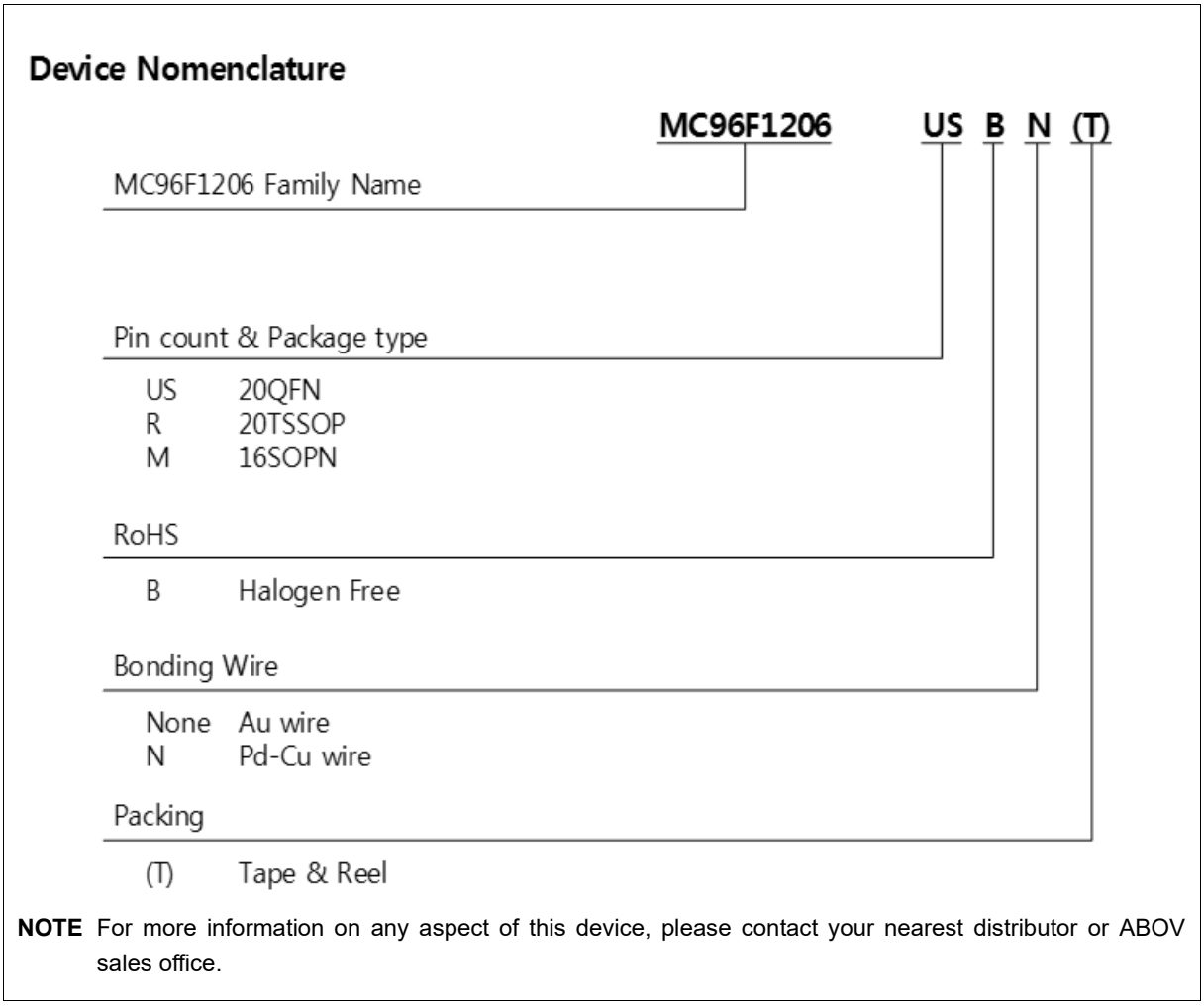
SCALE: NONE	DATE: 04/14/17	DRAWN: JS. KANG	TITLE: SOP 150MIL 16LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: XX DEC: XXX ANGLE: XXX	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OSO-1500016	APPROVED: YJ. CHAE	DRAWING NUMBER: OSO-1500016 / REV: – / SHEET: 1 OF 1

Figure 45. 16SOPN Package Outline

18 Ordering information

Table 21. MC96F1206 Device Ordering Information

Device Name	FLASH	IRAM	XRAM	ADC	I/O PORT	Package
MC96F1206USBN	6 Kbytes	256 bytes	-	15 inputs	18	20-QFN
MC96F1206RBN	6 Kbytes	256 bytes	-	15 inputs	18	20-TSSOP
MC96F1206MBN	6 Kbytes	256 bytes	-	12 inputs	14	16-SOPN



NOTE For more information on any aspect of this device, please contact your nearest distributor or ABOV sales office.

Figure 46. MC96F1206 Device Numbering Nomenclature

Appendix

A. Configure option

7	6	5	4	3	2	1	0
BSIZE[1]	BSIZE[0]	-	-	RSTEN	LOCKB	-	LOCKF
R	R	-	-	R	R	-	R

Initial value : 00H

BSIZE[1:0]	Select Specific Area for Write Protection. NOTE) When LOCKB is set, it's applied. 00 000h~7FFh (2KB) 01 000h~9FFh (2.5KB) 10 000h~BFFh (3KB) 11 000h~DFFh (3.5KB)
RSTEN	Select RESETB pin. 0 Enable RESETB pin. (default) 1 Disable RESETB pin.
LOCKB	Select Code Write Protection with Specific Area 0 Disable Code Write Protection 1 Enable Code Write Protection
LOCKF	Select Code Read Protection. 0 Disable Code Read Protection 1 Enable Code Read Protection

B. Instruction table

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column in tables shown below.
- Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following tables in this section.
- 1 machine cycle comprises 2 system clock cycles.

Table 22. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 23. Instruction Table: Logical

Logical				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 24. Instruction Table: Data Transfer

Data Transfer				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 25. Instruction Table: Boolean

Boolean				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3

SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 26. Instruction Table: Branching

Branching				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 27. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

Table 28. Instruction Table: Additional Instructions

Additional instructions (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, and the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

C. Flash protection for invalid erase/ write

Appendix C shows example code to prevent code or data from being changed by abnormal operations such as noise, unstable power, and malfunction.

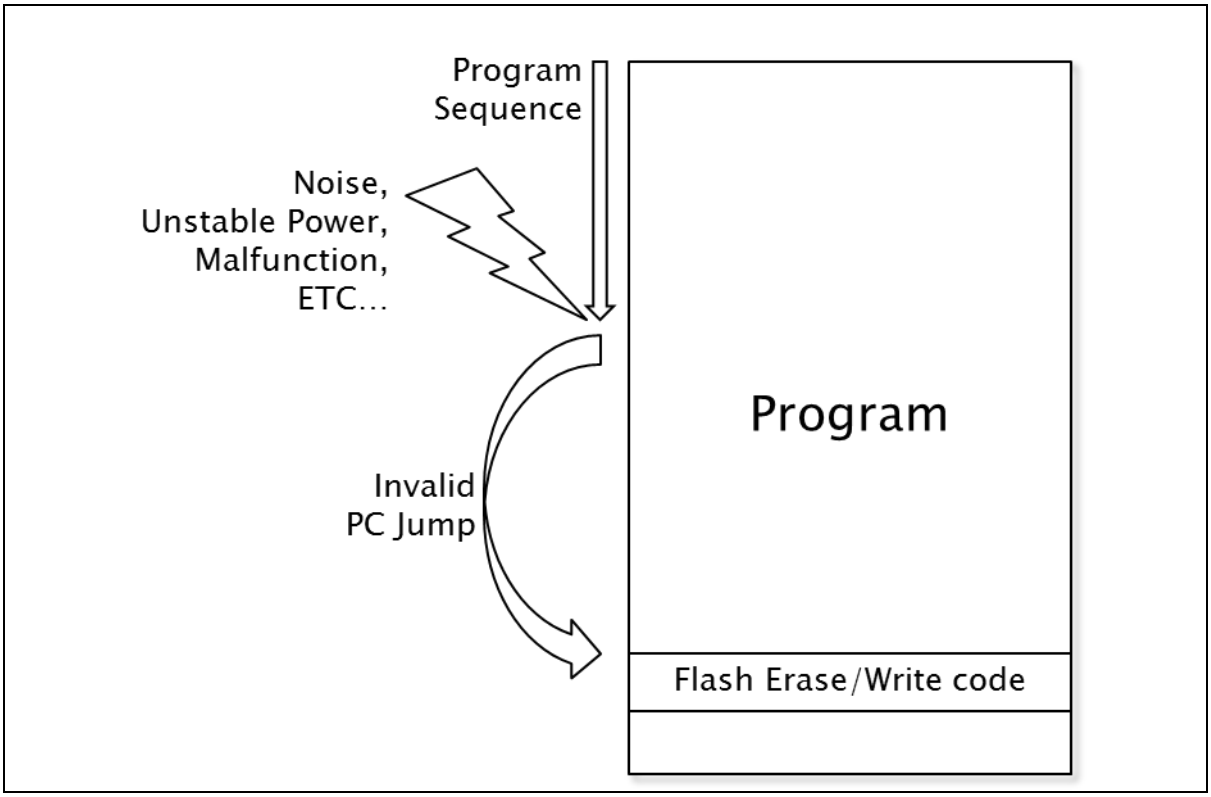


Figure 47. Flash Protection against Abnormal Operations

How to protect the flash

- Divide into decision and execution to Erase/Write in flash.
  - Check the program sequence from decision to execution in order of precedence about Erase/Write.
  - Setting the flags in program and check the flags in main loop at the end
  - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
  - If the flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
  - Set the flash sector address to dummy address in usually run time.
  - Change the flash sector address to real area range shortly before Erase/Write.
  - Even if invalid Erase/Write occurred, it will be Erase/Write in dummy address in flash.
- Use the LVR/LVI
  - Unstable or low powers give an adverse effect on MCU. So use the LVR/LVI

Protection flow description

The flash protection procedure is described in flowchart in figure 129, and each step in the figure 129 is introduced in the following lists:

1. Initialization
- Set the LVR/LVI. Check the power by LVR/LVI and do not execute under unstable or low power.
- Initialize User_ID1/2/3
- Set Flash Sector Address High/Middle/Low to Dummy address. Dummy address is set to unused area range in flash.
2. Decide to Write
- When the Erase/Write are determined, set flag. Do not directly Erase/Write in flash.
- Make the user data.
3. Check and Set User_ID1/2/3
- In the middle of source, insert code which can check and set the flags.
- By setting the User_ID 1/2/3 sequentially and identify the flow of the program.
4. Set Flash Sector Address
- Set address to real area range shortly before Erase/Write in flash.
- Set to Dummy address after Erase/Write. Even if invalid work occurred, it will be Erase/Write in Dummy address in flash.
5. Check Flags
— If every flag (User_ID1/2/3, LVI, Flash Address Min/Max) was set, than do Erase/Write.
— If the Flash Sector Address is outside of Min/Max, do not execute
— Address Min/Max is set to unused area.
6. Initialize Flags
— Initialize User_ID1/2/3
— Set Flash Sector Address to Dummy Address

• Sample Source
— Refer to the ABOV website (www.abovsemi.com).
— It is created based on the MC97F2664.
— Each product should be modified according to the Page Buffer Size and Flash Size

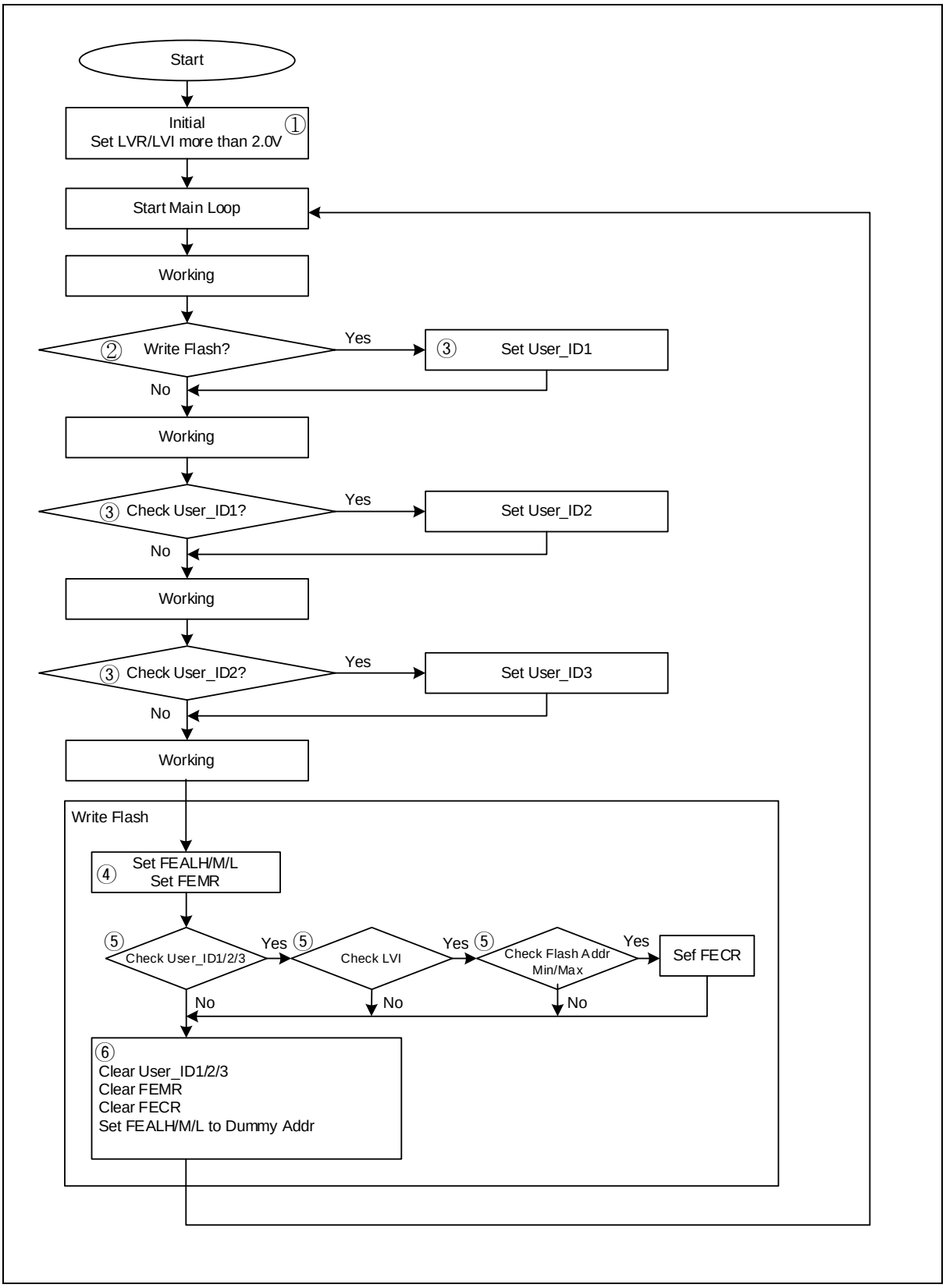


Figure 48. Flowchart of Flash Protection

Other protection by the configure options

- Protection by Configure option

— Set flash protection by MCU Write Tool (OCD, PGM+, etc.)
Vector Area:

00H~FFH

Specific Area:

2KBytes (Address 000H – 07FFH)

2.5KBytes (Address 0000H – 09FFH)

3KBytes (Address 0000H – 0BFFH)

3.5KBytes (Address 0000H – 0DFFH)

— The range of protection may be different each product.

Revision history

Date	Revision	Description
2019-09-05	1.00	First creation
2020-03-20	1.10	Renewal
2020-07-01	1.20	Changed the body information of 20 QFN package from 4x4 mm to 3x3 mm.
2020-07-20	1.21	Corrected the Flash size to 6KB at Table 1. Device Summary. Corrected Internal RC oscillator to 32MHz at Table 2. MC96F1206 Device Features and Peripheral Counts. Corrected the values for block diagram at Figure 1. MC96F1206 Block Diagram.
2022-10-27	1.22	Revised the font of this document

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