CMOS single-chip 8-bit MCU with 12-bit A/D converter and LCD driver

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 32 Kbytes Flash Code Memory
  - 1024 bytes SRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16MHz RC Oscillator (±1.5%, T_A = 0 ~ +50°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (16 inputs)
  - USI (USART + SPI + I2C) 2 sets
  - LCD Driver (21 segments x 8 commons)
- **I/O and Packages**
  - Up to 42 programmable I/O lines with 48/44-pin package
  - 48 QFN, 44 MQFP, 32 LQFP, 32/28 SOP, 24 QFN
- **Operating Conditions**
  - 2.2V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Small Home Appliance
  - BLDC Motor Controller

MC96F6432A
MC96F6332A

Data Sheet

V 1.9

Revised 26 October, 2022

Revision history

Version	Date	Revision list
0.0	2015.09.18	Published this book.
0.1	2015.12.16	Change symbol name from ILE, DLE, FSE, t_{CON}, V_{AN}, I_{AN} to INL, DNL, TOE, t_{CONV}, V_{AIN}, I_{AIN} in 7.3 A/D Converter Characteristics Fix typos.
1.0	2016.02.03	Add a “MC96F6432AU” 48 QFN package. Add IRC Max 16MHz in 7.6 High Internal RC Oscillator Characteristics. Add a note about IRC frequency in 11.1 Clock Generator.
1.1	2016.03.25	Modify 48-Pin QFN Package Diagram
1.2	2016.04.08	Add a “Full-flash erase mode method” in different table. Remove the note about “direct bit test and branch instructions”, Modify the program tips in Chapter 15. Flash Memory. Add an appendix about “Flash Protection for invalid Erase/Write”
1.3	2016.05.26	Change ‘8.5MHz (Max)’ to “Main X-TAL Operating Frequency” in Electrical Characteristics.
1.4	2016.05.30	Add a “MC96F6332AL” 32LQFP package.
1.5	2016.07.06	Remove the 28TSSOP package. Change Gang programmer from StandAlone GANG8 to E-GANG4/E-GANG6. Fixed typos of I2C Status Register.
1.6	2017.02.09	Updated Package diagrams in Chapter 4. Package Diagram. Added the note on the flash memory erase and write in Chapter 15. Flash Memory. Updated OCD dongle image in Chapter 1.3 Development tools.
1.7	2018.06.22	Fixed typos. Updated All Package Diagram.
1.8	2022.02.24	Add a “MC96F6232AU” 24 QFN package.
1.9	2022.10.26	Revised this book. Modify a font. Added Figure 1.1 Device Nomenclature.

Version 1.9

Published by FAE team

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1 Overview

1.1 Description

The MC96F6432A is an advanced CMOS 8-bit microcontroller with 32 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This offers the following features: 32 Kbytes of FLASH, 256 bytes of IRAM, 768 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, 10-bit PWM output, watch timer, buzzer driving port, SPI, USI, 12-bit A/D converter, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F6432A also supports power saving modes to reduce power consumption.

Device Name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
MC96F6432AU	32Kbytes	768bytes	256bytes	16 inputs	42	48 QFN
MC96F6432AQ				16 inputs	42	44 MQFP
MC96F6332AL				12 inputs	30	32 LQFP
MC96F6332AD				12 inputs	30	32 SOP
MC96F6332AM				11 inputs	26	28 SOP
MC96F6232AU				8 inputs	22	24 QFN

Table 1.1 Ordering Information of MC96F6432A

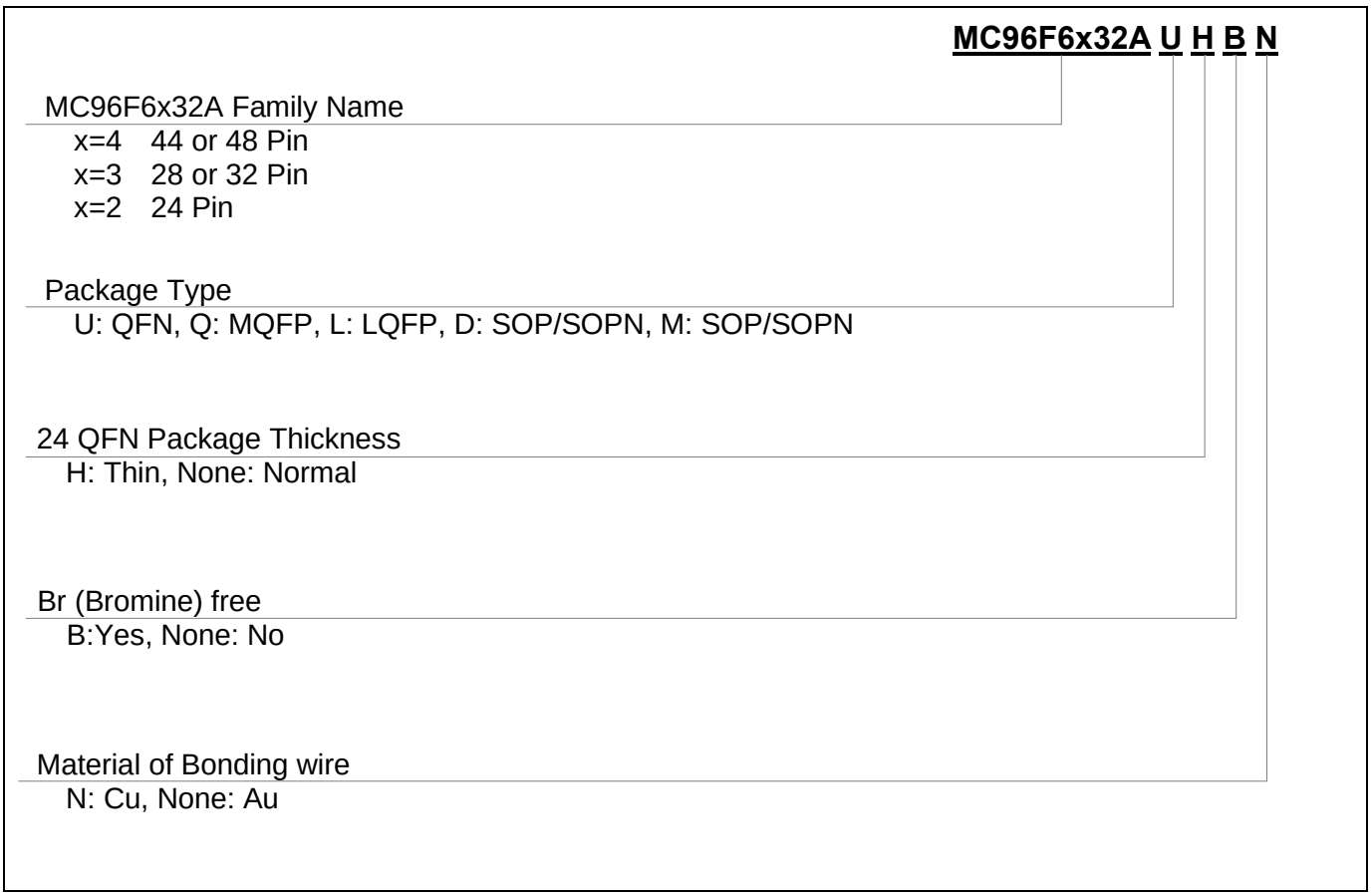


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 32Kbytes Flash with self-read and write capability
  - In-System Programming(ISP)
  - Endurance : 10,000 times (Sector 0~507)
    100,000 times(Sector 508~511)
  - Retention : 10 years
- **256bytes IRAM**
- **768bytes XRAM**
  - (27bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 9ports (P0[2:0], P5[5:0])
  - LCD shared I/O : 33ports (P0[7:3], P1, P2, P3, P4)
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit × 1-ch
  - Watch Dog Timer (WDT) 8-bit × 1-ch
    5kHz internal RC oscillator for WDT
  - 8-bit × 1-ch (T0), 16-bit × 2-ch (T1/T2)
  - 8-bit × 2-ch (T3/T4) or 16-bit × 1-ch (T3)
- **Programmable Pulse Generation**
  - Pulse generation (by T1/T2)
  - 8-bit PWM (by T0)
  - 6-ch 10-bit PWM for Motor (by T4)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s /1min interval at 32.768kHz
- **Buzzer**
  - 8-bit × 1-ch
- **SPI 2**
  - 8-bit × 1-ch
- **USI0/1 (UART + SPI + I2C)**
  - 8-bit UART × 2-ch, 8-bit SPI × 2-ch and I2C × 2-ch
- **12-bit A/D Converter**
  - 16 Input channels
- **LCD Driver**
  - 21segments and 8common terminals
  - Internal or external resistor bias
  - Two Internal Resistors Selectable
  - 1/2, 1/3, 1/4, 1/5, 1/6 and 1/8 duty selectable
  - Resistor Bias and 16-step contrast control
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 12 levels detect
    (1.85/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Low Voltage Indicator**
  - 11 levels detect
    (2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0~7, EINT8, EINT10, EINT11, EINT12) (12)
  - Timer(0/1/2/3/4) (5)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SPI 2 (1)
  - USI0/1 (6)
  - ADC (1)
- **Internal RC Oscillator**
  - Internal RC frequency: 16MHz ±1.5% (T_A= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.2V~ 5.5V (@32 ~ 38kHz with Crystal)
  - 2.2V~ 5.5V (@0.4 ~ 4.2MHz with Crystal)
  - 2.7V~ 5.5V (@0.4 ~ 8.5MHz with Crystal)
  - 2.2V~ 5.5V (@0.5 ~ 16.0MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 235ns (@8.5MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4 – 8.5MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 48 QFN
  - 44 MQFP-1010
  - 32 LQFP, 32 SOP
  - 28 SOP
  - 24 QFN
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compiler provider.
The MC96F6432A core is Mentor 8051 and the ROM size is smaller than 64 Kbytes. Therefore, developer can use the standard 8051 compiler from other providers.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD interface uses two-wire connection between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.
The OCD debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit) operating system. If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (http://www.abov.co.kr).

Connection:

- DSCL (MC96F6432 P01 port)
- DSDA (MC96F6432 P00 port)

NOTE)

1. MC96F6432A does not support the OCD function. MC96F6432 should be used for debugging.
2. Do not access to P0, P1, P2, P3, P4, P5 and EIFLAG0 registers through the "direct bit test and branch instructions" in the MC96F6432. Refer to the "MC96F6432 User's Manual".

OCD connector diagram: Connect OCD with user system

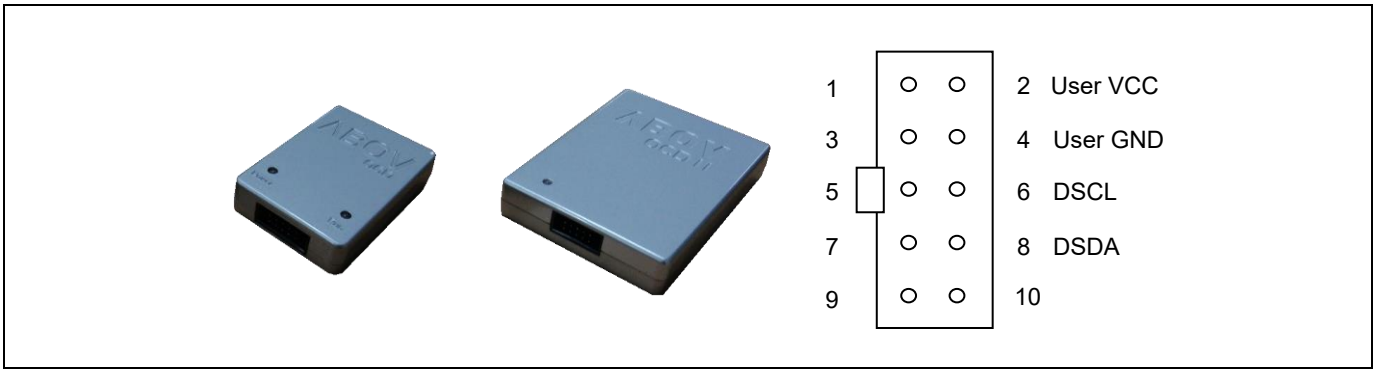


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

Subject	MC96F6432A	MC96F6432S	MC96F6432
On Chip Debugger (OCD)	Not supported	Not supported	Supported
Internal RC frequency (IRC)	Tolerance TA= 0°Cto+50°C : ±1.5% TA= -20°Cto+85°C : ±2.5% TA= -40°Cto+85°C : ±3.5%	Tolerance TA= 0°Cto+50°C : ±1.5% TA= -20°Cto+85°C : ±2.5% TA= -40°Cto+85°C : ±3.5%	Tolerance TA= 0°Cto+50°C : ±1.0% TA= -20°Cto+85°C : ±2.0% TA= -40°Cto+85°C : ±3.0%
x-tal filter selectable (XTFLSR Register)	x-tal filter selection register for noise immunity - 4.2MHz < x-tal ≤ 8.5MHz - x-tal ≤ 4.2MHz	Not supported	Not supported
LVR/LVI	12 Level Selectable - 1.85V, 2.2V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V
	11 Level Selectable - 2.2V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V
	LVR and LVI Current Both : 14.0(TYP)/24.0(MAX) uA One: 10.0(TYP)/18.0(MAX) uA	LVR and LVI Current Both : 14.0(TYP)/24.0(MAX) uA One: 10.0(TYP)/18.0(MAX) uA	LVR and LVI Current Both : 10.0(TYP)/15.0(MAX) uA One: 8.0(TYP)/12.0(MAX) uA
LCD	Internal LCD Bias Dividing Resistor Select - RLCD1 = 60kΩ - RLCD2 = 120kΩ	Internal LCD Bias Dividing Resistor Select - RLCD1 = 60kΩ - RLCD2 = 120kΩ	Internal LCD Bias Dividing Resistor - RLCD = 60kΩ
	RLCD1 - 40(MIN)/60(TYP)/80(MAX) kΩ RLCD2 - 80(MIN)/120(TYP)/160(MAX) kΩ	RLCD1 - 40(MIN)/60(TYP)/80(MAX) kΩ RLCD2 - 80(MIN)/120(TYP)/160(MAX) kΩ	RLCD - 40(MIN)/60(TYP)/80(MAX) kΩ
Vector Area Protection	En/Disable Vector Area(00H – FFH) Protection	Not supported	Not supported
Specific Area for Write Protection	8 kinds of protection size selectable - Address 0100H – 03FFH - Address 0100H – 07FFH - Address 0100H – 0BFFH - Address 0100H – 0FFFH - Address 0100H – 77FFH - Address 0100H – 7BFFH - Address 0100H – 7DFFH - Address 0100H – 7EFFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH
ADC	A/D Converter INL : ±6LSB DNL : ±1 LSB TOE : ±5 LSB ZOE : ±5 LSB	A/D Converter INL: ±6LSB DNL: ±1 LSB TOE: ±5 LSB ZOE: ±5 LSB	A/D Converter INL: ±4LSB DNL: ±1 LSB TOE: ±3 LSB ZOE: ±3 LSB
Supply Current IDD3 (Sub operation)	Typ/Max : 90/180 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃	Typ/Max : 60/90 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃	Typ/Max : 50/80 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃
Operating Voltage and Frequency	VDD: 2.2V to 5.5V, Freq.: Up to 16MHz - 2.2V to 5.5V @ 32 to 38kHz with x-tal - 2.2V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 8.5MHz with x-tal - 2.2V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC
Power-On Reset Characteristics	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/5.0[V/ms]
Full-flash erase mode method	Sector erase mode	Sector erase mode	Sector and byte erase mode

Table 1.2 Difference among MC96F6432A, MC96F6432S and MC96F6432

1.3.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

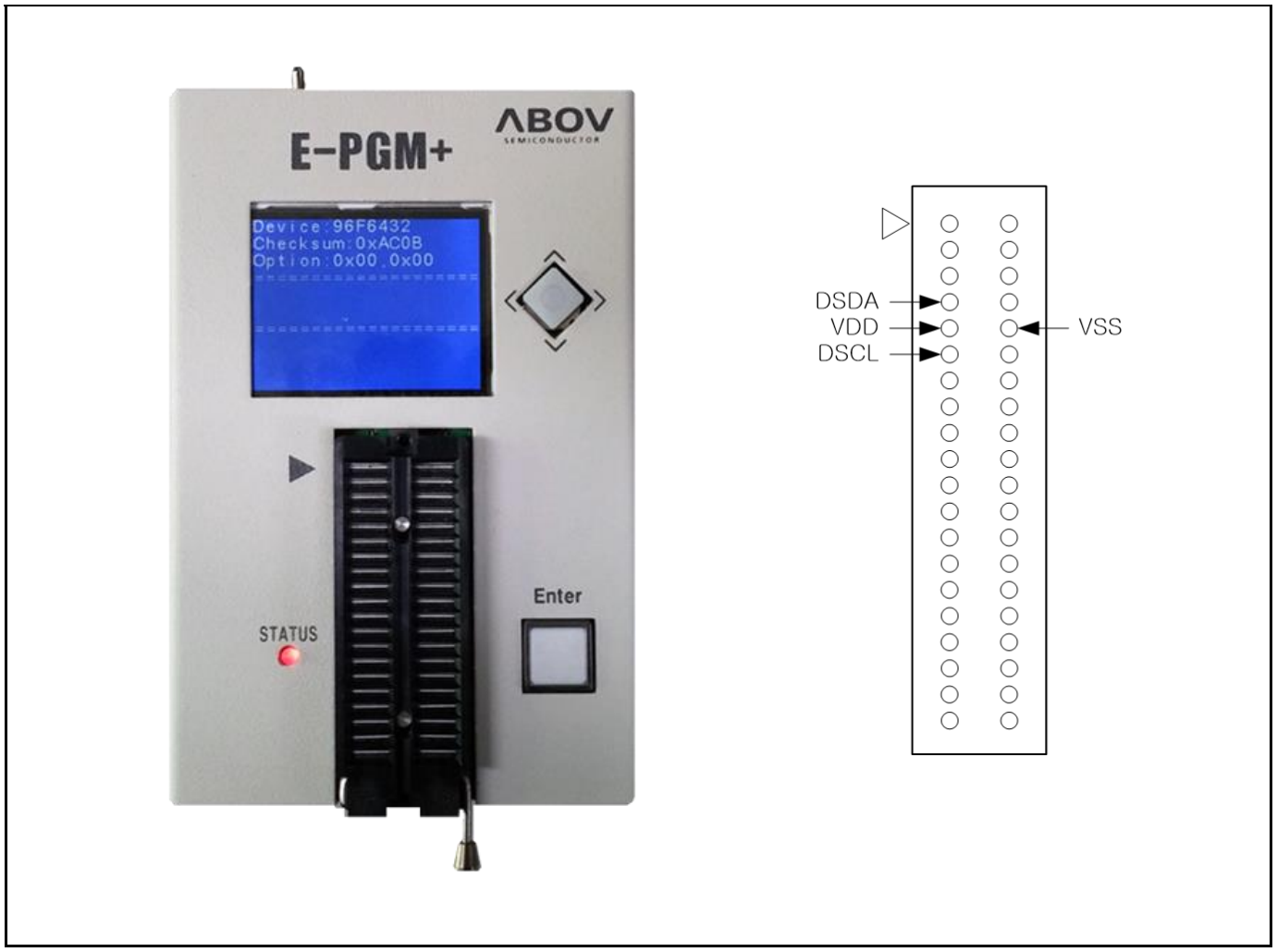


Figure 1.3 E-PGM+(Single writer)

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

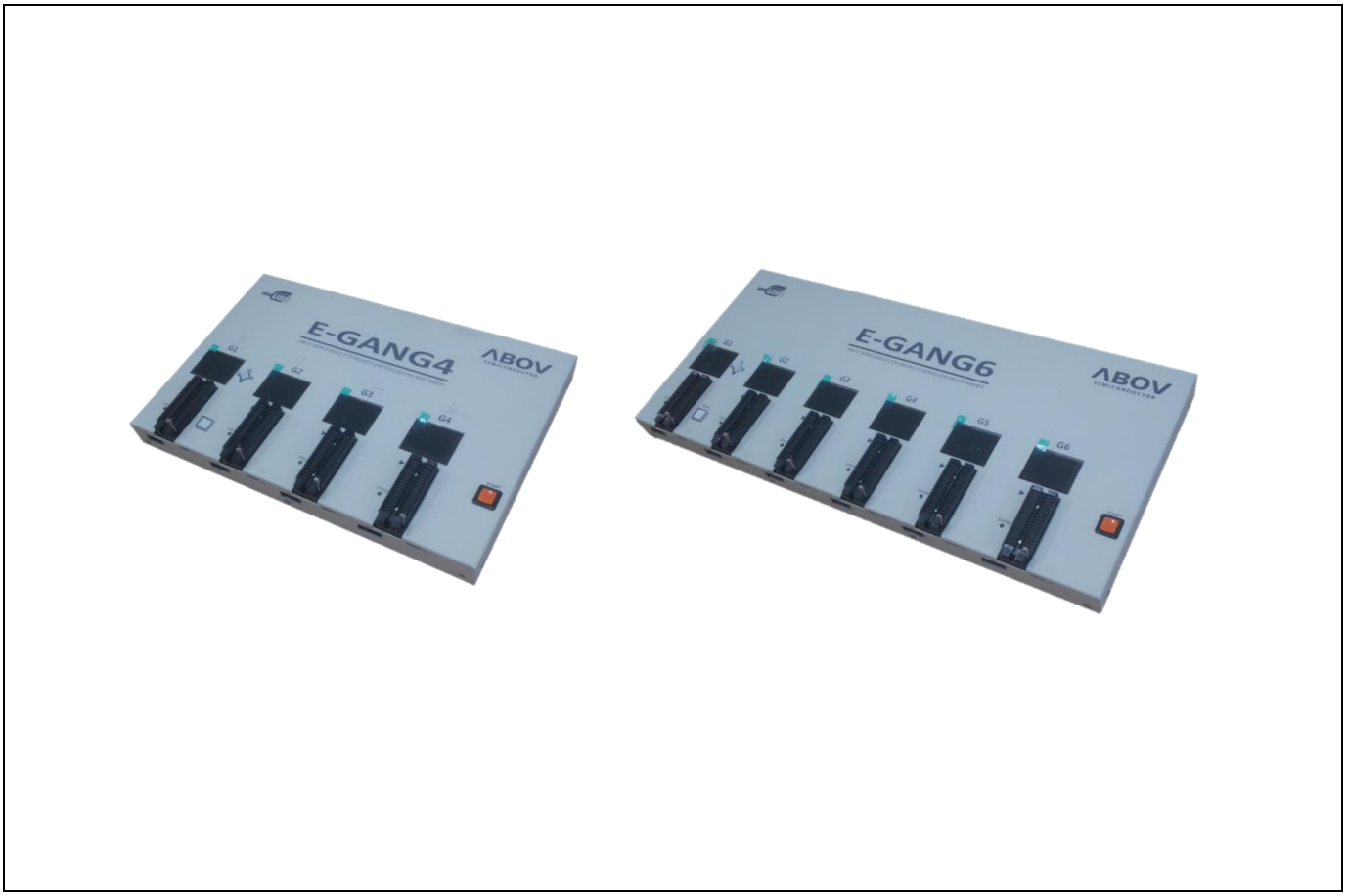


Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of MC96F6432A is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD and VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

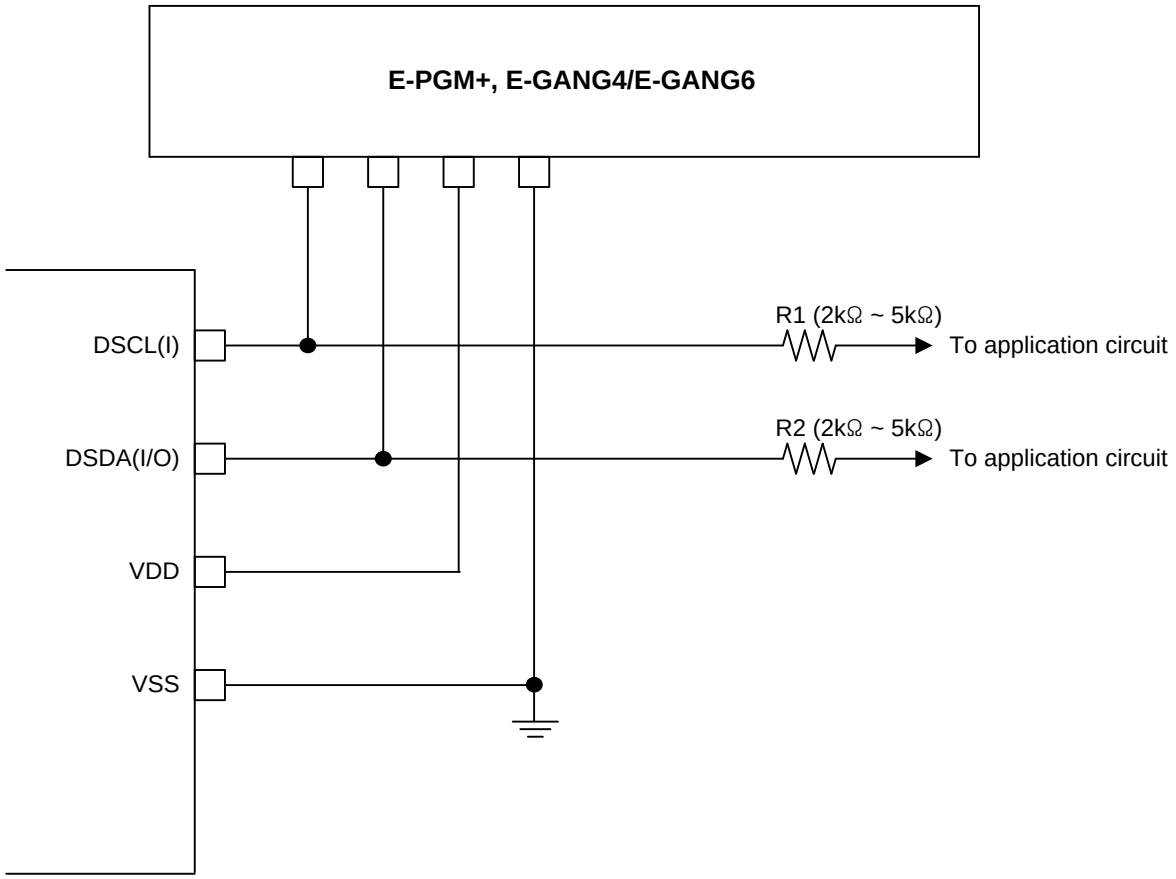
Table 1.3 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The MC96F6432A needs only four signal lines including VDD and VSS pins for programming FLASH with serial communication protocol. Therefore the on-board programming is possible if the programming signal lines are ready at the PCB of application board is designed.

1.4.2.1 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.
Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.5 PCB design guide for on board programming

2 Block diagram

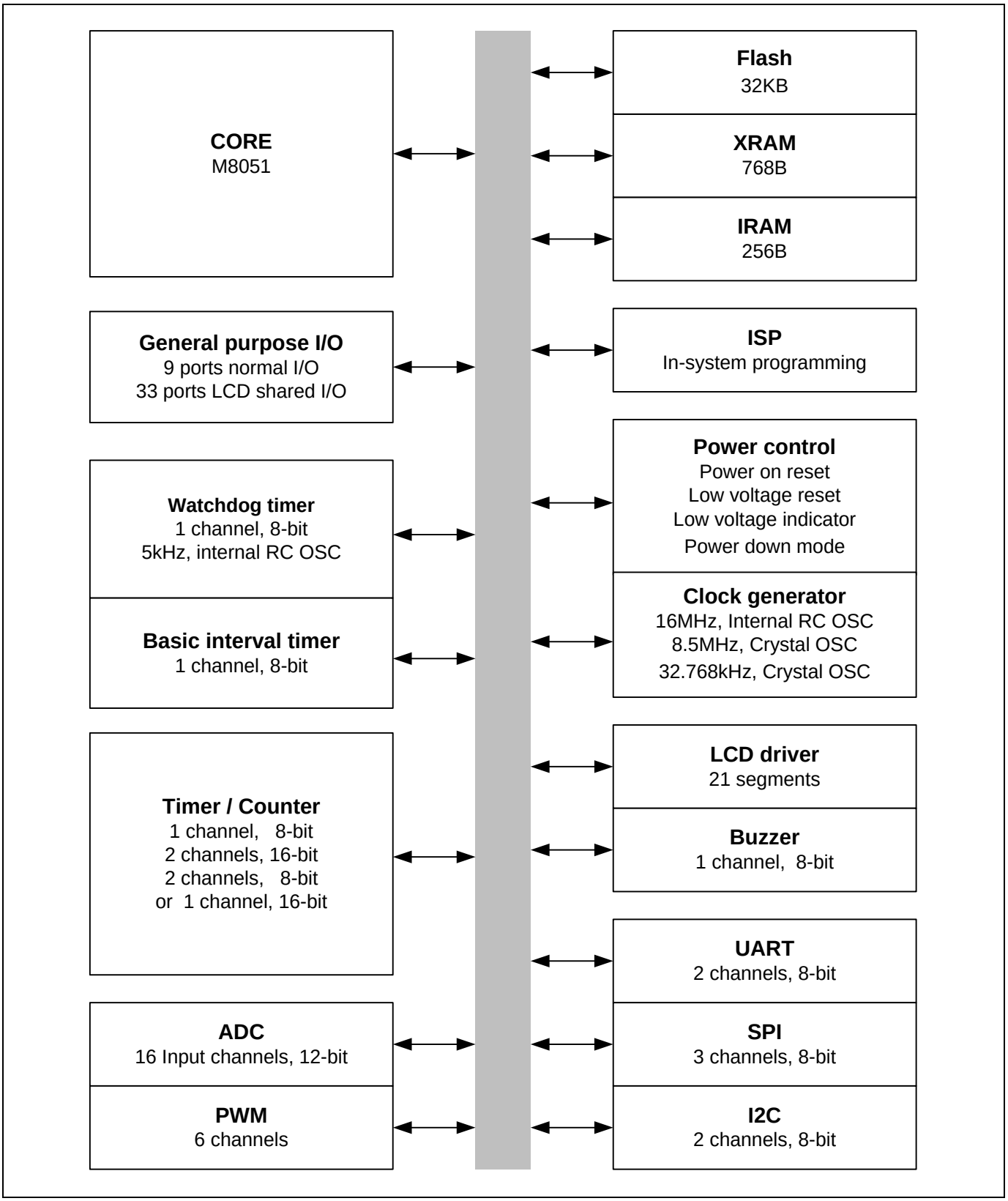
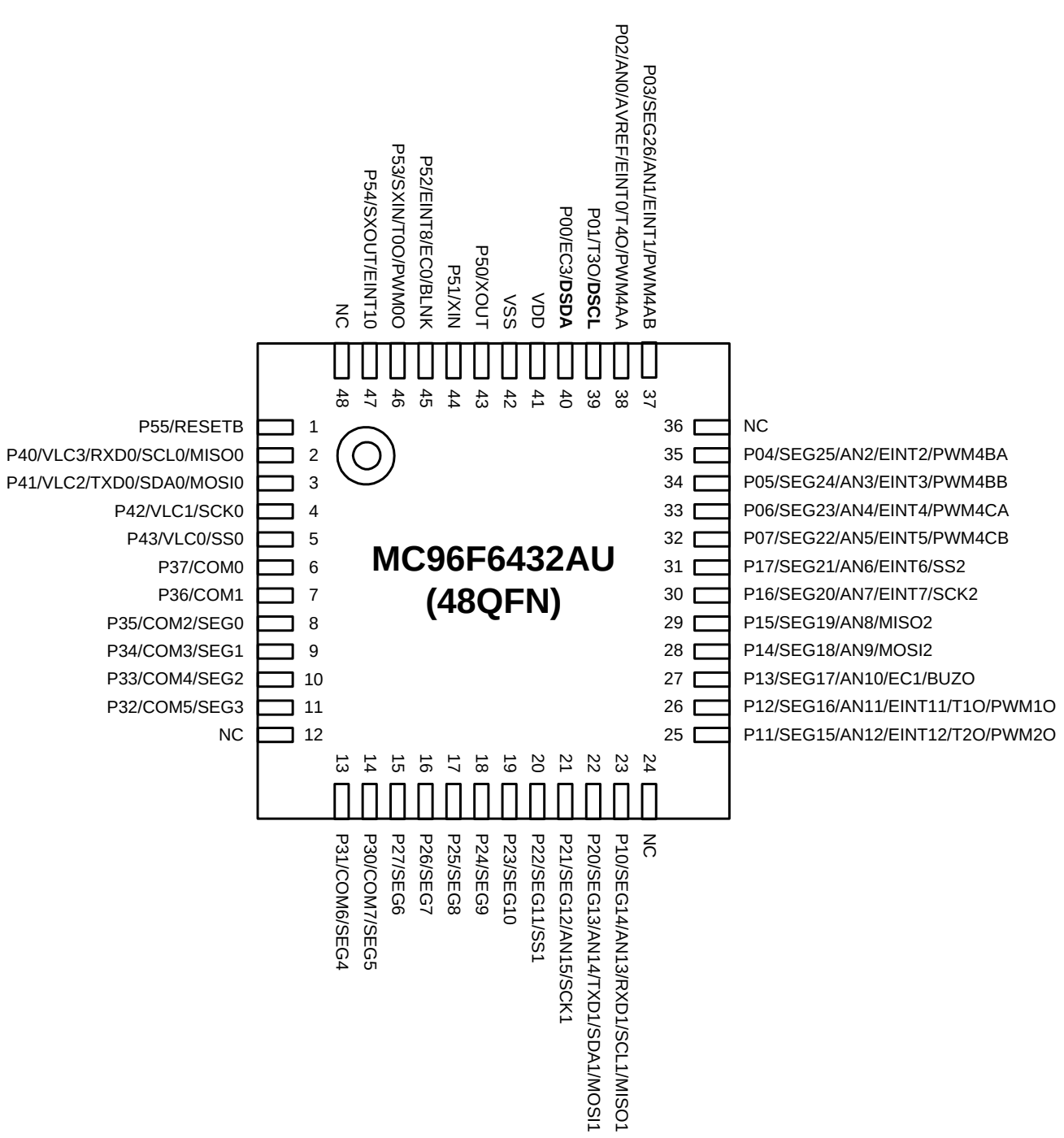


Figure 2.1 Block diagram of MC96F6432A

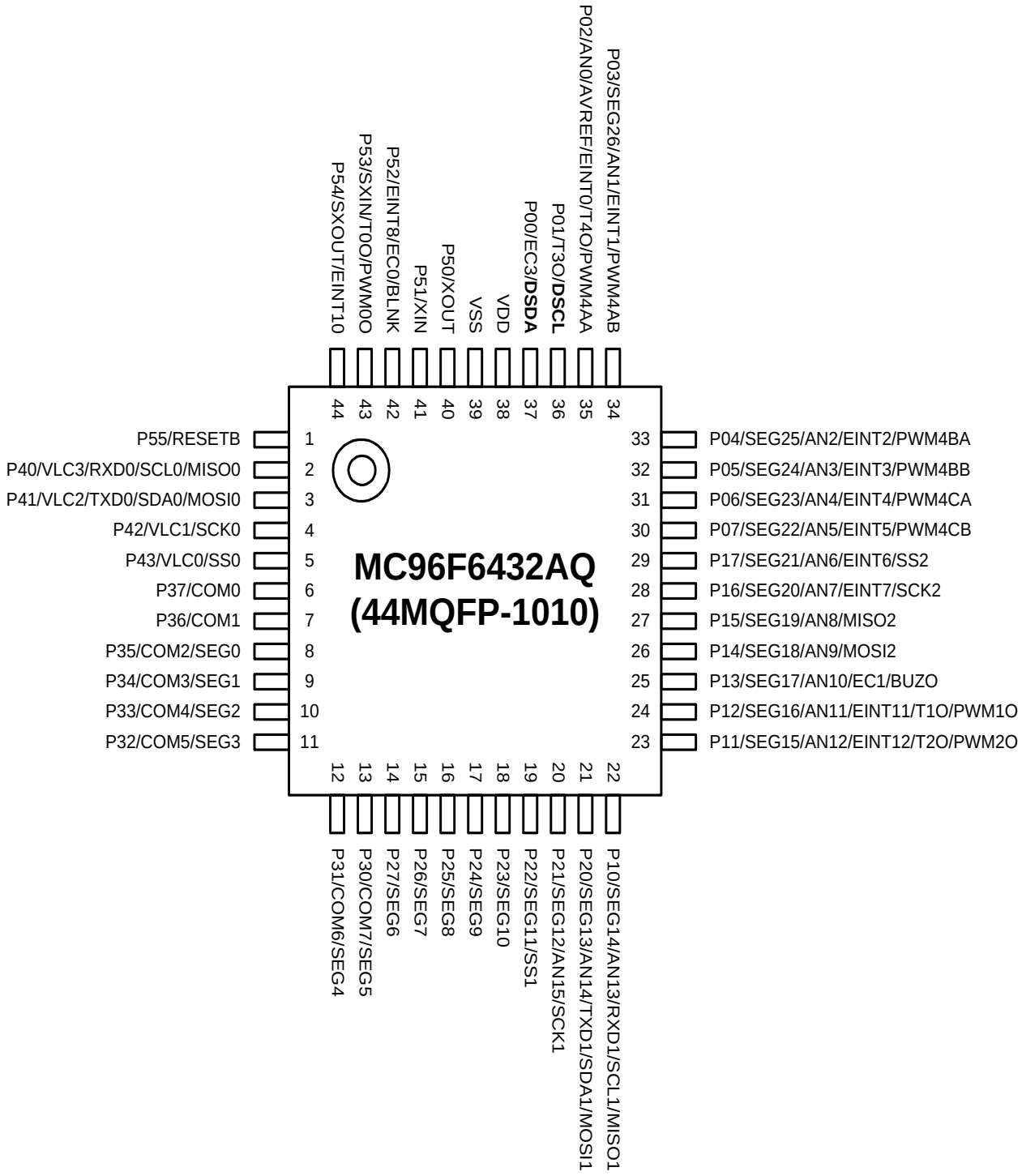
3 Pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. Do not connect anything to NC pin.

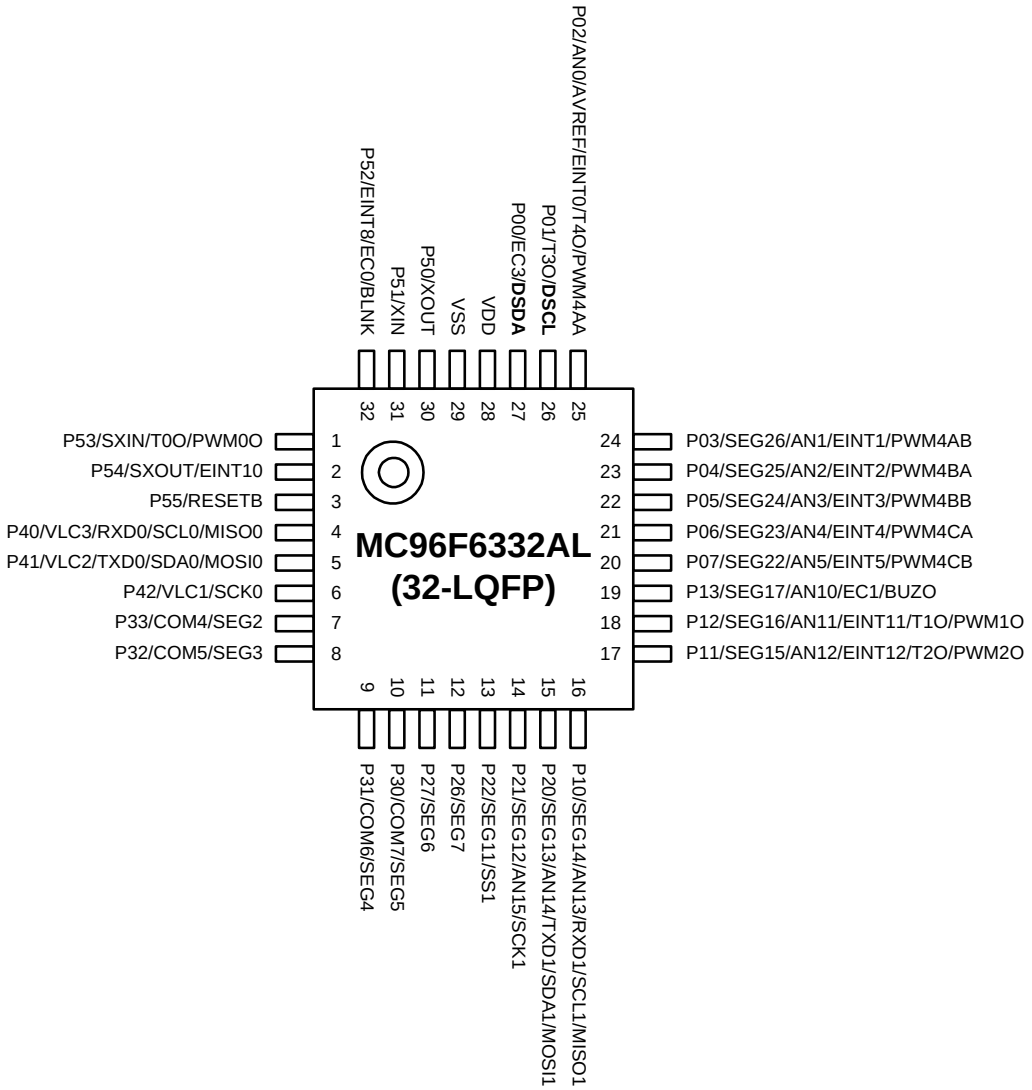
Figure 3.1 MC96F6432AU 48QFN pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.

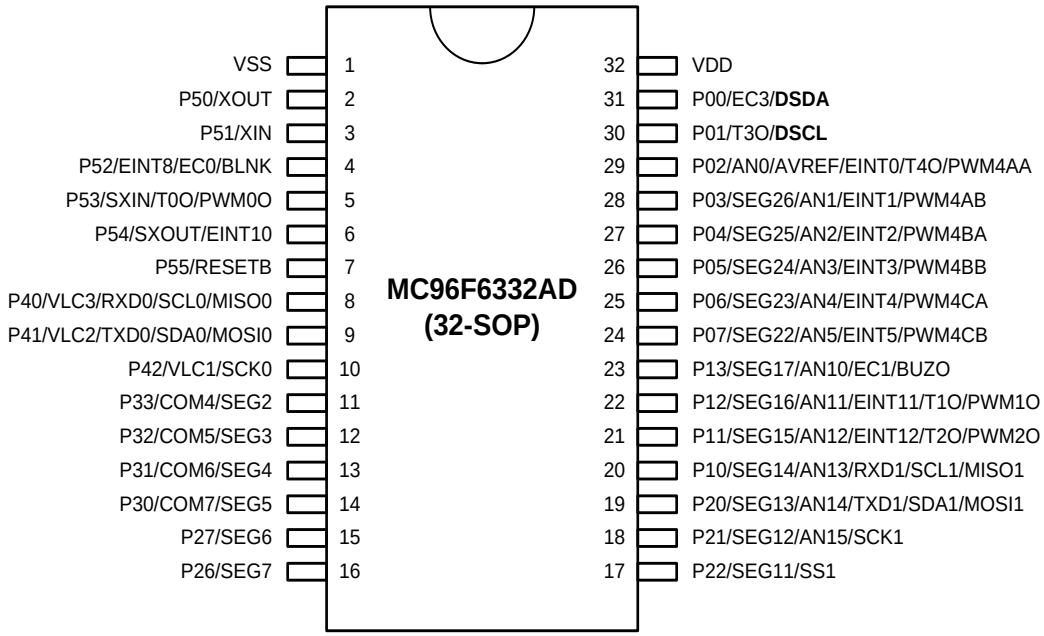
Figure 3.2 MC96F6432AQ 44MQFP-1010 pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P14-P17, P23-P25, P34-P37 and P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 32-pin package is used.

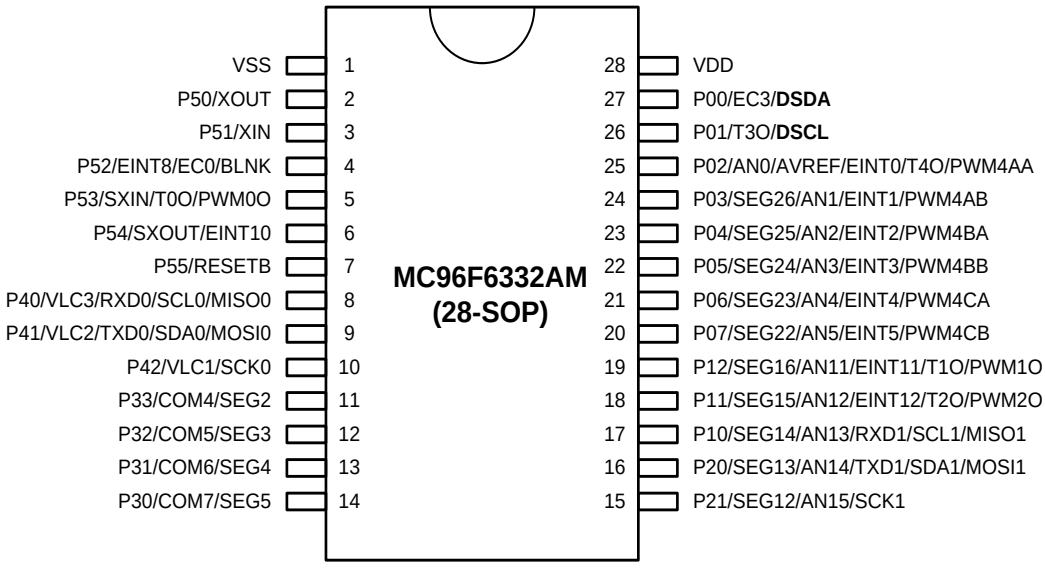
Figure 3.3 MC96F6432AL 32LQFP-0707 pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P14-P17, P23-P25, P34-P37 and P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 32-pin package is used.

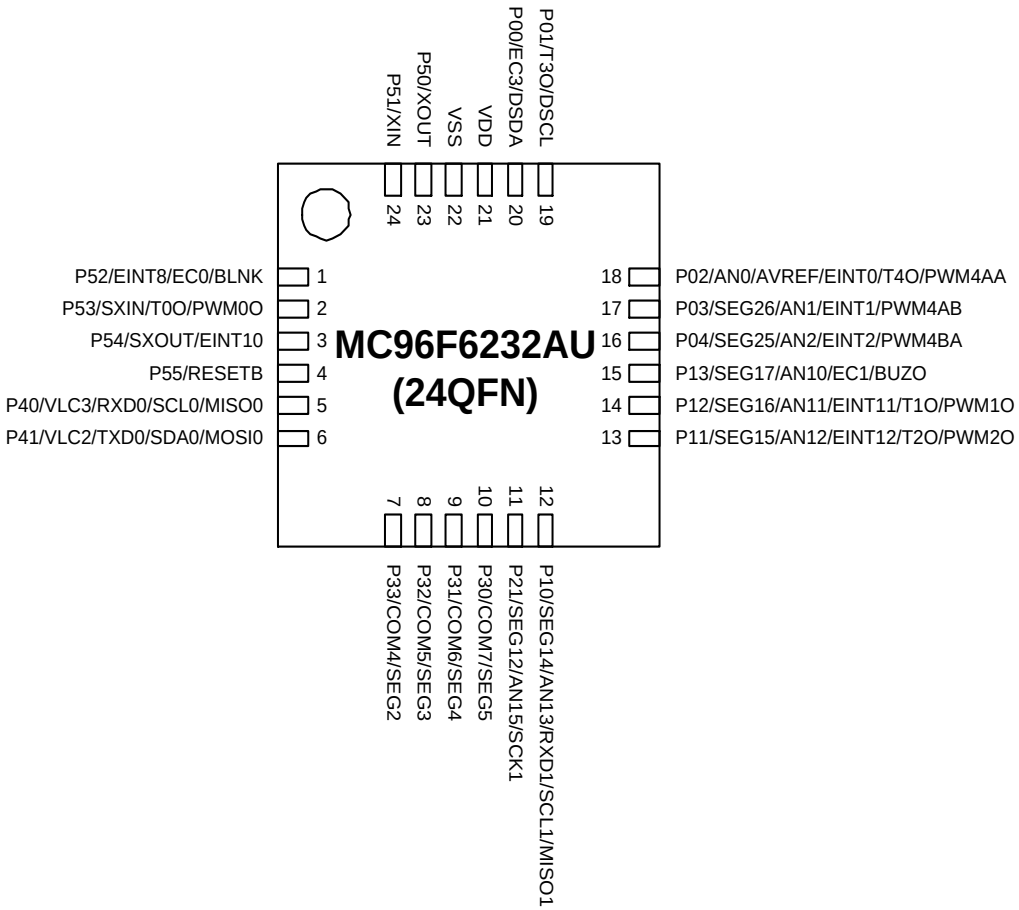
Figure 3.4 MC96F6332AD 32SOP pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P13-P17, P22-P27, P34-P37 and P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 28-pin package is used.

Figure 3.5 MC96F6332AM 28SOP pinassignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P05-P07, P14-P17, P20, P22-P27, P34-P37 and P42-P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 24-pin package is used.

Figure 3.6 MC96F6232AU 24QFN pin assignment

4 Package Diagram

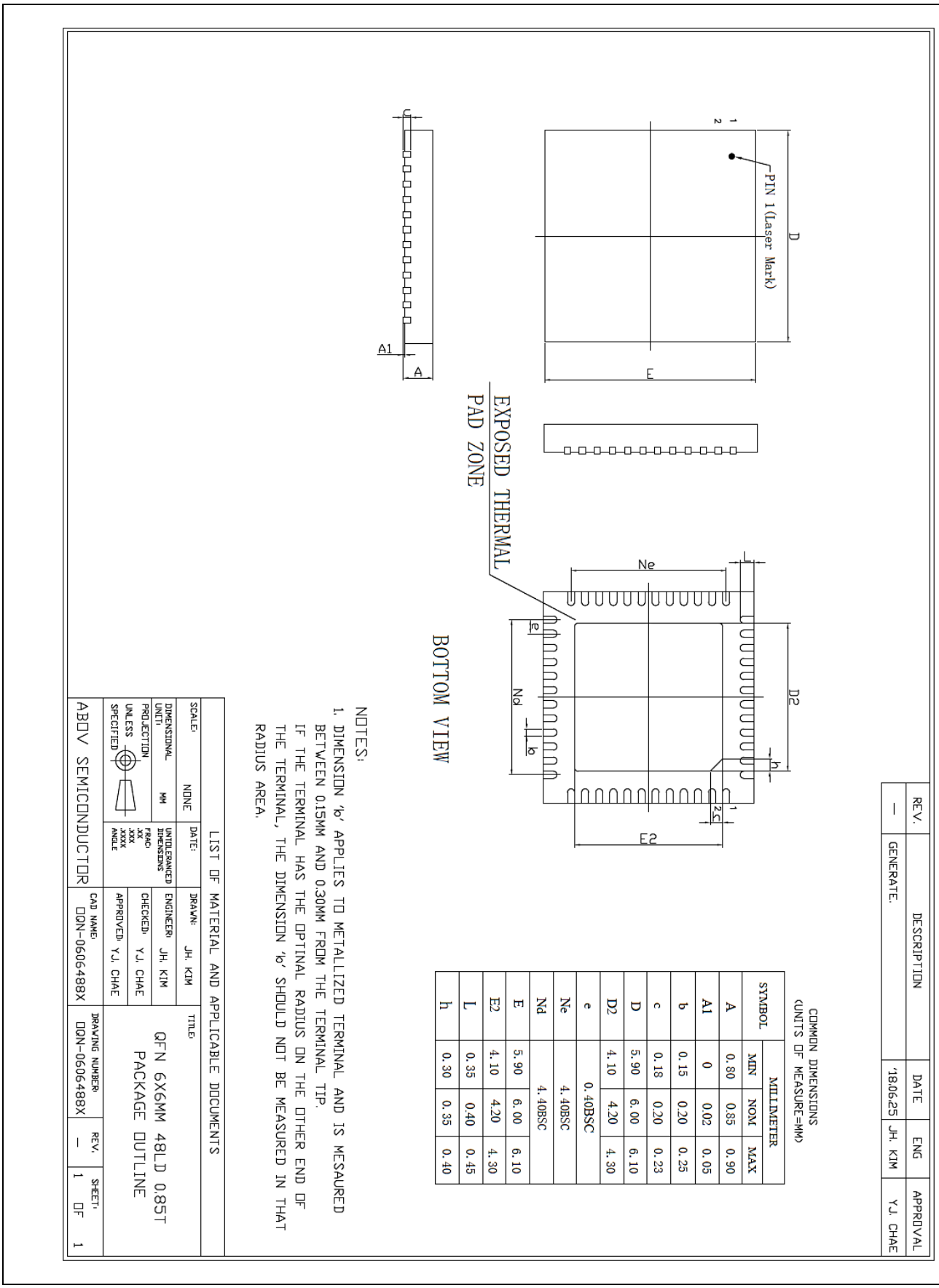
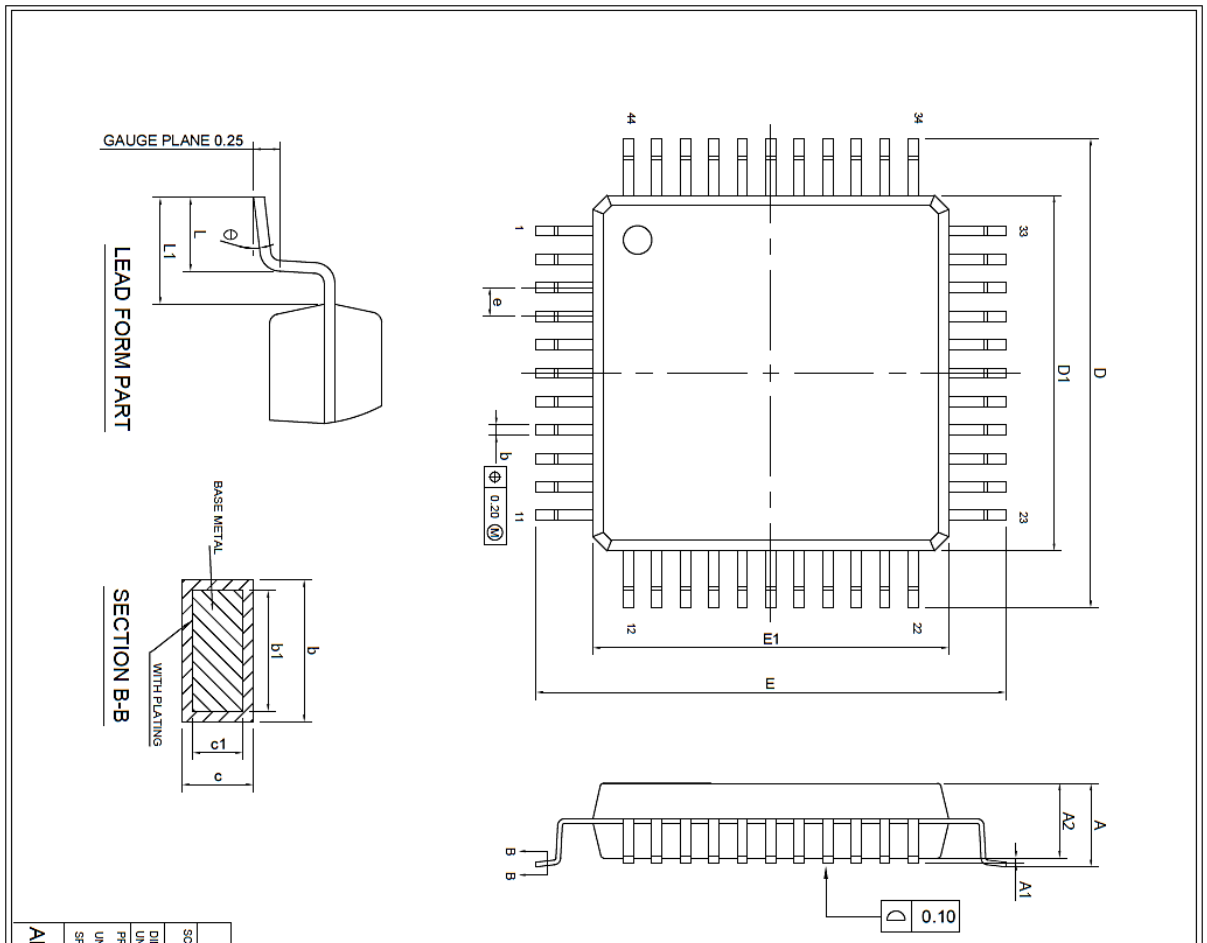


Figure 4.1 48-Pin QFN Package



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.45
A1	0.00	—	0.25
A2	1.80	2.10	2.20
b	0.28	—	0.45
b1	0.28	0.35	0.41
c	0.11	—	0.23
c1	0.11	0.15	0.19
D	12.90	13.20	13.50
D1	9.80	10.00	10.20
E	12.90	13.20	13.50
E1	9.80	10.00	10.20
e		0.80BSC	
L	0.60	—	1.03
L1		1.60 BSC	
θ	0°	—	8°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-022-AB.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS 'D1' AND 'E1' DO INCLUDE MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE: MQFP 10X10MM 44LD PACKAGE OUTLINE	
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM		
PROJECTION UNLESS SPECIFIED	FRAC: XX .XXX XXXX ANGLE	CHECKED: YJ. CHAE		
ABOV SEMICONDUCTOR		APPROVED: YJ. CHAE	CAD NAME: OMQ-1010044	DRAWING NUMBER: OMQ-1010044
				REV. —
				SHEET: 1 OF 1

Figure 4.2 44-Pin MQFP Package

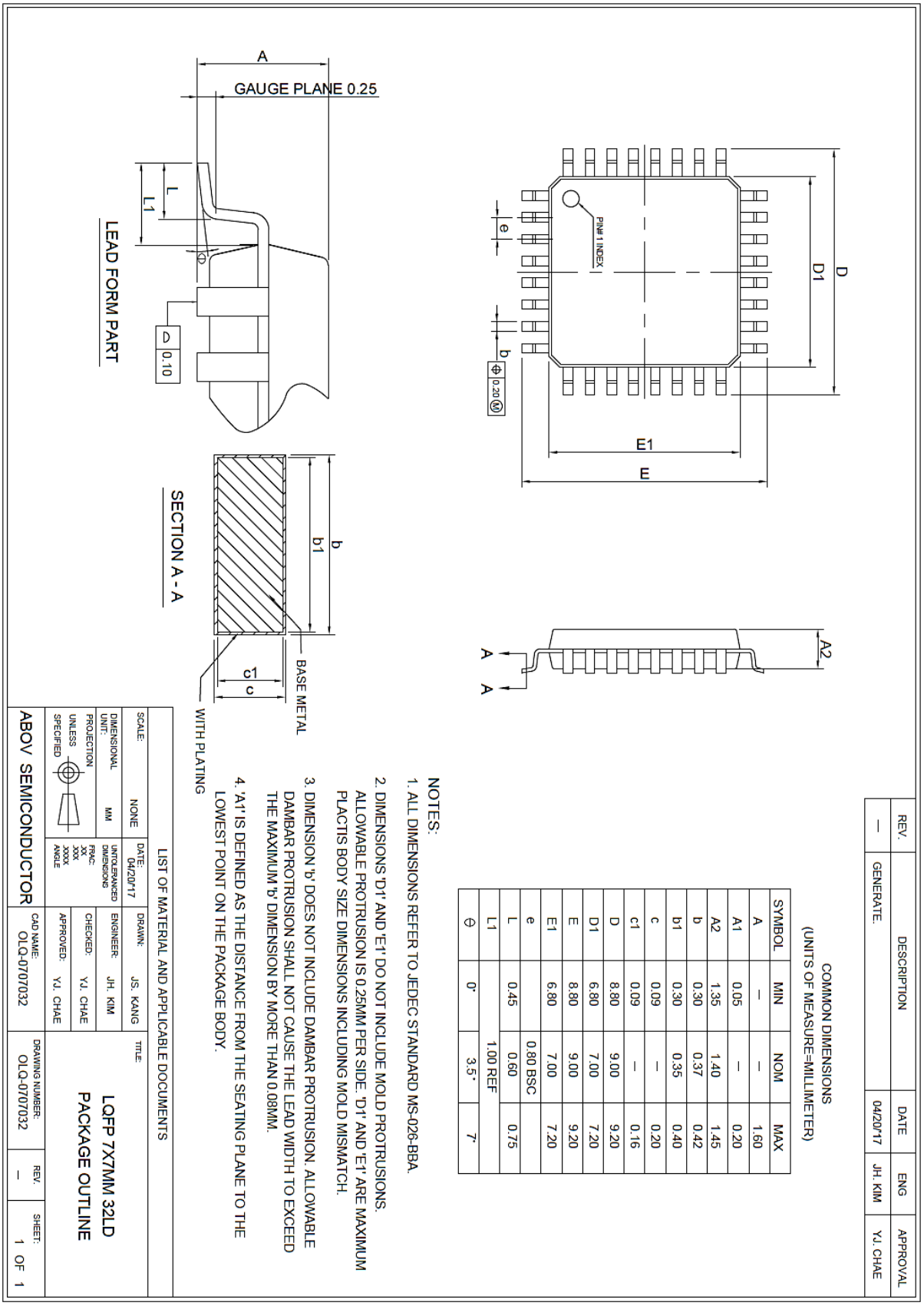


Figure 4.3 32-Pin LQFP Package

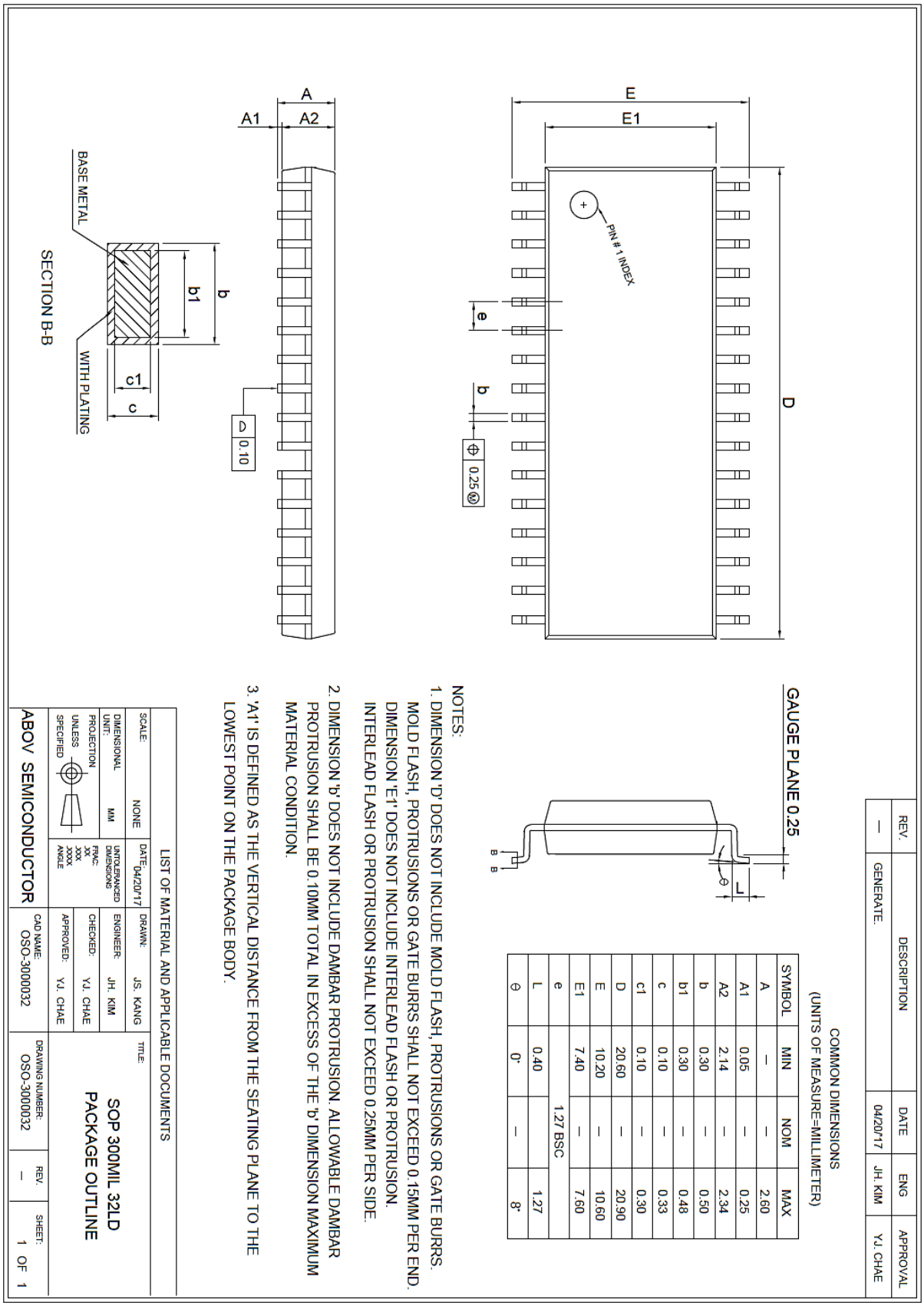


Figure 4.4 32-Pin SOP Package

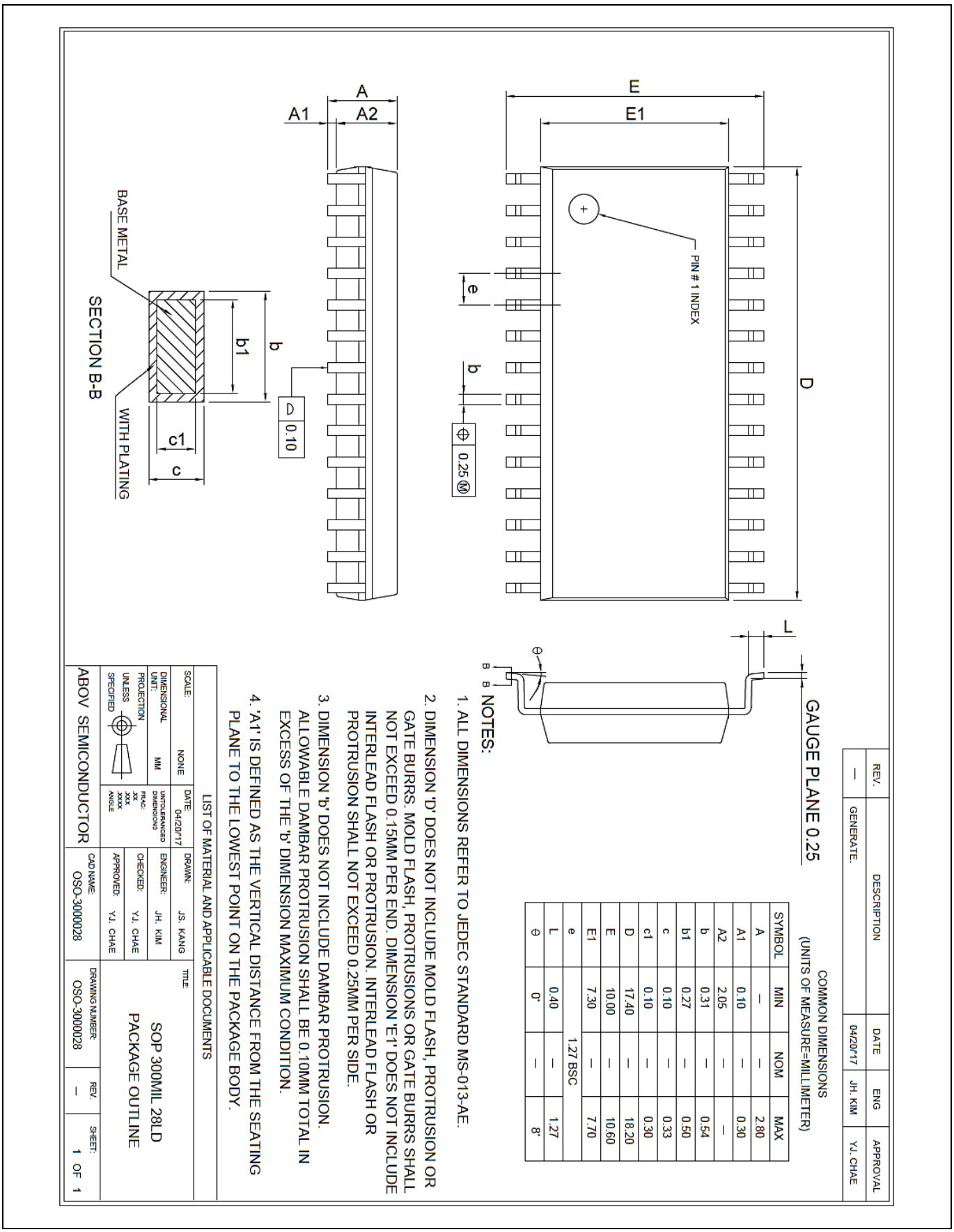


Figure 4.5 28-Pin SOP Package

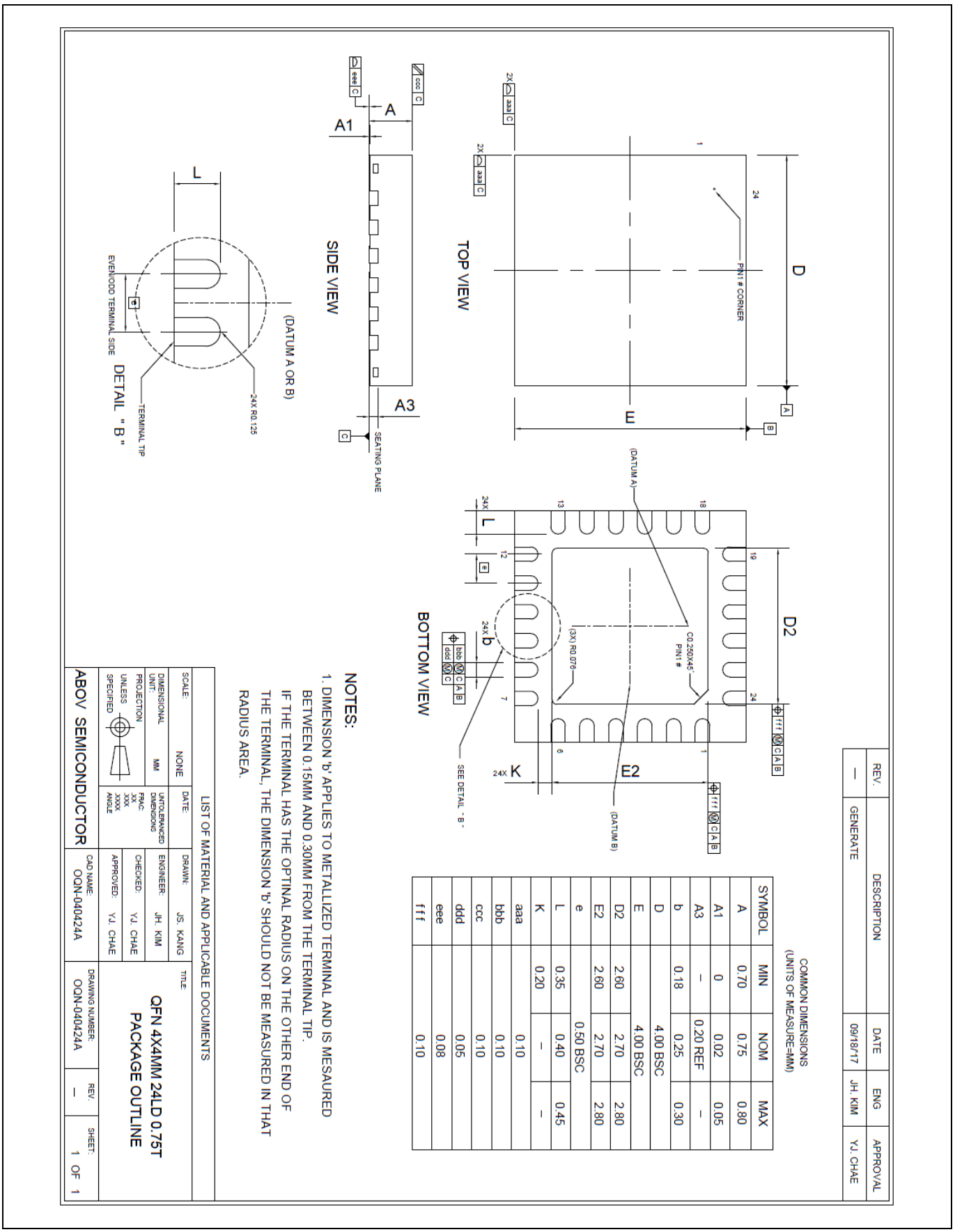


Figure 4.6 24-Pin QFN Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P05 – P07 are not in the 24-pin package.	Input	EC3/DSDA
P01				T3O/DSCL
P02				AN0/AVREF/EINT0/T4O/PWM4AA
P03				SEG26/AN1/EINT1/PWM4AB
P04				SEG25/AN2/EINT2/PWM4BA
P05				SEG24/AN3/EINT3/PWM4BB
P06				SEG23/AN4/EINT4/PWM4CA
P07				SEG22/AN5/EINT5/PWM4CB
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P14 – P17 are not in the 32-pin package. The P13 – P17 are not in the 28-pin package. The P14 – P17 are not in the 24-pin package.	Input	SEG14/AN13/RXD1/SCL1/MISO1
P11				SEG15/AN12/EINT12/T2O/PWM2O
P12				SEG16/AN11/EINT11/T1O/PWM1O
P13				SEG17/AN10/EC1/BUZO
P14				SEG18/AN9/MOSI2
P15				SEG19/AN8/MISO2
P16				SEG20/AN7/EINT7/SCK2
P17				SEG21/AN6/EINT6/SS2
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P23 – P25 are not in the 32-pin package. The P22 – P27 are not in the 28-pin package. The P20, P22 – P27 are not in the 24-pin package.	Input	SEG13/AN14/TXD1/SDA1/MOSI1
P21				SEG12/AN15/SCK1
P22				SEG11/SS1
P23				SEG10
P24				SEG9
P25				SEG8
P26				SEG7
P27				SEG6
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input, a push-pull output. A pull-up resistor can be specified in 1-bit unit. The P34 – P37 are only in the 32-pin package. The P34 – P37 are not in the 28-pin package. The P34 – P37 are not in the 24-pin package.	Input	COM7/SEG5
P31				COM6/SEG4
P32				COM5/SEG3
P33				COM4/SEG2
P34				COM3/SEG1
P35				COM2/SEG0
P36				COM1
P37				COM0
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P43 is not in the 32-pin package. The P43 is not in the 28-pin package. The P42 – P43 are not in the 24-pin package.	Input	VLC3/RXD0/SCL0/MISO0
P41				VLC2/TXD0/SDA0/MOSI0
P42				VLC1/SCK0
P43				VLC0/SS0

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input or a push-pull output. A pull-up resistor can be specified in 1-bit unit.	Input	XOUT
P51				XIN
P52				EINT8/EC0/BLNK
P53				SXIN/T0O/PWM0O
P54				SXOUT/EINT10
P55				RESETB
EINT0	I/O	External interrupt input and Timer 3 capture input	Input	P02/AN0/AVREF/T4O/PWM4AA
EINT1	I/O	External interrupt input and Timer 4 capture input	Input	P03/SEG26/AN1/PWM4AB
EINT2	I/O	External interrupt inputs	Input	P04/SEG25/AN2/PWM4BA
EINT3				P05/SEG24/AN3/PWM4BB
EINT4				P06/SEG23/AN4/PWM4CA
EINT5				P07/SEG22/AN5/PWM4CB
EINT6				P17/SEG21/AN6/SS2
EINT7				P16/SEG20/AN7/SCK2
EINT8				P52/EC0/BLNK
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P54/SXOUT
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P12/SEG16/AN11/T1O/PWM1O
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P11/SEG15/AN12/T2O/PWM2O
T0O	I/O	Timer 0 interval output	Input	P53/SXIN/PWM0O
T1O	I/O	Timer 1 interval output	Input	P12/SEG16/AN11/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P11/SEG15/AN12/EINT12/PWM2O
T3O	I/O	Timer 3 interval output	Input	P01/DSCL
T4O	I/O	Timer 4 interval output	Input	P02/AN0/AVREF/EINT0/PWM4AA
PWM0O	I/O	Timer 0 PWM output	Input	P53/SXIN/T0O
PWM1O	I/O	Timer 1 PWM output	Input	P12/SEG16/AN11/EINT11/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P11/SEG15/AN12/EINT12/T2O
PWM4AA	I/O	Timer 4 PWM outputs	Input	P02/AN0/AVREF/EINT0/T4O
PWM4AB				P03/SEG26/AN1/EINT1
PWM4BA				P04/SEG25/AN2/EINT2
PWM4BB				P05/SEG24/AN3/EINT3
PWM4CA				P06/SEG23/AN4/EINT4
PWM4CB				P07/SEG22/AN5/EINT5
BLNK	I/O	External sync signal input for 6-ch PWMs	Input	P52/EINT8/EC0
EC0	I/O	Timer 0 event count input	Input	P52/EINT8/BLNK
EC1	I/O	Timer 1 event count input	Input	P13/SEG17/AN10
EC3	I/O	Timer 3 event count input	Input	P00/DSDA

Table 5.2 Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
BUZO	I/O	Buzzer signal output	Input	P13/SEG17/AN10/EC1
SCK0	I/O	Serial 0 clock input/output	Input	P42/VLC1
SCK1	I/O	Serial 1 clock input/output	Input	P21/SEG12/AN15
SCK2	I/O	Serial 2 clock input/output	Input	P16/SEG20/AN7/EINT7
MOSI0	I/O	SPI 0 master output, slave input	Input	P41/VLC2/TXD0/SDA0
MOSI1	I/O	SPI 1 master output, slave input	Input	P20/SEG13/AN14/TXD1/SDA1
MOSI2	I/O	SPI 2 master output, slave input	Input	P14/SEG18/AN9
MISO0	I/O	SPI 0 master input, slave output	Input	P40/VLC3/RXD0/SCL0
MISO1	I/O	SPI 1 master input, slave output	Input	P10/SEG14/AN13/RXD1/SCL1
MISO2	I/O	SPI 2 master input, slave output	Input	P15/SEG19/AN8
SS0	I/O	SPI 0 slave select input	Input	P43/VLC0
SS1	I/O	SPI 1 slave select input	Input	P22/SEG11
SS2	I/O	SPI 2 slave select input	Input	P17/SEG21/AN6/EINT6
TXD0	I/O	UART 0 data output	Input	P41/VLC2/SDA0/MOSI0
TXD1	I/O	UART 1 data output	Input	P20/SEG13/AN14/SDA1/MOSI1
RXD0	I/O	UART 0 data input	Input	P40/VLC3/SCL0/MISO0
RXD1	I/O	UART 1 data input	Input	P10/SEG14/AN13/SCL1/MISO1
SCL0	I/O	I2C 0 clock input/output	Input	P40/VLC3/RXD0/MISO0
SCL1	I/O	I2C 1 clock input/output	Input	P10/SEG14/AN13/RXD1/MISO1
SDA0	I/O	I2C 0 data input/output	Input	P41/VLC2/TXD0/MOSI0
SDA1	I/O	I2C 1 data input/output	Input	P20/SEG13/AN14/TXD1/MOSI1
AVREF	I/O	A/D converter reference voltage	Input	P02/AN0/EINT0/T4O/PWM4AA
AN0	I/O	A/D converter analog input channels	Input	P02/AVREF/EINT0/T4O/PWM4AA
AN1				P03/SEG26/EINT1/PWM4AB
AN2				P04/SEG25/EINT2/PWM4BA
AN3				P05/SEG24/EINT3/PWM4BB
AN4				P06/SEG23/EINT4/PWM4CA
AN5				P07/SEG22/EINT5/PWM4CB
AN6				P17/SEG21/EINT6/SS2
AN7				P16/SEG20/EINT7/SCK2
AN8				P15/SEG19/MISO2
AN9				P14/SEG18/MOSI2
AN10				P13/SEG17/EC1
AN11				P12/SEG16/EINT11/T1O/PWM1O
AN12				P11/SEG15/EINT12/T2O/PWM2O
AN13				P10/SEG14/RXD1/SCL1/MISO1
AN14				P20/SEG13/TXD1/SDA1/MOSI1
AN15				P21/SEG12/SCK1

Table 5.3 Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
VLC0	I/O	LCD bias voltage pins	Input	P43/SS0
VLC1				P42/SCK0
VLC2				P41/TXD0/SDA0/MOSI0
VLC3				P40/RXD0/SCL0/MISO0
COM0 COM1	I/O	LCD common signal outputs	Input	P37–P36
COM2– COM3				P35–P34/SEG0–SEG1
COM4– COM7				P33–P30/SEG2–SEG5
SEG0– SEG1	I/O	LCD segment signal outputs	Input	P35–P34/COM2–COM3
SEG2– SEG5				P33–P30/COM4–COM7
SEG6– SEG10				P27–P23
SEG11				P22/SS1
SEG12				P21/SCK1/AN15
SEG13				P20/AN14/TXD1/SDA1/MOSI1
SEG14				P10/AN13/RXD1/SCL1/MISO1
SEG15				P11/AN12/EINT12/T2O/PWM2O
SEG16				P12/AN11/EINT11/T1O/PWM1O
SEG17				P13/AN10/EC1
SEG18				P14/AN9/MOSI2
SEG19				P15/AN8/MISO2
SEG20				P16/AN7/EINT7/SCK2
SEG21				P17/AN6/EINT6/SS2
SEG22				P07/AN5/EINT5/PWM4CB
SEG23				P06/AN4/EINT4/PWM4CA
SEG24				P05/AN3/EINT3/PWM4BB
SEG25				P04/AN2/EINT2/PWM4BA
SEG26				P03/AN1/EINT1/PWM4AB

Table 5.4 Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P55
DSDA	I/O	In-system programming data input/output	Input	P00/EC3
DSCL	I/O	In-system programming clock input	Input	P01/T3O
XIN	I/O	Main oscillator pins	Input	P51
XOUT				P50
SXIN	I/O	Sub oscillator pins	Input	P53/T0O/PWM0O
SXOUT				P54/EINT10
VDD, VSS	–	Power input pins	–	–

Table 5.5 Normal Pin Description (conclude)

NOTE)

1. The P14–P17, P23–P25, P34–P37 and P43 are not in the 32-pin package.
2. The P13–P17, P22–P27, P34–P37 and P43 are not in the 28-pin package.
3. The P05–P07, P14–P17, P20, P22–P27, P34–P37 and P42-P43 are not in the 24-pin package.
4. The P55/RESETB pin is configured as one of the P55 and RESETB pin by the “CONFIGURE OPTION.”
5. If the P00/EC3/DSDA and P01/T3O/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
6. The P00/EC3/DSDA and P01/T3O/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
7. The P50/XOUT, P51/XIN, P53/SXIN/T0O/PWM0O and P54/SXOUT/EINT10 pins are configured as a function pin by software control.

6 Port Structures

6.1 General Purpose I/O Port

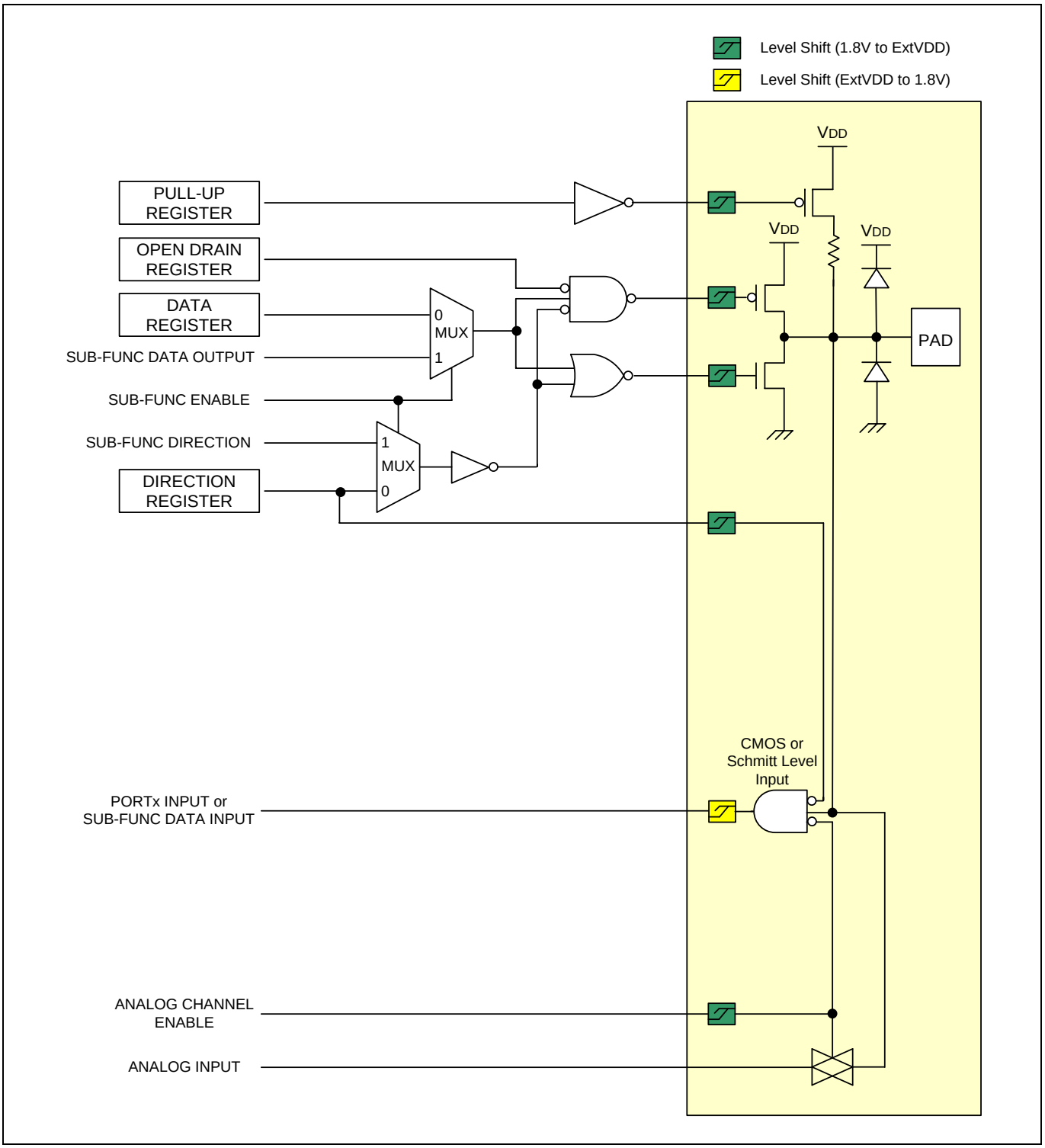


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

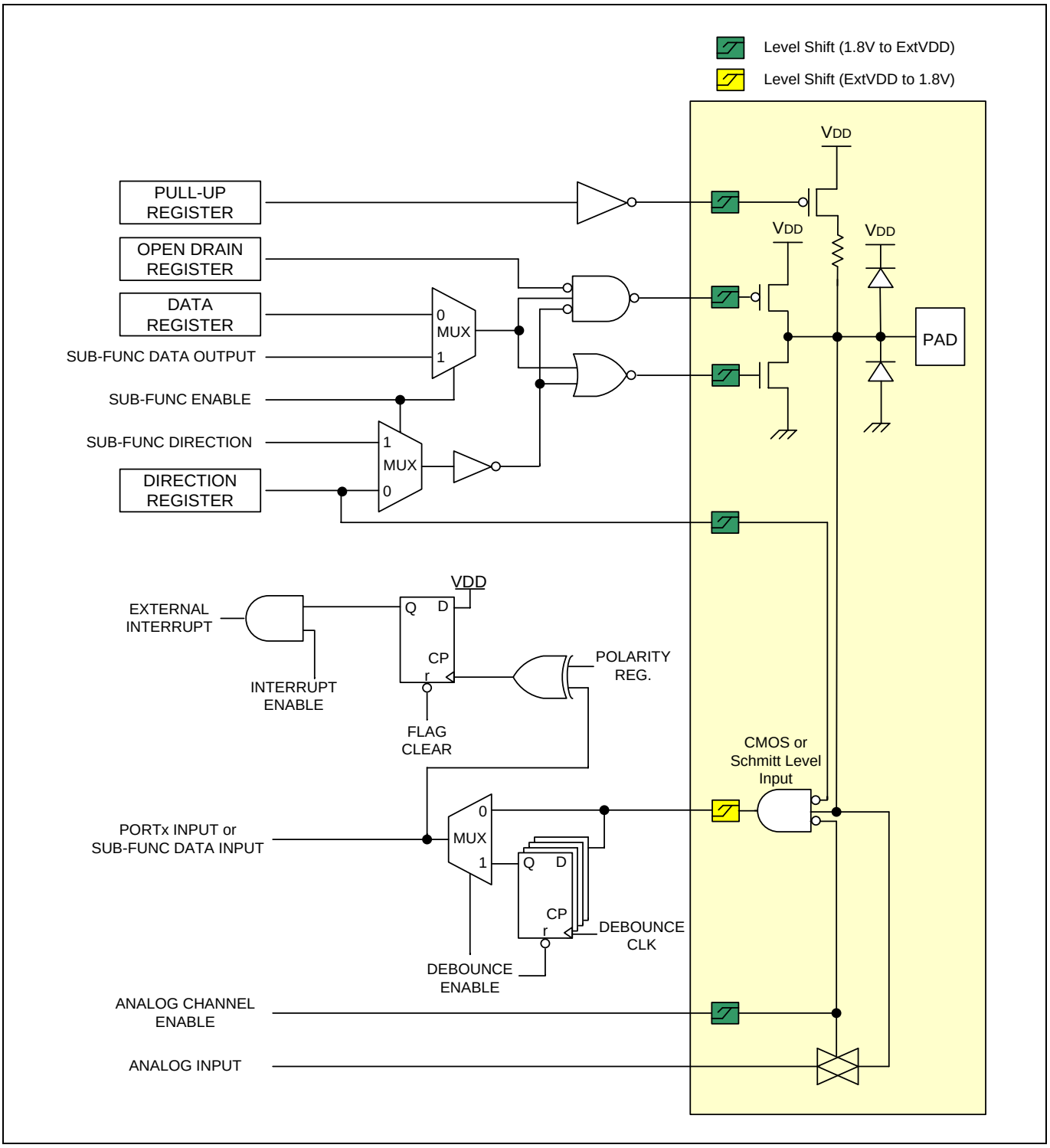


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A = -40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 32 ~ 38kHz	Sub Crystal	2.2	–	5.5	V
		f_X= 0.4 ~ 4.2MHz	Main Crystal	2.2	–	5.5	
		f_X= 0.4 ~ 8.5MHz		2.7	–	5.5	
		f_X= 0.5 ~ 16MHz	Internal RC	2.2	–	5.5	
Operating Temperature	T_{OPR}	VDD=2.2~5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–-	12	–	bit
Integral Non-Linear	INL	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±6	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	12-bit resolution, 8MHz		20	–	–	us
Analog Input Voltage	V_{AIN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		2.2	–	VDD	
Analog Input Leakage Current	I_{AIN}	AVREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.7V, the ADC resolution is worse.

7.4 Power-On Reset Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.4 Power-on Reset Characteristics

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.85V		–	1.85	2.15	V
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

Table 7.5 LVR and LVI Characteristics

7.6 High Internal RC Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.2 – 5.5V		–	16	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -20°C to +85°C				±2.5	
		T_A = -40°C to +85°C				±3.5	
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	T_{HFS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7.6 High Internal RC Oscillator Characteristics

NOTE)

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.7 Internal WDTRC Oscillator Characteristics

7.8 LCD Voltage Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
LCD Voltage	V_{LC0}	LCD contrast disabled,1/4 bias		Typx0.95	VDD	Typx1.05	V
		LCD contrast enabled, 1/4 bias, RLCD1, No panel load	LCDCCR=00H	Typx0.9	VDDx16/31	Typx1.1	V
			LCDCCR=01H		VDDx16/30		
			LCDCCR=02H		VDDx16/29		
			LCDCCR=03H		VDDx16/28		
			LCDCCR=04H		VDDx16/27		
			LCDCCR=05H		VDDx16/26		
			LCDCCR=06H		VDDx16/25		
			LCDCCR=07H		VDDx16/24		
			LCDCCR=08H		VDDx16/23		
			LCDCCR=09H		VDDx16/22		
			LCDCCR=0AH		VDDx16/21		
			LCDCCR=0BH		VDDx16/20		
			LCDCCR=0CH		VDDx16/19		
			LCDCCR=0DH		VDDx16/18		
			LCDCCR=0EH		VDDx16/17		
			LCDCCR=0FH		VDDx16/16		
LCD Mid Bias Voltage(note)	V_{LC1}	VDD=2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load		Typx0.9	3/4xVLC0	Typx1.1	V
	V_{LC2}			Typx0.9	2/4xVLC0	Typx1.1	
	V_{LC3}			Typx0.9	1/4xVLC0	Typx1.1	
LCD Driver Output Impedance	R_{LO}	VLCD=3V, ILOAD=±10uA		–	5	10	kΩ
LCD Bias Dividing Resistor	R_{LCD1}	T_A = 25°C		40	60	80	
	R_{LCD2}			80	120	160	

Table 7.8 LCD Voltage Characteristics

NOTE)

1. It is middle output voltage when the VDD and the V_{LC0} node are connected.

7.9 DC Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V, f_{XIN} = 8.0MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0, P1,P5, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1,P5, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	V
Output High Voltage	V_{OH}	VDD=4.5V, I_{OH}=-2mA, All output ports;		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 10mA; All output ports except V_{OL2}		–	–	1.0	
	V_{OL2}	VDD=4.5V, I_{OL}= 15mA; P1		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25°C, VDD=5V		2500	5000	10000	
Supply Current	I_{DD1} (RUN)	f_{XIN}= 8MHz	VDD= 5V±10%	–	2.6	5.2	mA
		f_{XIN}= 4MHz	VDD= 3V±10%	–	1.2	2.4	
		f_{IRC}= 16MHz	VDD= 5V±10%	–	3.0	6.0	
	I_{DD2} (IDLE)	f_{XIN}= 8MHz	VDD= 5V±10%	–	1.8	3.6	mA
		f_{XIN}= 4MHz	VDD= 3V±10%	–	0.8	1.6	
		f_{IRC}= 16MHz	VDD= 5V±10%	–	1.5	3.0	
	I_{DD3}	f_{XIN}=32.768kHz VDD= 3V±10% T_A= 25°C	Sub RUN	–	90.0	180.0	uA
	I_{DD4}		Sub IDLE	–	8.0	16.0	uA
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	3.0	uA

Table 7.9 DC Characteristics

NOTE)

1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{IRC} is an internal RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.10 AC Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB Input Low Width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt Input High, Low Width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5V (n= 0, 1, 3)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5V (n= 0, 1, 3)	20	–	–	

Table 7.10 AC Characteristics

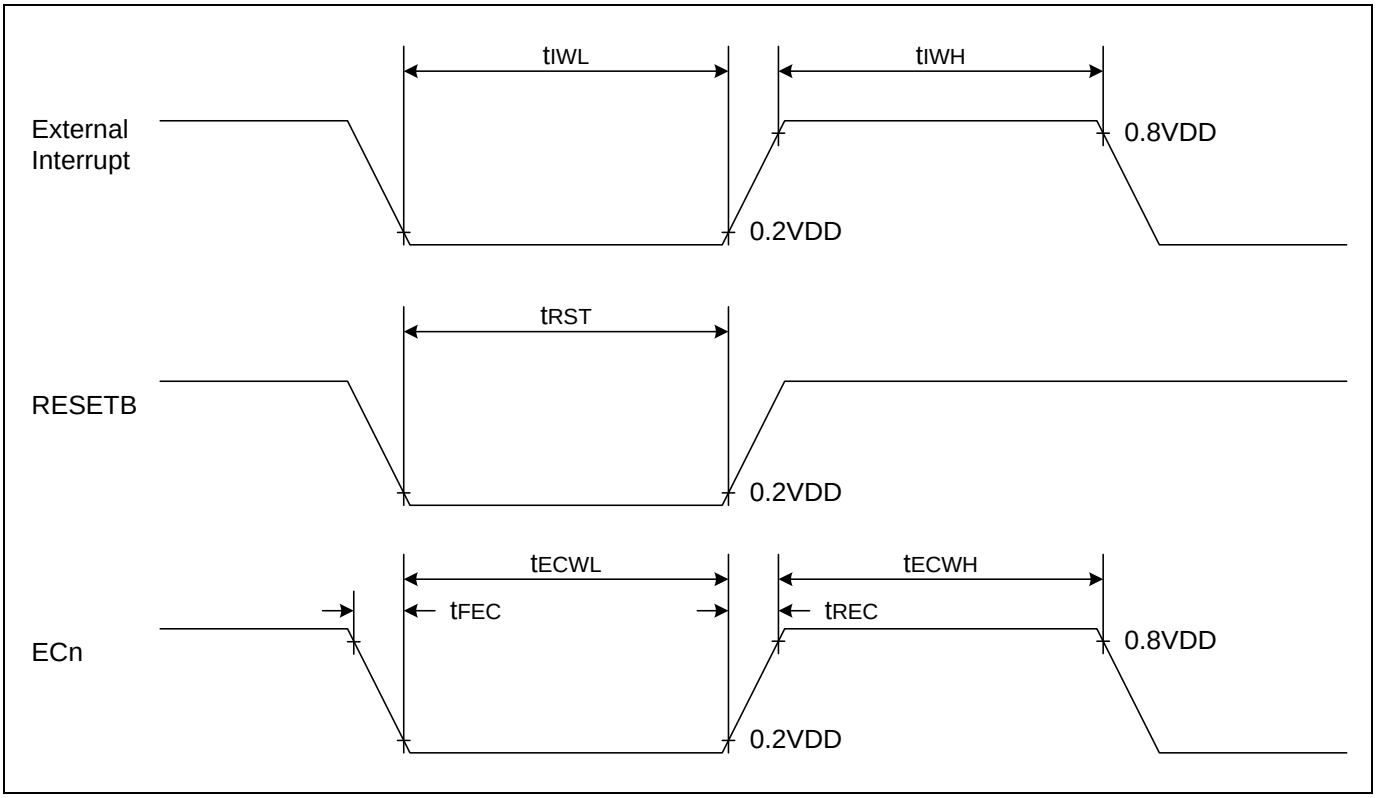


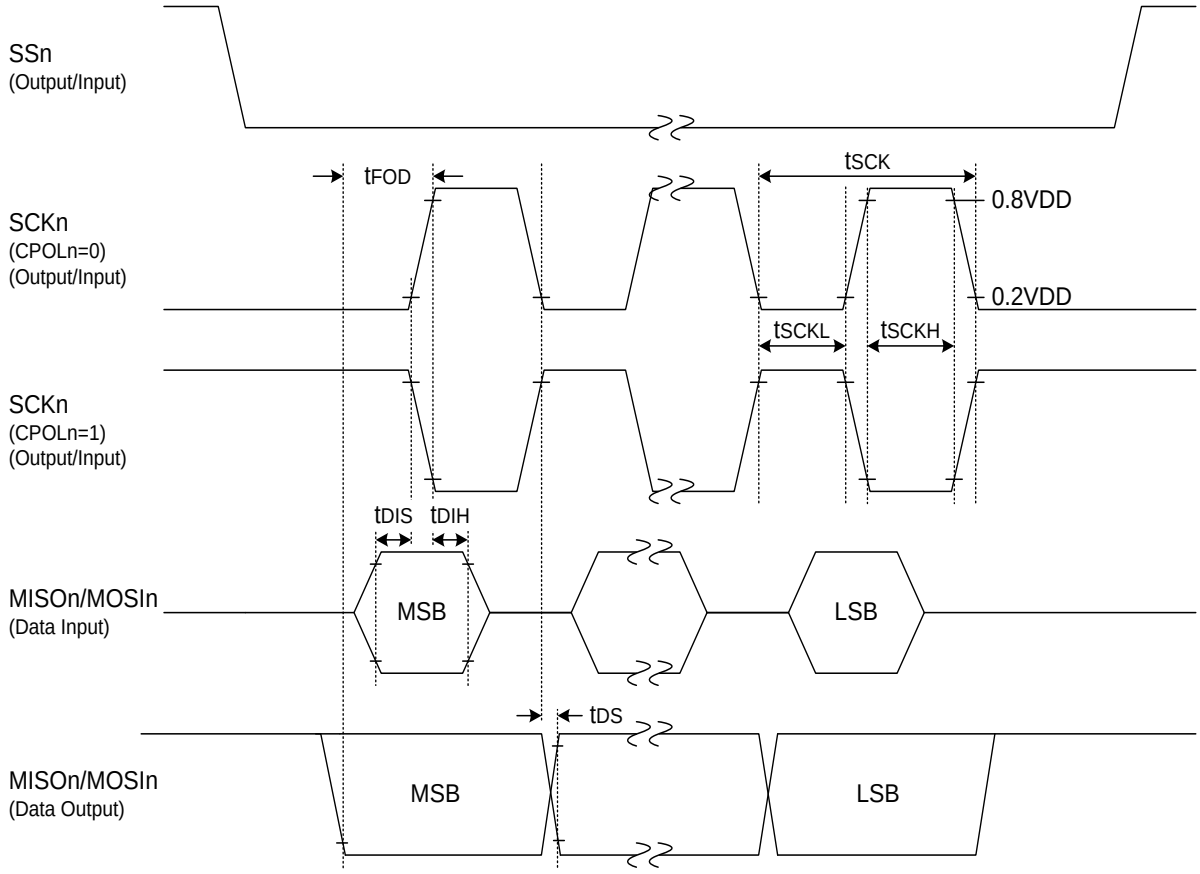
Figure 7.1 AC Timing

7.11 SPI0/1/2 Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	100	–	–	
Input Hold Time	t_{DIH}	–	150	–	–	

Table 7.11 SPI0/1/2 Characteristics



NOTE)

1. n = 0, 1 and 2

Figure 7.2 SPI0/1/2 Timing

7.12 UART0/1 Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, f_{XIN} = 8MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	$t_{CPU} \times 16$	2200	ns
Output data setup to clock rising edge	t_{S1}	810	$t_{CPU} \times 13$	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	$t_{CPU} \times 8$	1280	

Table 7.12 UART0/1 Characteristics

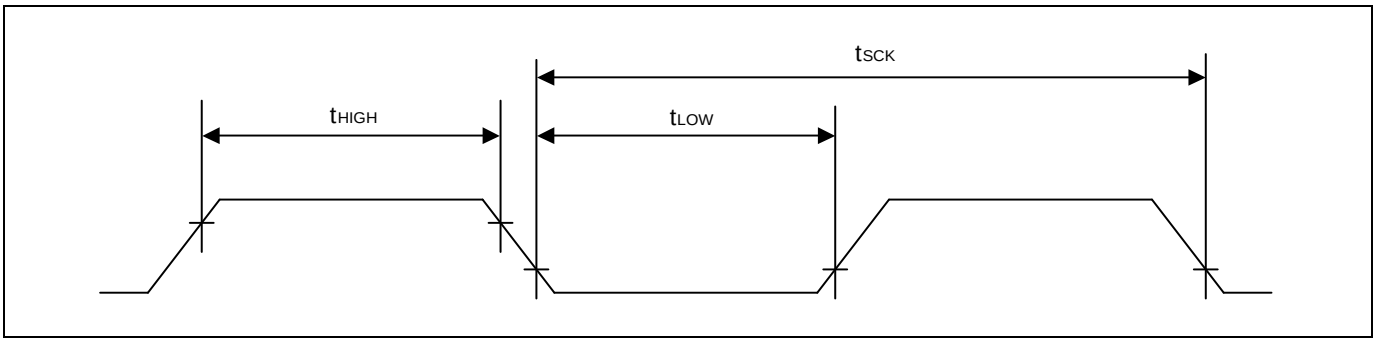


Figure 7.3 Waveform for UART0/1 Timing Characteristics

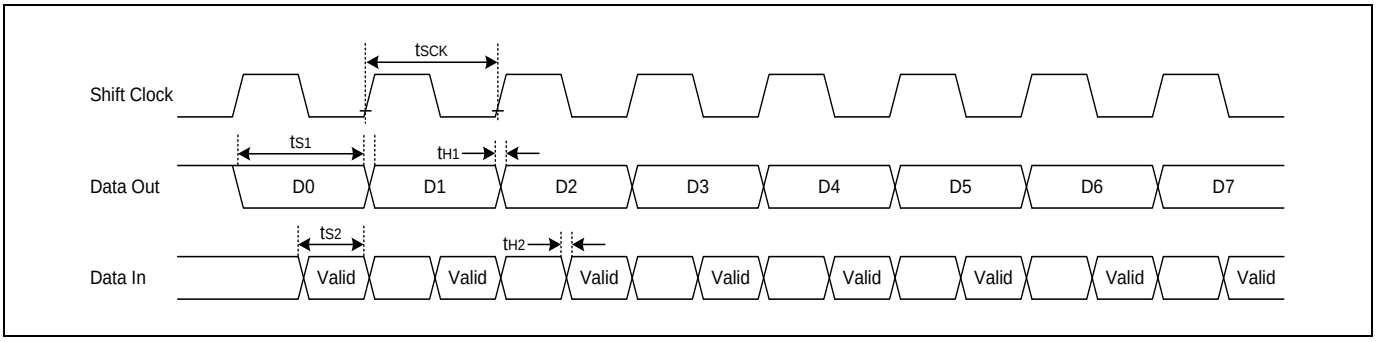


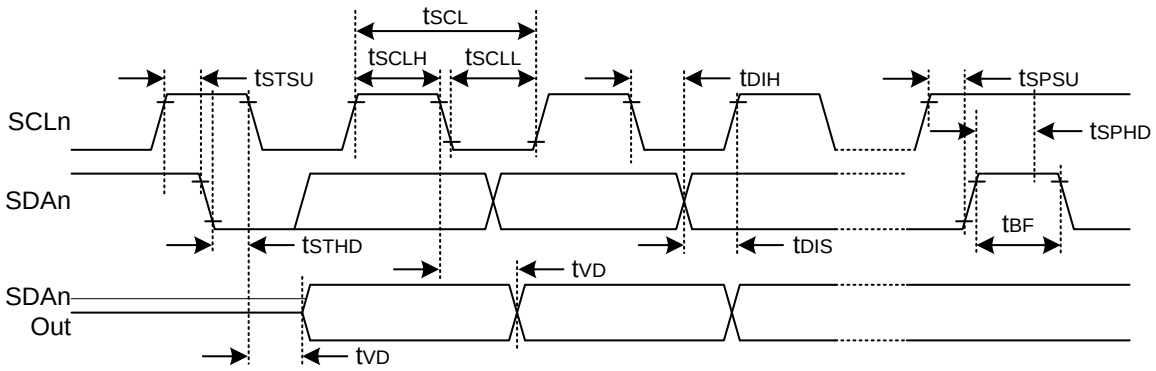
Figure 7.4 Timing Waveform for the UART0/1 Module

7.13 I2C0/1 Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.13 I2C0/1 Characteristics



NOTE)

1. n= 0 and 1

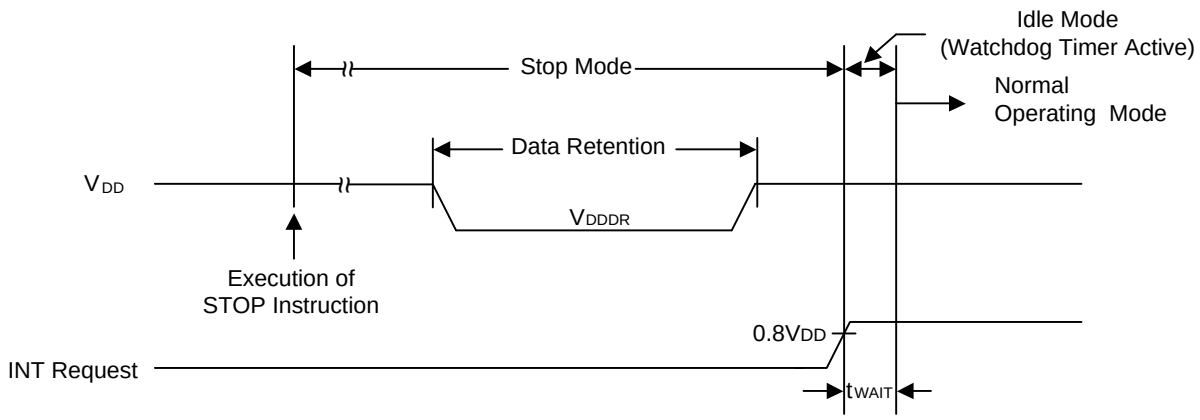
Figure 7.5 I2C0/1 Timing

7.14 Data Retention Voltage in Stop Mode

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

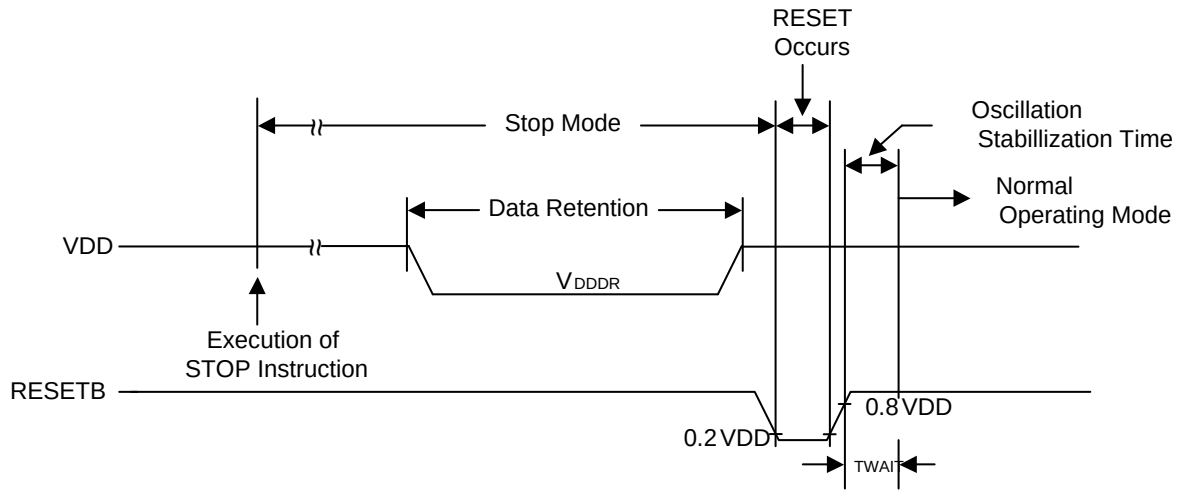
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDR} = 2.2V(T_A = 25°C), Stop mode	–	–	1	uA

Table 7.14 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.6 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 7.7 Stop Mode Release Timing when Initiated by RESETB

7.15 Internal Flash Rom Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	Sector 0 to 507	–	–	10,000	times
		Sector 508 to 511(256 bytes)	–	–	100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	years

Table 7.15 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.16 Input/Output Capacitance

(T_A = -40°C ~ +85°C, VDD = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.16 Input/Output Capacitance

7.17 Main Clock Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	8.5	
Ceramic Oscillator	Main oscillation frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	8.5	
External Clock	XIN input frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	8.5	

Table 7.17 Main Clock Oscillator Characteristics

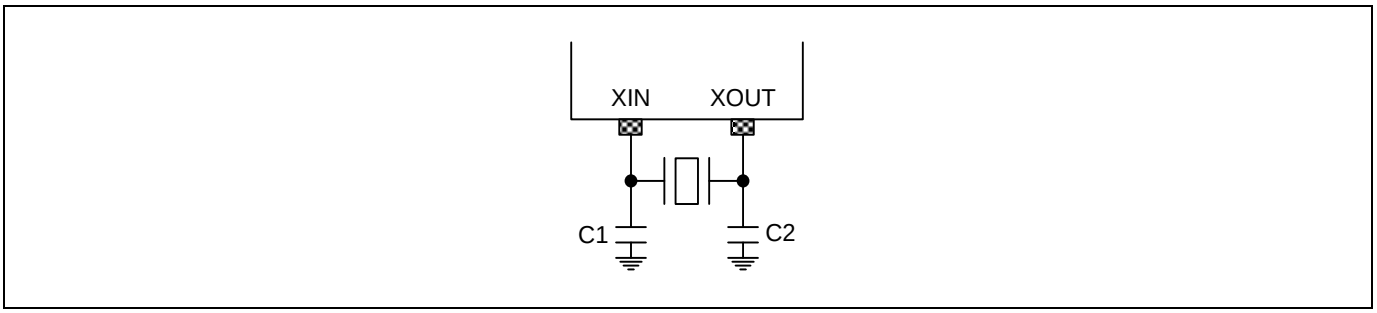


Figure 7.8 Crystal/Ceramic Oscillator

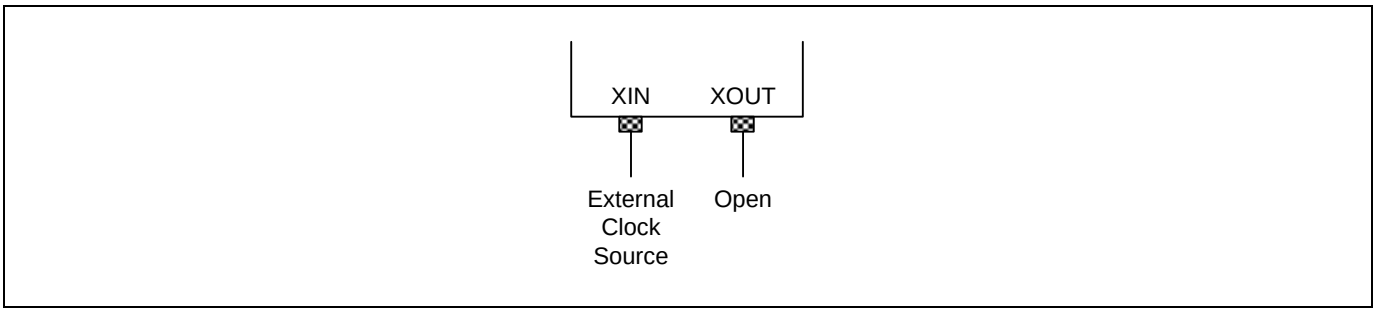


Figure 7.9 External Clock

7.18 Sub Clock Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	2.2V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

Table 7.18 Sub Clock Oscillator Characteristics

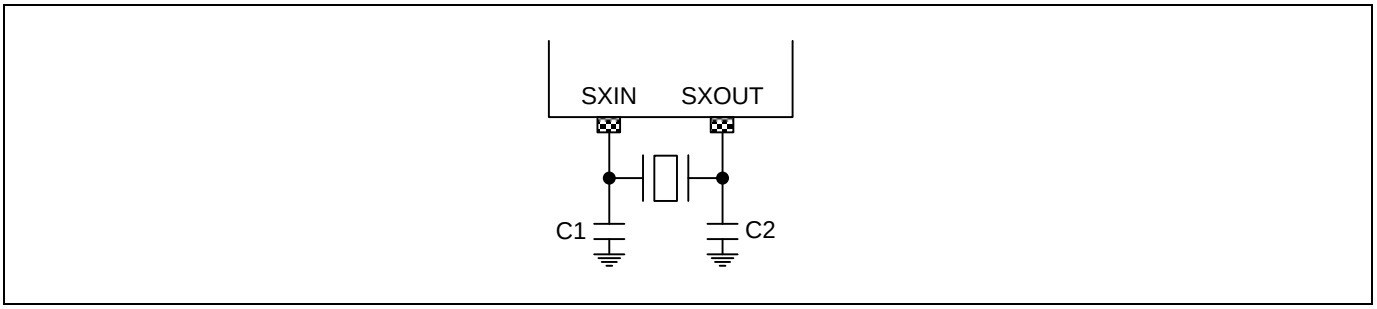


Figure 7.10 Crystal Oscillator

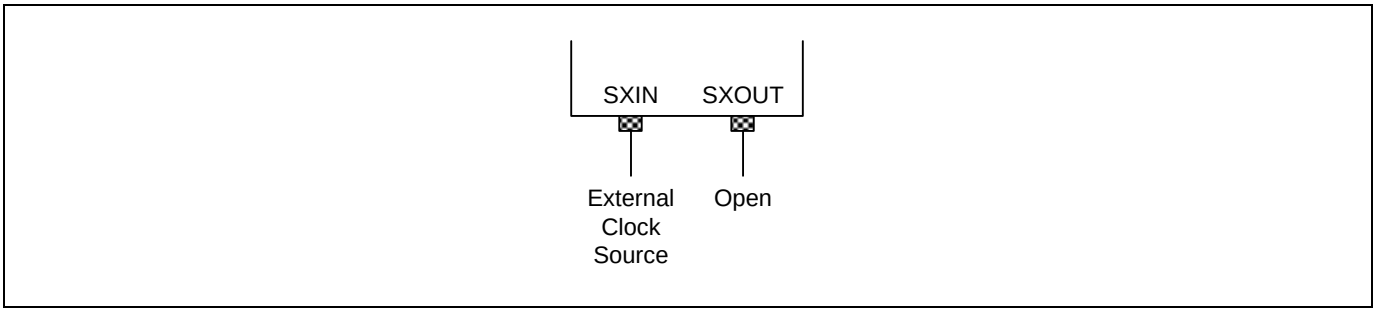


Figure 7.11 External Clock

7.19 Main Oscillation Stabilization Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 4MHz, VDD = 2.7V ~ 5.5V,	–	–	15	ms
	fx > 1MHz, VDD = 2.2V, T_A=-40°C			60	
Ceramic	-	–	–	10	ms
External Clock	f_{XIN} = 0.4 to 8.5MHz XIN input high and low width (t_{XH}, t_{XL})	58	–	1250	ns

Table 7.19 Main Oscillation Stabilization Characteristics

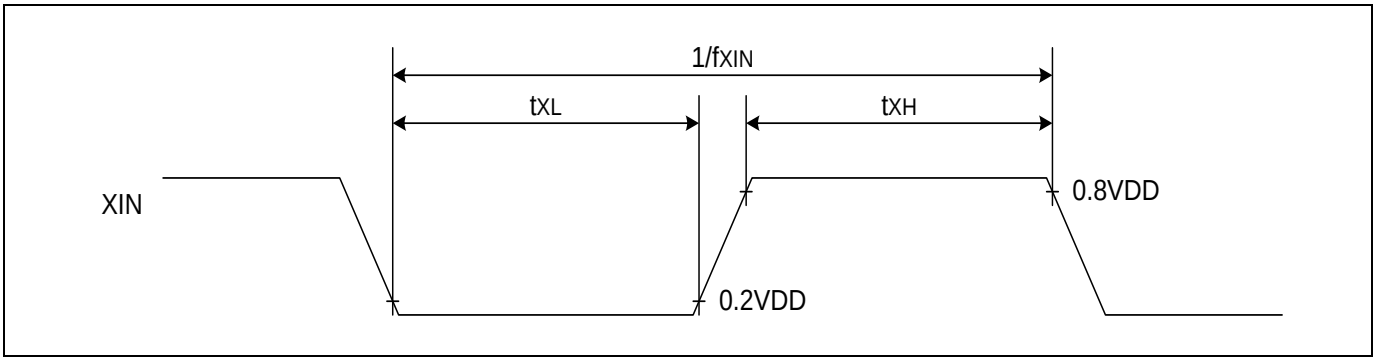


Figure 7.12 Clock Timing Measurement at XIN

7.20 Sub Oscillation Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

Table 7.20 Sub Oscillation Stabilization Characteristics

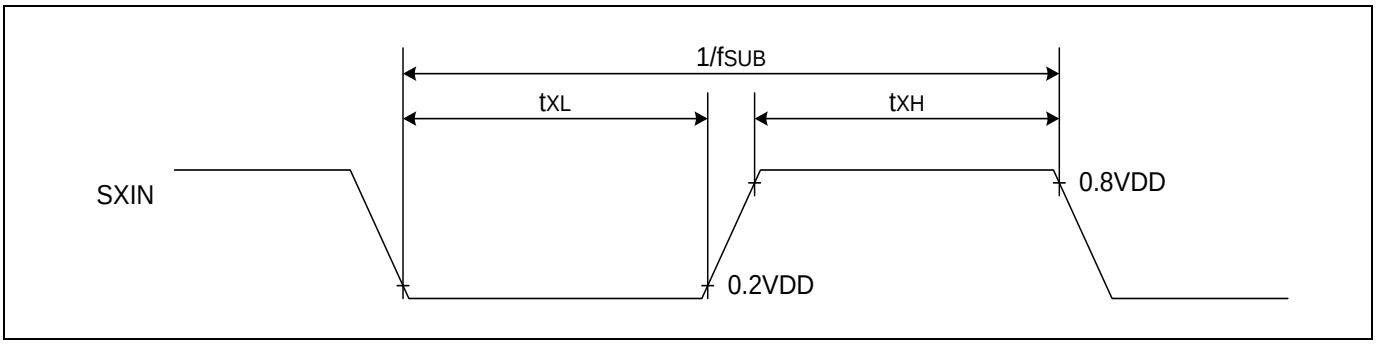


Figure 7.13 Clock Timing Measurement at SXIN

7.21 Operating Voltage Range

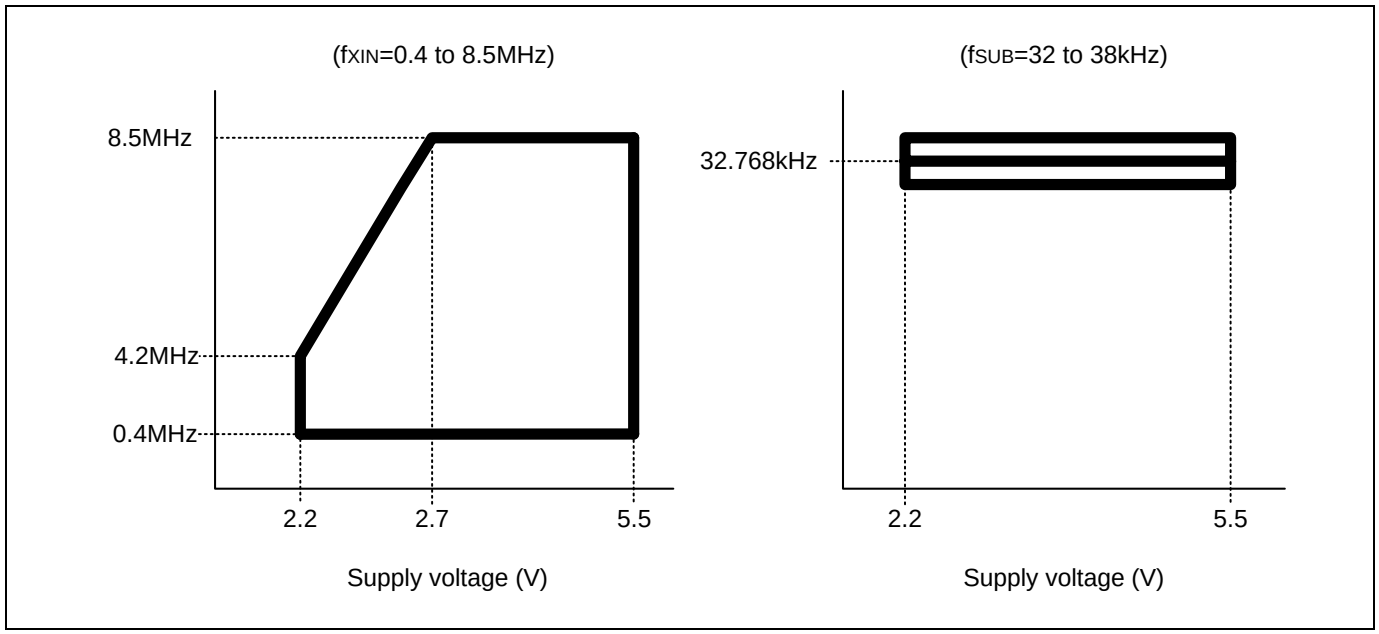


Figure 7.14 Operating Voltage Range

7.22 Recommended Circuit and Layout

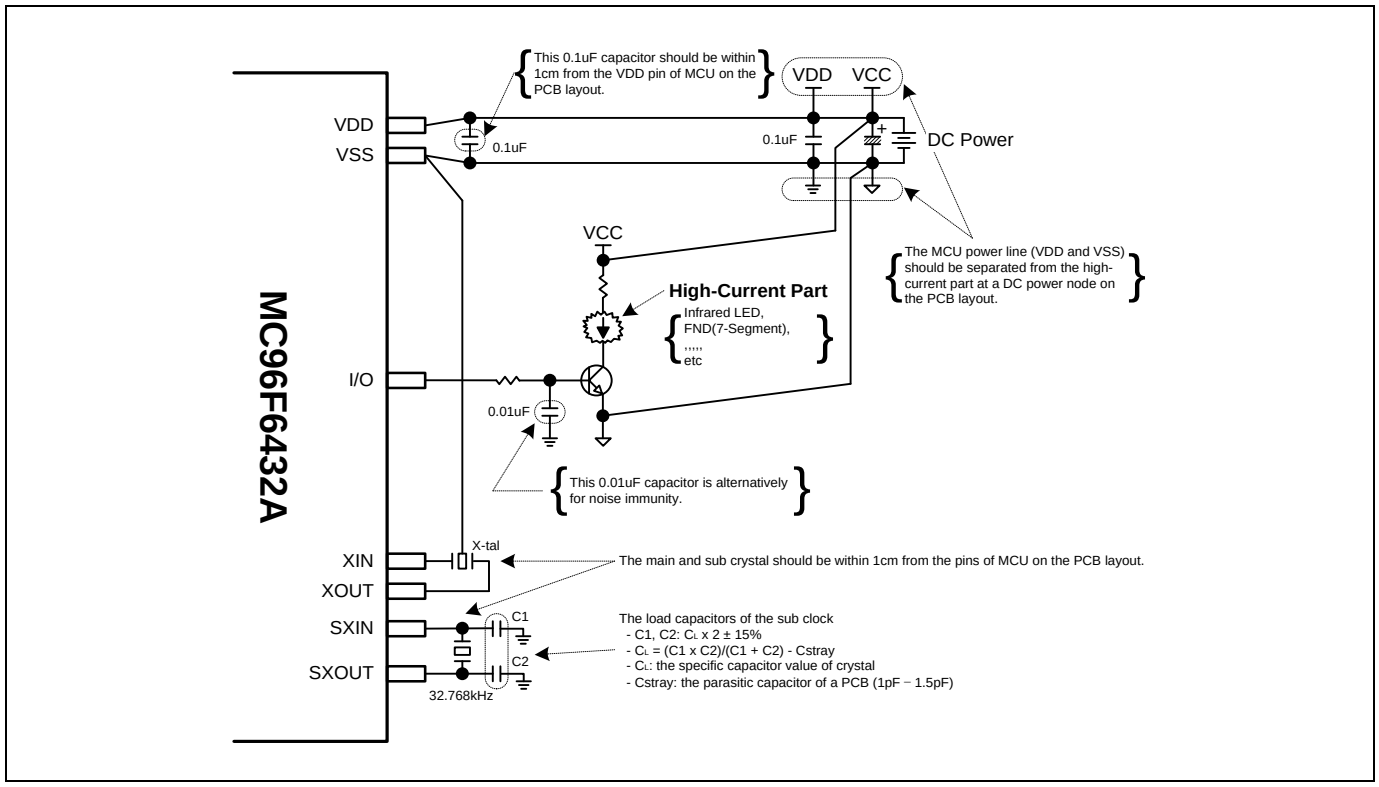
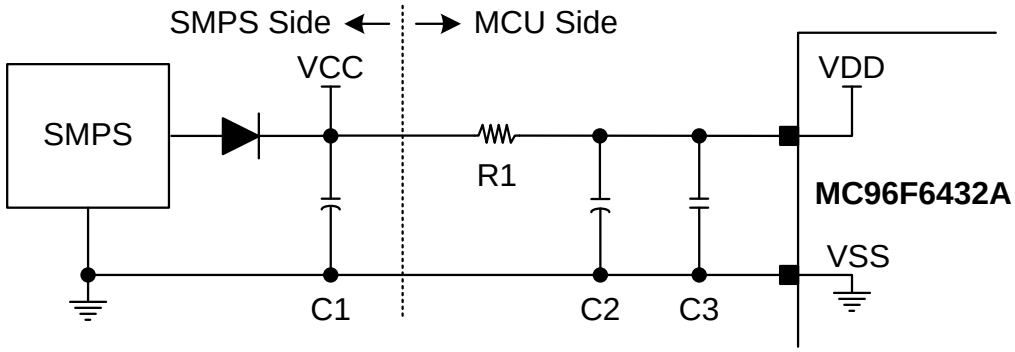


Figure 7.15 Recommended Circuit and Layout

7.23 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.16 Recommended Circuit and Layout with SMPS Power

7.24 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

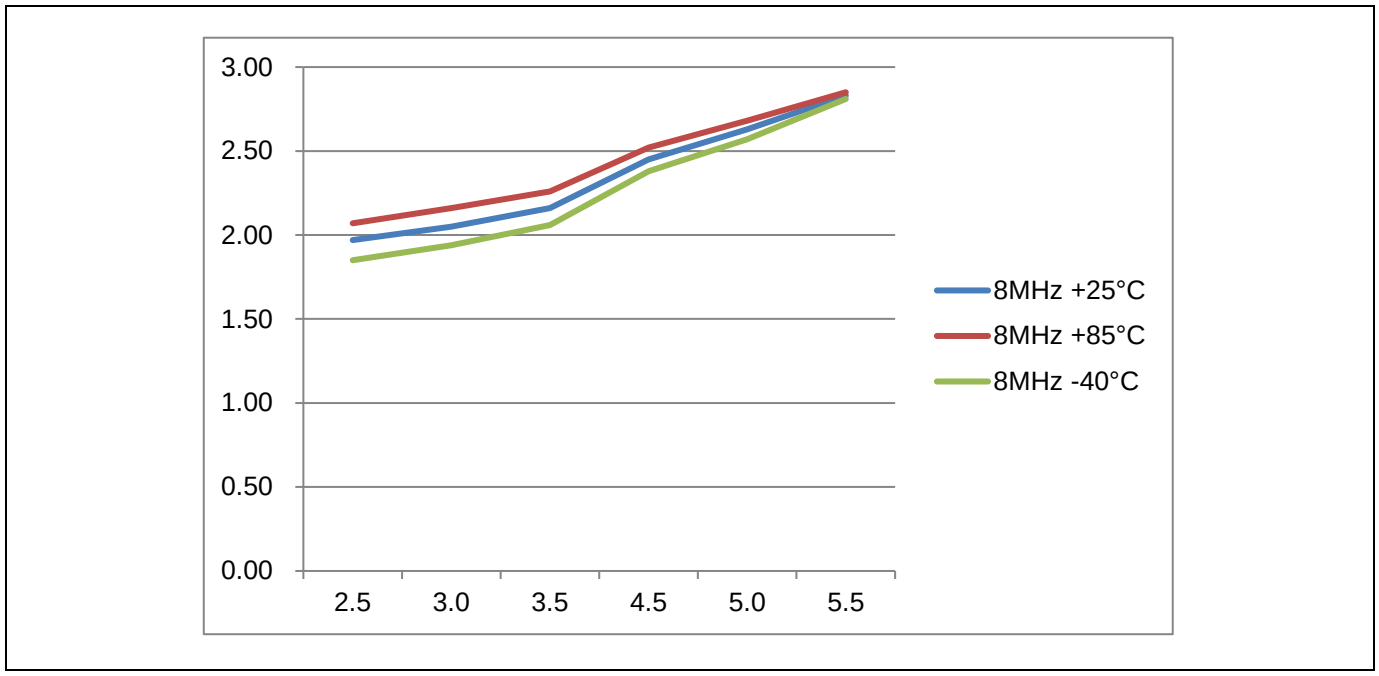


Figure 7.17 RUN (IDD1) Current

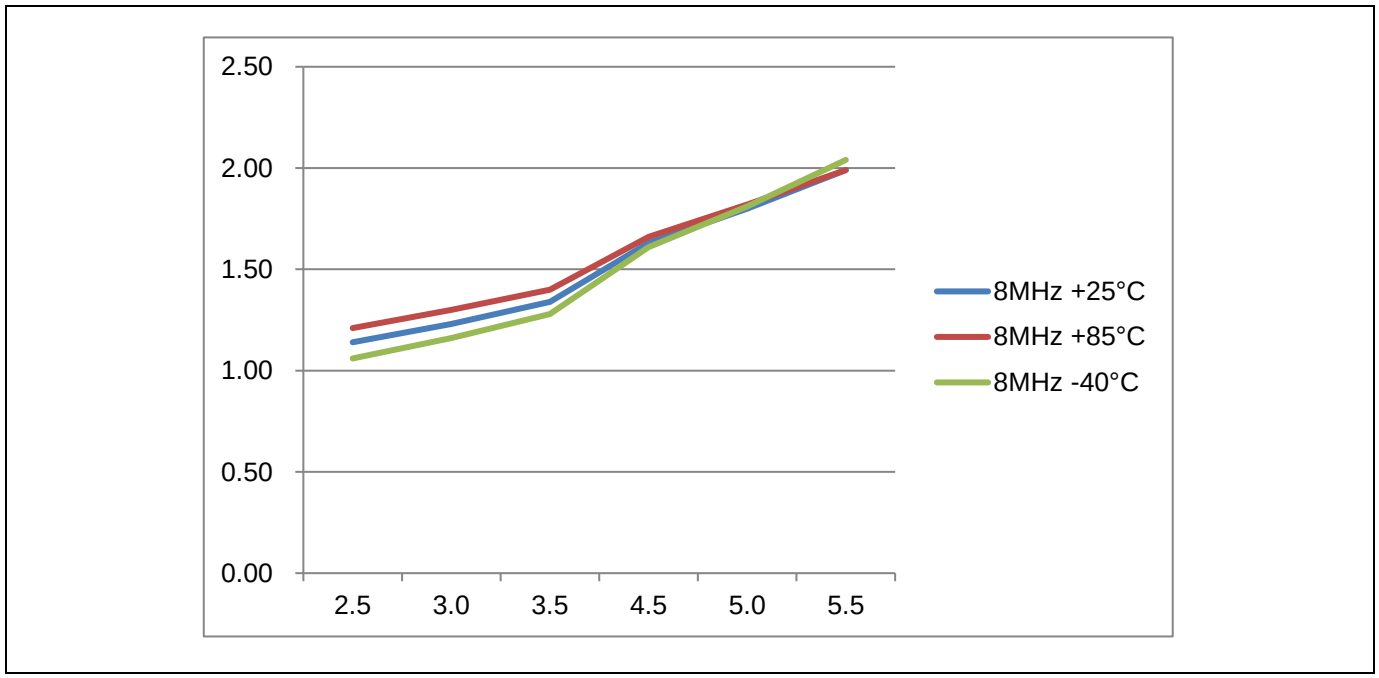


Figure 7.18 IDLE (IDD2) Current

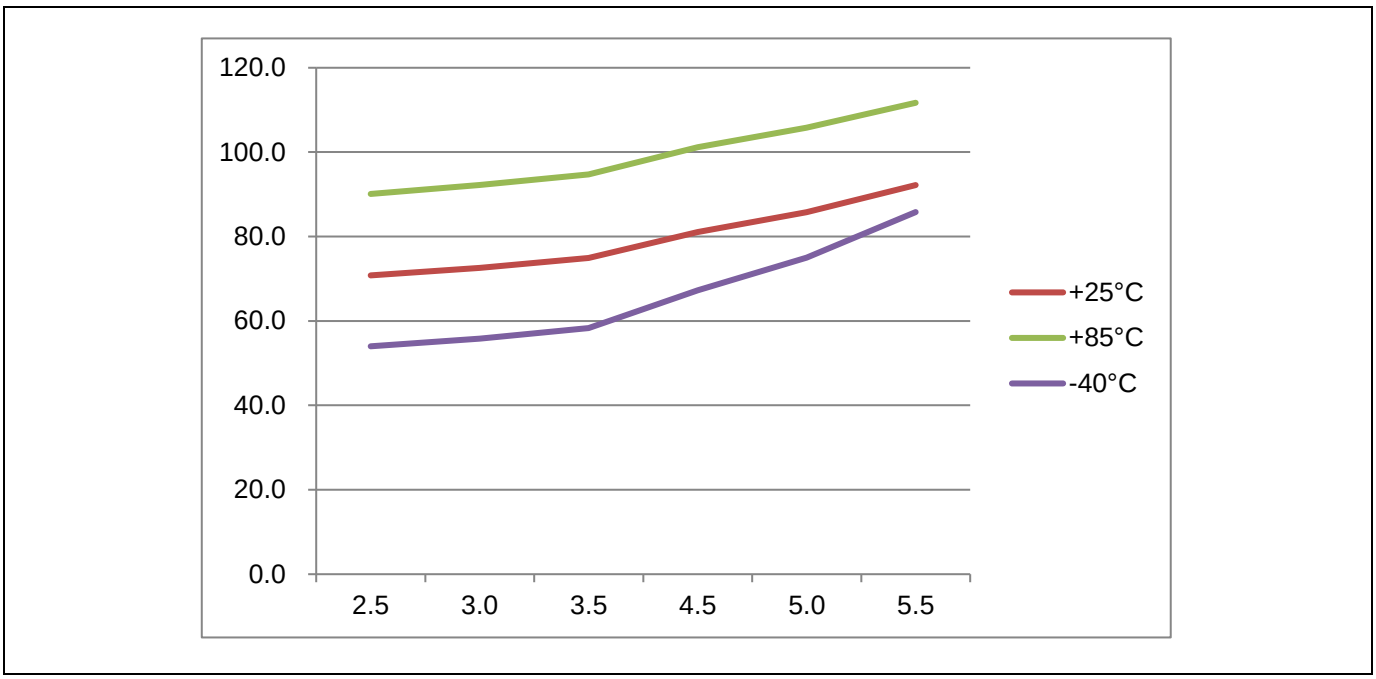


Figure 7.19 SUB RUN (IDD3) Current

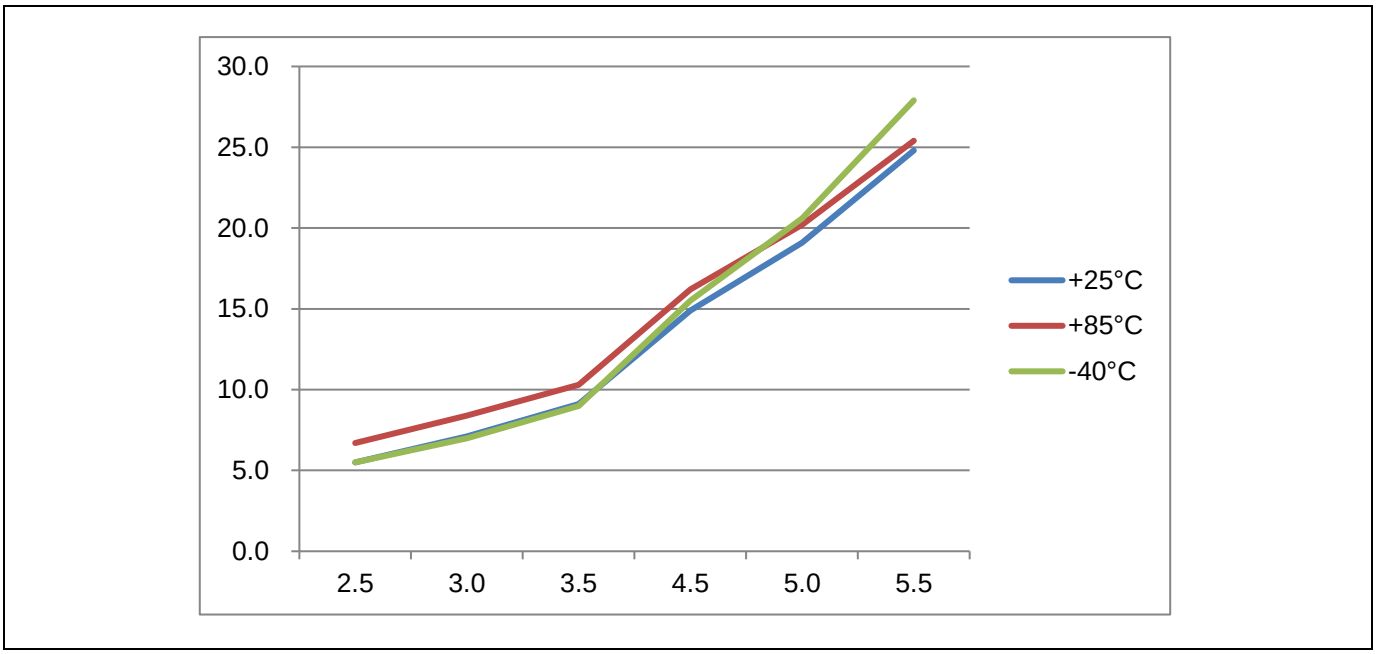


Figure 7.20 SUB IDLE (IDD4) Current

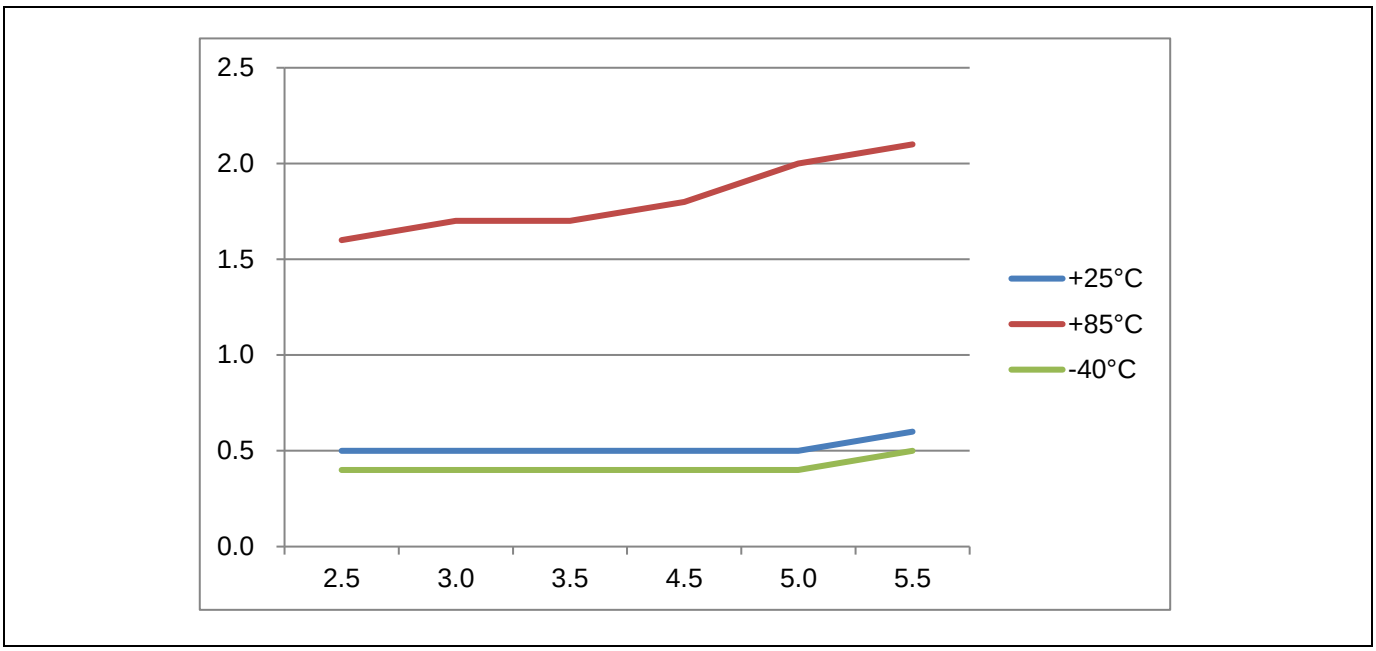


Figure 7.21 STOP (IDD5) Current

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