CMOS single-chip 8-bit MCU with BLDC Motor Driver

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 16Kbytes Flash Code Memory
  - 512bytes SRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 20 MHz RC oscillator (±2.0%,T_A= 0°C ~ +50 °C)
  - Watchdog Timer RC oscillator (5kHz)
- **Peripheral Features**
  - 10-bit Analog to Digital Converter (11 inputs)
  - OP-AMP
  - Analog Comparator (4Channels)
  - USI (USART + SPI + I2C)
  - Multiplier and Divider
  - Flash CRC Generator(16-Bit CRC Result)
- **I/O and Packages**
  - Up to 28 Programmable I/O lines with 32LQFP
  - 32LQFP, 24SSOP
- **Operating Conditions**
  - 2.0 V to 5.5V Wide Voltage Range
  - -40°C to +105°C Temperature Range
- **Application**
  - BLDC Motor Controller
  - Small Home Appliance

MC96FD316T

Data Sheet

V 1.2

Revised 12 September, 2017

Revision history

Version	Date	Revision list
1.0	2017.01.06	Published this book.
1.1	2017.01.09	Revised this book. Added the note on the flash memory erase and write. Updated Package diagrams.
1.2	2017.09.12	Revised this book. Added thermal resistance characteristics Updated package diagrams

Version 1.2

Published by FAE team

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1 Overview

1.1 Description

The MC96FD316T is an advanced CMOS 8-bit microcontroller with 16 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This offers the following features: 16 Kbytes of FLASH, 256 bytes of IRAM, 256 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 6-ch 16-bit PWM output, buzzer driving port, USI, 10-bit A/D converter, Analog Comparator, Operational Amplifier, Multiplier and Divider, Flash CRC Generator, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry.

Device Name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
MC96FD316TL	16 Kbytes	256 bytes	256 bytes	11 inputs	28	32LQFP
MC96FD316TS				7 inputs	20	24SSOP

Table 1.1 Ordering Information of MC96FD316T

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 16 Kbytes Flash with self-read and write capability
  - On chip debug and In-System Programming(ISP)
  - Parity bit check function for flash fail detection
  - Endurance : 10,000times
  - Retention : 10years
- **256 bytes IRAM**
- **256 bytes XRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 28ports (P0[5:0], P1, P2, P3[5:0])
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit × 1-ch
  - Watch Dog Timer (WDT)
    16Bit × 1ch
    50%, 75%, 100% Window
    5kHz internal RC oscillator
  - 8-bit × 1-ch (T0), 16-bit × 3-ch (T1/T2/T3)
- **Programmable Pulse Generation**
  - Pulse generation (by T1/T2)
  - 6-ch 16-bit PWM for Motor (by T3)
- **Buzzer**
  - 8-bit × 1-ch
- **USI (UART + SPI + I2C)**
  - 8-bit UART, 8-bit SPI and I2C
- **10-bit A/D Converter**
  - 11 Input channels
  - 4.5us conversion time
- **Analog Comparator**
  - 4-Channel
- **Operational Amplifier**
  - 1-Channel
- **Multiplier and Divider**
  - 16x16 Multiplier
  - 32÷16 Divider
  - Signed-signed and Unsigned-unsigned
- **Flash CRC Generator**
  - 16-Bit CRC Result
  - Auto and User CRC Mode
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 13 levels detect
    (1.60/ 2.10/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Low Voltage Indicator**
  - 12 levels detect
    (2.10/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Interrupt Sources**
  - External Interrupts
  - (EXINT0~7, EINT11, EINT12, EINT13) (11)
  - Timer(0/1/2/3) (5)
  - WDT (1)
  - BIT (1)
  - USI (3)
  - Comparator 0/1/2/3 (2)
  - ADC (1)
- **Internal RC Oscillator**
  - Internal RC frequency: 20MHz ±2.0% (T_A= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.0V~ 5.5V (@0.4 ~ 4.2MHz with Crystal)
  - 2.7V~ 5.5V (@0.4 ~ 12.0MHzwith Crystal)
  - 3.0V~ 5.5V (@0.4 ~ 16.0MHz with Crystal)
  - 3.3V~ 5.5V (@0.6 ~ 20.0MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 100ns (@20MHz main clock)
- **Operating Temperature**
  - –40 ~ +105℃
- **Oscillator Type**
  - 0.4 - 16MHz Crystal or Ceramic for main clock
- Package Type
  - 32LQFP
  - 24SSOP
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compier provider.
The MC96FD316T core is Mentor 8051, and the ROM size is smaller than 64 Kbytes. Therefore, developer can use the standard 8051 compiler from other providers.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.The OCD interface uses two-wire connection between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.
The OCD debugger program works on all Microsoft-Windows operating system.If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (http://www.abov.co.kr).

Connection:

- DSCL (MC96FD316T P33 port)
- DSDA (MC96FD316T P32 port)

OCD connector diagram: Connect OCD with user system

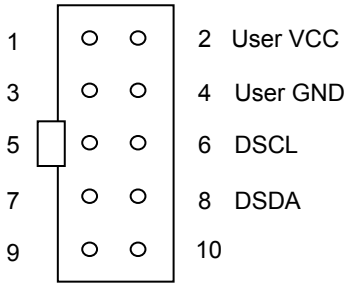


Figure 1.1 Debugger(OCD1/OCD2) and Pin description

1.3.3 Programmer

Single programmer :

E-PGM+ : It programs MCU device directly.

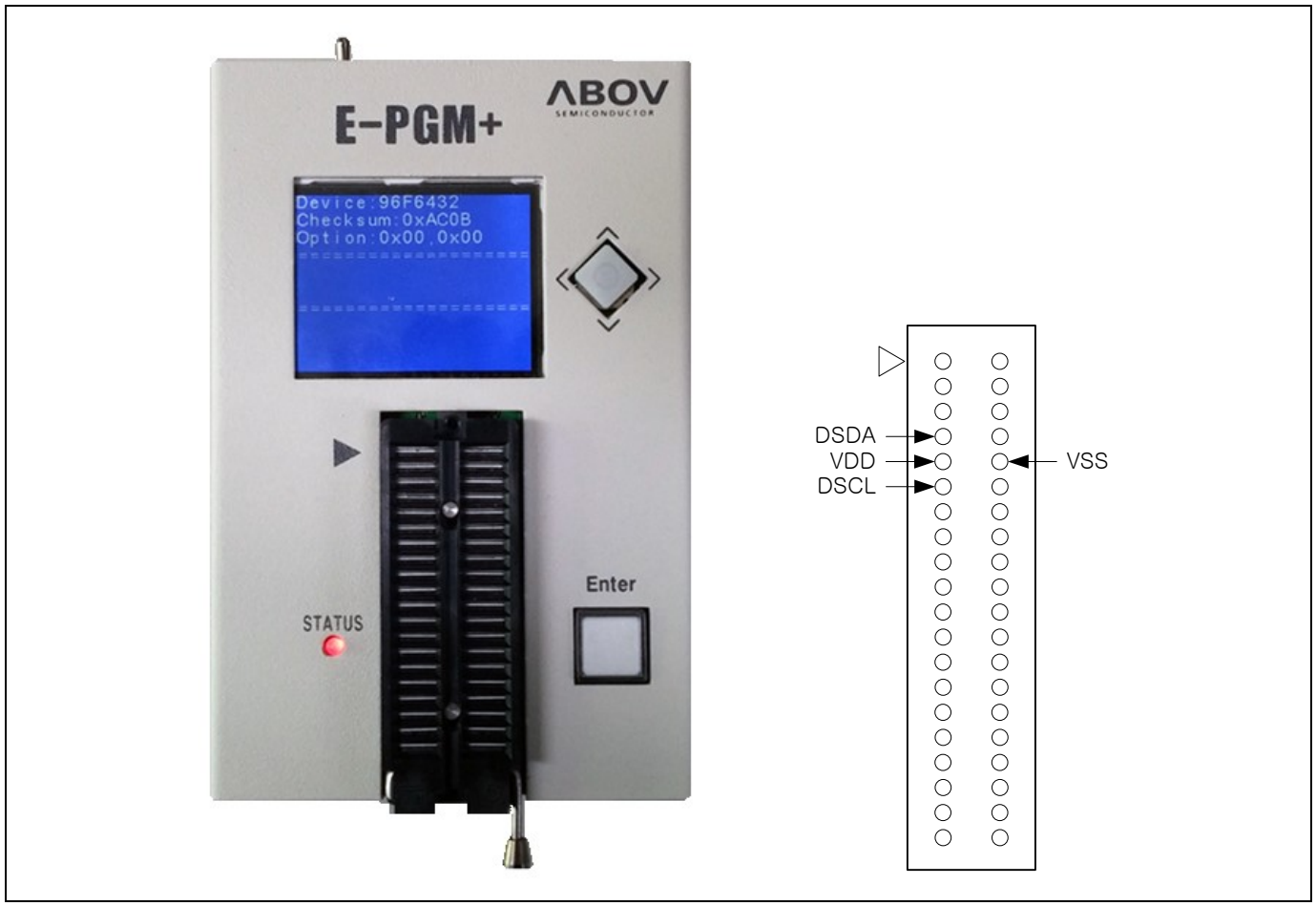


Figure 1.2 E-PGM+(Single writer)

OCD emulator:

It can write code to MCU device too, because OCD debugger supports ISP (In System Programming).It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.3 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of MC96FD316T is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, and VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P33	I	Serial clock pin. Input only pin.
DSDA	P32	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

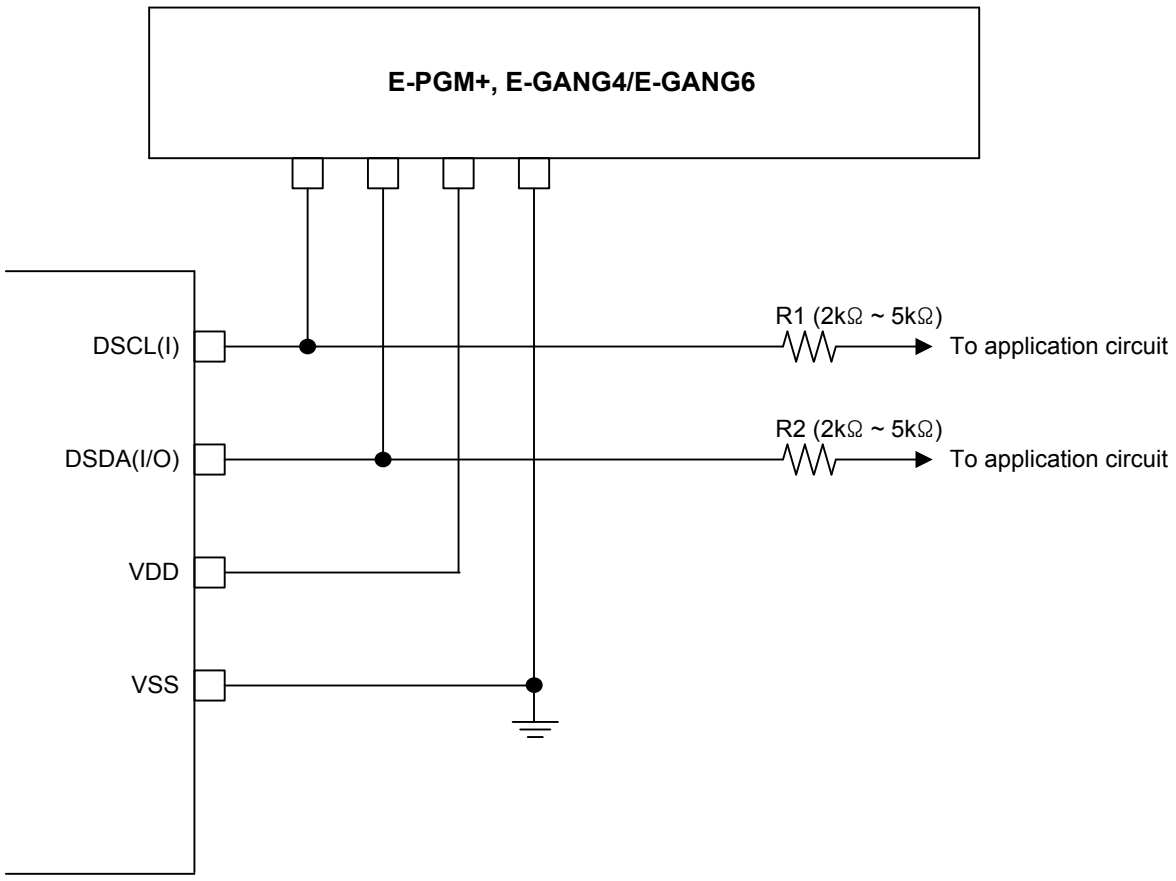
Table 1.2 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The MC96FD316T needs only four signal lines including VDD and VSS pins for programming FLASH with serial communication protocol. Therefore the on-board programming is possible if the programming signal lines are ready at the PCB of application board is designed.

1.4.2.1 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that areDSCL, DSDA, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.
Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.4 PCB design guide for on board programming

2 Block diagram

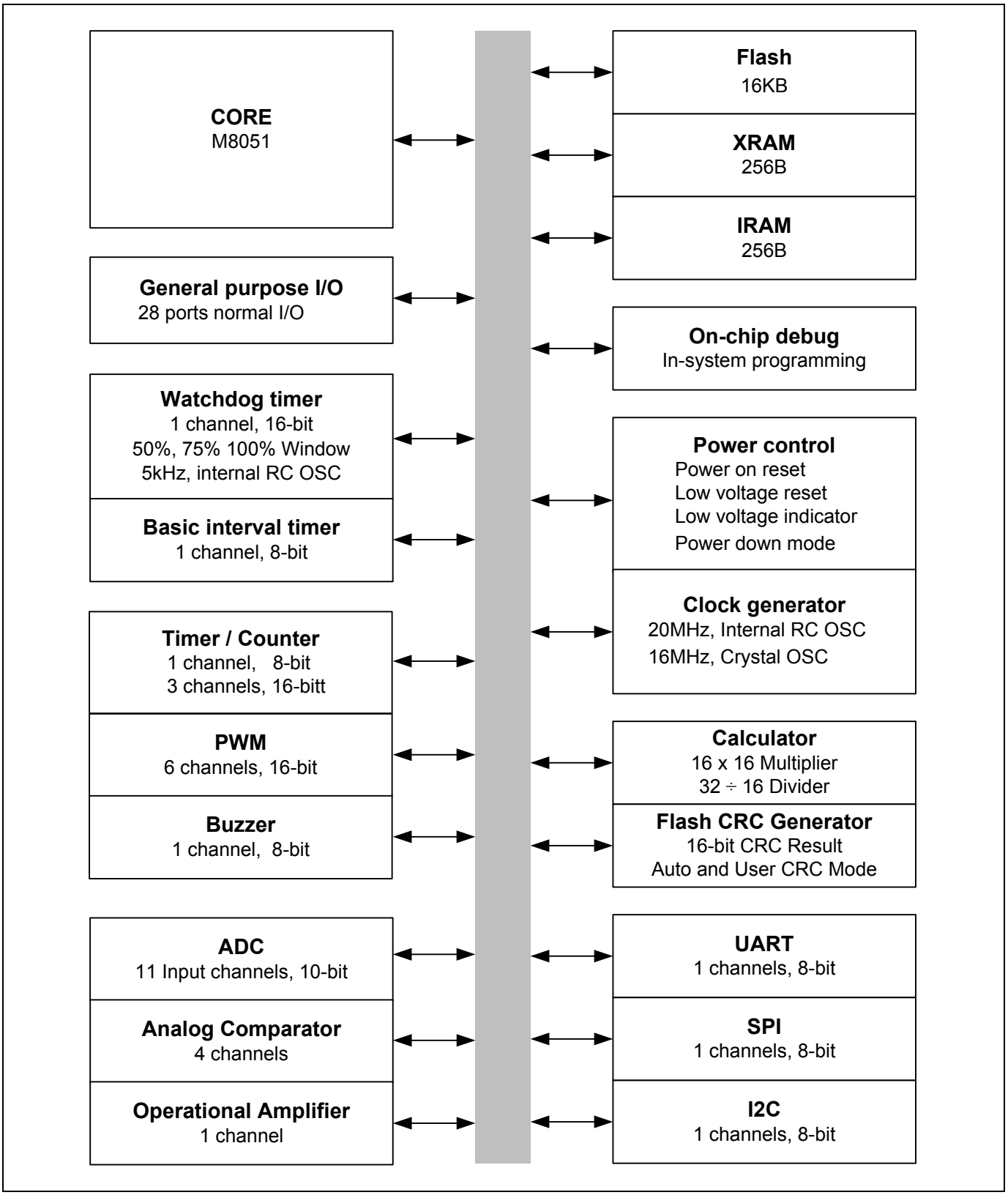
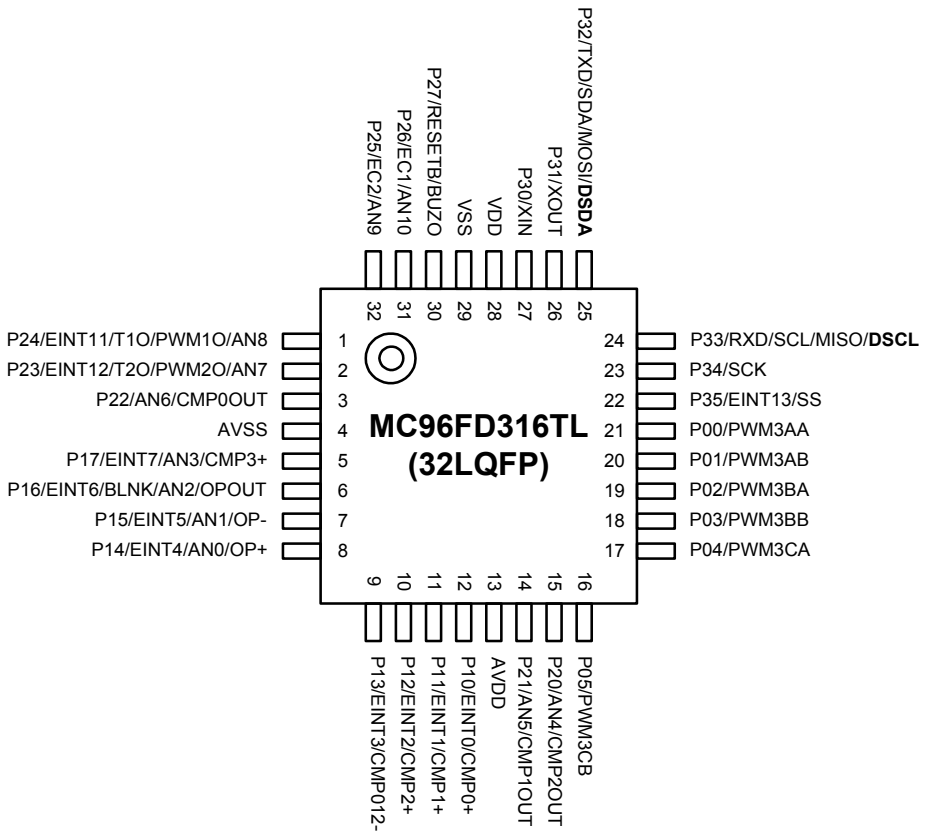


Figure 2.1 Block diagram of MC96FD316T

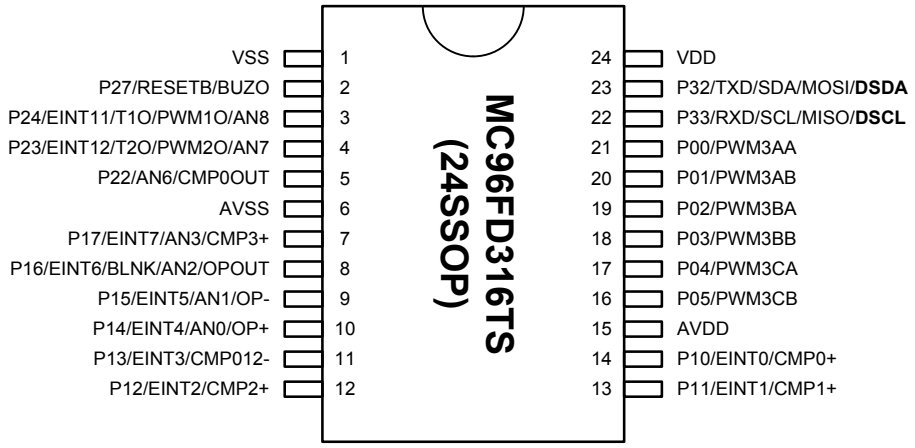
3 Pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.

Figure 3.1 MC96FD316TL 32LQFP pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.
2. The P20-P21, P25-P26, P30-P31, and P34-P35 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 24-pin package is used.

Figure 3.2 MC96FD316TS 24SSOP pin assignment

4 Package Diagram

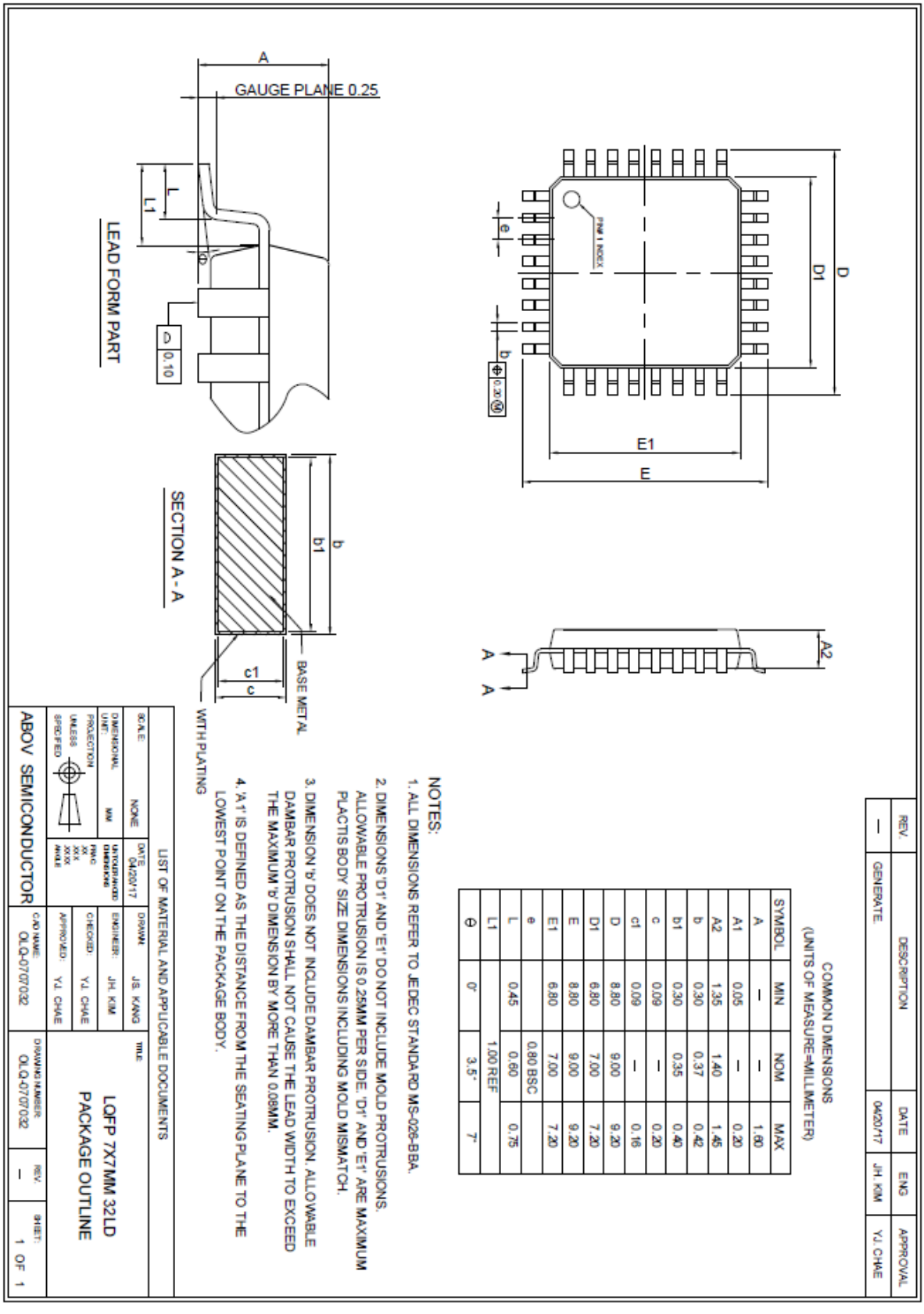


Figure 4.1 32-Pin LQFP Package

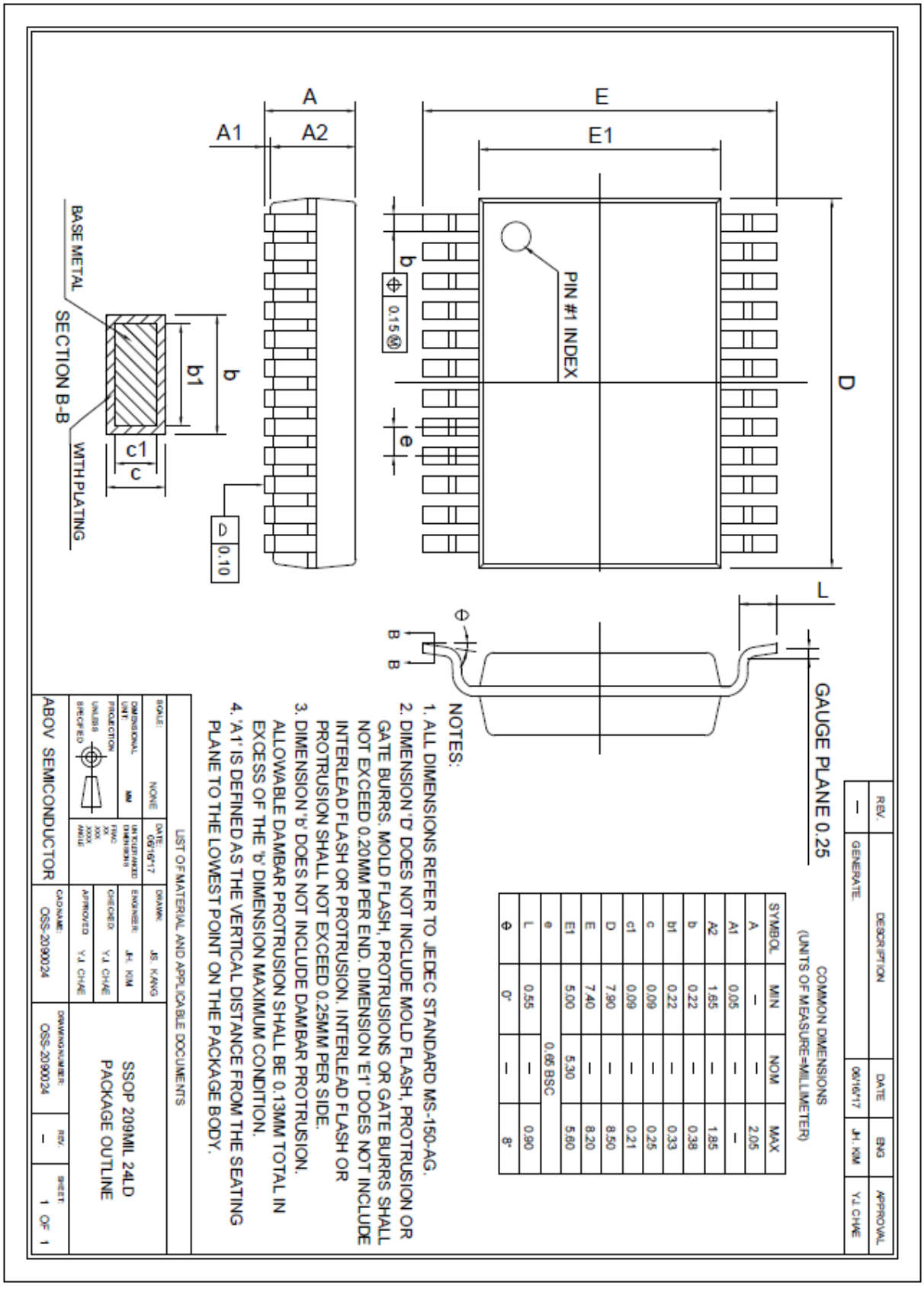


Figure 4.2 24-Pin SSOP Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	PWM3AA
P01				PWM3AB
P02				PWM3BA
P03				PWM3BB
P04				PWM3CA
P05				PWM3CB
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT0/CMP0+
P11				EINT1/CMP1+
P12				EINT2/CMP2+
P13				EINT3/CMP012-
P14				EINT4/AM0/OP+
P15				EINT5/AN1/OP-
P16				EINT6/BLNK/AN2/OPOUT
P17				EINT7/AN3/CMP3+
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P25-P26 are not in the 28-Pin package. The P20-P21 and P25-P26 are not in the 24-Pin package. P20-P27 are not in the 20-Pin package.	Input	AN4/CMP2OUT
P21				AN5/CMP1OUT
P22				AN6/CMP0OUT
P23				EINT12/T2O/PWM2O/AN7
P24				EINT11/T1O/PWM1O/AN8
P25				EC2/AN9
P26				EC1/AN10
P27				RESETB/BUZO
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P34-P35 are not in the 28-Pin package. The P30-P31 and P34-P35 are not in the 20/24-Pin package.	Input	XIN
P31				XOUT
P32				TXD/SDA/MOSI/DSDA
P33				RXD/SCL/MISO/DSCL
P34				SCK
P35				EINT13/SS

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
EINT0	I/O	External interrupt inputs	Input	P10/CMP0+
EINT1				P11/CMP1+
EINT2				P12/CMP2+
EINT3				P13/CMP012-
EINT4				P14/AM0/OP+
EINT5				P15/AN1/OP-
EINT6				P16/BLNK/AN2/OPOUT
EINT7				P17/AN3/CMP3+
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P24/T1O/PWM1O/AN8
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P23/T2O/PWM2O/AN7
EINT13	I/O	External interrupt input and Timer 3 capture input	Input	P35/SS
BLNK	I/O	External sync signal input for 6-ch PWMs	Input	P16/EINT6/AN2/OPOUT
T1O	I/O	Timer 1 interval output	Input	P24/EINT11/PWM1O/AN8
T2O	I/O	Timer 2 interval output	Input	P23/EITN12/PWM2O/AN7
PWM1O	I/O	Timer 1 pulse output	Input	P24/EINT11/T1O/AN8
PWM2O	I/O	Timer 2 pulse output	Input	P23/EITN12/T2O/AN7
PWM3AA	I/O	Timer 3 PWM outputs	Input	P00
PWM3AB				P01
PWM3BA				P02
PWM3BB				P03
PWM3CA				P04
PWM3CB				P05
EC1	I/O	Timer 1 event count input	Input	P26/AN10
EC2	I/O	Timer 2 event count input	Input	P25/AN9
BUZO	I/O	Buzzer signal output	Input	P27/RESETB
SCK	I/O	Serial clock input/output	Input	P34
MOSI	I/O	SPI master output, slave input	Input	P32/TXD/SDA/DSDA
MISO	I/O	SPI master input, slave output	Input	P33/RXD/SCL/DSCL
SS	I/O	SPI slave select input	Input	P35/EINT13
TXD	I/O	UART data output	Input	P32/SDA/MOSI/DSDA
RXD	I/O	UART data input	Input	P33/SCL/MISO/DSCL
SCL	I/O	I2C clock input/output	Input	P33/RXD/MISO/DSCL
SDA	I/O	I2C data input/output	Input	P32/TXD/MOSI/DSDA

Table 5.2 Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
AN0	I/O	A/D converter analog input channels	Input	P14/EINT4/OP+
AN1				P15/EINT5/OP-
AN2				P16/EINT6/BLNK/OPOUT
AN3				P17/EINT7/CMP3+
AN4				P20/CMP2OUT
AN5				P21/CMP1OUT
AN6				P22/CMP0OUT
AN7				P23/EINT12/T2O/PWM2O
AN8				P24/EINT11/T1O/PWM1O
AN9				P25/EC2
AN10				P26/EC1
CMP0+	I/O	Analog comparator positive inputs	Input	P10/EINT0
CMP1+				P11/EINT1
CMP2+				P12/EINT2
CMP3+				P17/EINT7/AN3
CMP012-	I/O	Analog comparator 0/1/2 negative inputs	Input	P13/EINT3
CMP0OUT	I/O	Analog comparator outputs	Input	P22/AN6
CMP1OUT				P21/AN5
CMP2OUT				P20/AN4
OP+	I/O	Operational amplifier positive input	Input	P14/EINT4/AM0
OP-	I/O	Operational amplifier negative input	Input	P15/EINT5/AN1
OPOUT	I/O	Operational amplifier output	Input	P16/EINT6/BLNK/AN2
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P27/BUZO
DSDA	I/O	On chip debugger data input/output (NOTE5,6)	Input	P32/TXD/SDA/MOSI
DSCL	I/O	On chip debugger clock input (NOTE5,6)	Input	P33/RXD/SCL/MISO
XIN	I/O	Main oscillator pins	Input	P30
XOUT				P31
AVDD, AVSS	–	Analog power input pins	–	–
VDD, VSS	–	Power input pins	–	–

Table 5.3 Normal Pin Description (continue)

NOTE)

1. The P25-P26 and P34-P35 are not in the 28-Pin package.
2. The P20-P21, P25-P26, P30-P31, and P34-P35 are not in the 24-Pin package.
3. The P20-P27, P30-P31, and P34-P35 are not in the 20-Pin package
4. The P27/RESETB/BUZ pin is configured as one of the P27/BUZO and the RESETB pin by the “CONFIGURE OPTION.”
5. If the P32/TXD/SDA/MOSI/DSDA and P33/RXD/SCL/MISO/DSCL pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
6. The P32/TXD/SDA/MOSI/DSDA and P33/RXD/SCL/MISO/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
7. The P30/XIN and P31/XOUT pins are configured as a function pin by software control.

6 Port Structures

6.1 General Purpose I/O Port

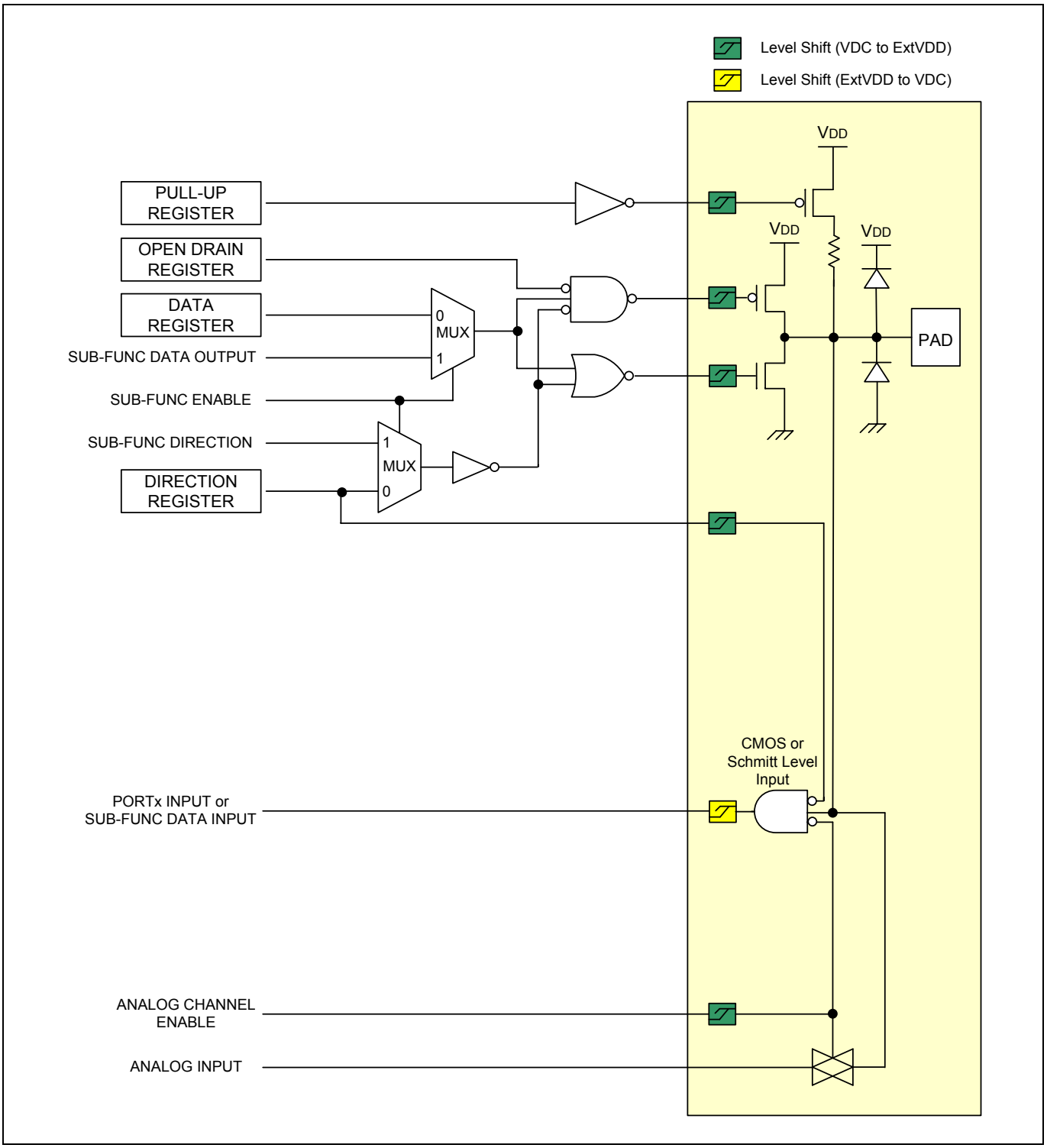


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

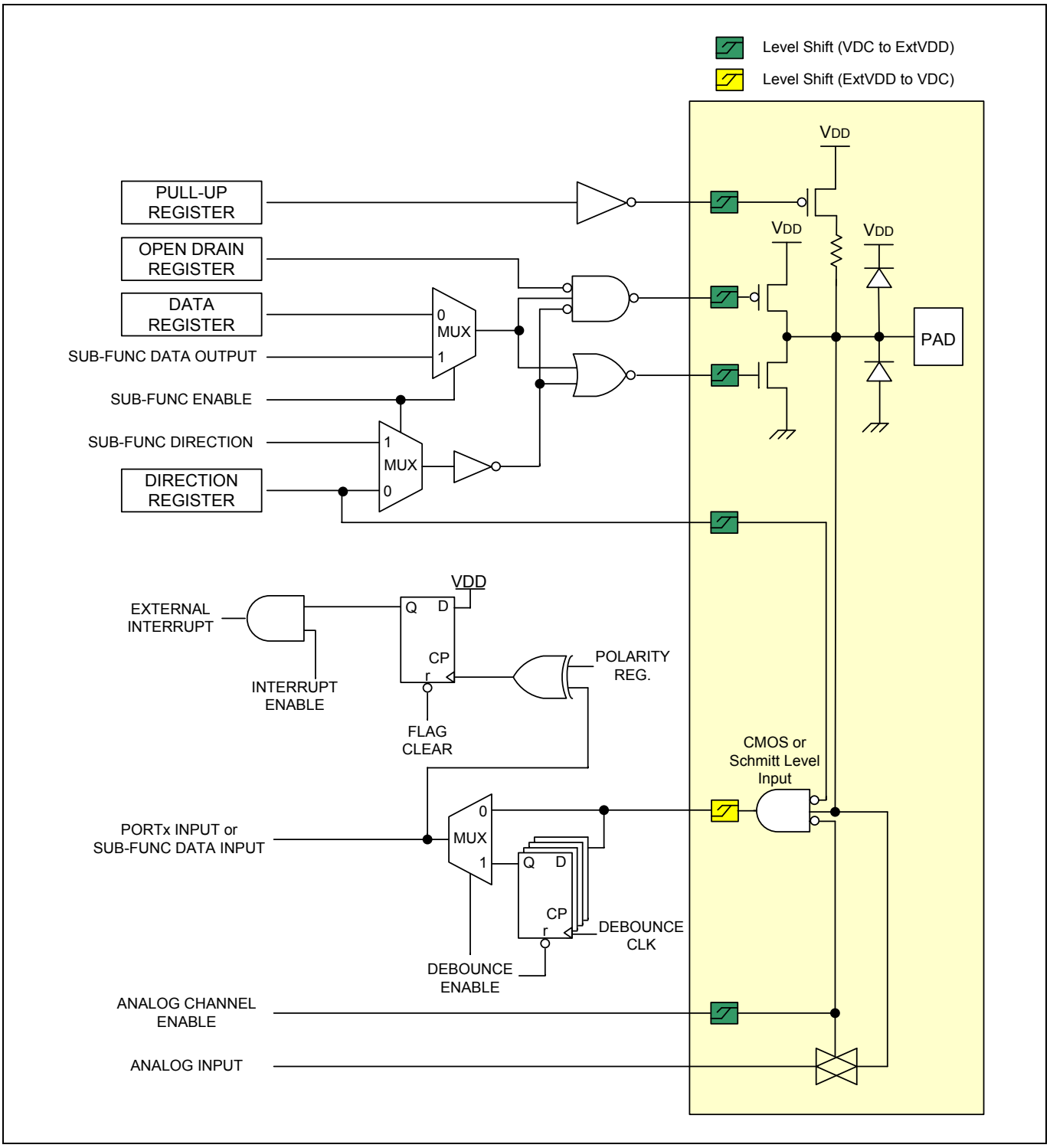


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +105°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 0.4 ~ 4.2MHz	Main Crystal	2.0	–	5.5	V
		f_X= 0.4 ~12MHz		2.7	–	5.5	
		f_X= 0.4 ~16MHz		3.0	–	5.5	
		f_X= 0.6 ~ 10MHz	Internal RC	2.0	–	5.5	
		f_X= 0.6 ~ 20MHz		3.3	–	5.5	
Operating Temperature	T_{OPR}	VDD=2.0~5.5V		-40	–	105	°C

Table 7.2 Recommended Operating Conditions

7.3 Analog Comparator Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=0V, Comparator 0/1/2)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input Offset Voltage	V_{OF}	V_{DD} = 4.5V, V_{IN} = 1/2V_{DD}		–	±10	±30	mV
Response Time	T_{CR}			–	1.0	3.0	us
Comparator Input Voltage	V_{CIN}			100	–	–	mVp-p
Hysteresis	△V	V_{DD} = 4.5V	HYSSEL=0	–	5	20	mV
			HYSSEL=1	–	20	100	mV
Comparator Current	I_{CMP}	Enable	V_{DD} = 4.5V	–	100	200	uA
		Disable		–	–	0.1	uA

Table 7.3 Analog Comparator Characteristics, Comparator 0/1/2

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=0V, Comparator 3)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input Offset Voltage	V_{OF}	V_{DD} = 4.5V, V_{IN} = 1/2V_{DD}		–	±10	±30	mV
Response Time	T_{CR}			–	0.1	0.3	us
Hysteresis	△V			–	20	100	mV
Comparator Current	I_{CMP}	Enable	V_{DD} = 4.5V	–	400	600	uA
		Disable		–	–	0.1	uA

Table 7.4 Analog Comparator Characteristics, Comparator 3

7.4 Operational Amplifier Characteristics

(T_A=-20°C ~ +60°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input Offset Voltage	V_{OF}	V_{DD} = 4.5V, V_{IN} = 1/2V_{DD}		–	–	±20	mV
Common-mode Rejection Ratio	CMRR	VDD=4.5V, VIN=1.0V		50	70	–	dB
Power Supply Rejection Ratio	PSRR	VDD=4.5V, VIN=1.0V		40	70	–	
Open Loop Voltage Gain (AMP0)	–	V_{DD} = 4.5V		–	96	–	dB
Common-mode Input Voltage	V_{IN}	V_{DD} = 4.5V		0	–	V_{DD}-1.5V	V
Output Voltage High	V_{AMPH}	V_{DD}=4.5V, IOH=-0.5mA		V_{DD}-0.2	–	–	V
Output Voltage Low	V_{AMPL}	V_{DD}=4.5V, IOL=0.5mA		–	–	0.2	V
Gain Bandwidth	f_{GB}	VDD=4.5V		–	–	3	MHz
Supply Voltage	V_{AMP}	–		2.8	–	5.5	V
OP-AMP Current	I_{AMP}	Enable	V_{DD}=4.5V	–	240	360	uA
		Disable		–	–	0.1	

Table 7.5 Operational Amplifier Characteristics

7.5 A/D Converter Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=AVSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–-	10	–	bit
Integral Non-Linear	INL	AVDD= 2.7V – 5.5V fx= 8MHz		–	–	±3	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	AVDD=4.0V – 5.5V		4.5	–	–	us
		AVDD=3.0V – 5.5V		9.0	–	–	
		AVDD=2.7V – 5.5V		18.0	–	–	
Analog Input Voltage	V_{AIN}	–		AVSS	–	AVDD	V
Analog Power Voltage	AVDD	*Note 3		VDD-0.3	VDD	VDD+0.3	
Internal VDC Voltage	VDD19	VDD=3V, T_A= 25°C		1.85	1.95	2.05	V
Analog Input Leakage Current	I_{AIN}	AVDD=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.6 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (VDD).
3. When AVDD is lower than 2.7V, the ADC resolution is worse.

7.6 Power-On Reset Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.7 Power-on Reset Characteristics

7.7 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V		–	1.60	1.79	V
				1.90	2.10	2.30	
				2.00	2.20	2.40	
				2.12	2.32	2.52	
				2.24	2.44	2.64	
				2.34	2.59	2.84	
				2.50	2.75	3.00	
				2.68	2.93	3.18	
				2.89	3.14	3.39	
				3.13	3.38	3.63	
				3.32	3.67	4.02	
				3.65	4.00	4.35	
				4.05	4.40	4.75	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	35.0	uA
		Enable (One of two)		–	10.0	25.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

Table 7.8 LVR and LVI Characteristics

7.8 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.2 – 5.5V		–	20	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±2.0	%
		T_A = -40°C to +105°C				±5.0	
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	T_{HFS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.4	–	mA
		Disable		–	–	0.1	uA

Table 7.9 Internal RC Oscillator Characteristics

NOTE)

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.9 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	Run, Idle Mode	3	5	7	kHz
		Stop Mode	1.7	5	11.5	
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.10 Internal WDTRC Oscillator Characteristics

7.10 DC Characteristics

(T_A= -40°C ~ +105°C, VDD= 2.0V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P1, P2,P3, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P1, P2,P3, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD=4.5V, I_{OH}=-2mA, All output ports except V_{OH2}		VDD-1.0	–	–	V
	V_{OH2}	VDD=4.5V, I_{OH}=-10mA; P0		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 10mA; All output ports except V_{OL2}		–	–	1.0	V
	V_{OL2}	VDD=4.5V, I_{OL}= 15mA; P1, P2		–	–	1.0	
Input High Leakage Current	I_{IH}	All input ports		–	–	1.0	uA
Input Low Leakage Current	I_{IL}	All input ports		-1.0	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
OSC feedback resistor	R_X	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ

Table 7.11 DC Characteristics

(T_A= -40°C ~ +105°C, VDD= 2.0V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Current	I_{DD1} (RUN)	f_{XIN}= 16MHz, VDD= 5V±10%	–	4.5	9.0	mA
		f_{XIN}= 12MHz, VDD= 3V±10%	–	3.0	6.0	
		f_{IRC}= 20MHz, VDD= 5V±10%	–	4.0	8.0	
	I_{DD2} (IDLE)	f_{XIN}= 16MHz, VDD= 5V±10%	–	2.0	4.0	mA
		f_{XIN}= 12MHz, VDD= 3V±10%	–	1.0	2.0	
		f_{IRC}= 20MHz, VDD= 5V±10%	–	1.5	3.0	
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C	–	0.5	3.0	uA

Table 7.12 DC Characteristics(Continued**)**

NOTE)

1. Where the f_{XIN} is an external main oscillator, the f_{IRC} is an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.11 AC Characteristics

(T_A= -40°C ~ +105°C, VDD= 2.0V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5V (n= 1, 2)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5V (n= 1, 2)	20	–	–	

Table 7.13 AC Characteristics

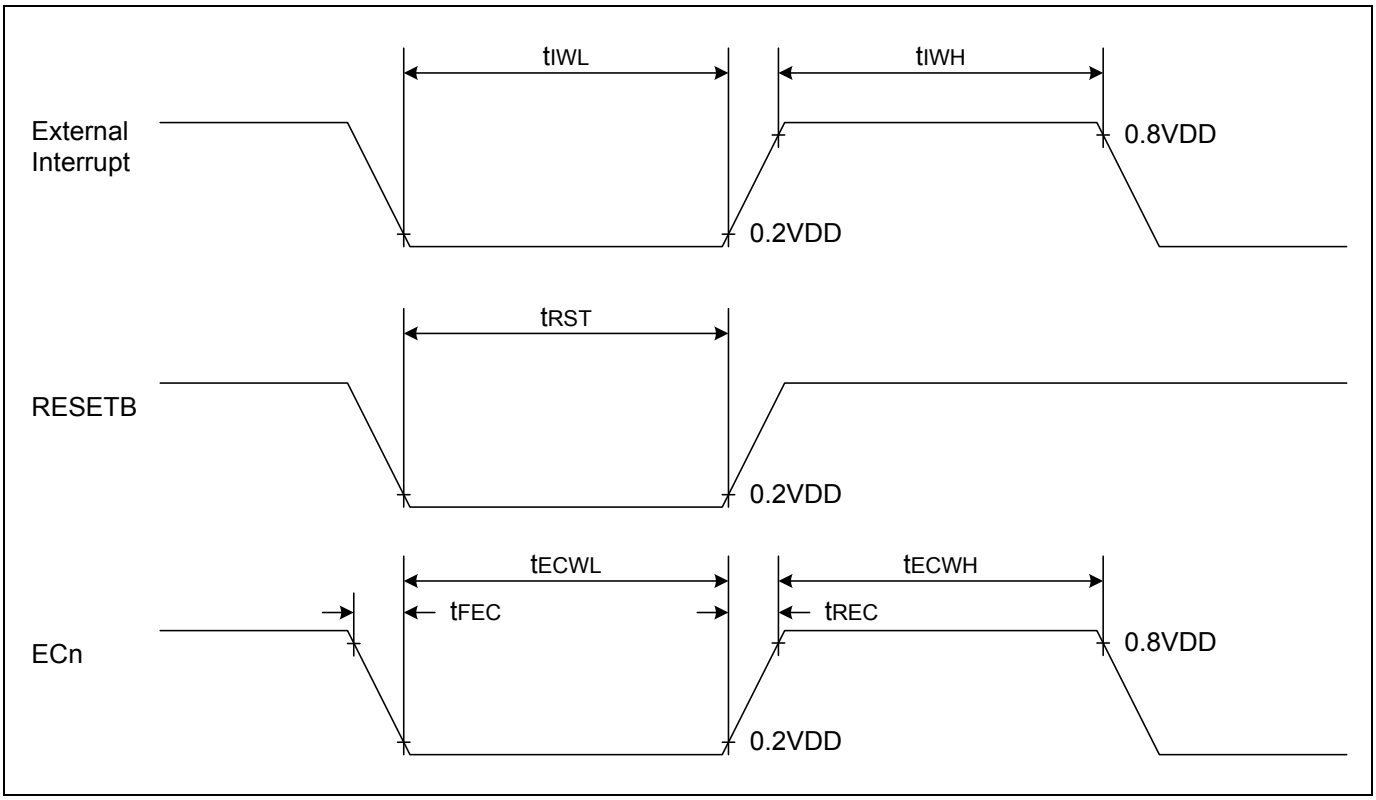


Figure 7.1 AC Timing

7.12 SPI Characteristics

(T_A=-40°C– +105°C, VDD=2.0V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	100	–	–	
Input Hold Time	t_{DIH}	–	150	–	–	

Table 7.14 SPI Characteristics

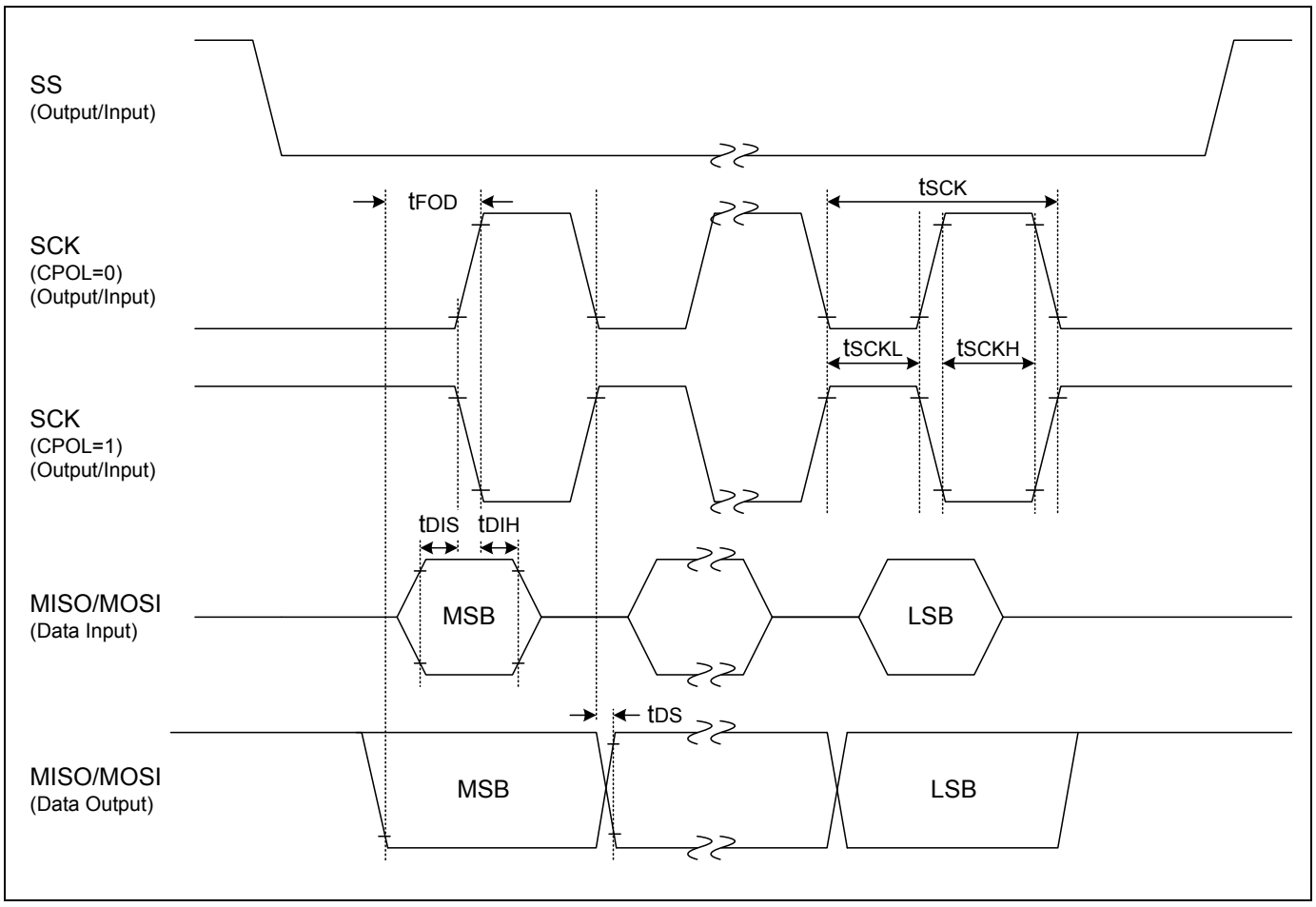


Figure 7.2 SPI Timing

7.13 UART Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	ns

Table 7.15 UART Characteristics

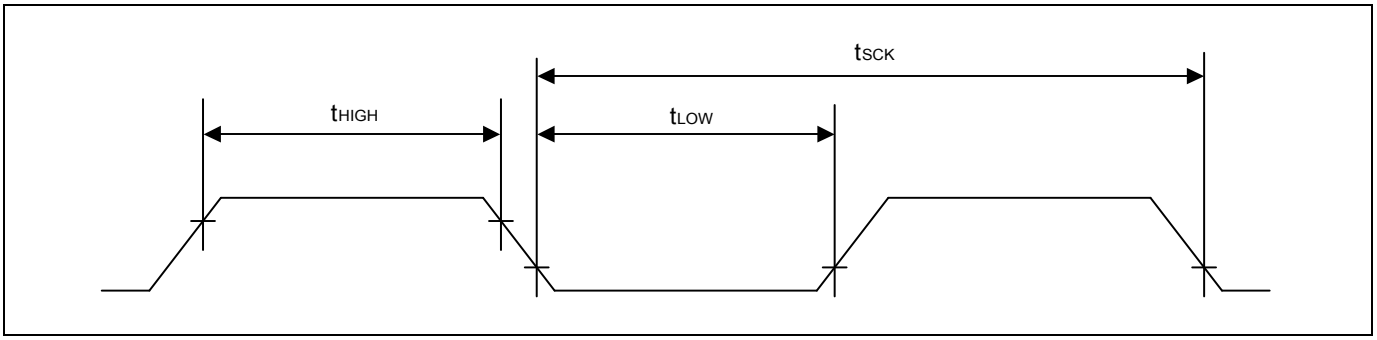


Figure 7.3 Waveform for UART Timing Characteristics

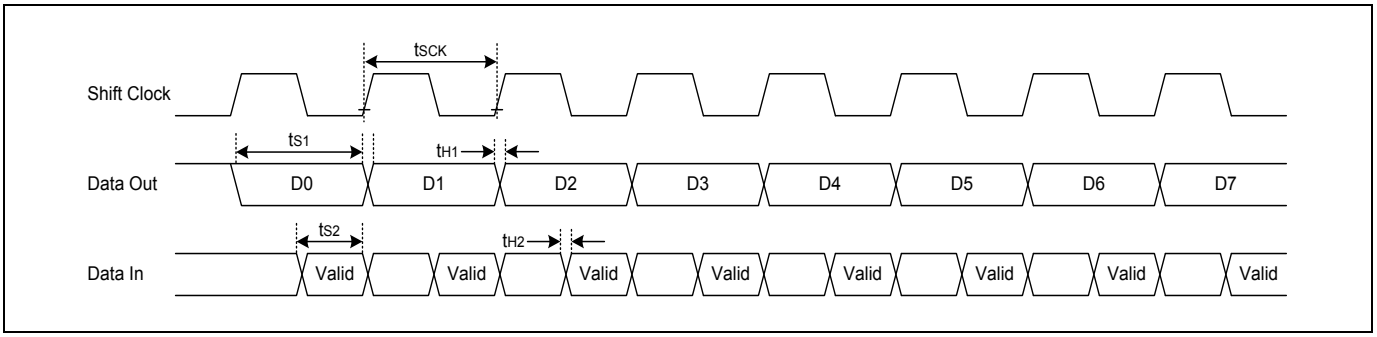


Figure 7.4 Timing Waveform for the UART Module

7.14 I2C Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.16 I2C Characteristics

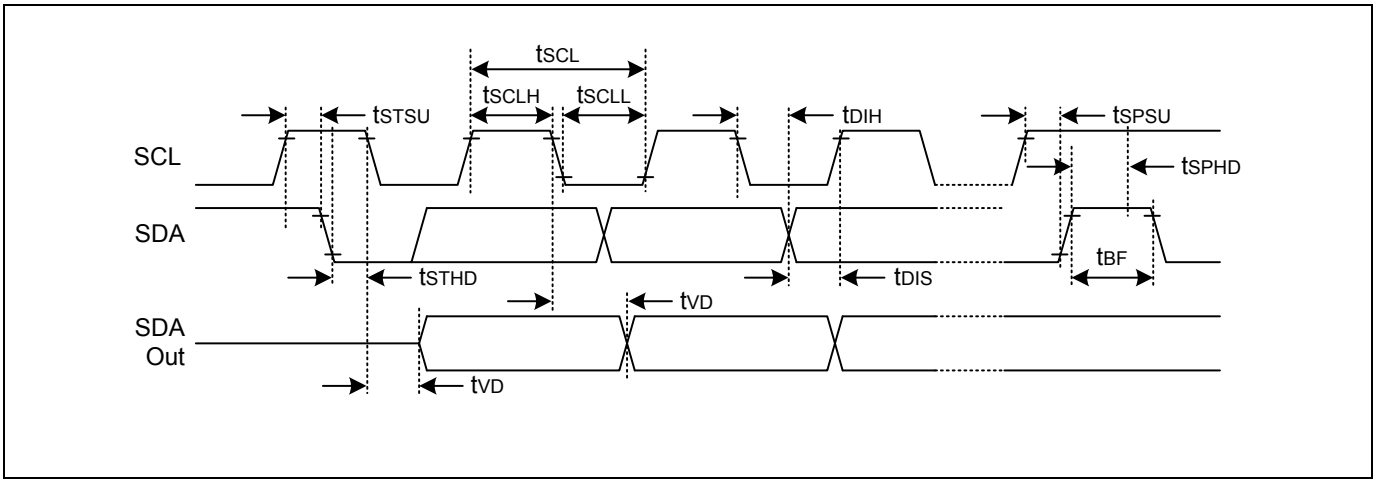


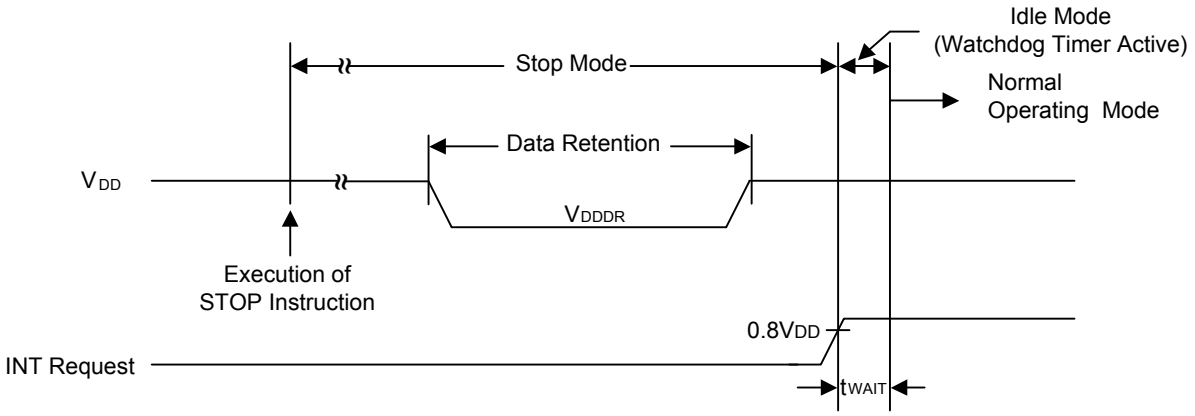
Figure 7.5 I2C Timing

7.15 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V)

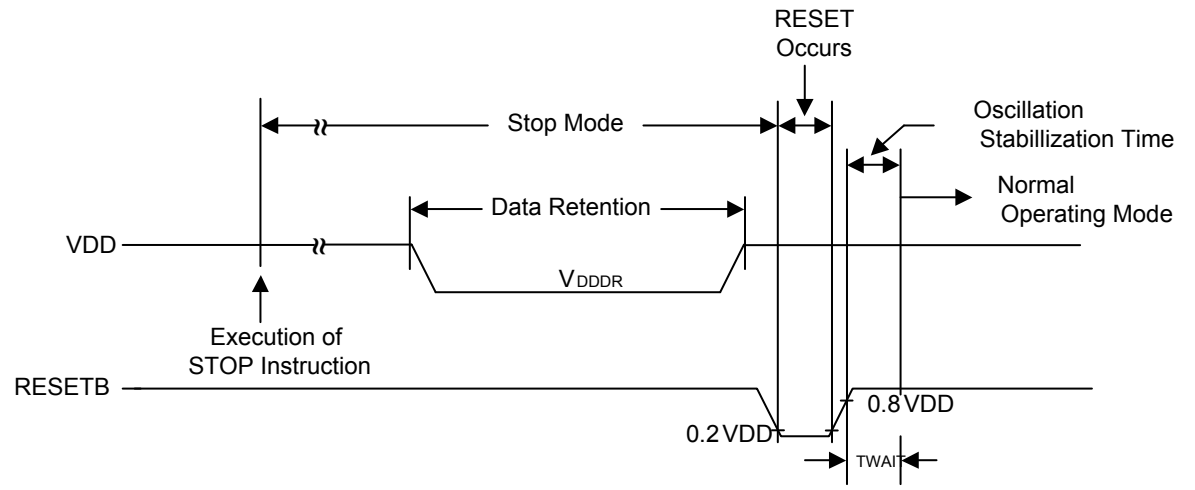
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 2.0V, (T_A= 25°C), Stop mode	–	–	1	uA

Table 7.17 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.6 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 16/f_{IRC}) = (13.1mS at fx=1.25MHz).

Figure 7.7 Stop Mode Release Timing when Initiated by RESETB

7.16 Internal Flash Rom Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	10,000	times
Flash Data Retention Time	t_{FR}	–	10	–	–	years

Table 7.18 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.17 Input/Output Capacitance

(T_A=-40°C ~ +105°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.19 Input/Output Capacitance

7.18 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
		3.0V – 5.5V	0.4	–	16.0	
Ceramic Oscillator	Main oscillation frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
		3.0V – 5.5V	0.4	–	16.0	
External Clock	XIN input frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
		3.0V – 5.5V	0.4	–	16.0	

Table 7.20 Main Clock Oscillator Characteristics

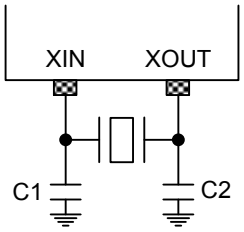


Figure 7.8 Crystal/Ceramic Oscillator

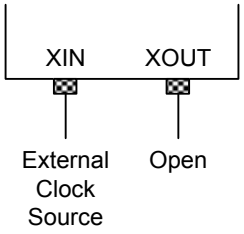


Figure 7.9 External Clock

7.19 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +105°C, VDD=2.0V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	f_{XIN} ≥ 1 MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	f_{XIN} = 0.4 to 16MHz XIN input high and low width (t_{XH}, t_{XL})	32.25	–	1250	ns

Table 7.21 Main Oscillation Stabilization Characteristics

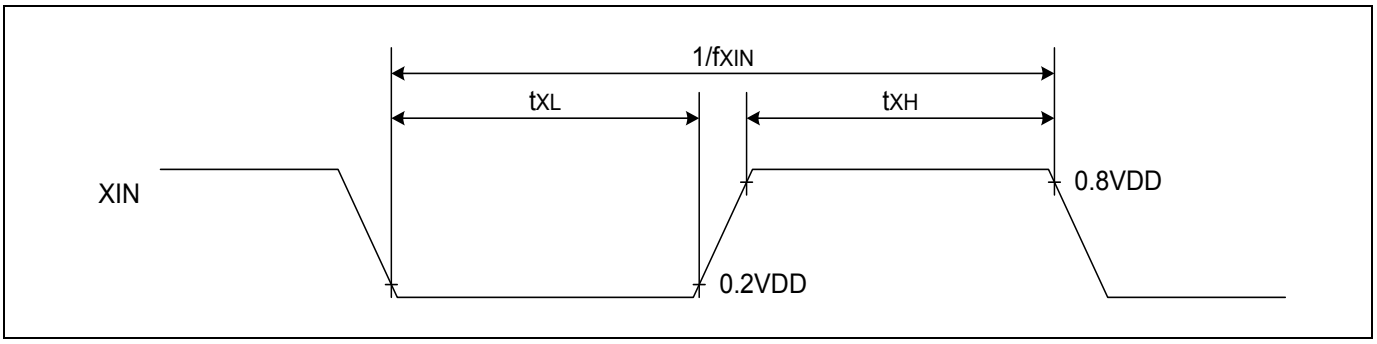


Figure 7.10 Clock Timing Measurement at XIN

7.20 Operating Voltage Range

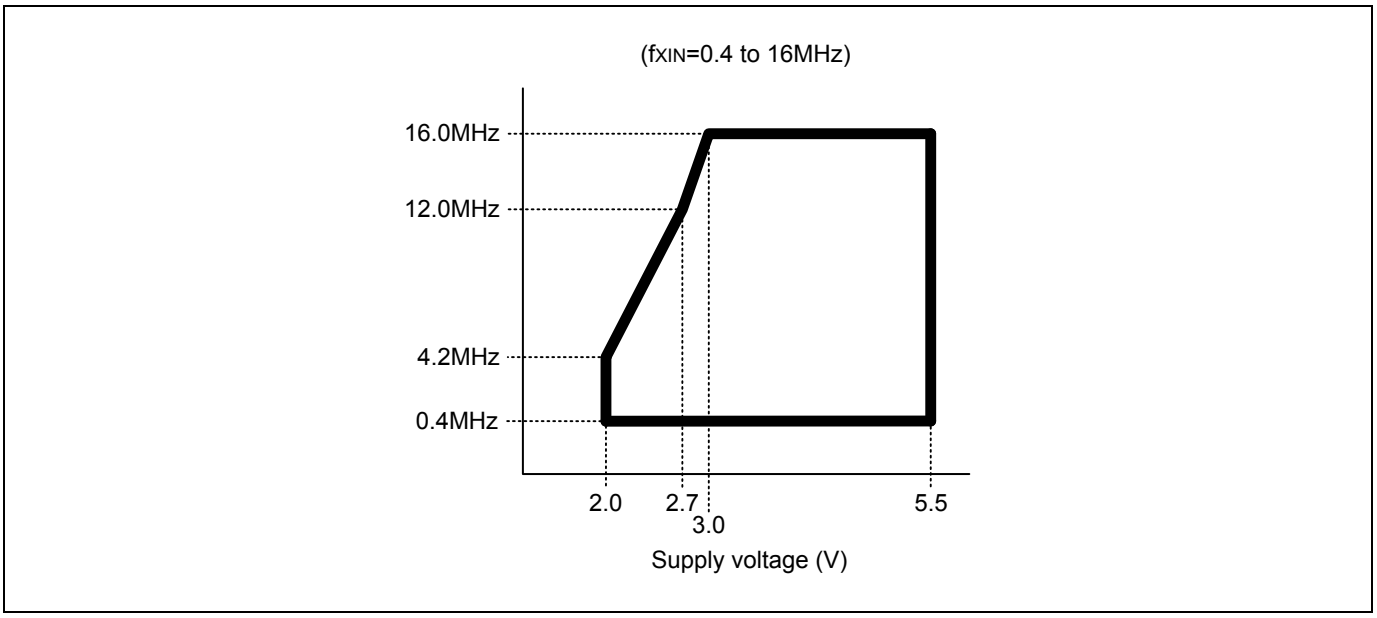


Figure 7.11 Operating Voltage Range

7.21 Recommended Circuit and Layout

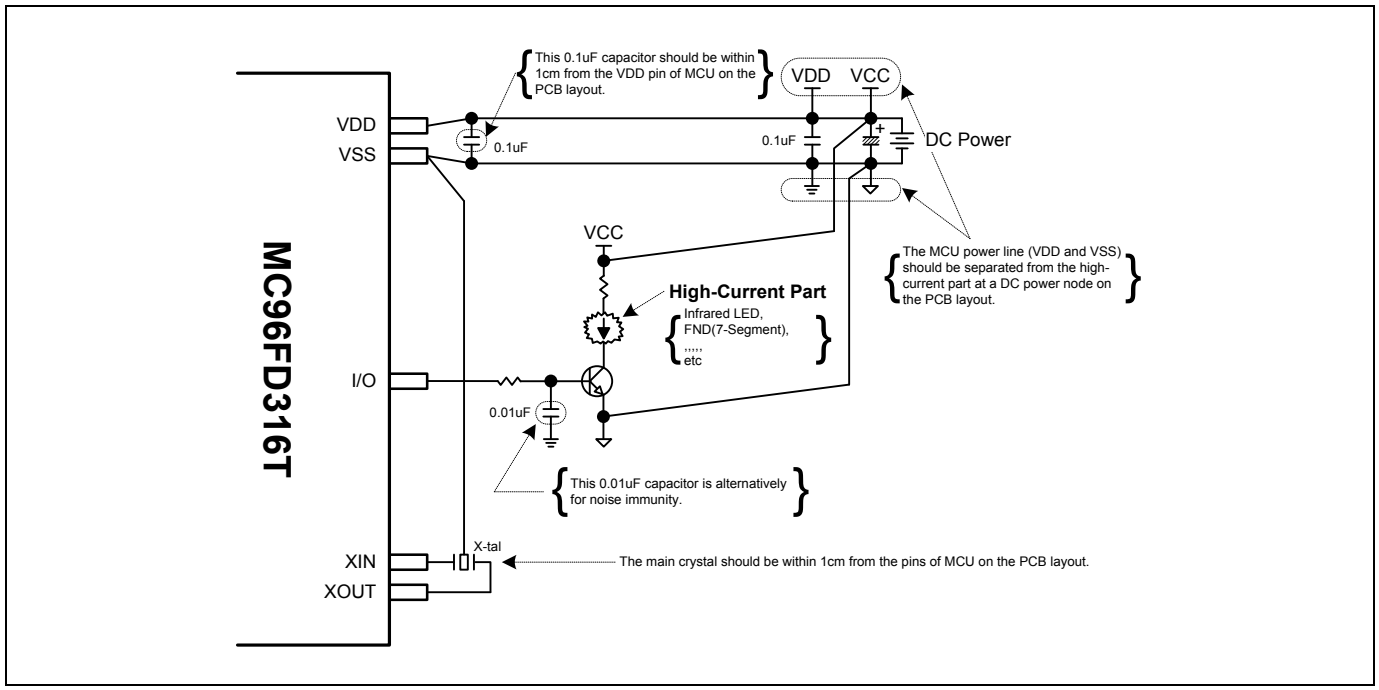
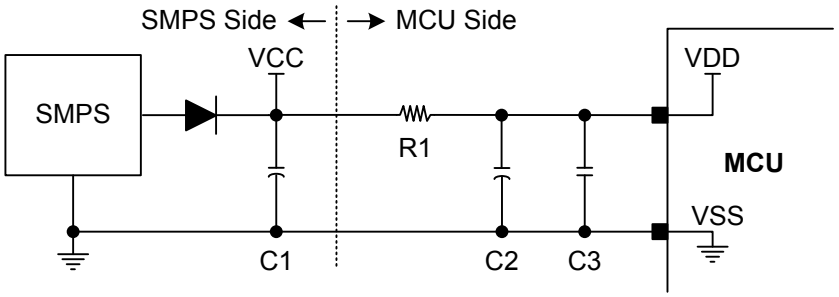


Figure 7.12 Recommended Circuit and Layout

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.13 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

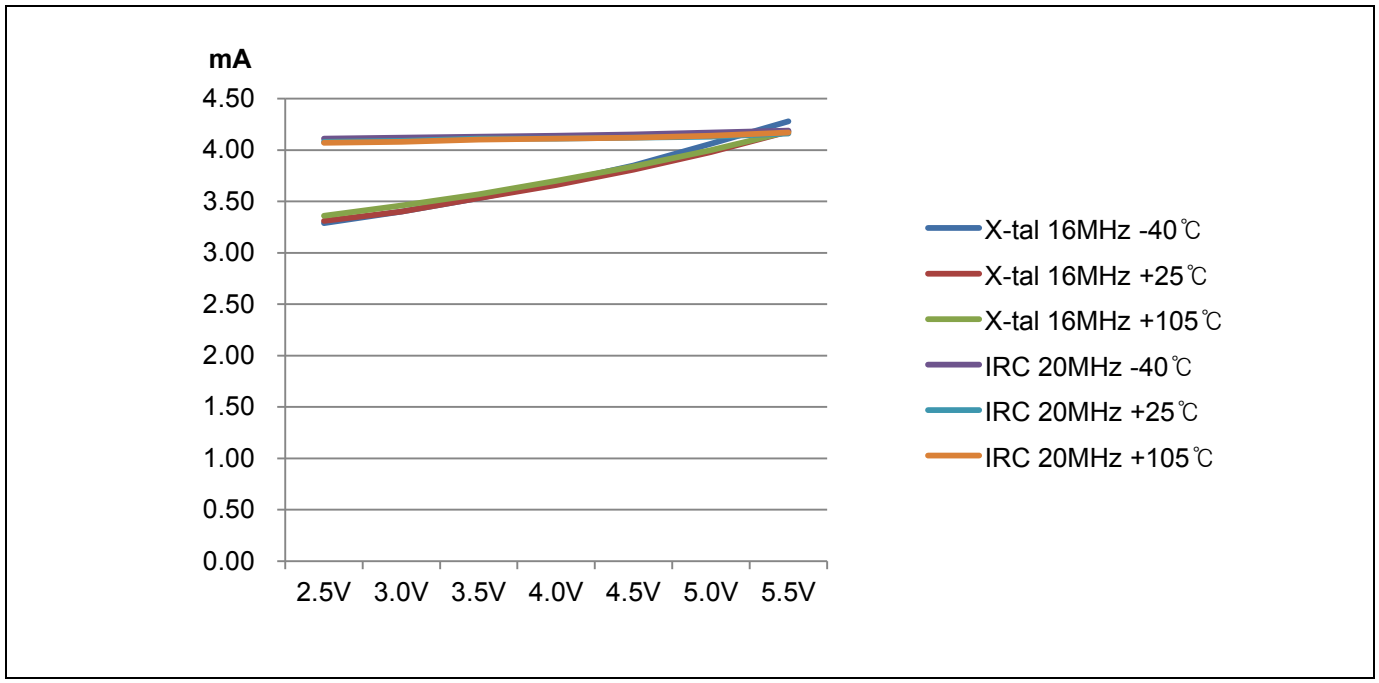


Figure 7.14 RUN (IDD1) Current

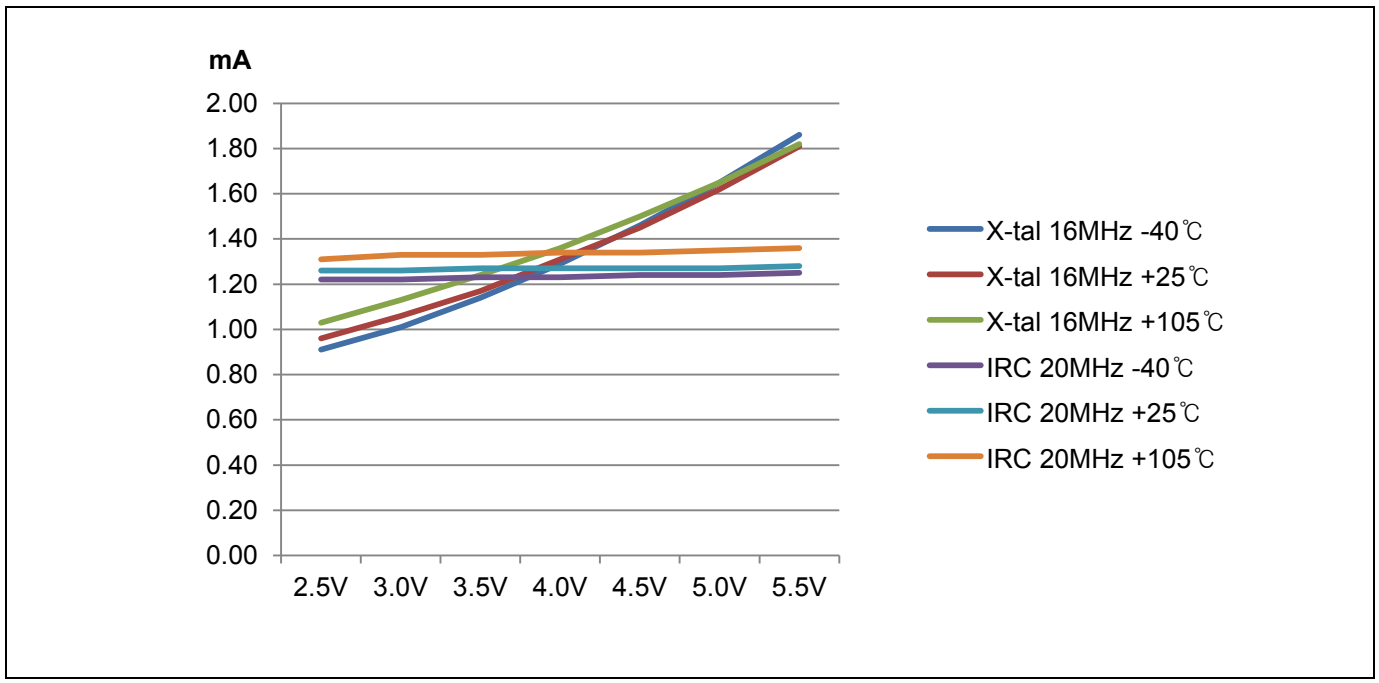


Figure 7.15 IDLE (IDD2) Current

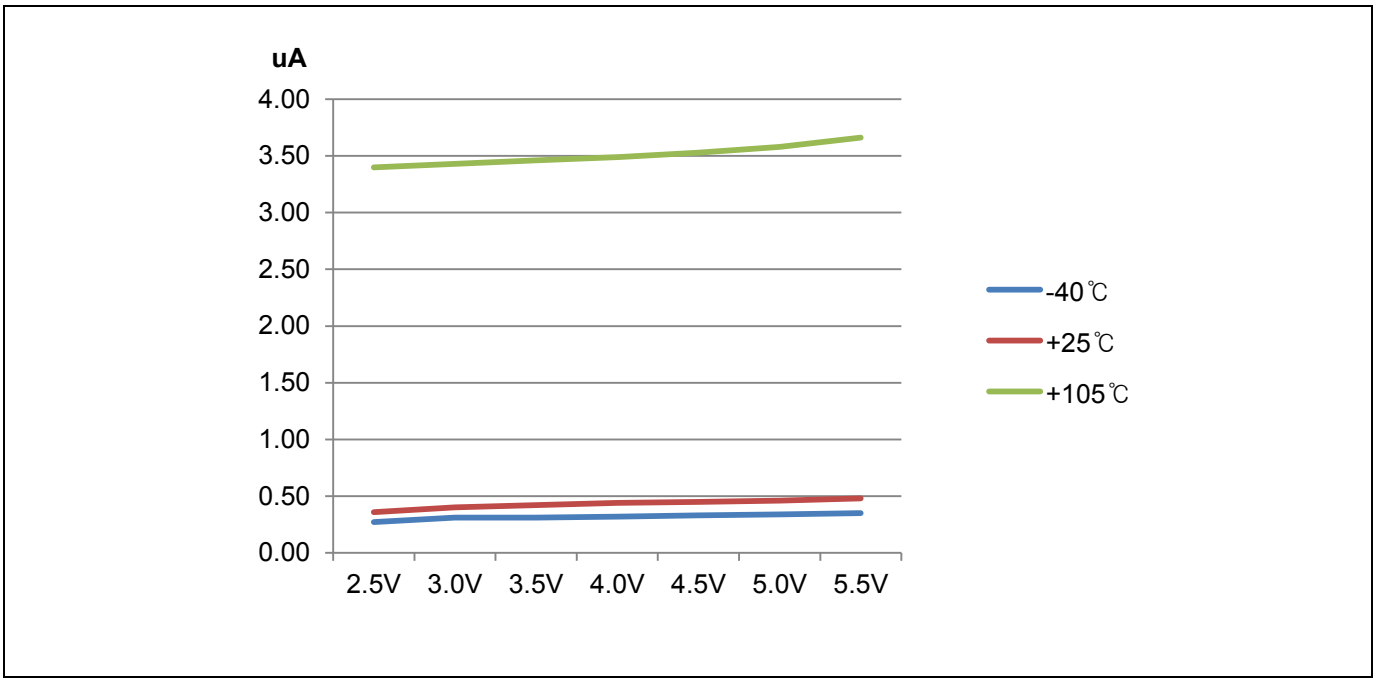


Figure 7.16 STOP (IDD5) Current

7.24 Thermal Resistance Characteristics

Junction Temp. (°C)	Case Temp. (°C)	Ambient Temp. (°C)	Theta-Ja (°C/W)
156.045	154.764	105	85.075

Table 7.22 24SSOP(0.65-D1.50, 110X110)

Junction Temp. (°C)	Case Temp. (°C)	Ambient Temp. (°C)	Theta-Ja (°C/W)
146.685	146.118	105	69.475

Table 7.23 32LQFP(150X150)

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