CMOS single-chip 8-bit MCU with 12-bit A/D converter

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 64 Kbytes Flash Code Memory
  - 4352 bytes SRAM(IRAM 256 bytes + XRAM 4096 bytes)
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16MHz RC Oscillator (±2.0%, T_A= 0 ~ +50°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (15 inputs)
  - 16-bit CRC/Checksum Generator
  - UART 8-bit x 3-ch
  - SPI 8-bit x 2-ch
  - USI (UART + SPI + I2C) 2 sets
- **I/O and Packages**
  - Up to 61 Programmable I/O lines with 64-pin package
  - 64LQFP-1010, 64LQFP-1414, 64QFN, 44MQFP, 44LQFP
  - Pb-free package
- **Operating Conditions**
  - 2.2V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Home appliance, Industrial Control

MC97F2664A

Datasheet

V 1.5

Revised 27 October, 2022

Revision history

Version	Date	Revision list
1.0	2017.06.14	Published this book.
1.1	2017.12.14	Added Figure 1.1 Device Nomenclature. Updated 64LQFP-1010 and 64LQFP-1414 package diagrams in Chapter 4. Package Diagram. Updated Chapter 1.3.2 OCD2 emulator and debugger. Updated Figure 1.3 E-PGM+(Single writer). Updated Chapter 1.4 MTP programming. Updated Chapter 7.22 Recommended Circuit and Layout with SMPS Power.
1.2	2020.01.15	Added a description of debounce function in Chapter 9. I/O Ports. Added a note about the Capture mode in all Timer.
1.3	2021.05.13	Added a Package Type “MC97F2464AL (44LQFP-1010)”
1.4	2021.07.06	Revised this book. Modify Exposed pad connection of QFN package.
1.5	2022.10.27	Modify a font.

Version 1.5

Published by FAE team

1 Overview

1.1 Description

The MC97F2664A is advanced CMOS 8-bit microcontroller with 64 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 64 Kbytes of FLASH, 256 bytes of IRAM, 4096 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, watch timer, buzzer driving port, SPI, UART, I2C, 12-bit A/D converter, 16-bit CRC/Checksum Generator, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC97F2664A also supports power down modes to reduce power consumption.

Device Name	FLASH	IRAM	XRAM	ADC	I/O PORT	Package
MC97F2664AL	64 Kbytes	256 bytes	4,096 bytes	15 inputs	61	64LQFP-1010
MC97F2664AL14				15 inputs	61	64LQFP-1414
MC97F2664AUB				15 inputs	61	64QFN
MC97F2464AQ				10 inputs	41	44MQFP
MC97F2464AL				10 inputs	41	44LQFP

Table 1.1 Ordering Information of MC97F2664A

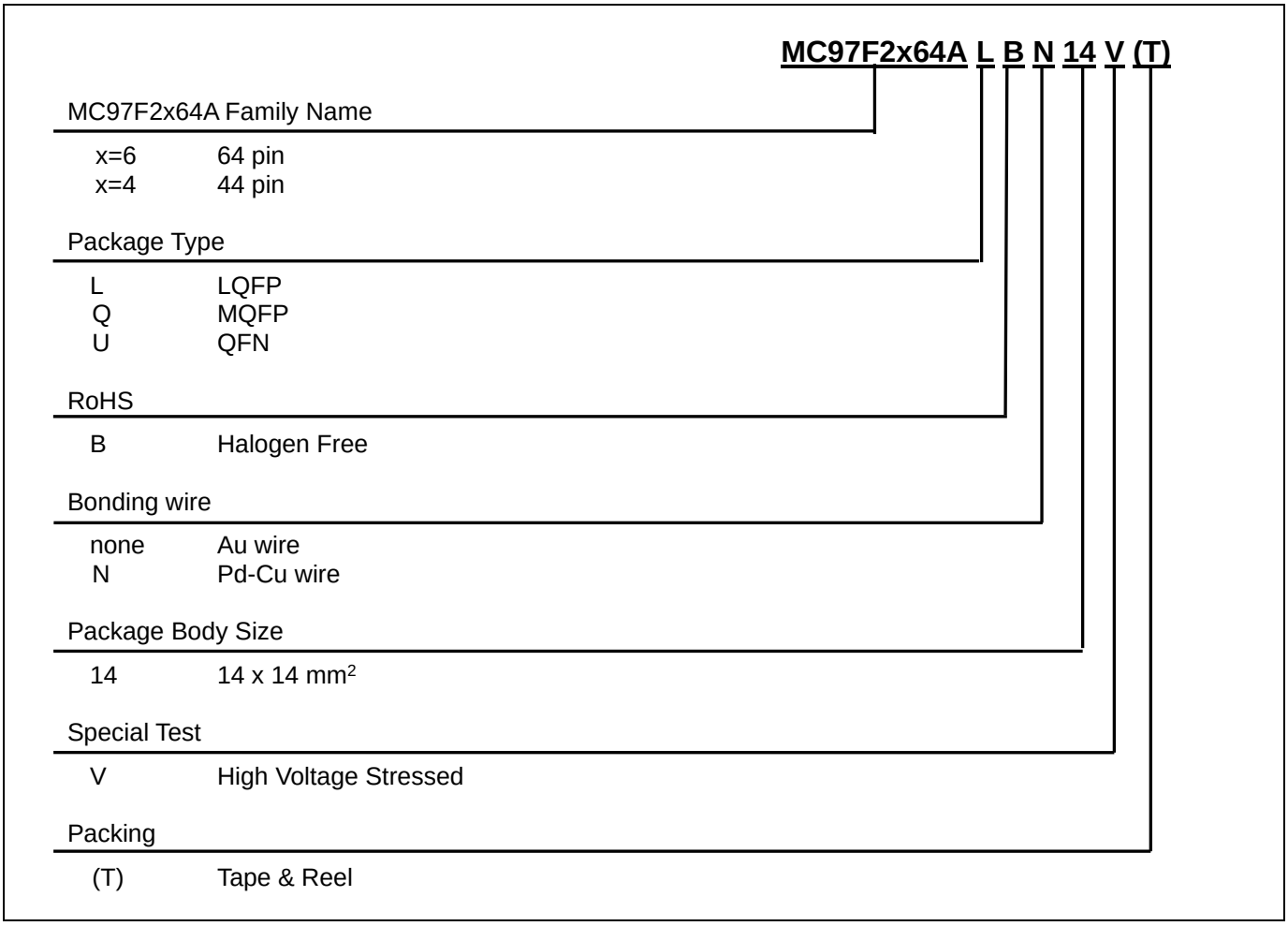


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 64 Kbytes Flash with self read/write capability
  - On Chip debug and In-System Programming(ISP)
  - Endurance : 10,000 times(Sector 0~1019)
    100,000 times(Sector 1020~1023)
  - Retention : 10 years (Min)
- **256 bytes IRAM**
- **4,096 bytes XRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 61 Ports
    (P0, P1,P2,P3,P4,P5,P6,P7[4:0])
- **Basic Interval Timer (BIT)**
  - 8-bit× 1-ch
- **Watch Dog Timer (WDT)**
  - 8-bit× 1-ch
  - 5kHz internal RC oscillator
- **Timer/Counter**
  - 8-bit× 4-ch(T0/T1/T2/T3),
  - 16-bit× 6-ch (T4/T5/T6/T7/T8/T9)
- **Programmable Pulse Generation**
  - Pulse generation (by T4/T5/T6/T7/T8/T9)
  - 8-Bit PWM (by T0/T1/T2/T3)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz
- **Buzzer**
  - 8-bit× 1-ch
- **SPI 2/3**
  - 8-bit× 2-ch
- **UART 2/3/4**
  - 8-bit× 3-ch
- **USI0/1 (UART + SPI + I2C)**
  - 8-bit UART × 2-ch, 8-bit SPI × 2-ch and I2C × 2-ch
- **12-bit A/D Converter**
  - 15 Input channels
- **16-Bit CRC/Checksum Generator**
  - Auto CRC/Checksum mode
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 12 level detect (1.85/2.20/2.32/2.44/2.59/2.75/2.93/ 3.14/3.38/3.67/4.00/4.40V)
- **Low Voltage Indicator**
  - 11 level detect (2.20/2.32/2.44/2.59/2.75/2.93/3.14/ 3.38/3.67/4.00/4.40V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0 ~ EINTA, EINT10 ~ EINT19) (21)
  - Timer0/1/2/3/4/5/6/7/8/9 (14)
  - WDT (1), BIT (1), WT (1)
  - SPI 2/3 (2), UART 2/3/4 (6), USI0/1 (4)
  - ADC (1), Stack OVF (1)
- **Internal RC Oscillator**
  - Internal RC frequency:
    16MHz ±2.0% (T_A= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.2V ~ 5.5V (@ 32 ~ 38kHz with SX-tal)
  - 2.2V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal)
  - 2.7V ~ 5.5V (@ 0.4 ~ 12.0MHz with X-tal)
  - 3.0V ~ 5.5V (@ 0.4 ~ 16.0MHz with X-tal)
  - 2.2V ~ 5.5V (@ 0.5MHz ~ 16MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 125ns (@16MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4-16MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 64-Pin LQFP-1010
  - 64-Pin LQFP-1414
  - 64-Pin QFN
  - 44-Pin MQFP
  - 44-Pin LQFP
  - Pb-free package

Subject	MC97F2664A	MC97F2664
Internal RC frequency (IRC)	Tolerance TA= 0°C to +50°C : ±2.0% TA= -20°C to +85°C : ±3.0% TA= -40°C to +85°C : ±4.0%	Tolerance TA= 0°C to +50°C : ±1.5% TA= -20°C to +85°C : ±2.5% TA= -40°C to +85°C : ±3.5%
Supply Current IDD3 (Sub operation)	Typ/Max : 90/180 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃	Typ/Max : 60/90 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃
Operating Voltage and Frequency	VDD: 2.2V to 5.5V, Freq.: Up to 16MHz - 2.2V to 5.5V @ 32 to 38kHz with x-tal - 2.2V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 12MHz with x-tal - 3.0V to 5.5V @ 0.4 to 16MHz with x-tal - 2.2V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 12MHz with x-tal - 3.0V to 5.5V @ 0.4 to 16MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC
Power-On Reset Characteristics	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/5.0[V/ms]
ADC Channel Input Voltage	1.95V @ ADSEL[3:0] = “1111b”	1.8V @ ADSEL[3:0] = “1111b”
x-tal filter selectable (XTFLSR Register)	x-tal filter selection register for noise immunity - 12.5MHz < x-tal ≤ 16.5MHz - 10.5MHz < x-tal ≤ 12.5MHz - 8.5MHz < x-tal ≤ 10.5MHz - 6.5MHz < x-tal ≤ 8.5MHz - 4.5MHz < x-tal ≤ 6.5MHz - x-tal ≤ 4.5MHz	Not supported
LVR	12 Level Selectable - 1.85V, 2.2V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V
LVI	11 Level Selectable - 2.2V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V
CRC/Checksum Generator	Flash CRC/Checksum Generator - Auto Mode	Not supported
Specific Area for Write Protection	8 kinds of protection size selectable - Address 0100H – 03FFH - Address 0100H – 07FFH - Address 0100H – 0BFFH - Address 0100H – 0FFFH - Address 0100H – F7FFH - Address 0100H – FBFFH - Address 0100H – FDFFH - Address 0100H – FEFFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH
Full-flash erase mode method	Sector erase mode	Sector and byte erase mode
Configure mirror registers	Supported configure mirror registers	Not supported

Table 1.2 Difference among MC97F2664A and MC97F2664

1.3 Development tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC97F2664A is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD2 emulator and debugger

The OCD2 (On Chip Debug 2) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD2 interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD2 can read or change the value of MCU internal memory and I/O peripherals. And the OCD2 also controls MCU internal debugging logic, it means OCD2 controls emulation, step run, monitoring, etc.

The OCD2 is very flexible, powerful and faster than OCD1(Real time monitoring, RAM break, Emulation time measuring…). The MC97x series is supported by only OCD2.

The OCD2 Debugger program works on all Microsoft-Windows operating system.

If you want to see more details, please refer to OCD2 debugger manual. You can download debugger S/W and manual from our web-site(http://www.abov.co.kr).

Connection:

- DSCL (MC97F2664A P62 port)
- DSDA (MC97F2664A P63 port)
- RTIME (MC97F2664A RUNFLAG port, Option)

NOTE) MC97F2664A Use Only OCD2.

OCD2 connector diagram: Connect OCD2 with user system

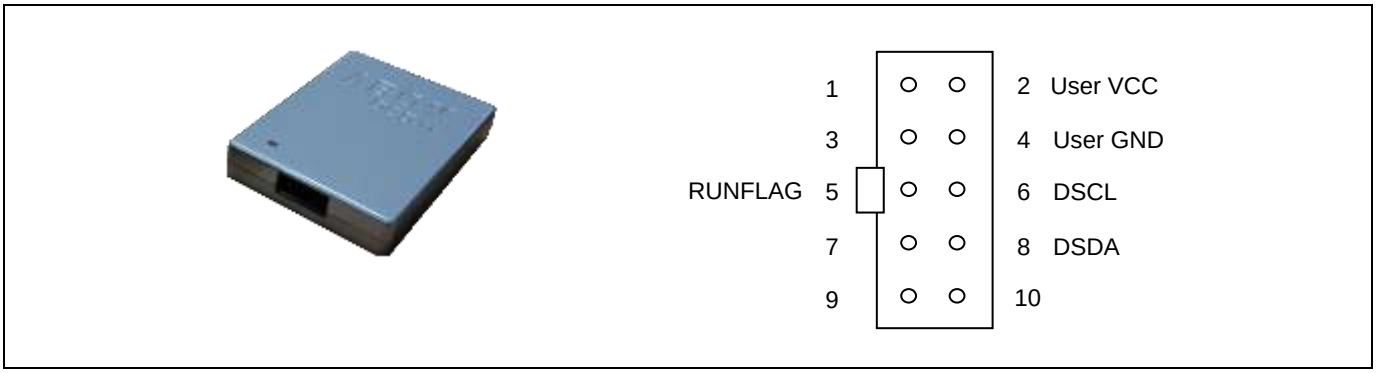


Figure 1.2 Debugger(OCD2) and Pin description

1.3.3 Programmer

Single programmer : E-PGM+

- It programs MCU device directly.

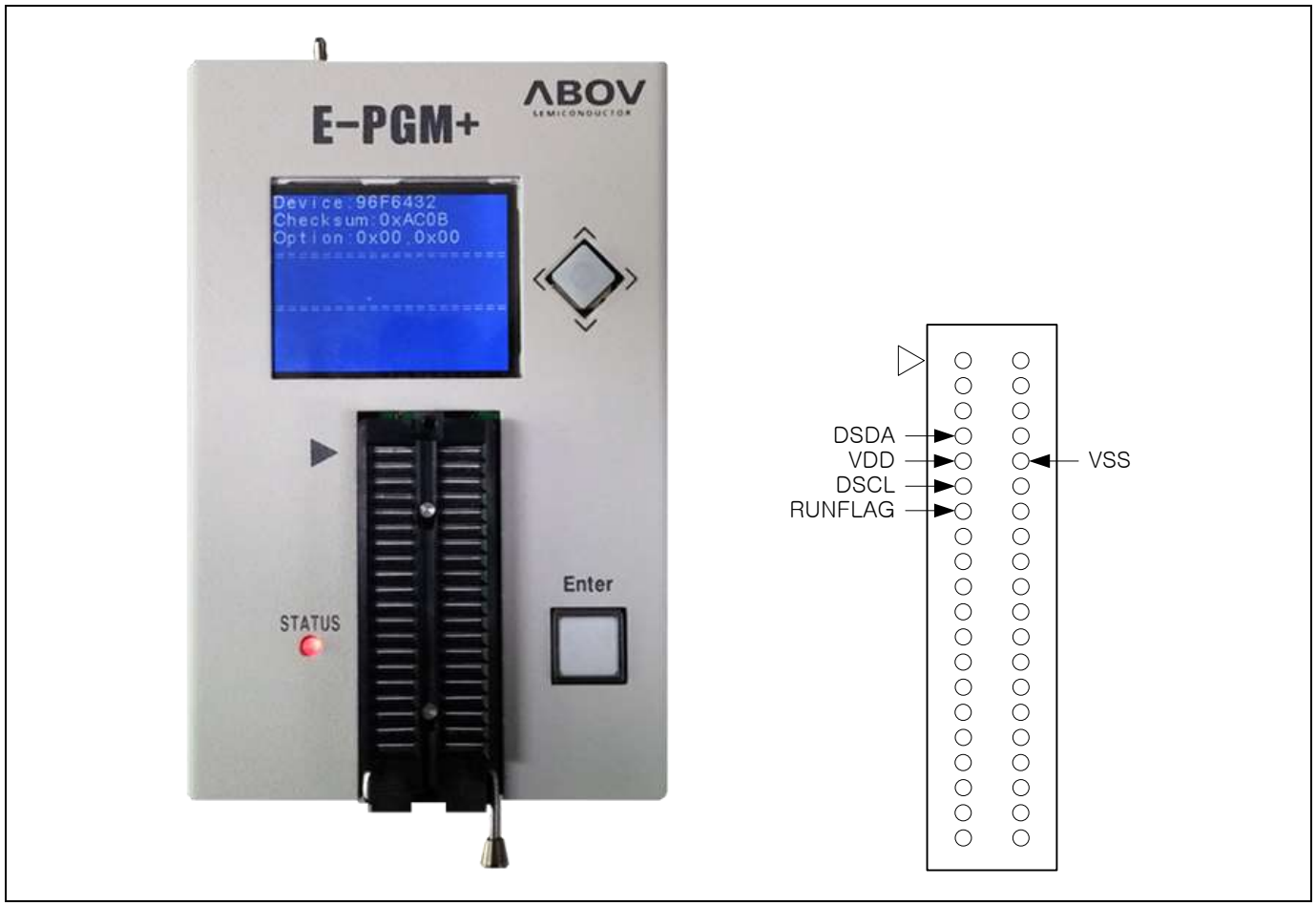


Figure 1.3 E-PGM+(Single writer)

OCD2 emulator :

- It can write code to MCU device too, because OCD debugger supports ISP (In System Programming). It does not require additional H/W, except developer's target system.

Gang programmer : E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of MC97F2664A is MTP Type. This flash is accessed by serial data format. There are five pins(DSCL, DSDA, RUNFLAG, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P62	I	Serial clock pin. Input only pin.
DSDA	P63	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.
RUNFLAG	RUNFLAG	I/O	On chip debugger run flag with a pull-down resistor.

Table 1.3 Descriptions of pins which are used to programming/reading the Flash

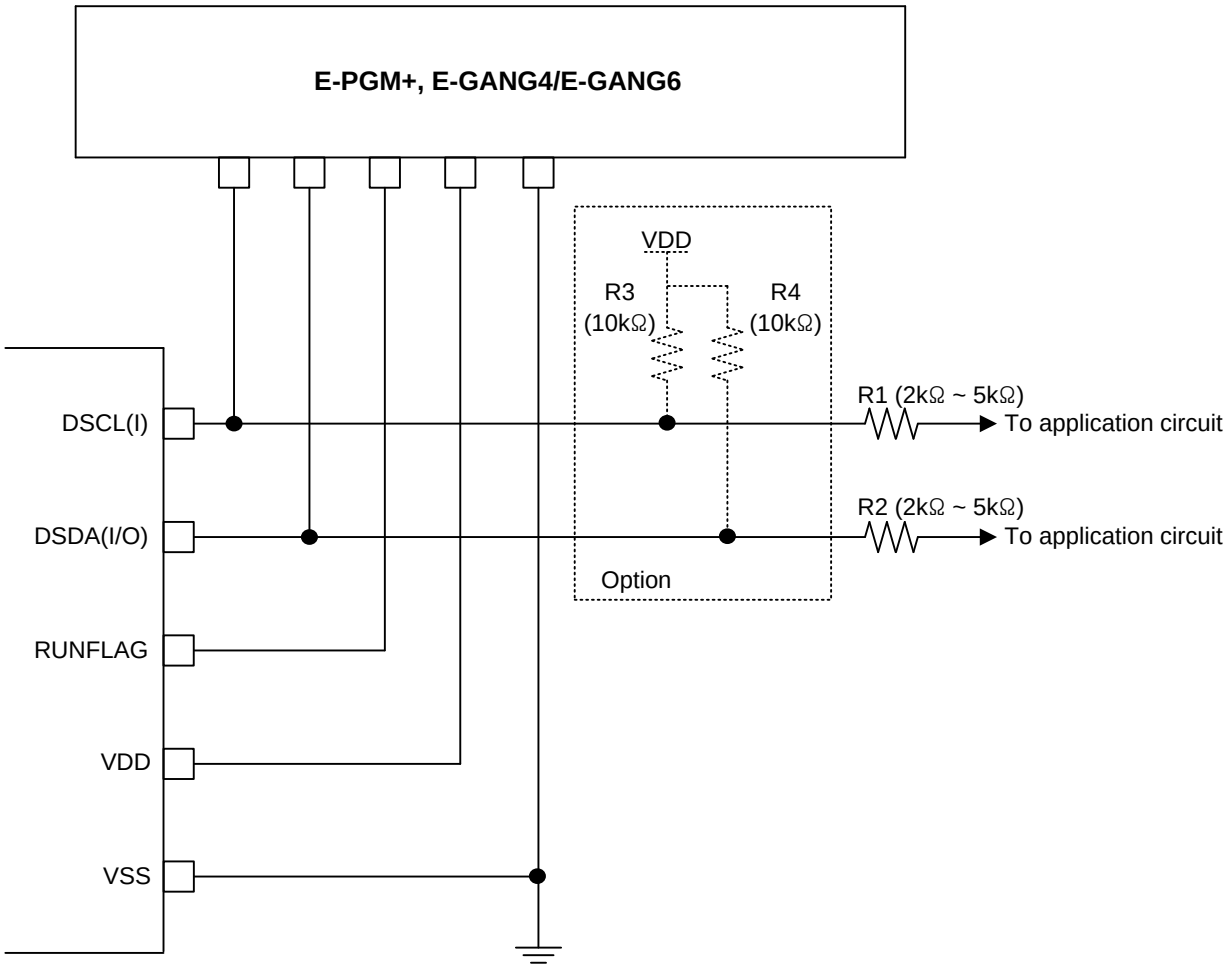
1.4.2 On-Board programming

The MC97F2664A needs only five signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 5 signal lines that are DSCL, DSDA, RUNFLAG, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.
3. The RUNFLAG has an internal pull-down resistor(Typ 50kΩ @ 5V).
4. The DSCL and DSDA have an internal pull-up resistor(Typ 50kΩ @ 5V) during power on or OCD mode.
5. The option is recommended if the DSCL and DSDL is not used to application circuit. This can increase the stability of the system.

Figure 1.5 PCB design guide for on board programming

2 Block diagram

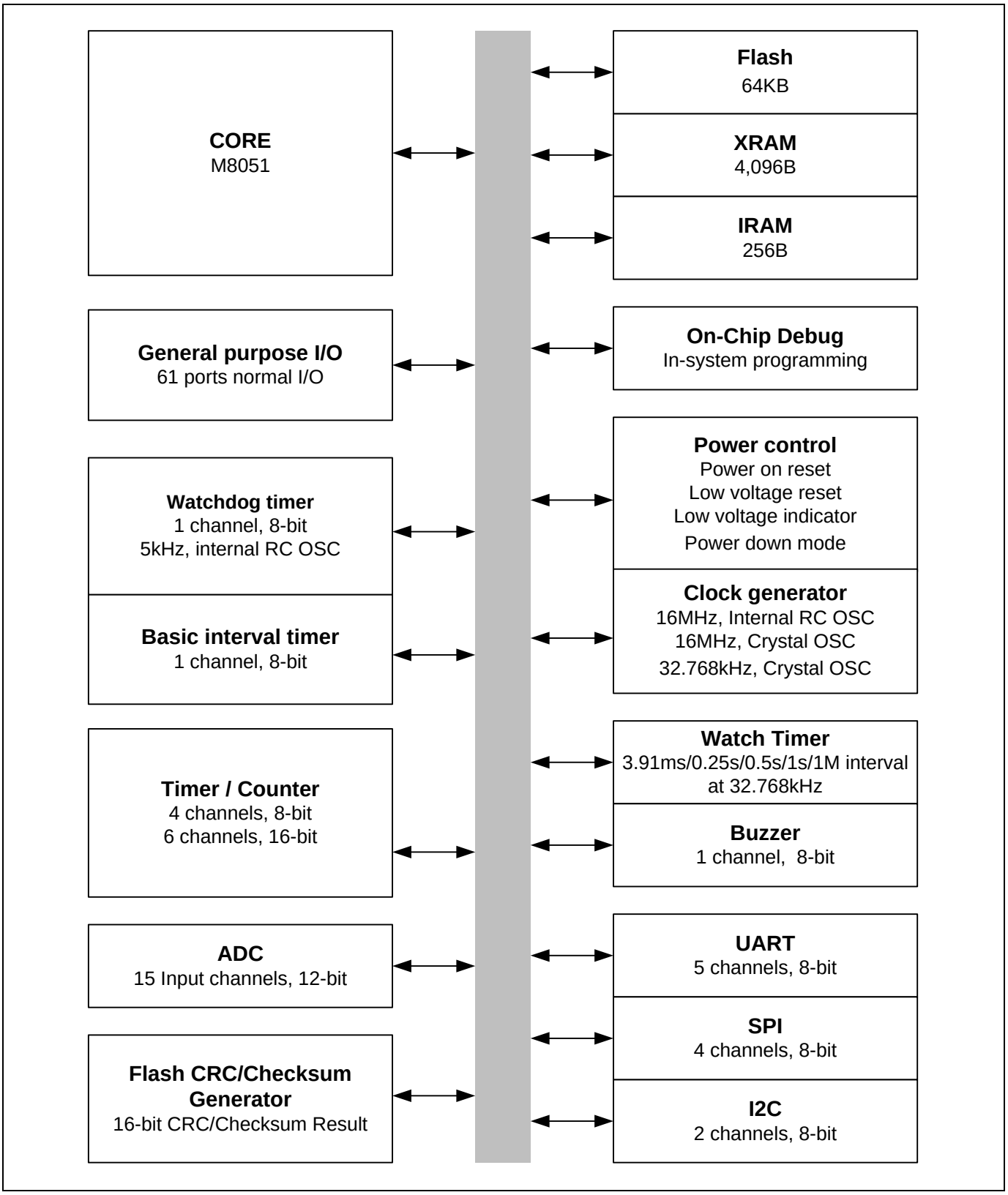
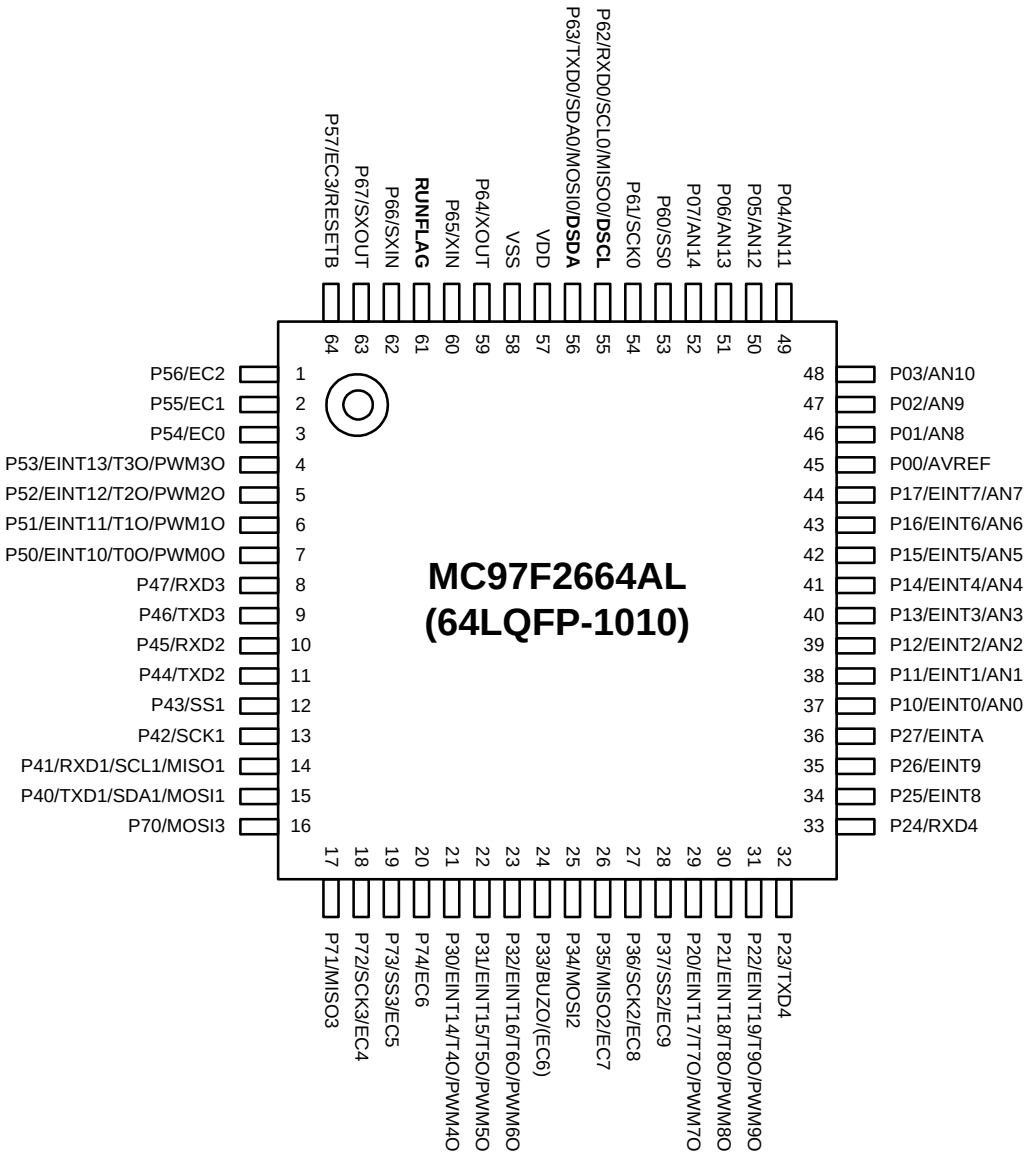


Figure 2.1 Block diagram of MC97F2664A

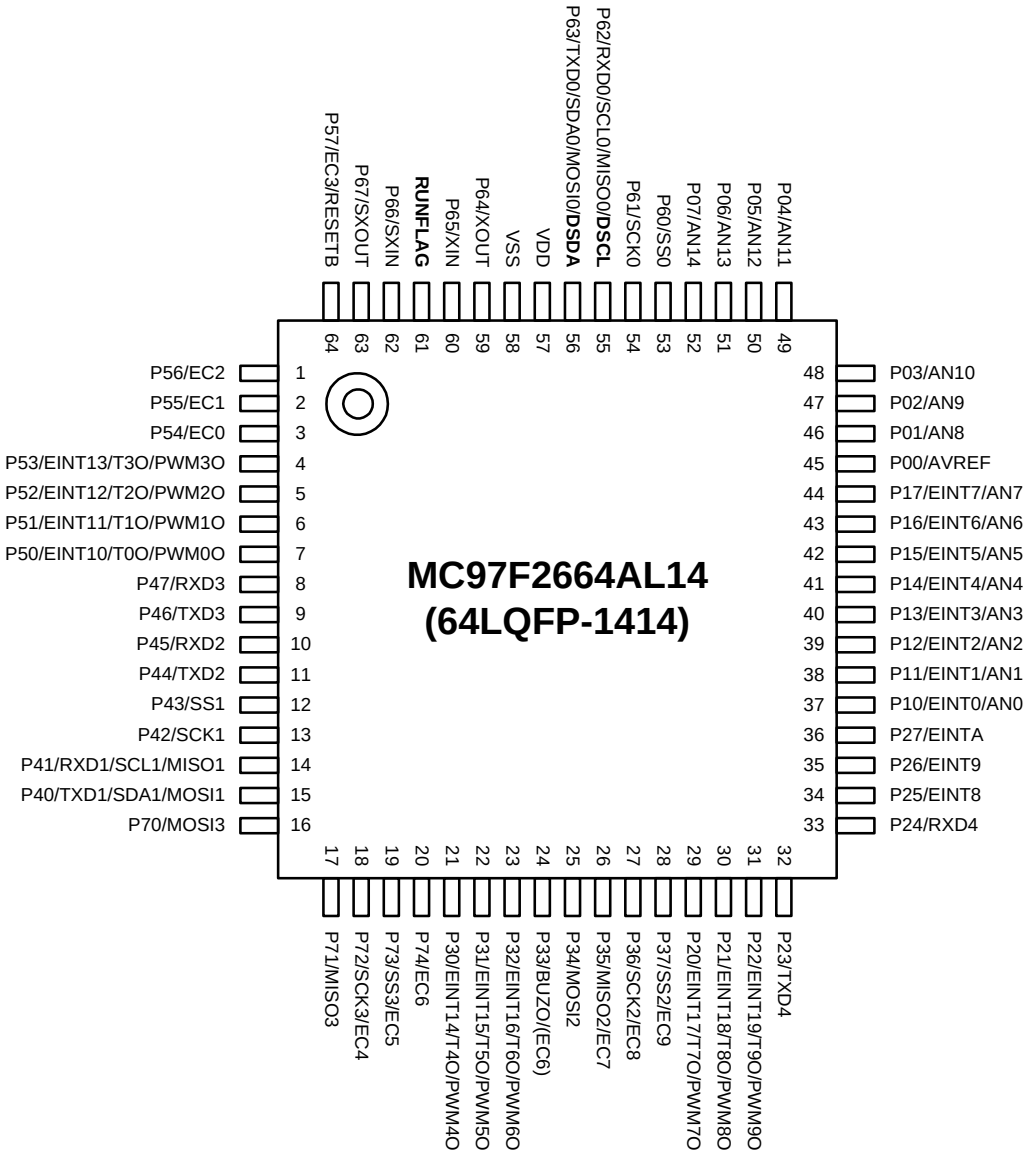
3 Pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P6[2:3] pin as DSCL, DSDA.

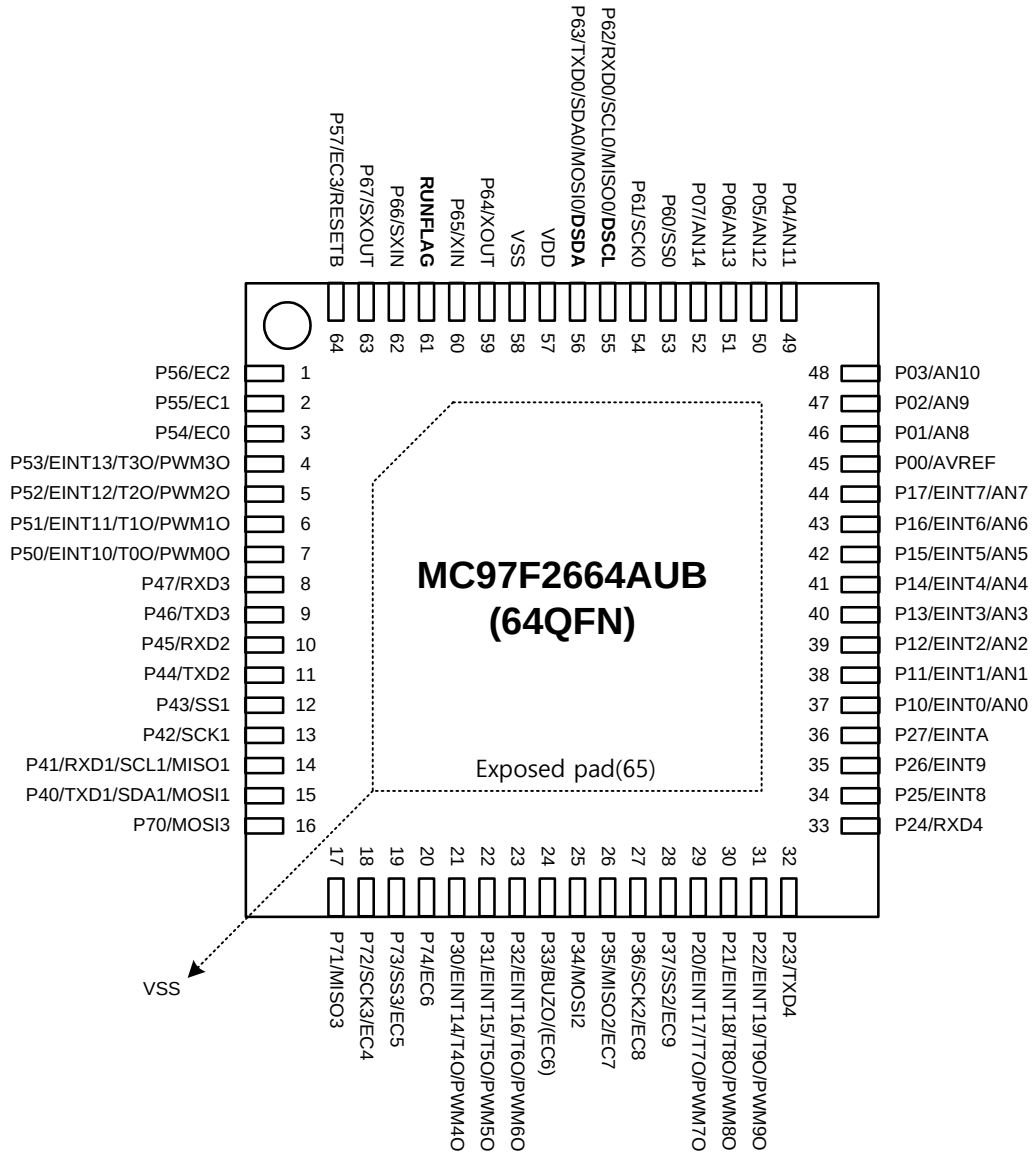
Figure 3.1 MC97F2664AL 64LQFP-1010 Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P6[2:3] pin as DSCL, DSDA.

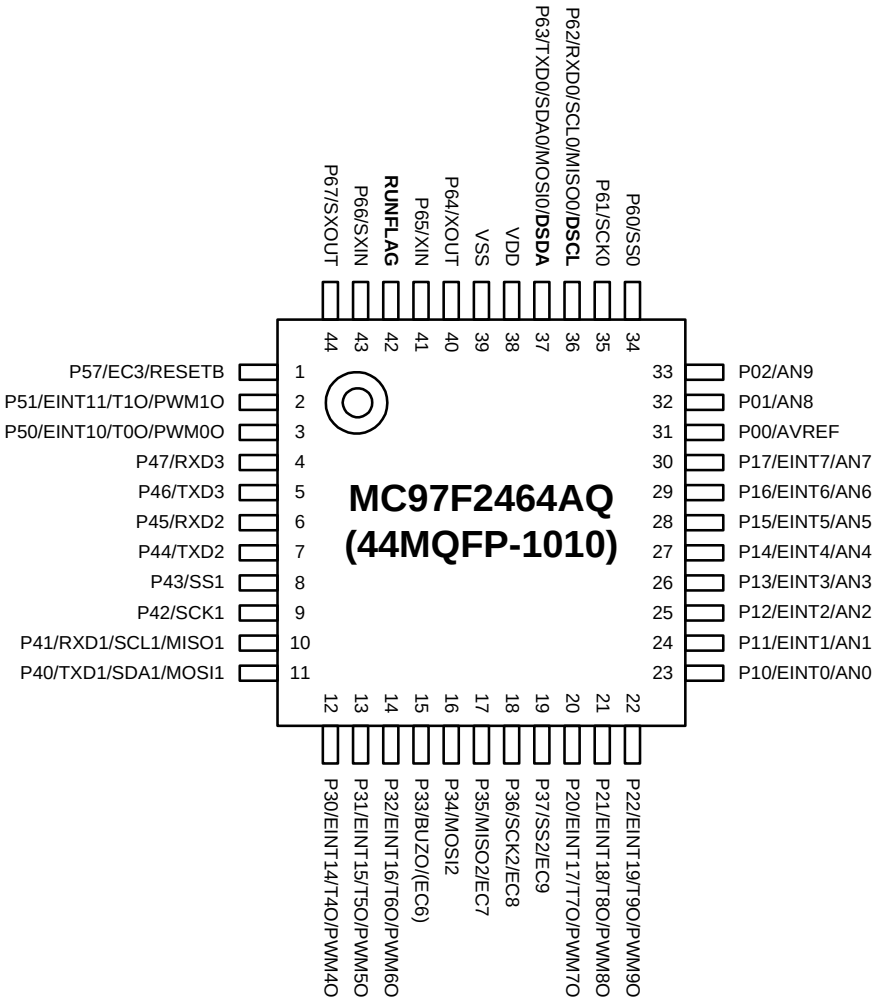
Figure 3.2 MC97F2664AL14 64LQFP-1414 Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P6[2:3] pin as DSCL, DSDA.

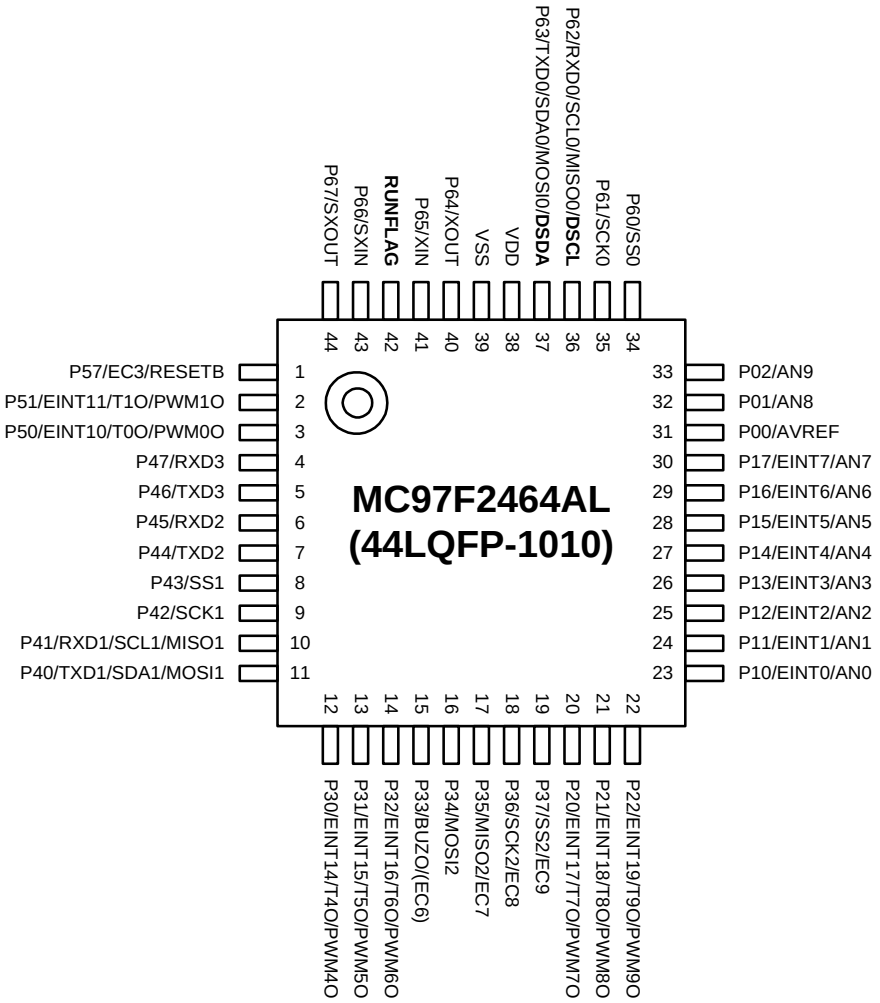
Figure 3.3 MC97F2664AUB 64QFN Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P6[2:3] pin as DSCL, DSDA.
2. The P03-P07, P23-P27, P52-P56 and P7 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 44-pin package is used.

Figure 3.4 MC97F2464AQ 44MQFP Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P6[2:3] pin as DSCL, DSDA.
2. The P03-P07, P23-P27, P52-P56 and P7 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 44-pin package is used.

Figure 3.5 MC97F2464AL 44LQFP Pin Assignment

4 Package Diagram

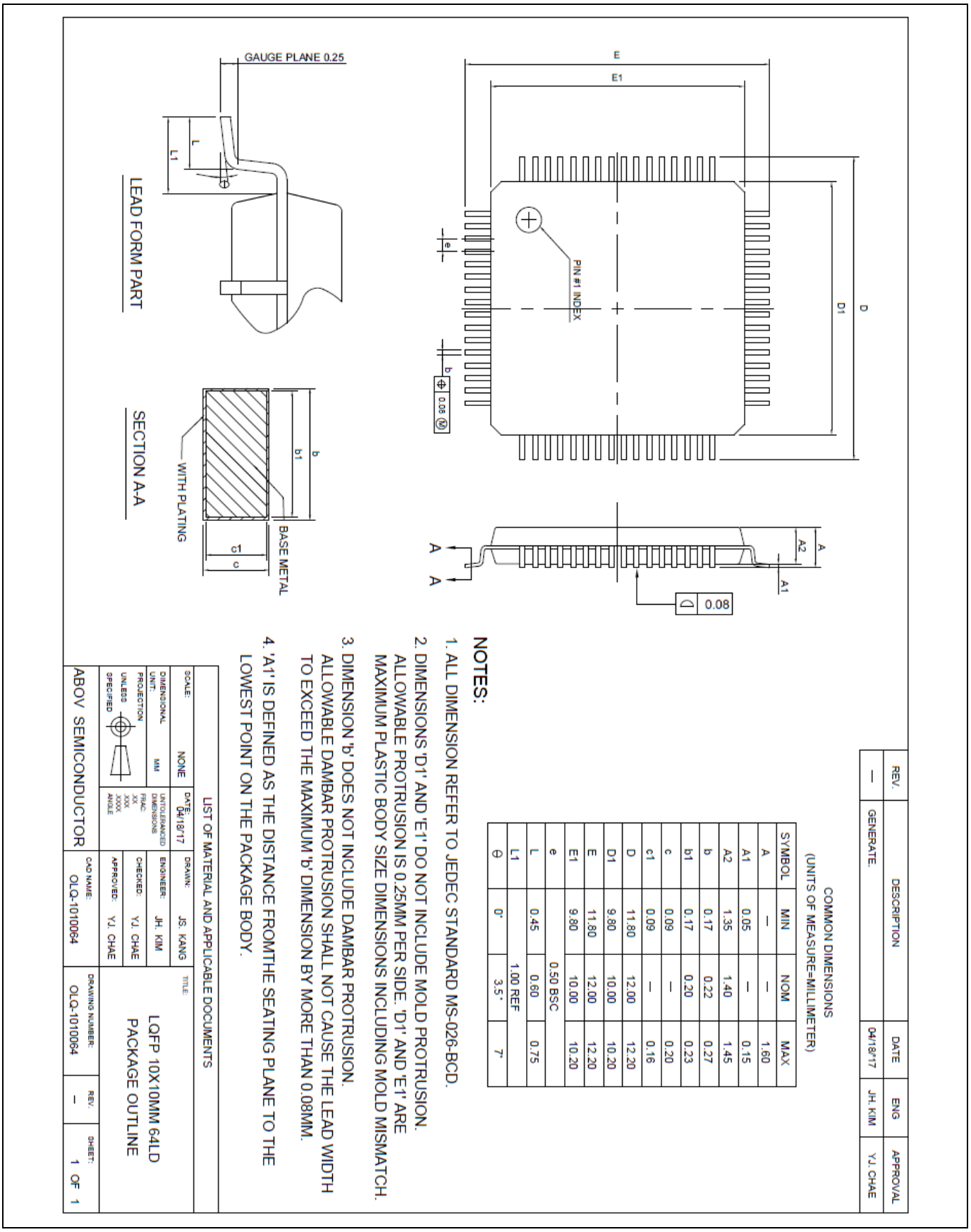


Figure 4.1 64-Pin LQFP-1010 Package

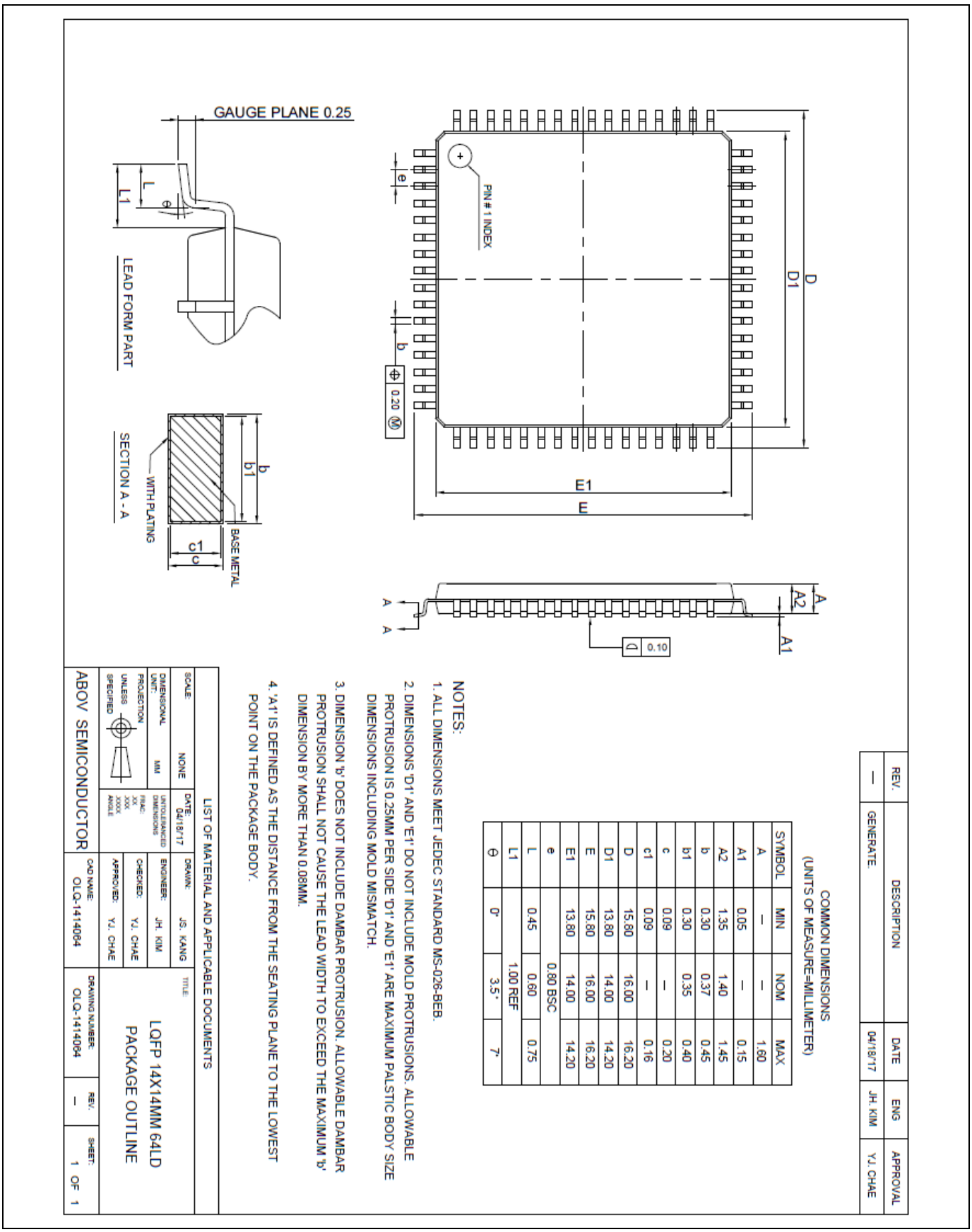


Figure 4.2 64-Pin LQFP-1414 Package

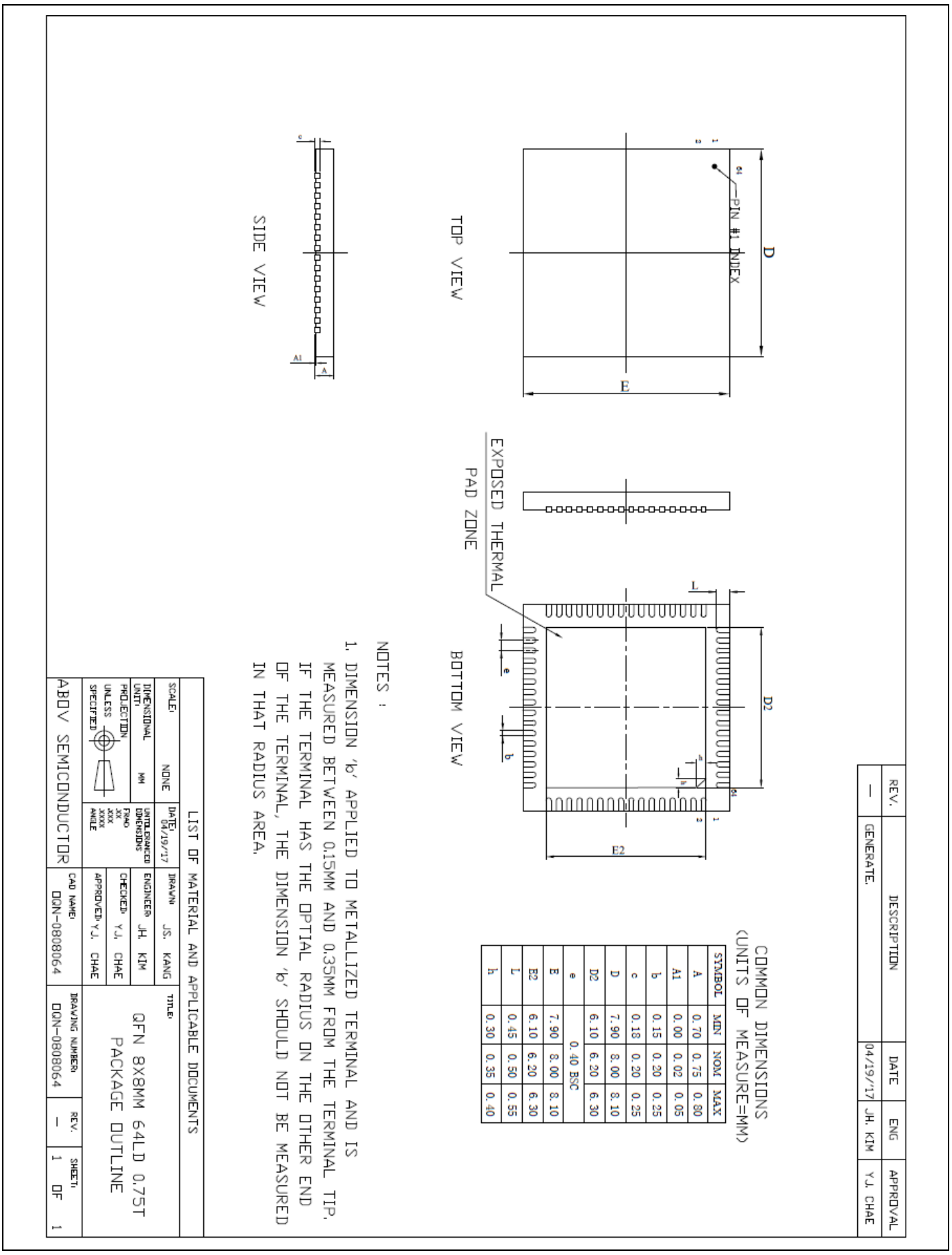
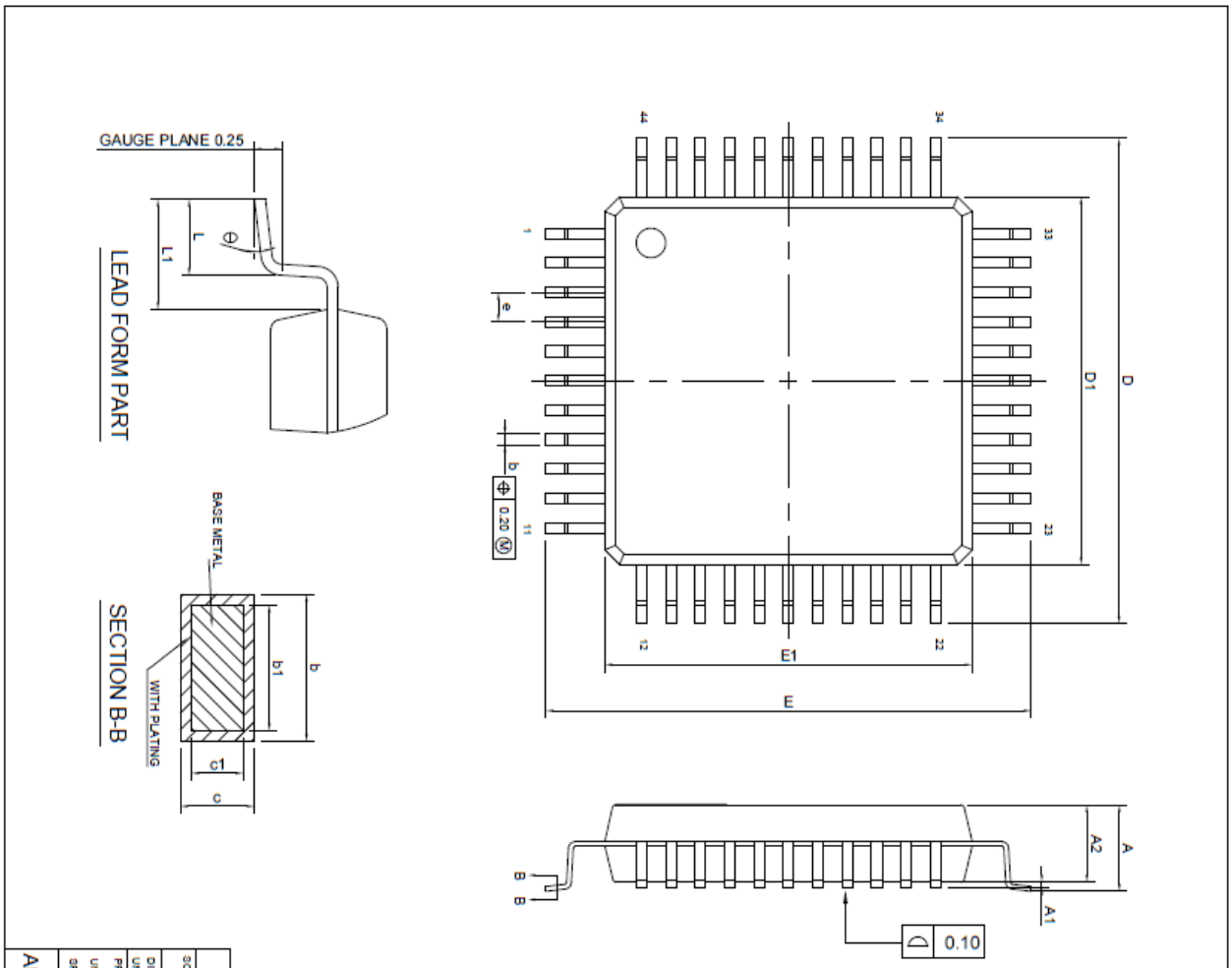


Figure 4.3 64-Pin QFN-0808 Package



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.45
A1	0.00	—	0.25
A2	1.80	2.10	2.20
b	0.28	—	0.45
b1	0.28	0.35	0.41
c	0.11	—	0.23
c1	0.11	0.15	0.19
D	12.90	13.20	13.50
D1	9.80	10.00	10.20
E	12.90	13.20	13.50
E1	9.80	10.00	10.20
e		0.80BSC	
L	0.60	—	1.03
L1		1.60 BSC	
θ	0°	—	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-022-AB.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS 'D1' AND 'E1' DO INCLUDE MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE: MQFP 10X10MM 44LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS TRAC: XX ±0.1 XXX ±0.05 XXXX ANGLE ± 1°	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OMQ-1010044	APPROVED: YJ. CHAE	DRAWING NUMBER: OMQ-1010044 / REV: — / SHEET: 1 OF 1

Figure 4.4 44-Pin MQFP-1010 Package

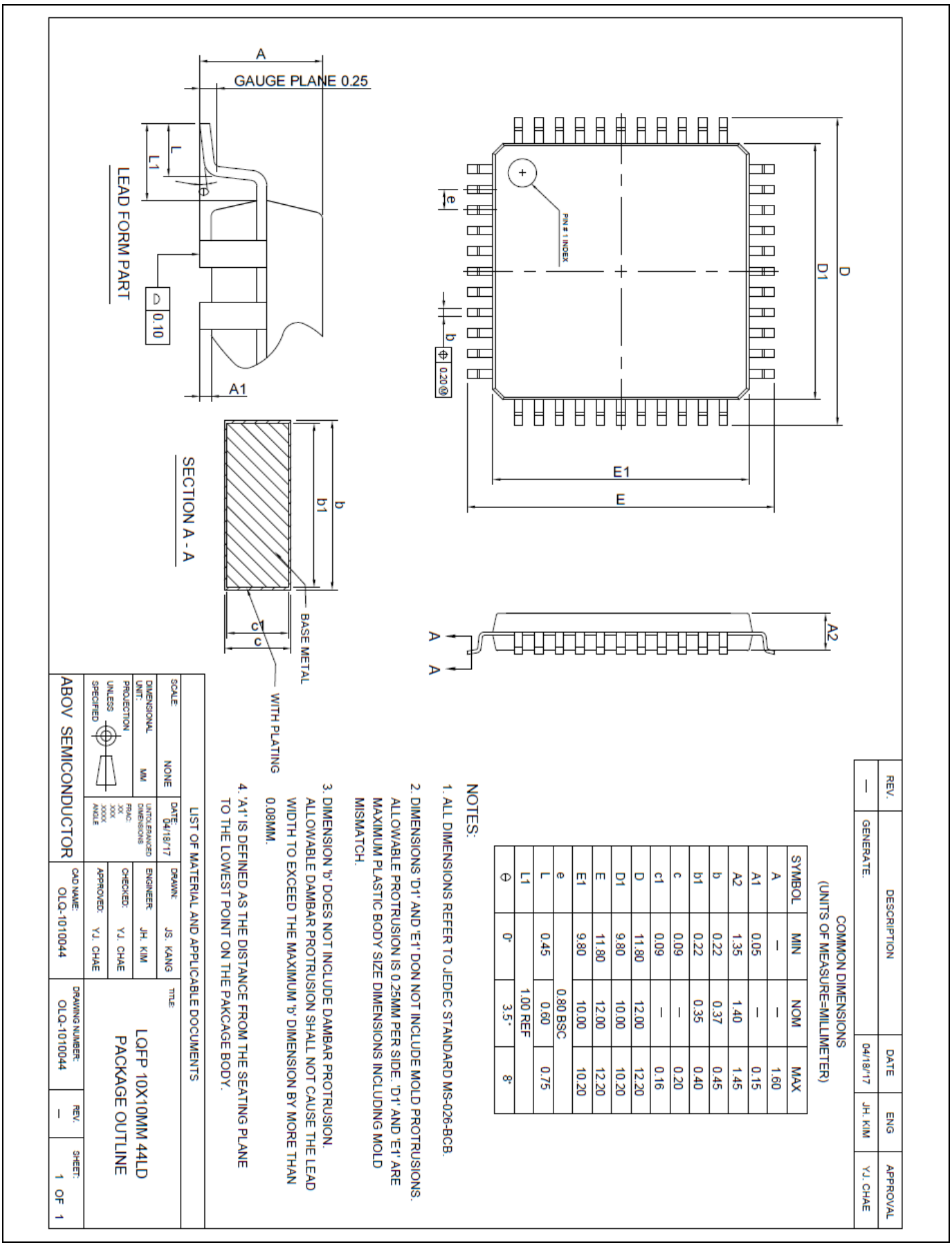


Figure 4.5 44-Pin LQFP-1010 Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P03–P07 are not in the 44-Pin package.	Input	AVERF
P01				AN8
P02				AN9
P03				AN10
P04				AN11
P05				AN12
P06				AN13
P07				AN14
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0/EINT0
P11				AN1/EINT1
P12				AN2/EINT2
P13				AN3/EINT3
P14				AN4/EINT4
P15				AN5/EINT5
P16				AN6/EINT6
P17				AN7/EINT7
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P23–P27 are not in the 44-Pin package.	Input	EINT17/T7O/PWM7O
P21				EINT18/T8O/PWM8O
P22				EINT19/T9O/PWM9O
P23				TXD4
P24				RXD4
P25				EINT8
P26				EINT9
P27				EINTA
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT14/T4O/PWM4O
P31				EINT15/T5O/PWM5O
P32				EINT16/T6O/PWM6O
P33				BUZO/(EC6)
P34				MOSI2
P35				MISO2/EC7
P36				SCK2/EC8
P37				SS2/EC9
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	TXD1/SDA1/MOSI1
P41				RXD1/SCL1/MISO1
P42				SCK1
P43				SS1
P44				TXD2
P45				RXD2
P46				TXD3
P47				RXD3

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P52–P56 is not in the 44-Pin package.	Input	EINT10/T0O/PWM0O
P51				EINT11/T1O/PWM1O
P52				EINT12/T2O/PWM2O
P53				EINT13/T3O/PWM3O
P54				EC0
P55				EC1
P56				EC2
P57				EC3/RESETB
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SS0
P61				SCK0
P62				RXD0/SCL0/MISO0/DSCL
P63				TXD0/SDA0/MOSI0/DSDA
P64				XOUT
P65				XIN
P66				SXIN
P67				SXOUT
P70	I/O	Port 7 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P7 is not in the 44-Pin package.	Input	MOSI3
P71				MISO3
P72				SCK3/EC4
P73				SS3/EC5
P74				EC6
EINT0–EINT7	I/O	External interrupts	Input	P10–P17/AN0–AN7
EINT8				P25
EINT9				P26
EINTA				P27
EINT10	I/O	External interrupt and Timer 0 capture input	Input	P50/T0O/PWM0O
EINT11	I/O	External interrupt and Timer 1 capture input	Input	P51/T1O/PWM1O
EINT12	I/O	External interrupt and Timer 2 capture input	Input	P52/T2O/PWM2O
EINT13	I/O	External interrupt and Timer 3 capture input	Input	P53/T3O/PWM3O
EINT14	I/O	External interrupt and Timer 4 capture input	Input	P30/T4O/PWM4O
EINT15	I/O	External interrupt and Timer 5 capture input	Input	P31/T5O/PWM5O
EINT16	I/O	External interrupt and Timer 6 capture input	Input	P32/T6O/PWM6O
EINT17	I/O	External interrupt and Timer 7 capture input	Input	P20/T7O/PWM7O
EINT18	I/O	External interrupt and Timer 8 capture input	Input	P21/T8O/PWM8O
EINT19	I/O	External interrupt and Timer 9 capture input	Input	P22/T9O/PWM9O
T0O	I/O	Timer 0 interval output	Input	P50/EINT0/PWM0O
T1O	I/O	Timer 1 interval output	Input	P51/EINT1/PWM1O
T2O	I/O	Timer 2 interval output	Input	P52/EINT2/PWM2O
T3O	I/O	Timer 3 interval output	Input	P53/EINT3/PWM3O
T4O	I/O	Timer 4 interval output	Input	P30/EINT4/PWM4O
T5O	I/O	Timer 5 interval output	Input	P31/EINT5/PWM5O
T6O	I/O	Timer 6 interval output	Input	P32/EINT6/PWM6O
T7O	I/O	Timer 7 interval output	Input	P20/EINT7/PWM7O

Table 5.1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
T8O	I/O	Timer 8 interval output	Input	P21/EINT8/PWM8O
T9O	I/O	Timer 9 interval output	Input	P22/EINT9/PWM9O
PWM0O	I/O	Timer 0 PWM output	Input	P50/EINT0/T0O
PWM1O	I/O	Timer 1 PWM output	Input	P51/EINT1/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P52/EINT2/T2O
PWM3O	I/O	Timer 3 PWM output	Input	P53/EINT3/T3O
PWM4O	I/O	Timer 4 PWM output	Input	P30/EINT4/T4O
PWM5O	I/O	Timer 5 PWM output	Input	P31/EINT5/T5O
PWM6O	I/O	Timer 6 PWM output	Input	P32/EINT6/T6O
PWM7O	I/O	Timer 7 PWM output	Input	P20/EINT7/T7O
PWM8O	I/O	Timer 8 PWM output	Input	P21/EINT8/T8O
PWM9O	I/O	Timer 9 PWM output	Input	P22/EINT9/T9O
EC0	I/O	Timer 0 event count input	Input	P54
EC1	I/O	Timer 1 event count input	Input	P55
EC2	I/O	Timer 2 event count input	Input	P56
EC3	I/O	Timer 3 event count input	Input	P57/RESETB
EC4	I/O	Timer 4 event count input	Input	P72/SCK3
EC5	I/O	Timer 5 event count input	Input	P73/SS3
EC6	I/O	Timer 6 event count input	Input	P74
EC7	I/O	Timer 7 event count input	Input	P35/MISO2
EC8	I/O	Timer 8 event count input	Input	P36/SCK2
EC9	I/O	Timer 9 event count input	Input	P37/SS2
BUZO	I/O	Buzzer signal output	Input	P33/(EC6)
SCK0	I/O	Serial 0 clock input/output	Input	P61
SCK1	I/O	Serial 1 clock input/output	Input	P42
SCK2	I/O	Serial 2 clock input/output	Input	P36/EC8
SCK3	I/O	Serial 3 clock input/output	Input	P72/EC4
MOSI0	I/O	SPI 0 master output, slave input	Input	P63/TXD0/SDA0/DSDA
MOSI1	I/O	SPI 1 master output, slave input	Input	P40/TXD1/SDA1
MOSI2	I/O	SPI 2 master output, slave input	Input	P34
MOSI3	I/O	SPI 3 master output, slave input	Input	P70
MISO0	I/O	SPI 0 master input, slave output	Input	P62/RXD0/SCL0/DSCL
MISO1	I/O	SPI 1 master input, slave output	Input	P41/RXD1/SCL1
MISO2	I/O	SPI 2 master input, slave output	Input	P35/EC7
MISO3	I/O	SPI 3 master input, slave output	Input	P71
SS0	I/O	SPI 0 slave select input	Input	P60
SS1	I/O	SPI 1 slave select input	Input	P43
SS2	I/O	SPI 2 slave select input	Input	P37/EC9
SS3	I/O	SPI 3 slave select input	Input	P73/EC5
TXD0	I/O	UART 0 data output	Input	P63/SDA0/MOSI0/DSDA
TXD1	I/O	UART 1 data output	Input	P40/SDA1/MOSI1
TXD2	I/O	UART 2 data output	Input	P44
TXD3	I/O	UART 3 data output	Input	P46
TXD4	I/O	UART 4 data output	Input	P23

Table 5.1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
RXD0	I/O	UART 0 data input	Input	P62/SCL0/MISO0/DSCL
RXD1	I/O	UART 1 data input	Input	P41/SCL1/MISO1
RXD2	I/O	UART 2 data input	Input	P45
RXD3	I/O	UART 3 data input	Input	P47
RXD4	I/O	UART 4 data input	Input	P24
SCL0	I/O	I2C 0 clock input/output	Input	P62/RXD0/MISO0/DSCL
SCL1	I/O	I2C 1 clock input/output	Input	P41/RXD1/MISO1
SDA0	I/O	I2C 0 data input/output	Input	P63/TXD0/MOSI0/DSDA
SDA1	I/O	I2C 1 data input/output	Input	P40/TXD1/MOSI1
AVREF	I/O	A/D converter reference voltage	Input	P00
AN0–AN7	I/O	A/D converter analog input channels	Input	P10–P17/EINT0–EINT7
AN8–AN14				P01–P07
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION”	Input	P57/EC3
DSDA	I/O	On chip debugger data input/output	Input	P63/TXD0/SDA0/MOSI0
DSCL	I/O	On chip debugger clock input	Input	P62/RXD0/SCL0/MISO0
RUNFLAG	I/O	On chip debugger run flag with a pull-down resistor	Input	–
XIN	I/O	Main oscillator pins	Input	P65
XOUT				P64
SXIN	I/O	Sub oscillator pins	Input	P66
SXOUT				P67
VDD, VSS	–	Power input pins	–	–

Table 5.1 Normal Pin Description (Concluded)

NOTE)

1. The P57/EC3/RESETB pin is configured as one of the P57/EC3 and the RESETB pin by the “CONFIGURE OPTION”
2. If the P63/TXD0/SDA0/MOSI0/DSDA, P62/RXD0/SCL0/MISO0/DSCL, and RUNFLAG pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P63/TXD0/SDA0/MOSI0/DSDA, P62/RXD0/SCL0/MISO0/DSCL, and RUNFLAG pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
4. The P64/XOUT, P65/XIN, P66/SXIN, and P67/SXOUT pins are configured as a function pin by a software control.
5. The P03-P07, P23-P27, P52-P56, and P7are not in the 44-Pin package..

6 Port Structures

6.1 General Purpose I/O Port

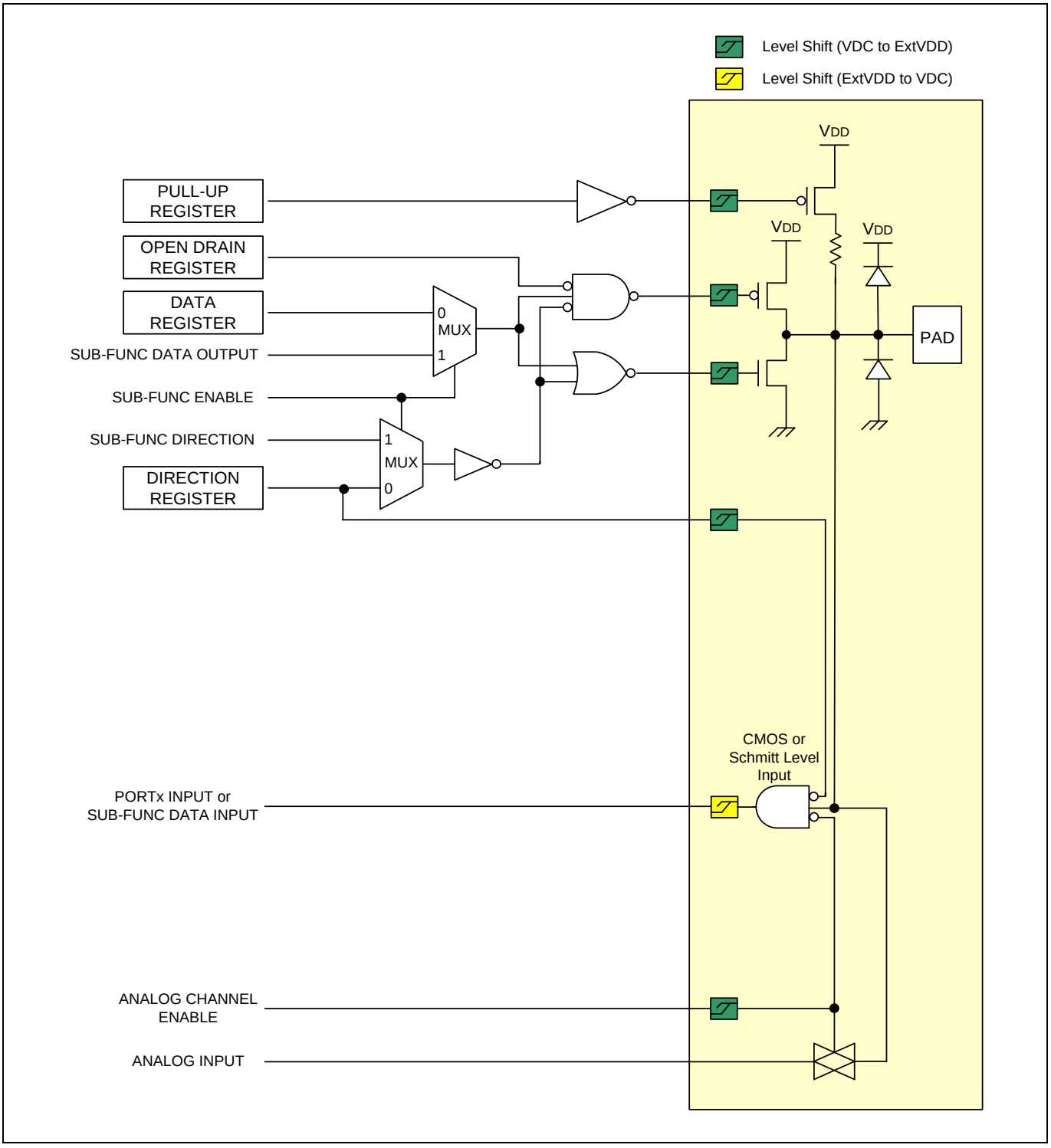


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

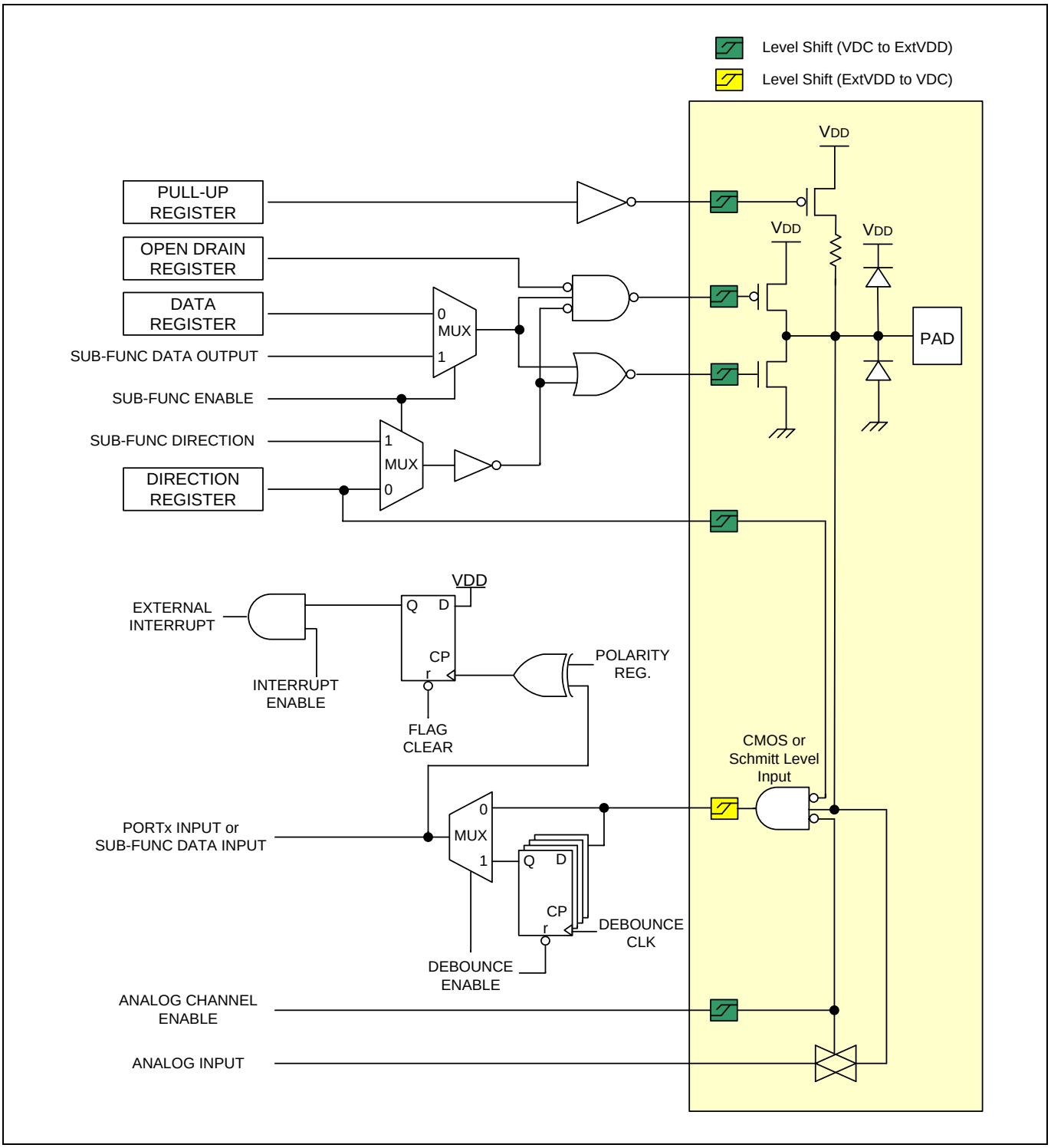


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	–
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to Vss
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-80	mA	Maximum current (ΣI_{OH})
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	120	mA	Maximum current (ΣI_{OL})
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 – +150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions		Min	Max	Units
Operating Voltage	VDD	fx = 32 – 38kHz	SX-tal	2.2	5.5	V
		fx = 0.4 – 4.2MHz	X-tal	2.2	5.5	
		fx = 0.4 – 12MHz		2.7	5.5	
		fx = 0.4 – 16MHz		3.0	5.5	
		fx = 0.5 – 16MHz	Internal RC	2.2	5.5	
Operating Temperature	T_{OPR}	VDD = 2.2 – 5.5V		-40	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral Non-Linear	INL	AVREF=2.7V – 5.5V, fx=8MHz		–	–	±6	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	12bit resolution, 8MHz		20	–	–	us
Analog Input Voltage	V_{AIN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	–		2.2	–	VDD	
VDD19	–	–		–	1.95	–	V
A/DC Input Leakage Current	I_{AIN}	AVREF=5.12V		–	–	2	uA
A/DC Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 111111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Release Level	V_{POR}	–	–	1.4	–	V
Hysteresis	△V	–	–	0.2	–	V
VDD Voltage Rising Time	t_R	0.5V **–** 2.2V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.4 Power-on Reset Characteristics

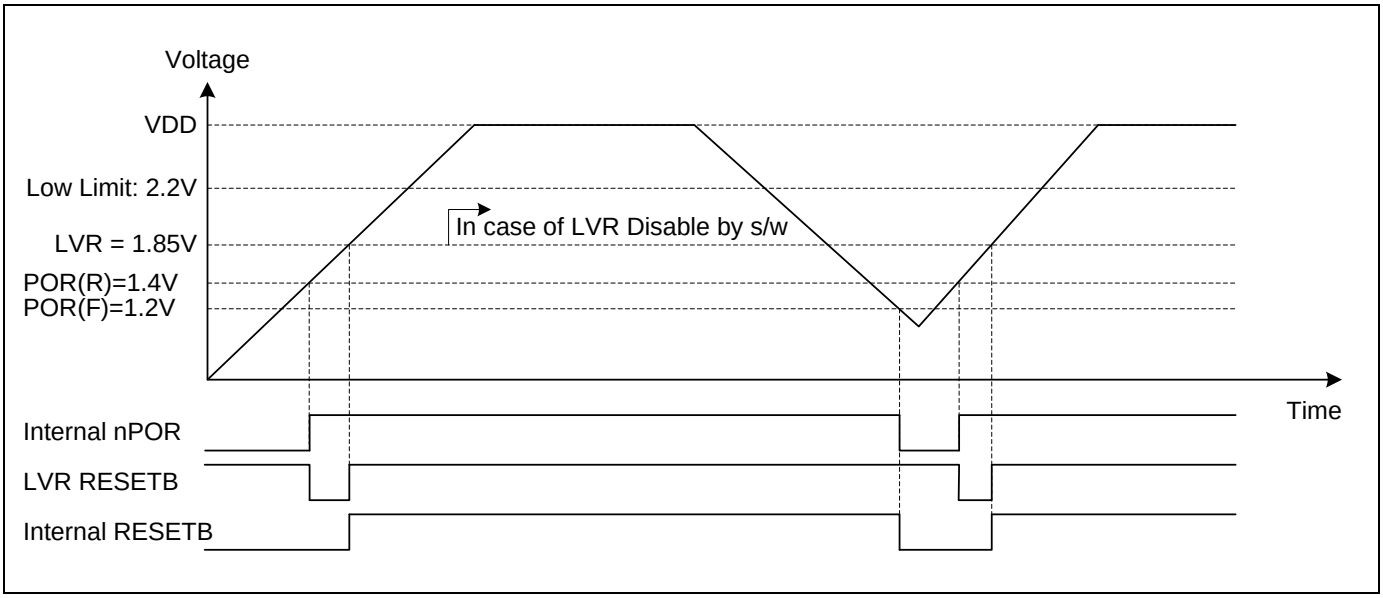


Figure 7.1 Power-on Reset Timing

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.85V.		–	1.85	2.15	V
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD=3V, Run mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD=3V	–	–	0.1	

Table 7.5 LVR and LVI Characteristics

7.6 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{IRC}	VDD = 2.2V **–** 5.5V		–	16	–	MHz
Tolerance	**–**	T_A = 0 °C to + 50°C	With 0.1uF bypass capacitor	-2.0	–	+2.0	%
		T_A = - 20 °C to + 85°C		-3.0	–	+3.0	
		T_A = - 40 °C to + 85°C		-4.0	–	+4.0	
Clock duty ratio	TOD	–		40	50	60	%
Stabilization Time	t_{HFS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7.6 Internal RC Oscillator Characteristics

NOTE)

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.7 Internal WDTRC Oscillator Characteristics

7.8 DC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	V_{IH1}	P1, P2, P3, P5, P6, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	
Input Low Voltage	V_{IL1}	P1, P2, P3, P5, P6, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	
Output High Voltage	V_{OH}	VDD=4.5V, I_{OH} = – 2mA; All output ports		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}=5mA; All output ports except V_{OL2}		–	–	1.0	V
	V_{OL2}	VDD=4.5V, I_{OL}=15mA; P2, P3, P50-P53		–	–	1.0	
Input high leakage current	I_{IH}	All Input ports		–	–	1	uA
Input low leakage current	I_{IL}	All Input ports		– 1	–	–	uA
Pull-up resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=5V	25	50	100	kΩ
			VDD=3V	50	100	200	
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=5V	150	250	400	
			VDD=3V	300	500	700	
Pull-down resistor	R_{PD}	VDD=5V, TA=25°C RUNFLAG		10	20	30	kΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS TA=25°C, VDD=5V		600	1200	2000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS TA=25°C, VDD=5V		2500	5000	10000	kΩ

Table 7.8 DC Characteristics

7.8 DC Characteristics (Continued)

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply current	I_{DD1} (Run)	fxin=16MHz, VDD=5V±10%		–	4.5	9.0	mA
		fxin=12MHz, VDD=3V±10%		–	3.0	6.0	
		fIRC=16MHz, VDD=5V±10%		–	4.0	8.0	
	I_{DD2} (Idle)	fxin=16MHz, VDD=5V±10%		–	2.0	4.0	mA
		fxin=12MHz, VDD=3V±10%		–	1.0	2.0	
		fIRC=16MHz, VDD=5V±10%		–	1.2	2.4	
	I_{DD3}	fsub=32.768kHz VDD=3V±10%, TA=25°C	Sub Run	–	90.0	180.0	uA
	I_{DD4}		Sub Idle	–	8.0	16.0	uA
	I_{DD5}	Stop, VDD=5V±10%, TA=25°C		–	0.5	3.0	uA

Table 7.8 DC Characteristics (Continued)

NOTE)

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator, the f_{IRC} is an internal y RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.9 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 5 V	10	–	–	us
Interrupt Input High, Low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 5 V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5 V (n=0~9)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5 V (n=0~9)	20	–	–	

Table 7.9 AC Characteristics

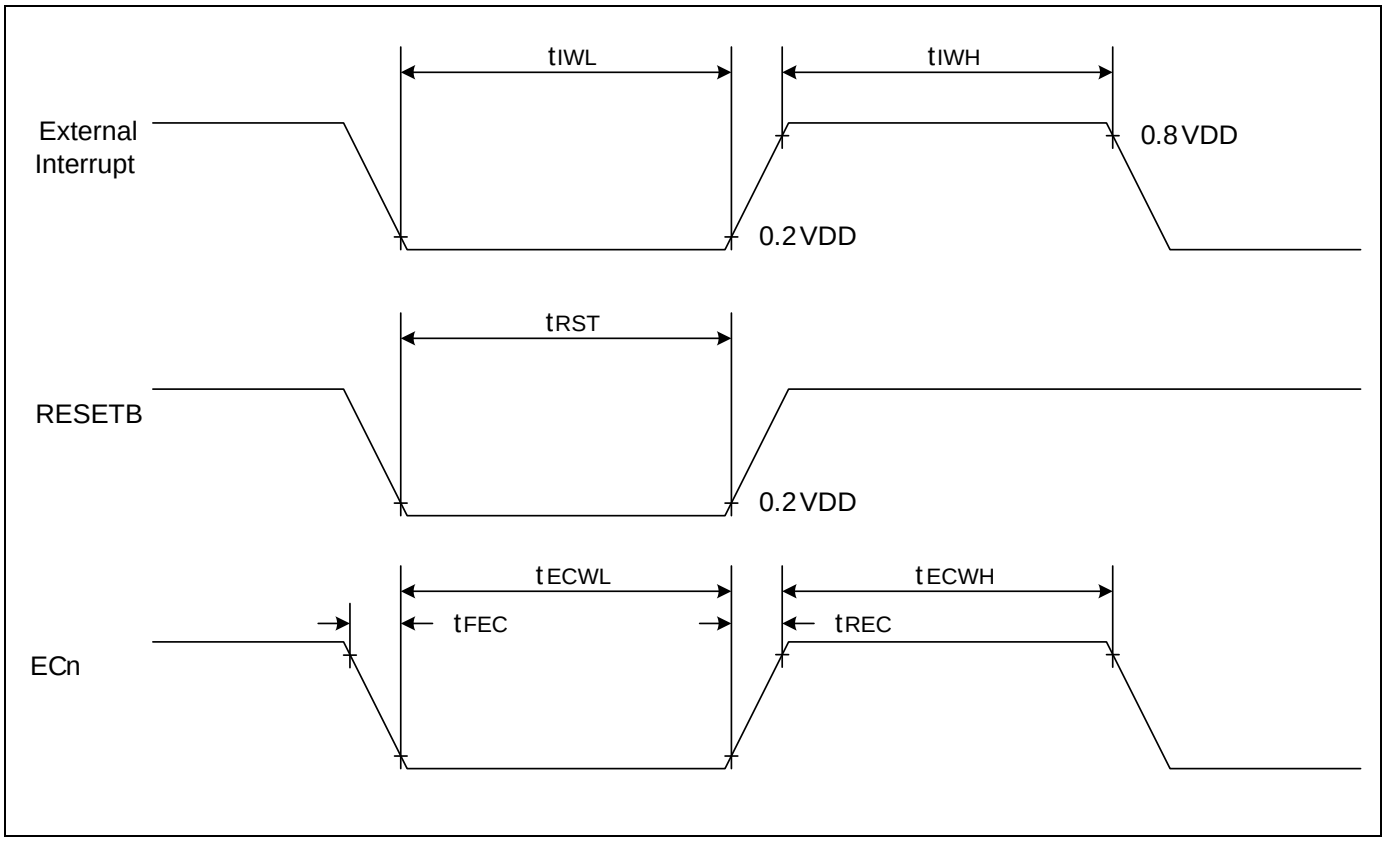


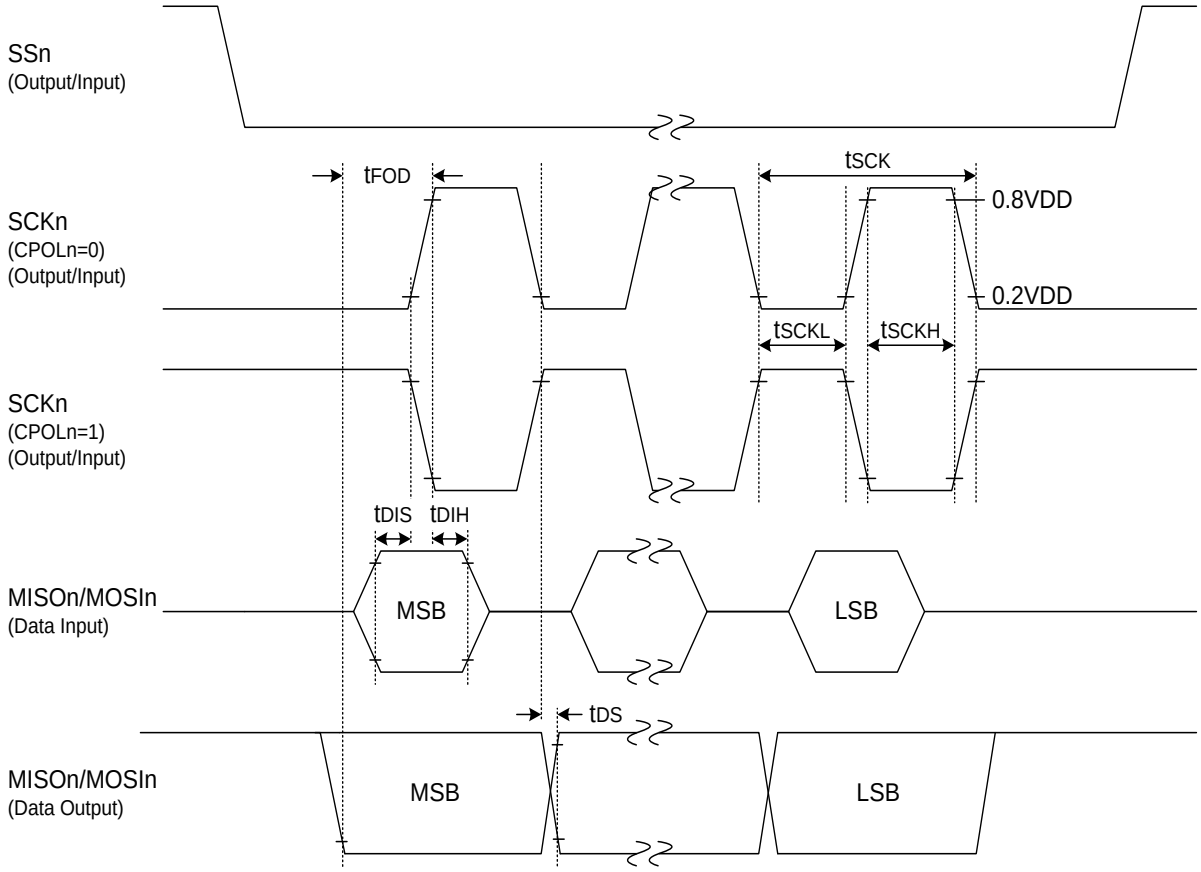
Figure 7.2 AC Timing

7.10 SPI0/1/2/3 Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	100	–	–	
Input Hold Time	t_{DIH}	–	150	–	–	

Table 7.10 SPI0/1/2/3 Characteristics



NOTE)

1. n = 0, 1, 2 and 3

Figure 7.3 SPI0/1/2/3 Timing

7.11 UART0/1/2/3/4 TIMING CHARACTERISTICS

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	$t_{CPU} \times 16$	1650	ns
Output data setup to clock rising edge	t_{S1}	590	$t_{CPU} \times 13$	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	$t_{CPU} \times 8$	970	

Table 7.11 UART TIMING CHARACTERISTICS

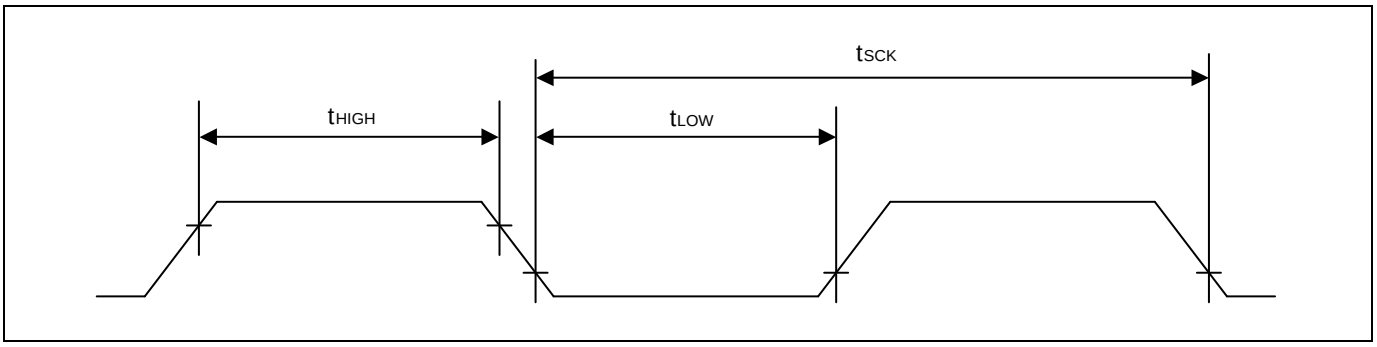


Figure 7.4 Waveform for UART Timing

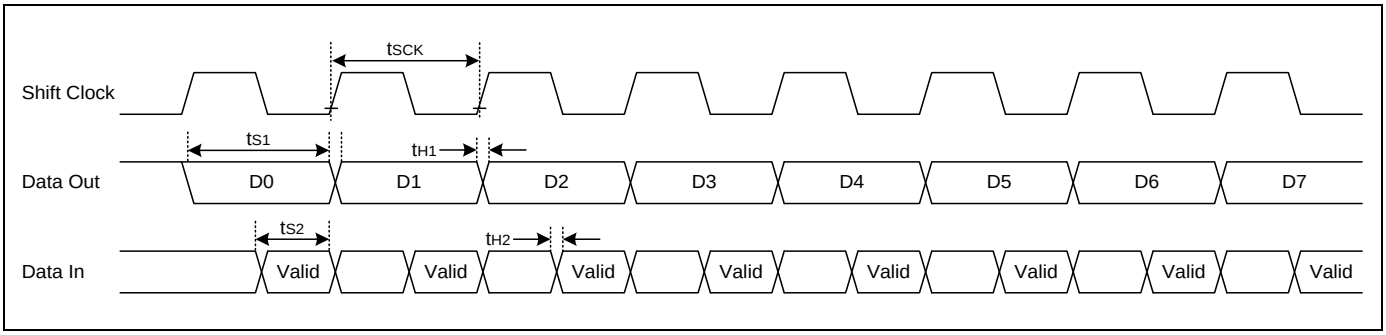


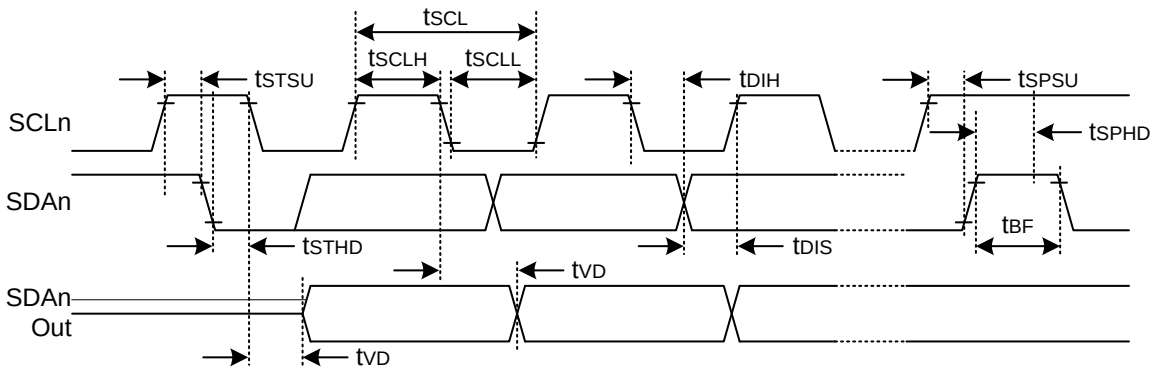
Figure 7.5 Timing Waveform for UART Module

7.12 I2C0/1 Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.12 I2C0/1 Characteristics



NOTE)

1. n= 0 and 1

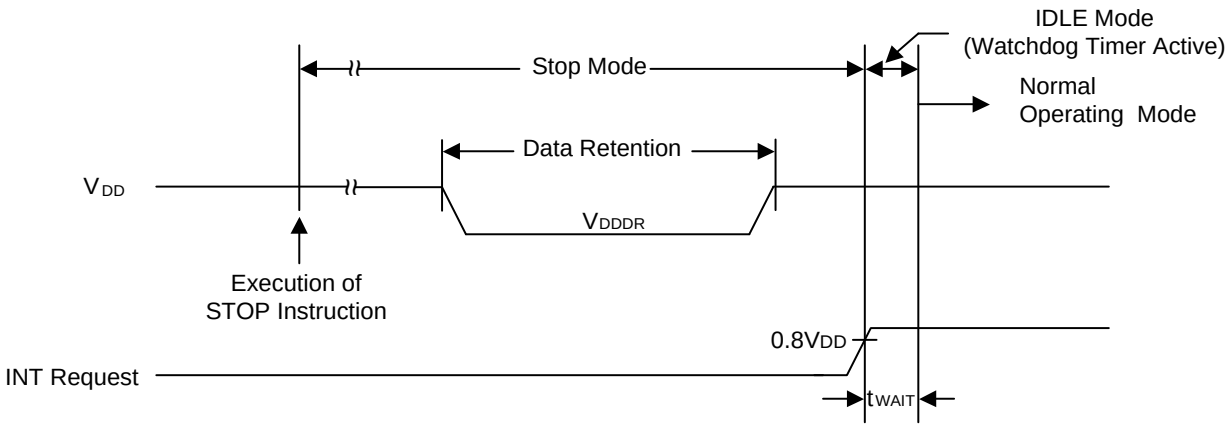
Figure 7.6 I2C0/1 Timing

7.13 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

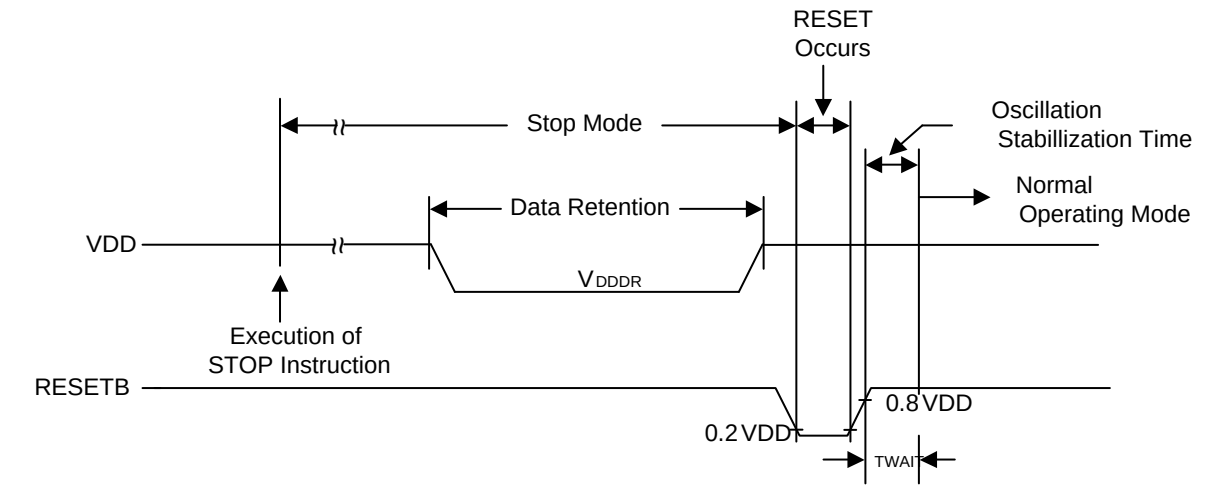
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	2.2	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.2V (T_A = 25°C), Stop mode	–	–	1	uA

Table 7.13 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.7 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 16/f_{IRC}) = (16.4 ms at fx=1MHz).

Figure 7.8 Stop Mode Release Timing when Initiated by RESETB

7.14 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Sector Write Time	t_{FSW}	–		–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–		–	2.5	2.7	
Hard-Lock Time	t_{FHL}	–		–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–		–	–	5	us
Flash Programming Frequency	f_{PGM}	–		0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	T_A = 25°C	Sector 0 to 1019	–	–	10,000	Times
			Sector 1020 to 1023	–	–	100,000	
Flash Data Retention Time	t_{RT}	–		10	–	–	Years

Table 7.14 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.15 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{IN}	fx=1MHz Unmeasured pins are connected to Vss	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.15 Input/Output Capacitance

7.16 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal, Ceramic	Main oscillation frequency	2.2 V – 5.5 V	0.4	–	4.2	MHz
		2.7 V – 5.5 V	0.4	–	12.0	
		3.0 V – 5.5 V	0.4	–	16.0	
External Clock	XIN input frequency	2.2 V – 5.5 V	0.4	–	4.2	MHz
		2.7 V – 5.5 V	0.4	–	12.0	
		3.0 V – 5.5 V	0.4	–	16.0	

Table 7.16 Main Clock Oscillator Characteristics

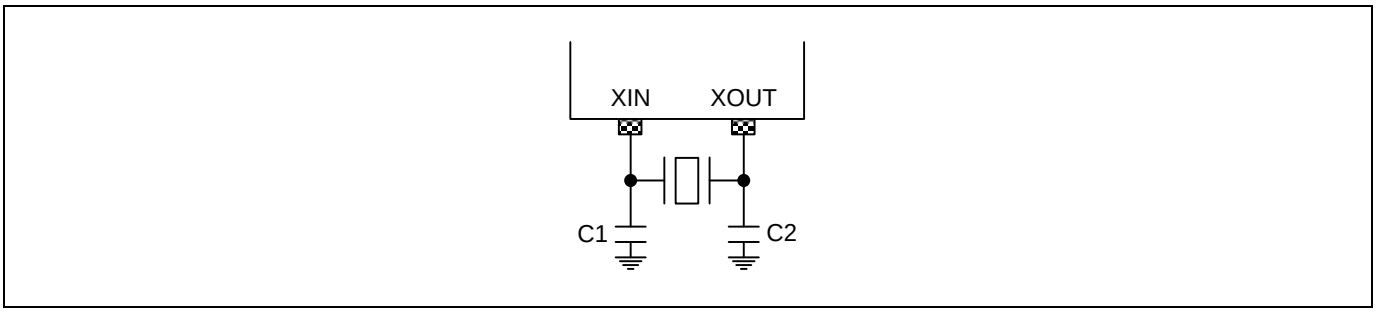


Figure 7.9 Crystal/Ceramic Oscillator

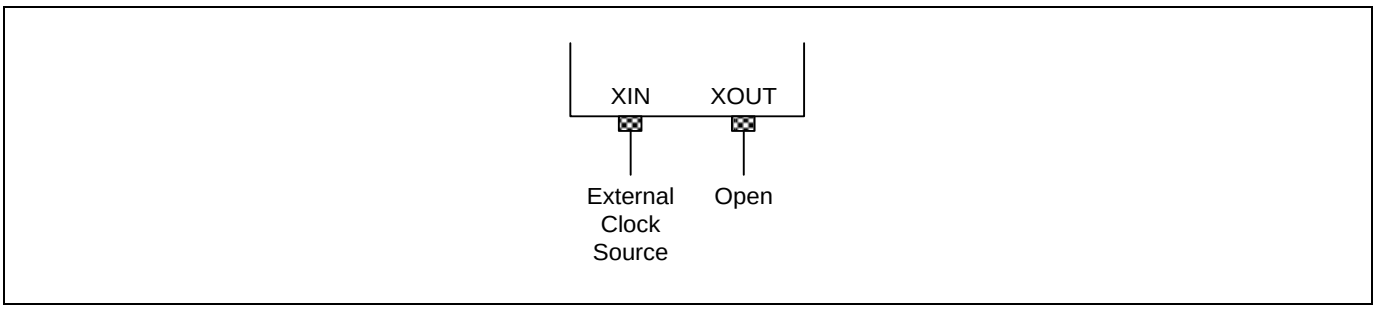


Figure 7.10 External Clock

7.17 Sub Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Sub oscillation frequency	2.2 V – 5.5 V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	

Table 7.17 Sub Clock Oscillator Characteristics

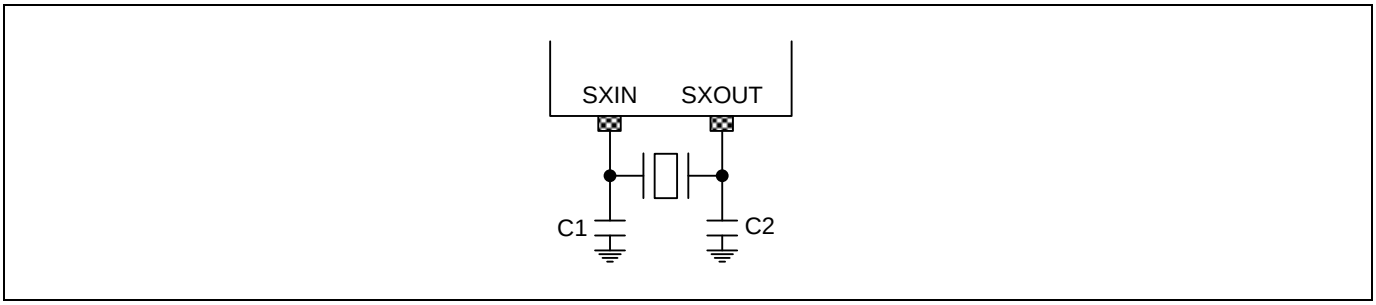


Figure 7.11 Crystal Oscillator

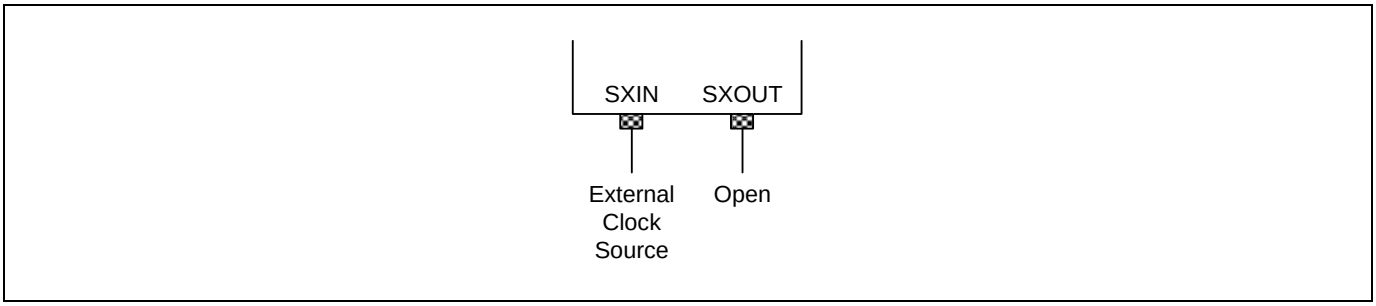


Figure 7.12 External Clock

7.18 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	fXIN ≥ 1 MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	
External Clock	fXIN = 0.4 to 16 MHz XIN input high and low width (t_{XL}, t_{XH})	31	–	1250	ns

Table 7.18 Main Oscillation Stabilization Characteristics

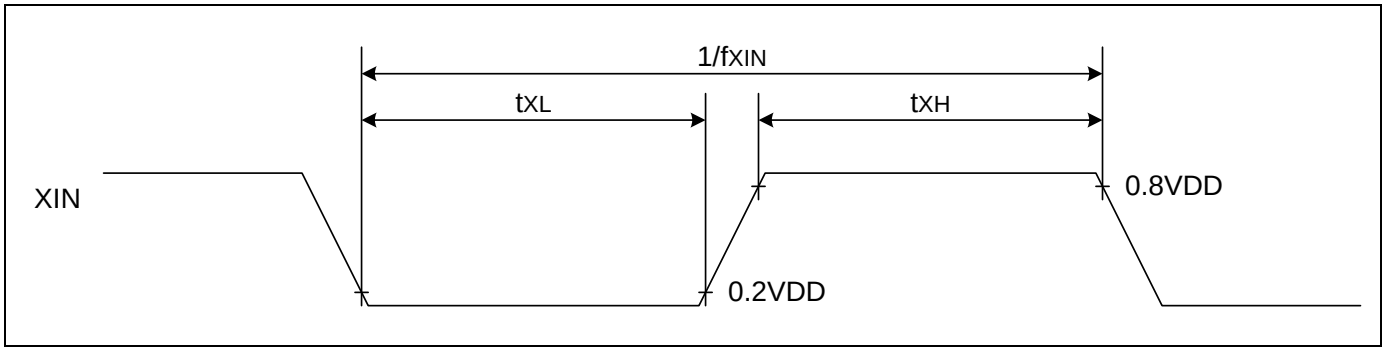


Figure 7.13 Clock Timing Measurement at XIN

7.19 Sub Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
External Clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	us

Table 7.19 Sub Oscillation Stabilization Characteristics

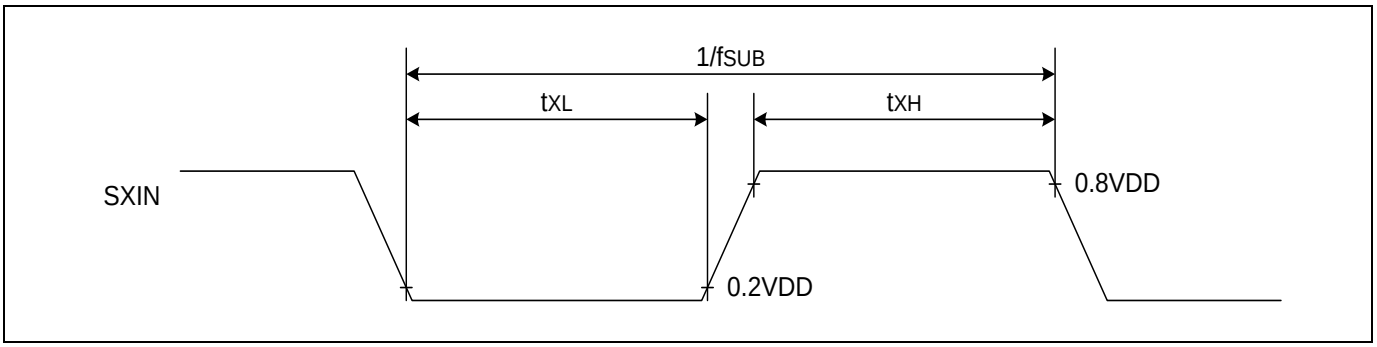


Figure 7.14 Clock Timing Measurement at SXIN

7.20 Operating Voltage Range

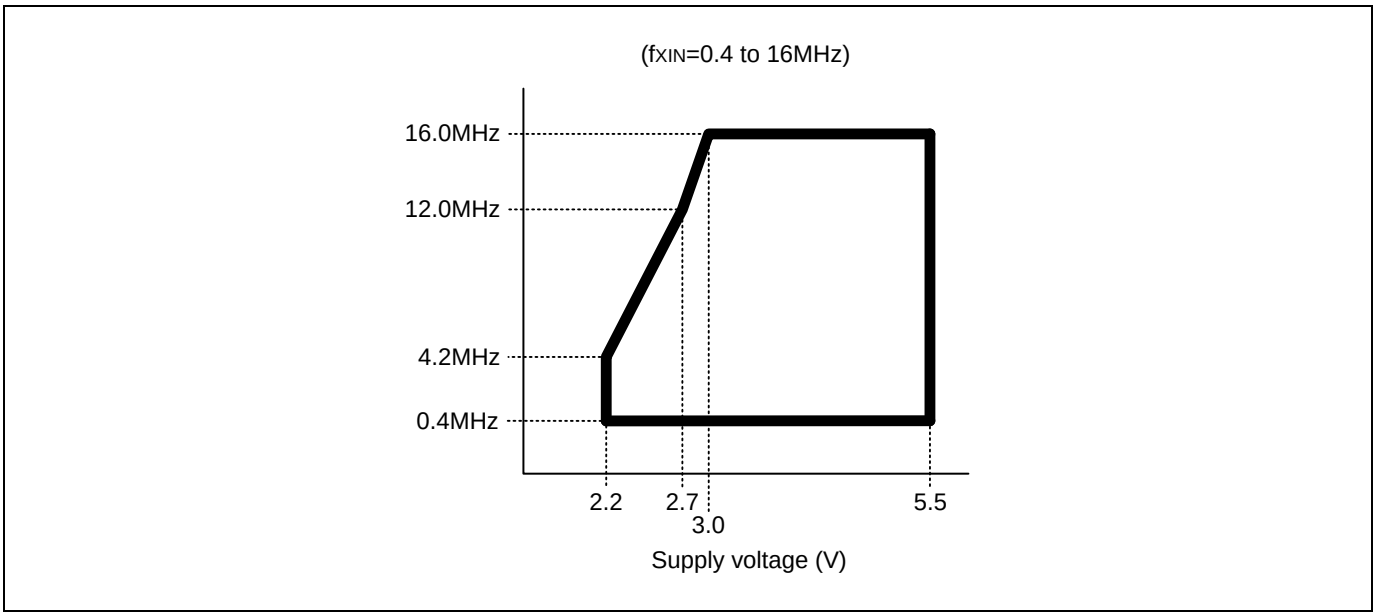


Figure 7.15 Operating Voltage Range (Main OSC)

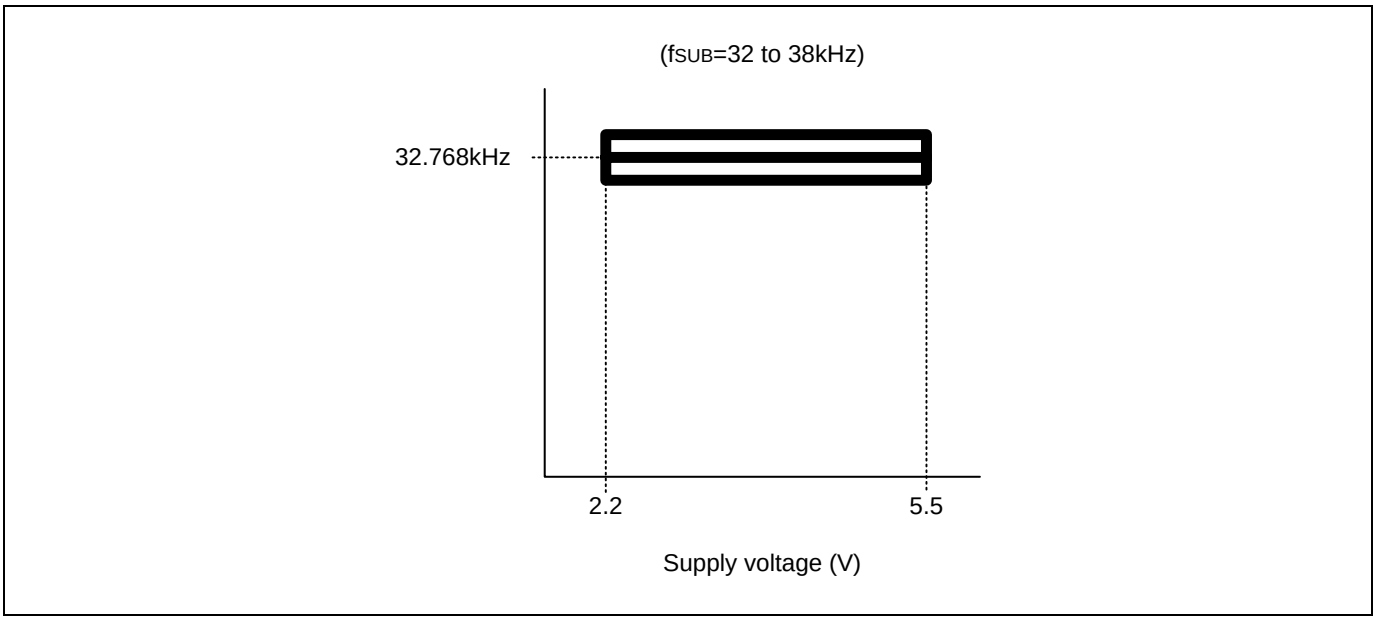


Figure 7.16 Operating Voltage Range (Sub OSC)

7.21 Recommended Circuit and Layout

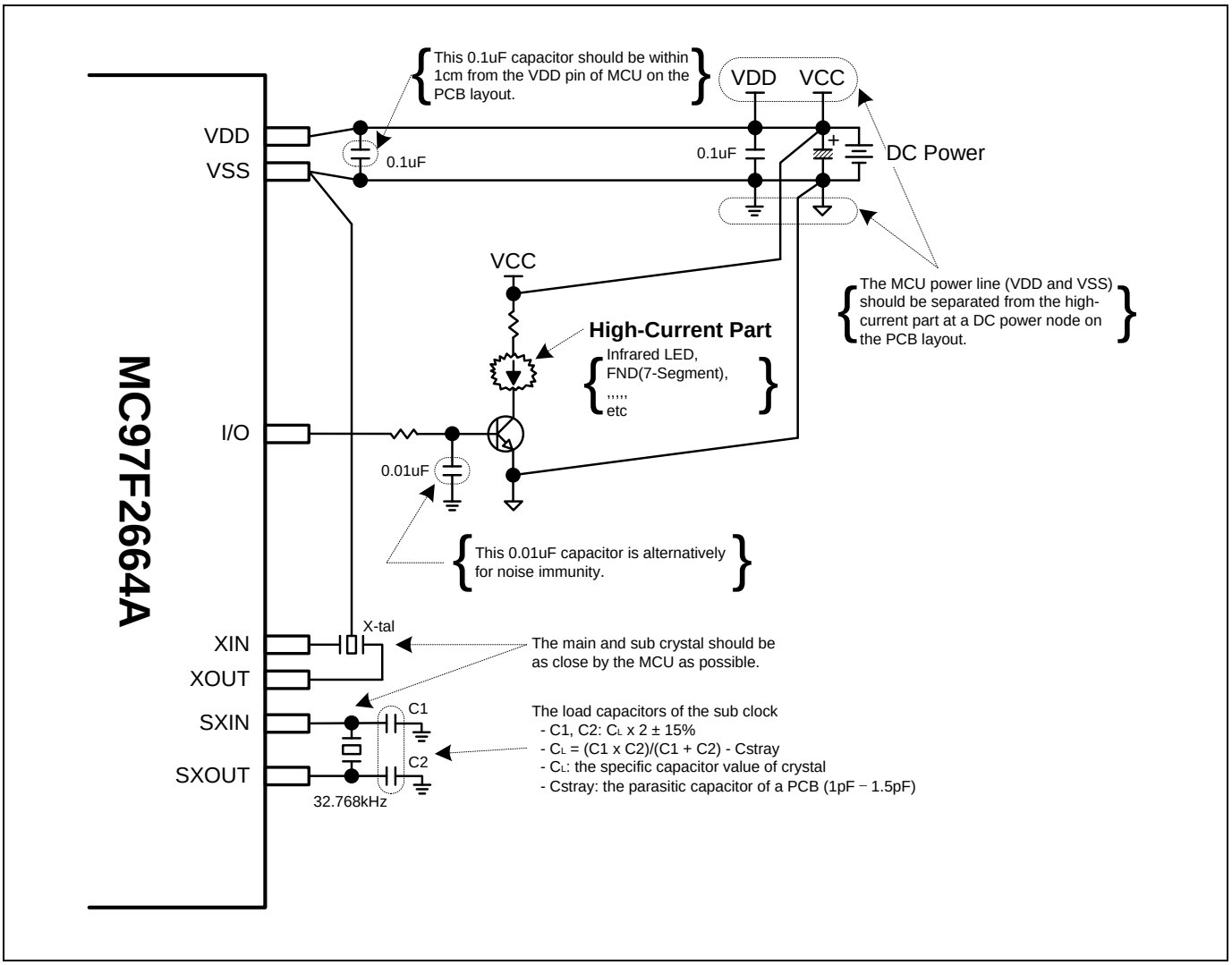
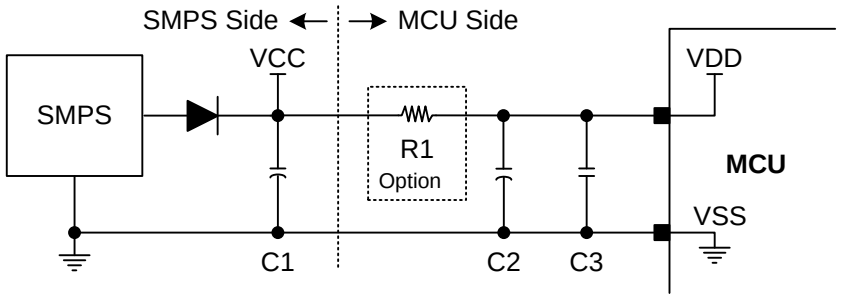


Figure 7.17 Recommended Circuit and Layout

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
   √ The R1 is optional so it may not apply.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.18 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

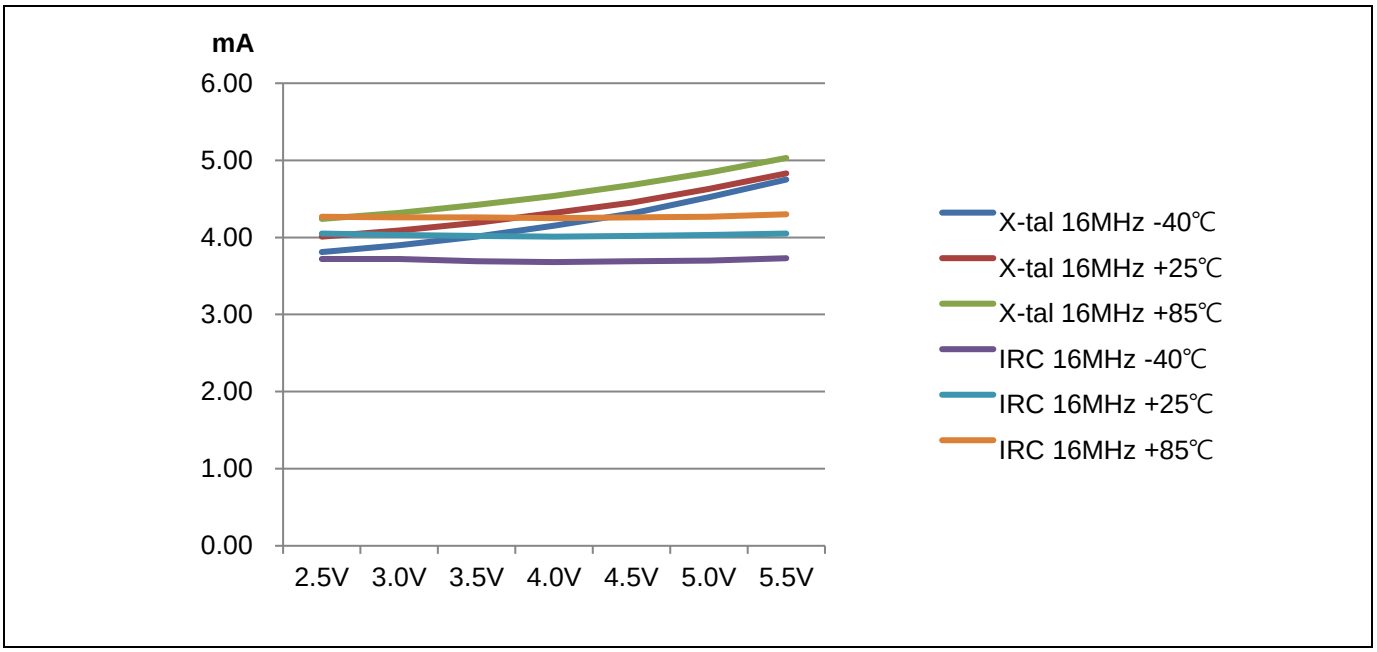


Figure 7.19 RUN (IDD1) Current

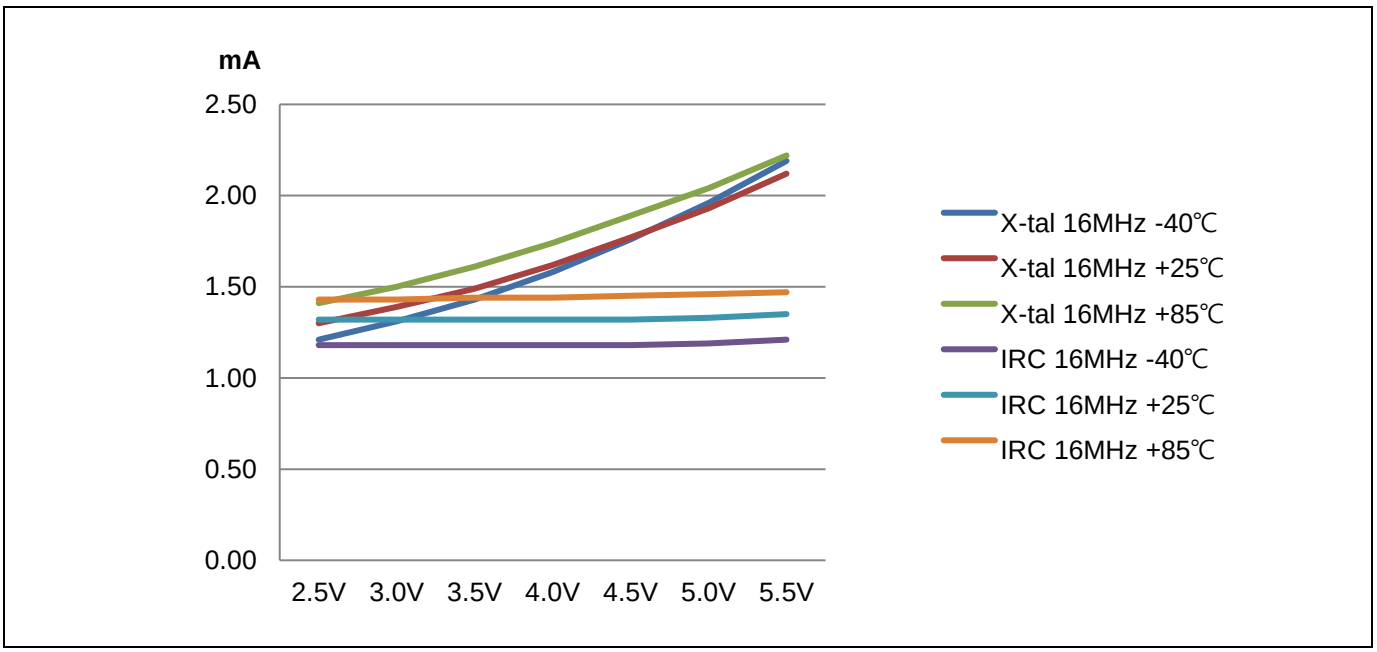


Figure 7.20 IDLE (IDD2) Current

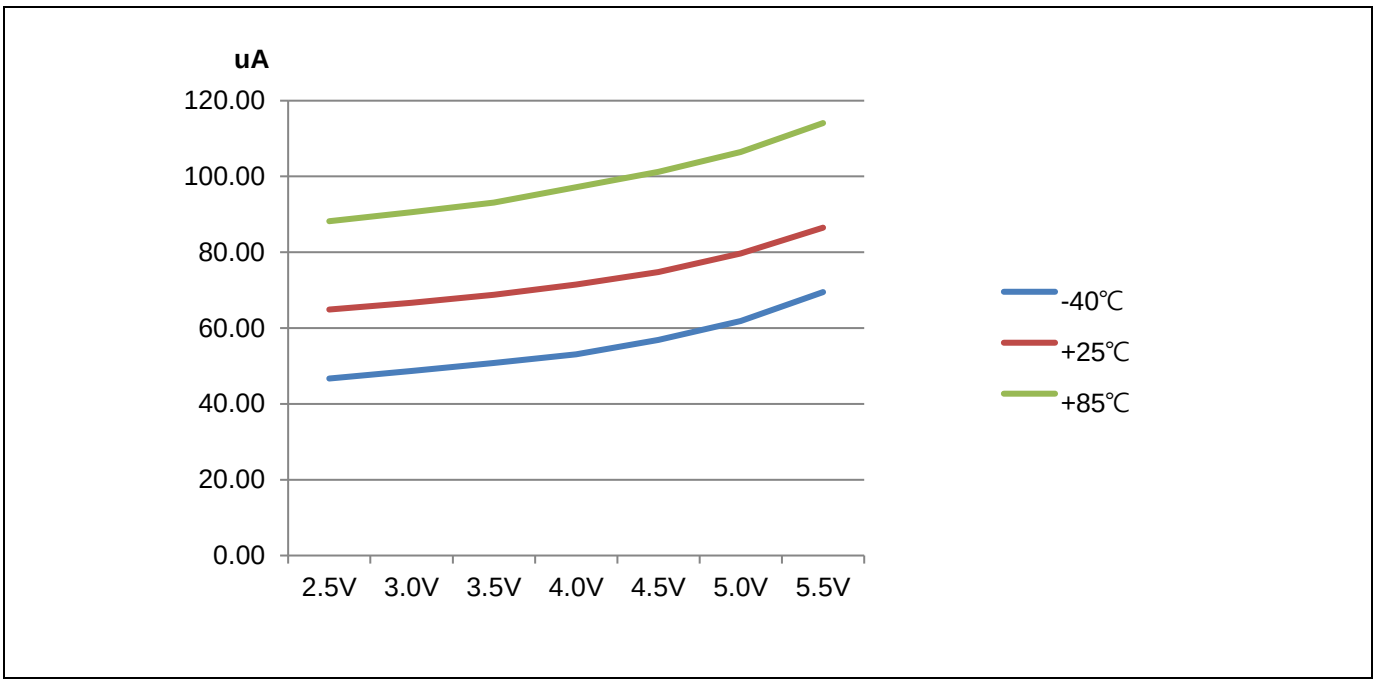


Figure 7.21 RUN (IDD3) Current

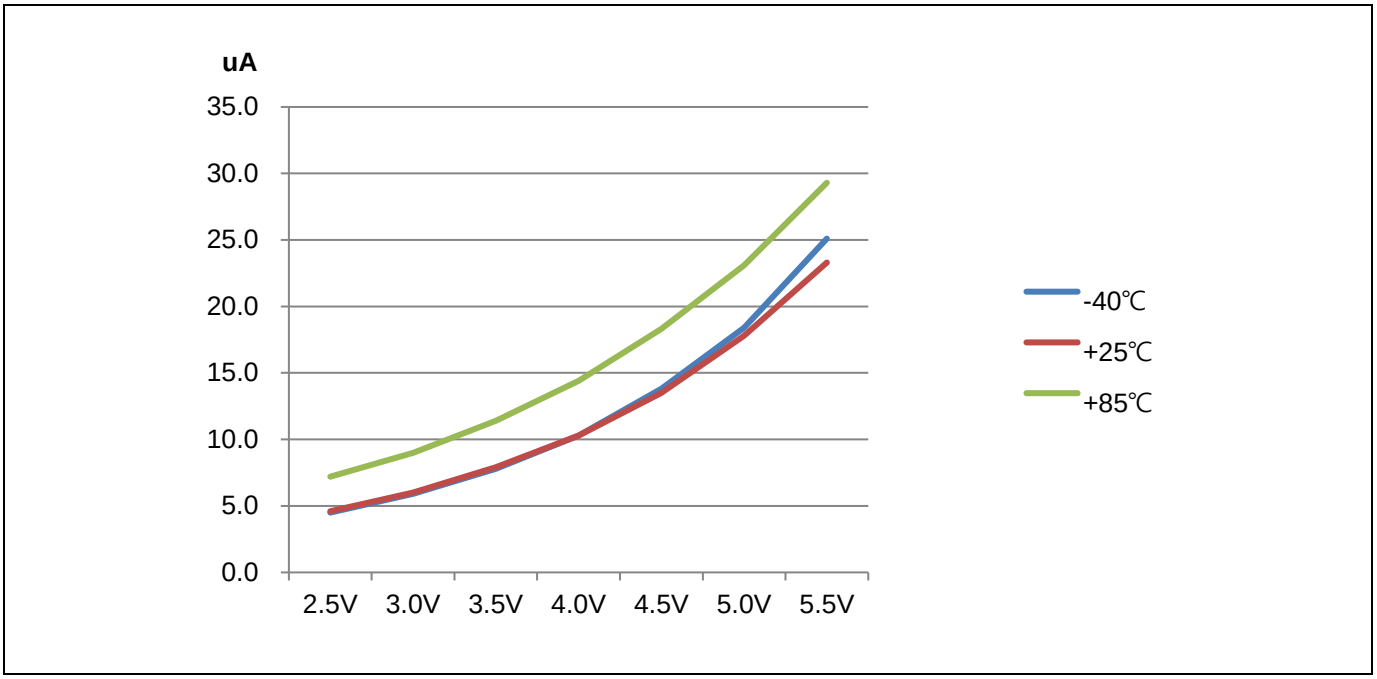


Figure 7.22 IDLE (IDD4) Current

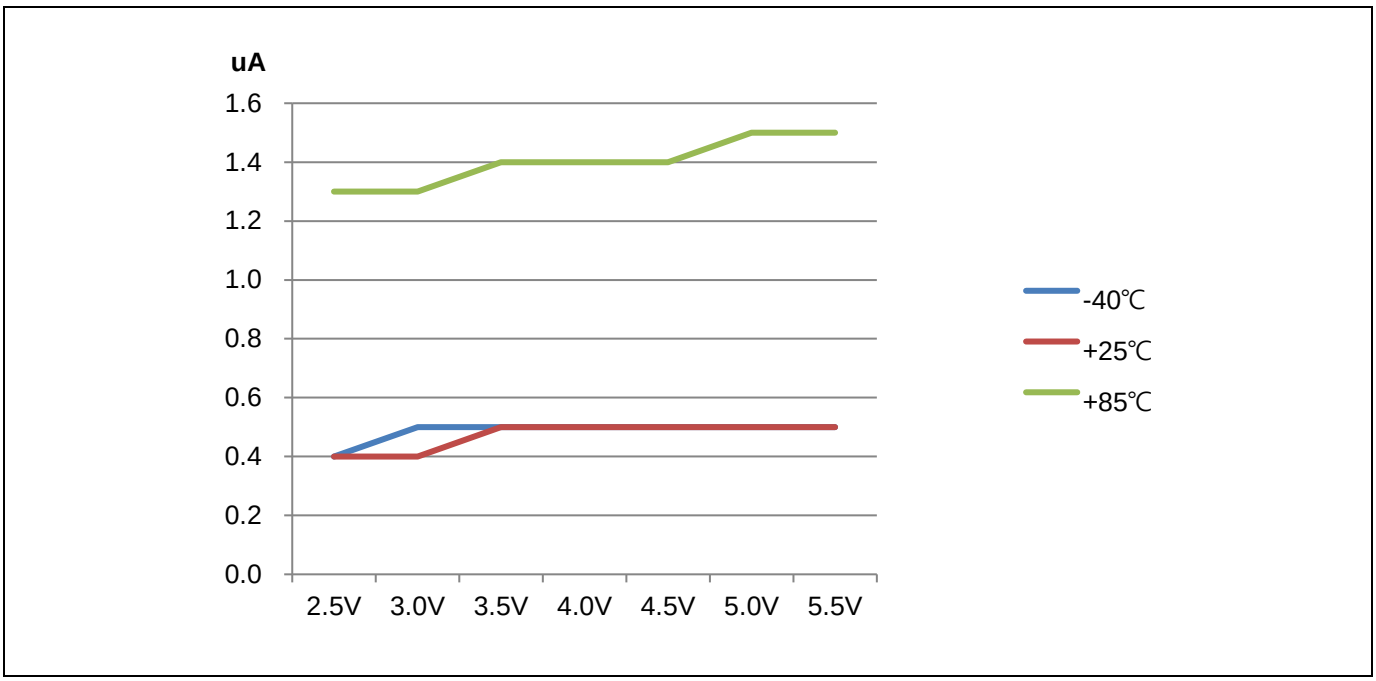


Figure 7.23 STOP (IDD5) Current

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