16 MHz 8-bit MC97FG316/MC97FG216 Microcontroller
16 Kbyte Flash memory, 512 bytes EEPROM, 12-bit ADC

Datasheet Version 1.13

Features

Core and memory
- 8-bit CISC M8051 core
- 16 Kbytes On-Chip FLASH
- 256 bytes IRAM/ 768 bytes XRAM
- 512 bytes Data EEPROM

General Purpose I/O (GPIO)
- 32 Pin : 30 Port, 28 Pin : 26 Port, 20 Pin : 18 Port

Timer/Counter
- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watchdog Timer (WDT) 8-bit × 1-ch
- 8-bit x 4-ch (16-bit x 2-ch, T0/T1/T2/T3)
- 16-bit x 1-ch (T4)

Pulse Width Modulation
- 3 High Frequency 10-bit PWM (Using Timer1)
- 10-bit PWM (Using Timer3)

Watch Timer (WT)
- 62.5ms/0.25s/0.5s/1s/1min interval at 32.768 kHz

Buzzer
- 8-bit × 1-ch

Analog Comparator
- On chip analog comparator 1-ch

Serial Communication
- USART x 2ch, SPI x 1ch, I2C x 1ch

12-bit A/D Converter
- 32 Pin : 15 Input channels

Power-down Mode
- STOP, IDLE mode

Power-on Reset
- Reset release level (1.4V)

Low Voltage Reset
- 4 levels detect (1.6/2.5/3.6/4.2V)

Internal RC Oscillator
- HSI 16MHz ±3.0%/±5.0% (TA=-40~+85°C/105°C)
- LSI 1MHz ±20%/±30% (TA= -40~+85°C/105°C)

Operating Voltage and Frequency
- 1.8V~ 5.5V (@32.768kHz Crystal)
- 1.8V~ 5.5V (@4 ~ 16MHz with Crystal)
- 1.8V~ 5.5V (@1 ~ 16MHz with Internal RC)
- 1.8V~ 5.5V (@125kHz with internal Ring OSC)

Minimum Instruction Execution Time
- 125ns (@16MHz main clock)
- 61us (@ 32.768kHz sub clock)

Operating temperature
- –40 ~ +85℃ / –40 ~ +105℃

Package Type, Pb-free package
- 32 LQFP/QFN, 28 TSSOP, 20 TSSOP

Product selection table

Table 1. Device Summary

Part Number	Flash	XRAM/ IRAM	EEPROM	Timer (PWM)	USART	SPI	I2C	ADC 12-bit (channel)	GPIO	Package	Temp.
MC97FG316L	16KB	768/ 256bytes	512 bytes	5(3+1)	2	1	1	15	30	32LQFP	-40°C to +85°C
MC97FG316U				5(3+1)	2	1	1	15	30	32QFN	
MC97FG316R				5(3+1)	2	1	1	12	26	28TSSOP	
MC97FG216R				5(3+1)	0	1	1	10	18	20TSSOP	
MC97FG316LB2*	16KB	768/ 256bytes	512 bytes	5(3+1)	2	1	1	15	30	32LQFP	-40°C to +105°C
MC97FG316UB2*				5(3+1)	2	1	1	15	30	32QFN	
MC97FG316RB2*				5(3+1)	2	1	1	12	26	28TSSOP	
MC97FG216RB2*				5(3+1)	0	1	1	10	18	20TSSOP	

* For available options or further information on the device with an "*" mark, please contact the ABOV sales office.

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1 Description

MC97FG316/MC97FG216 is an advanced CMOS 8-bit microcontroller with 16Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost-effective solution to many embedded control applications.

1.1 Device overview

In this section, features of MC97FG316/MC97FG216 and peripheral counts are introduced.

Table 2. MC97FG316/MC97FG216 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	8-bit CISC core (M8051, 2 clocks per cycle)
	Interrupt	Up to 24 peripheral interrupts supported. • External Interrupts (7) • Pin Change Interrupt(P0) (1) • USART0,1 (4) • SPI (1) • Timer (5) • I2C (1) • ADC (1) • Analog Comparator (1) • WDT (1) • WT (1) • BIT (1)
Memory	ROM (FLASH) capacity	• 16 Kbytes FLASH with self-read and write capability • Optional boot code section with protection • In-system programming (ISP) • Endurance: 10,000 times at room temperature • Retention: 10 years
	IRAM	256Bytes
	XRAM	768Bytes
	EEPROM	• 512Bytes • Endurance: 300,000 times at room temperature • Retention: 10 years
PWM(Pulse Width Modulation)		• 3 High Frequency 10-bit PWM (Using Timer1) • 10-bit PWM (Using Timer3)
Buzzer		8-bit × 1-ch
Minimum instruction execution time		125ns (@ 16MHz main clock)

Table 2. MC97FG316/MC97FG216 Device Features and Peripheral Counts (continued)

Peripherals		Description
Analog comparator		On chip analog comparator 1-ch
Power down mode		• STOP1, STOP2 mode • IDLE mode
General Purpose I/O (GPIO)		• 30Ports (P0[7:0], P1[6:0], P2[6:0], P3[7:0]): 32-Pin • 26Ports (P0[7:0], P1[6:0], P2[2:0], P3[7:0]): 28-Pin • 18Ports (P0[7:0], P1[6:0], P2[2:0]): 20-Pin
Reset	Power on reset	Reset release level: 1.4V
	Low voltage reset	• 4 levels detect • 1.6/2.5/3.6/4.2V
Watch Timer (WT)		62.5ms/0.25s/0.5s/1s/1min interval at 32.768 kHz
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Watchdog timer (WDT) 8-bit x 1-ch. • 8-bit x 4-ch (16-bit x 2-ch, T0/T1/T2/T3), 16-bit x 1-ch (T4)
Communication function	USART	8-bit USART x 2-ch or 8-bit SPI x 2-ch
	SPI	8-bit SPI x 1-ch
	I2C	8-bit I2C x 1-ch
12-bit A/D Converter		15 input channels: 32-pin
Oscillator type		• 4MHz to 16MHz crystal or ceramic for main clock • 32.768kHz Crystal for sub clock
Internal RC oscillator		• HSI 16MHz ±3.0%/±5.0% (T_A=-40~ +85°C/105°C) • LSI 1MHz ±20%/±30% (T_A= -40~ +85°C/105°C)
Operating voltage and frequency		• 1.8V to 5.5V @ 32.768kHz with crystal • 1.8V to 5.5V @ 4MHz to 16MHz with crystal • 1.8V to 5.5V @ 1MHz to 16MHz with internal RC • 1.8V to 5.5V @ 128kHz with internal Ring OSC
Operating temperature		-40℃ to +85℃, -40℃ to +105℃
Package		• Pb-free packages • 32 LQFP/QFN • 28 TSSOP • 20 TSSOP

1.2 MC97FG316/MC97FG216 block diagram

In this section, MC97FG316/MC97FG216 device with peripherals are described in a block diagram.

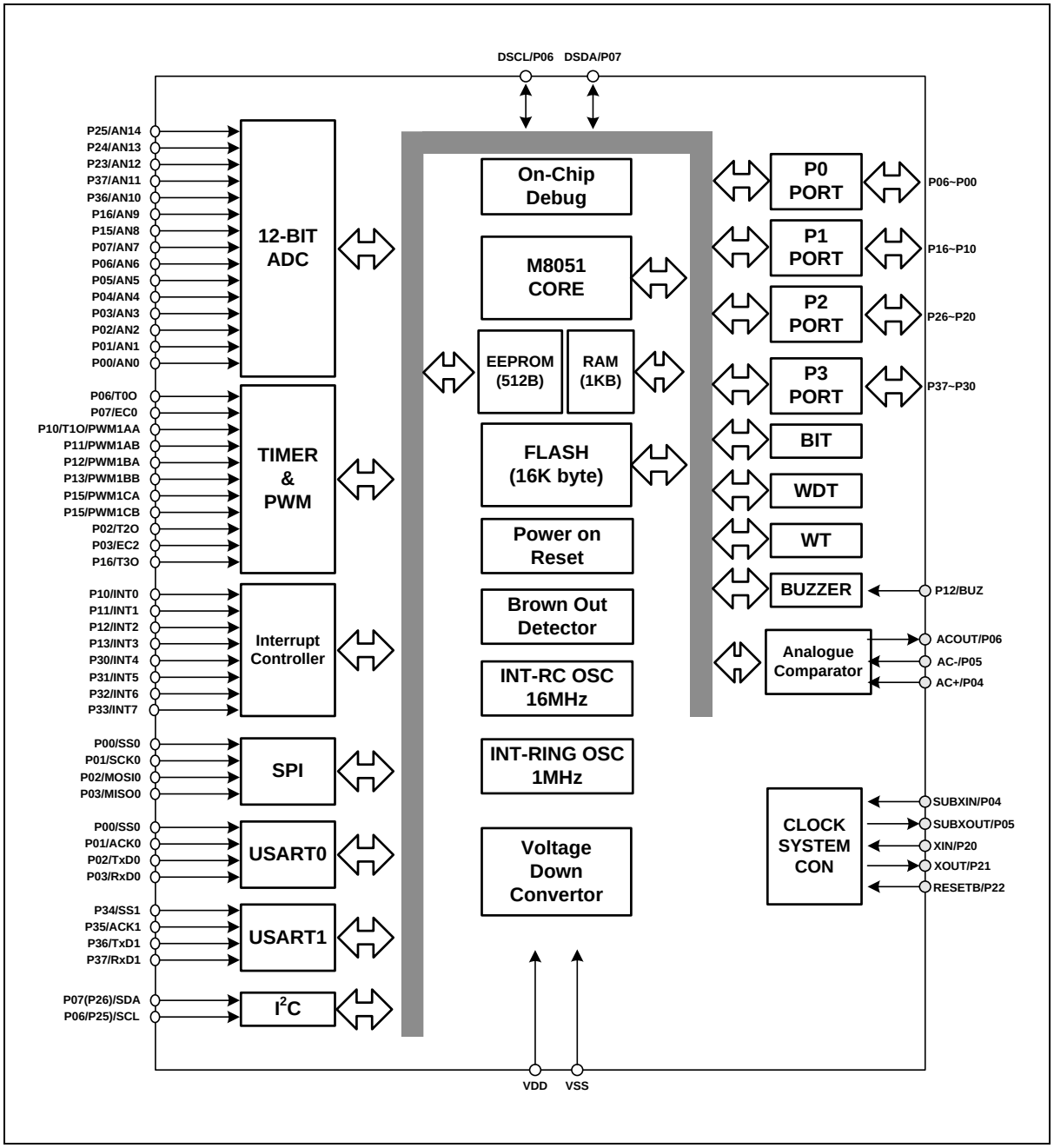
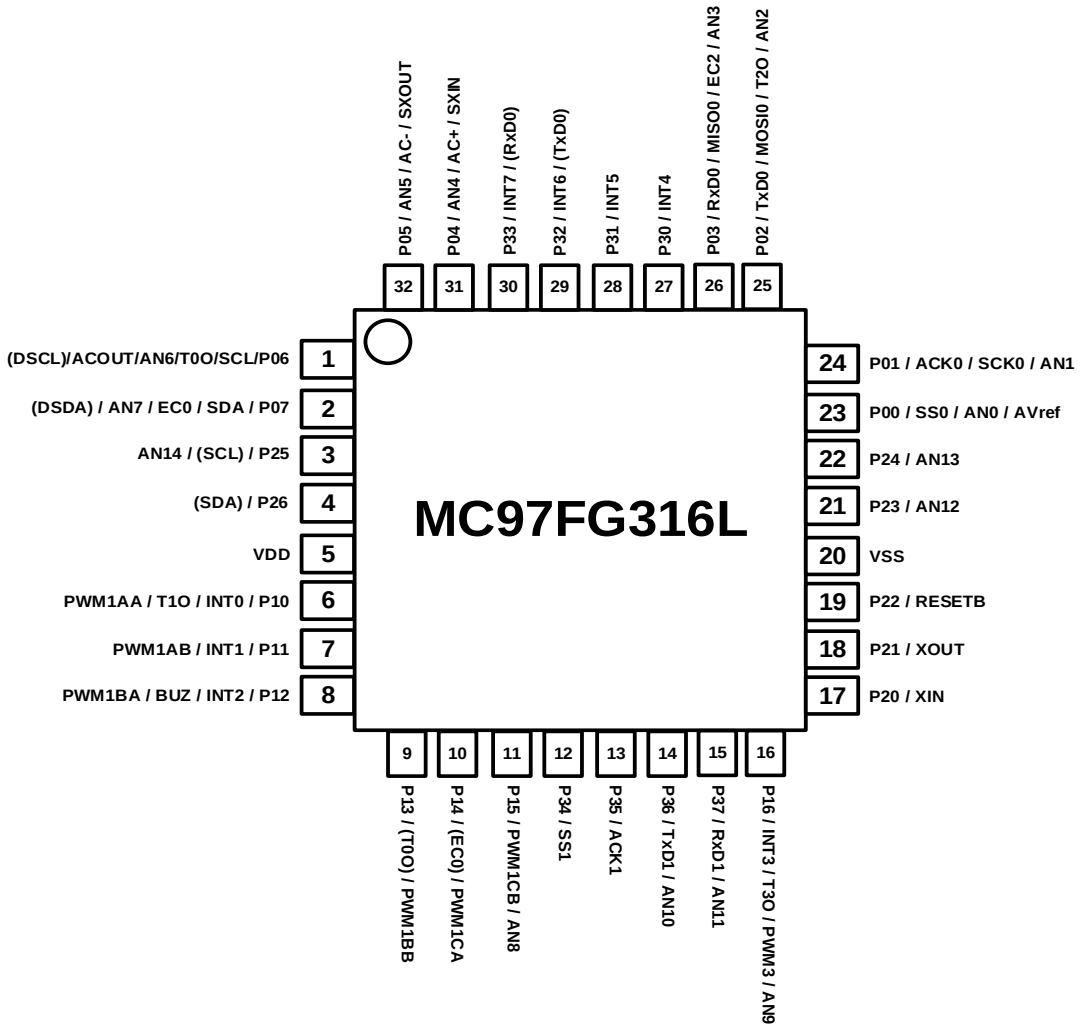


Figure 1. MC97FG316/MC97FG216 Block Diagram

2 Pinouts and pin description

In this chapter, MC97FG316/MC97FG216 device pinouts and pin descriptions are introduced.

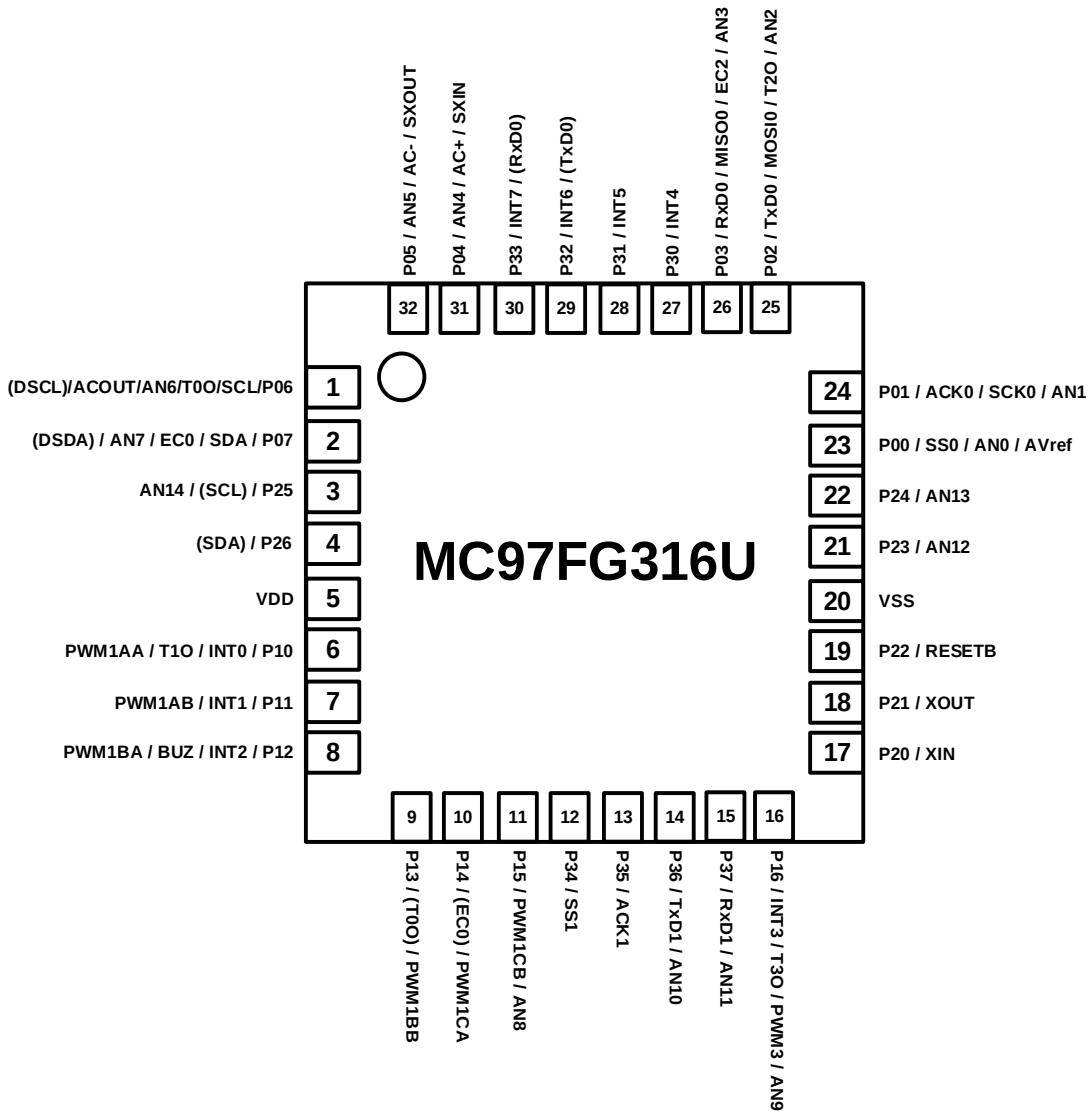
2.1 Pinouts



NOTES:

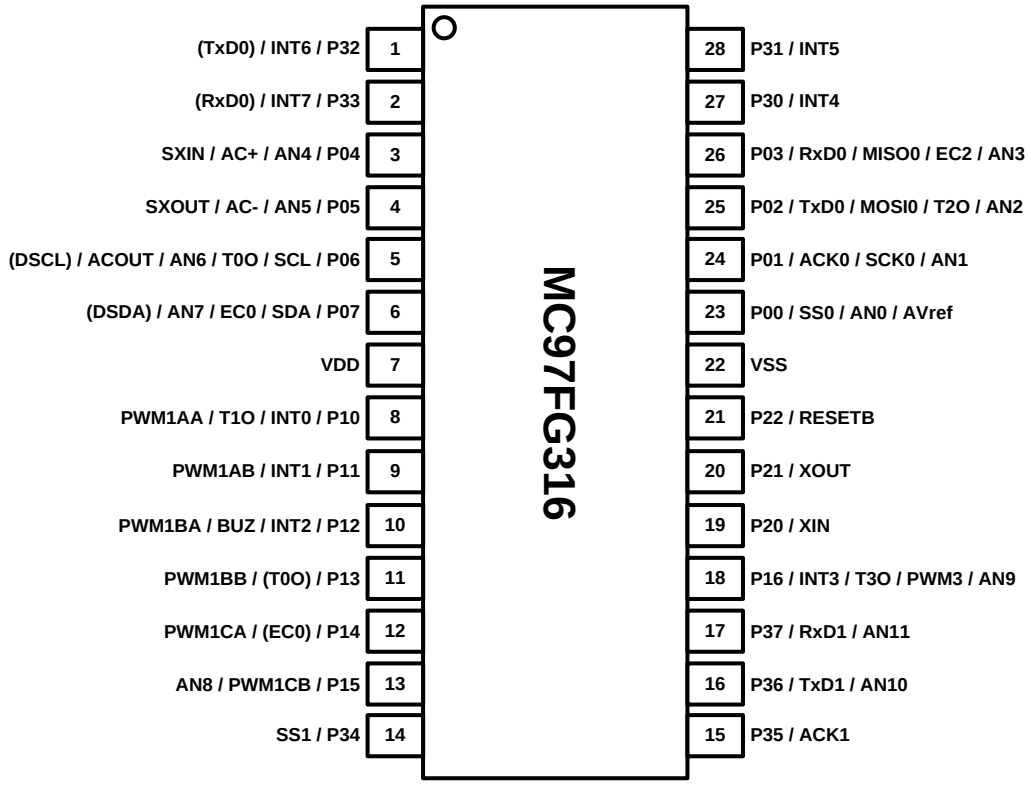
1. At 28TSSOP PKG, P2[6:3] in 32-pin package are removed and their function can't operate.
2. At 20TSSOP PKG, P2[6:3] and P3[7:0] in 32-pin package are removed and their function can't operate.
3. When On-Chip Debugging, ISP uses P0[7:6] pin as DSDA, DSCL.
4. The outside pin operation has higher priority than the inside pin operation. Ex) In pin26, if P03, RxD0, MISO0, EC2 and AN3 are set, AN3 will be operated.

Figure 2. MC97FG316 32LQFP Pin Assignment



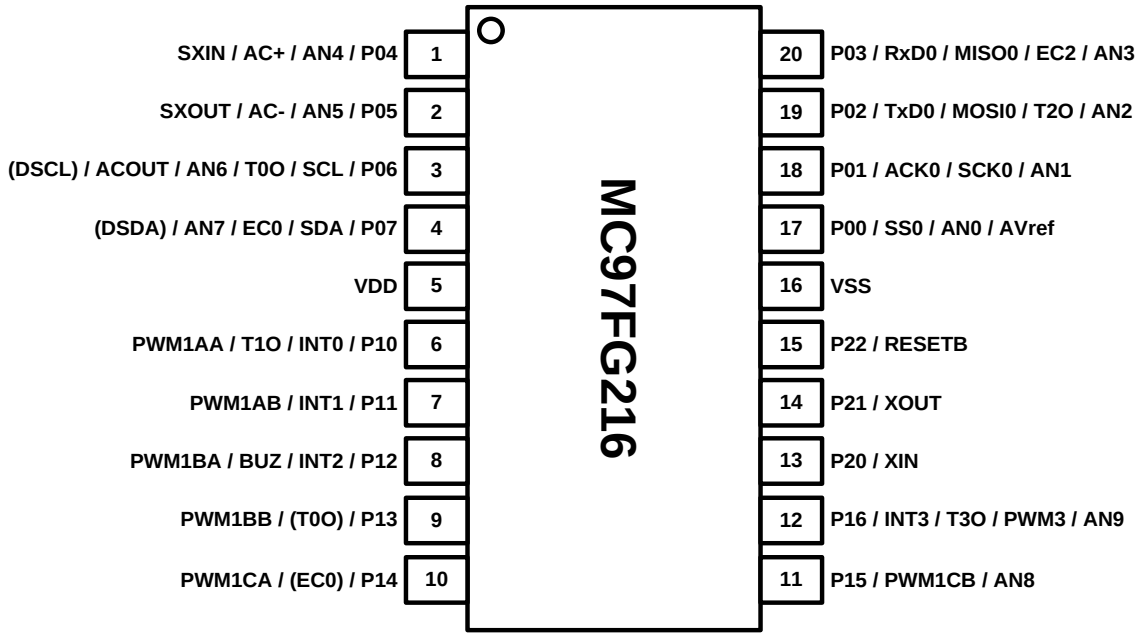
NOTE: The programmer (E-PGM+, E-Gang4/6) uses P0[7:6] pin as DSDA, DSCL.

Figure 3. MC97FG316 32QFN Pin Assignment



NOTE: The programmer (E-PGM+, E-Gang4/6) uses P0[7:6] pin as DSDA, DSCL.

Figure 4. MC97FG316 28TSSOP Pin Assignment



NOTE: The programmer (E-PGM+, E-Gang4/6) uses P0[7:6] pin as DSDA, DSCL.

Figure 5. MC97FG216 20TSSOP Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

Pin no.				Pin Name	I/O(1)	Description	Remark
32 LQFP	32 QFN	28 TSSOP	20 TSSOP				
23	23	23	17	P00*	IOUS	Port 0 bit 0 Input/output	
				SS0	IO	USART0 slave select signal	
				AN0	IA	ADC input ch-0	
				AVref	P	A/D converter reference voltage	
24	24	24	18	P01*	IOUS	Port 0 bit 1 Input/output	
				ACK0	IO	USART0 external clock(XCK for USART)	
				SCK0	IO	USART0 external clock(XCK for SPI)	
				AN1	IA	ADC input ch-1	
25	25	25	19	P02*	IOUS	Port 0 bit 2 Input/output	
				TxD0	O	USART0(USART) transmit data	
				MOSI0	IO	USART0(SPI) MOSI(master output slave input)	
				T2O	O	Timer 2 interval output	
				AN2	IA	ADC input ch-1	
26	26	26	20	P03*	IOUS	Port 0 bit 3 Input/output	
				RxD0	I	USART0(USART) receive data	
				MISO0	IO	USART0(SPI) MISO(master input slave output)	
				EC2	I	Timer 2 event counter input	
				AN3	IA	ADC input ch-3	
31	31	3	1	P04*	IOUS	Port 0 bit 4 Input/output	
				AN4	IA	ADC input ch-4	
				AC+	I	Analog comparator positive input	
				SXIN	I	Sub oscillator input	
32	32	4	2	P05*	IOUS	Port 0 bit 5 Input/output	
				AN5	IA	ADC input ch-5	
				AC-	I	Analog comparator negative input	
				SXOUT	O	Sub oscillator output	
1	1	5	3	P06*	IOUS	Port 0 bit 6 Input/output	
				SCL	IO	I2C clock signal	
				T0O	O	Timer 0 interval output	
				AN6	IA	ADC input ch-6	
				ACOUT	O	Analog comparator output	
				DSCL	IOU	OCD debugger clock	Pull-up

Table 3. Normal Pin Description (continued)

Pin no.				PIN Name	I/O[1]	Description	Remark
32 LQFP	32 QFN	28 TSSOP	20 TSSOP				
IOUS	2	6	4	P07*		Port 0 bit 7 Input/output	
				SDA	IO	I2C data signal	
				EC0	I	Timer 0 event counter input	
				AN7	IA	ADC input ch-7	
				DSDA	IOU	OCD debugger data input/output	Pull-up
6	6	8	6	P10*	IOUS	Port 1 bit 0 Input/output	
				INT0	I	External interrupt input ch-0	
				T1O	O	Timer 1 interval output	
				PWM1AA	O	Timer1 PWM A output	
7	7	9	7	P11*	IOUS	Port 1 bit 1 Input/output	
				INT1	I	External interrupt input ch-1	
				PWM1AB	O	Timer1 PWM A output	
8	8	10	8	P12*	IOUS	Port 1 bit 2 Input/output	
				INT2	I	External interrupt input ch-2	
				BUZ	O	Buzzer output	
				PWM1BA	O	Timer1 PWM B output	
9	9	11	9	P13*	IOUS	Port 1 bit 3 Input/output	
				(T0O)	O	Timer 0 interval output(by PSR2)	
				PWM1BB	O	Timer1 PWM B output	
10	10	12	10	P14*	IOUS	Port 1 bit 4 Input/output	
				(EC0)	O	Timer 0 event counter input(by PSR2)	
				PWM1CA	O	Timer1 PWM C output	
11	11	13	11	P15*	IOUS	Port 1 bit 5 Input/output	
				PWM1CB	O	Timer1 PWM C output	
				AN8	IA	ADC input ch-8	
16	16	18	12	P16*	IOUS	Port 1 bit 6 Input/output	
				INT3	I	External interrupt input ch-3	
				T3O	O	Timer 3 interval output	
				PWM3	O	Timer 3 PWM output	
				AN9	IA	ADC input ch-9	
17	17	19	13	P20*	IOUS	Port 2 bit 0 Input/output	
				XIN	I	Main oscillator input	
18	18	20	14	P21*	IOUS	Port 2 bit 1 Input/output	
				XOUT	O	Main oscillator output	
19	19	21	15	P22*	IOUS	Port 2 bit 2 Input/output	
				RESETB	IU	RESETB input	Pull-up
21	21	-	-	P23*	IOUS	Port 2 bit 3 Input/output	
				AN12	IA	ADC input ch-12	
22	22	-	-	P24*	IOUS	Port 2 bit 4 Input/output	
				AN13	IA	ADC input ch-13	
3	3	-	-	P25*	IOUS	Port 2 bit 7 Input/output	
				(SCL)	IO	I2C clock signal(by PSR1)	
				AN14	IA	ADC input ch-14	
4	4	-	-	P26*	IOUS	Port 2 bit 6 Input/output	
				(SDA)	IO	I2C data signal(by PSR1)	
27	27	27	-	P30*	IOUS	Port 3 bit 0 Input/output	
				INT4	I	External interrupt input ch-4	
28	28	28	-	P31*	IOUS	Port 3 bit 1 Input/output	
				INT5	I	External interrupt input ch-5	
29	29	1	-	P32*	IOUS	Port 3 bit 2 Input/output	

Table 3. Normal Pin Description (continued)

Pin no.				PIN Name	I/O(1)	Description	Remark
32 LQFP	32 QFN	28 TSSOP	20 TSSOP				
				INT6	I	External interrupt input ch-6	
				(TxD0)	O	USART0(USART) transmit data(by PSR2)	
30	30	2	-	P33*	IOUS	Port 3 bit 3 Input/output	
				INT7	I	External interrupt input ch-7	
				(RxD0)	I	USART0(USART) receive data(by PSR2)	
12	12	14	-	P34*	IOUS	Port 3 bit 4 Input/output	
				SS1	IO	USART1 slave select signal	
13	13	15	-	P35*	IOUS	Port 3 bit 5 Input/output	
				ACK1	IO	USART1 external clock(XCK for USART)	
14	14	16	-	P36*	IOUS	Port 3 bit 6 Input/output	
				TxD1	O	USART1(USART) transmit data	
				AN10	IA	ADC input ch-10	
15	15	17	-	P37*	IOUS	Port 3 bit 7 Input/output	
				RxD1	I	USART1(USART) receive data	
				AN11	IA	ADC input ch-11	
5	5	7	5	VDD	P	VDD	
20	20	22	16	VSS	P	VSS	

NOTES:

1. At 28TSSOP PKG, P2[6:3] in 32-pin package is removed and their functions are not allowed.
2. At 20TSSOP PKG, P2[6:3] and P3[7:0] in 32-pin package are removed and their functions are not allowed.
3. The P22/RESETB pin is configured as one of the P22 and RESETB pin by the “CONFIGURE OPTION”.
4. The P21/XOUT, P20/XIN, P04/AN4/AC+/SXIN and P05/AN5/AC-/SXOUT pins are configured as OSC pins by the “CONFIGURE OPTION”.
5. If the (DSCL)/ACOUNT/AN6/T0O/SCL/P06 and (DSDA)/AN7/EC0/SDA/P07 pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.

6. When On-Chip Debugging, ISP uses P0[7:6] pin as DSDA, DSCL.
7. The (DSCL)/ACOUNT/AN6/T0O/SCL/P06 and (DSDA)/AN7/EC0/SDA/P07 pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
8. The outside pin operation has higher priority than the inside pin operation.
   Ex) In pin26, if P03, RxD0, MISO0, EC2 and AN3 are set, AN3 will be operated.
9. (1) I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power.
10. The * means ‘Selected pin function after reset condition.

3 Port structures

In this chapter, two port structures are introduced in Figure 6 and Figure 7 regarding general purpose I/O port and external interrupt I/O port respectively.

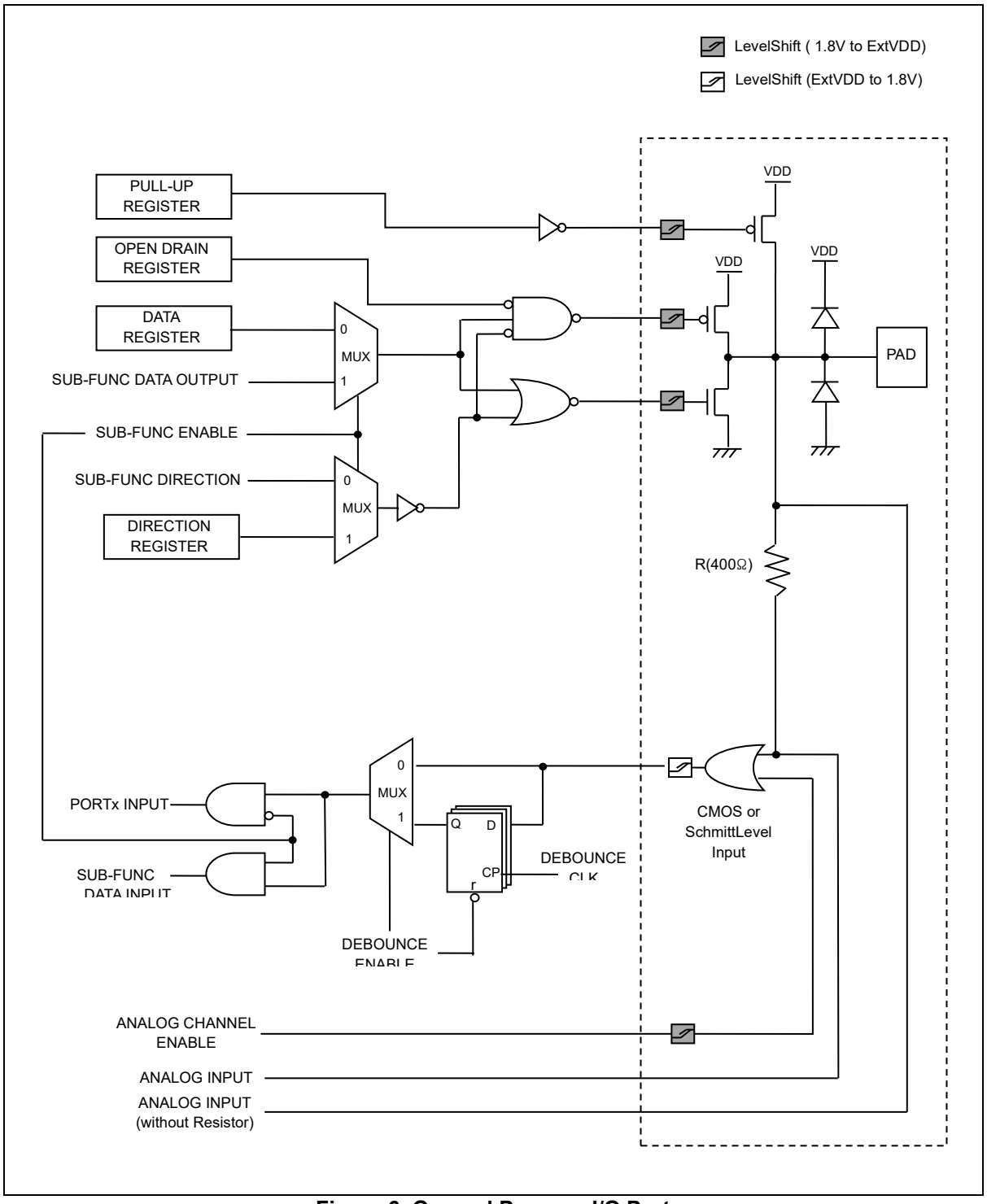


Figure 6. General Purpose I/O Port

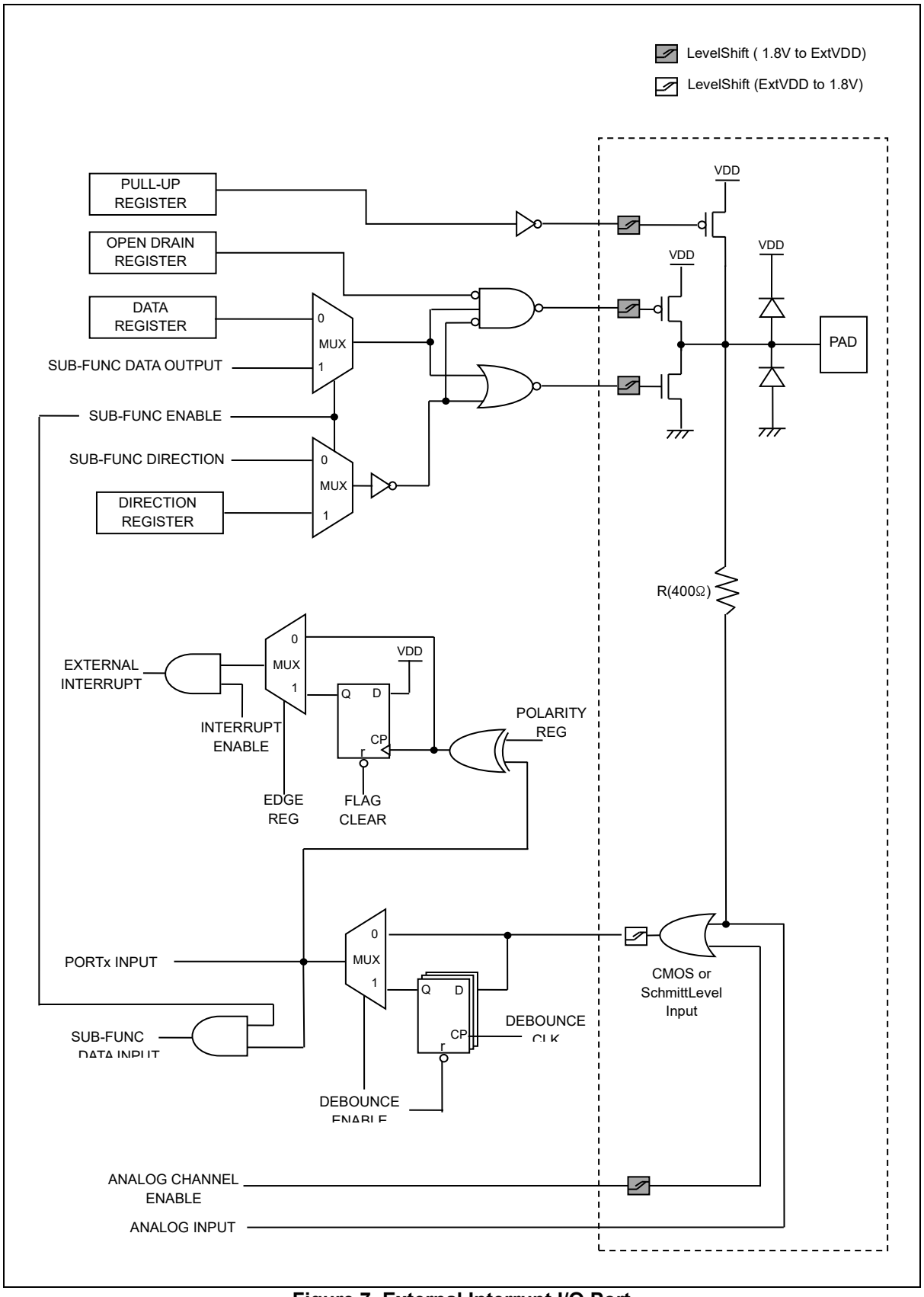


Figure 7. External Interrupt I/O Port

4 Memory organization

MC97FG316/MC97FG216 addresses two separate address memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the Data Memory more rapidly. 16-bit Data Memory address is generated through the DPTR register.

MC97FG316/MC97FG216 provides on-chip 16Kbytes of the ISP type flash program memory, which readable and writable. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 768bytes and internal EEPROM is 512bytes.

4.1 Program memory

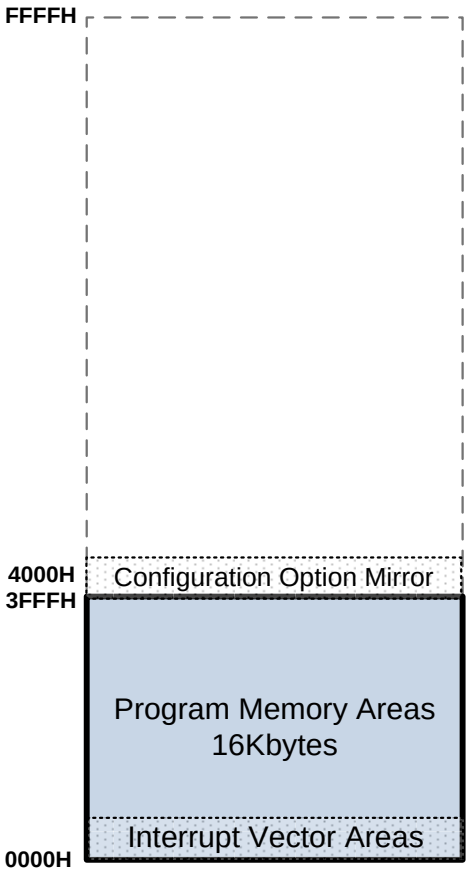
A 16-bit program counter is capable of addressing up to 64Kbytes, and MC97FG316/MC97FG216 has just 16Kbytes program memory space.

Figure 8 shows a map of the lower part of the program memory.

After reset, CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in the program memory. An interrupt causes the CPU to jump to the corresponding location, where it commences execution of the service routine.

An external interrupt 11, for example, is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within an interval of 8-bytes.

Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.



NOTES:

1. The 16Kbytes includes the Interrupt Vector Region.
2. The value of Configuration Option can be read at address 0x4000.
3. Non-volatile and reprogramming memory: Flash memory based on EEPROM cell

Figure 8. Program Memory Map

4.2 Data memory

Internal data memory space is divided into three blocks, which are generally referred to as lower 128bytes, upper 128bytes, and SFR space. Internal data memory addresses are always one byte wide, which implies an address space of 256bytes. In fact, the addressing modes for the internal data memory can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space, while indirect addresses higher than 7FH access a different memory space. Thus as shown in Figure 9, the upper 128bytes and SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 10. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes of RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

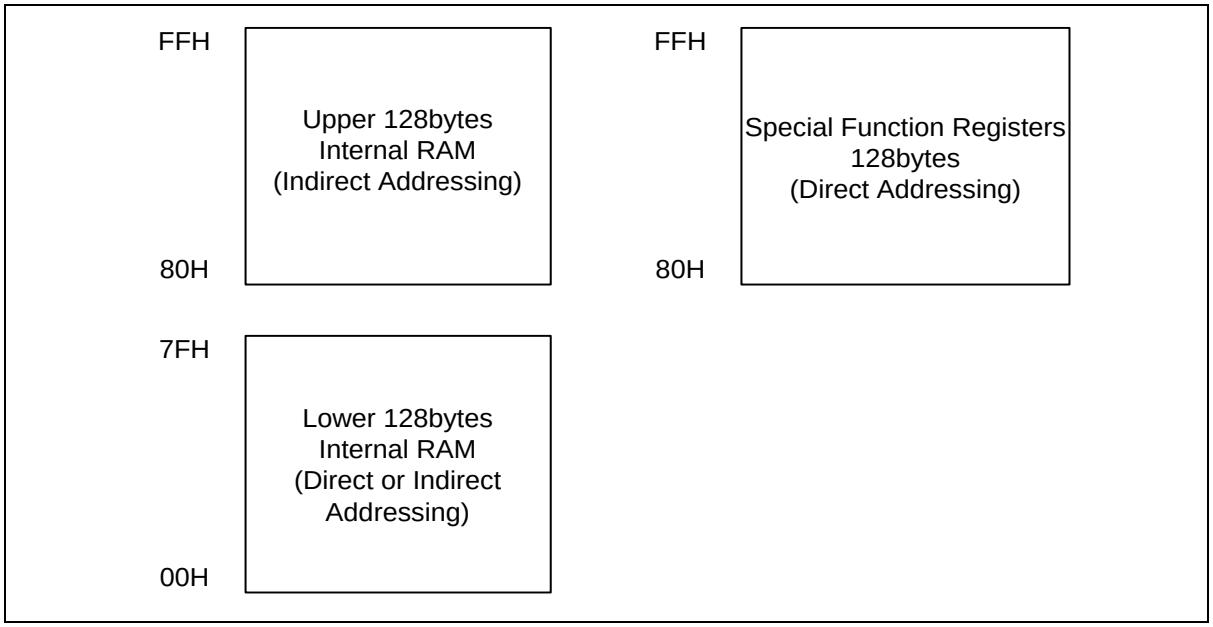


Figure 9. Data Memory Map

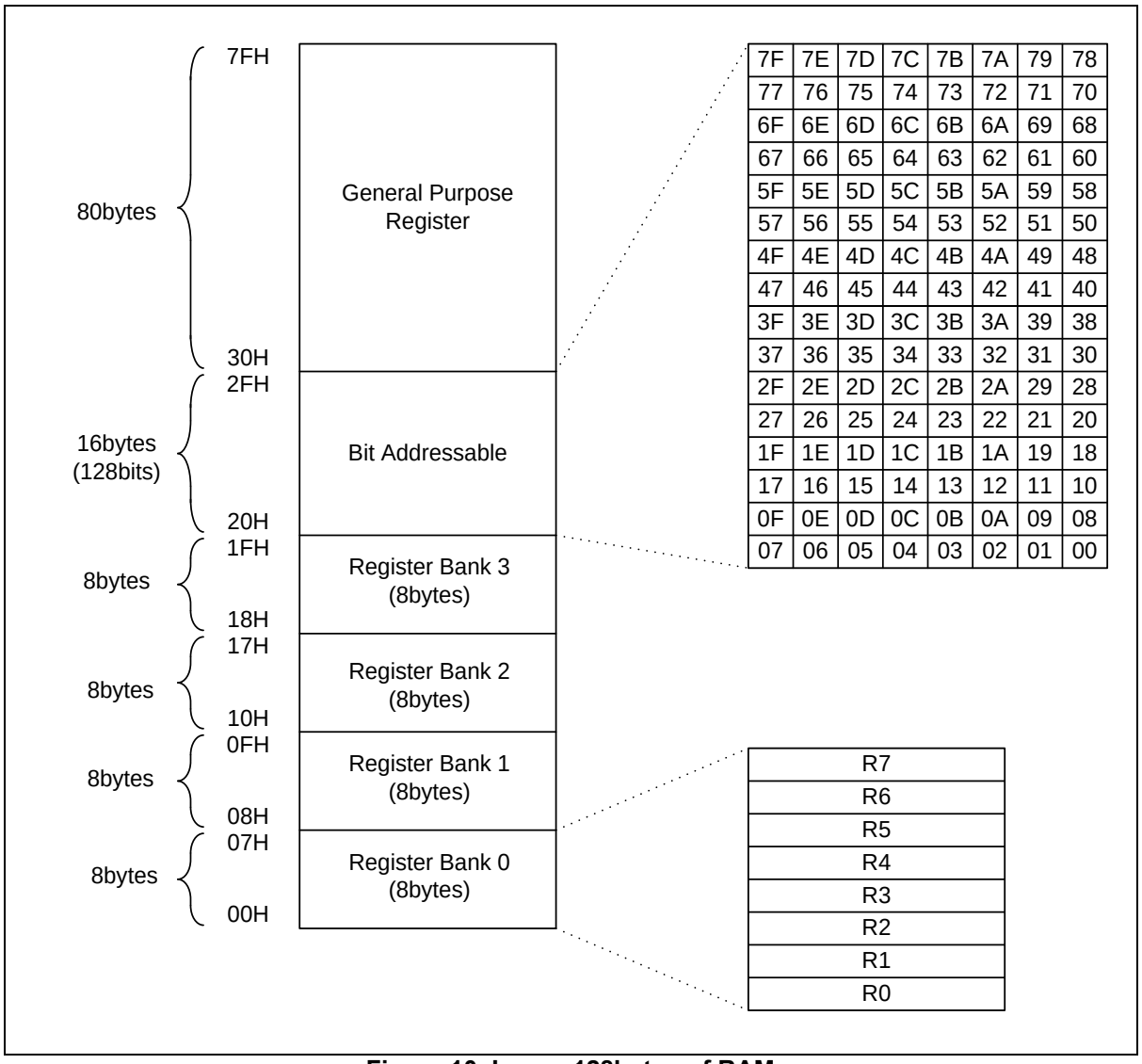


Figure 10. Lower 128bytes of RAM

4.3 EEPROM data memory and external data memory

MC97FG316/MC97FG216 has 512bytes of EEPROM, 768bytes of XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

For more information about EEPROM Data memory, see chapter 18 Memory programming.

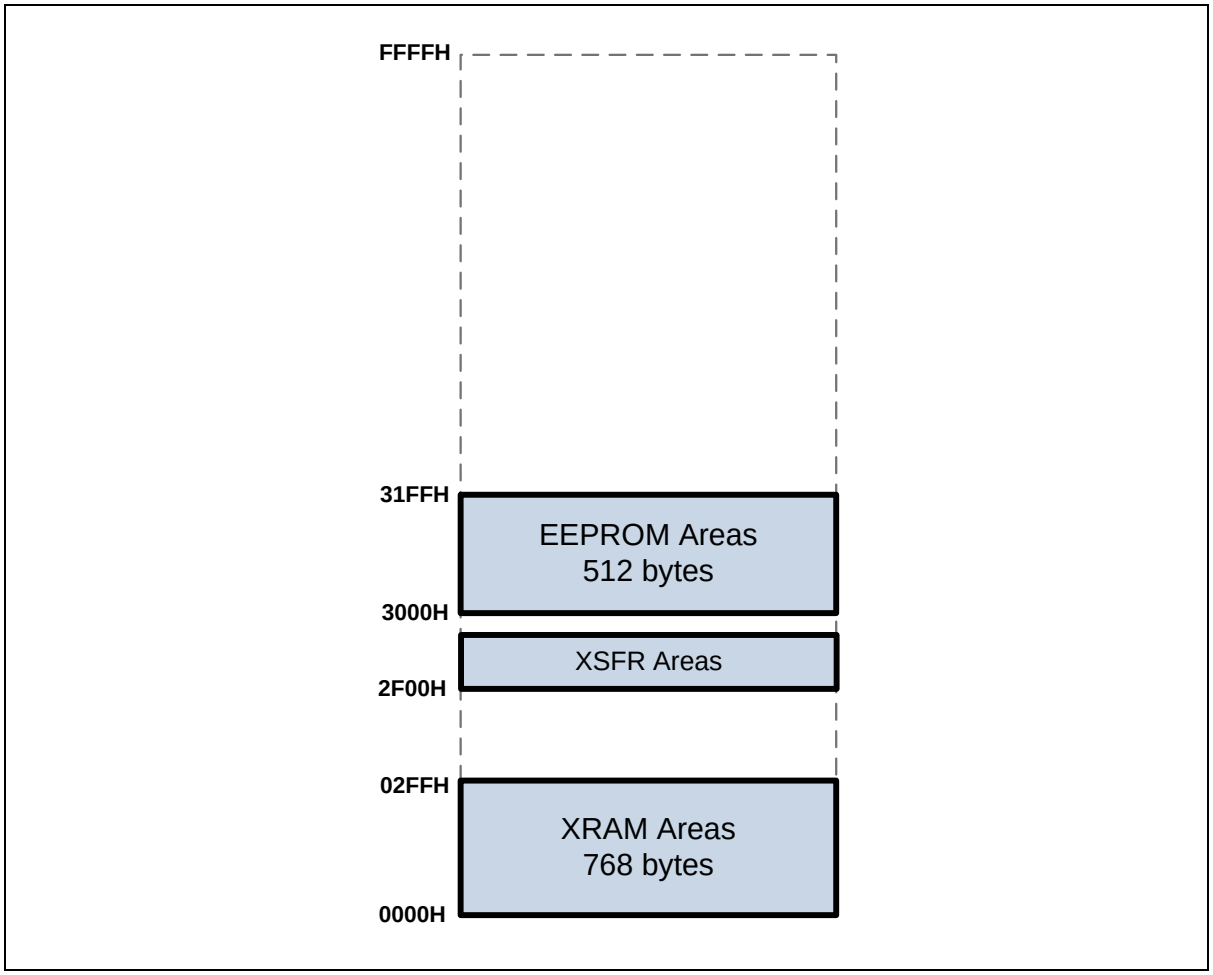


Figure 11. XDATA Memory Area

4.4 SFR map

4.4.1 SFR map summary

Table 4. SFR Map Summary

						-	Reserved	
							M8050 Compatible	
	0H/8H(1)	**1H/9H**	**2H/AH**	**3H/BH**	**4H/CH**	**5H/DH**	**6H/EH**	**7H/FH**
F8H	-	ACCSR	UCTRL11	UCTRL12	UCTRL13	USTAT1	UBAUD1	UDATA1
F0H	B	-	FEARL	FEARM	FEARH	FEDR	-	-
E8H	-	-	FEMR	FECR	FESR	FETCR	-	-
E0H	ACC	-	UCTRL01	UCTRL02	UCTRL03	USTAT0	UBAUD0	UDATA0
D8H	-	-	I2CMR	I2CSR	I2CSCLLR	I2CSCLHR	I2CSDAHR	I2CDR
D0H	PSW	-	SPICR	SPIDR	SPISR	T4H/ T4HDR/ HCDR4	I2CSAR1	I2CSAR
C8H	ADCRL	ADCRH	T3CR	T3DR / T3PPR	T3 /T3PDR / CDR3	T3PWHR	T4CR	T4L/ T4LDR/ LCDR4
C0H	ADCM	ADCM2	T1DLYB	T1DLYC	T1ISR	T1IMSK	T2CR	T2 / T2DR / CDR2
B8H	-	T1BDRL	T1BDRH	T1CDRL	T1CDRH	T1PCR2	T1PCR3	T1DLYA
B0H	T1 / T1ADRL / CDR1	T1ADRH	T0CR	T0 / T0DR / CDR0	T1CR	T1DR /T1PPRL	T1PPRH	T1PCR
A8H	IE	IE1	IE2	IE3	-	-	PCI0	TMISR
A0H	XBANK	P3IO	EO	EIENAB	EIFLAG	EIEDGE	EIPOLA	EIBOTH
98H	P3	P2IO	IP1	IP1H	IP2	IP2H	IP3	IP3H
90H	P2	P1IO	IP	IPH	PLLCR	WTMR	WTR / WTCR	BUZCR
88H	P1	P0IO	SCCR	BCCR	BITR	WDTCR	WDTIDR	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVRCR	PCON

NOTE: 00H/8H, these registers are bit-addressable

Table 5. XSFR Map Summary

	0H/8H[1]	1H/9H	2H/AH	3H/BH	4H/CH	5H/DH	6H/EH	7H/FH
2F58H	-	-	-	-	-	-	-	-
2F50H	FUSE_CONF	-	-	-	-	-	-	-
2F48H	-	-	-	-	-	-	-	-
2F40H	-	-	-	-	-	-	-	-
2F38H	-	-	-	-	-	-	-	-
2F30H	-	-	-	-	-	-	-	-
2F28H	-	-	-	-	-	-	-	-
2F20H	-	-	-	-	-	-	-	-
2F18H	-	-	-	-	-	-	-	-
2F10H	PSR0	PSR1	PSR2	-	WDTC	WDTSR	WDTCNTH	WDTCNTL
2F08H	P0DB	P1DB	P2DB	P3DB	-	-	-	-
2F00H	P0PU	P1PU	P2PU	P3PU	P0OD	P1OD	P2OD	P3OD

4.4.2 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVRCR	R/W	1	0	0	0	0	0	0	1
87H	Power Control Register	PCON	R/W	0	0	0	0	0	0	0	0
88H	P1 Data Register	P1	R/W	-	0	0	0	0	0	0	0
89H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	0	0	0	0	0	1	0	0
8BH	Basic Interval Timer Clock Control Register	BCCR	R/W	0	0	0	0	0	1	0	1
8CH	Basic Interval Timer Counter Register	BITR	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	0	0	1	1	1
8EH	Watch Dog Timer Identification Register	WDTIDR	R/W	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	-	0	0	0	0	0	0	0
91H	P1 Direction Register	P1IO	R/W	-	0	0	0	0	0	0	0
92H	Interrupt Priority Register	IP	R/W	0	0	0	0	0	0	0	0
93H	Interrupt Priority Register High	IPH	R/W	0	0	0	0	0	0	0	0
94H	Timer1 PLL Control Register	PLLCR	R/W	0	1	0	0	0	0	1	0
95H	Watch Timer Mode Register	WTMR	R/W	0	0	0	0	0	0	0	0
96H	Watch Timer Counter Register	WTCR	R	0	0	0	0	0	0	0	0
	Watch Timer Register	WTR	W	0	1	1	1	1	1	1	1
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
99H	P2 Direction Register	P2IO	R/W	-	0	0	0	0	0	0	0
9AH	Interrupt Priority Register 1	IP1	R/W	0	0	0	0	0	0	0	0
9BH	Interrupt Priority Register 1 High	IP1H	R/W	0	0	0	0	0	0	0	0
9CH	Interrupt Priority Register 2	IP2	R/W	0	0	0	0	0	0	0	0
9DH	Interrupt Priority Register 2 High	IP2H	R/W	0	0	0	0	0	0	0	0
9EH	Interrupt Priority Register 3	IP3	R/W	0	0	0	0	0	0	0	0
9FH	Interrupt Priority Register 3 High	IP3H	R/W	0	0	0	0	0	0	0	0
A0H	XRAM Bank Pointer	XBANK	R/W	0	0	0	0	0	0	0	0
A1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	-	-	-	0	-	-	-	0
A3H	External Interrupt Enable Register	EIENAB	R/W	0	0	0	0	0	0	0	0
A4H	External Interrupt Flag Register	EIFLAG	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Edge Register	EIEDGE	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A6H	External Interrupt Polarity Register	EIPOLA	R/W	0	0	0	0	0	0	0	0
A7H	External Interrupt Both Edge Enable Register	EIBOTH	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	0	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	0	0	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	0	0	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	0	0	0	0	0	0	0	0
AEH	P0 Pin Change Interrupt Enable Register	PCI0	R/W	0	0	0	0	0	0	0	0
AFH	Timer Interrupt Status Register	TMISR	R/W	-	-	0	0	0	0	0	0
B0H	Timer 1 Register	T1	R	0	0	0	0	0	0	0	0
	Timer 1 PWM 1A Duty Register	T1ADRL	R/W	0	1	1	1	1	1	1	1
	Capture 1 Data Register	CDR1	R	0	0	0	0	0	0	0	0
B1H	Timer 1 PWM 1A Duty Register High	T1ADRH	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Mode Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
B3H	Timer 0 Register	T0	R	0	0	0	0	0	0	0	0
	Timer 0 Data Register	T0DR	W	1	1	1	1	1	1	1	1
	Capture 0 Data Register	CDR0	R	0	0	0	0	0	0	0	0
B4H	Timer 1 Mode Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
B5H	Timer 1 Data Register	T1DR	W	1	1	1	1	1	1	1	1
	Timer 1 PWM Period Register Low	T1PPRL	W	1	1	1	1	1	1	1	1
B6H	Timer 1 PWM Period Register HIGH	T1PPRH	W	1	1	1	1	1	1	1	1
B7H	Timer 1 PWM Control Register	T1PCR	R/W	0	0	0	0	0	0	0	0
B9H	Timer 1 PWM 1B Duty Register Low	T1BDRL	R/W	0	1	1	1	1	1	1	1
BAH	Timer 1 PWM 1B Duty Register High	T1BDRH	R/W	0	0	0	0	0	0	0	0
BBH	Timer 1 PWM 1C Duty Register Low	T1CDRL	R/W	0	1	1	1	1	1	1	1
BCH	Timer 1 PWM 1C Duty Register High	T1CDRH	R/W	0	0	0	0	0	0	0	0
BDH	Timer 1 PWM Control Register 2	T1PCR2	R/W	0	0	0	0	0	0	0	0
BEH	Timer 1 PWM Control Register 3	T1PCR3	R/W	0	0	0	0	0	0	0	0
BFH	PWM1 Non-Overlap Delay Register for ch. A/AB	T1DLYA	R/W	0	0	0	0	0	0	0	0
C0H	A/D Converter Mode Register	ADCM	R/W	1	0	0	0	1	1	1	1
C1H	A/D Converter Mode 2 Register	ADCM2	R/W	1	0	0	0	1	1	1	1
C2H	PWM1 Non-Overlap Delay Register for ch. B/BB	T1DLYB	R/W	0	0	0	0	0	0	0	0
C3H	PWM1 Non-Overlap Delay Register for ch. C/CB	T1DLYC	R/W	0	0	0	0	0	0	0	0
C4H	Timer 1 Interrupt Status Register	T1ISR	R/W	0	0	0	0	0	0	0	0
C5H	Timer 1 Interrupt Mask Register	T1IMSK	R/W	0	0	0	0	0	0	0	0
C6H	Timer 2 Mode Control Register	T2CR	R/W	0	0	0	0	0	0	0	0
C7H	Timer 2 Register	T2	R	0	0	0	0	0	0	0	0
	Timer 2 Data Register	T2DR	W	1	1	1	1	1	1	1	1
	Capture 2 Data Register	CDR2	R	0	0	0	0	0	0	0	0
C8H	A/D Converter Result High Register	ADCRL	R	-	-	-	-	-	-	-	-
C9H	A/D Converter Result Low Register	ADCRH	R	-	-	-	-	-	-	-	-
CAH	Timer 3 Mode Control Register	T3CR	R/W	0	0	0	0	0	0	0	0
CBH	Timer 3 Data Register	T3DR	W	1	1	1	1	1	1	1	1
	Timer 3 PWM Period Register	T3PPR	W	1	1	1	1	1	1	1	1

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
CCH	Timer 3 Register	T3	R	0	0	0	0	0	0	0	0
	Timer 3 PWM Duty Register	T3PDR	R/W	1	1	1	1	1	1	1	1
	Capture 3 Data Register	CDR3	R	0	0	0	0	0	0	0	0
CDH	Timer 3 PWM High Register	T3PWHR	W	0	0	0	0	0	0	0	0
CEH	Timer 4 Mode Control Register	T4CR	R/W	0	0	0	0	0	0	0	0
CFH	Timer 4 Low Register	T4L	R	0	0	0	0	0	0	0	0
	Timer 4 Low Data Register	T4LDR	W	1	1	1	1	1	1	1	1
	Low Capture 4 Data Register	LCDR4	R	0	0	0	0	0	0	0	0
D0H	Program Status Word	PSW	R/W	0	0	0	0	0	0	0	0
D2H	SPI Control Register	SPICR	R/W	0	0	0	0	0	0	0	0
D3H	SPI Data Register	SPIDR	R/W	0	0	0	0	0	0	0	0
D4H	SPI Status Register	SPISR	R/W	0	0	0	0	0	0	0	0
D5H	Timer 4 High Register	T4H	R	0	0	0	0	0	0	0	0
	Timer 4 High Data Register	T4HDR	W	1	1	1	1	1	1	1	1
	High Capture 4 Data Register	HCDR4	R	0	0	0	0	0	0	0	0
D6H	I2C Slave Address Register 1	I2CSAR1	R/W	0	0	0	0	0	0	0	0
D7H	I2C Slave Address Register	I2CSAR	R/W	0	0	0	0	0	0	0	0
DAH	I2C Mode Control Register	I2CMR	R/W	0	0	0	0	0	0	0	0
DBH	I2C Status Register	I2CSR	R	0	0	0	0	0	0	0	0
DCH	SCL Low Period Register	I2CSCLLR	R/W	0	0	1	1	1	1	1	1
DDH	SCL High Period Register	I2CSCLHR	R/W	0	0	1	1	1	1	1	1
DEH	SDA Hold Time Register	I2CSDAHR	R/W	0	0	0	0	0	0	0	1
DFH	I2C Data Register	I2CDR	R/W	1	1	1	1	1	1	1	1
E0H	Accumulator	ACC	R/W	0	0	0	0	0	0	0	0
E2H	USART Control 1 Register 0	UCTRL01	R/W	0	0	0	0	0	0	0	0
E3H	USART Control 2 Register 0	UCTRL02	R/W	0	0	0	0	0	0	0	0
E4H	USART Control 3 Register 0	UCTRL03	R/W	0	0	0	0	0	0	0	0
E5H	USART Status Register 0	USTAT0	R	1	0	0	0	0	0	0	0
E6H	USART Baud Rate Generation Register 0	UBAUD0	R/W	1	1	1	1	1	1	1	1
E7H	USART Data Register 0	UDATA0	R/W	1	1	1	1	1	1	1	1
EAH	Flash and EEPROM Mode Register	FEMR	R/W	0	0	0	0	0	0	0	0
EBH	Flash and EEPROM Control Register	FECR	R/W	0	0	0	0	0	0	1	1
ECH	Flash and EEPROM Status Register	FESR	R/W	1	0	0	0	0	0	0	0
EDH	Flash and EEPROM Time Control Register	FETCR	R/W	0	0	0	0	0	0	0	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F2H	Flash and EEPROM Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0
F3H	Flash and EEPROM Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
F4H	Flash and EEPROM Address High Register	FEARH	R/W	0	0	0	0	0	0	0	0
F5H	Flash and EEPROM Data Register	FEDR	R/W	0	0	0	0	0	0	0	0
F9H	Analog Comparator Control & Status Register	ACCSR	R/W	0	0	0	0	0	0	0	0
FAH	USART Control 1 Register 1	UCTRL11	R/W	0	0	0	0	0	0	0	0
FBH	USART Control 2 Register 1	UCTRL12	R/W	0	0	0	0	0	0	0	0
FCH	USART Control 2 Register 1	UCTRL13	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
FDH	USART Status Register 1	USTAT1	R	1	0	0	0	0	0	0	0
FEH	USART Baud Rate Generation Register 1	UBAUD1	R/W	1	1	1	1	1	1	1	1
FFH	USART Data Register 1	UDATA1	R/W	1	1	1	1	1	1	1	1
-	-	-	-	-	-	-	-	-	-	-	-
2F00H	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
2F01H	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
2F02H	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
2F03H	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
2F04H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
2F05H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
2F06H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
2F07H	P3 Open-drain Selection Register	P3OD	R/W	0	0	0	0	0	0	0	0
2F08H	P0 Debounce Enable Register	P0DB	R/W	0	0	0	0	0	0	0	0
2F09H	P1 Debounce Enable Register	P1DB	R/W	0	0	0	0	0	0	0	0
2F0AH	P2 Debounce Enable Register	P2DB	R/W	0	0	0	0	0	0	0	0
2F0BH	P3 Debounce Enable Register	P3DB	R/W	0	0	0	0	0	0	0	0
2F10H	Port Selection Register 0	PSR0	R/W	0	0	0	0	0	0	0	0
2F11H	P1,P2,P3 Port Selection Register	PSR1	R/W	0	0	0	0	0	0	0	0
2F12H	Special Port Selection Register	PSR2	R/W	0	0	0	0	0	0	0	0
2F14H	Watch Dog Timer Clear Register	WDTC	R/W	0	0	0	0	0	0	0	0
2F15H	Watch Dog Timer Status Register	WDTSR	R/W	0	0	0	0	0	0	0	0
2F16H	Watch Dog Timer Count H Register	WDTCNTH	R	0	0	0	0	0	0	0	0
2F17H	Watch Dog Timer Count L Register	WDTCNTL	R	0	0	0	0	0	0	0	0
2F50H	Pseudo-Configure Data	FUSE_CONF	R/W	0	0	0	0	0	0	0	0

5 I/O ports

MC97FG316/MC97FG216 has four groups of I/O ports (P0 ~ P3). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. P0 includes a function that can generate interrupt signals according to state of a pin.

5.1 P0 port description

P0 is an 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), P0 pull-up resistor selection register (P0PU), P0 open-drain selection register (P0OD), debounce enable register (P0DB) and pin change interrupt register (PCI0). Refer to the port selection registers for the P0, P1, P2 and P3 function selection.

5.2 P1 port description

P1 is a 7-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), P1 pull-up resistor selection register (P1PU), P1 open-drain selection register (P1OD) and debounce enable register (P1DB). Refer to the port selection registers for the P0, P1, P2 and P3 function selection.

5.3 P2 port description

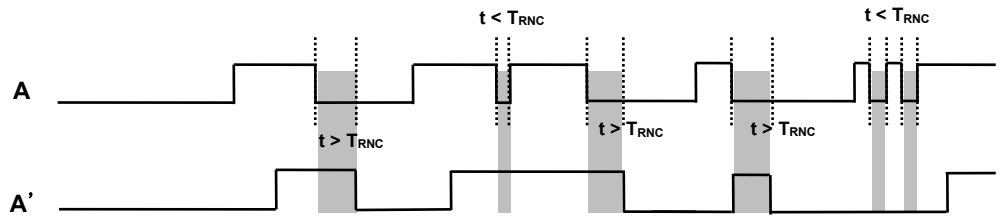
P2 is a 7-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU), P2 open-drain selection register (P2OD) and debounce enable register (P2DB). Refer to the port selection registers for the P1, P2, P3 and P3 function selection.

5.4 P3 port description

P3 is an 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO), P3 pull-up resistor selection register (P3PU) and debounce enable register (P3DB). Refer to the port selection registers for the P1, P2, P3 and P3 function selection.

5.5 Port noise canceller

Figure 12 is the noise canceller time diagram for Noise cancel of Port. The noise cancel value is about 4us to Port input.



NOTE: Noise canceller clock of port is about 1MHz/4(about 4us).

Figure 12. Port Noise Canceller Time Diagram

6 Interrupt controller

MC97FG316/MC97FG216 supports up to 24 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. In addition, they have four levels of priority assigned to themselves.

A non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources and is not controllable by software.

Interrupt controller of MC97FG316/MC97FG216 has following features:

- Request receive from the 24 interrupt sources
- 6 groups of priority
- 4 levels of priority
- Multi Interrupt possibility
- A request of higher priority level is served first, when multiple requests of different priority levels are received simultaneously.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency of 3 to 9 machine cycles in single interrupt system

A non-maskable interrupt is always enabled, while maskable interrupts are enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source.

Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction.

The MC97FG316/MC97FG216 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP, IPH, IP1, IP1H, IP2, IP2H, IP3 and IP3H.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Figure 13 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IPx, another one from IPxH).

Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one. And small number interrupt has higher priority than large number interrupt in the same level.

Figure 13 shows INT10 is higher priority small than any interrupt (Priority order: INT10 > INT4 > INT19 > INT0 > INT1 > ~~ > INT23).

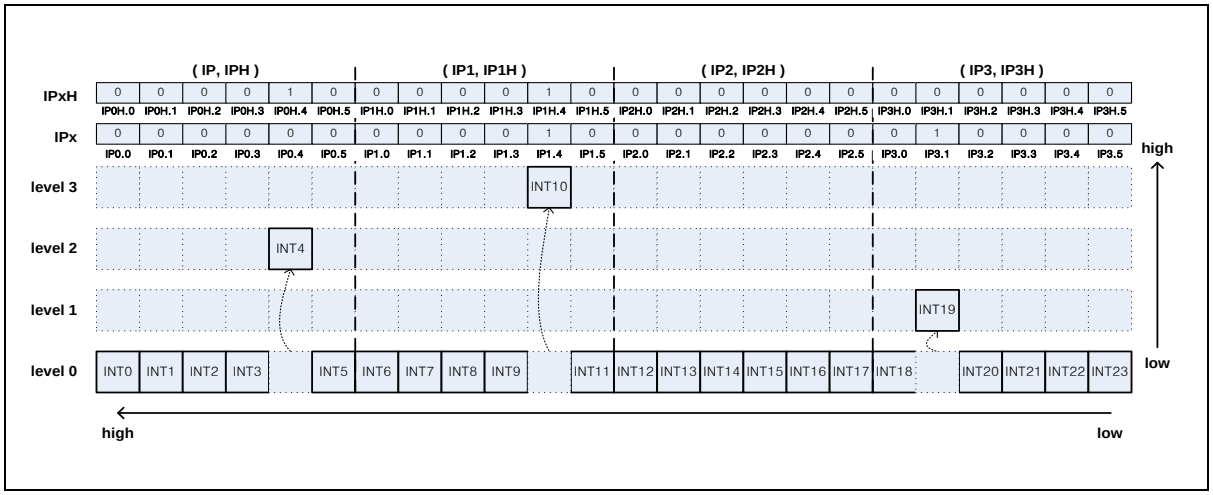
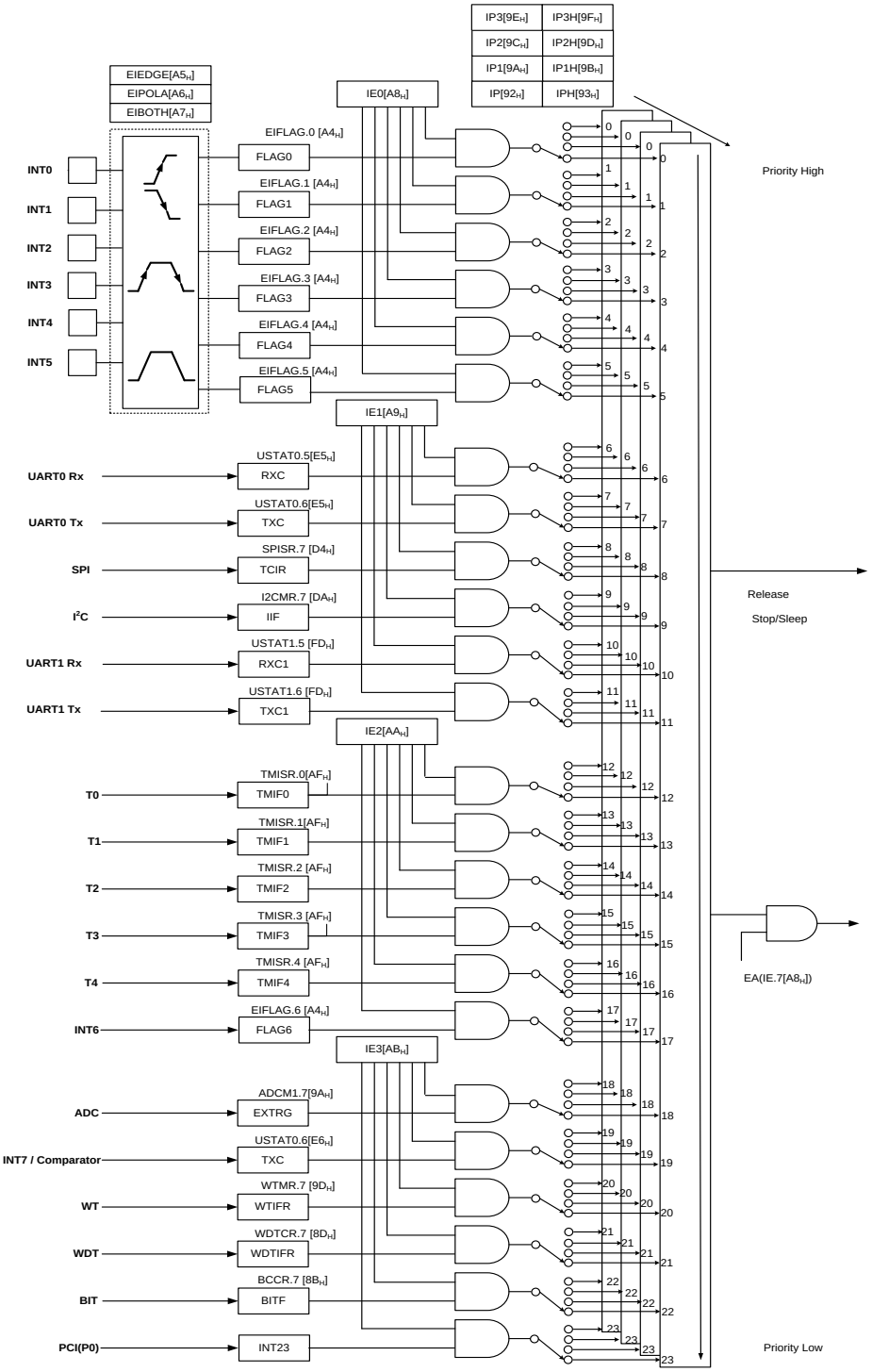


Figure 13. Interrupt Group Priority Level

6.1 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

Figure 14. Interrupt Controller Block Diagram

6.2 Interrupt vector table

Interrupt controller of MC97FG316/MC97FG216 supports 24 interrupt sources as shown in Table 7. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 7. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware Reset	RESETB	—	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
External Interrupt 2	INT2	IE.2	3	Maskable	0013H
External Interrupt 3	INT3	IE.3	4	Maskable	001BH
External Interrupt 4	INT4	IE.4	5	Maskable	0023H
External Interrupt 5	INT5	IE.5	6	Maskable	002BH
USART0 Rx Interrupt	INT6	IE1.0	7	Maskable	0033H
USART0 TX Interrupt	INT7	IE1.1	8	Maskable	003BH
SPI0 Interrupt	INT8	IE1.2	9	Maskable	0043H
I2C Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
UART1 Rx Interrupt	INT10	IE1.4	11	Maskable	0053H
UART1 Tx Interrupt	INT11	IE1.5	12	Maskable	005BH
T0 Match Interrupt	INT12	IE2.0	13	Maskable	0063H
T1 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T2 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T3 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T4 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
External Interrupt 6	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
External Interrupt 7 / Comparator Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
Pin Change Interrupt	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’.

And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

7 Clock generator

As shown in Figure 15, a clock generator produces basic clock pulses which provide a system clock for CPU and peripheral hardware.

It contains main/sub-frequency clock oscillator. The main/sub clock can operate easily by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. For this, it is necessary to place external clock signal into the XIN/SXIN pin and open XOUT/SXOUT pin.

Default system clock is 16MHz INT-RC Oscillator. To stabilize the system internally, 1MHz RING INT-RC oscillator on POR is used for BIT, WDT and ports de-bounce function.

Oscillators in the clock generator are introduced in the followings:

- Calibrated high internal RC oscillator (16MHz)
  - INT-RC OSC/1 (16MHz, default system clock)
  - INT-RC OSC/2 (8MHz)
  - INT-RC OSC/4 (4MHz)
  - INT-RC OSC/8 (2MHz)
- Main crystal oscillator (4~16MHz)
- Sub-crystal Oscillator (32.768kHz)
- Internal RING oscillator (1MHz)

7.1 Clock generator block diagram

In this section, a clock generator of MC97FG316/MC97FG216 is described in a block diagram.

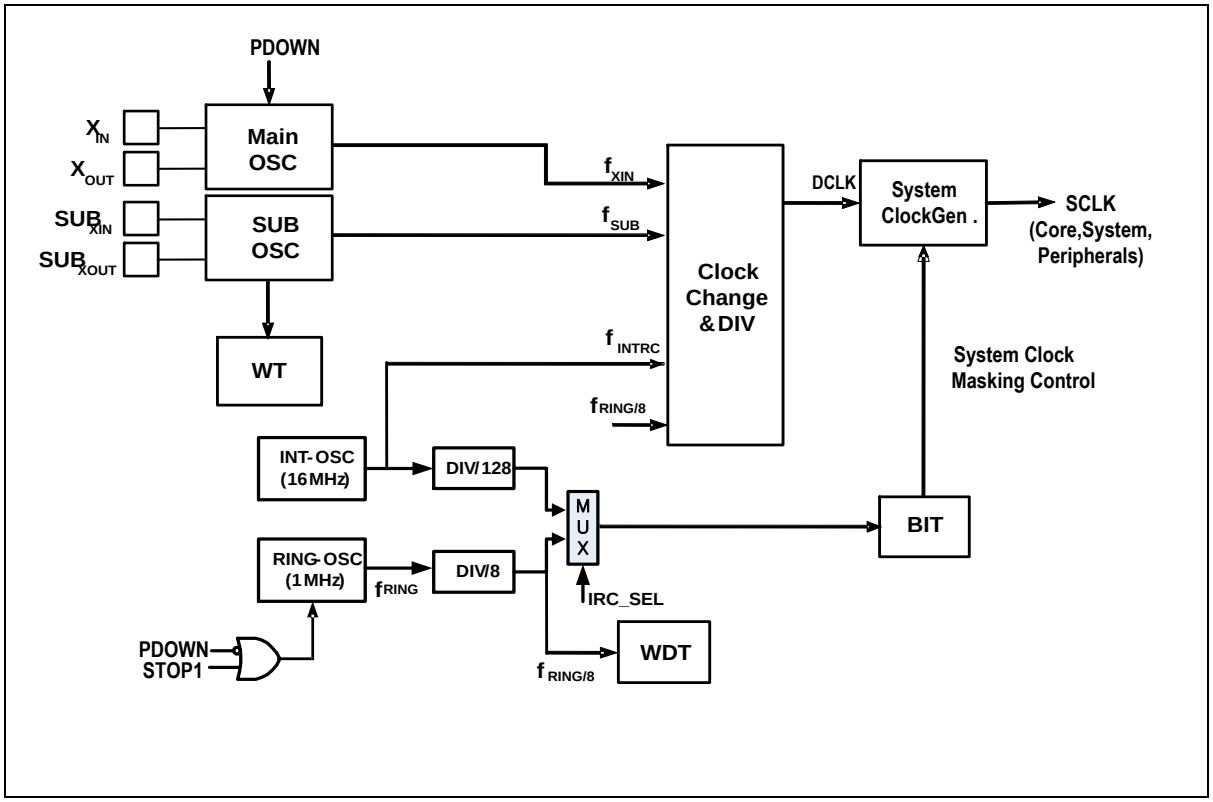


Figure 15. Clock Generator Block Diagram

8 Basic Interval Timer (BIT)

MC97FG316/MC97FG216 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting and provides a basic interval timer interrupt (BITF).

BIT of MC97FG316/MC97FG216 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

8.1 BIT block diagram

In this section, the BIT of MC97FG316/MC97FG216 is described in a block diagram.

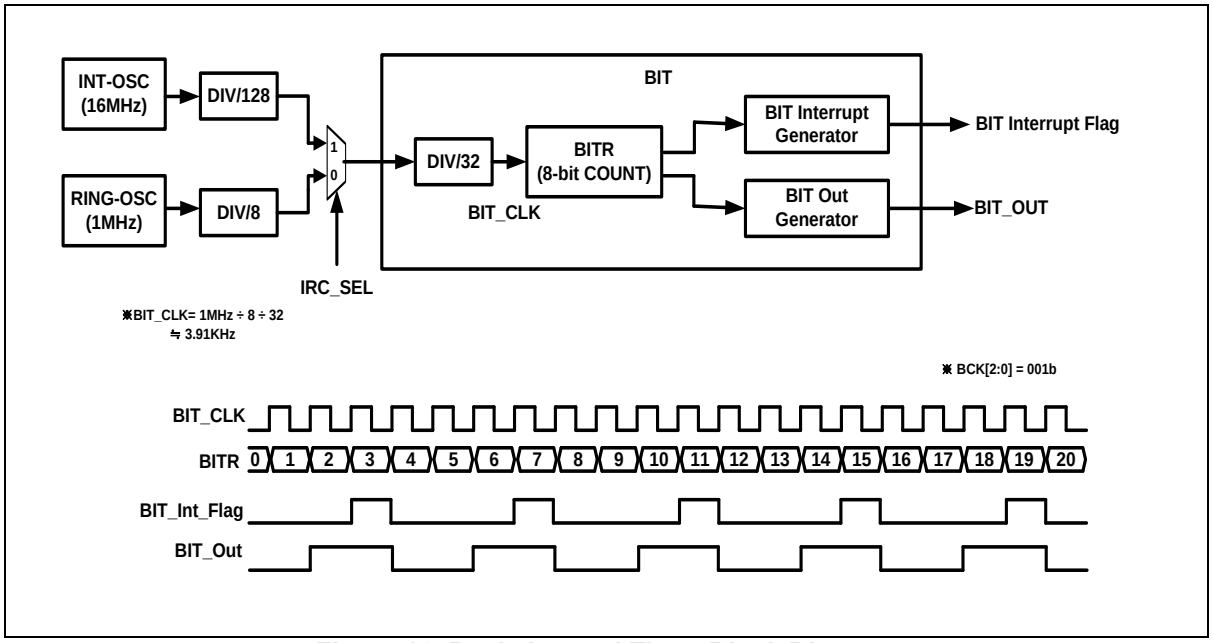


Figure 16. Basic Interval Timer Block Diagram

9 Watchdog Timer (WDT)

Watchdog Timer (WDT) rapidly detects the CPU malfunction such as endless looping caused by noise or something like that and resumes the CPU to the normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

When 75% of the overflow time is reached, a watchdog interrupt can be generated. The overflow time of the watchdog timer can select by WDTOVF [2:0] of WDTCR. If an overflow occurs, an internal reset is generated. The WDTRC operation in the STOP/IDLE mode differs as follows depending on the setting value of WDTPDON. If WDTPDON = 0, the WDTRC operation stop in the STOP/IDLE mode and if WDTPDON = 1, the WDTRC operation in the STOP/IDLE mode. The watchdog timer operate on the 3.9 kHz, based on clock that divided the embedded 1MHz Ring oscillator clock by 8.

A watchdog reset is occurred in the following cases:

- When the watchdog timer counter overflows,
- When the data except “96H” is written to the WDTC register,
- When the data “96H” is written to the WDTC register during a window close period,

9.1 WDT block diagram

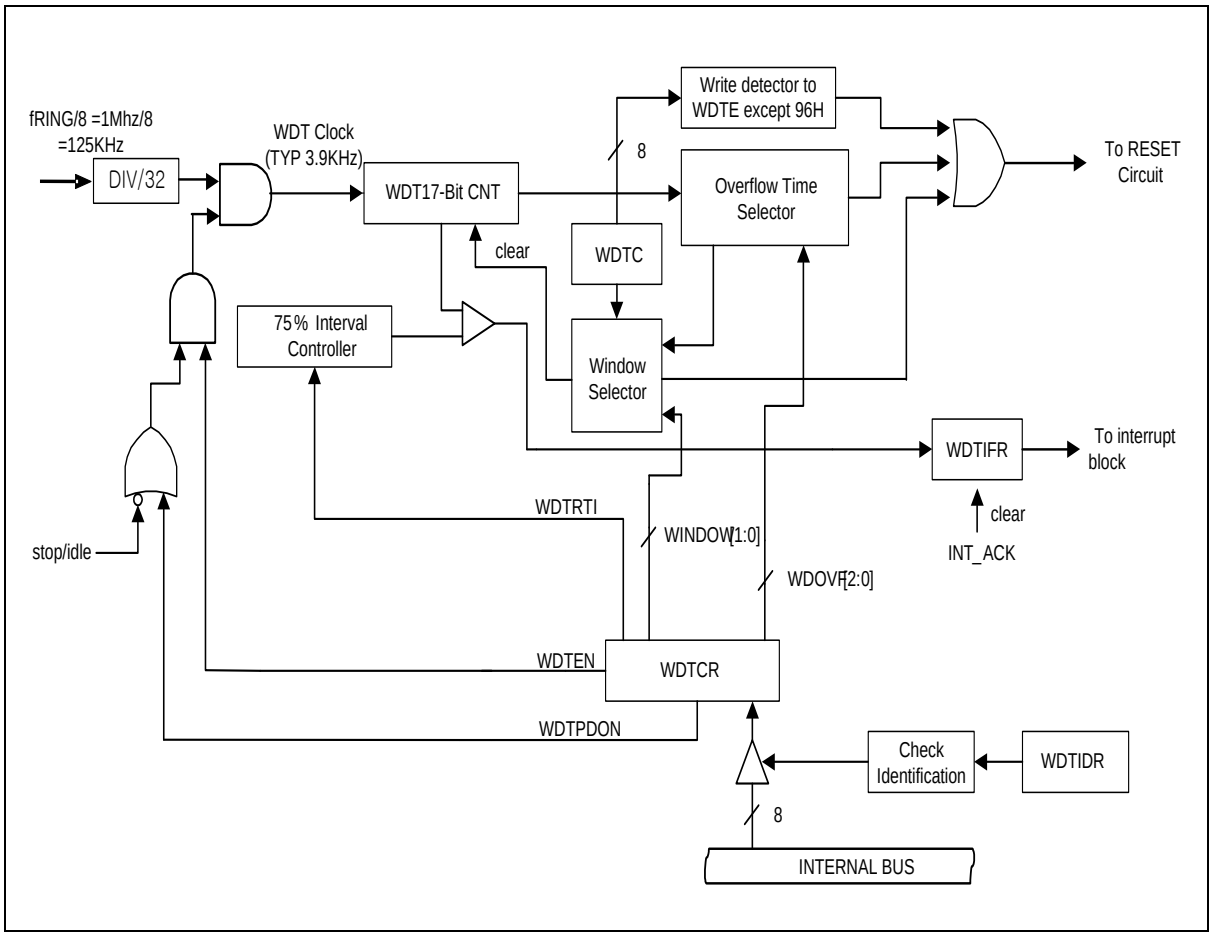


Figure 17. WDT Block Diagram

10 Watch Timer (WT)

Watch Timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval and to set WTEN to '1' in watch timer mode register (WTMR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTMR register.

Although CPU is in STOP mode, a sub clock can be alive so that WT continues its operation. Watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to increase resolution. In WTR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

10.1 WT block diagram

In this section, watch timer of MC97FG316/MC97FG216 is described in a block diagram.

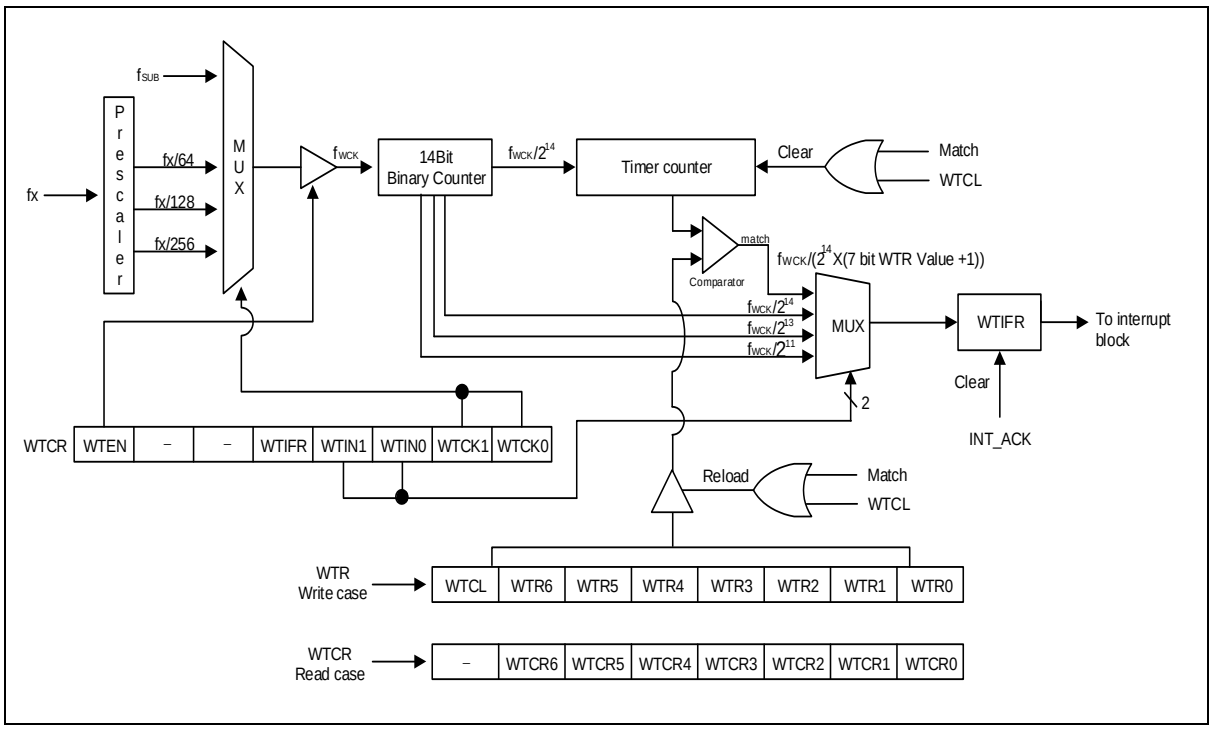


Figure 18. Watch Timer Block Diagram

11 Timer/PWM

11.1 8-bit timer/event counter 0, 1

Timer 0 and timer 1 can be used as either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter consists of a multiplexer, a timer data register, a counter register, a mode register, an input capture register and a comparator. For PWM, it has PWM register (T1PPRH, T1PPRL, T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CDR, T1PCR, T1PCR2, T1PCR3, T1PHR, T1DLYA, T1DLYB, T1DLYC, T1ISR, T1IMSK).

Timer/Event Counter 0, 1 operates one of seven modes introduced in followings:

- 8-bit timer/counter mode
- 8-bit capture mode
- 8-bit compare output mode
- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit compare output mode
- PWM mode

NOTE: TxDR must be set to higher than 0x03 for guaranteeing operation.

Timer/counter can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock select logic which is controlled by the clock select (T0CK[2:0], T1CK[3:0]). Also Timer/PWM/Event counter 1 can use more clock sources than Timer/Event counter 0.

- TIMER0 clock source: fX/(2, 4, 8, 32, 128, 512, 2048), EC0
- TIMER1 clock source: fX/(1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384), T0CK

In capture mode, the data is captured into input capture register (CDR0, CDR1) by INT0, INT1. In timer/counter mode, whenever counter 0 (T0) value is equal to T0DR, T0O port toggles in 8/16-bit mode. In addition, Timer 1 outputs the result to T1O port in the timer mode. In addition, Timer 1 outputs PWM wave form through PWMAA, PWMAB (bar), PWMBA, PWMBB (bar), PWMCA and PWMCB (bar) Port in the 6-channel PWM mode.

Table 8. Timer 0, 1 Operating Modes

16BIT	CAP0	CAP1	PWM1E	T0CK[2:0]	T1CK[3:0]	T0/1_PE	Timer 0	Timer 1
0	0	0	0	XXX	XXXX	00	8-bit Timer	8-bit Timer
0	0	1	0	111	XXXX	00	8-bit Event Counter	8-bit Capture
0	1	0	0	XXX	XXXX	01	8-bit Capture	8-bit Compare Output
0	0	0	1	XXX	XXXX	11	8-bit Timer/Counter	10-bit PWM
1	0	0	0	XXX	1111	00	16-bit Timer	
1	0	0	0	111	1111	00	16-bit Event Counter	
1	1	1	0	XXX	1111	00	16-bit Capture	
1	0	0	0	XXX	1111	01	16-bit Compare Output	

11.1.1 8-bit timer/event counter block diagram

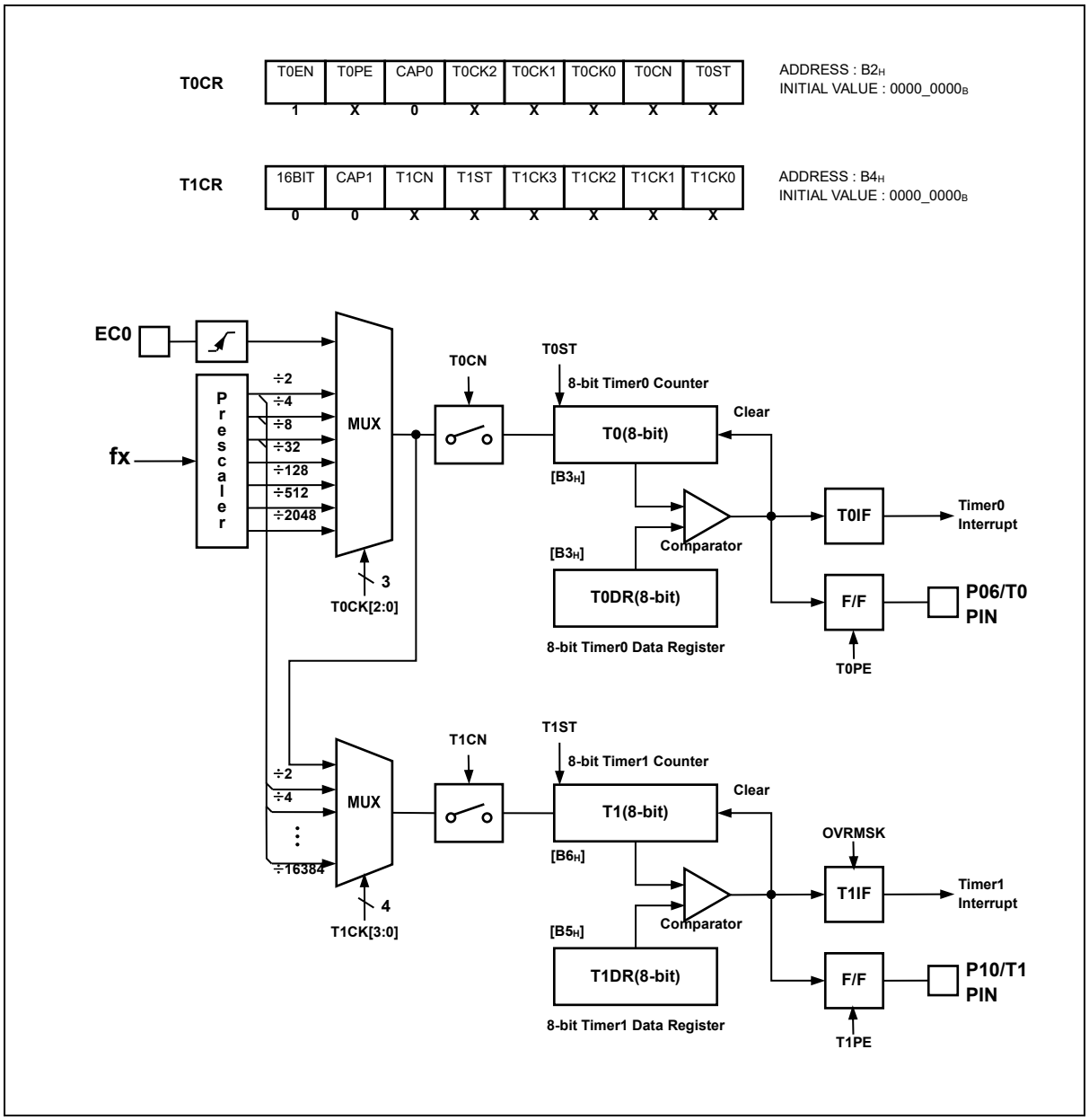


Figure 19. 8-bit Timer/Event Counter 0, 1 Block Diagram

11.1.2 16-bit timer/counter mode block diagram

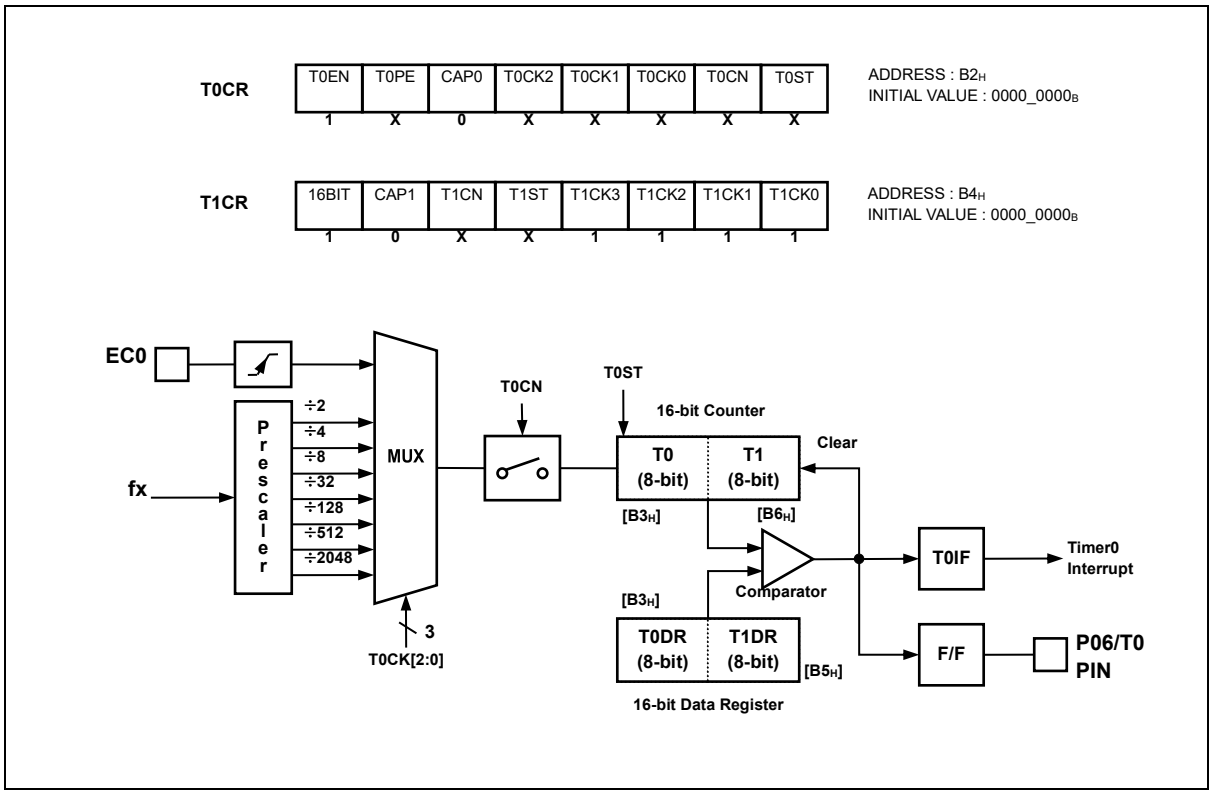


Figure 20. 16-bit Timer/Counter for Time 0, 1

11.1.3 8-bit capture mode block diagram

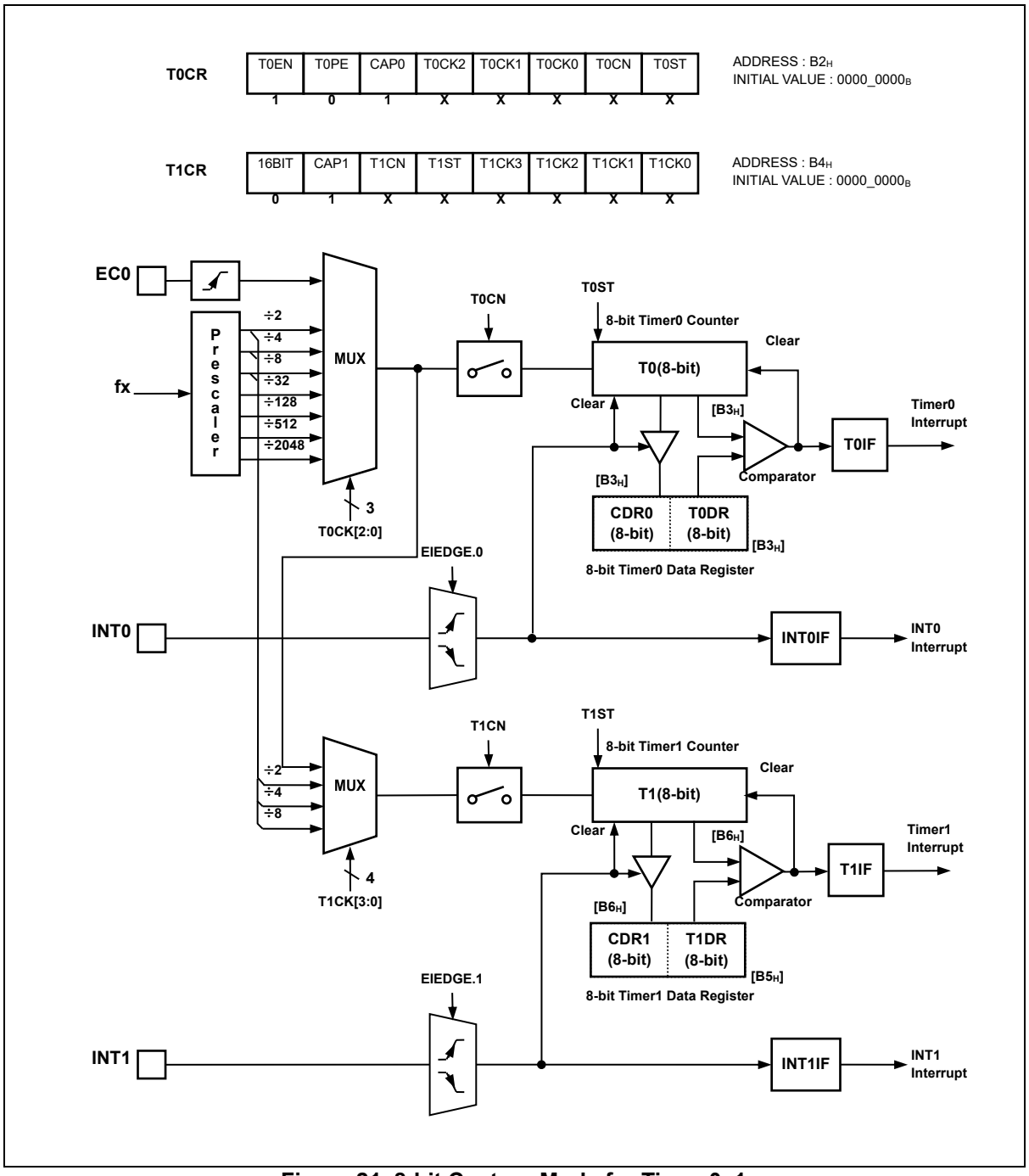


Figure 21. 8-bit Capture Mode for Timer 0, 1

11.1.4 16-bit capture mode block diagram

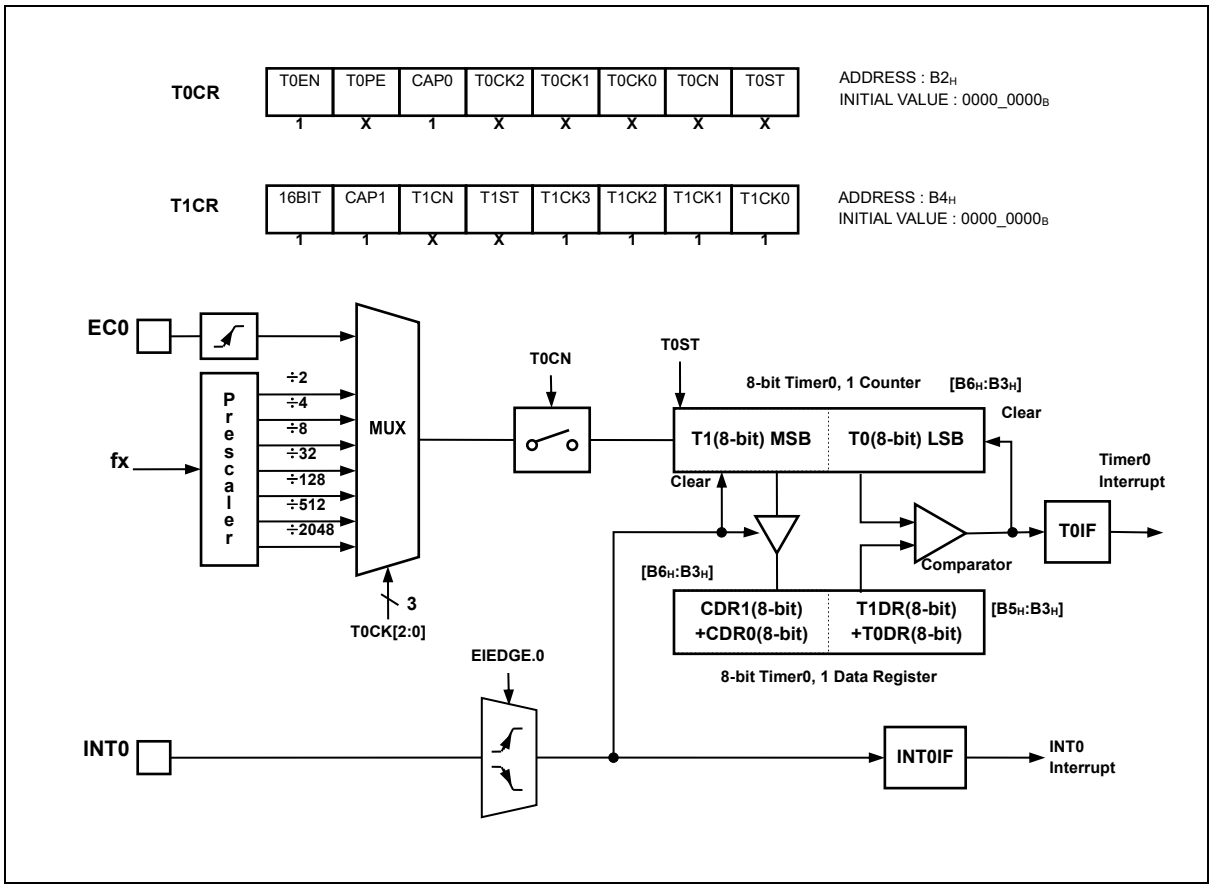


Figure 22. 16-bit Capture Mode of Timer 0, 1

11.1.5 PWM mode block diagram

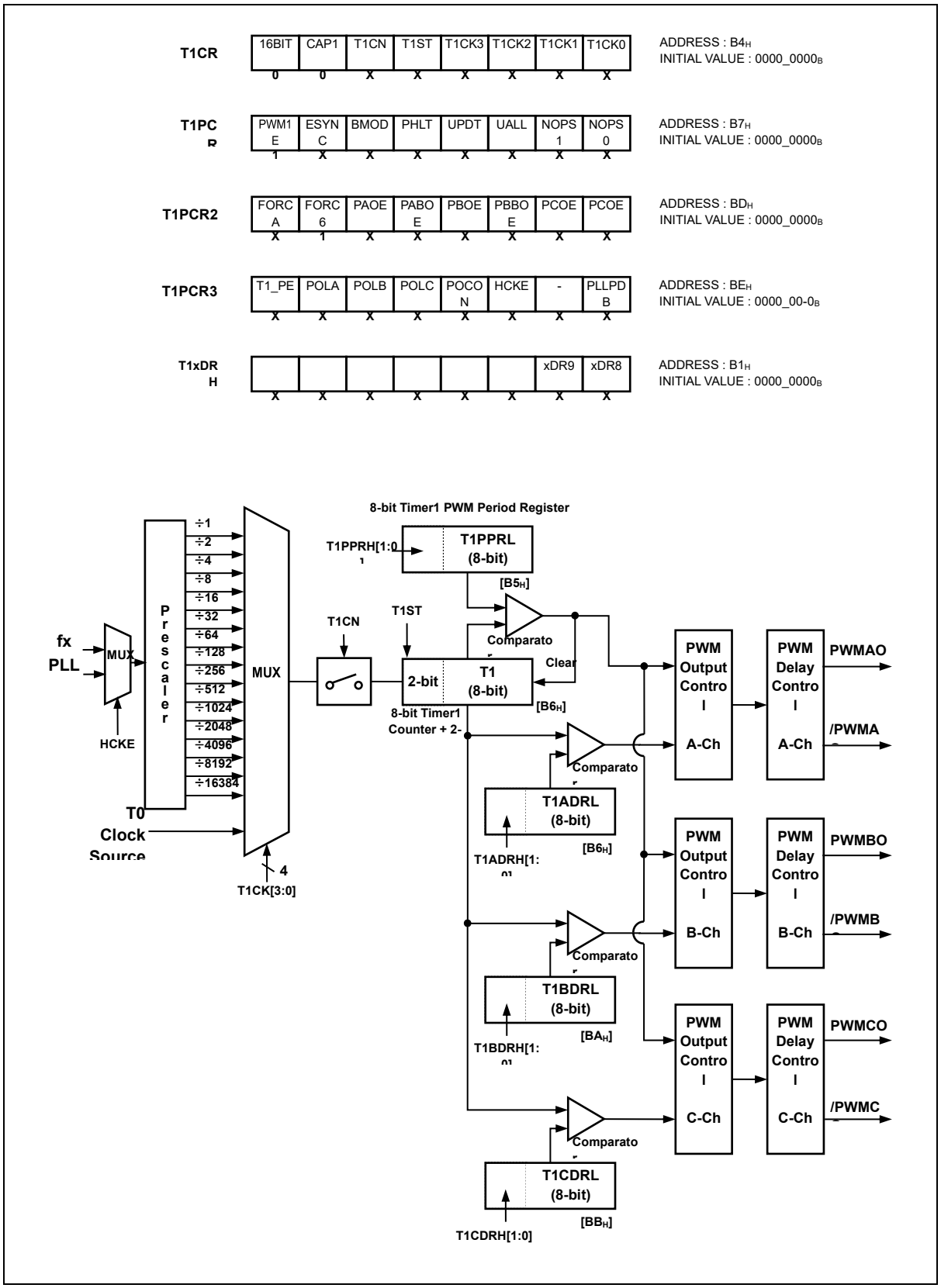


Figure 23. PWM Mode (Force 6-ch) for Timer 1

11.2 8-bit timer/event counter 2, 3

Timer 2 and timer 3 can be used as either two 8-bit timer/counter or one 16-bit timer/counter. Each 8-bit timer/event counter consists of a multiplexer, a timer data register, a counter register, a mode register, an input capture register and a comparator. For PWM, it has PWM register (T3PPR, T3PDR, T3PWHR).

Timer/Event Counter 2, 3 operates one of seven modes introduced in followings:

- 8-bit Timer/Counter Mode
- 8-bit Capture Mode
- 8-bit Compare Output Mode
- 16-bit Timer/Counter Mode
- 16-bit Capture Mode
- 16-bit Compare Output Mode
- PWM Mode

Timer/counter can be clocked by an internal or external clock source (EC2). The clock source is selected by clock select logic which is controlled by the clock select (T2CK[2:0], T3CK[1:0]).

- TIMER2 clock source: fX/(1, 2, 4, 64, 256, 1024, 4096), EC2
- TIMER3 clock source: fX/(1, 2, 16), T2CK

In the capture mode, the data is captured into the input capture register (CDR2, CDR3) by INT2, INT3. In timer/counter mode, whenever counter 2 (T2) value is equal to T2DR, T2O port toggles in 8/16-bit mode. Also, Timer 3 outputs the result T3O port in the timer mode. In addition, Timer 3 outputs PWM waveform through PWM3 in the PWM mode.

Table 9. Operating Modes of Timer

16BIT	CAP2	CAP3	PWM3E	T2CK[2:0]	T3CK[1:0]	T2/3_PE	Timer 2	Timer 3
0	0	0	0	XXX	XX	00	8-bit Timer	8-bit Timer
0	0	1	0	111	XX	00	8-bit Event Counter	8-bit Capture
0	1	0	0	XXX	XX	01	8-bit Capture	8-bit Compare Output
0	0	0	1	XXX	XX	11	8-bit Timer/Counter	10-bit PWM
1	0	0	0	XXX	11	00	16-bit Timer	
1	0	0	0	111	11	00	16-bit Event Counter	
1	1	1	0	XXX	11	00	16-bit Capture	
1	0	0	0	XXX	11	01	16-bit Compare Output	

11.2.1 8-bit timer/event counter mode block diagram

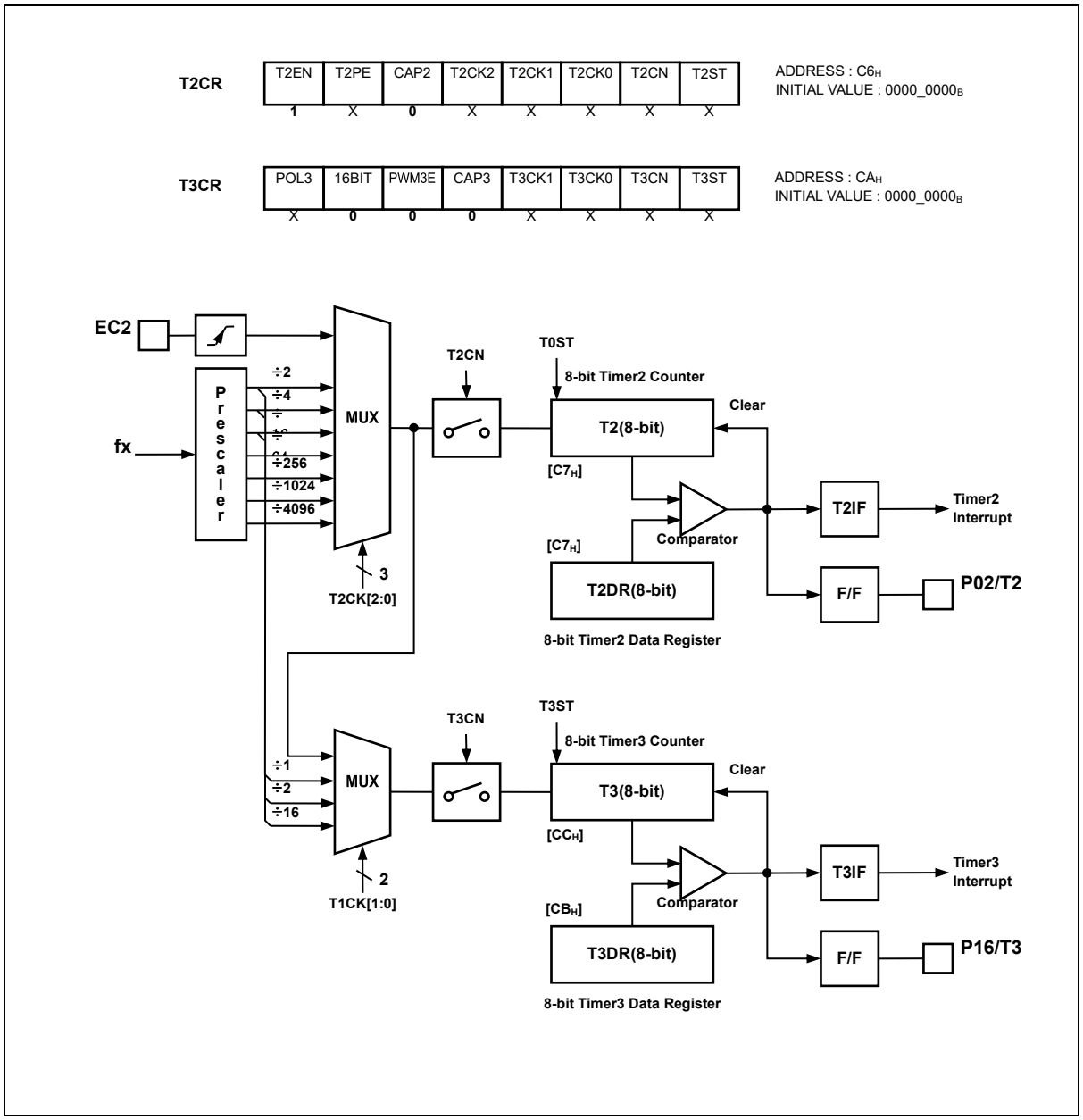


Figure 24. 8-bit Timer/Event Counter2, 3 Block Diagram

11.2.2 16-bit timer/counter mode block diagram

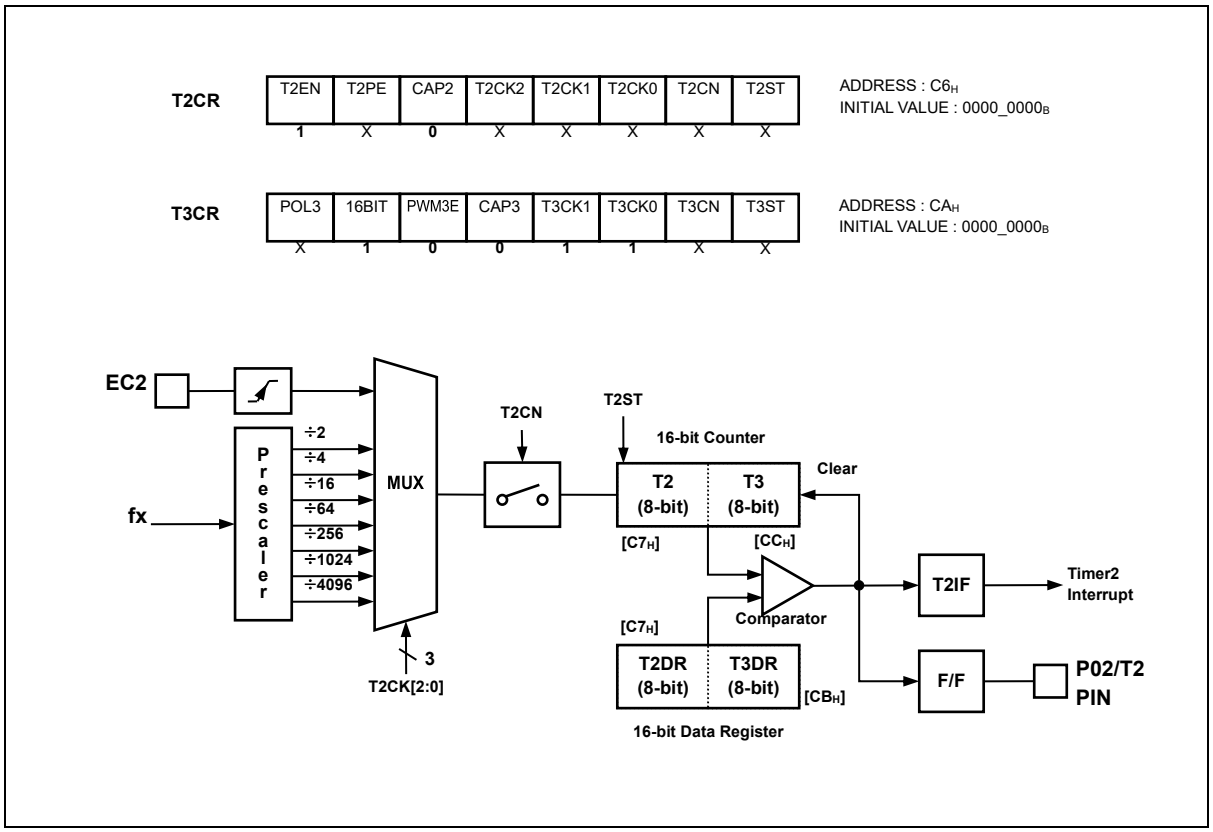


Figure 25. 16-bit Timer/Event Counter2, 3 Block Diagram

11.2.3 8-bit capture mode block diagram

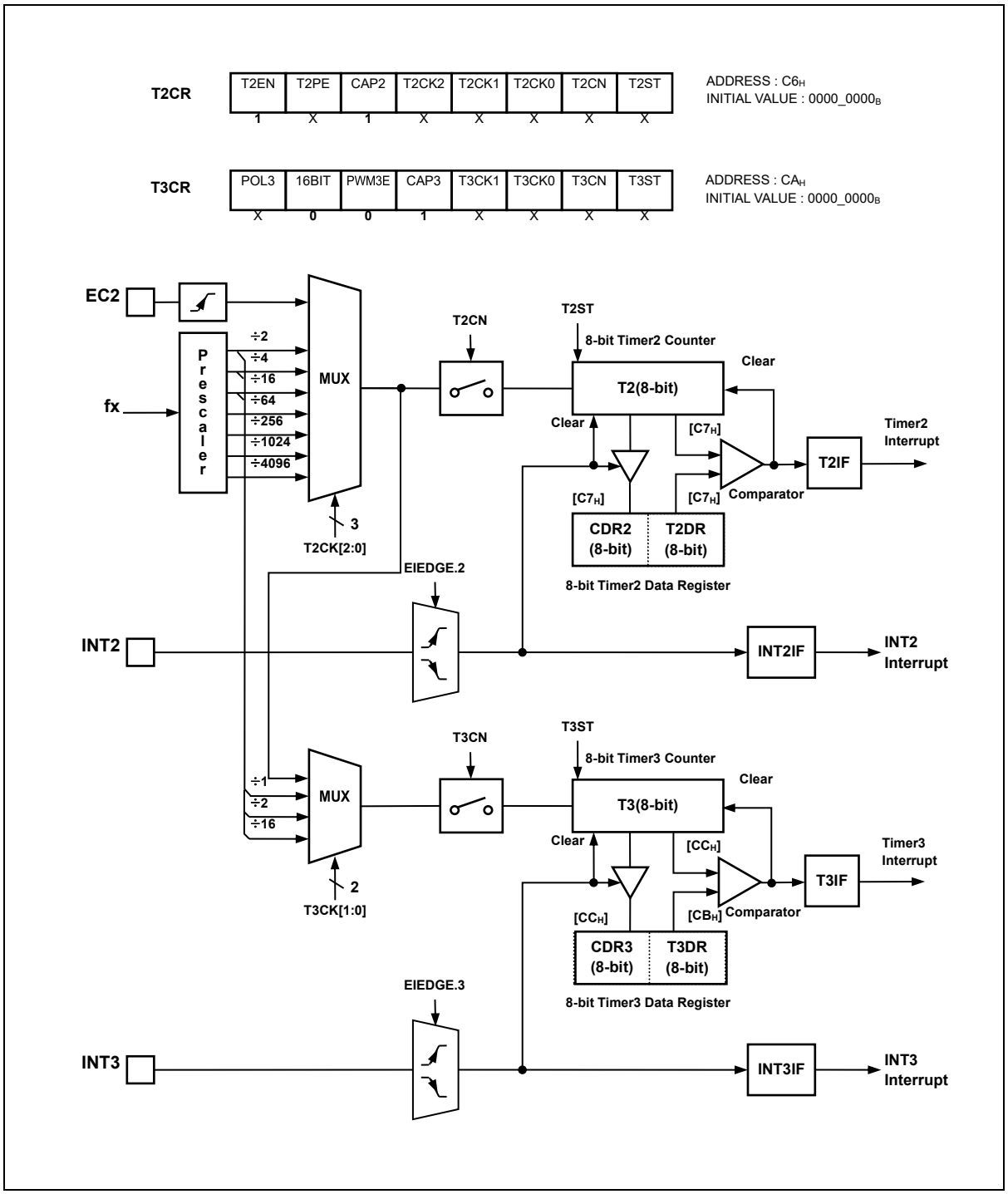


Figure 26. 8-bit Capture Mode for Timer2, 3

11.2.4 16-bit capture mode block diagram

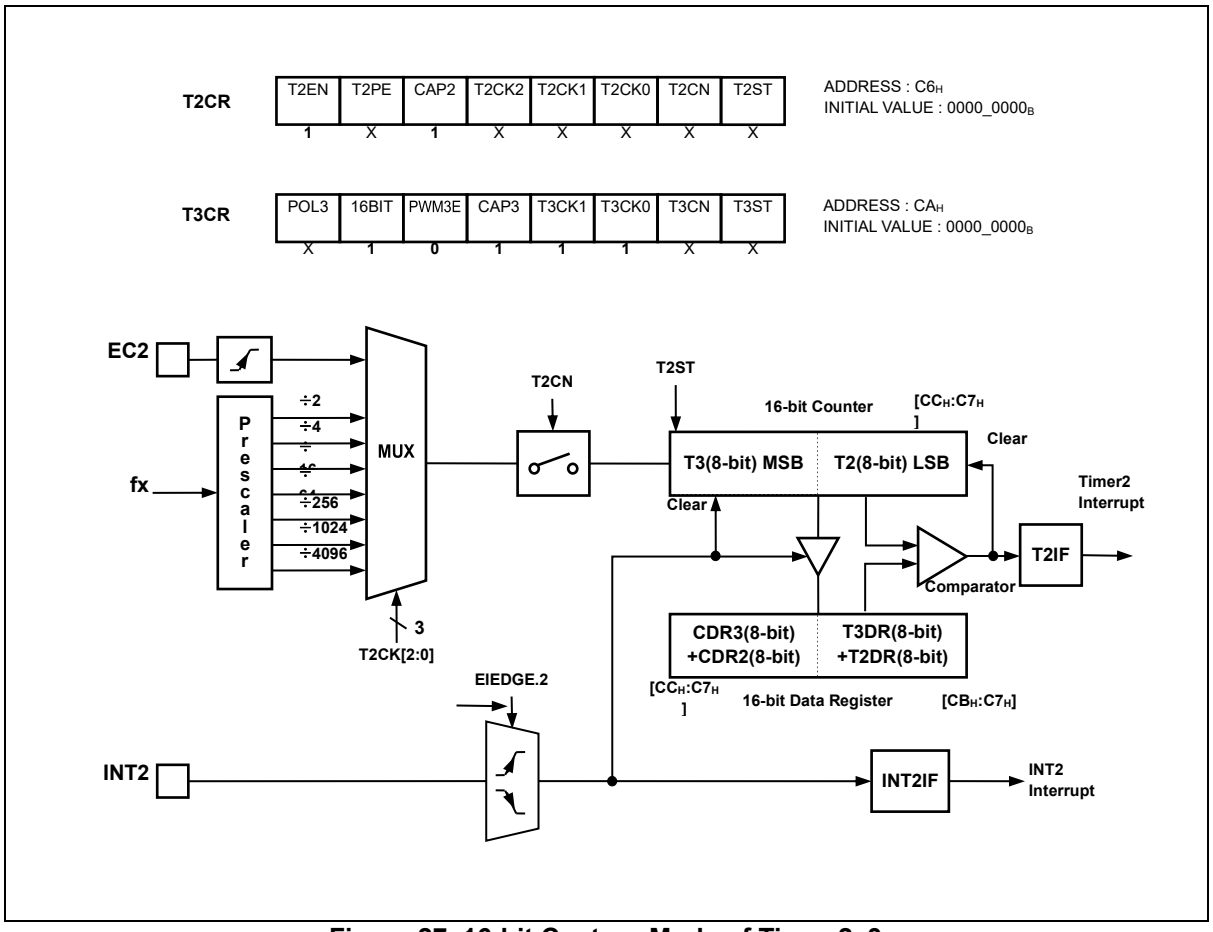


Figure 27. 16-bit Capture Mode of Timer 2, 3

11.2.5 PWM mode block diagram

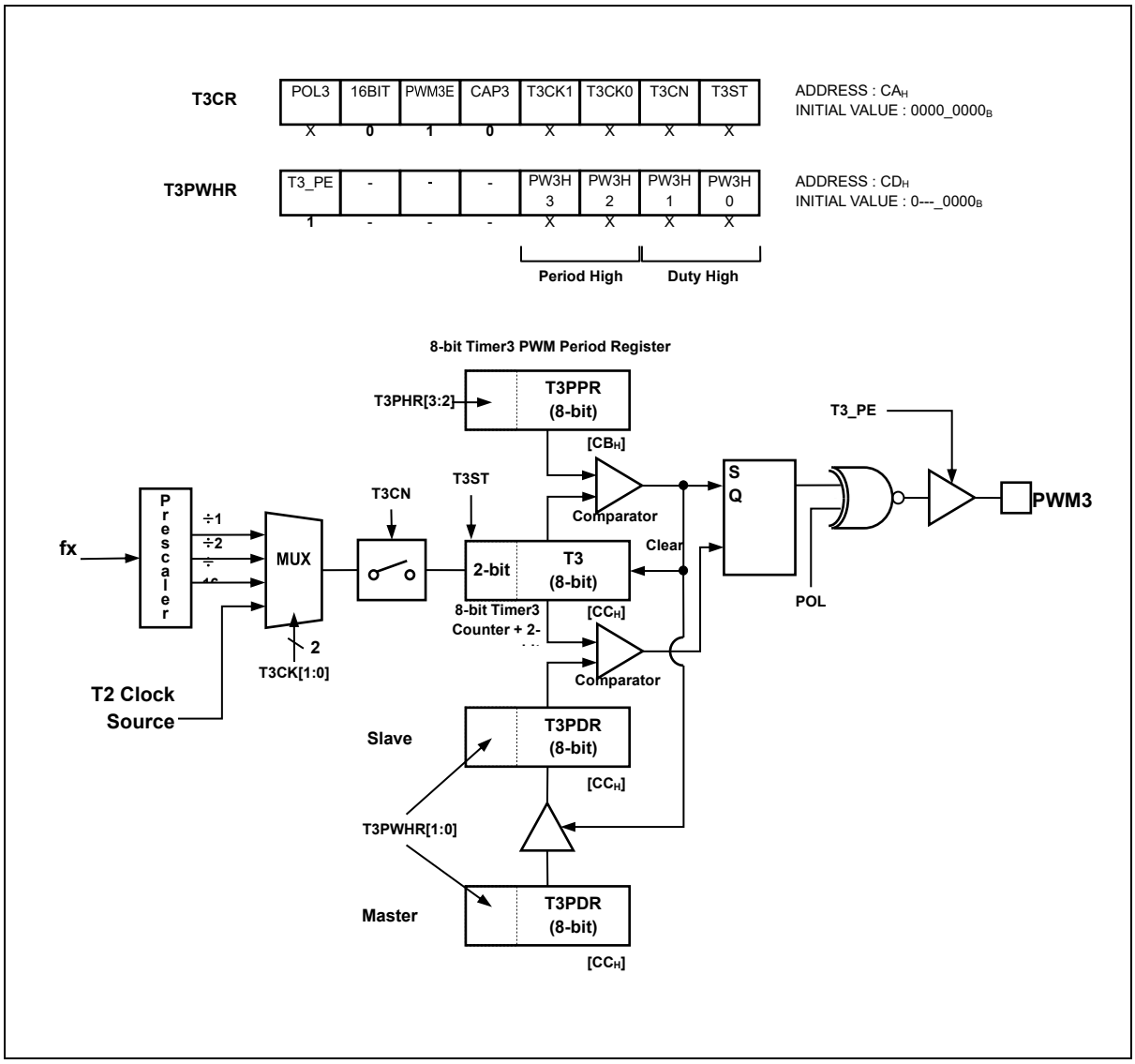


Figure 28. PWM Mode for Timer 3

11.3 16-bit timer 4

16-bit timer 4 consists of Multiplexer, Timer Data Register High/Low, Timer Register High/Low, Timer Mode Control Register. It is able to use internal 16-bit timer/ counter without a port output function.

The 16-bit timer 4 is able to use the divided clock of the main clock selected from pre-scalar output.

11.3.1 16-bit timer/counter 4 block diagram

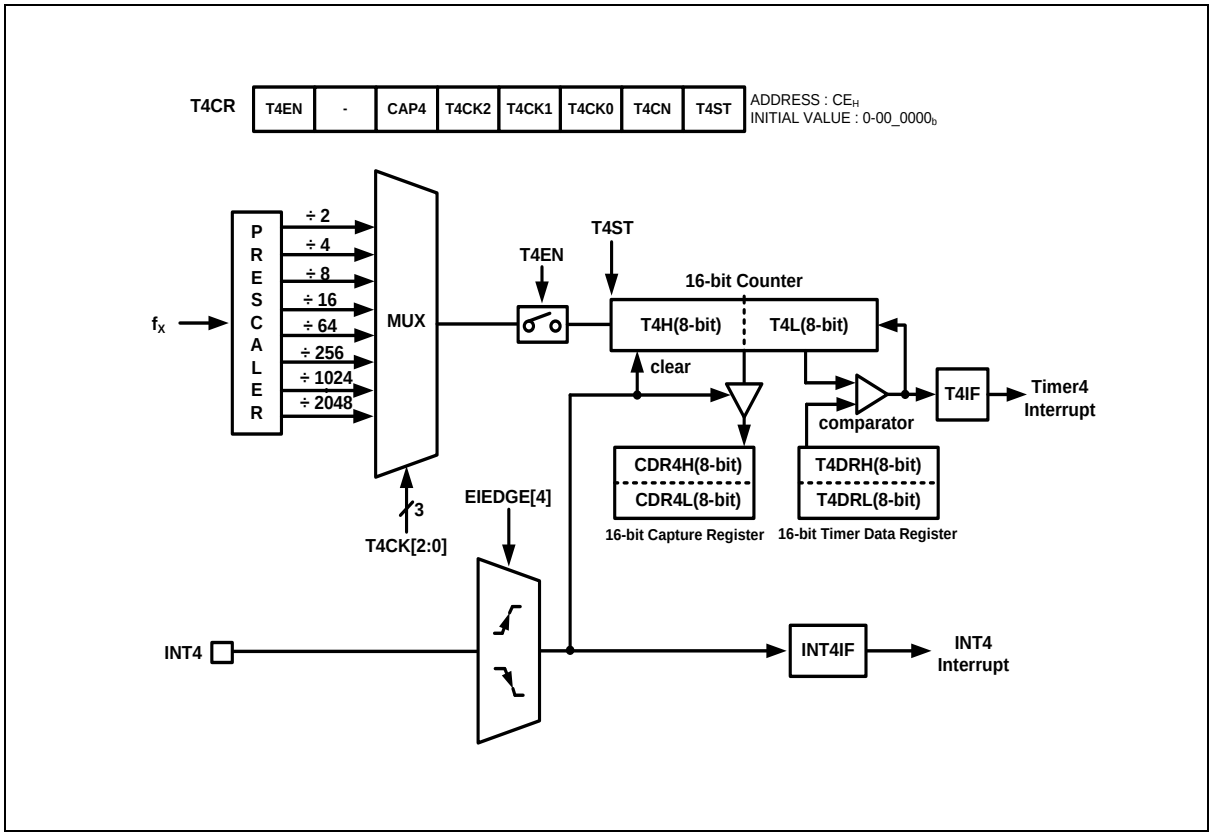


Figure 29. Timer4 16-bit Mode Block Diagram

12 Buzzer driver

The Buzzer consists of 6 bit counter, buzzer data register (BUZDR), and buzzer control register (BUZCR). The Square Wave is outputted through P12/BUZO pin. In buzzer data register BUZDR[5:0] controls the buzzer frequency and BUZDIV[1:0] selects fBUZ divided by DIV block. In buzzer control register (BUZCR), BUCK[2:0] selects source clock divided by prescaler

$$f_{BUZO} = \frac{f_{BUZ}}{2 \times BUZDIV \times (BUZDATA + 1)} (Hz)$$

Table 10. Buzzer Frequency at 1MHz

BUZDATA [5:0]	BUZDIV[1:0]			
	00 (fbuz/8)	01 (fbuz/16)	10 (fbuz/32)	11 (fbuz/64)
0	62.500	31.250	15.625	7.813
1	31.250	15.625	7.813	3.906
2	20.833	10.417	5.208	2.604
3	15.625	7.813	3.906	1.953
4	12.500	6.250	3.125	1.563
5	10.417	5.208	2.604	1.302
6	8.929	4.464	2.232	1.116
7	7.813	3.906	1.953	0.977
8	6.944	3.472	1.736	0.868
9	6.250	3.125	1.563	0.781
10	5.682	2.841	1.420	0.710
11	5.208	2.604	1.302	0.651
12	4.808	2.404	1.202	0.601
13	4.464	2.232	1.116	0.558
14	4.167	2.083	1.042	0.521
15	3.906	1.953	0.977	0.488
16	3.676	1.838	0.919	0.460
17	3.472	1.736	0.868	0.434
18	3.289	1.645	0.822	0.411
19	3.125	1.563	0.781	0.391
20	2.976	1.488	0.744	0.372
21	2.841	1.420	0.710	0.355
22	2.717	1.359	0.679	0.340
23	2.604	1.302	0.651	0.326
24	2.500	1.250	0.625	0.313
25	2.404	1.202	0.601	0.300
26	2.315	1.157	0.579	0.289
27	2.232	1.116	0.558	0.279
28	2.155	1.078	0.539	0.269
29	2.083	1.042	0.521	0.260
30	2.016	1.008	0.504	0.252
31	1.953	0.977	0.488	0.244

BUZDATA [5:0]	BUZDIV[1:0]			
	00 (fbuz/8)	01 (fbuz/16)	10 (fbuz/32)	11 (fbuz/64)
32	1.894	0.947	0.473	0.237
33	1.838	0.919	0.460	0.230
34	1.786	0.893	0.446	0.223
35	1.736	0.868	0.434	0.217
36	1.689	0.845	0.422	0.211
37	1.645	0.822	0.411	0.206
38	1.603	0.801	0.401	0.200
39	1.563	0.781	0.391	0.195
40	1.524	0.762	0.381	0.191
41	1.488	0.744	0.372	0.186
42	1.453	0.727	0.363	0.182
43	1.420	0.710	0.355	0.178
44	1.389	0.694	0.347	0.174
45	1.359	0.679	0.340	0.170
46	1.330	0.665	0.332	0.166
47	1.302	0.651	0.326	0.163
48	1.276	0.638	0.319	0.159
49	1.250	0.625	0.313	0.156
50	1.225	0.613	0.306	0.153
51	1.202	0.601	0.300	0.150
52	1.179	0.590	0.295	0.147
53	1.157	0.579	0.289	0.145
54	1.136	0.568	0.284	0.142
55	1.116	0.558	0.279	0.140
56	1.096	0.548	0.274	0.137
57	1.078	0.539	0.269	0.135
58	1.059	0.530	0.265	0.132
59	1.042	0.521	0.260	0.130
60	1.025	0.512	0.256	0.128
61	1.008	0.504	0.252	0.126
62	0.992	0.496	0.248	0.124
63	0.977	0.488	0.244	0.122

12.1 Buzzer driver block diagram

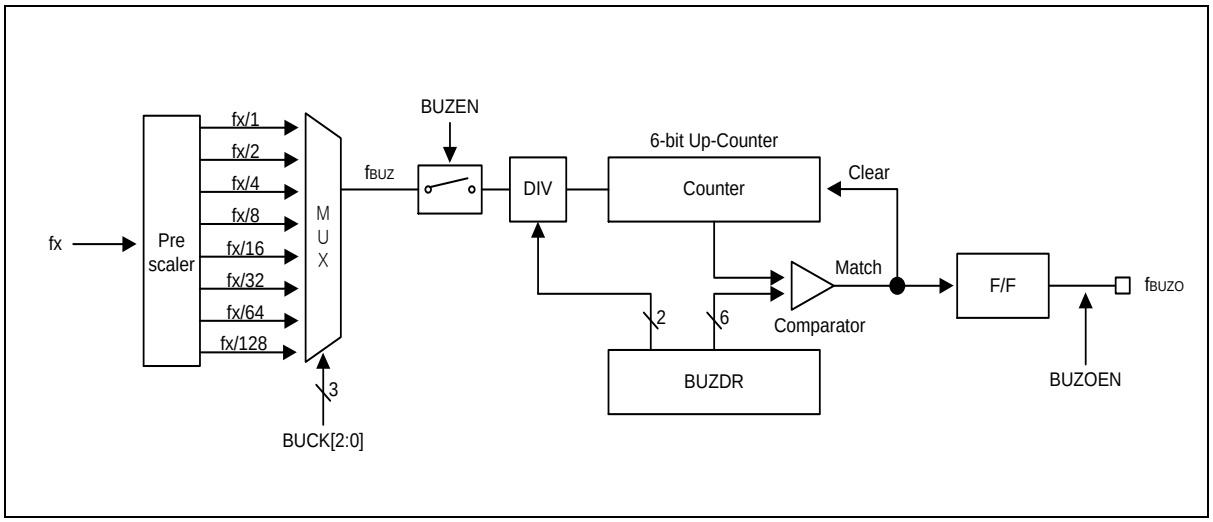


Figure 30. Buzzer Driver Block Diagram

13 12-bit ADC

Analog-to-digital converter (ADC) of MC97FG316/MC97FG216 allows conversion of an analog input signal to corresponding 12-bit digital value. This A/D module has tenth analog inputs. Output of the multiplexer becomes input into the converter which generates the result through successive approximation.

The A/D module has four registers which are the control register ADCM (A/D Converter Mode Register), ADCM2 (A/D Converter Mode Register 2) and A/D result register ADCRH (A/D Converter Result High Register) and ADCRL (A/D Converter Result Low Register).

It is selected for the corresponding channel to be converted by setting ADSEL[3:0]. To executing A/D conversion, ADST bit sets to '1'. The register ADCRH and ADCRL contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCHR and ADCRL, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. For processing A/D conversion, AFLAG bit is read as '0'. If using STBY (power down) bit, the ADC is disabled. Also internal timer, external generating event, comparator, the trigger of timer1pwm and etc. can start ADC regardless of interrupt occurrence.

ADC Conversion Time = ADCLK * 60 cycles

After STBY bit is reset (ADC power enable) and it is restarted, during some cycle, ADC conversion value may have an inaccurate value.

13.1 12-bit ADC block diagram

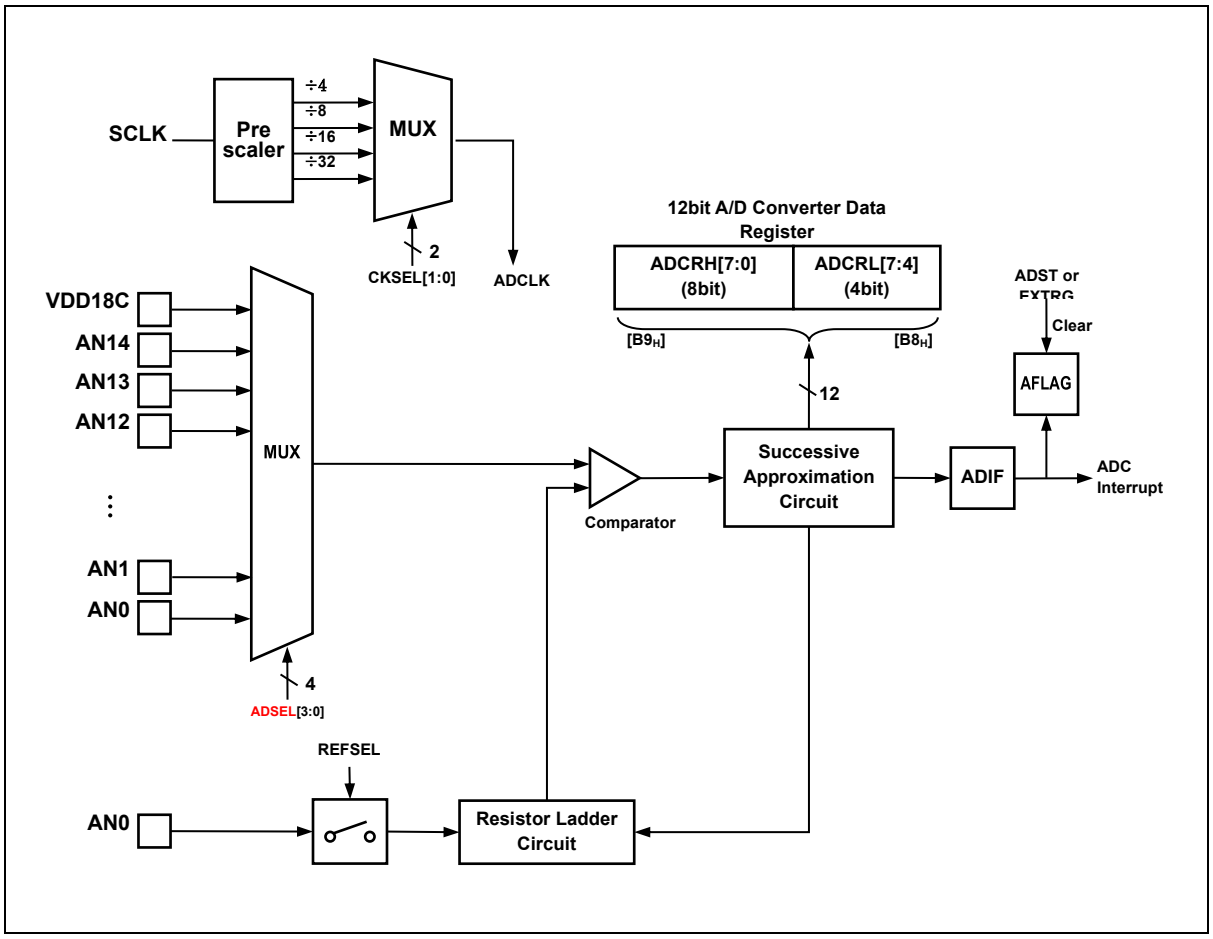


Figure 31. ADC Block Diagram

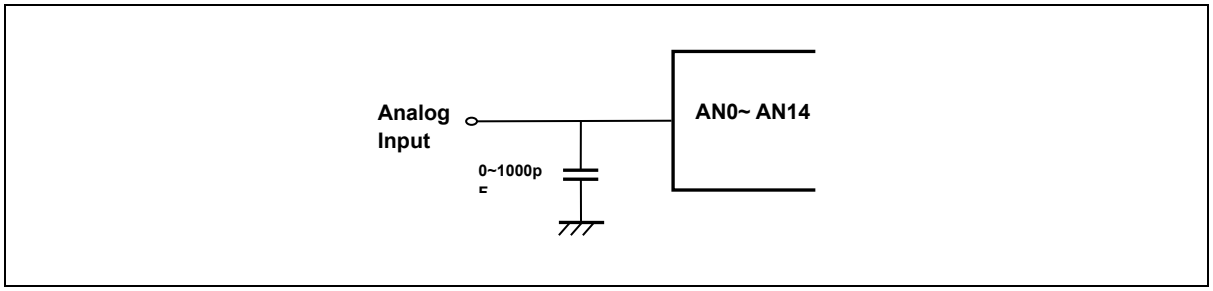


Figure 32. A/D Analog Input Pin Connecting Capacitor

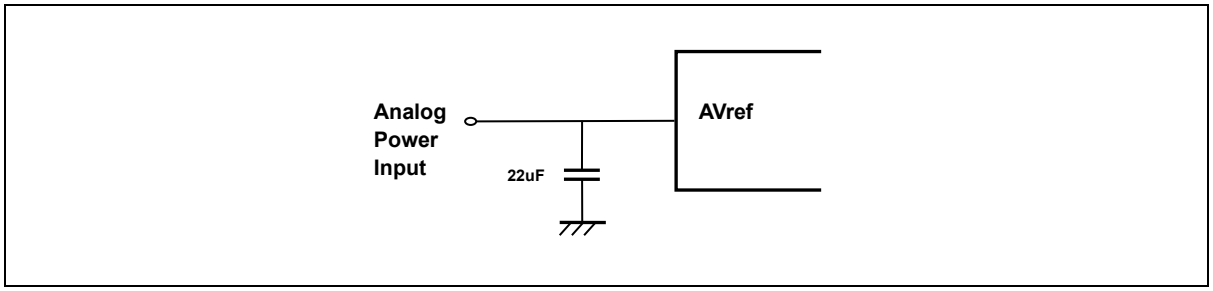


Figure 33. AVref Pin Connecting Capacitor

14 Analog comparator

The Analog Comparator compares the input values on the positive pin AC+ and the negative pin AC-. When the voltage on the positive pin AC+ is higher than the voltage on the negative pin AC-, the Analog Comparator output, ACOUT, is set.

14.1 Analog comparator block diagram

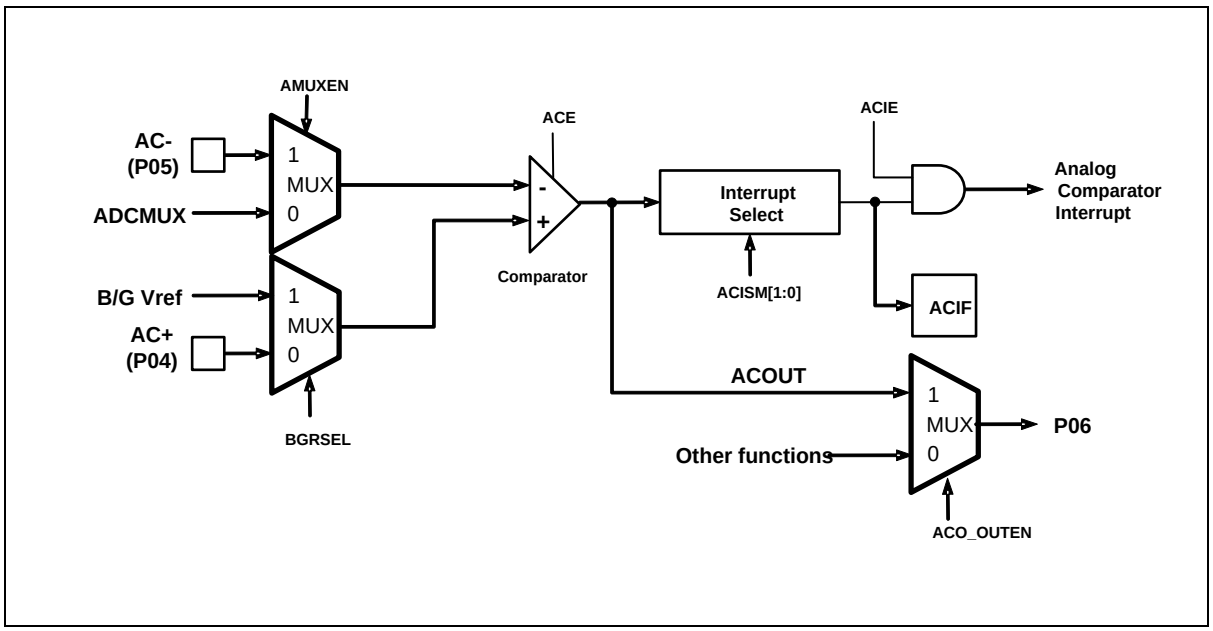


Figure 34. Analog Comparator Block Diagram

15 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. USART of MC97FG316/MC97FG216 features the followings:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

USART has three main parts such as a Clock Generator, Transmitter and Receiver. The Clock Generation logic consists of synchronization logic for external clock input used by synchronous or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

Receiver is the most complex part of the USART module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATAx) and control logic. Receiver supports the same frame formats as Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

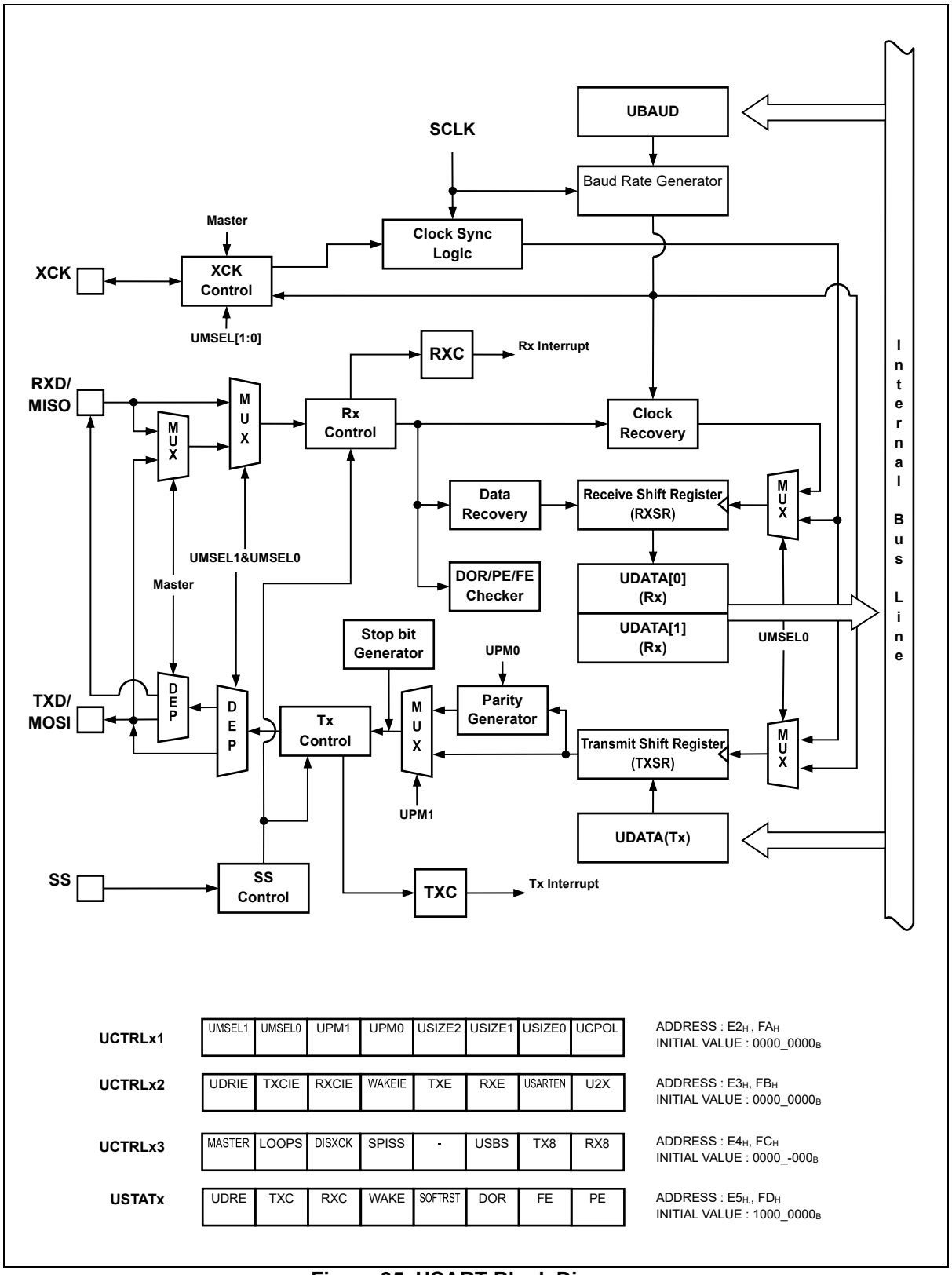
USART can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

- Full duplex, three-wire synchronous data transfer
- Master or Slave operation
- Supports all four SPI modes of operation (mode0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (UMSEL[1:0]=3), the Slave Select (SS) pin becomes active low input in slave mode operation, or can be output in master mode operation if SPISS bit is set.

Note that during SPI mode of operation, the pin RXD is renamed as MISO and TXD is renamed as MOSI for compatibility to other SPI devices.

15.1 USART block diagram



UCTRLx1	UMSEL1	UMSEL0	UPM1	UPM0	USIZE2	USIZE1	USIZE0	UCPOL
UCTRLx2	UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	USARTEN	U2X
UCTRLx3	MASTER	LOOPS	DISXCK	SPISS	-	USBS	TX8	RX8
USTATx	UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE

ADDRESS : $E2_H$, FA_H
INITIAL VALUE : 0000_0000_B

ADDRESS : $E3_H$, FB_H
INITIAL VALUE : 0000_0000_B

ADDRESS : $E4_H$, FC_H
INITIAL VALUE : 0000_-000_B

ADDRESS : $E5_H$., FD_H
INITIAL VALUE : 1000_0000_B

Figure 35. USART Block Diagram

16 SPI

There is Serial Peripheral Interface (SPI) one channel in MC97FG316. The SPI allows synchronous serial data transfer between the external serial devices. It can do Full-duplex communication by 4-wire (MOSI, MISO, SCK, SS), support Master/Slave mode, can select serial clock (SCK) polarity, phase and whether LSB first data transfer or MSB first data transfer.

16.1 SPI block diagram

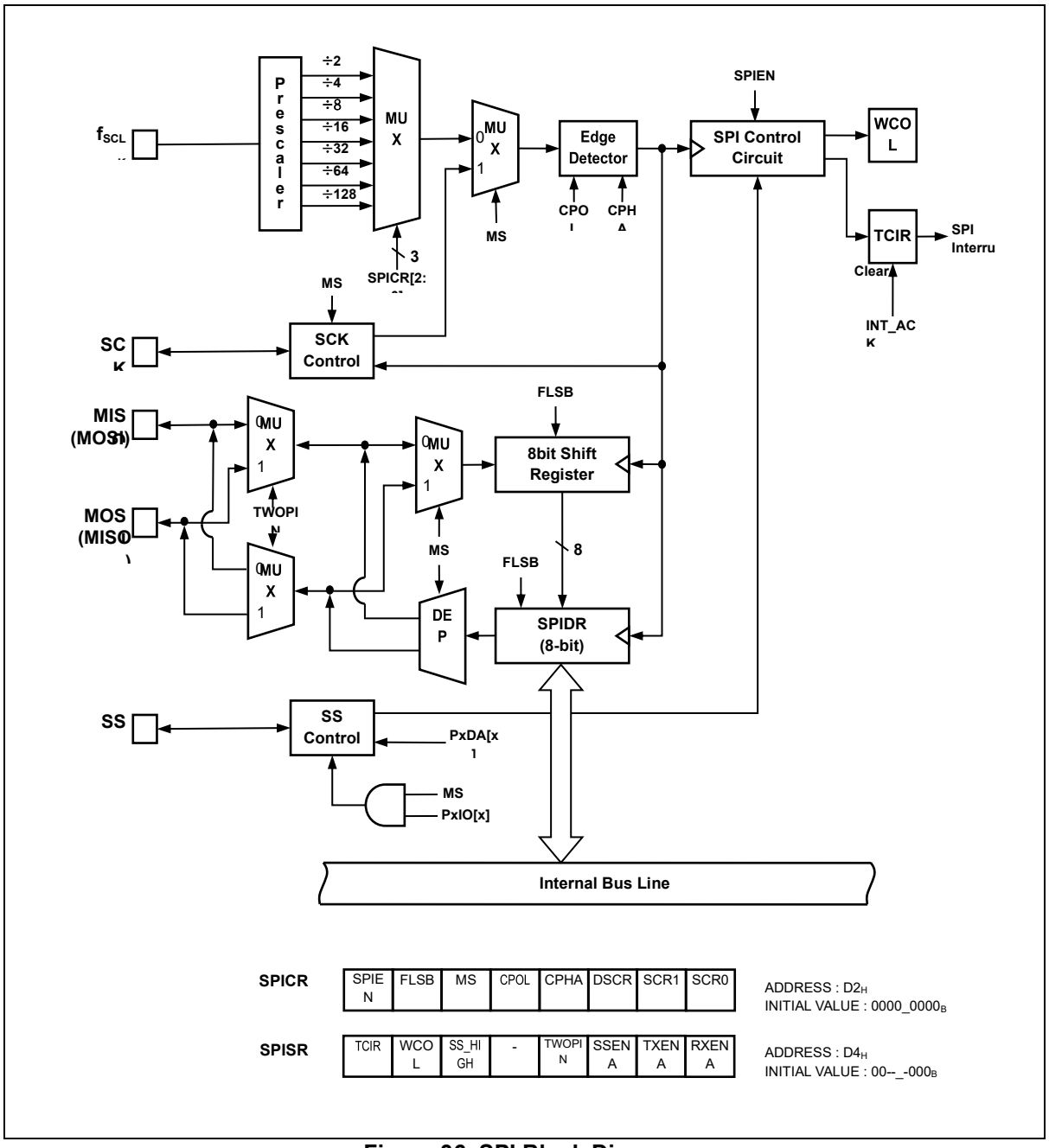


Figure 36. SPI Block Diagram

17 I2C

The I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer speed
- 7-bit address
- Support two slave addresses
- Both master and slave operation
- Bus busy detection

17.1 I2C block diagram

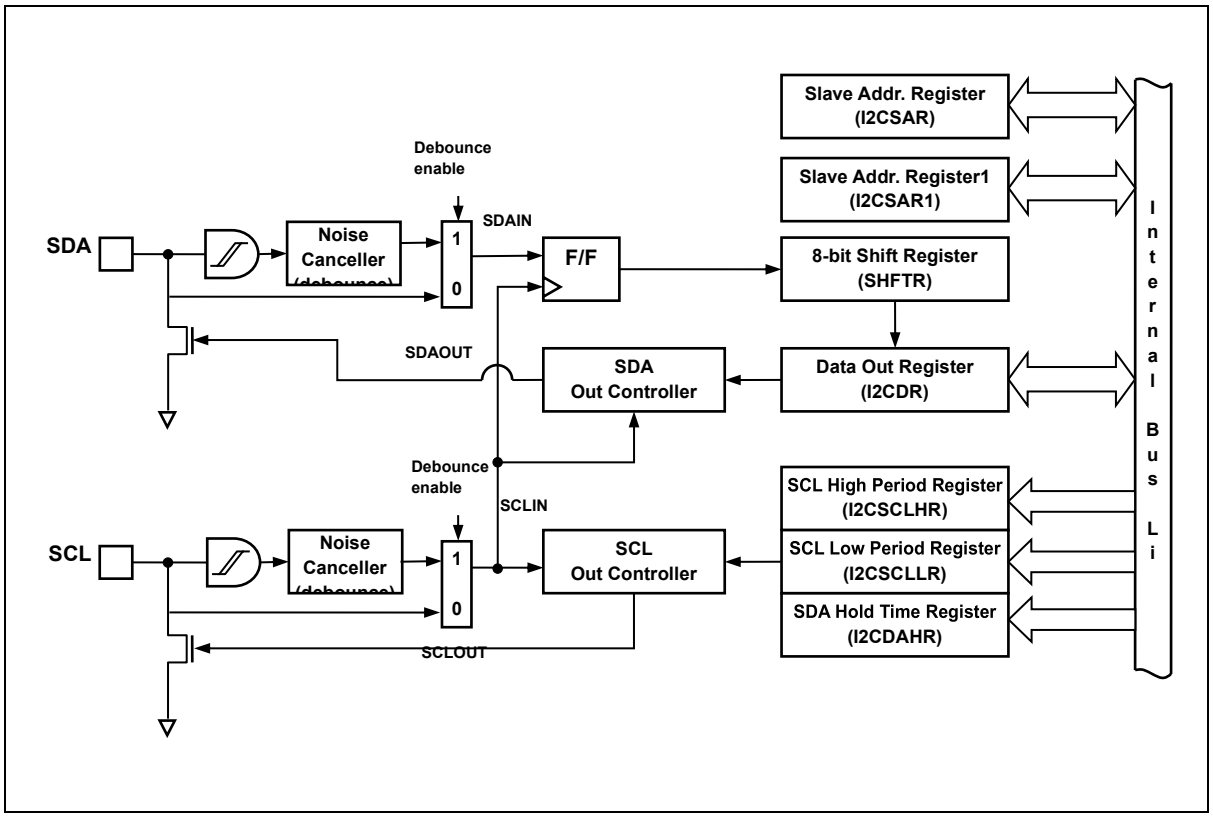


Figure 37. I2C Block Diagram

18 Power down operation

MC97FG316/MC97FG216 has three power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. MC97FG316/MC97FG216 provides three kinds of power saving functions, IDLE, STOP1 and STOP2 mode. In three modes, program is stopped.

18.1 Peripheral operation in IDLE/STOP mode

Table 11. Peripheral Operation during Power down Mode

Peripheral	IDLE mode	STOP1 mode	STOP2 mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain	Retain
Basic Interval Timer	Operates Continuously	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Operates Continuously	Stop
Watch Timer	Operates Continuously	Stop (Only operate in sub clock mode)	Stop (Only operate in sub clock mode)
TimerP0~4	Operates Continuously	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)
ADC	Operates Continuously	Stop	Stop
BUZ	Operates Continuously	Stop	Stop
SPI/SCI	Operates Continuously	Only operate with external clock	Only operate with external clock
I2C	Operates Continuously	Stop	Stop
Internal OSC (16MHz)	Oscillation	Stop	Stop
Main OSC (1~12MHz)	Oscillation	Stop	Stop
Sub OSC (32.768kHz)	Oscillation	Oscillation	Oscillation
Internal RCOSC (125kHz)	Oscillation	Oscillation	Stop
I/O Port	Retain	Retain	Retain
Control Register	Retain	Retain	Retain
Address Data Bus	Retain	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC2), SIO (External clock), External Interrupt, UART by ACK PCI, I2C (slave mode), WT (sub clock), AC, WDT, BIT	By RESET, Timer Interrupt (EC0, EC2), SIO (External clock), External Interrupt, UART by ACK PCI, I2C (slave mode), WT (sub clock), AC

19 Reset

MC97FG316 has reset by external RESETB pin. The following is the hardware setting value.

Table 12. Reset State

On chip hardware	Initial value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Peripheral Registers refer
Brown-Out Detector	Enable

MC97FG316/MC97FG216 has five types of reset sources as shown in the following.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- LVR Reset (In the case of LVREN = `1 `)
- OCD Reset

19.1 Reset block diagram

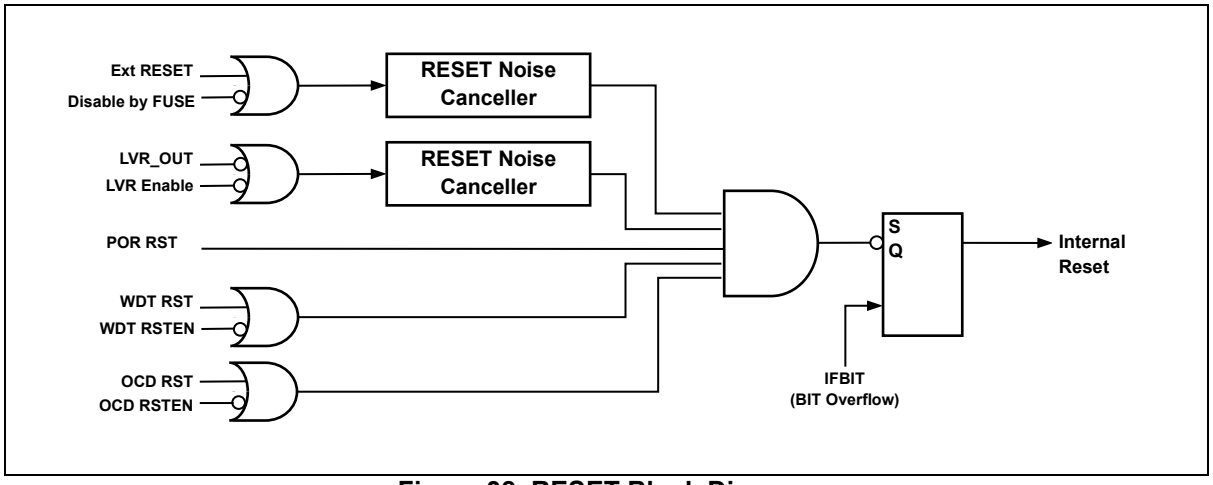


Figure 38. RESET Block Diagram

20 Memory programming

MC97FG316 incorporates flash and data EEPROM memory to which a program can be written, erased, and overwritten while mounted on the board. Also, data EEPROM can be programmed or erased in user program. Flash area can be programmed in only OCD II or parallel ROM mode.

Serial ISP modes and byte-parallel ROM writer mode are supported.

Flash of MC97FG316/MC97FG216 features the followings:

- Flash Size : 16Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
- Up to 300,000 program/erase cycles at typical voltage and temperature for data EEPROM memory
- Security feature

20.1 Memory map

20.1.1 Flash memory map

Program memory uses 16-Kbyte of Flash memory. It is read by byte and written by byte or page. One page is 32-byte

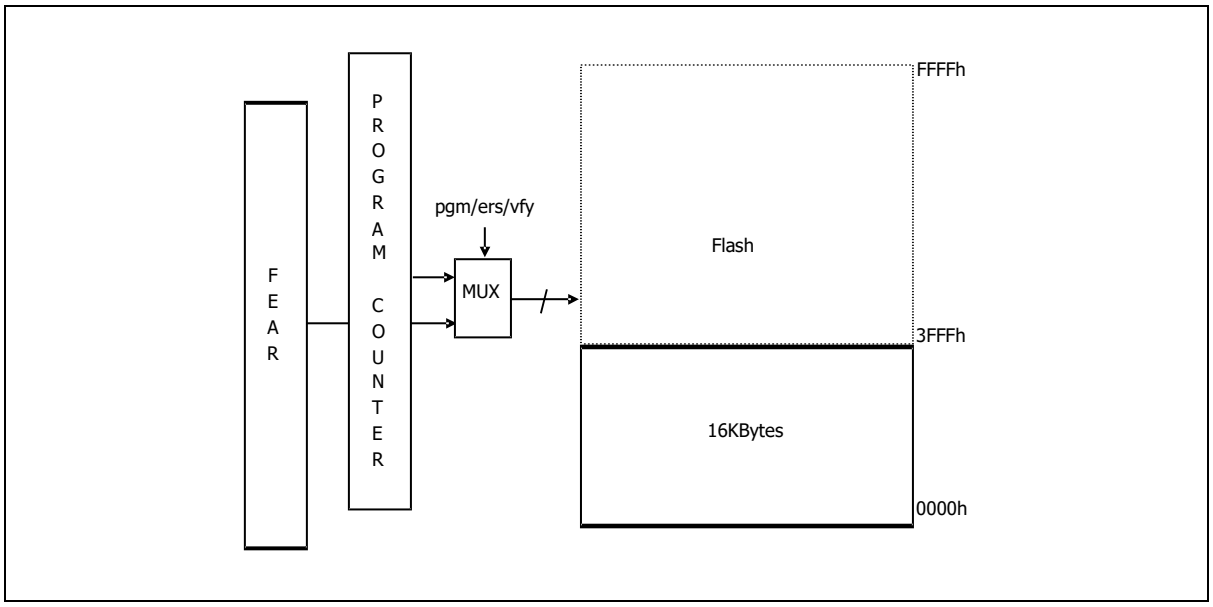


Figure 39. Flash Memory Map

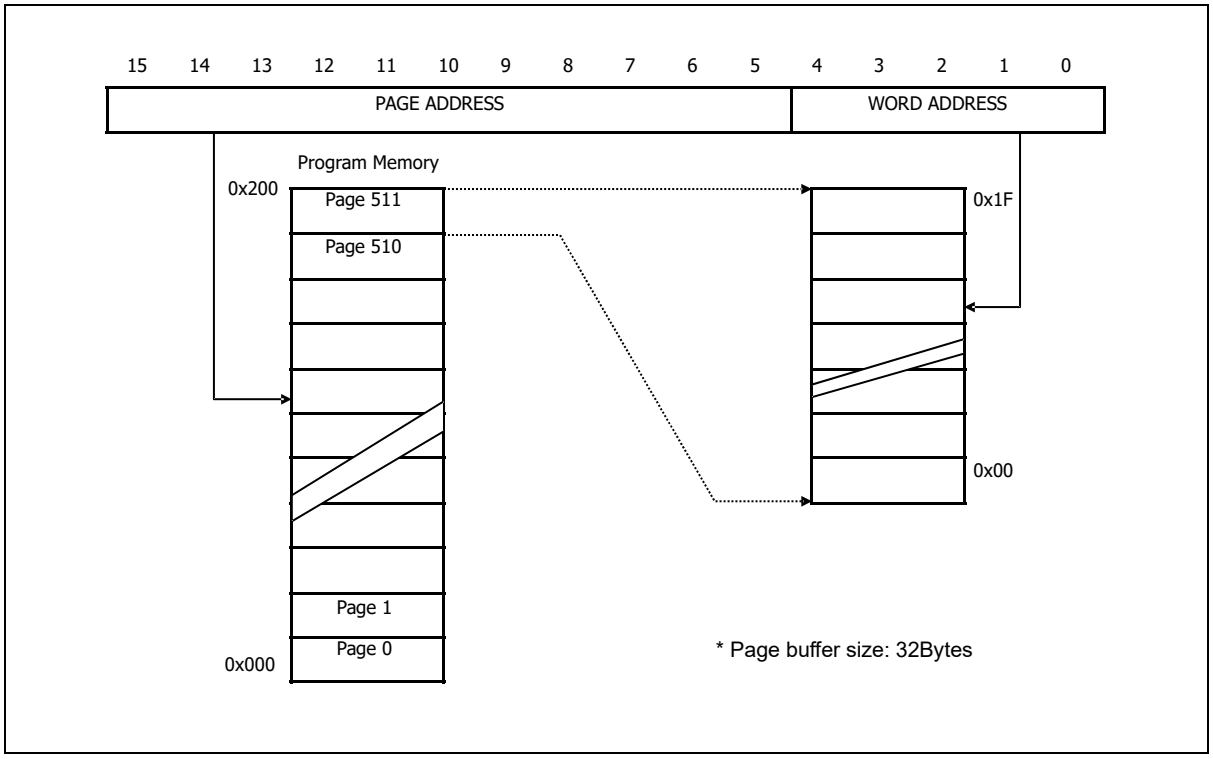


Figure 40. Address Configuration of Flash Memory

20.1.2 Data EEPROM memory map

Data EEPROM memory uses 512-byte of EEPROM. It is read by byte and written by byte or page. One page is 16-byte. It is mapped to external data memory of 8051

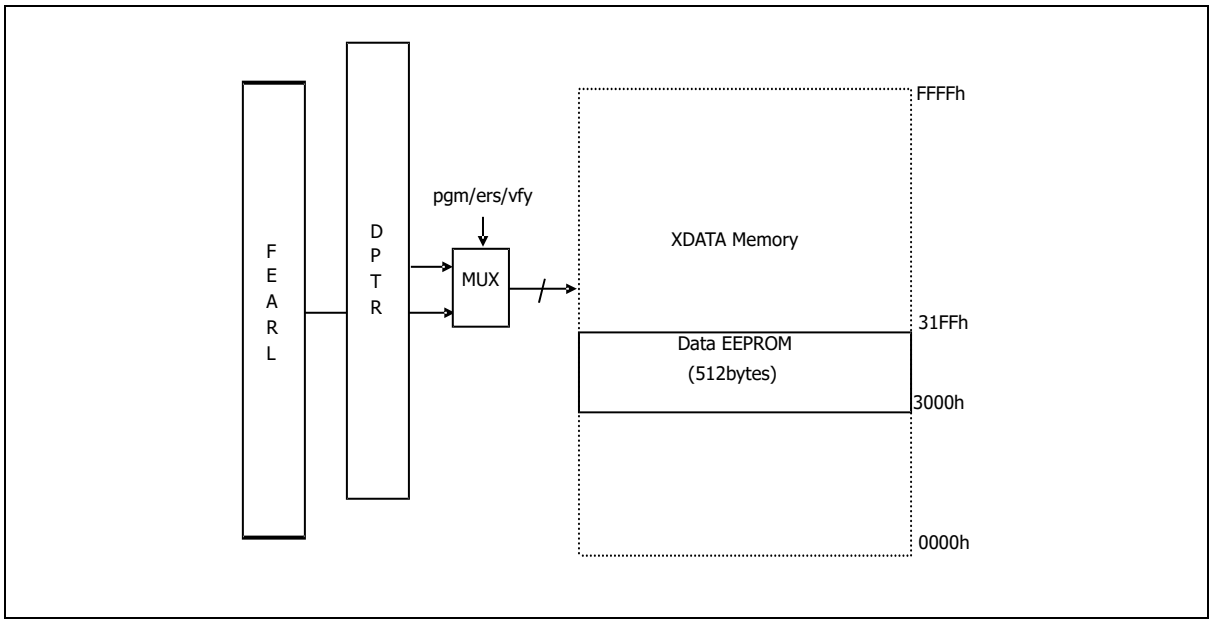


Figure 41. Data EEPROM Memory Map

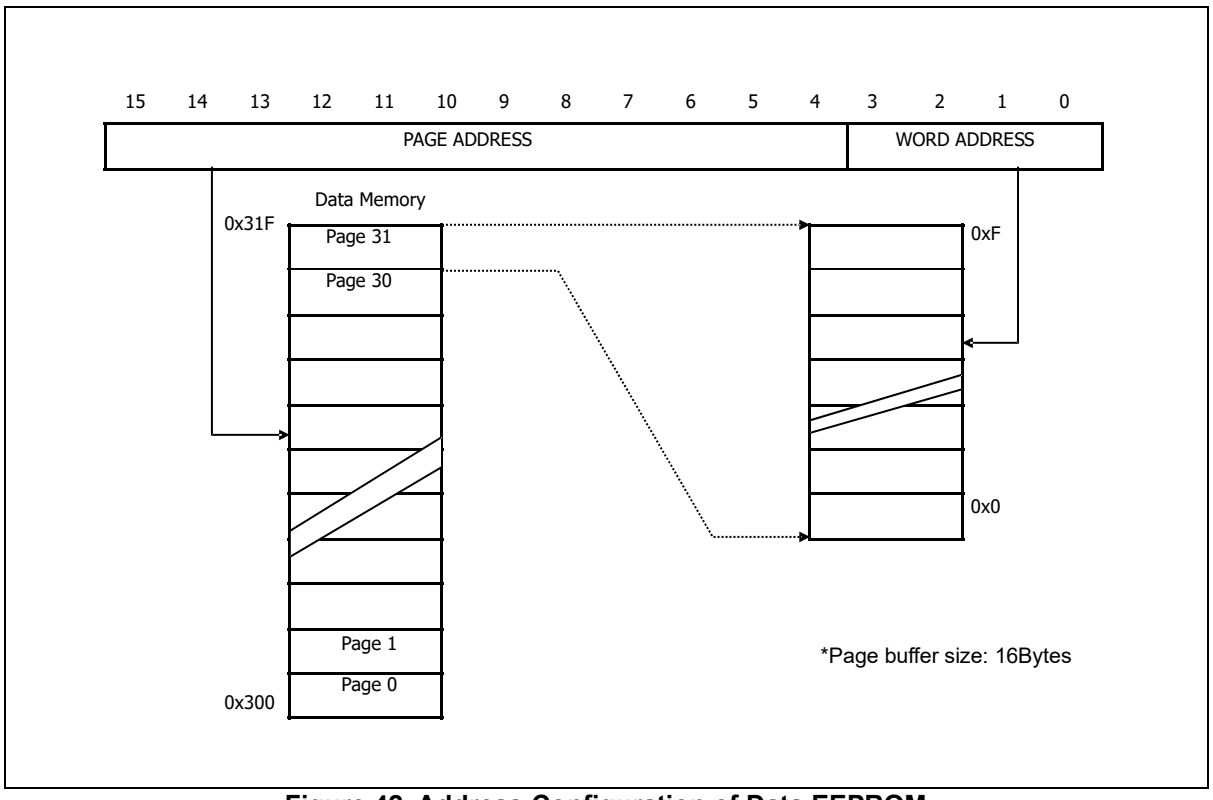


Figure 42. Address Configuration of Data EEPROM

20.2 Configure option

For the configure option control, corresponding data should be written in the configure option area by programmer (writer tools). Also, the value of configure option can be read at address 0x4000.

Because the configure option is very important for MCU operation, it is recommended to write configure option again in user program for enhancing MCU operation stability.

20.2.1 How to write the configure option in user program

To reapply the configure value to be written by programmer (writer tool)

```
#define coderom ((unsigned char volatile code *) 0)
#define FUSE_CONF *(volatile unsigned char xdata *) 0x2F50
void main(void)
{
    FUSE_CONF=coderom[0x4000];    //To reapply the value of CONFIG OPTION
   …
}
```

To write the configure value directly in user program

```
#define coderom ((unsigned char volatile code *) 0)
#define FUSE_CONF *(volatile unsigned char xdata *) 0x2F50
void main(void)
{
   FUSE_CONF=0x??;    //The value(??) is decided by setting of FUSE_CONF
   …
}
```

21 Electrical characteristics

21.1 Absolute maximum ratings

Table 13. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	**VDD**	-0.3~+6.5	V	–
Normal voltage pin	**V_I**	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	30	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	160	mA	Maximum current ($\sum I_{OL}$)
Total power dissipation	**P_T**	400	mW	–
Storage temperature	**T_{STG}**	-65~+150	°C	–

NOTE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

21.2 Recommended operating conditions

Table 14. Recommended Operating Conditions

(TA=-40°C ~ +85°C or TA=-40°C ~ +105°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating voltage	**VDD**	f_X= 1, 4, 8, 16MHz	Internal RC	1.8	–	5.5	V
		f_X= 4~ 16MHz	X-tal				
		f_X= 32.768kHz	Sub crystal				
		f_X= 1kHz	Internal Ring OSC				
Operating temperature	**T_{OPR}**	VDD=1.8~5.5V		-40	–	85	°C
				-40	–	105	

21.3 A/D converter characteristics

Table 15. A/D Converter Characteristics

(TA=-40°C ~ +85°C or T_A=-40°C ~ +105°C, VDD=AVDD=2.7V ~ 5.5V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
A/D converting Resolution	-	-	-	12	-	bits
Integral non-linearity	INL	Vref=5.12V, Vss=0V, TA=+25℃	-	-	±3	LSB
Differential non-linearity	DNL		-	-	±2	
Zero Offset Error	ZOE		-	±1	±3	
Overall Accuracy	OA		-	±3	-	
Conversion time	t_{CONV}	-	-	60	-	Cycle
Analog input voltage	V_{AIN}	-	VSS	-	Vref	V
Analog reference voltage	AVREF	(note)	2.7	-	5.5	V
Analog input current	I_{AIN}	VDD=Vref=5V	-	-	10	uA
Analog block current	I_{AVDD}	VDD=Vref=5V VDD=Vref=3V	-	1 0.5	3 1.5	mA
		VDD=Vref=5V Power down mode	-	100	500	nA

NOTES:

1. When analog reference is lower than 2.7V, the ADC resolution becomes worse.
2. ADC clock should be used below 3MHz. If the Analog Reference Voltage is low, the A/D clock speed should also be slow.

21.4 Analog comparator characteristics

Table 16. Analog Comparator Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Leakage Current	I_L	VDDEXT=5V, Vin=1/2VDDEXT	-50	-	50	nA
Input Offset Voltage	V_{offset}	VDDEXT=5V, Vin=1/2VDD	±10	-	±40	mV
Operating Current	I_{OP}	COMP_EN=H	-	30	-	uA
Power Down Current	I_{PD}	COMP_EN=L	-	1	-	uA
Response Time	VRT	CL= 50pF, VDDEXT=5V	-	-	1	us
BGR	-	VDD=4V, T_A=+25°C	-	1.174	-	V

21.5 Power-on reset characteristics

Table 17. Power-On Reset Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ +105°C, VDD=1.8 ~ 5.5V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
RESET release level	V_{POR}	-	1.3	1.4	1.5	V
RESET release level	t_R	-	0.05	-	5	V/ms
POR current	I_{POR}	-	-	-	10	uA

21.6 Low voltage reset characteristics

Table 18. LVR Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ +105°C, VDD=1.8 ~ 5.5V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating voltage	V_{OP}	-	VSS	-	5.5	V
Detection level	V_{LVR}	-	4.0	4.2V	4.4	V
		-	3.4	3.6V	3.8	V
		-	2.3	2.5V	2.7	V
		-	1.4	1.6V	1.8	V
Hysteresis	△V	-	-	20	-	mV
Operating Current	I_{LVR}	Enable	-	-	50	uA
		Disable	-	-	1	uA

21.7 Internal RC oscillator characteristics

Table 19. Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ +105°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 1.8 ~ 5.5V		15.52	16	16.48	MHz
Tolerance	–	T_A = 0°C to 50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -20°C to +85°C				±2.5	
		T_A = -40°C to +85°C				±3.0	
		T_A = -40°C to +105°C				±5.0	
Stabilization time	T_{HFS}	–		–	10	-	ms
Operating current	I_{IRC}	Enable		–	200	–	uA
		Disable		–	–	1	uA

21.8 Ring-oscillator characteristics

Table 20. Ring-Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ +105°C, VDD=1.8 ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{RING}	V_{DD} = 1.8 ~ 5.5V		0.8	1	1.2	MHz
Tolerance	-	T_A = -40°C to +85°C	With 0.1uF Bypass capacitor	-	-	±20	%
		T_A=-40°C to +105°C				±30	
Stabilization time	T_{HFS}	–		–		TBD	ms
IRC current	I_{RING}	Enable		–	10	–	uA
		Disable		-	-	1	uA

21.9 PLL characteristics

Table 21. PLL Characteristics

(TA = 0°C ~ +70°C, VDD18 = 1.6V ~ 2.0V, VSS = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PLL current	I_{PLL}	-	-	1.2	-	mA
Input clock frequency	f_{xin}	-	2	4	16	MHz
Output clock frequency	f_{out}	-	6.25	64	128	MHz
Output clock duty	TOD	-	40	-	60	%
Setting time	t_D	-	-	-	0.5	ms
Accuracy (Jitter)	-	Peak to peak	-	-	500	ps

21.10 DC characteristics

Table 22. DC Characteristics

(VDD =2.7~5.5V, VSS =0V, INTOSC=16.0MHz, T_A=-40~+85°C or T_A=-40°C ~ +105°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input low voltage	V_{IL1}	P2[2]	-0.5	-	0.2VDD	V
	V_{IL2}	All others PAD	-0.5	-	0.2VDD	V
Input high voltage	V_{IH1}	P2[2]	0.8VDD	-	VDD	V
	V_{IH2}	All others PAD	0.7VDD	-	VDD	V
Output low voltage	V_{OL1}	ALL I/O (IOL=20mA, VDD=4.5V)	-	-	1	V
Output high voltage	V_{OH1}	ALL I/O (IOH=-8.57mA, VDD=4.5V)	3.5	-	-	V
Input high leakage current	I_{IH}	ALL PAD	-	-	1	uA
Input low leakage current	I_{IL}	ALL PAD	-1	-	-	uA
Pull-Up resister	R_{PU}	ALL PAD	20	-	50	kΩ
Power supply current	I_{DD1}	Run Mode, INTOSC=16MHz @5V	-	*4.0	10	mA
	I_{DD2}	Sleep Mode, INTOSC=16MHz @5V	-	*2.6	5	mA
	I_{DD3}	Sub Active Mode, fSUBXIN=32.768kHz @5V	-	*270	500	uA
	I_{DD4}	STOP1 Mode, WDT Active @5V (LVR enable)	-	*50	200	uA
	I_{DD5}	STOP1 Mode, WDT Active @5V (LVR disable)	-	*25	100	uA
	I_{DD6}	STOP2 Mode, WDT Disable @5V (LVR enable)	-	*27	100	uA
	I_{DD7}	STOP2 Mode, WDT Disable @5V (LVR disable)	-	*1	7 (room temp)	uA

NOTES:

1. STOP1: WDT running
2. STOP2: WDT disable.
3. (*) typical test condition: VDD=5V, Internal RC-OSC=16MHz, ROOM TEMP, all PORT output LOW, Timer0 Active, 1 PORT toggling

21.11 AC characteristics

Table 23. AC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ +105°C, VDD= 1.8V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD=5V	15	-	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD=5V	125	–	–	ns
External Counter Input High, Low Pulse Width	**tECWH, tECWL**	ECn, VDD=5V (n=0, 1, 2)	125	–	–	ns
External Counter Transition Time	**tREC, tFEC**	ECn, VDD=5V (n=0, 1, 2)	-	–	20	ns

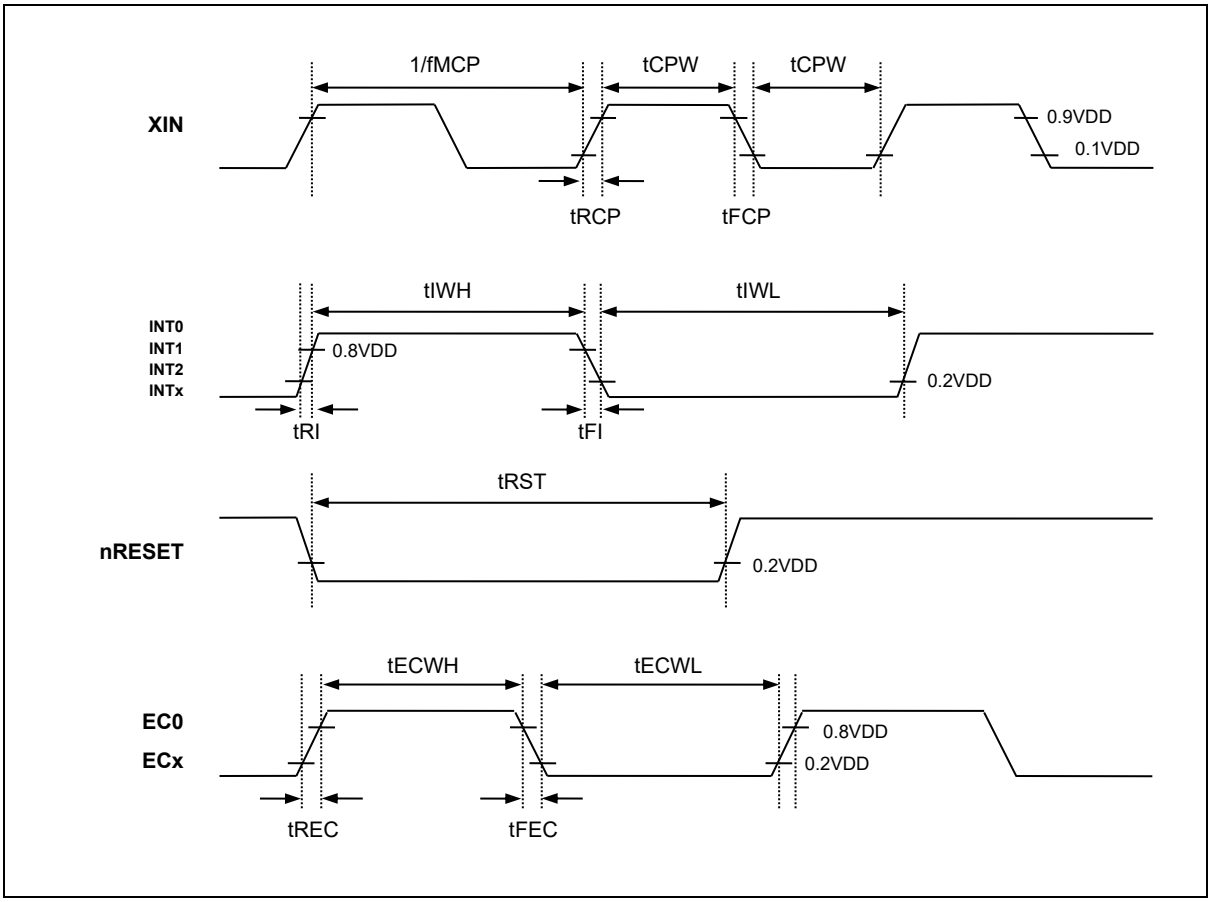


Figure 43. AC Timing

21.12 SPI characteristics

Table 24. SPI Characteristics

(T_A= -40°C – +85°C or T_A=-40°C ~ +105°C, VDD= 1.8V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output clock pulse period	t_{SCK}	Internal SCK source	200	-	–	ns
Input clock pulse period		External SCK source	200	–	–	
Output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal SCK source	70			
Input clock high, low pulse width		External SCK source	70			
First output clock delay time	t_{FOD}	Internal/External SCK source	100			
Output clock delay time	t_{DS}				50	
Input setup time	t_{DIS}		100			
Input hold time	t_{DIH}		150			

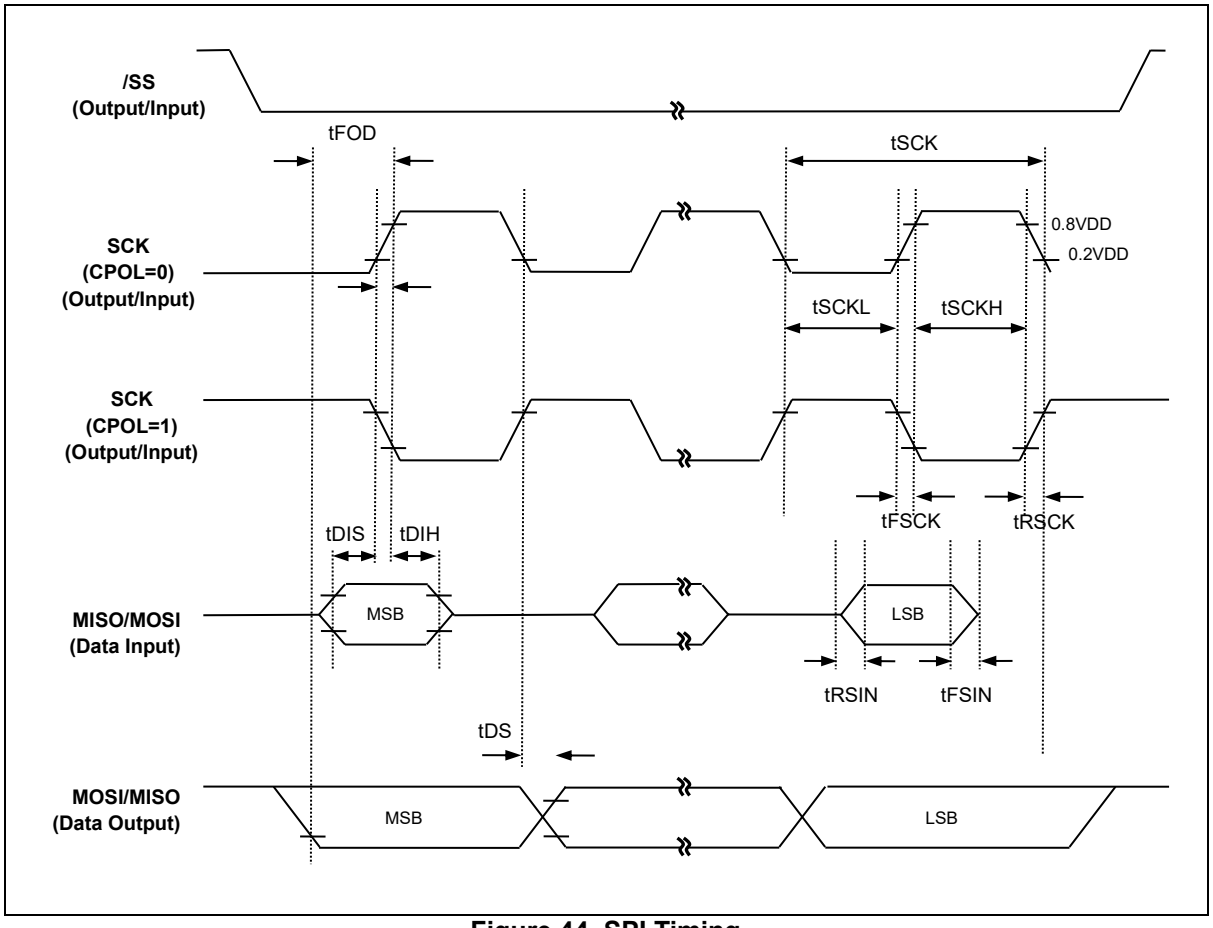


Figure 44. SPI Timing

21.13 I2C characteristics

Table 25. I2C Characteristics

(T_A= -40°C – +85°C or T_A=-40°C ~ +105°C, VDD= 1.8V – 5.5V)

Parameter	Symbol	Standard mode		High-speed mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock high pulse width	t_{SCLH}	4.0	–	0.6	–	us
Clock low pulse width	t_{SCLL}	4.7	–	1.3	–	
Bus free time	t_{BF}	4.7	–	1.3	–	
Start condition setup time	t_{STSU}	4.7	–	0.6	–	
Start condition hold time	t_{STHD}	4.0	–	0.6	–	
Stop condition setup time	t_{SPSU}	4.0	–	0.6	–	
Stop condition hold time	t_{SPHD}	4.0	–	0.6	–	
Output valid from clock	t_{VD}	0	–	0	–	
Data input hold time	t_{DIH}	0	–	0	1.0	
Data input setup time	t_{DIS}	250	–	100	–	ns

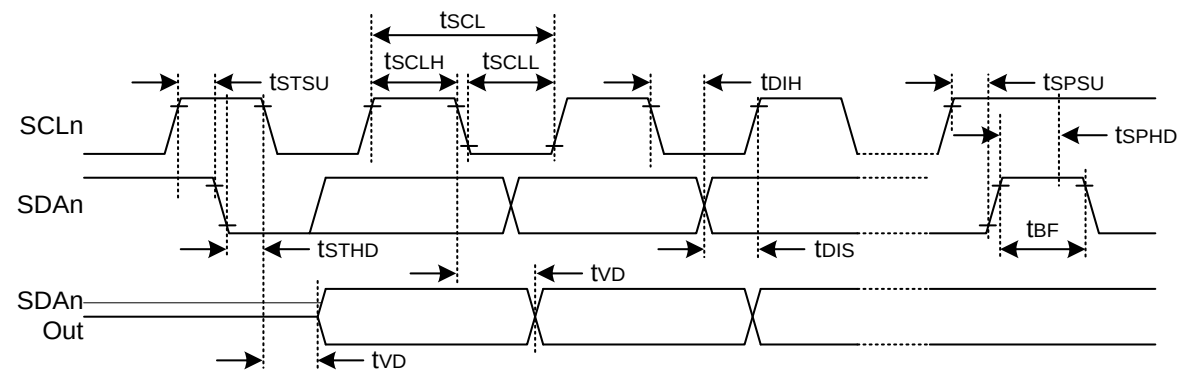


Figure 45. I2C Timing

21.14 Main clock oscillator characteristics

Table 26. Main Clock Oscillator Characteristics

(VDD=5.0V±10%, VSS=0V, T_A=-40~+85℃ or T_A=-40°C ~ +105°C)

Parameter	MIN	TYP	MAX	ETC
Operating Voltage (VDDEXT)	1.5V		5.5V	
TEMP	-40℃		85℃	
IDD	-	660uA	-	@4Mhz, VDDEXT(5V)
Operating Frequency	-		16Mhz	
Ext. Load Cap	5pF	22pF	35pF	C1,C2

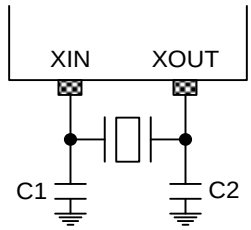


Figure 46. Crystal Oscillator

21.15 Sub clock oscillator characteristics

Table 27. Sub Clock Oscillator Characteristics

(VDD=5.0V±10%, VSS=0V, TA=-40~+85℃ or T_A=-40°C ~ +105°C)

Parameter	MIN	TYP	MAX	ETC
Operating Voltage	-	1.8V	-	
TEMP	-40℃	-	85℃	
IDD	-	3uA	-	
Operating Frequency	-	32.768kHz	-	
Ext. Load Cap	5pF	15pF	20pF	C1,C2

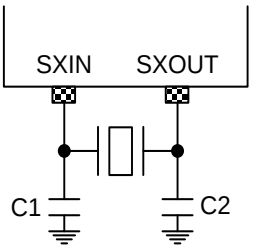


Figure 47. Sub-Crystal Oscillator

21.16 Operating voltage range

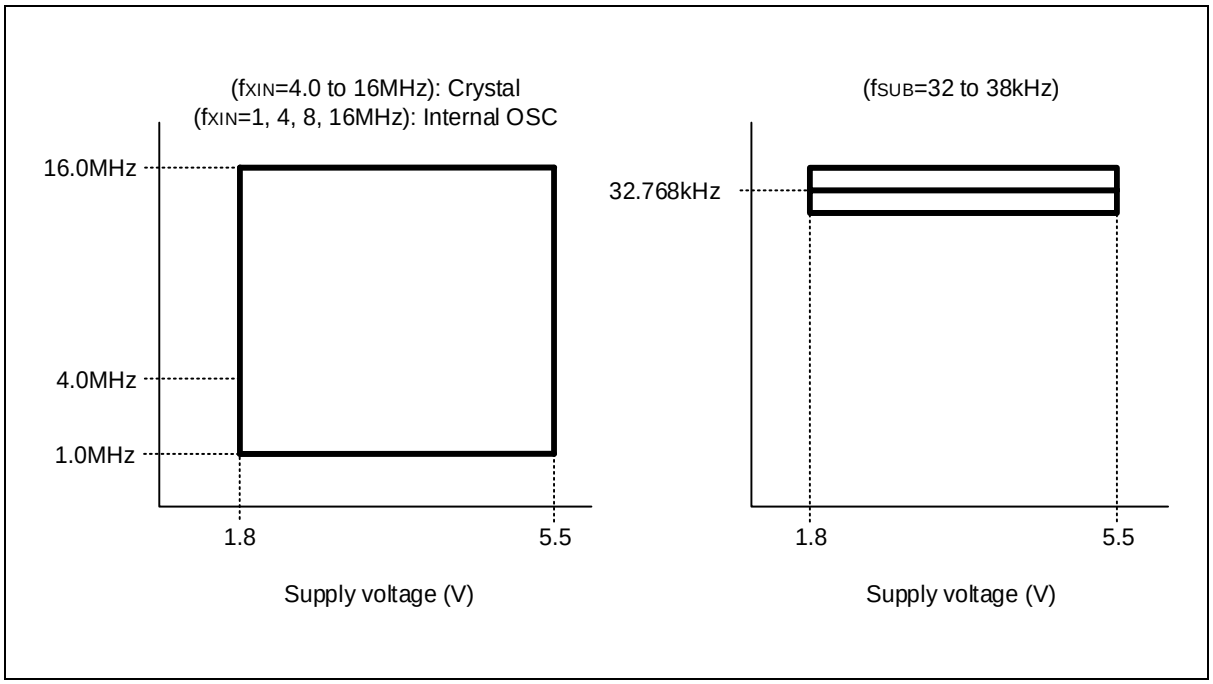


Figure 48. Operating Voltage Range

21.17 Typical characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

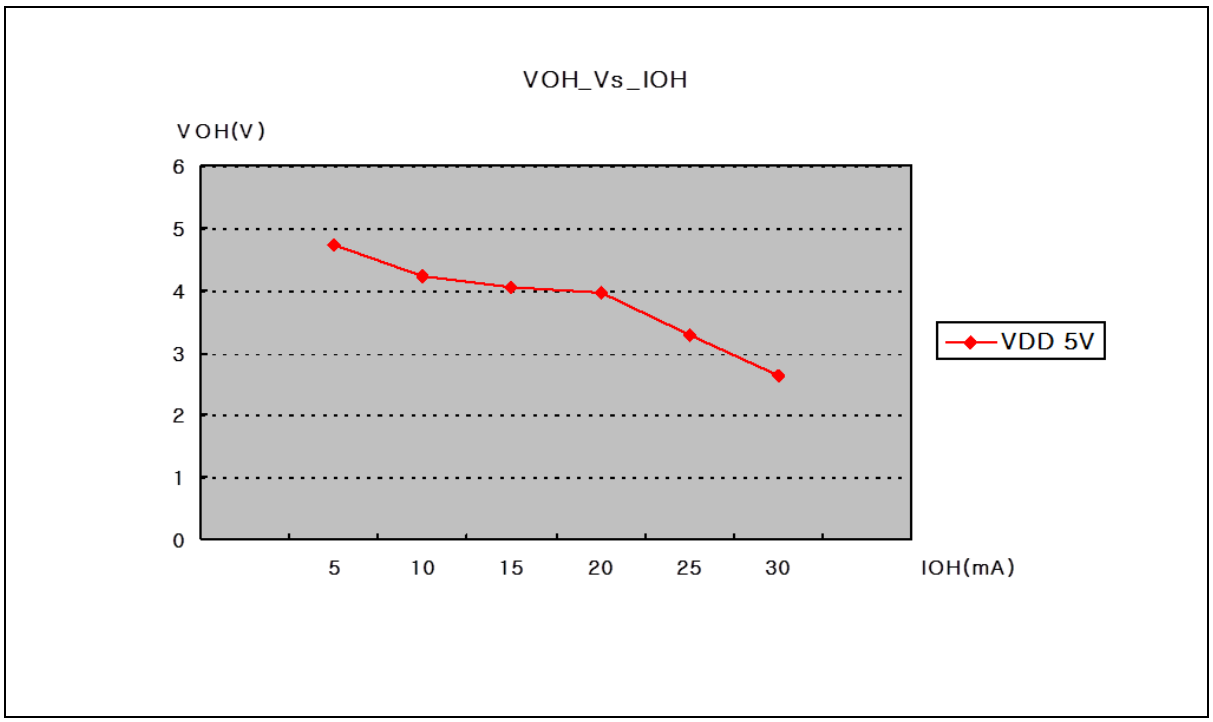


Figure 49. VOH vs IOH

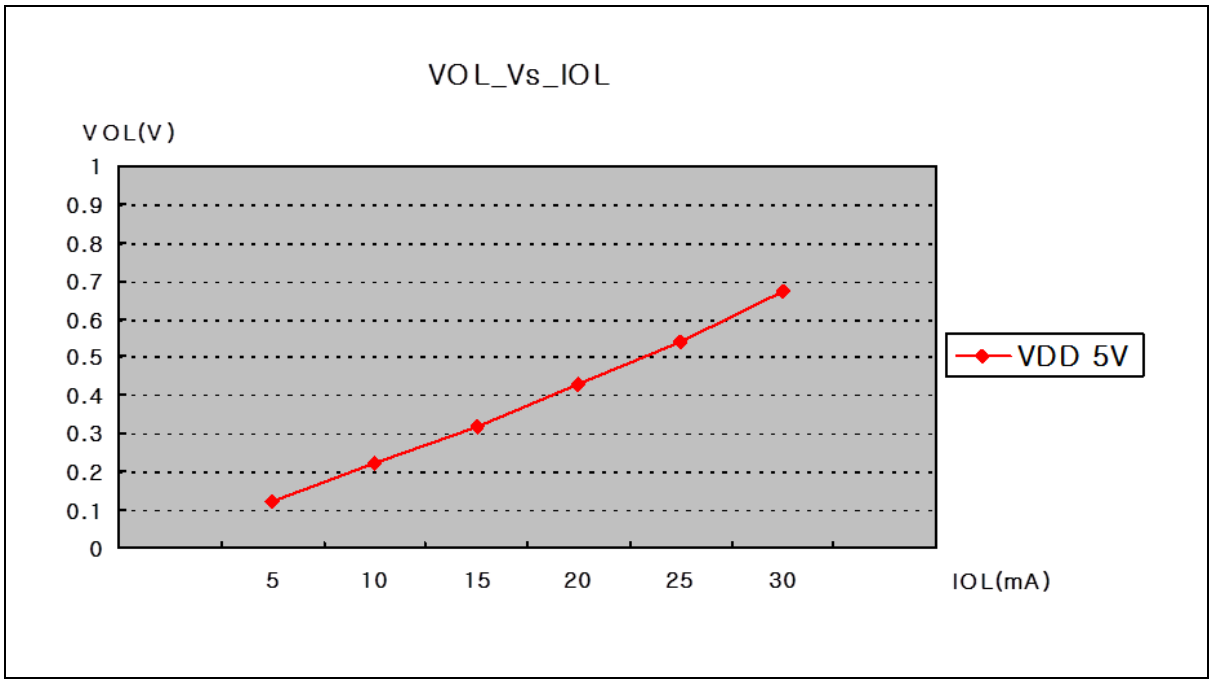


Figure 50. VOL vs IOL

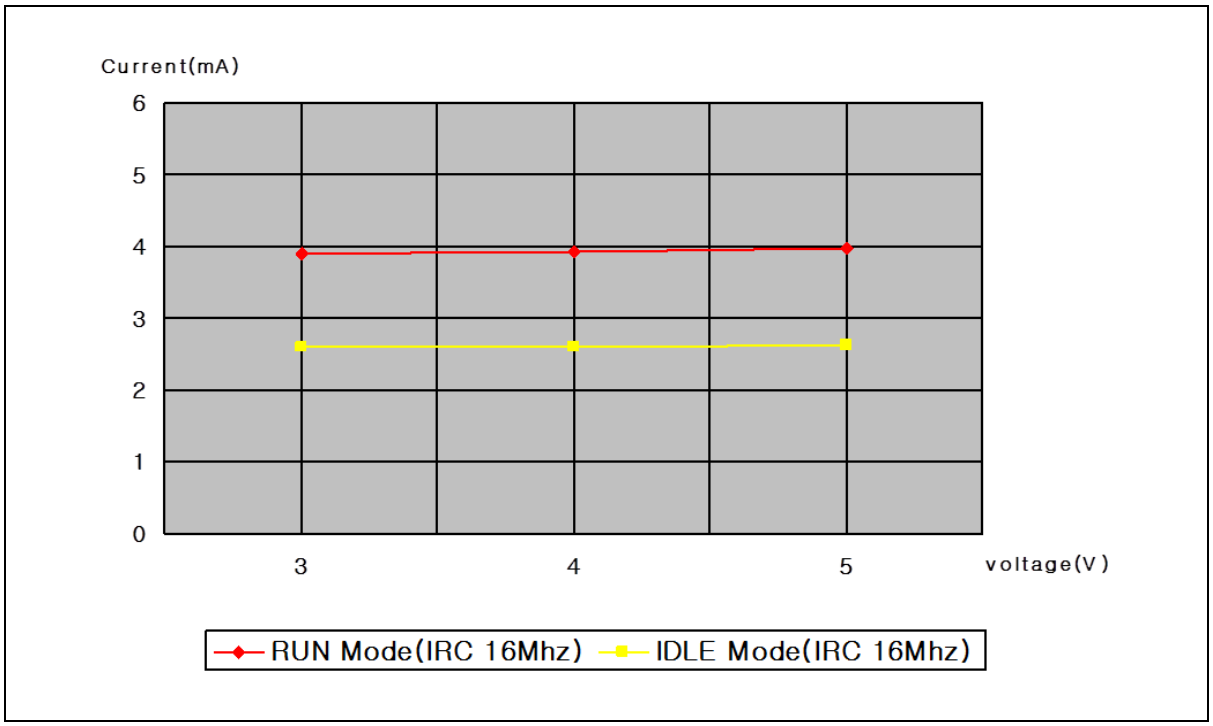


Figure 51. Power Supply Current (RUN, IDLE)

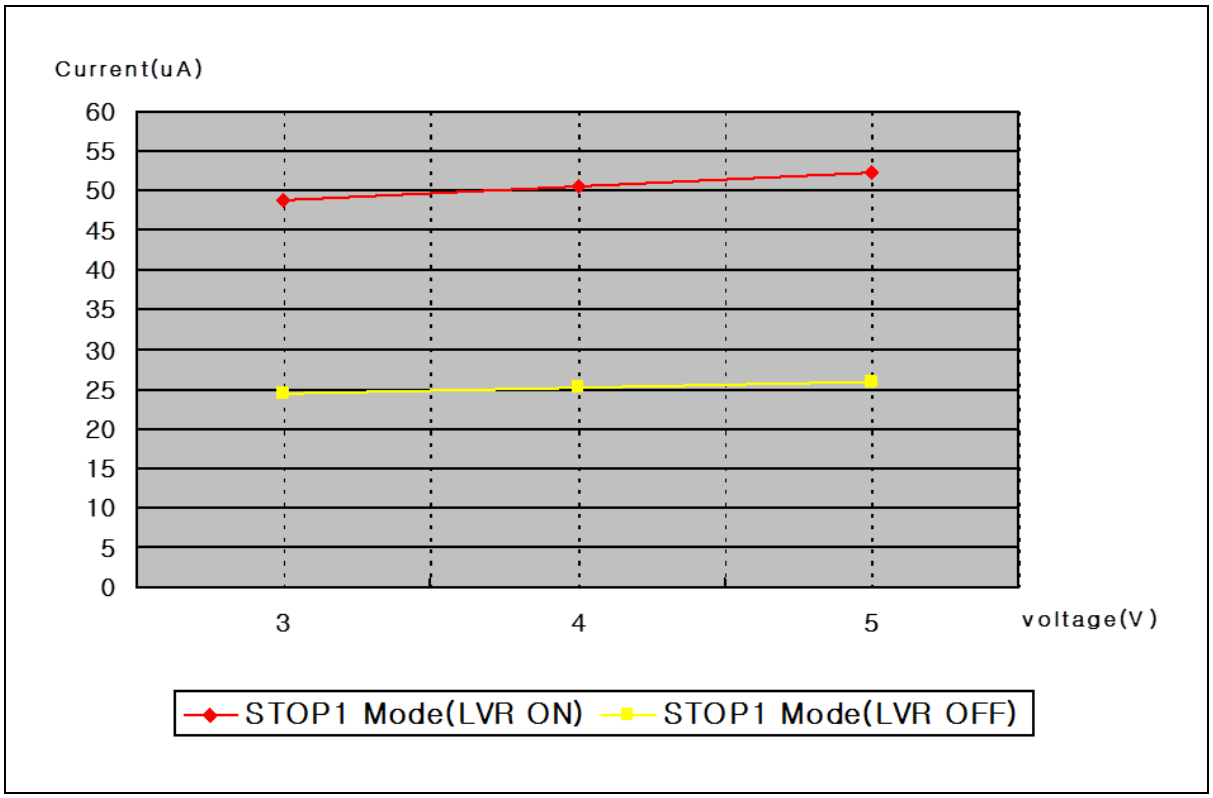


Figure 52. Stop1 Current

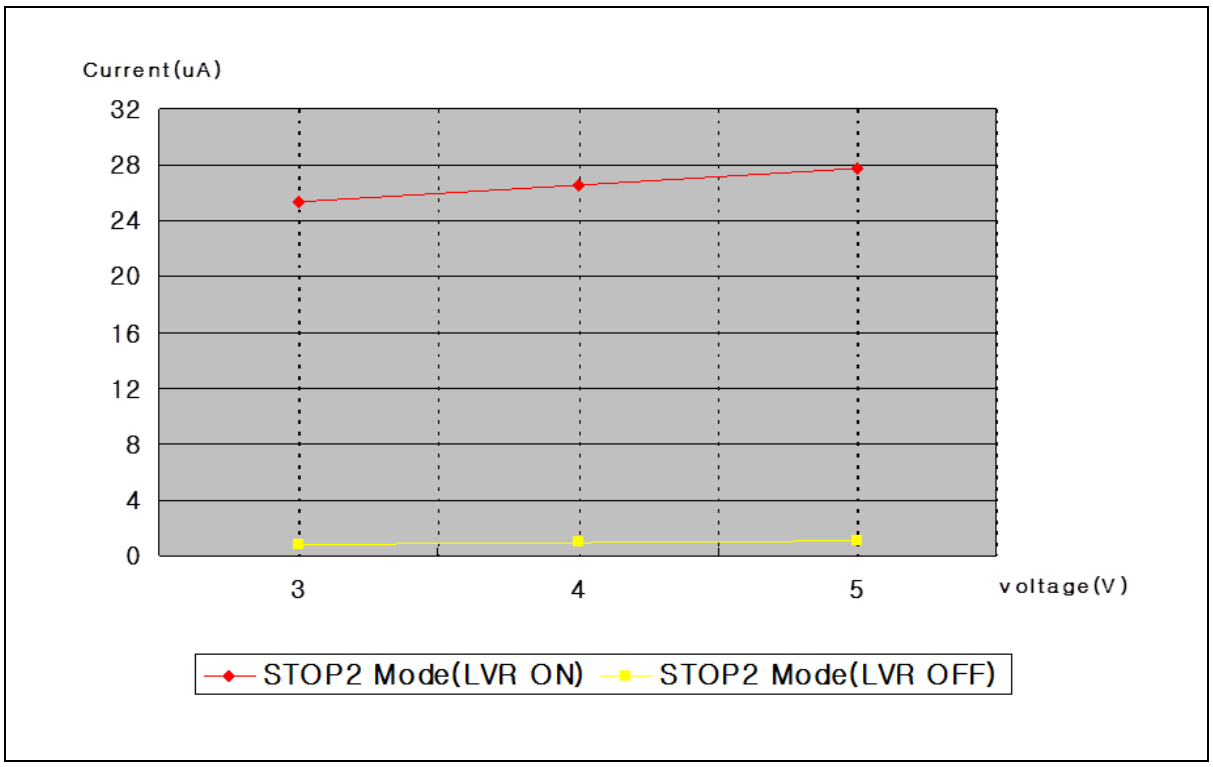


Figure 53. Stop2 Current

21.18 Recommended circuit and layout

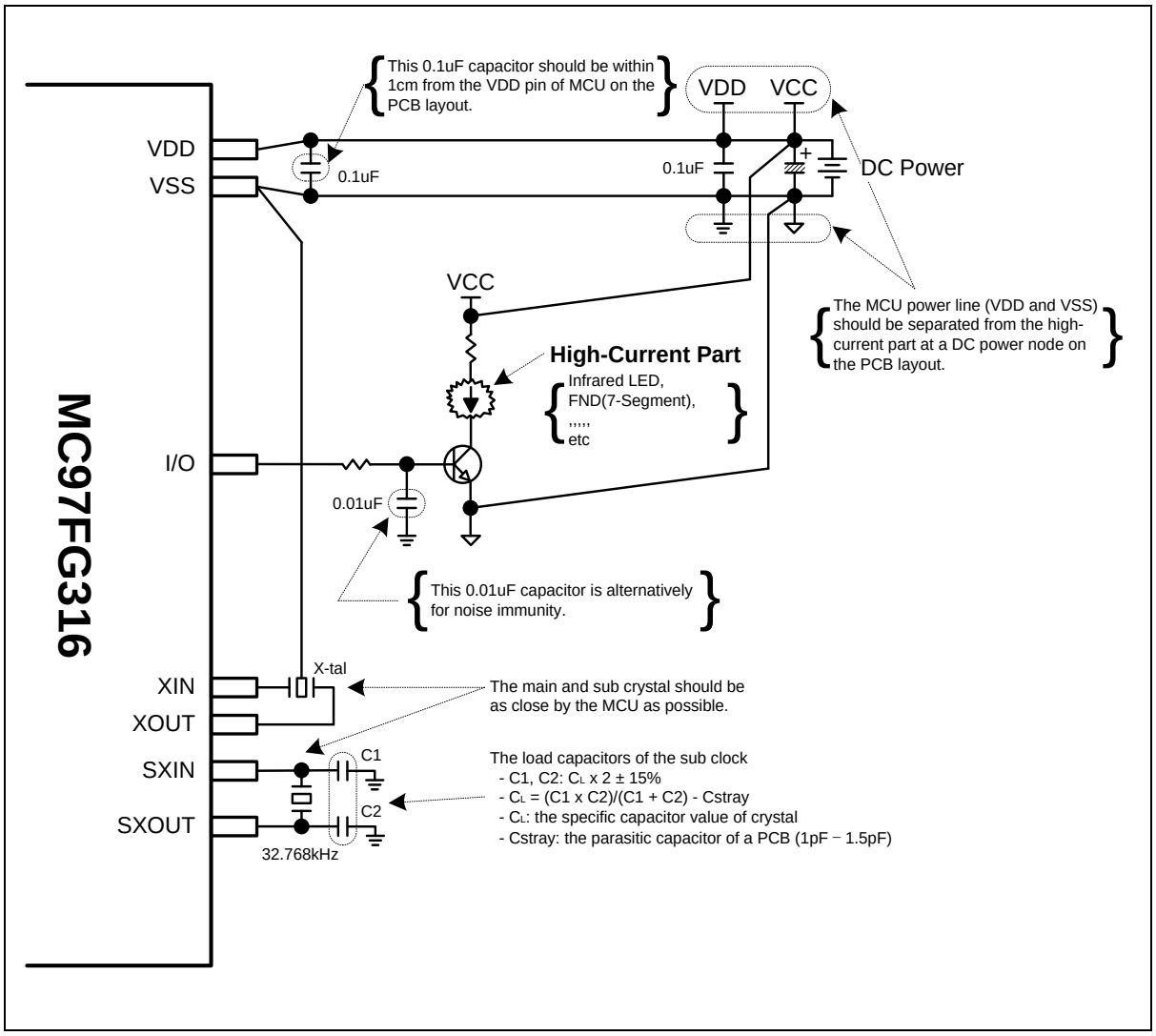


Figure 54. Recommended Circuit and Layout

22 Package information

This chapter provides MC97FG316/MC97FG216 package information.

22.1 32 LQFP package information

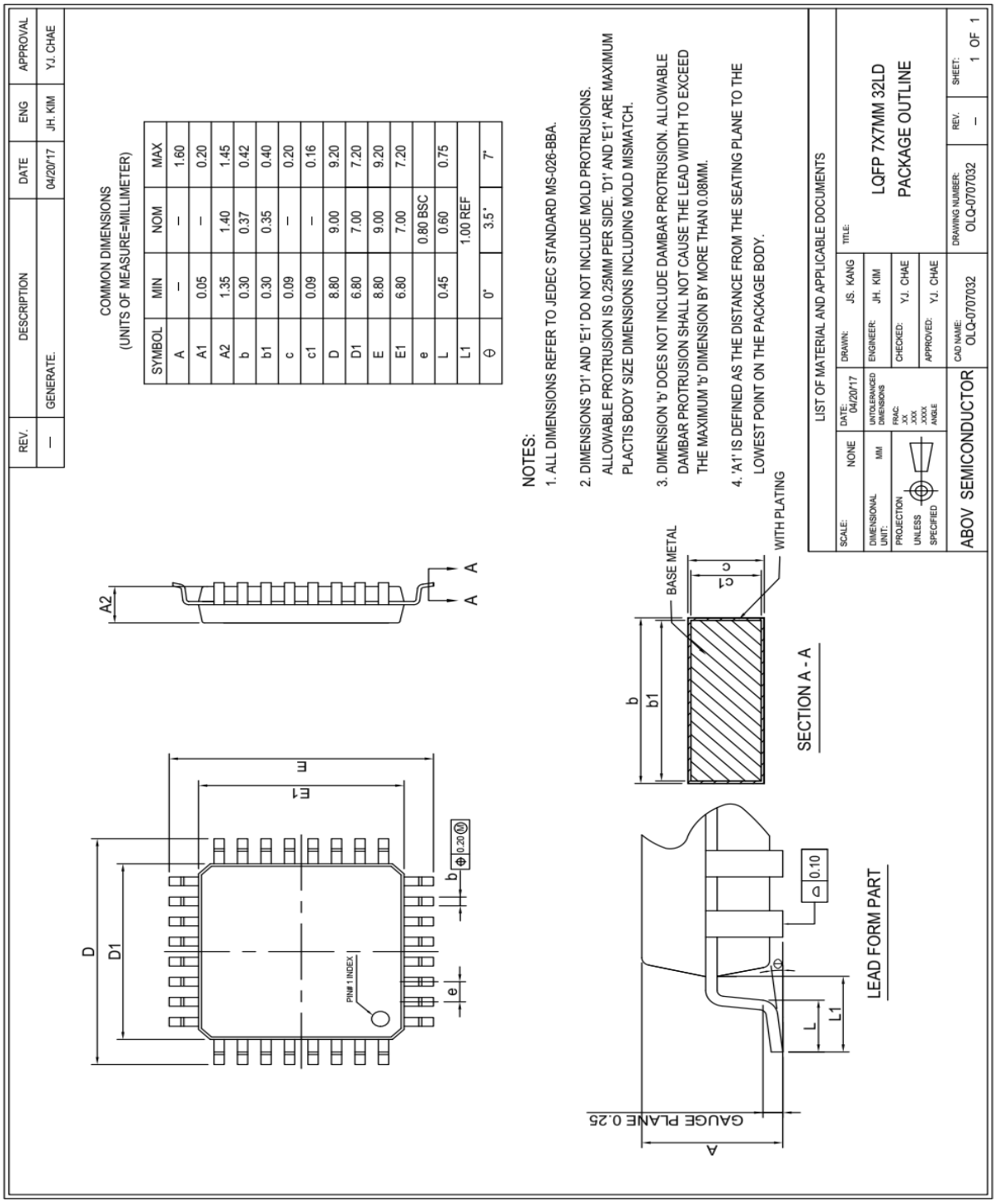


Figure 55. 32 LQFP Package Outline

22.2 32 QFN package information

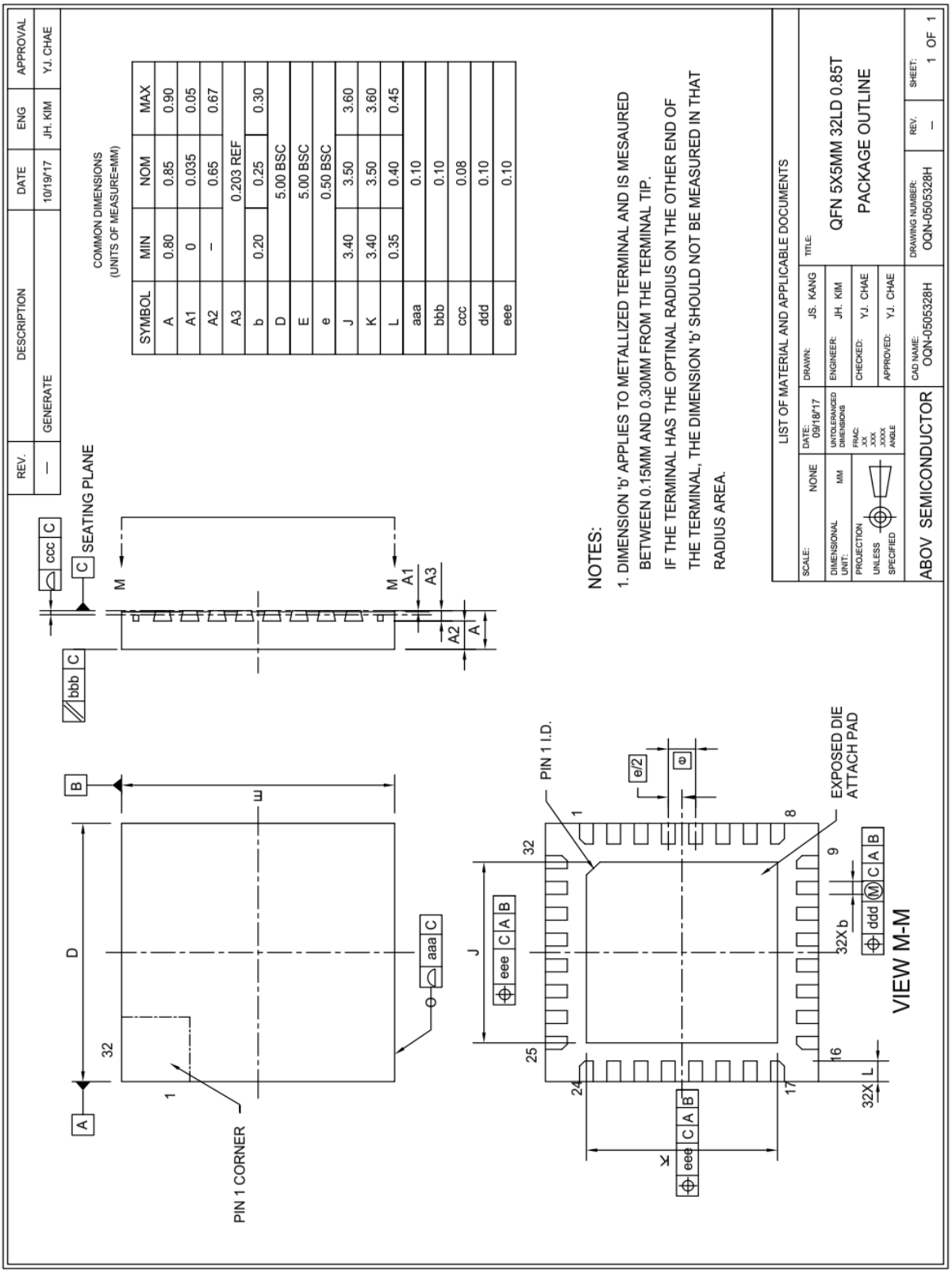


Figure 56. 32 QFP Package Outline

22.3 28 TSSOP package information

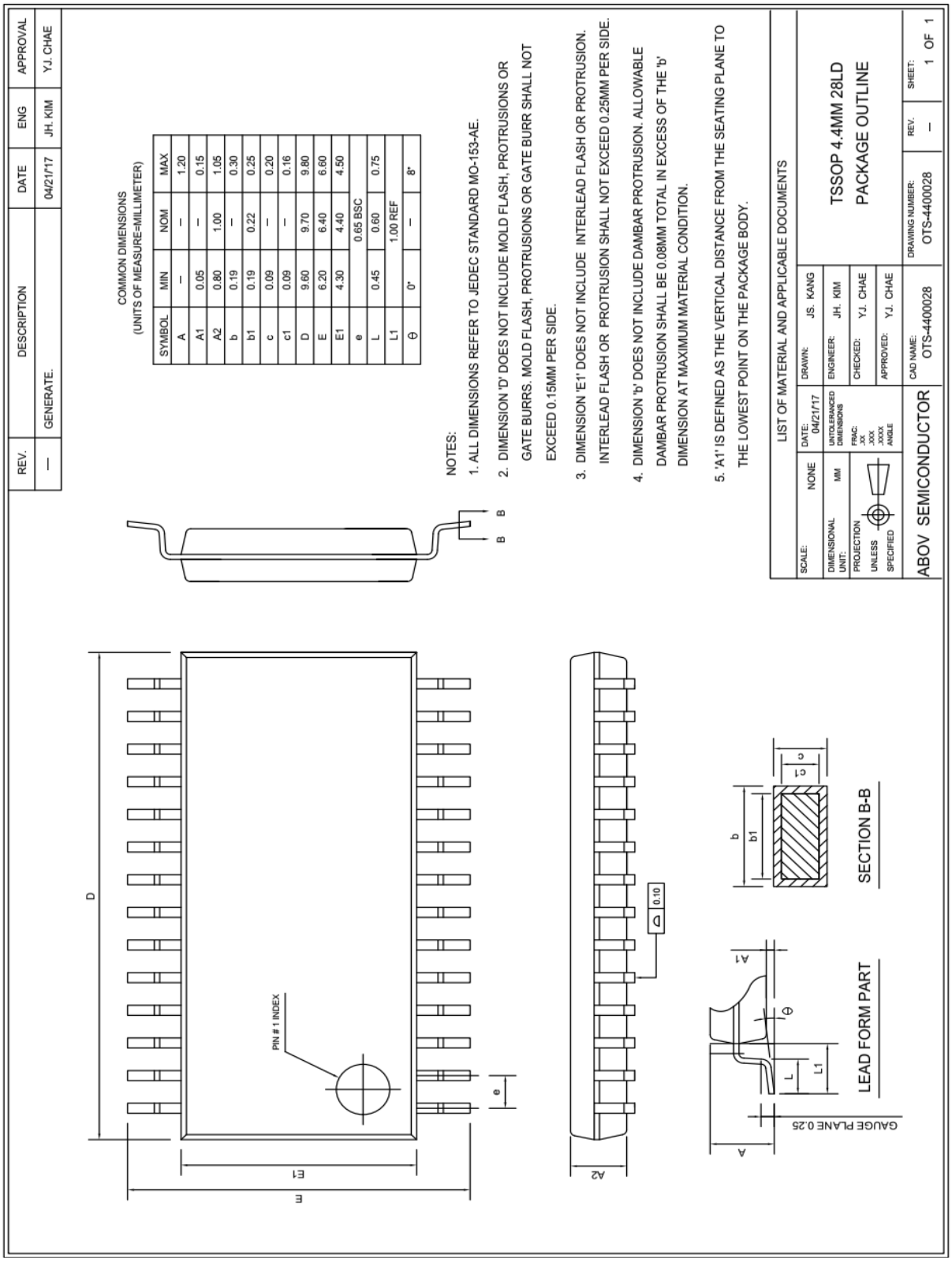


Figure 57. 28 TSSOP Package Outline

22.4 20 TSSOP package information

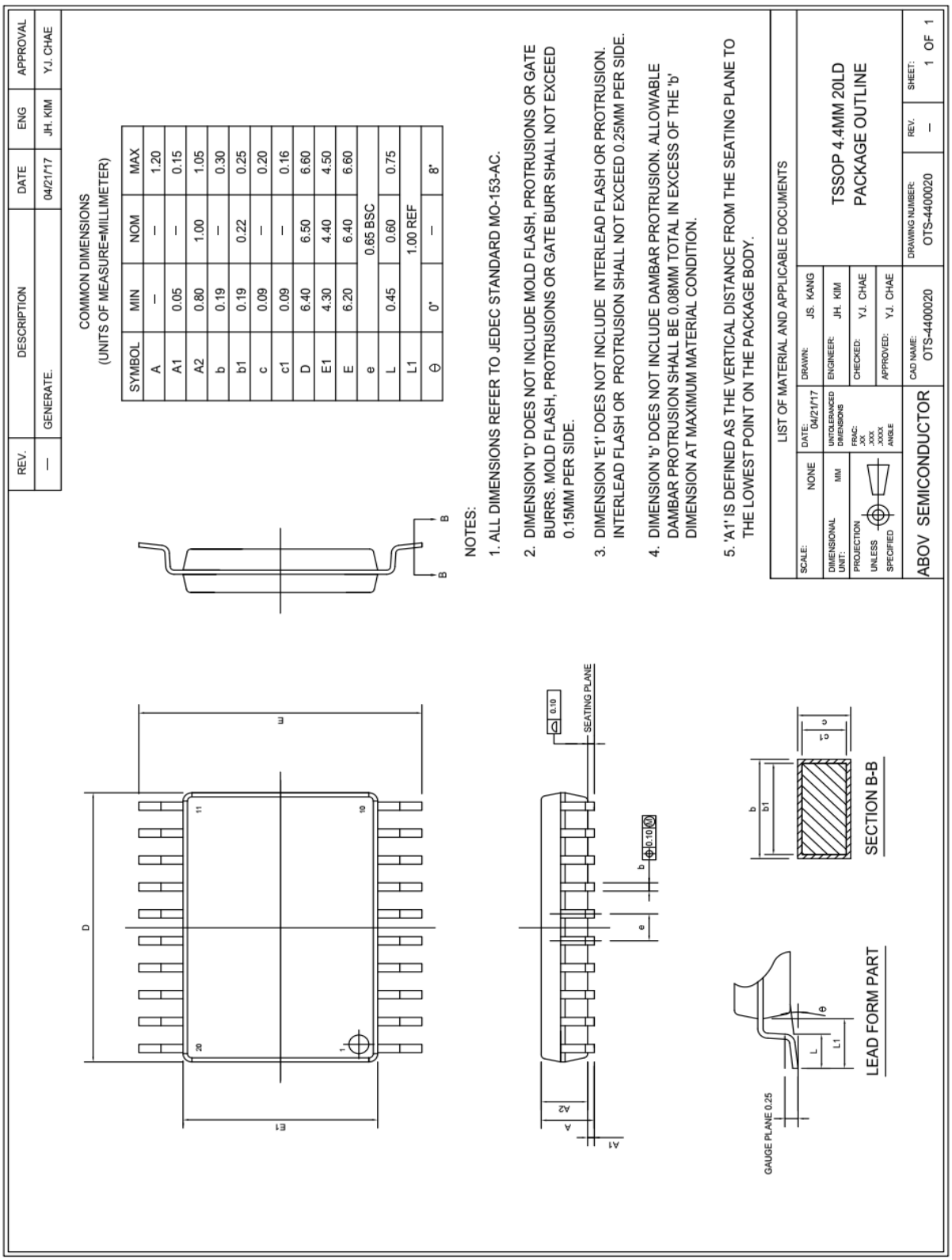


Figure 58. 20 TSSOP Package Outline

23 Ordering information

Table 28. MC97FG316/MC97FG216 Device Ordering Information

Device name	Flash	XRAM/ IRM	EEPROM	ADC input	I/O port	Package	Temperature
MC97FG316L	16K bytes	768 / 256 bytes	512 bytes	15	30	32LQFP	-40~+85°C
MC97FG316U				15	30	32QFN	
MC97FG316R				12	26	28TSSOP	
MC97FG216R				10	18	20TSSOP	
MC97FG316LB2*	16K bytes	768 / 256 bytes	512 bytes	15	30	32LQFP	-40~+105°C
MC97FG316UB2*				15	30	32QFN	
MC97FG316RB2*				12	26	28TSSOP	
MC97FG216RB2*				10	18	20TSSOP	

* For available options or further information on the device with an "*" mark, please contact the ABOV sales office.

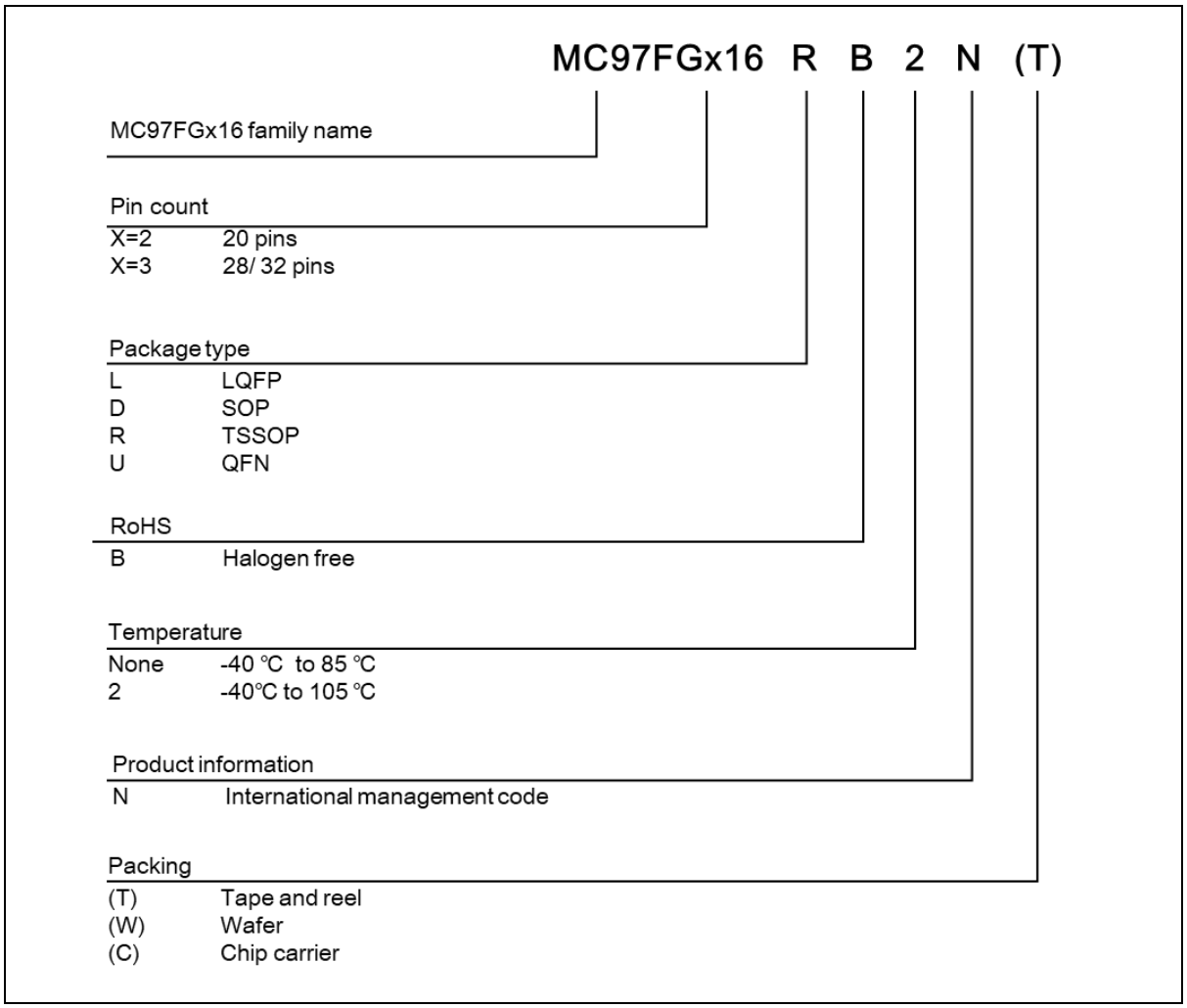


Figure 59. MC97FG316/MC97FG216 Device Numbering Nomenclature

24 Development tools

This chapter introduces wide range of development tools for MC97FG316/MC97FG216. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

24.1 Compiler

ABOV semiconductor does not provide any compiler for MC97FG316/MC97FG216. It is recommended to consult a compiler provider.

Since MC97FG316/MC97FG216 has Mentor 8051 as its core, and ROM is smaller than 32Kbytes in size, a developer can use any standard 8051 compiler of other providers.

24.2 OCD II (On-chip debugger) emulator and debugger

The OCD II emulator supports ABOV′s 8051 series MCU emulation. The OCD II uses two wires interfacing between PC and MCU, which is attached to user′s system. The OCD II can read or change the value of MCU′s internal memory and I/O peripherals. In addition, the OCD II controls MCU′s internal debugging logic. This means OCD II controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD II debugger program runs underneath MS operating system such as MS-Windows 10/NT/ 2000/ XP/ Vista (32-bit). If a user wants to see more details, it is recommend to refer to OCD II debugger manual by visiting ABOV′s website (http://www.abovsemi.com) and downloading debugger S/W and corresponding manuals.

- Connection:
  - DSCL (MC97FG316/MC97FG216 P06 port)
  - DSDA (MC97FG316/MC97FG216 P07 port)

Figure 60 shows pinouts of OCD connector.

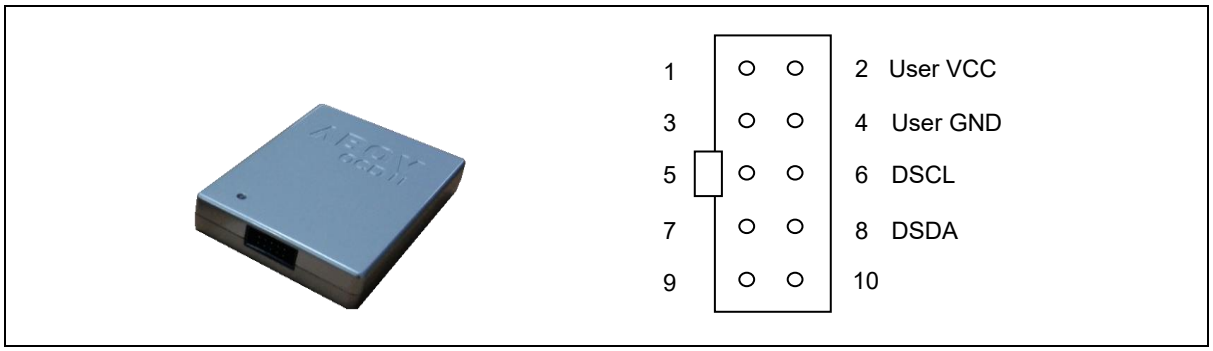


Figure 60. Debugger (OCD2) and Pinouts

24.3 Programmers

24.3.1 E-PGM+

E-PGM+ USB is a single programmer. A user can program MC97FG316/MC97FG216 directly using the E-PGM+.

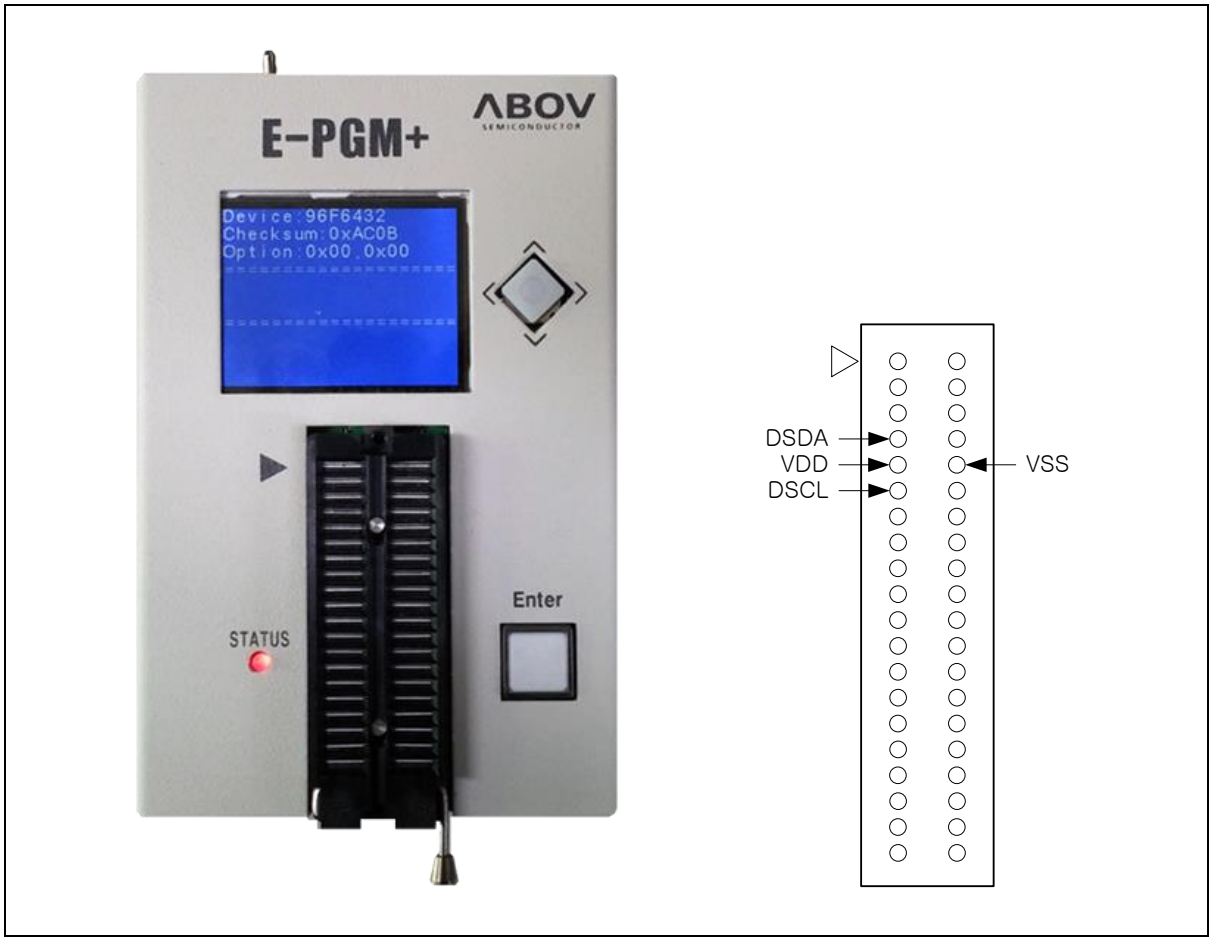


Figure 61. E-PGM+ (Single Writer) and Pinouts

24.3.2 OCD II emulator

OCD II emulator allows a user to write code on the device too, since OCD II debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

24.3.3 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

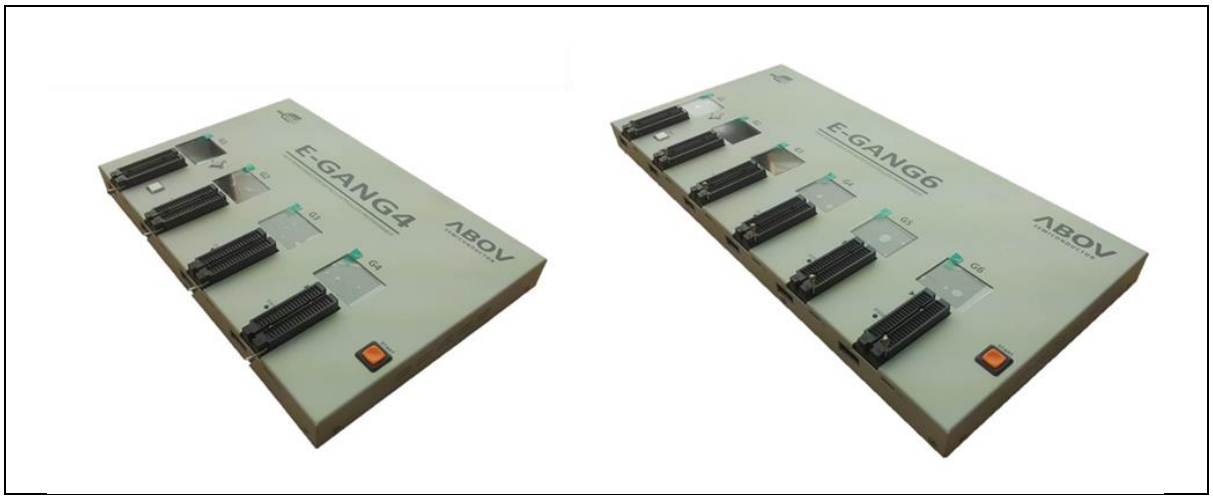


Figure 62. E-Gang4 and E-Gang6 (for Mass Production)

24.4 Flash programming

Program memory of MC97FG316/MC97FG216 is a flash type. This flash ROM is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. For more information about flash memory programming, please refer to **20. Memory programming.**

Table 29 introduces each pin and corresponding I/O status.

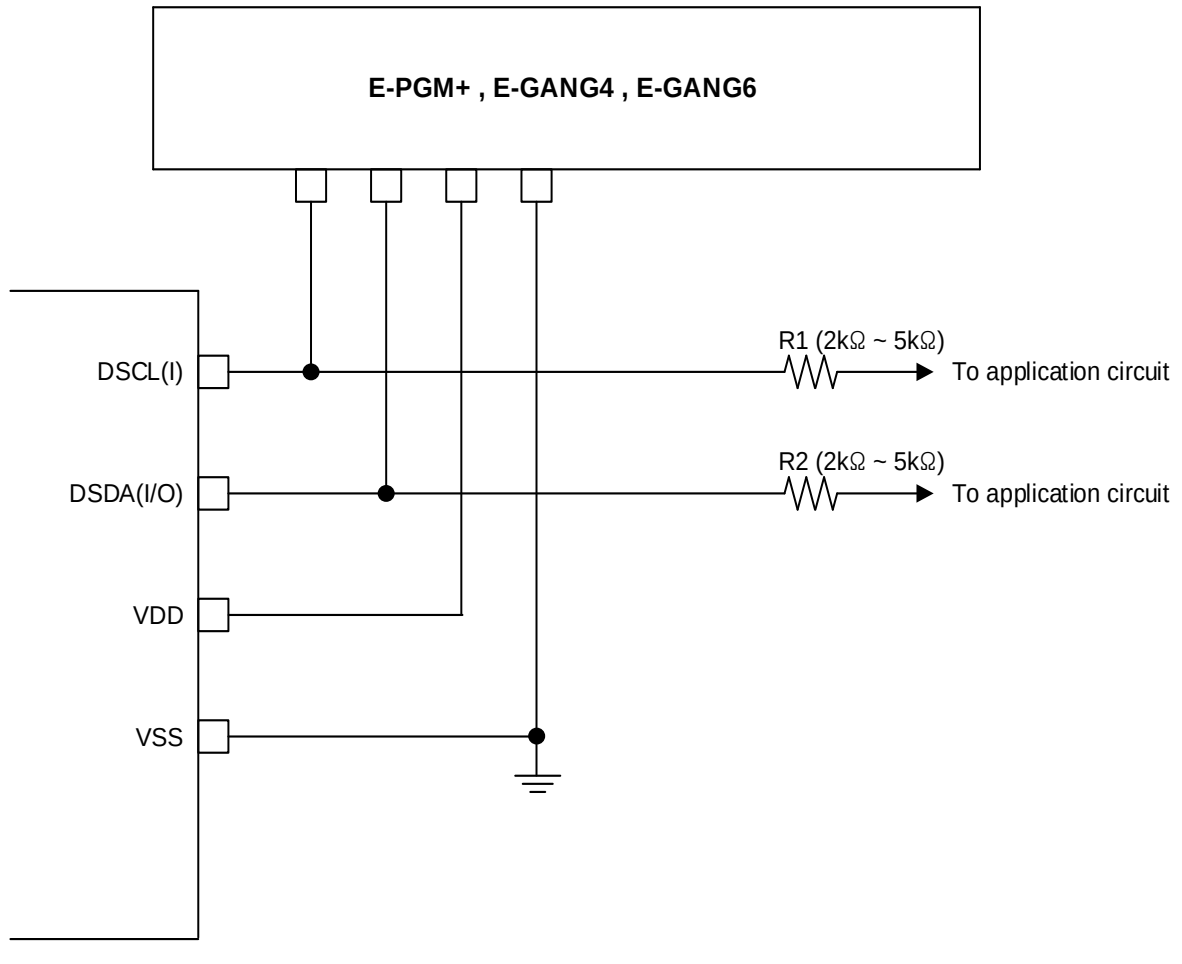
Table 29. Pins for Flash Programming

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

24.4.1 Circuit design guide

When programming flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. If a user designs a PCB circuit, the user should consider the usage of these 4 signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 63. PCB Design Guide for On-Board Programming

24.5 On-chip debug system

MC97FG316/MC97FG216 supports On-chip debug II (OCD II) system. We recommend to develop and debug program with MC97FG316/MC97FG216. On-chip debug system of MC97FG316/MC97FG216 can be used for programming the non-volatile memories and on-chip debugging. Detail descriptions for programming via the OCD II interface can be found in this section.

Table 30 introduces features of OCD II.

Table 30. OCD II Features

Two wire external interface	1 for serial clock input 1 for bi-directional serial data bus
Debugger accesses	All internal peripherals Internal data RAM Program Counter Flash memory and data EEPROM memory Support all OCD II device series Run-time data monitoring function Operating frequency measurement function
Extensive On-Chip Debugging supports for Break Conditions	Break instruction Single step break Program memory break points on single address Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface On-Chip Debugging supported by OCD II Support up to 12 breaks points
Operating frequency	The maximum frequency of a target MCU.

Figure 64 shows a block diagram of the OCD II interface and the On-chip Debug system.

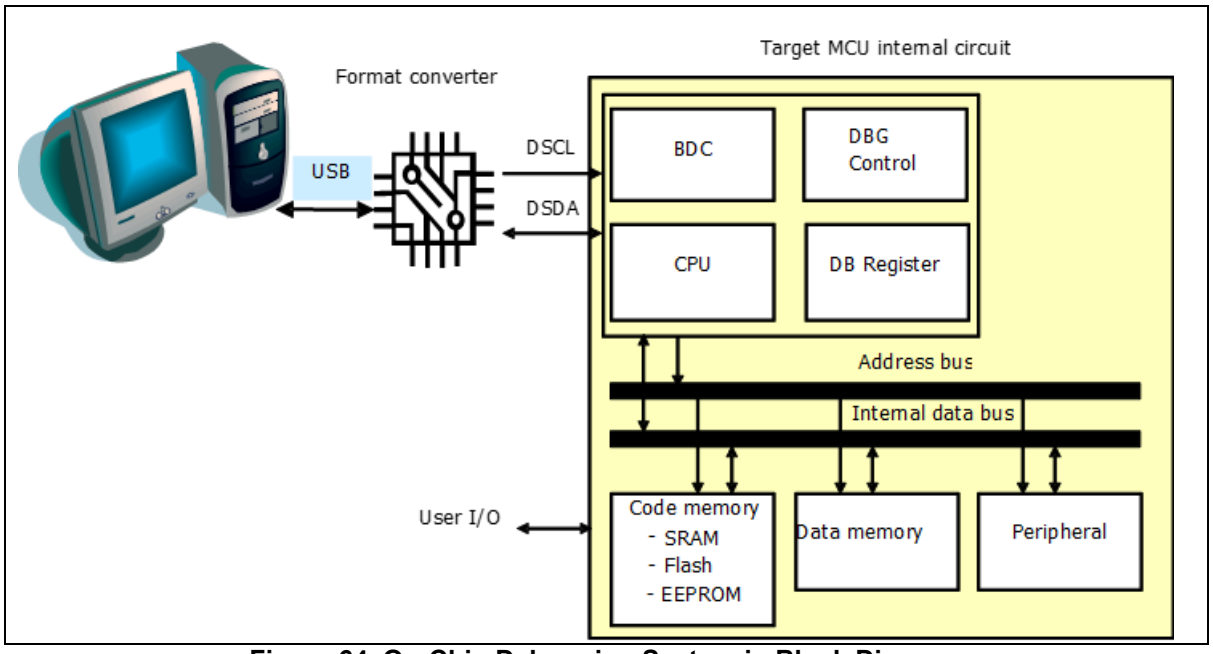


Figure 64. On-Chip Debugging System in Block Diagram

24.5.1 Two-pin external interface

Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

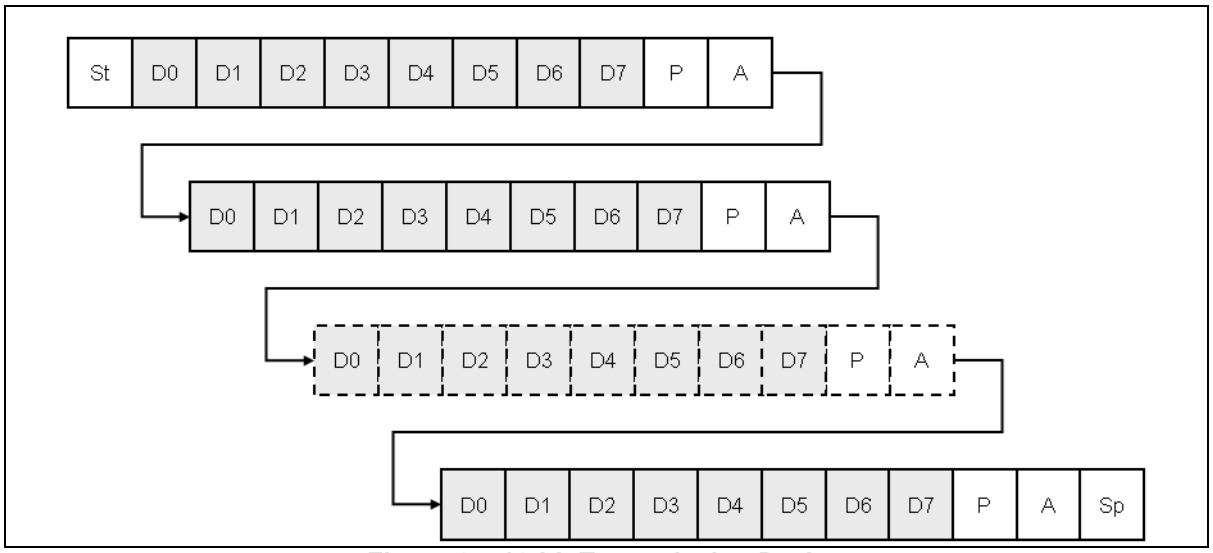


Figure 65. 10-bit Transmission Packet

Packet transmission timing

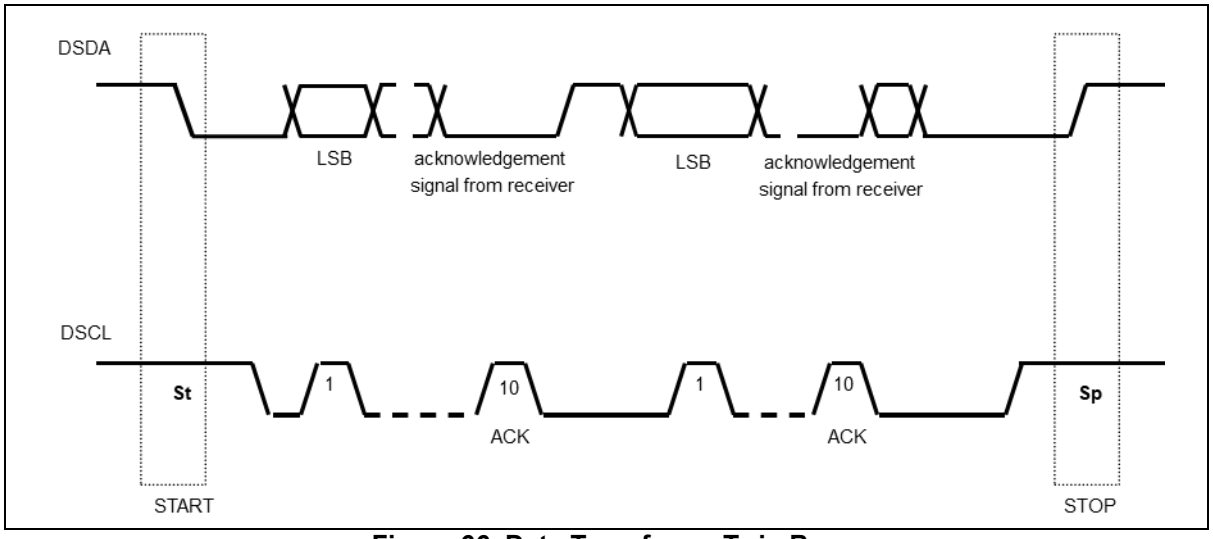


Figure 66. Data Transfer on Twin Bus

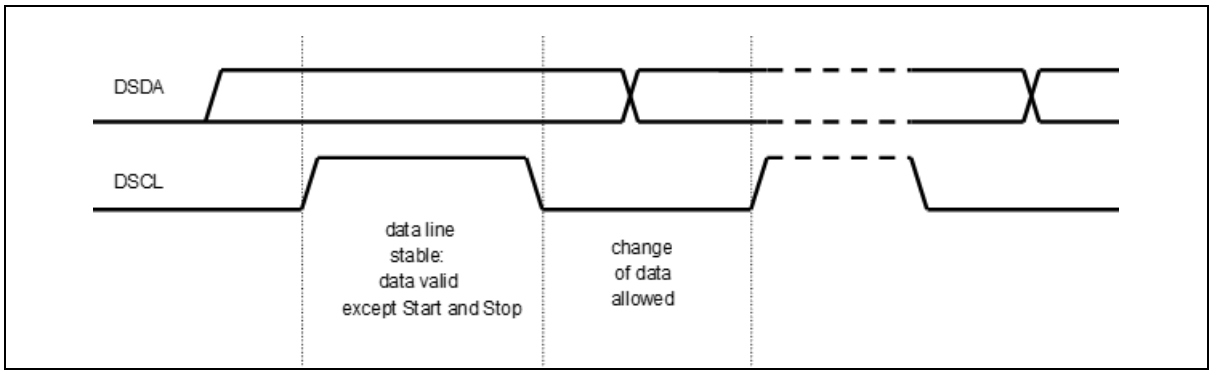


Figure 67. Bit Transfer on Serial Bus

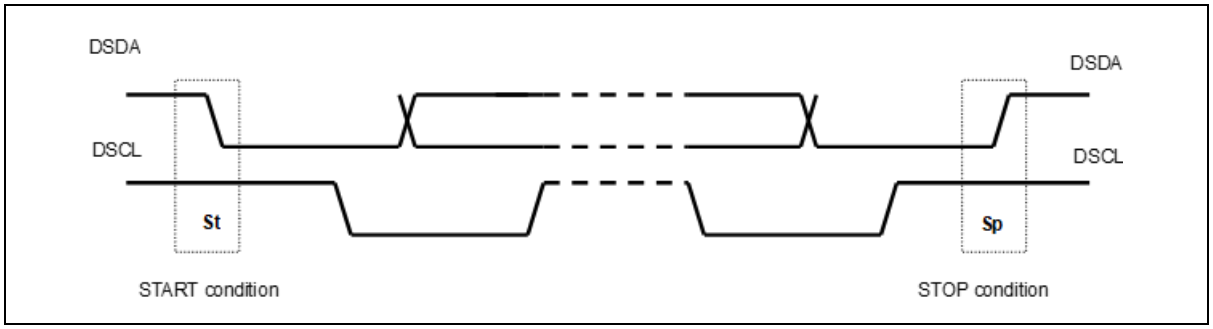


Figure 68. Start and Stop Condition

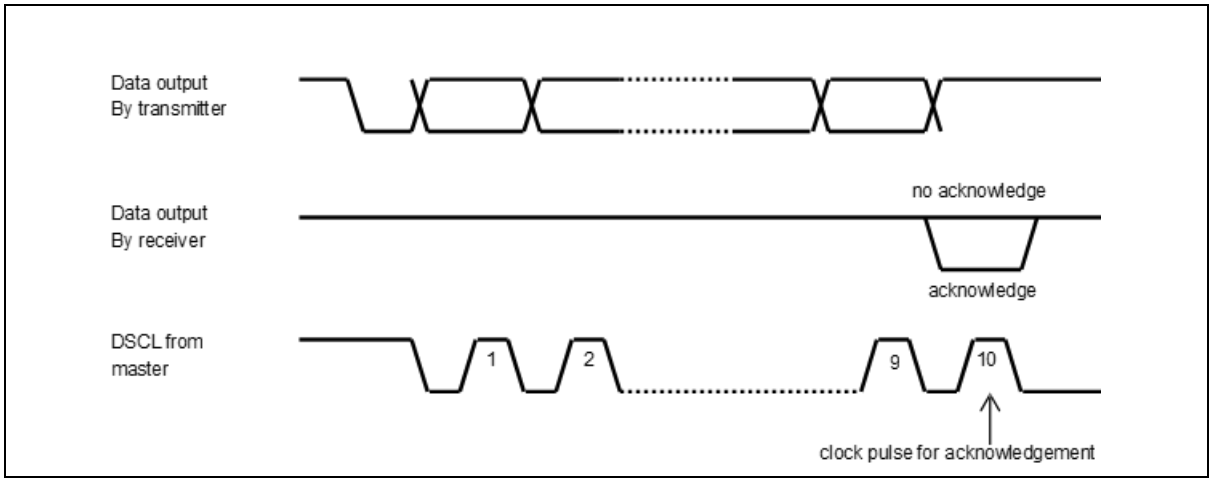


Figure 69. Acknowledge on Serial Bus

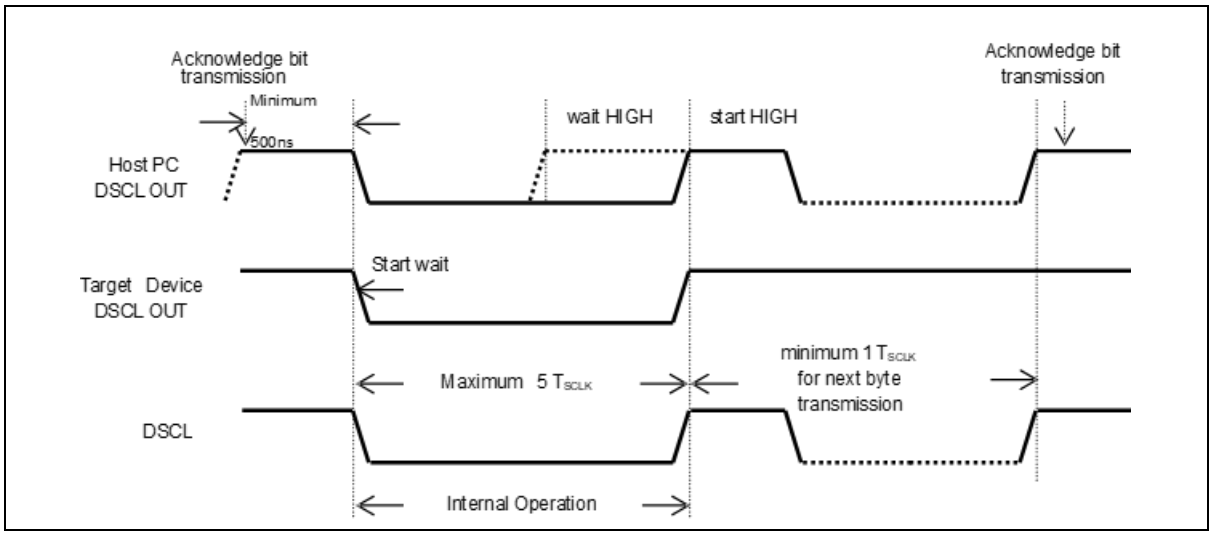


Figure 70. Clock Synchronization during Wait Procedure

Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

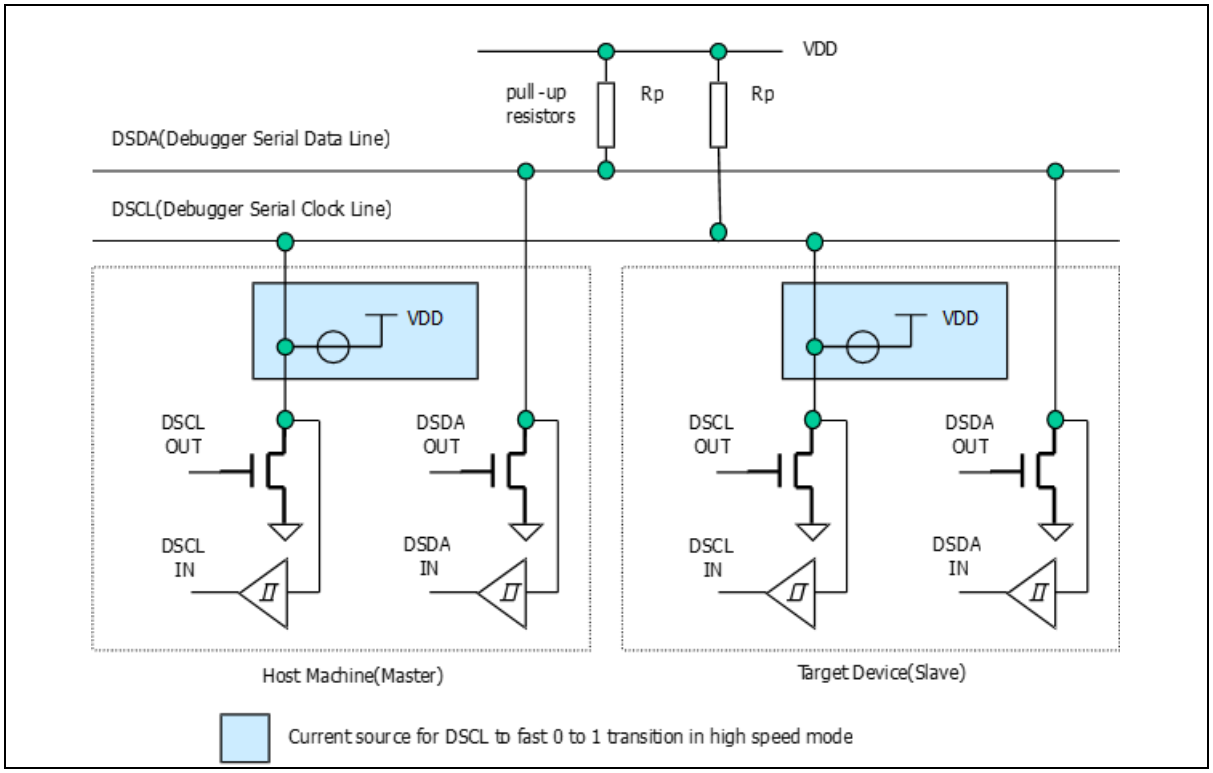


Figure 71. Connection of Transmission

Appendix

Instruction table

Instructions are either1, 2 or 3bytes long as listed in the ‘Bytes’ column below. Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

Table 31. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 32. Instruction Table: Logical

Logical				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 33. Instruction Table: Data Transfer

Data transfer				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 34. Instruction Table: Boolean

Boolean				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 35. Instruction Table: Branching

Branching				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 36. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00
Additional instructions (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, entries such as E8-EF indicate continuous blocks of hex opcodes used for 8 different registers. Register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as ′11→F1′ (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

CJNE instructions use abbreviation of #d for immediate data; other instructions use #data as an abbreviation.

Revision history

Date	Version	Description
2015.06.05	1.00	First creation
2015.08.12	1.01	Added 32QFN
2015.08.18	1.02	Updated 28TSSOP device name and Analog Comparator description
2015.10.29	1.03	Added the description for using external reset. Add E-PGM+(single writer) in Chapter 24.3 Programmers Changed to '-10mA/-80mA for IOH & ∑IOH in absolute maximum ratings. Changed to 15us for "nReset input plus L width" in AC characteristics. Added PWM1 description Corrected 28/20 TSSOP package diagram
2015.12.03	1.04	Modified WDT description
2016.02.12	1.05	Changed to '±10/±40 (Min/Max)' for "Voffset" in Analog comparator electrical characteristics
2016.04.26	1.06	Updated table format and contents in 21 Electrical characteristics. Added Operating Voltage Range and Typical Characteristics Changed the name of BOD to LVR
2017.08.09	1.07	Update table format and contents in 21 Electrical characteristics. Changed Ring-OSC characteristics(symbol) Changed DC characteristics (IDD1/IDD2) Modified Clock Generator Block diagram Modified incorrect contents of SCCR register Modified the contents of WDT Modified WDT Block diagram Updated timing chart and contents in Power Down Operation Updated Pin Assignment (32LQFP/20TSSOP/28TSSOP) in 22 Package information. Modified incorrect contents of PSR1/PSR2 register
2018.01.24	1.08	Added Device Nomenclature Modified Internal RC Oscillator Spec. Updated Package Diagram in 22 Package information
2020.04.09	1.09	Added the caution for setting of PLLCR register Changed sales contact information
2020.04.21	1.10	Expanded Ordering Information and Device Nomenclature to 105°C MCU
2020.05.28	1.11	Renewed the contents of a manual including text format, description and so on Expanded the operating temperature to 105°C at electrical characteristics Added how to write the configure option in user program
2020.07.20	1.12	Corrected EEPROM size at Table 2. MC97FG316/MC97FG216 Device Features and Peripheral Counts.
2022.11.11	1.13	Revised the font of this document.

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