QEC CESIGN IP (CSMC 0.18um)

Atomic Pulse Generator

Features

- 3.0V~3.6V supply voltage available.
- Photodiode
  - ✓ Integrated Si PN photodiode.
- Tran-Impedance Amplifier.
  - ✓ 200K trans-impedance gain.
  - ✓ 10MHz unit gain bandwidth.
- Comparator
  - ✓ 5mV hysteresis level.
  - ✓ 10ns propagation delay time.
  - ✓ 5V interface with open drain NFET
- Voltage reference
  - ✓ 1.2V internal voltage reference.

General Description

The QEC Cesign IP is an analog IP that consist of 1.2V voltage reference, trans-impedance amplifier, gain amplifier, comparator with integrated Si PN photodiode.

Applications

- Atomic random pulse generator.
- Photo sensor.

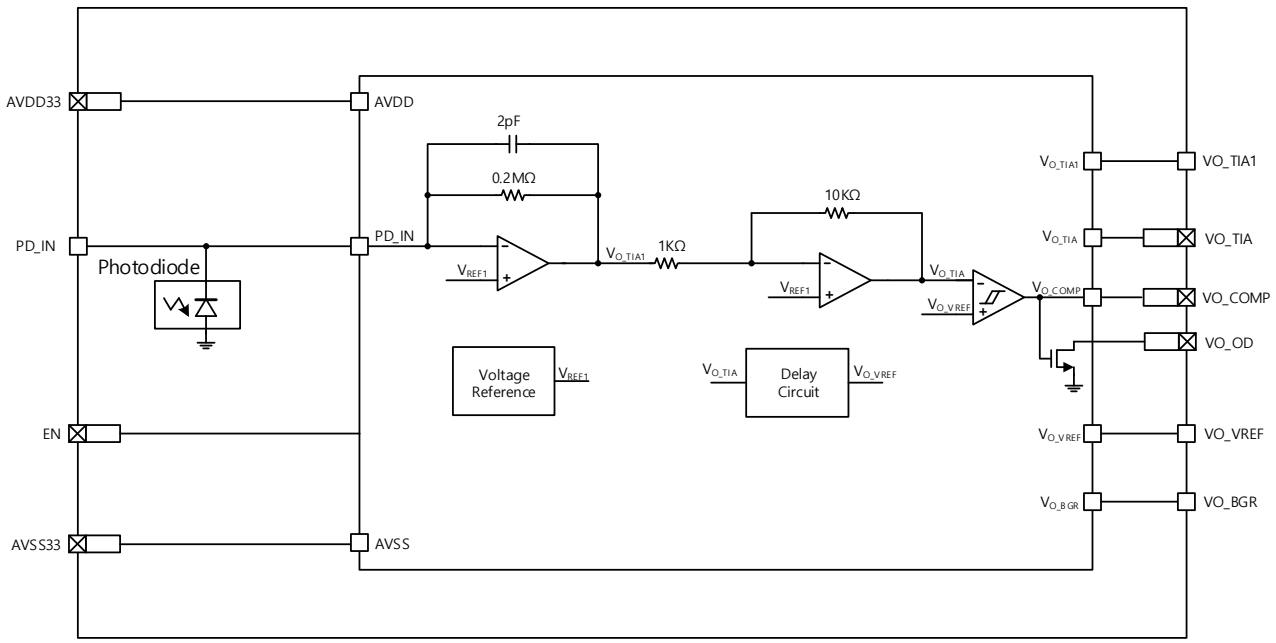

Figure 1. Functional Block Diagram

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted)

Symbol	Rating	Max	Unit
AVDD33	Supply Voltage	3.6	V
T_A	Operating free-air temperature range	-40 to 85	°C

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Symbol	Rating	MIN	TYP	MAX	Unit
AVDD33	Analog Supply voltage	3.0	3.3	3.6	V
T_A	Operating free-air temperature range	-40	25	85	°C

Electrical Specifications

Table 3. Electrical Specifications

(Condition: T_A = 25 ºC, AVDD = 3.3 V unless otherwise noted)

Parameter (condition)	Values			Unit
	Min.	Typ.	Max.	
Supply voltage	3.0	3.3	3.6	V
Operating temperature	-40	25	85	°C
Current consumption		0.9		mA
IP size		1.4*1.4		mm^2
Photodiode				
Reverse voltage		1.2		V
Junction capacitance		100		pF
Dark current		1		nA
Trans-Impedance Amplifier				
Trans-impedance gain		0.2//2		MΩ//pF
Unit gain bandwidth		10		MHz
Equivalent input referred noise (@f=1KHz)		30		nV/√Hz
Comparator				
Unit gain bandwidth		10		MHz
Hysteresis level		20		mV
Min. differential input		5		mV
Propagation delay		10		ns

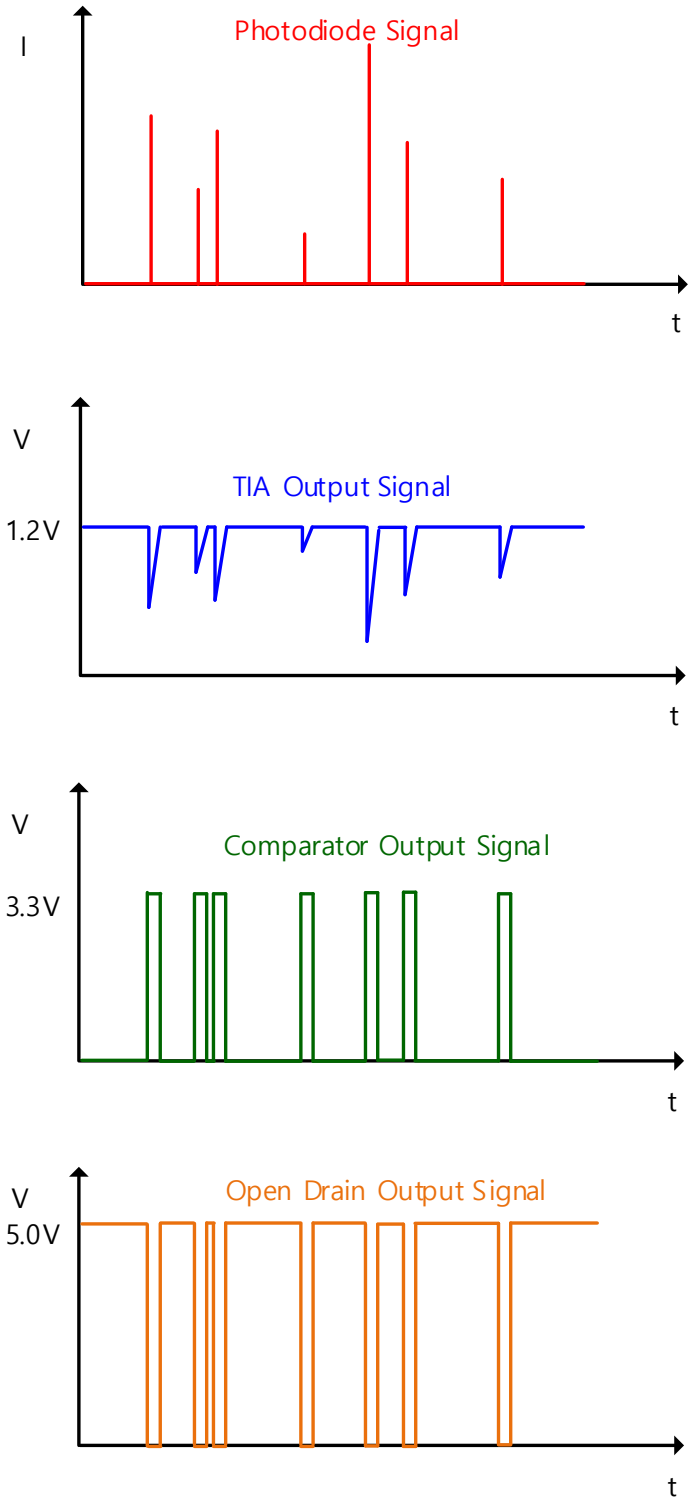

Figure 2. Input / Output Signal Features

Pin Description

Table 4. Pin Description

Pin No.	Pin Name	Type	Pin Position		Description
			X[um]	Y[um]	
1	VO_OD	DO	1357.5	213.5	5V interface pin. (Open drain NMOS)
2	VO_COMP	DO	1357.5	357.5	Comparator output pin.
3	VO_VREF	AO	1357.5	501.5	TIA reference voltage output pin.
4	AVSS33	AG	1357.5	645.5	Analog ground pin.
5	AVDD33	AP	1357.5	789.5	Analog power pin.
6	VO_TIA	AO	1357.5	933.5	2nd TIA output pin. (Gain amplifier output)
7	VO_TIA1	AO	1357.5	1077.5	1st TIA output pin.
8	AVSS33	AG	1077.5	1357.5	Analog ground pin.
9	AVDD33	AP	933.5	1357.5	Analog power pin.
10	PD_IN	AI	789.5	1357.5	Photodiode output pin. (1st TIA input)
11	VO_BGR	AO	645.5	1357.5	Bandgap reference voltage output pin.
12	AVSS33	AG	501.5	1357.5	Analog ground pin.
13	AVDD33	AP	357.5	1357.5	Analog power pin.
14	EN	DI	213.5	1357.5	Chip enable pin. (H=On, L=Off)

1) D = Digital, A = Analog, I = In, O = Out, P = Power, G = Ground

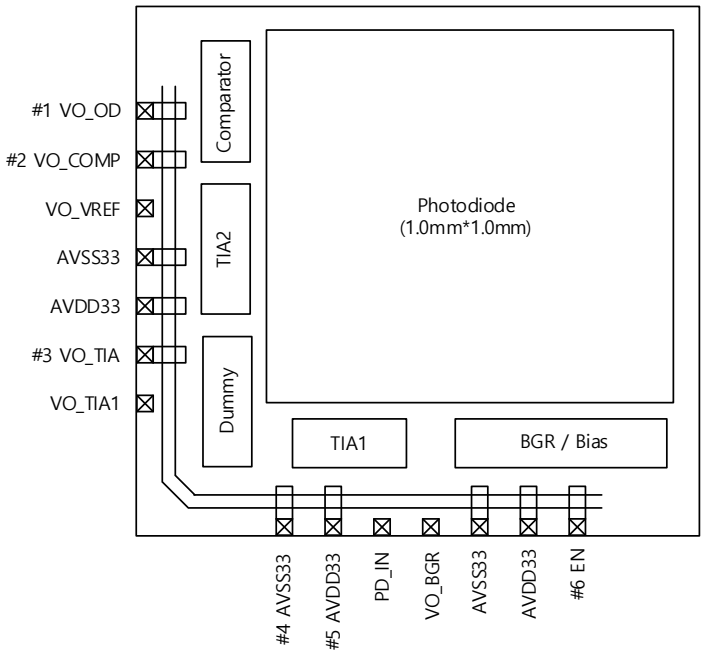

Figure 3. Pin Configuration

Revision History

Version	Date	Description
0.1	2018-07-04	Datasheet released