CSC510D Chip Preliminary Datasheet Sensor Applications

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1 Features

1.1 Core

- 32-bit Cortex-M0 processor core
- Up to 48 MHz operating frequency
- Single-cycle multiplication
- Included Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer
- Selectable core operating frequency among mid-frequency (8 MHz) and high-frequency (48 MHz)

The Cortex-M0 processor is a smallest gate count, highly energy efficient processor that is used for micro controller and area-optimized embedded applications. The processor supports ARM-v6 architecture, Thumb instruction sets, hardware multiplier and low latency interrupt response time.

1.2 On-chip Memory

- 32 KB on-chip Flash memory for instruction/data and option storage (calibration, 2 KB)
- 6 KB on-chip SRAM

The maximum address range of the Cortex-M0 is 4 GB since it has a 32-bit bus address width. A pre-defined memory map is provided by the Cortex-M0 processor to reduce the software complexity.

The memory map of the device is shows on Figure 2 in the chapter 1. It describes code and data (SRAM), peripheral and other pre-defined regions.

1.3 Flash Memory Controller - FMC

- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP) via SWD interface
- Also supports embedded on-chip flash memory erase/program/read operations via I2C interface.

1.4 ROIC Control Unit - ROICU

- Supports dedicated host interface (slave) for ROIC control unit.
- User can control most of functions of the device via I2C interface registers without MCU.
- Used for various ROIC operational mode change – ROIC IDLE/MCU/ATEST/FWUP mode.
- Supports ROIC/MCU/AFE control & testing operations.
- Supports MCU firmware update operations.
- Supports AFE trimming & trim results storing to flash.
- Supports Power-on Initial Process – AFE trim data read from flash (AUTORECALL), and MCU boot (AUTOBOOT).
- Supports I2C device address programming – 3-bit programming, device address[3:1], default address (0xC0).
- Supports Host-MCU communications – Transferring a user-defined command to MCU & Receiving a command processing results from MCU.

The ROIC Control Unit provides a method for controlling & testing AFE blocks, erasing or programming internal flash memory without MCU operation. By making I2C connection to ROIC unit, a user can do following tasks - initializing an internal flash, programming ROIC control flags & MCU firmware, and testing & trimming of analog components.

The ROIC control unit has control flags for controlling power-on boot sequence such as AUTORECALL, & AUTOBOOT. If you do not set any flags, the power-on default ROIC mode is ROIC IDLE mode. A user have to do initialization tasks for purpose of application.

1.5 Power on Reset Unit – APOR/DPOR

- Power on Reset for Analog block and Digital block (APOR/DPOR)
- Supports control registers by I2C interface.

1.6 Oscillator Control Unit – HF/MF/LFOSC

- Internal 48-MHz/8-MHz/32-kHz oscillator trimmed to ±2% accuracy at 25℃ operating temperature (HFOSC/MFOSC/LFOSC)
- 32 kHz clock is used for dual-input timer and watchdog timer.
- 8 MHz clock is used for ROIC control unit and MCU block.
- 8 MHz or 48 MHz clock is used for MCU block – Selectable System Clock.
- Supports control registers by I2C interface.

1.7 Power Control Unit – ALDO/DLDO

- Single power supply (HVDD): 1.8 V to 3.6 V (ALDO/DLDO)
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply.
- Automatic power control by ROIC operation mode change - ROIC IDLE/MCU/ATEST/FWUP mode
- Supports control registers by I2C interface.

1.8 24-Bit Delta-Sigma Analog-to-Digital Converter - DSADC

- Internal Programmable Gain Amplifier
- Internal I2C interface for external communication
- 4 kHz – 500 kHz ADC output data rate
- Internal temperature sensor for compensation

1.9 MCU System Control Unit - MSCU

- Two MCU power saving modes: Sleep/Deep-sleep
- Supports software RESET bit of MCU block and some peripheral block.
- Supports MCU main clock divisions (1/2, 1/4, 1/8).

The MCU parts has system control unit for the special configuration of MCU, which is software RESET setting, MCU main clock divider setting, and MCU power saving mode changing.

A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by debugger signal, ROICU signal, and internal events such as user software reset generation and watchdog event.

1.10 Host Interface Unit - HIFU

- Host-MCU communication block via I2C channel in ROIC control unit
- Supports internal flash access through the ROIC control unit
- Supports command pass and results return by registers that mapped into both ROIC control unit and MCU

The host interface unit supports both of master and slave access in the MCU AHB bus. It can make possible to access an internal bus by the ROIC control unit. Therefore, a user in the host side can access an internal flash or SRAM via ROIC control unit.

The HIFU supports interrupt generation and have own registers for receiving data from the host and for sending to the host. That registers are accessible both ROIC control unit and CPU.

1.11 ADC Control Unit - ADCU

- Supports accessing Internal ADC & Digital filter control registers.
- Supports ADC interrupt when raw ADC data received.

1.12 Internal Temperature Sensor Control Unit - ITSU

- Supports accessing Internal Temperature Sensor (ITS) control registers.
- Supports ITS interrupt when raw ITS data received.

1.13 I/O Ports - GPIO

- Eight GPIOs
- All of GPIO pins are mapped as 8 GPIO interrupts.
- GPIO2 and GPIO3 interrupts are shared with other interrupt signals (ADC and Internal Temperature Sensor interrupts).

There are 8 General Purpose I/O pins for the implementation of logic input/output functions. Each of the GPIO pins can be configured with a related control registers to use various user applications.

The GPIO pins are pin-multiplexed with other alternative functions for flexible usage of the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers.

1.14 Basic Function Timer - BFTM

- Two timers with system clock input
- 32-bit down-counter

Basic Timers is a very simple 32-bit down-counter in system clock domain. It generates interrupts counter values reaches 0. Initial value for the down-counter is stored in the RELOAD register before timer enabling.

1.15 Dual-input Timer - DUTM

- One dual-input timer with low-frequency (32 kHz) clock input, TIMCLK
- Two programmable 32-bit or 16-bit down-counters
- Timer operation mode
  - A 32-bit or a 16-bit counter
  - Free-running, Periodic, One-shot mode
- A pre-scale bits in control register controls count rates of each timers.

The Dual-input timer has three operational mode – free-running, periodic, and one-shot. In free-running mode the counters wraps after reaching its zero values, and continues to count down from maximum value. In periodic mode the counter generates an interrupt at a constant interval, reloading the original value after wrapping past zero. In one-shot mode the counter generates an interrupt once. When the counter reaches 0, it halts until you reprogram it.

1.16 Watchdog Timer - WDT

- 32-bit down-counter that is initialized from the reload register.
- Low-frequency clock input (32 kHz), WDOGCLK
- Reset event for the system
- Register lock function - disabling write access of WDT registers

The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes. You can enable or disable the watchdog unit as required.

The register lock function is a write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly. Writing a value of 0x1ACCE551 enables write access to all other registers. Writing any other value disables write accesses.

1.17 Universal Asynchronous Receiver Transmitter - UART

- Asynchronous serial communication with simple operating baud-rate divider setting
- Full duplex communication
- Programmable serial communication characteristics including:
  - Word length: 8-bit character
  - Parity: no-parity bit generation
  - Stop bit: 1 stop bit generation
- Error detection: full, overrun error

The UART provides a simple full duplex data communication and usually is used for RS232 communication. Typical usage of the UART is a serial print function for software debugging.

Before enabling the UART, you must program the baud rate divider register. For example, if the MCU is running at 48 MHz, and the required baud rate is 115200, program the baud rate divider register as $48 \times 10^6 / 115200 = 417$.

1.18 Debug Support

- Serial Wire Debug Port: SWD
- Four comparators for hardware breakpoint or code / literal patch
- Two comparators for hardware watch points

1.19 Operation Temperature

- Operation temperature range: -40℃ to +85℃

2 Overview

2.1 Device Information

Table 1 Features and Peripheral List

Peripherals		CSC510D
Main Flash (KB)		32
Option Bytes Flash (KB)		2
SRAM (KB)		6
Timers	BFTM	2
	DUTM	1
	WDT	1
Communication	UART	1
	I2C (slave)	1
24-bit ADC		1
Number of Channels		4 Channels
GPIO		8
CPU frequency		Up to 48 MHz
Operating Voltage		1.8 ~ 5.0 V
Operating Temperature		-40 ~ 85℃

2.2 Block Diagram

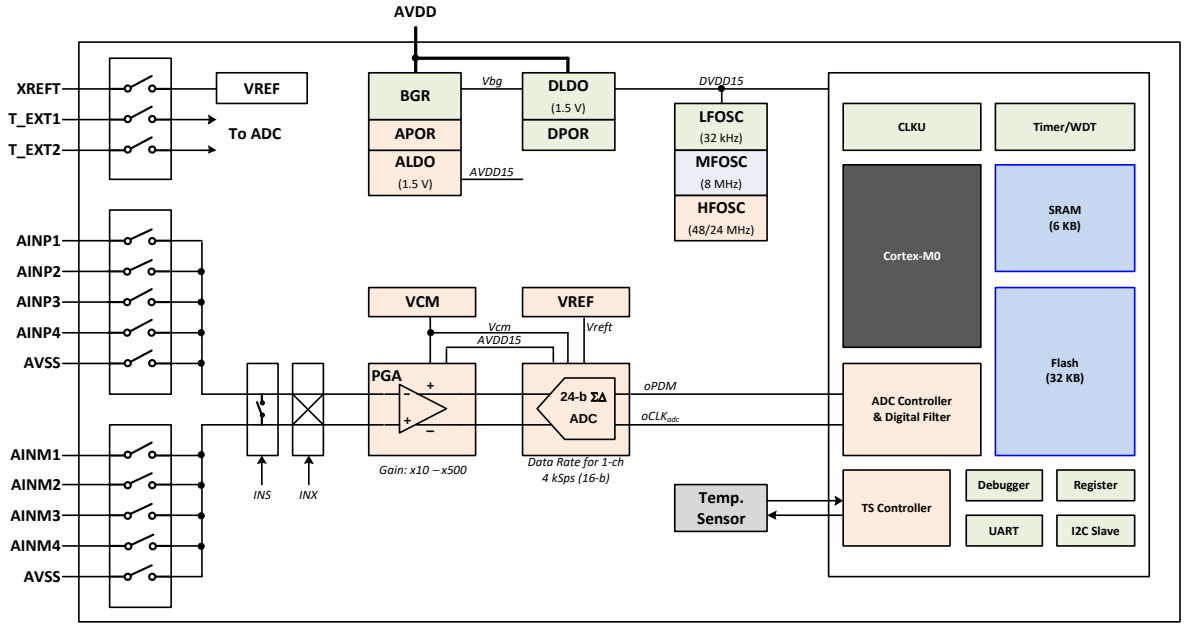

Figure 1 Block Diagram