ABOV SEMICONDUCTOR Co., Ltd.
8-BIT MICROCONTROLLERS

MC96F7816S
MC96F7616ST

Data Sheet (Ver. 1.10)

REVISION HISTORY

VERSION 0.0 (August 11, 2021)
VERSION 0.8 (December 13, 2021)
VERSION 0.9 (January 25, 2022)
VERSION 1.0 (February 25, 2022)
VERSION 1.1 (September 13, 2022)

Version 1.10
Published by FAE Team

Additional information of this manual may be served by ABOV Semiconductor offices in Korea or Distributors.

ABOV Semiconductor reserves the right to make changes to any information here in at any time without notice.

The information, diagrams and other data in this manual are correct and reliable; however, ABOV Semiconductor is in no way responsible for any violations of patents or other rights of the third party generated by the use of this manual.

Table of Contents

List of Figures

List of Tables

MC96F7816S

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 12-BIT A/D CONVERTER

1. Overview

1.1 Description

The MC96F7816S is advanced CMOS 8-bit microcontroller with 16Kbytes. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 16Kbytes of FLASH, 256bytes of IRAM, 256bytes of XRAM , general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, carrier generation, programmable pulse generation, 8-bit PWM output, watch timer, buzzer driving port, SIO, UART, 12-bit A/D converter, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F7816S also supports power saving modes to reduce power consumption.

Device Name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
MC96F7816SL	16Kbytes	256bytes	256bytes	8ch	71	80 LQFP
MC96F7616ST					55	64 TQFP

1.2 Features

- **CPU**
  - 8 Bit CISC Core (8051 Compatible)
- **ROM (FLASH) Capacity**
  - 16Kbytes
  - Flash with self read/write capability
  - On chip debug and In-system programming (ISP)
  - Endurance : 100,000 times
  - Retention : 10 years
- **256bytes IRAM**
- **256bytes XRAM**
  - (37bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 27 Ports
    (P0, P1, P2[7:4], P3[4:0], P9[3:2])
  - LCD shared I/O : 44 Ports
    (P2[3:0], P4, P5, P6, P7, P8)
- **Basic Interval Timer (BIT)**
  - 8Bit × 1ch
- **Watch Dog Timer (WDT)**
  - 8Bit × 1ch, 6kHz internal RC oscillator
- **Timer/ Counter**
  - 8Bit × 2ch (T0/T1), 16Bit x 2ch (T2/T3)
- **Carrier Generation**
  - Carrier Generation (by T1), T3 Clock source
- **Programmable Pulse Generation**
  - Pulse generation (by T2/T3)
- **PWM**
  - 8Bit × 1ch (by T0)
- **Watch Timer (WT)**
  - 3.91mS/0.25S/0.5S/1S/1M interval at 32.768kHz
- **Buzzer**
  - 8Bit × 1ch
- **SIO**
  - 8Bit × 1ch
- **UART**
  - 8Bit × 1ch
- **12 Bit A/D Converter**
  - 8 Input channels
- **LCD Driver**
  - 30 Segments and 8 Common terminals
  - Internal or external resistor bias
  - Capacitor bias (Voltage boost)
  - 16-step contrast control
  - Static, 2, 3, 4, 5, 6, and 8 duty selectable
  - 1/2, 1/3, and 1/4 bias selectable
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60V/ 2.00V/ 2.10V/ 2.20V/ 2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/ 3.67V/ 4.00V/ 4.40V)
- **Low Voltage Indicator**
  - 13 level detect (2.00V/ 2.10V/ 2.20V/ 2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/ 3.67V/ 4.00V/ 4.40V)
  - External reference detect
- **Interrupt Sources**
  - External Interrupts
    (EXINT0~7, EINT8, EINT10, EINT12, EINT13) (5)
  - Timer(0/1/2/3) (5)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SIO (1)
  - UART(TX/RX) (2)
  - ADC (1)
- **Internal RC Oscillator**
  - 4MHz ± 1.5% (T_A= 0°C ~ +70°C)
  - 4MHz ± 2.5% (T_A= -20°C ~ +85°C)
  - 4MHz ± 3.5% (T_A= -40°C ~ +85°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@ 32 ~ 38kHz)
  - 1.8V ~ 5.5V (@ 0.4 ~ 4.2MHz)
  - 2.7V ~ 5.5V (@ 0.4 ~ 10.0MHz)
  - 3.0V ~ 5.5V (@ 0.4 ~ 12.0MHz)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 167nS (@ 12MHz main clock)
  - 61μS (@t 32.768kHz sub clock)
- **Operating Temperature: – 40 ~ + 85℃**
- **Oscillator Type**
  - 0.4-12MHz crystal or ceramic for main clock
  - 32.768kHz crystal for sub clock
- **Package Type**
  - 80 LQFP-1212
  - 64 TQFP-0707

1.3 Ordering Information

Table 1-1 Ordering Information of MC96F7816

Device name	ROM size	IRAM size	XRAM size	Package
MC96F7816SL	16Kbytes	256bytes	256bytes	80 LQFP
MC96F7616ST				64 TQFP

1.4 Development Tools

1.4.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96F7816S is Mentor 8051. And, device ROM size is smaller than 64Kbytes. Developer can use all kinds of third party's standard 8051 compiler.

1.4.2 OCD emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- SCLK (MC96F7816S P23 port)
- SDATA (MC96F7816S P22 port)

OCD connector diagram: Connect OCD with user system

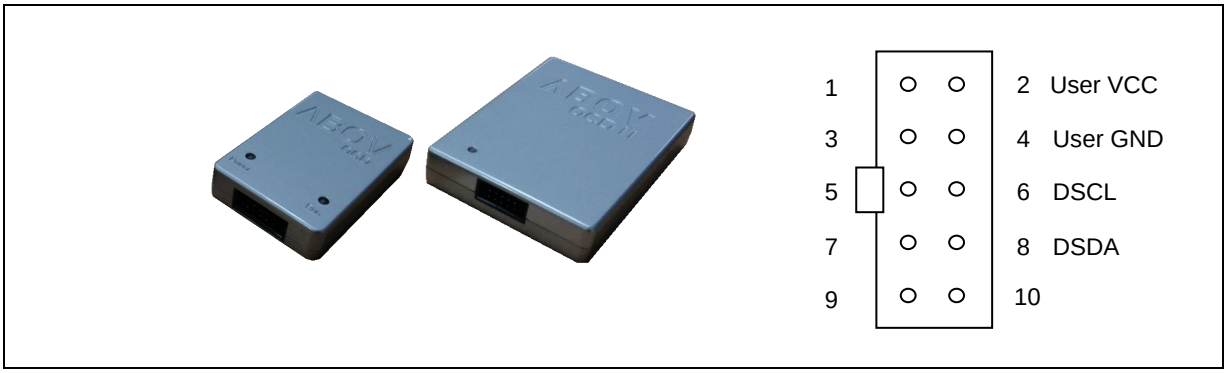


Figure 1.1 Debugger(OCD1/OCD2) and Pin description

1.4.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

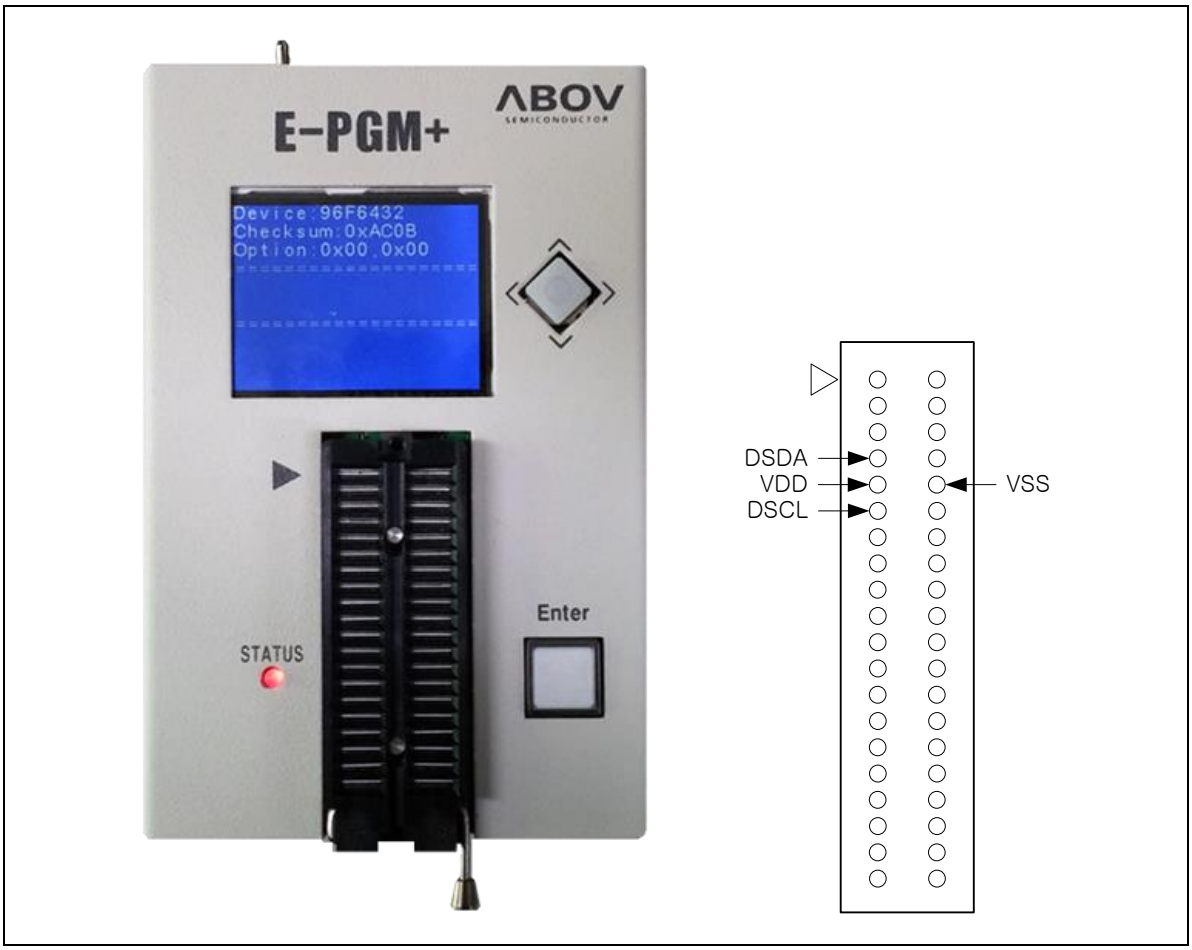


Figure 1.2 E-PGM+(Single writer)

OCD emulator: It can write code in MCU device too, because OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.3 E-GANG4 and E-GANG6 (for Mass Production)

2. Block Diagram

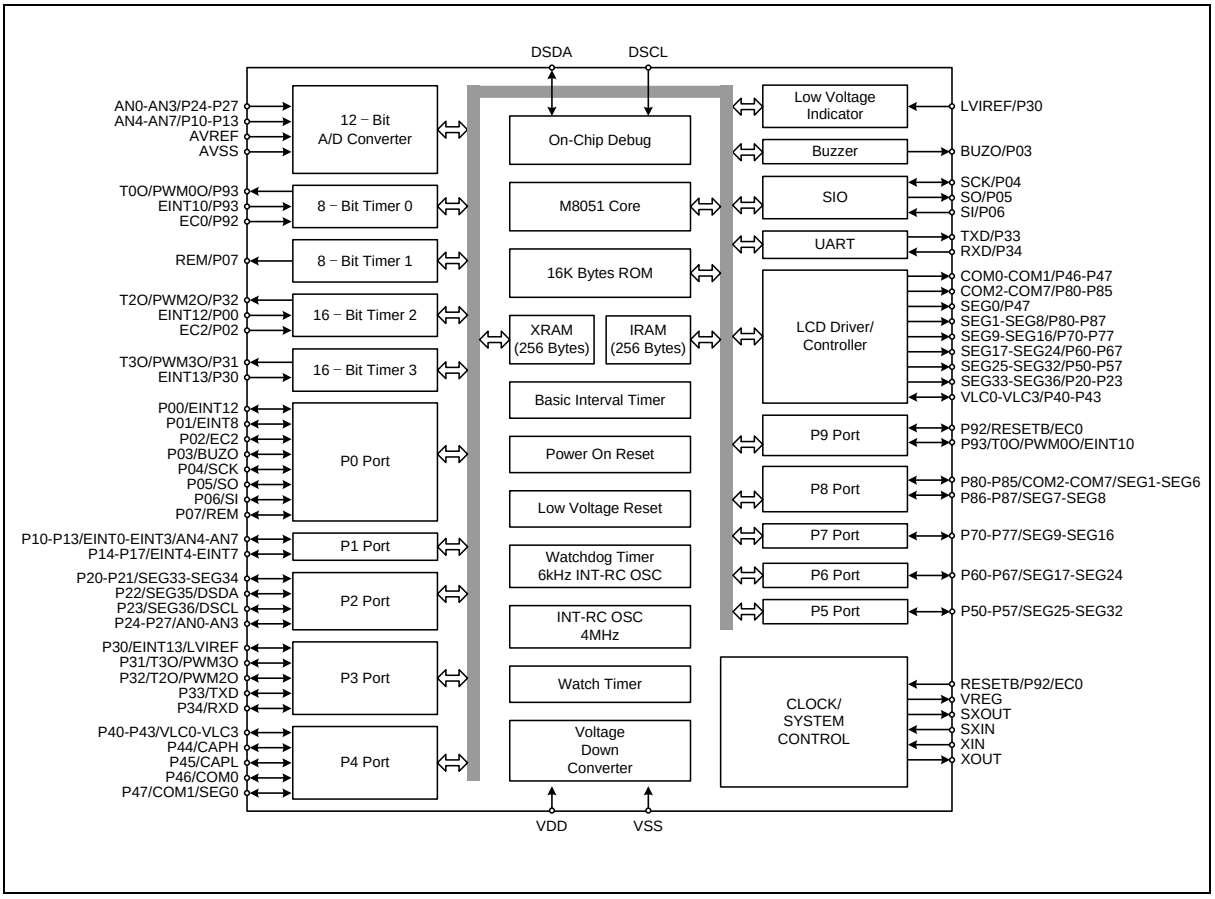


Figure 2.1 MC96F7816S Block Diagram

NOTE) The P20-P21, P30, P32, P34, P52-P57, P82-P85 and P93 are not in the 64-Pin package.

3. Pin Assignment

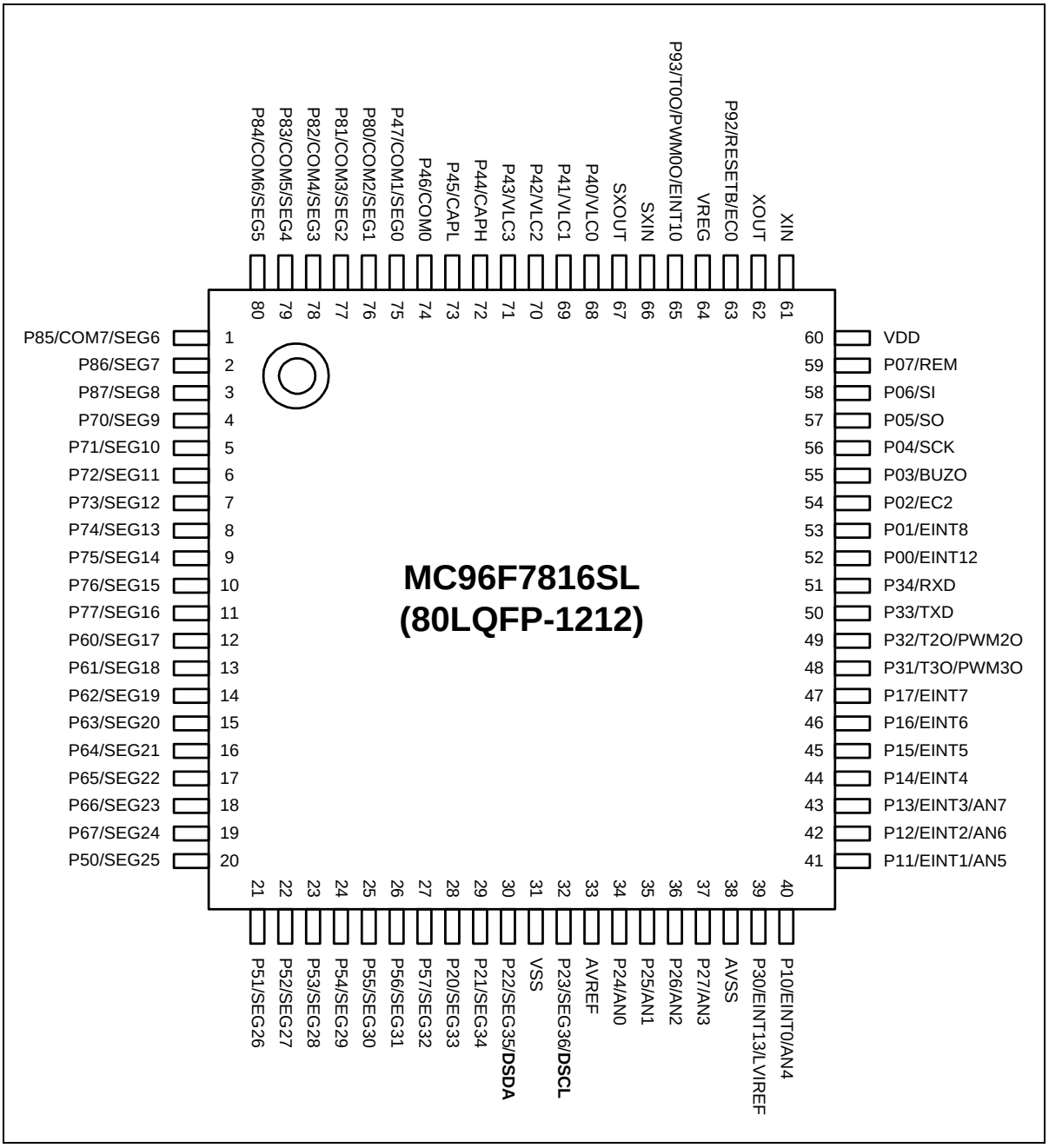


Figure 3.1 MC96F7816SL 80LQFP-1212 Pin Assignment

NOTE) On On-Chip Debugging, ISP uses P2[2:3] pin as DSDA, DSCL.

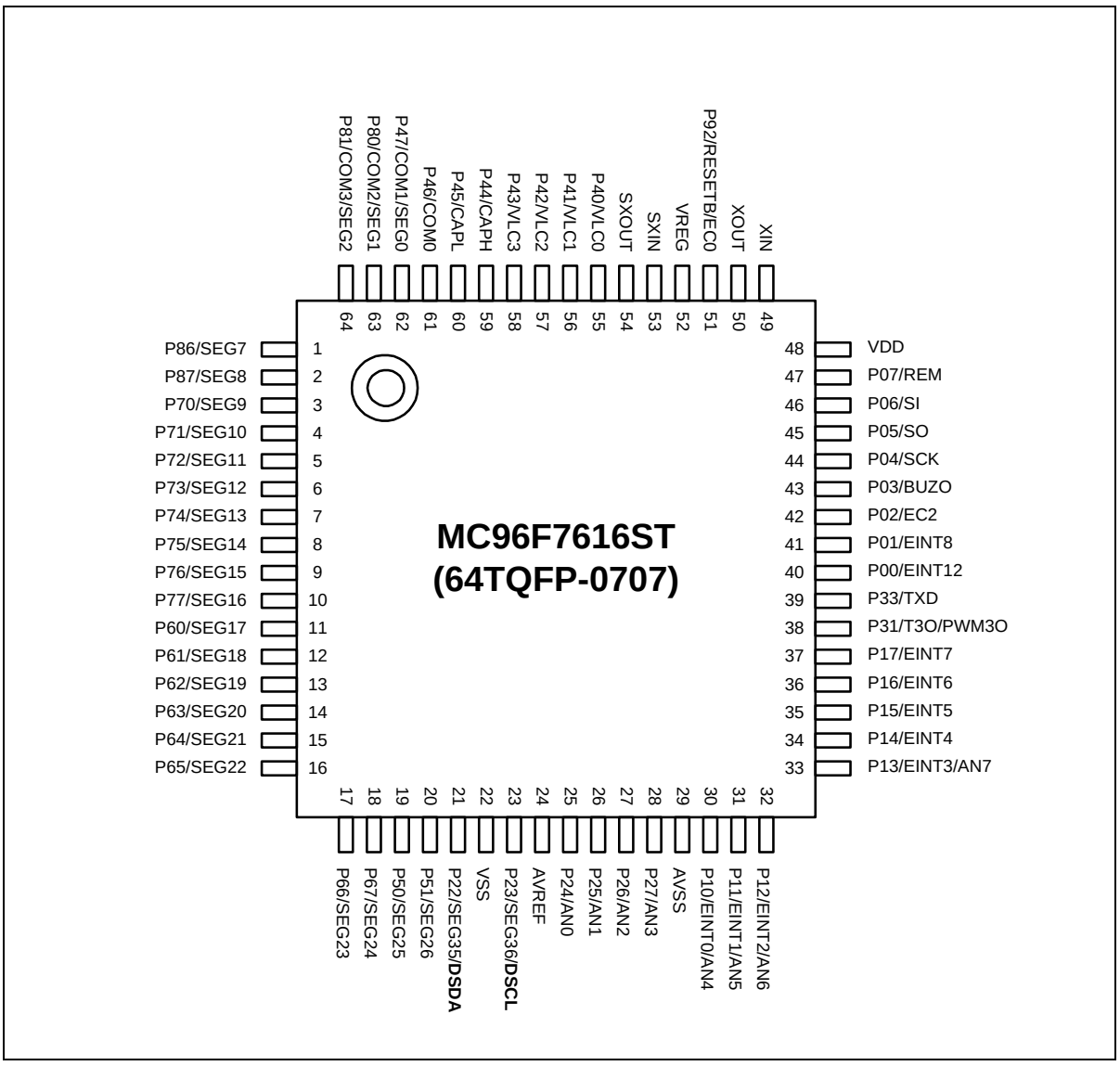
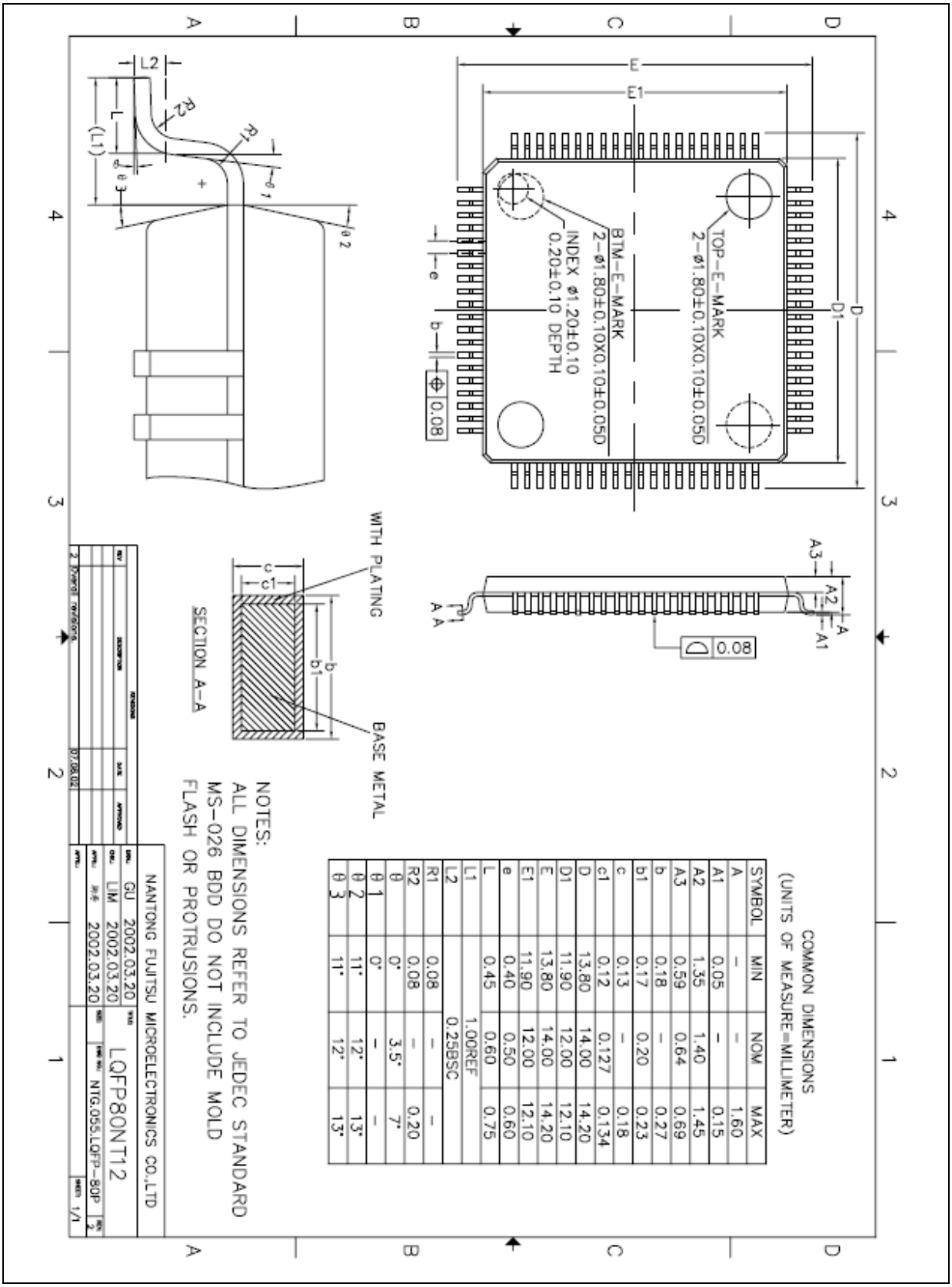


Figure 3.2 MC96F7616ST 64TQFP-0707 Pin Assignment

NOTES) 1. On On-Chip Debugging, ISP uses P2[2:3] pin as DSDA, DSCL.
2. The P20-P21, P30, P32, P34, P52-P57, P82-P85 and P93 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 64-pin package is used.

4. Package Diagram



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

Figure 4.1 80-Pin LQFP Package

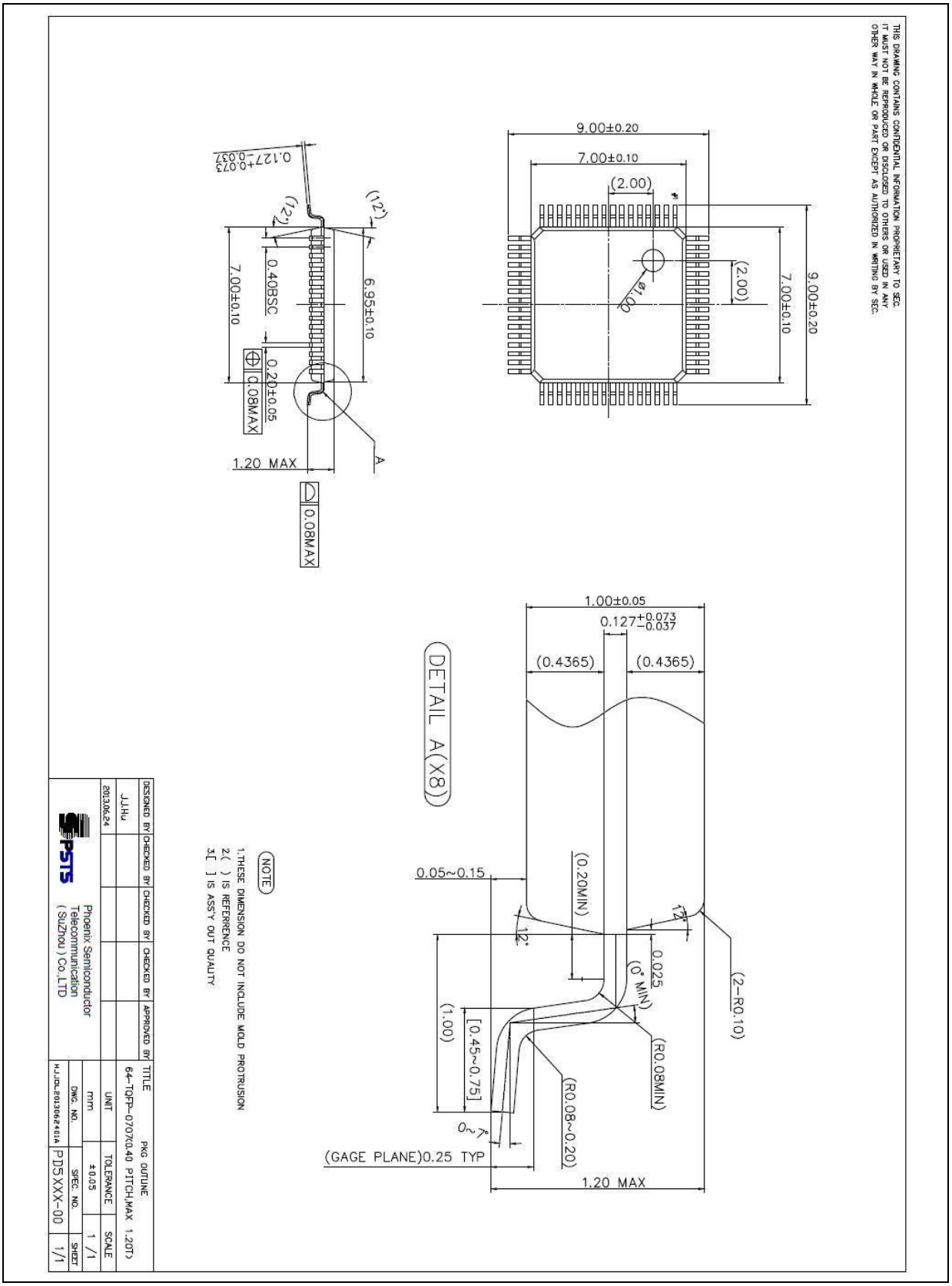


Figure 4.2 64-Pin TQFP Package

5. Pin Description

Table 5-1 Normal pin description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT12
P01				EINT8
P02				EC2
P03				BUZO
P04				SCK
P05				SO
P06				SI
P07				REM
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT0/AN4
P11				EINT1/AN5
P12				EINT2/AN6
P13				EINT3/AN7
P14				EINT4
P15				EINT5
P16				EINT6
P17				EINT7
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20 – P21 are not in the 64-Pin package.	Input	SEG33
P21				SEG34
P22				SEG35/DSDA
P23				SEG36/DSCL
P24				AN0
P25				AN1
P26				AN2
P27				AN3
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input (P30: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P30, P32 and P34 are not in the 64-Pin package.	Input	EINT13/LVIREF
P31				T3O/PWM3O
P32				T2O/PWM2O
P33				TXD
P34				RXD
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	VLC0
P41				VLC1
P42				VLC2
P43				VLC3
P44				CAPH
P45				CAPL
P46				COM0
P47				COM1/SEG0

Table 5-1 Normal pin description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P52 – P57 are not in the 64-Pin package.	Input	SEG25
P51				SEG26
P52				SEG27
P53				SEG28
P54				SEG29
P55				SEG30
P56				SEG31
P57				SEG32
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG17
P61				SEG18
P62				SEG19
P63				SEG20
P64				SEG21
P65				SEG22
P66				SEG23
P67				SEG24
P70	I/O	Port 7 is a bit-programmable I/O port which can be configured as an input or a push-pull output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG9
P71				SEG10
P72				SEG11
P73				SEG12
P74				SEG13
P75				SEG14
P76				SEG15
P77				SEG16
P80	I/O	Port 8 is a bit-programmable I/O port which can be configured as an input or a push-pull output. A pull-up resistor can be specified in 1-bit unit. The P82 – P85 are not in the 64-Pin package.	Input	COM2/SEG1
P81				COM3/SEG2
P82				COM4/SEG3
P83				COM5/SEG4
P84				COM6/SEG5
P85				COM7/SEG6
P86				SEG7
P87				SEG8
P92	I/O	Port 9 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit The P93 is not in the 64-Pin package.	Input	RESETB/EC0
P93				T0O/PWM0O/EINT10

Table 5-1 Normal pin description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P93/T0O/PWM0O
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P00
EINT13	I/O	External interrupt input and Timer 3 capture input	Input	P30/LVIREF
EINT0	I/O	External interrupt inputs	Input	P10/AN4
EINT1				P11/AN5
EINT2				P12/AN6
EINT3				P13/AN7
EINT4				P14
EINT5				P15
EINT6				P16
EINT7				P17
EINT8				P01
T0O	I/O	Timer 0 interval output	Input	P93/PWM0O/EINT10
T2O	I/O	Timer 2 interval output	Input	P32/PWM2O
T3O	I/O	Timer 3 interval output	Input	P31/PWM3O
REM	I/O	Carrier generation output	Input	P07
PWM0O	I/O	Timer 0 PWM output	Input	P93/T0O/EINT10
PWM2O	I/O	Timer 2 pulse output	Input	P32/T2O
PWM3O	I/O	Timer 3 pulse output	Input	P31/T3O
EC0	I/O	Timer 0 event count input	Input	P92/RESETB
EC2	I/O	Timer 2 event count input	Input	P02
BUZO	I/O	Buzzer signal output	Input	P03
SCK	I/O	Serial clock input/output	Input	P04
SO	I/O	Serial data output	Input	P05
SI	I/O	Serial data input	Input	P06
TXD	I/O	UART data output	Input	P33
RXD	I/O	UART data input	Input	P34
AN0–AN3	I/O	A/D converter analog input channels	Input	P24–P27
AN4–AN7				P10/EINT0– P13/EINT3
LVIREF	I/O	Low Voltage Indicator reference voltage	Input	P30/EINT13
VLC0– VLC3	I/O	LCD bias voltage pins	Input	P40–P43
CAPH	I/O	Capacitor terminals for voltage booster	Input	P44
CAPL				P45
COM0	I/O	LCD common signal output	Input	P46
COM1				P47/SEG0
COM2– COM7				P80/SEG1– P85/SEG6

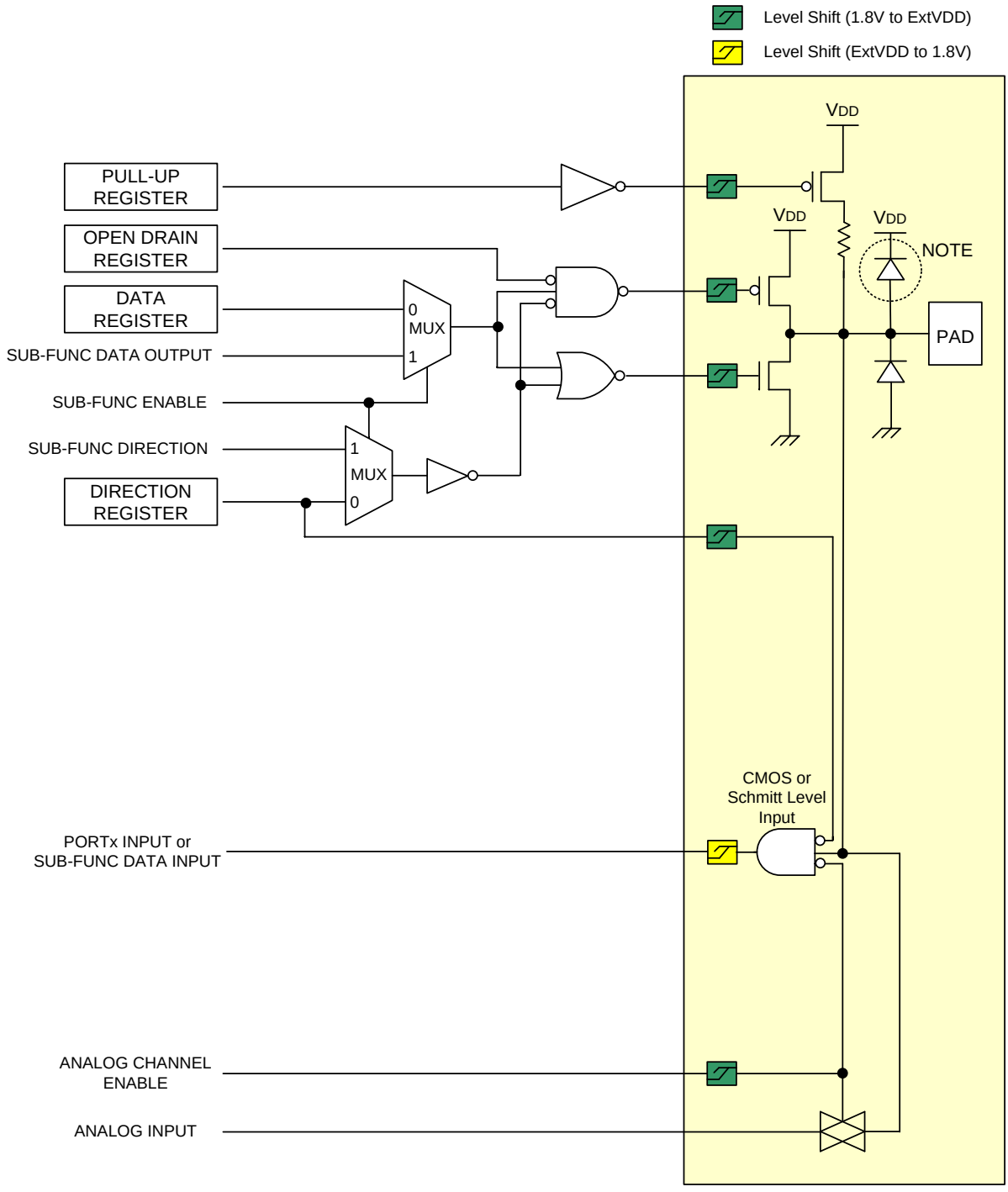
Table 5-1 Normal pin description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
SEG0	I/O	LCD segment signal output	Input	P47/COM1
SEG1–SEG6				P80/COM2–P85/COM7
SEG7–SEG8				P86–P87
SEG9–SEG16				P70–P77
SEG17–SEG24				P60–P67
SEG25–SEG32				P50–P57
SEG33–SEG34				P20–P21
SEG35				P22/DSDA
SEG36				P23/DSCL
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION”	Input	P92/EC0
DSDA	I/O	On chip debugger data input/output(NOTE2,3)	Input	P22/SEG35
DSCL	I/O	On chip debugger clock input(NOTE2,3)	Input	P23/SEG36
XIN, XOUT	I/O	Main oscillator pins	Input	–
SXIN, SXOUT	I/O	Sub oscillator pins	Input	–
VREG	–	Regulator voltage output for sub clock 0.1μF capacitor needed	–	–
AVREF	–	A/D converter reference voltage	–	–
AVSS	–	A/D converter ground	–	–
VDD, VSS	–	Power input pins	–	–

Notes) 1. The P20-P21, P30, P32, P34, P52-P57, P82-P85 and P93 are not in the 64-Pin package.
2. The P92/RESETB/EC0 pin is configured as one of the P92/EC0 and the RESETB pin by the “CONFIGURE OPTION”.
3. If the P22/SEG35/DSDA and P23/SEG36/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
4. The P22/SEG35/DSDA and P23/SEG36/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.

6. Port Structures

6.1 General Purpose I/O Port

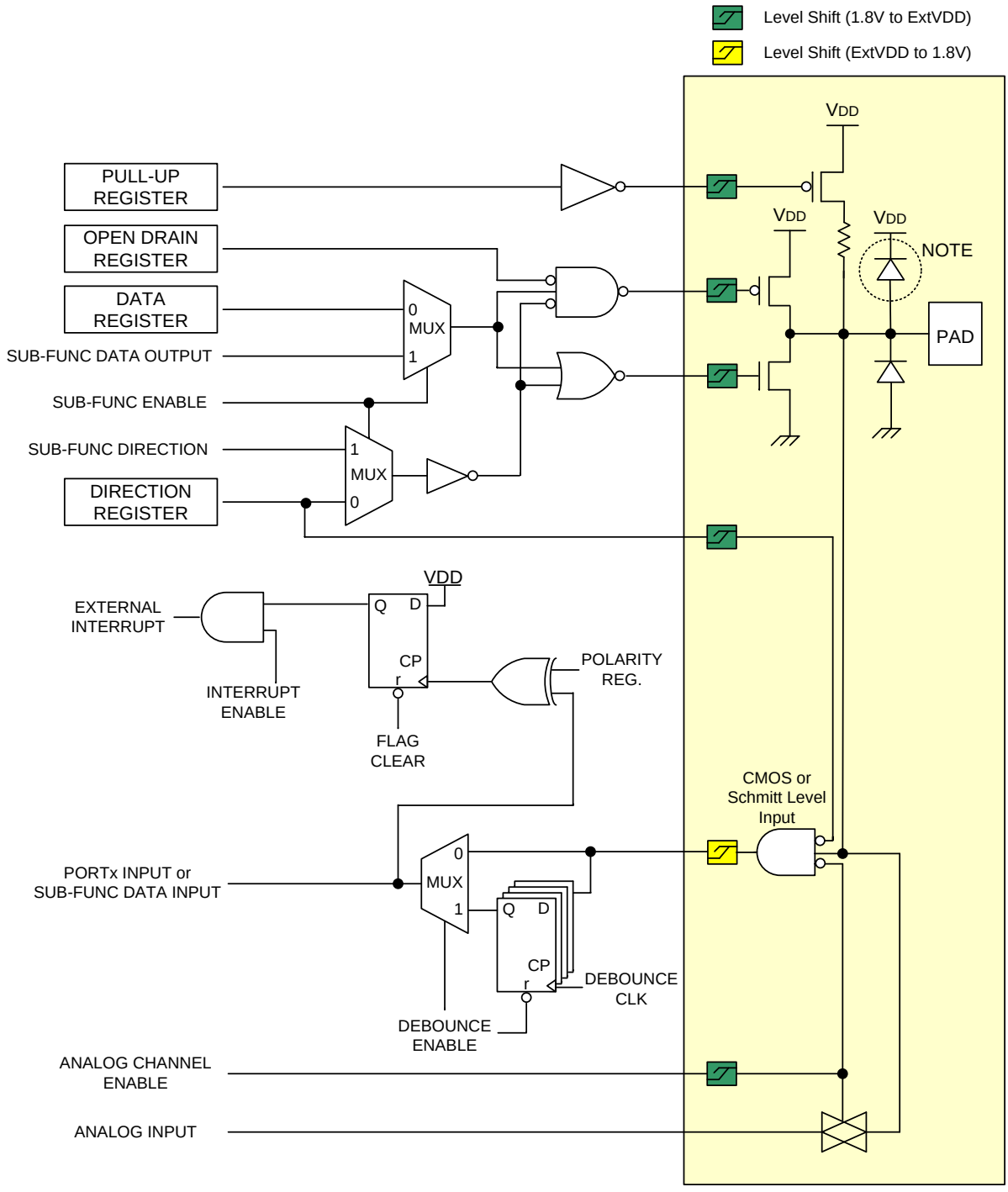


Note)

The P20-P23, P40-P47, P50–P57, P60-P67, P70-P77 and P80-P87 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port



Note)

The P20-P23, P40-P47, P50–P57, P60-P67, P70-P77 and P80-P87 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

Figure 6.2 External Interrupt I/O Port

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

Note) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Table 7-2 Recommended Operating Conditions

(T_A= -40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Supply Voltage	VDD	f_X= 32 ~ 38kHz	SX-tal	1.8	–	5.5	V
		f_X= 0.4 ~ 4.2MHz	X-tal, Internal RC	1.8	–	5.5	
		f_X= 0.4 ~ 10.0MHz		2.7	–	5.5	
		f_X= 0.4 ~ 12.0MHz		3.0	–	5.5	
Operating Temperature	T_{OPR}	VDD= 1.8 ~ 5.5V		-40	–	85	°C

7.3 A/D Converter Characteristics

Table 7-3 A/D Converter Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–-	12	–	bit
Integral Non-Linear	INL	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±4	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±3	
Zero Offset Error	ZOE			–	–	±3	
Conversion Time	t_{CONV}	12bit resolution, fx=8MHz		20	–	–	us
Analog Input Voltage	V_{AIN}	–		AVSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		1.8	–	VDD	
Analog Ground Voltage	AVSS	–		VSS	–	VSS+0.3	
Analog Input Leakage Current	I_{AIN}	AVREF= 5.12V		–	–	10	uA
ADC Operating Current	I_{ADC}	Enable	VDD = 5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Notes) 1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage(VSS);

2. Top offset error is the difference between 111111111111 and the converted output for top input voltage (AVREF)

3. When AVREF is lower than 2.7V, the ADC resolution is worse.

7.4 Power-On Reset Characteristics

Table 7-4 Power-On Reset Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

Table 7-5 LVR and LVI Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V.		–	1.60	1.75	V
				1.85	2.00	2.15	
				1.95	2.10	2.25	
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
Hysteresis	△V	–		–	10	100	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V	–	8.0	14.0	uA
		Enable (One of two)		–	6.0	12.0	
		Disable (Both)		–	–	0.1	

7.6 Internal RC Oscillator Characteristics

Table 7-6 Internal RC Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	–		–	4.0	–	MHz
Tolerance	–	VDD= 2.0V – 5.5V	T_A= 0°C – +70°C	-1.5	–	+1.5	%
			T_A= -20°C – +85°C	-2.5	–	+2.5	%
			T_A= -40°C – +85°C	-3.5	–	+3.5	%
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	t_{WDTS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.5	–	mA
		Disable		–	–	0.1	uA

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

Table 7-7 Internal WDTRC Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	3	6	9	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

7.8 LCD Voltage Characteristics

Table 7-8 LCD Voltage Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD Voltage	VLC3	Voltage booster enabled, 1/2,1/3 bias	LCDCCR=0000b	**Typx0.9**	1.000	**Typx1.1**	V
			LCDCCR=0001b		1.045		
			LCDCCR=0010b		1.090		
			LCDCCR=0011b		1.135		
			LCDCCR=0100b		1.180		
			LCDCCR=0101b		1.225		
			LCDCCR=0110b		1.270		
			LCDCCR=0111b		1.315		
			LCDCCR=1000b		1.360		
			LCDCCR=1001b		1.405		
			LCDCCR=1010b		1.450		
			LCDCCR=1011b		1.500		
			LCDCCR=1100b		1.550		
			LCDCCR=1101b		1.600		
			LCDCCR=1110b		1.650		
			LCDCCR=1111b		1.700		
LCD Mid Bias Voltage	VLC0/1/2	Voltage booster enabled, 1/2 bias, No panel load, VDD=3V		Typx0.9	2xVLC3	Typx1.1	V
	VLC0/1	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V		Typx0.9	3xVLC3	Typx1.1	V
	VLC2			Typx0.9	2xVLC3	Typx1.1	
	VLC1	Voltage booster disabled, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, VLC0=VDD		Typx0.95	0.75xVDD	Typx1.05	V
	VLC2			Typx0.95	0.5xVDD	Typx1.05	
	VLC3			Typx0.95	0.25xVDD	Typx1.05	
LCD Driver Output Impedance	RLO	VLCD=3V, ILOAD=±10uA		–	5	10	kΩ
LCD Bias Dividing Resistor	RLCD	Internal resistor mode, T_A = 25°C		40	60	80	
LCD Block Current	ILCD	Voltage booster mode, VDD=3V, VLCD=3.15V, 1/3Bias		–	3	6	uA

Note) It is middle output voltage when the VDD and the V_{LC0} node are connected in the case of resister bias.

Table 7-8 LCD Voltage Characteristics(Condinued)

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD Voltage	VLC3	Voltage booster enabled, 1/4 bias	LCDCCR=0000b	**Typx0.9**	0.856	**Typx1.1**	V
			LCDCCR=0001b		0.887		
			LCDCCR=0010b		0.918		
			LCDCCR=0011b		0.949		
			LCDCCR=0100b		0.980		
			LCDCCR=0101b		1.011		
			LCDCCR=0110b		1.052		
			LCDCCR=0111b		1.073		
			LCDCCR=1000b		1.104		
			LCDCCR=1001b		1.135		
			LCDCCR=1010b		1.166		
			LCDCCR=1011b		1.197		
			LCDCCR=1100b		1.228		
			LCDCCR=1101b		1.259		
			LCDCCR=1110b		1.290		
			LCDCCR=1111b		1.321		
LCD Mid Bias Voltage	VLC0	Voltage booster enabled, 1/4 bias, No panel load, VDD=3V		Typx0.9	4xVLC3	Typx1.1	V
	VLC1			Typx0.9	3xVLC3	Typx1.1	
	VLC2			Typx0.9	2xVLC3	Typx1.1	

Note) It is middle output voltage when the VDD and the V_{LC0} node are connected in the case of resister bias.

7.9 DC Characteristics

Table 7-9 DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0x, P1x, P30, P9x, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0x, P1x, P30, P9x, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD= 4.5V, I_{OH}= -2mA; All output ports except V_{OH2};		VDD-1.0	–	–	V
	V_{OH2}	VDD= 3.0V, I_{OH}= -10mA; P07		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD= 4.5V, I_{OL}= 15mA; All output ports		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
OSC Feedback Resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25°C ,VDD=5V		1750	3500	7000	
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz, VDD= 5V±10%		–	3.0	6.0	mA
		f_{XIN}= 10MHz, VDD= 3V±10%		–	2.2	4.4	
		f_{IRC}= 4MHz, VDD= 5V±10%		–	1.4	2.8	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz, VDD= 5V±10%		–	2.0	4.0	mA
		f_{XIN}= 10MHz, VDD= 3V±10%		–	1.3	2.6	
		f_{IRC}= 4MHz, VDD= 5V±10%		–	0.6	1.2	
	I_{DD3}	f_{SUB}= 32.768kHz VDD= 3V±10% T_A= 25°C,PSAVE=1	Sub RUN	–	50.0	80.0	uA
	I_{DD4}		Sub IDLE	–	4.0	8.0	uA
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	3.0	uA

Notes) 1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{IRC} is an internal RC oscillator, and the fx is the selected system clock.

2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.

3. All supply current items include the current of the power-on reset (POR) block.

7.10 AC Characteristics

Table 7-10 AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB Input Low Width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt Input High, Low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5 V (n=0, 2)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5 V (n=0, 2)	20	–	–	

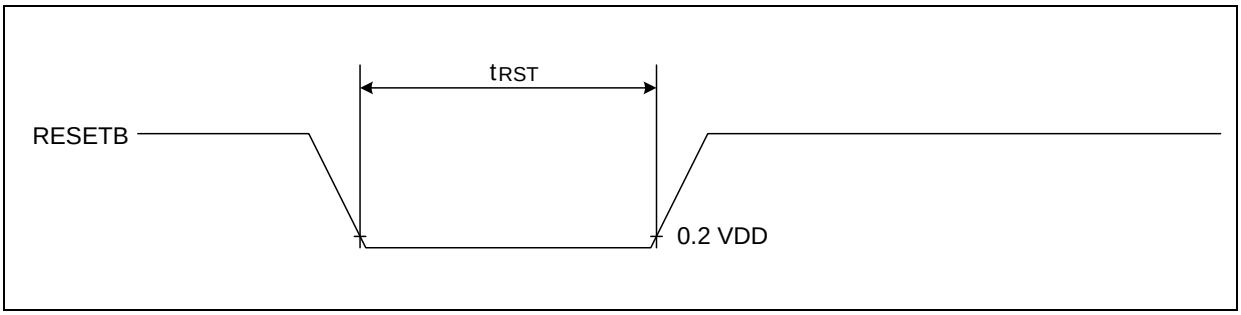


Figure 7.1 Input Timing for RESETB

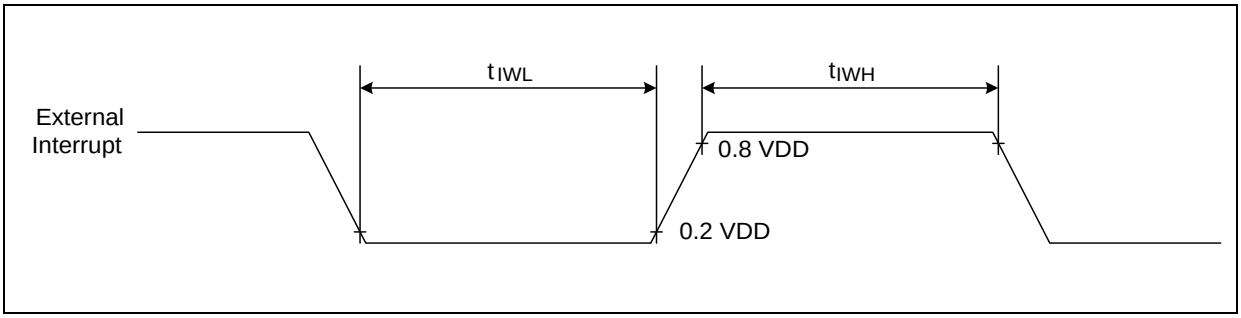


Figure 7.2 Input Timing for External Interrupts

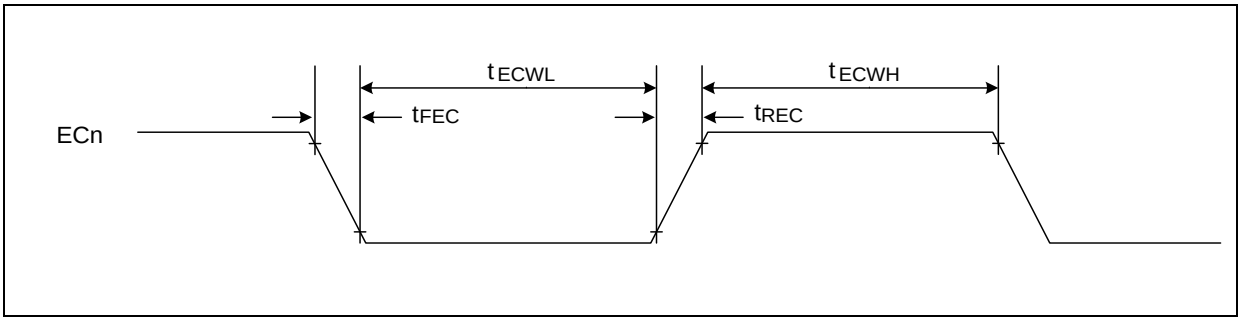


Figure 7.3 Input Timing for EC0, EC2

7.11 Serial I/O Characteristics

Table 7-11 Serial I/O Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCK Cycle Time	t_{KCY}	External SCK source	1,000	–	–	ns
		Internal SCK source	1,000			
SCK High, Low width	t_{KH}, t_{KL}	External SCK source	500			ns
		Internal SCK source	t_{KCY}/2-50			
SI Setup Time to SCK High	t_{SIK}	External SCK source	250			ns
		Internal SCK source	250			
SI Hold Time to SCK High	t_{KSI}	External SCK source	400			ns
		Internal SCK source	400			
Output Delay for SCK to SO	t_{KSO}	External SCK source	–	–	300	ns
		Internal SCK source			250	

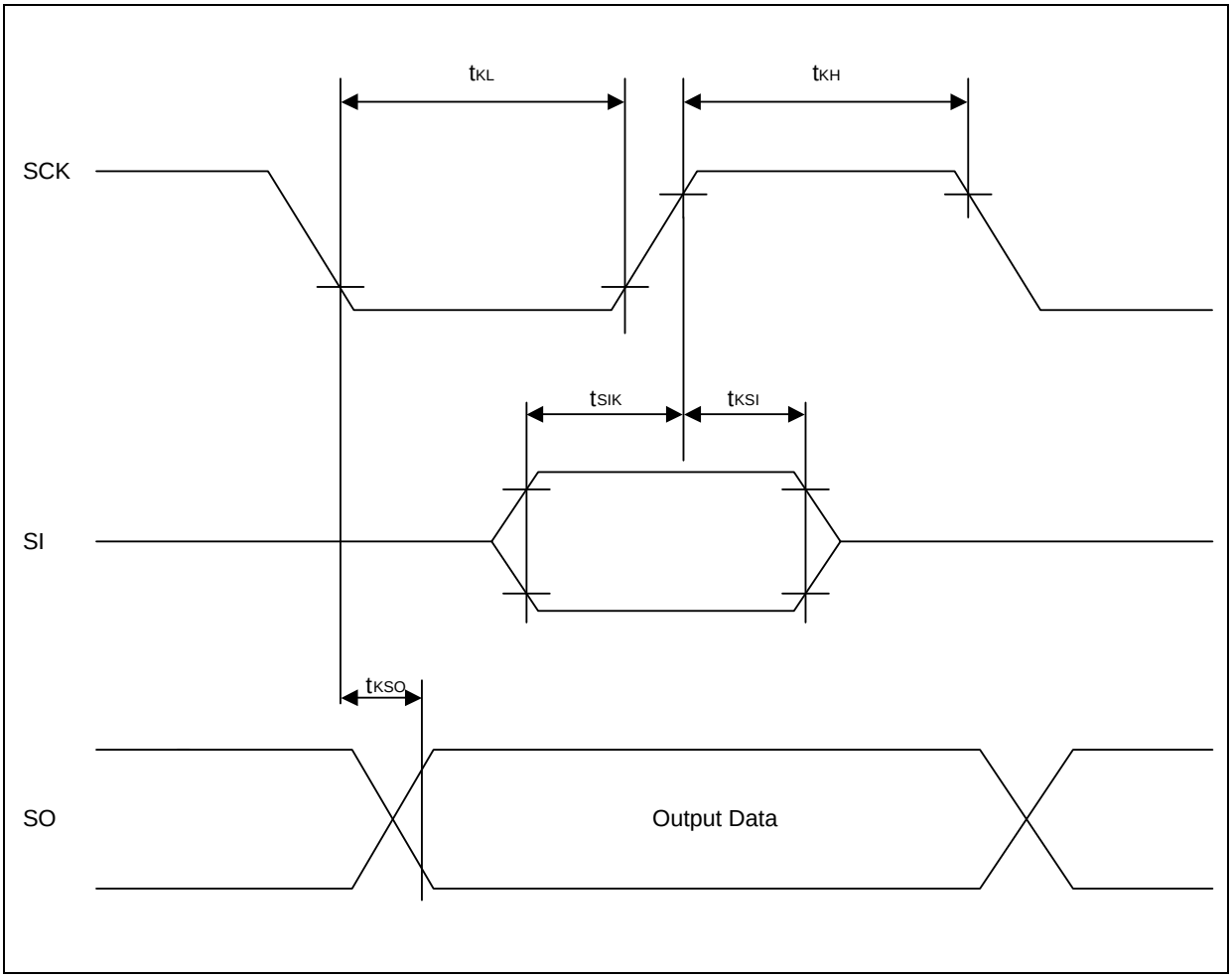


Figure 7.4 Serial Interface Data Transfer Timing

7.12 UART Characteristics

Table 7-12 UART Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial Port Clock Cycle Time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output Data Setup to Clock Rising Edge	t_{S1}	590	t_{CPU} x 13	–	ns
Clock Rising Edge to Input Data Valid	t_{S2}	–	–	590	ns
Output Data Hold after Clock Rising Edge	t_{H1}	t_{CPU} - 50	t_{CPU}	–	ns
Input Data Hold after Clock Rising Edge	t_{H2}	0	–	–	ns
Serial Port Clock High, Low Level Width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	ns

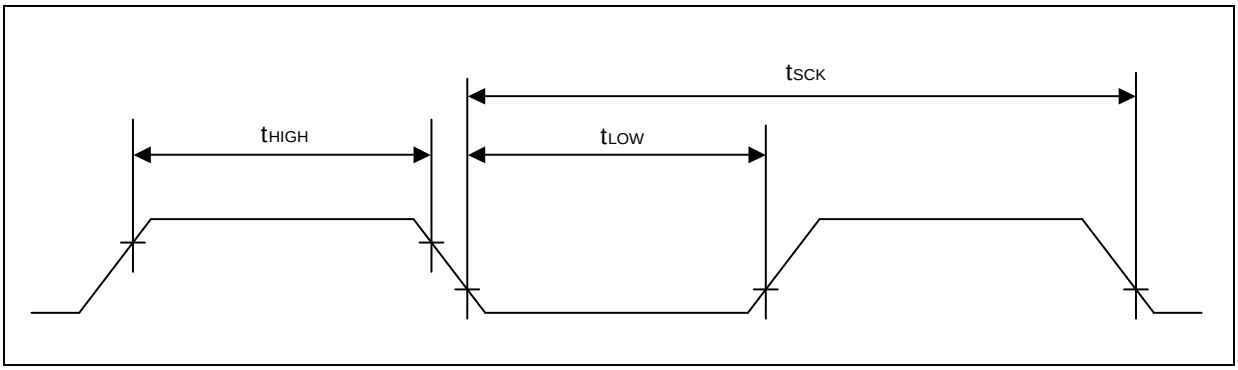


Figure 7.5 Waveform for UART Timing Characteristics

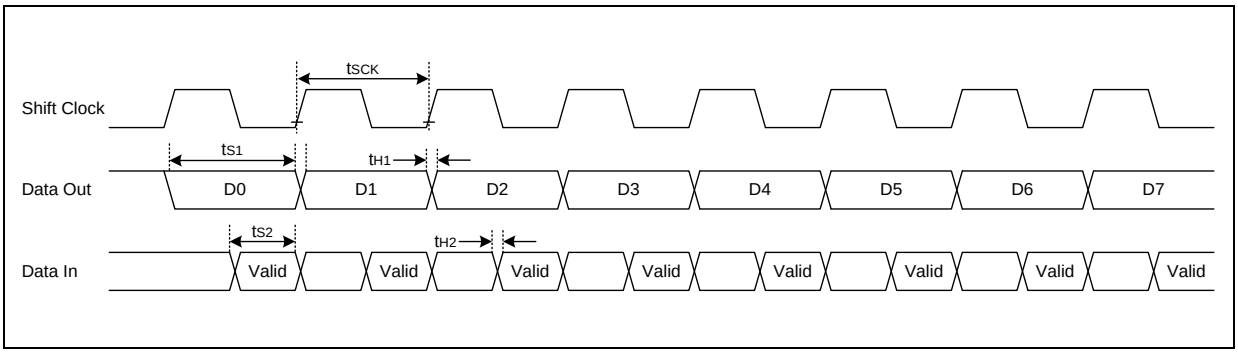


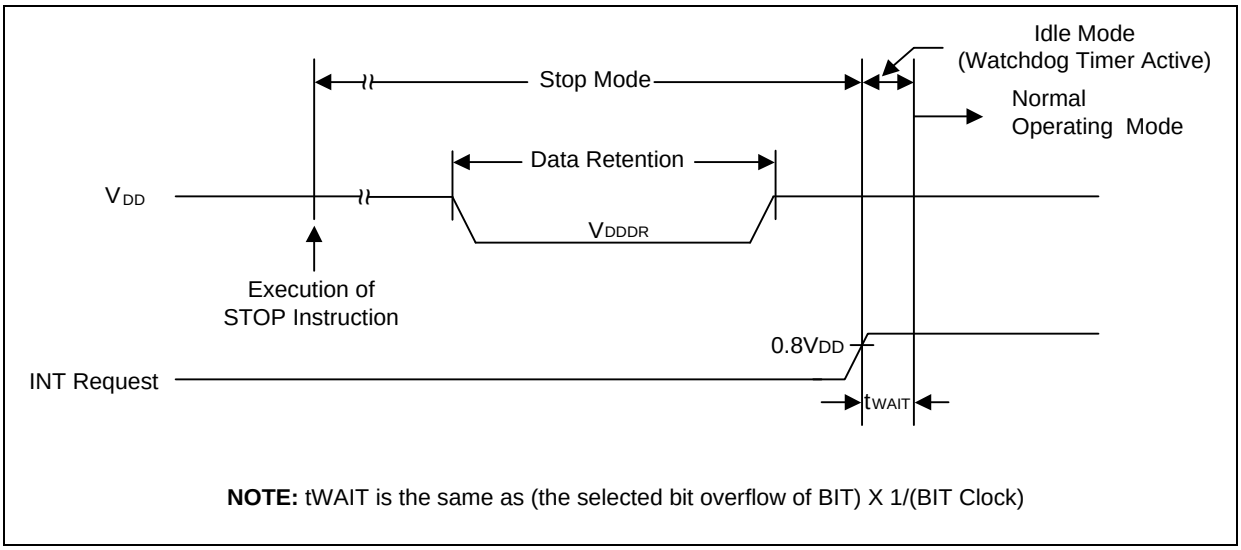
Figure 7.6 Timing Waveform for the UART Module

7.13 Data Retention Voltage in Stop Mode

Table 7-13 Data Retention Voltage in Stop Mode

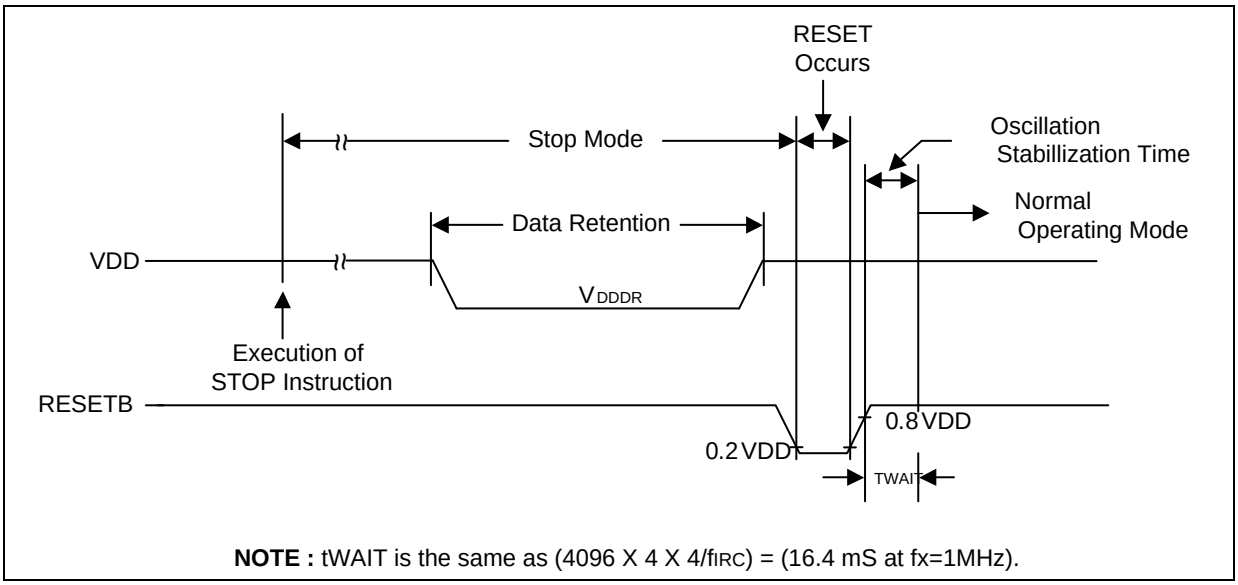
(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data Retention Supply Voltage	V_{DDDR}	–	1.8	–	5.5	V
Data Retention Supply Current	I_{DDDR}	VDDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.7 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 4/f_{IRC}) = (16.4 mS at fx=1MHz).

Figure 7.8 Stop Mode Release Timing when Initiated by RESETB

7.14 Internal Flash Rom Characteristics

Table 7-14 Internal Flash Rom Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	100,000	Times
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

Note) During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.15 Input/Output Capacitance

Table 7-15 Input/Output Capacitance

(T_A= -40°C ~ +85°C, VDD= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

7.16 Main Clock Oscillator Characteristics

Table 7-16 Main Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main Oscillation Frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main Oscillation Frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	
External Clock	XIN Input Frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	

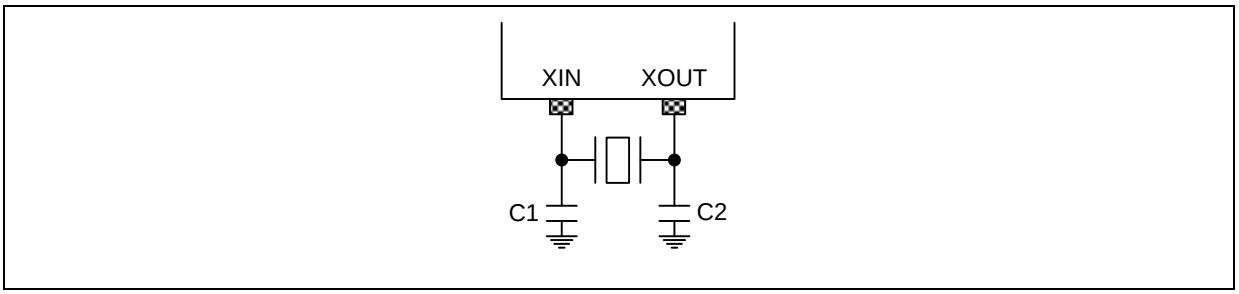


Figure 7.9 Crystal/Ceramic Oscillator

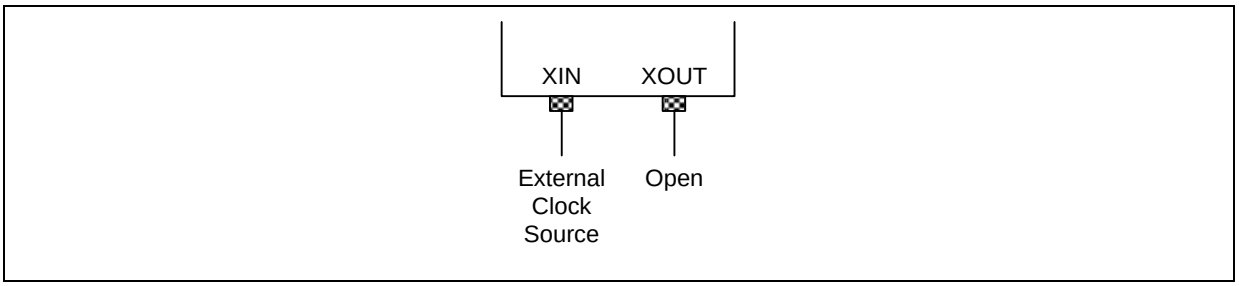


Figure 7.10 External Clock

7.17 Sub Clock Oscillator Characteristics

Table 7-17 Sub Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

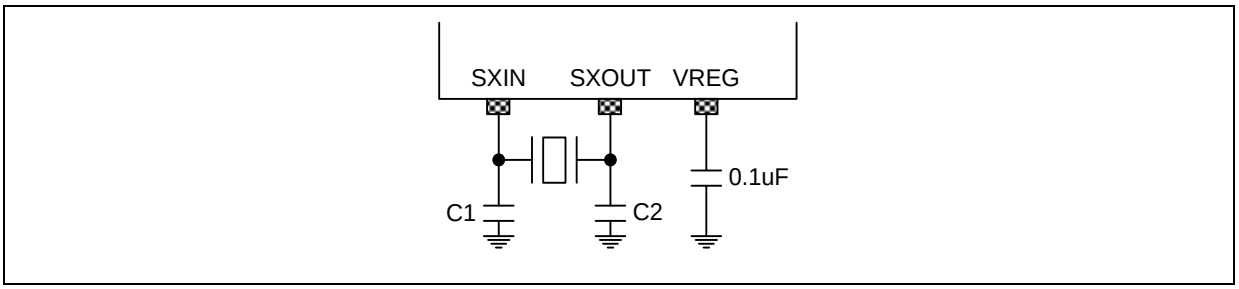


Figure 7.11 Crystal Oscillator

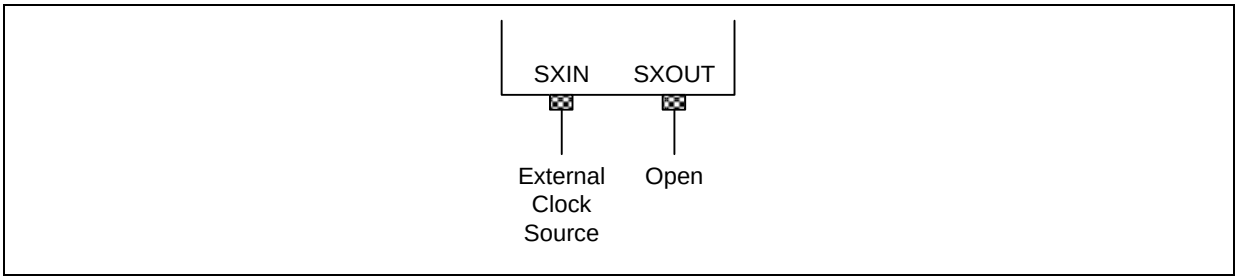


Figure 7.12 External Clock

7.18 Main Oscillation Stabilization Characteristics

Table 7-18 Main Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 1MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	f_{XIN} = 0.4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

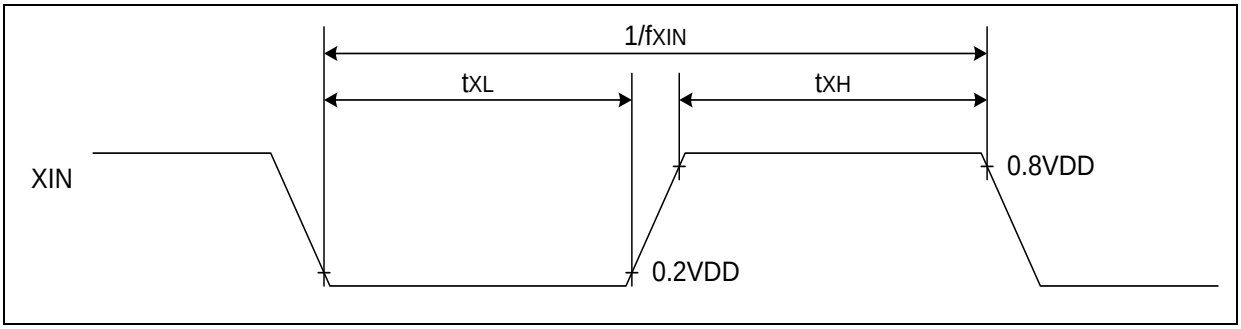


Figure 7.13 Clock Timing Measurement at XIN

7.19 Sub Oscillation Characteristics

Table 7-19 Sub Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN Input High and Low Width (t_{XH}, t_{XL})	5	–	15	us

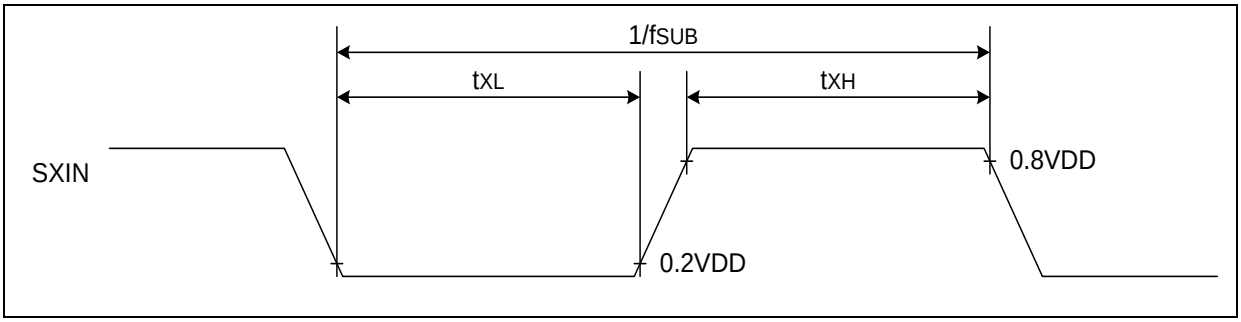


Figure 7.14 Clock Timing Measurement at SXIN

7.20 Operating Voltage Range

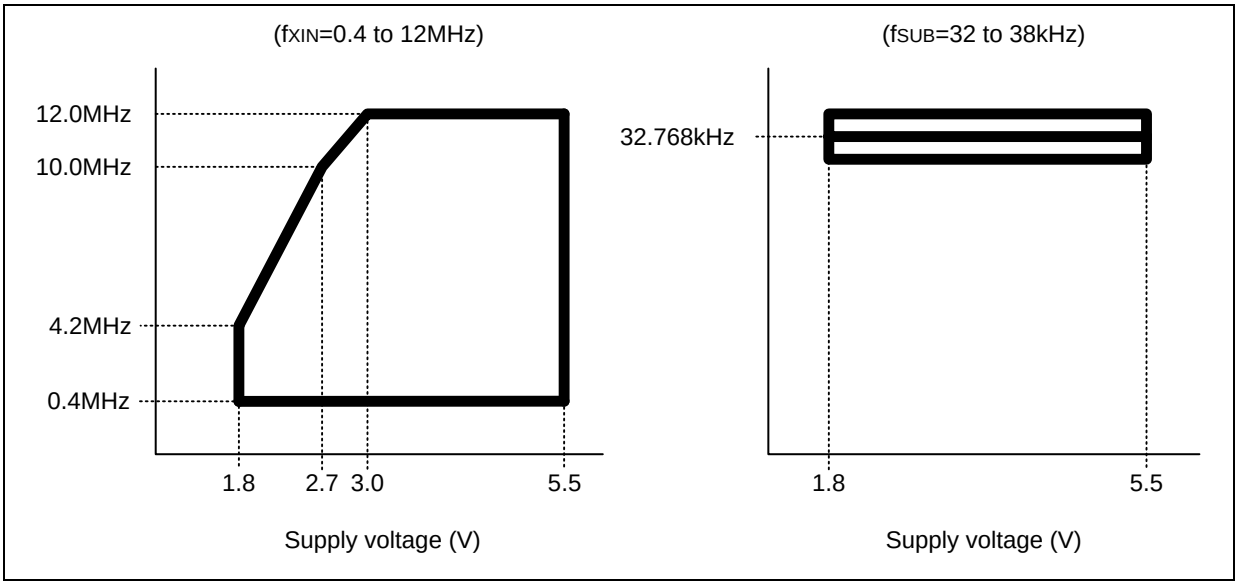


Figure 7.15 Operating Voltage Range

7.21 Recommended Circuit and Layout

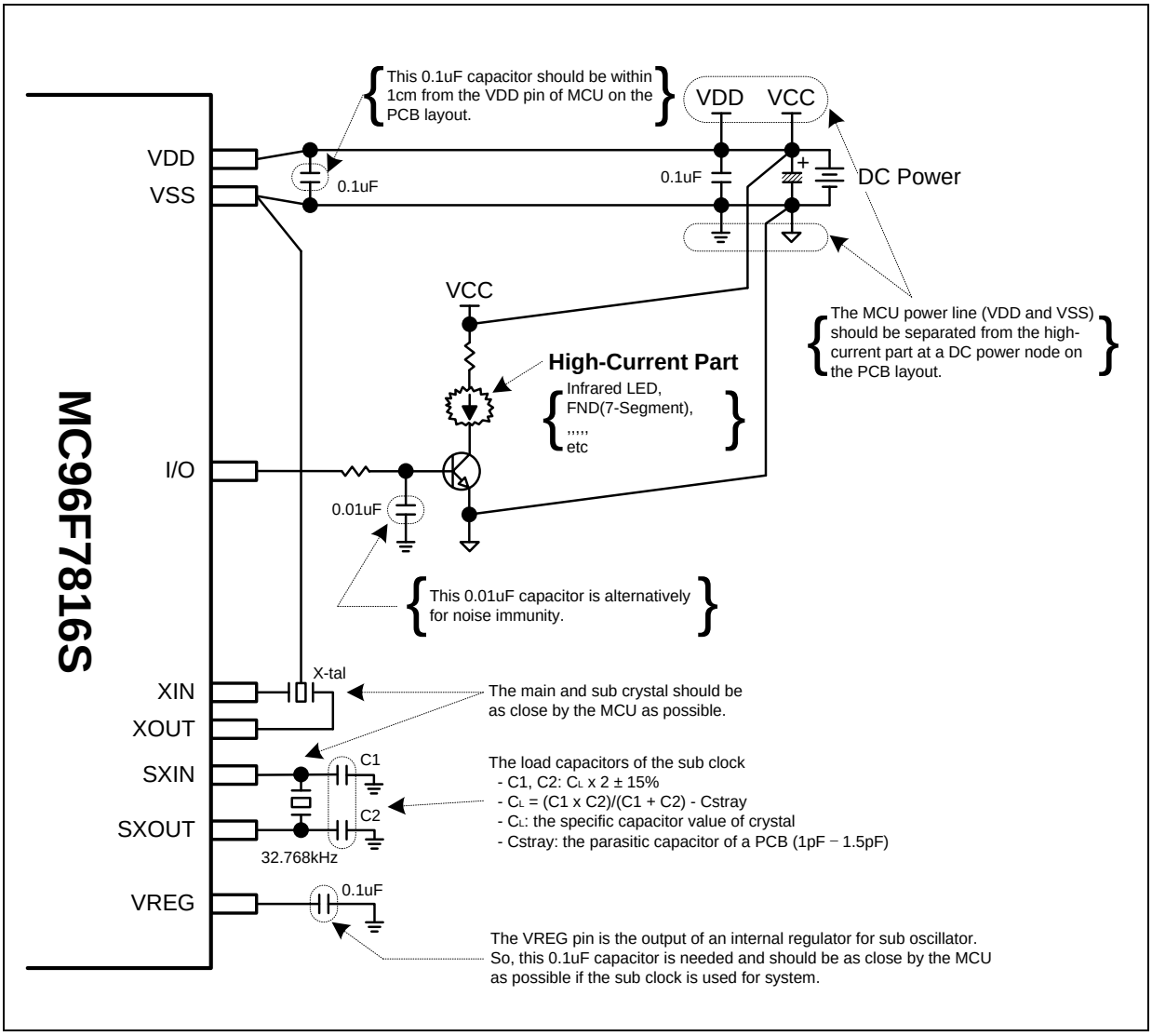
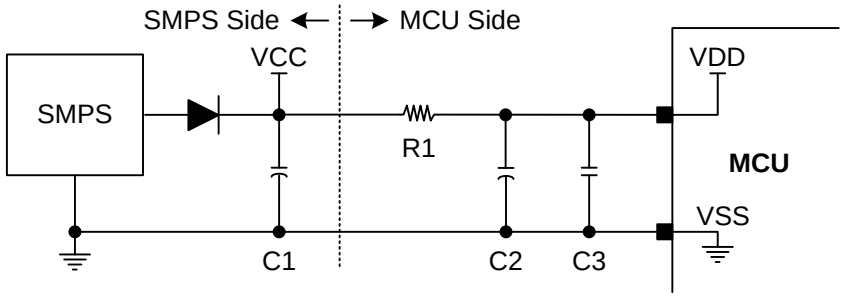


Figure 7.16 Recommended Circuit and Layout

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.17 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

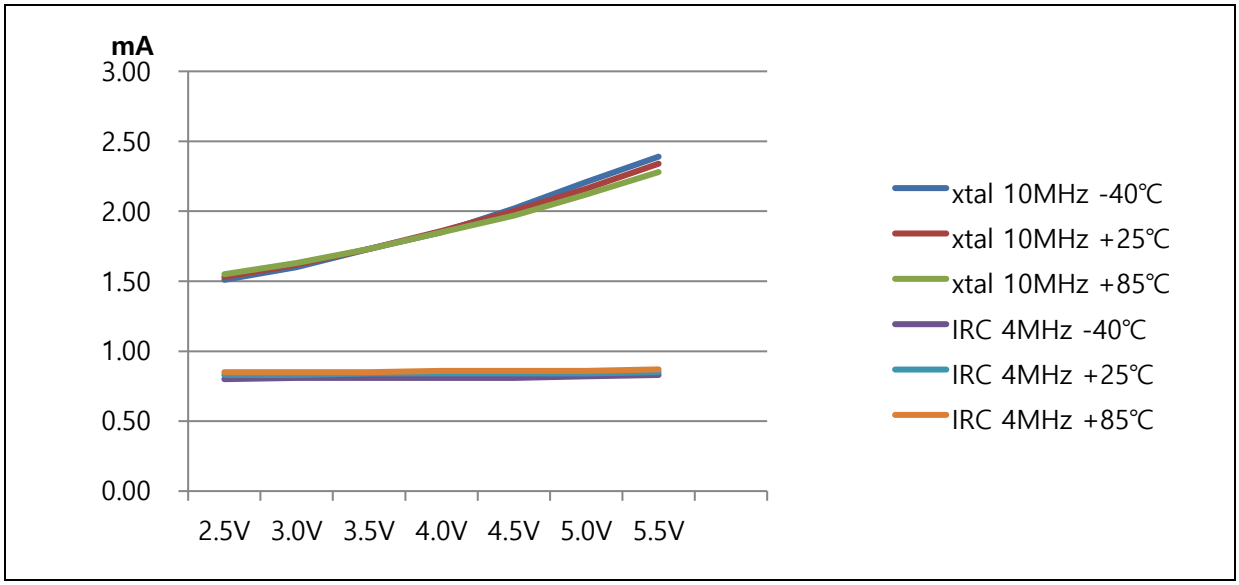


Figure 7.18 RUN (IDD1) Currnet

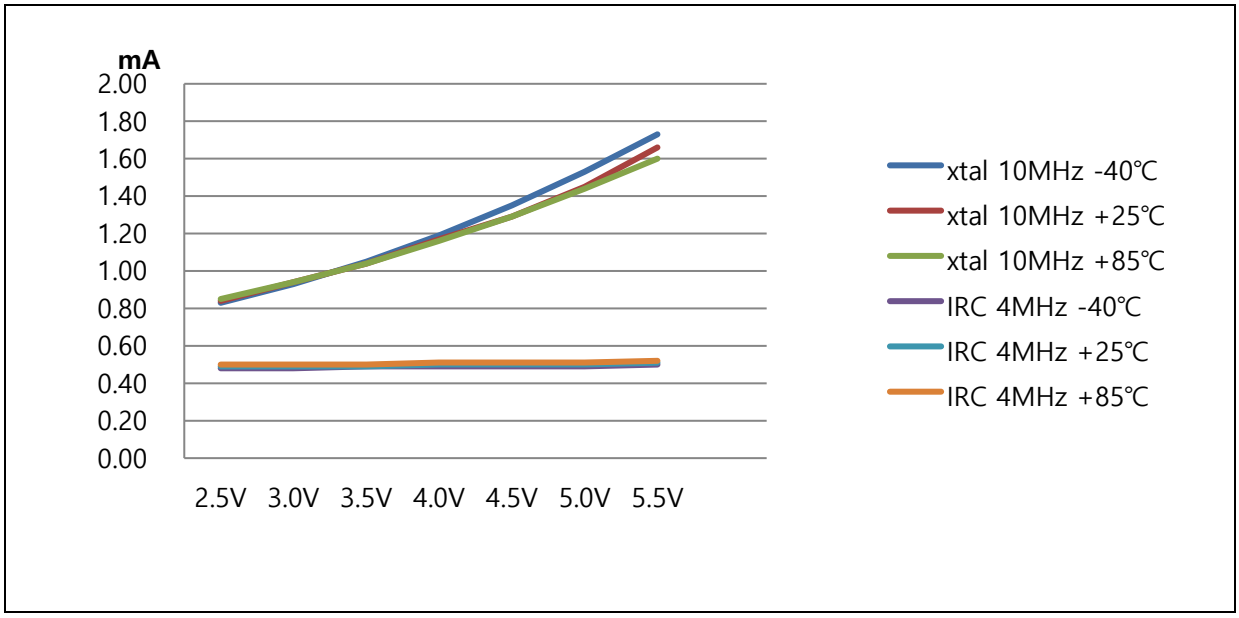


Figure 7.19 IDLE (IDD2) Current

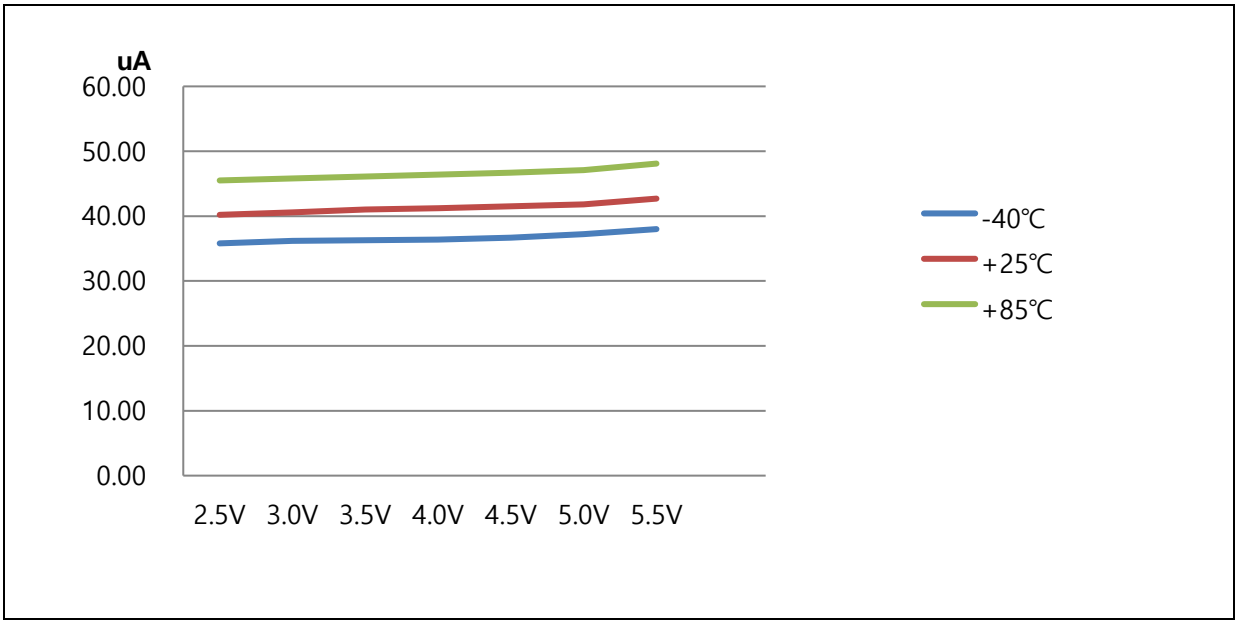


Figure 7.20 SUB RUN (IDD3) Current

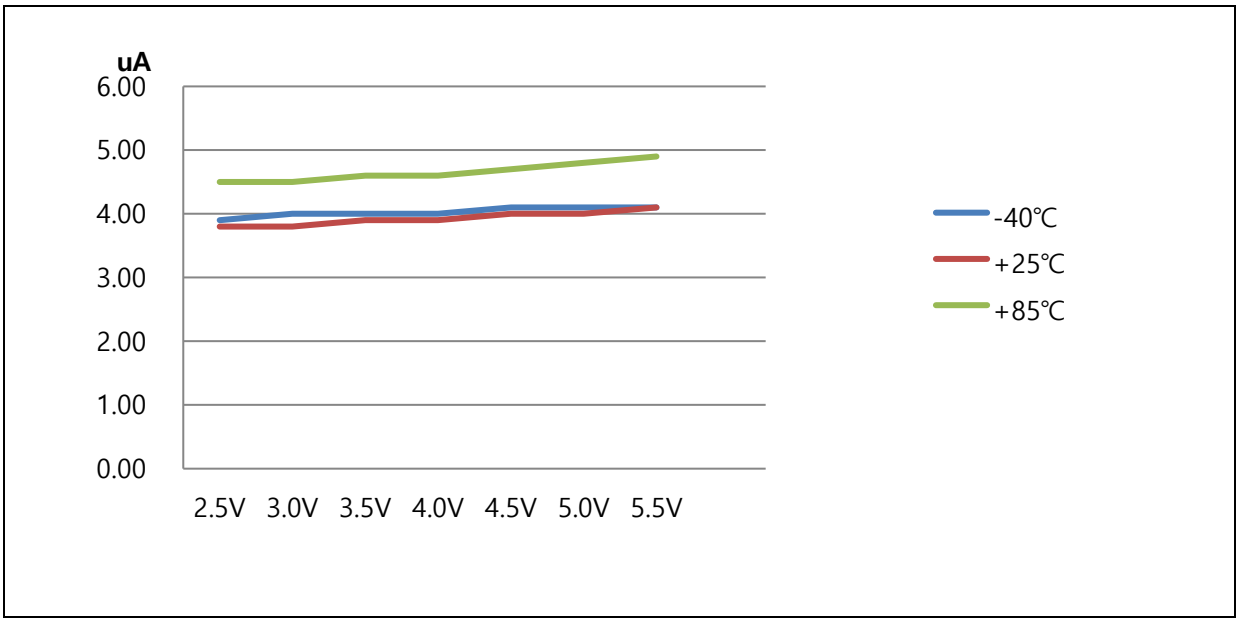


Figure 7.21 SUB IDLE (IDD4) Currnet

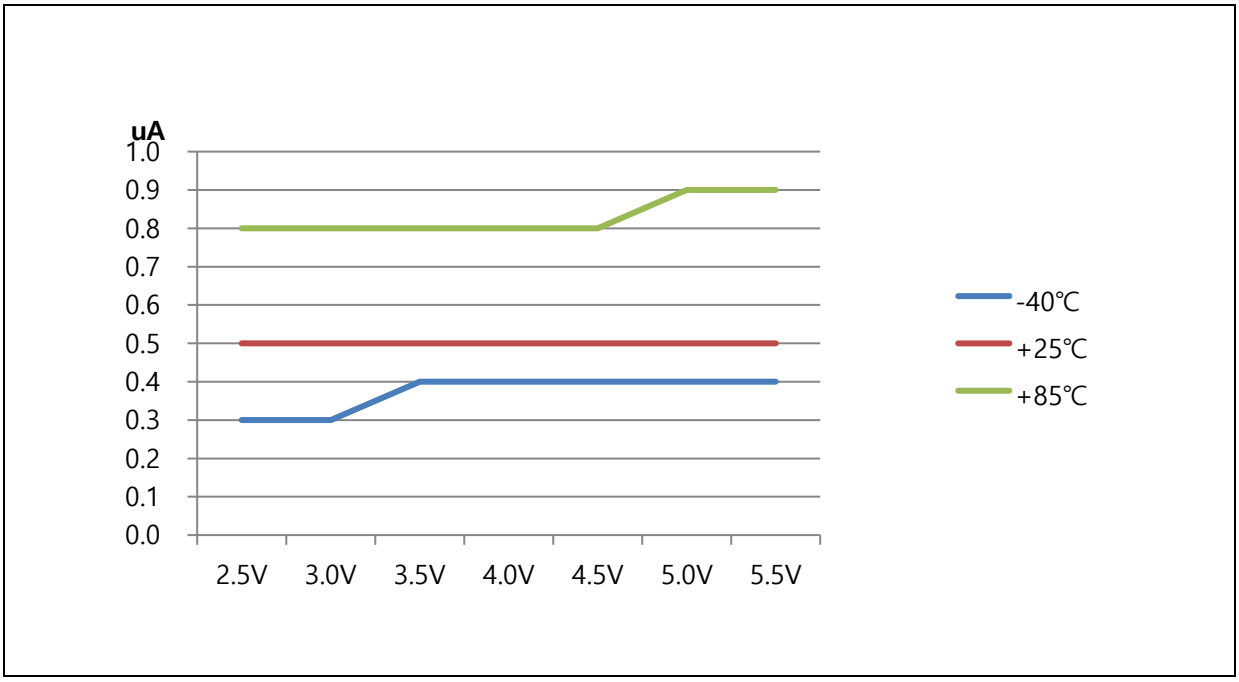


Figure 7.22 STOP (IDD5) Current