

ABOV SEMICONDUCTOR Co., Ltd.  
8-BIT MICROCONTROLLERS

# MC96F7864S

*Data Sheet (Ver. 1.2)*



## REVISION HISTORY

**VERSION 0.1 (December 8, 2021)****VERSION 0.5 (January 25, 2022)**

Fix the typos.

Change Internal VDC voltage value in A/D Converter characteristics.

Change Sector Erase Time typ/max value in Internal Flash Rom characteristics

Change RLCD1 min/max value in LCD Voltage characteristics.

**VERSION 0.6 (February 16, 2022)**

Change "IDD1~IDD5" in DC electrical characteristics.

Change LVR/LVI current typ/max value in LVR and LVI characteristics.

Change PLL parameter in PLL characteristics.

**VERSION 0.7 (February 25, 2022)**

Add IDD graph in Typical characteristics.

**VERSION 1.0 (April 19, 2022)**

Add MC96F7664SL 64LQFP-1010 Package

**VERSION 1.1 (November 17, 2022)**

Add POR graph in Power-On Reset characteristics.

**VERSION 1.2 (November 22, 2022)**

Add Revision history.

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Version 1.2

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# MC96F7864S

## CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 12-BIT A/D CONVERTER

### 1. Overview

#### 1.1 Description

The MC96F7864S is advanced CMOS 8-bit microcontroller with 64k bytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 64k bytes of FLASH, 256 bytes of IRAM, 3,072 bytes of XRAM , general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, 10-bit PWM output, watch timer, buzzer driving port, SPI, UART, I2C, 12-bit A/D converter, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F7864S also supports power saving modes to reduce power consumption.

Device Name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
MC96F7864SL	64k bytes	3,072 bytes	256 bytes	12 channel	71	80 LQFP-1212
MC96F7664SL				10 channel	55	64 LQFP-1010
MC96F7664SL14				10 channel	55	64 LQFP-1414

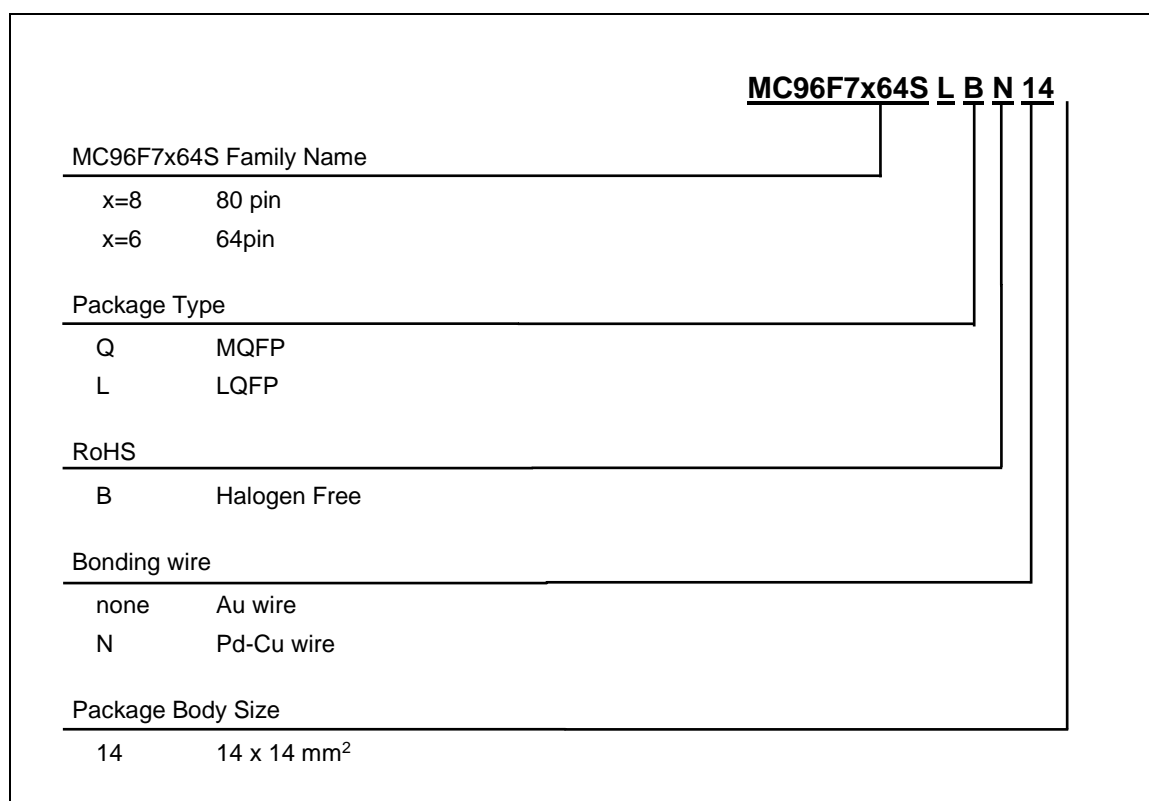


Figure 1.1 Device Nomenclature

## 1.2 Features

- **CPU**
  - 8 Bit CISC Core (8051 Compatible)
- **ROM (FLASH) Capacity**
  - 64k Bytes
  - Flash with self read/write capability
  - Parity bit check function for flash fail detection
  - On chip debug and In-system programming (ISP)
  - Endurance : 10,000 times (Sector 0~1019)  
100,000 times (Sector 1020~1023)
  - Retention : 10 years
- **256 Bytes IRAM**
- **3,072 Bytes XRAM**
  - (40 Bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 21 Ports  
(P0, P1, P6[6:2])
  - LCD shared I/O : 50 Ports  
(P2, P3, P4, P5, P6[1:0], P7, P8)
- **Basic Interval Timer (BIT)**
  - 8Bit × 1ch
- **Watch Dog Timer (WDT)**
  - 8Bit × 1ch
  - 5kHz internal RC oscillator
- **10Bit PWM Generator**
  - Emergency/Shot stop available
- **Timer/ Counter**
  - 8Bit × 3ch (T0/T1/T2), 16Bit × 4ch (T3/T4/T5/T6)
  - 8Bit × 2ch (T7/T8) or 16 Bit × 1ch (T7)
- **Programmable Pulse Generation**
  - 8Bit PWM (by T0/T1/T2)
  - Pulse generation (by T3/T4/T5/T6)
  - 6-ch 10Bit PWM for Motor (by T8)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1m interval at 32.768kHz
- **Buzzer**
  - 8Bit × 1ch
- **SPI**
  - 8Bit × 2ch
- **UART**
  - 8Bit × 3ch
- **USI (UART + SPI + I2C)**
  - 8Bit UART × 2ch, 8Bit SPI × 2ch, and I2C × 2ch
- **LCD Driver**
  - 36 Segments and 8 Common terminals
  - Internal or external resistor bias
  - Capacitor bias (Voltage Booster)
  - 16-step contrast control
  - 1/2, 1/3, 1/4, 1/5, 1/6, and 1/8 duty selectable
  - 1/2, 1/3, and 1/4 bias selectable
- **12 Bit A/D Converter**
  - 12 Input channels
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60V/ 2.00V/ 2.10V/ 2.20V/  
2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/  
3.38V/ 3.67V/ 4.00V/ 4.40V)
- **Low Voltage Indicator**
  - 13 level detect (2.00V/ 2.10V/ 2.20V/ 2.32V/  
2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/  
3.67V/ 4.00V/ 4.40V)
  - External reference detect
- **Interrupt Sources**
  - External Interrupts  
(EINT0~9, EINT10~18) (19)
  - Timer(0/1/2/3/4/5/6/7/8) (13)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - PWM (3)
  - SPI 2/3 (2)
  - UART 2/3/4 (6)
  - USI0/1 (4)
  - ADC (1)
- **Internal RC Oscillator**
  - Internal RC frequency:  
16MHz ±1.5% (TA= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode

- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@32 ~ 38kHz with X-tal)
  - 1.8V ~ 5.5V (@0.4 ~ 4.2MHz with X-tal)
  - 2.7V ~ 5.5V (@0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 5.5V (@0.5 ~ 8.0MHz with Internal RC)
  - 2.0V ~ 5.5V (@0.5 ~ 16.0MHz with Internal RC)
  - 2.0V ~ 5.5V (@1.0 ~ 16.0MHz with PLL)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 125ns (@ 16MHz main clock)
  - 61 $\mu$ s (@t 32.768kHz sub clock)
- **Operating Temperature:** – 40 ~ + 85 $^{\circ}$ C
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
  - Phase locked loop (Max. 16.4MHz with sub clock)
- **Package Type**
  - 80 LQFP-1212
  - 64 LQFP-1010
  - 64 LQFP-1414
  - Pb-free package



### 1.3 Ordering Information

**Table 1-1 Ordering Information of MC96F7864S**

Device name	ROM size	IRAM size	XRAM size	Package
MC96F7864SL	64k bytes FLASH	256 bytes	3,072 bytes	80 LQFP-1212
MC96F7664SL				64 LQFP-1010
MC96F7664SL14				64 LQFP-1414

## 1.4 Development Tools

### 1.4.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96F7864S is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

### 1.4.2 OCD emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- DSCL (MC96F7864S P14 port)
- DSDA (MC96F7864S P15 port)

OCD connector diagram: Connect OCD with user system

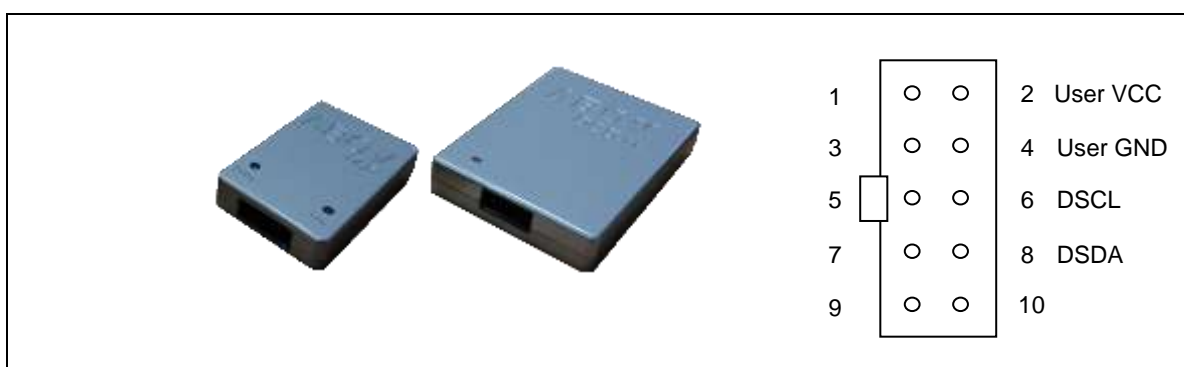


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

### 1.4.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

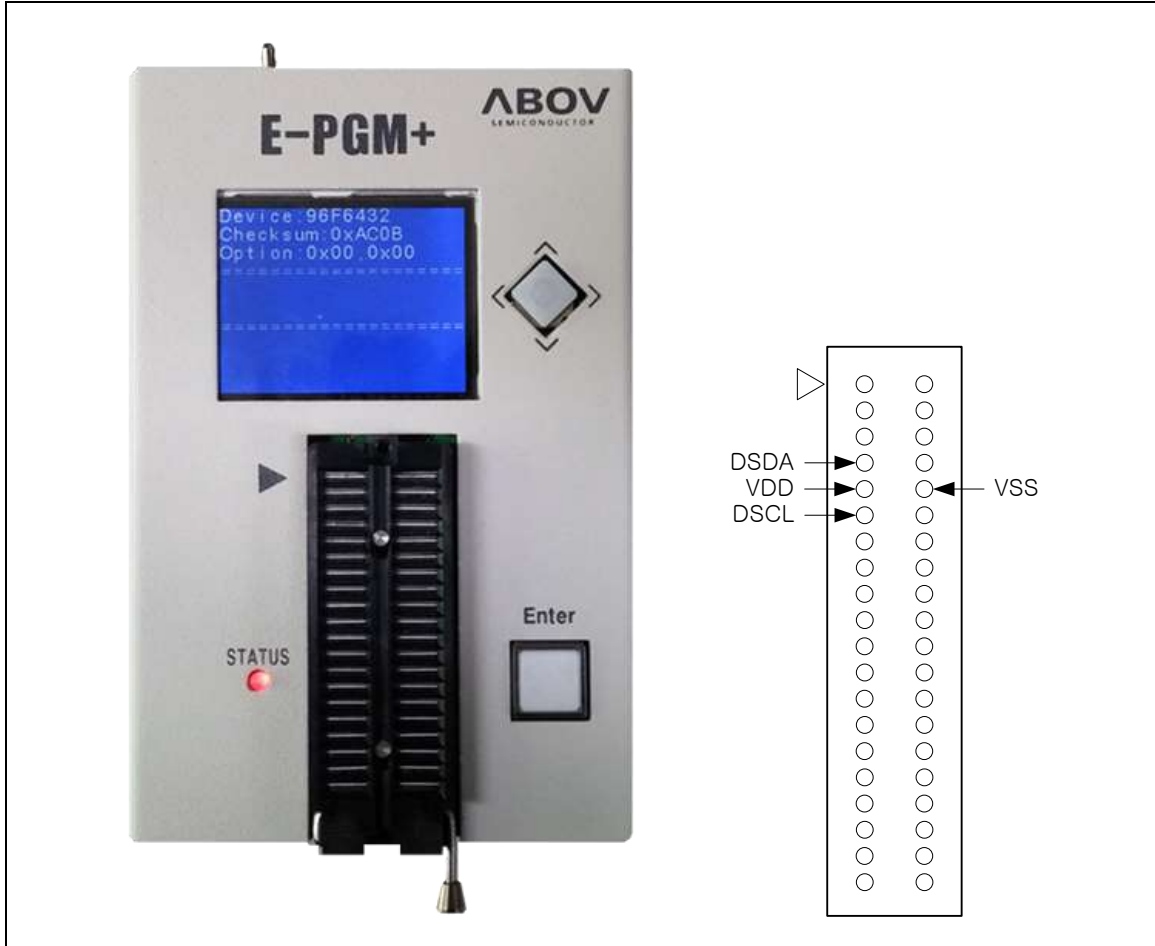


Figure 1.3 E-PGM+(Single writer)

OCD emulator: It can write code in MCU device too, because OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

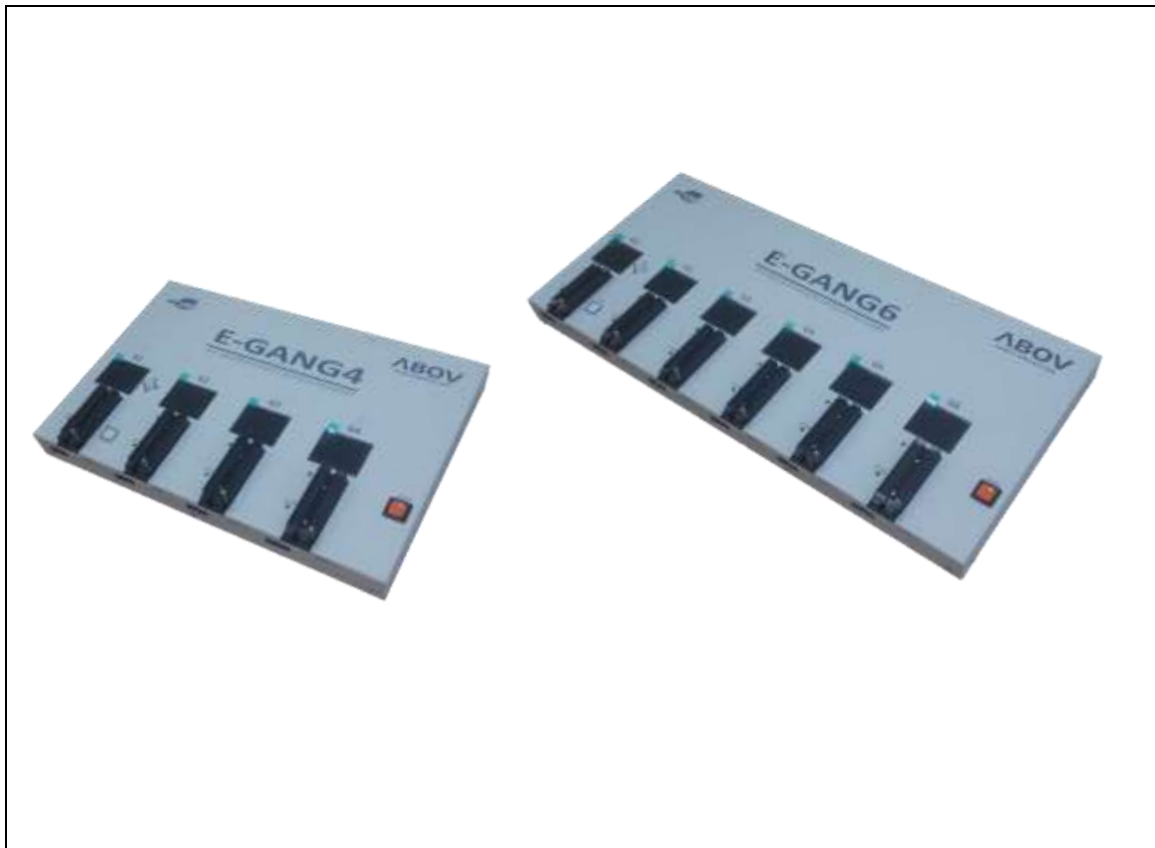


Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

## 2. Block Diagram

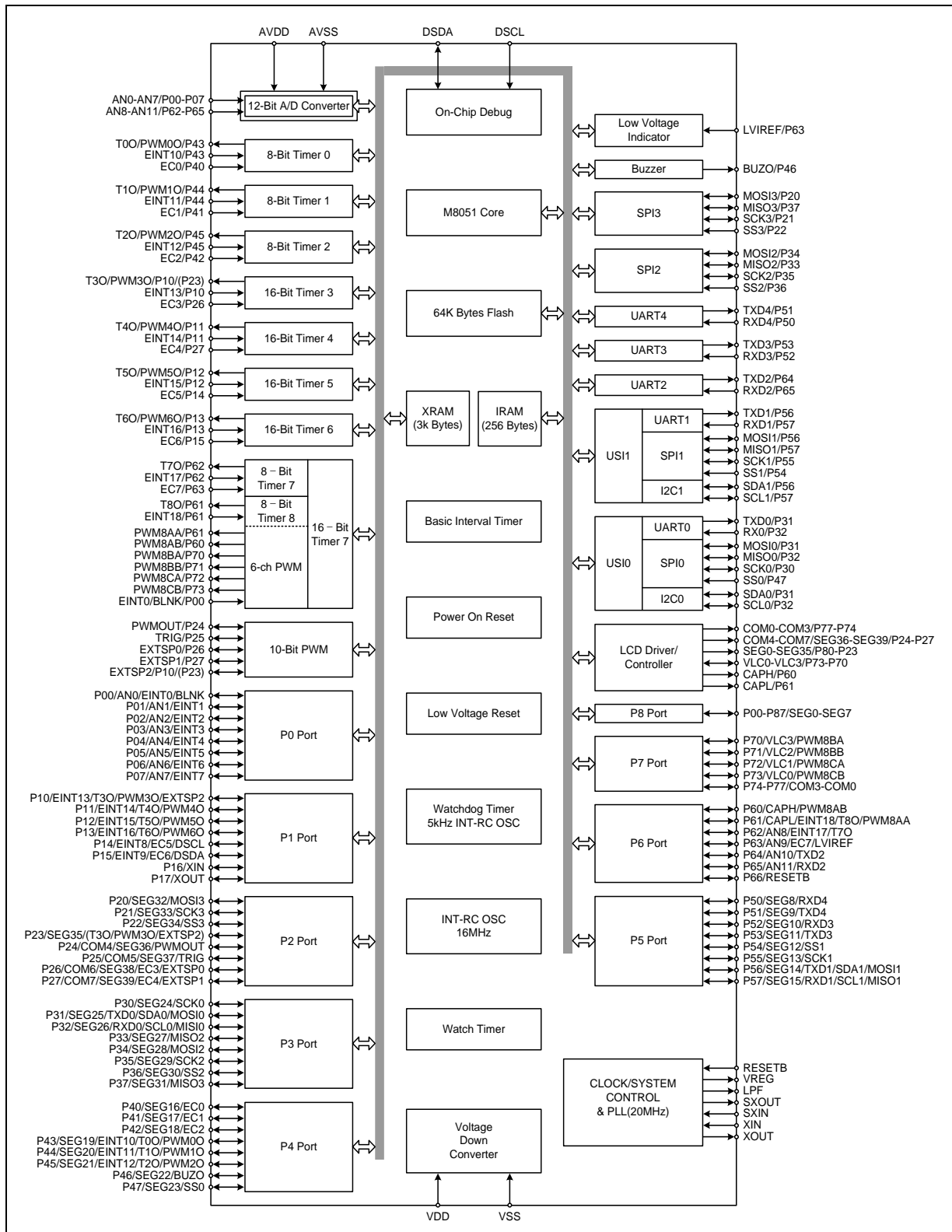


Figure 2.1 Block Diagram

NOTE) The P06-P07, P20-P23, P36-P37, and P8 are not in the 64-pin package.

### 3. Pin Assignment

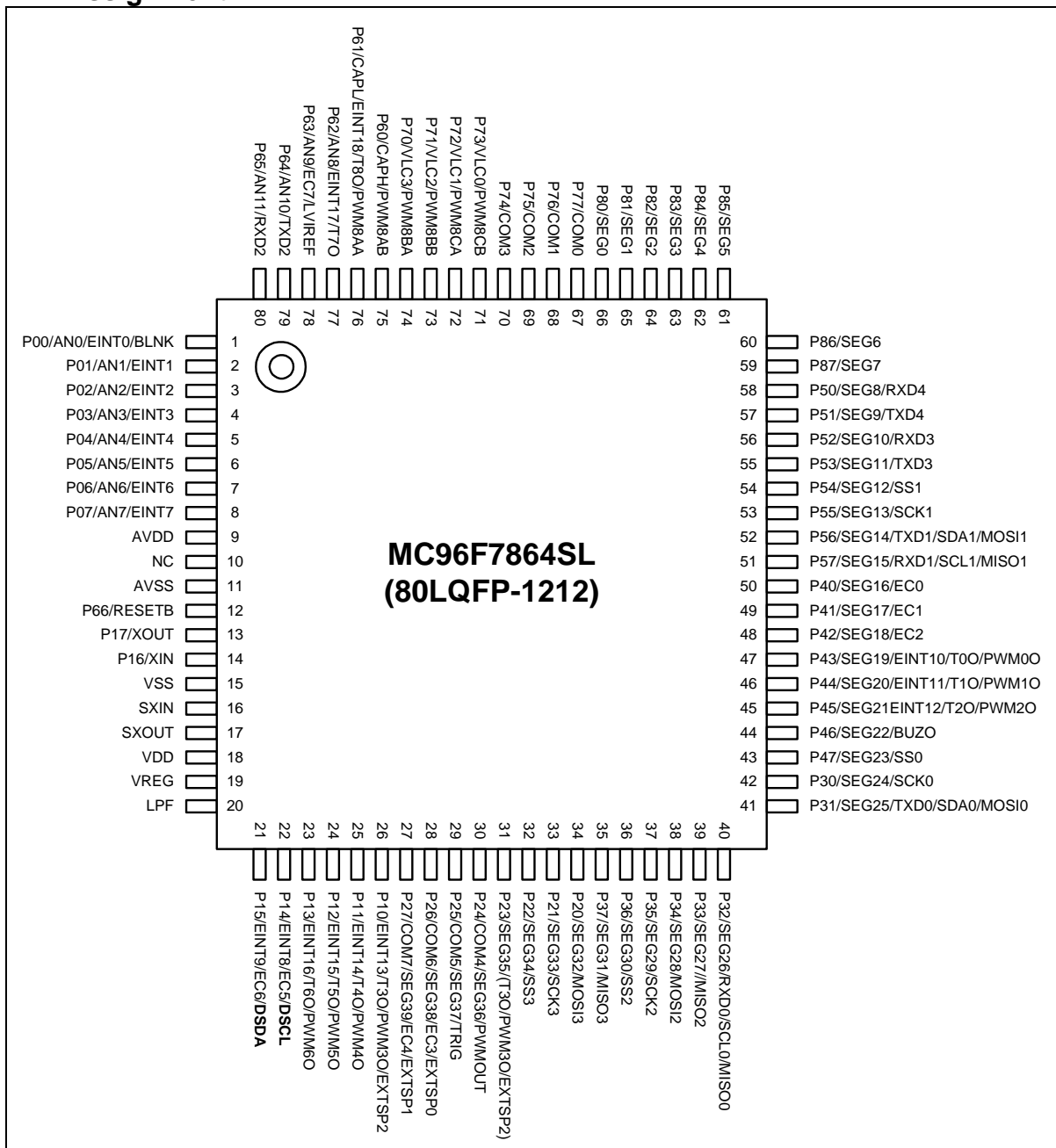


Figure 3.1 MC96F7864SL 80LQFP-1212 Pin Assignment

- NOTES) 1. On On-Chip Debugging, ISP uses P1[5:4] pin as DSDA, DSCL.  
 2. The pin in parentheses can be configured by software control.

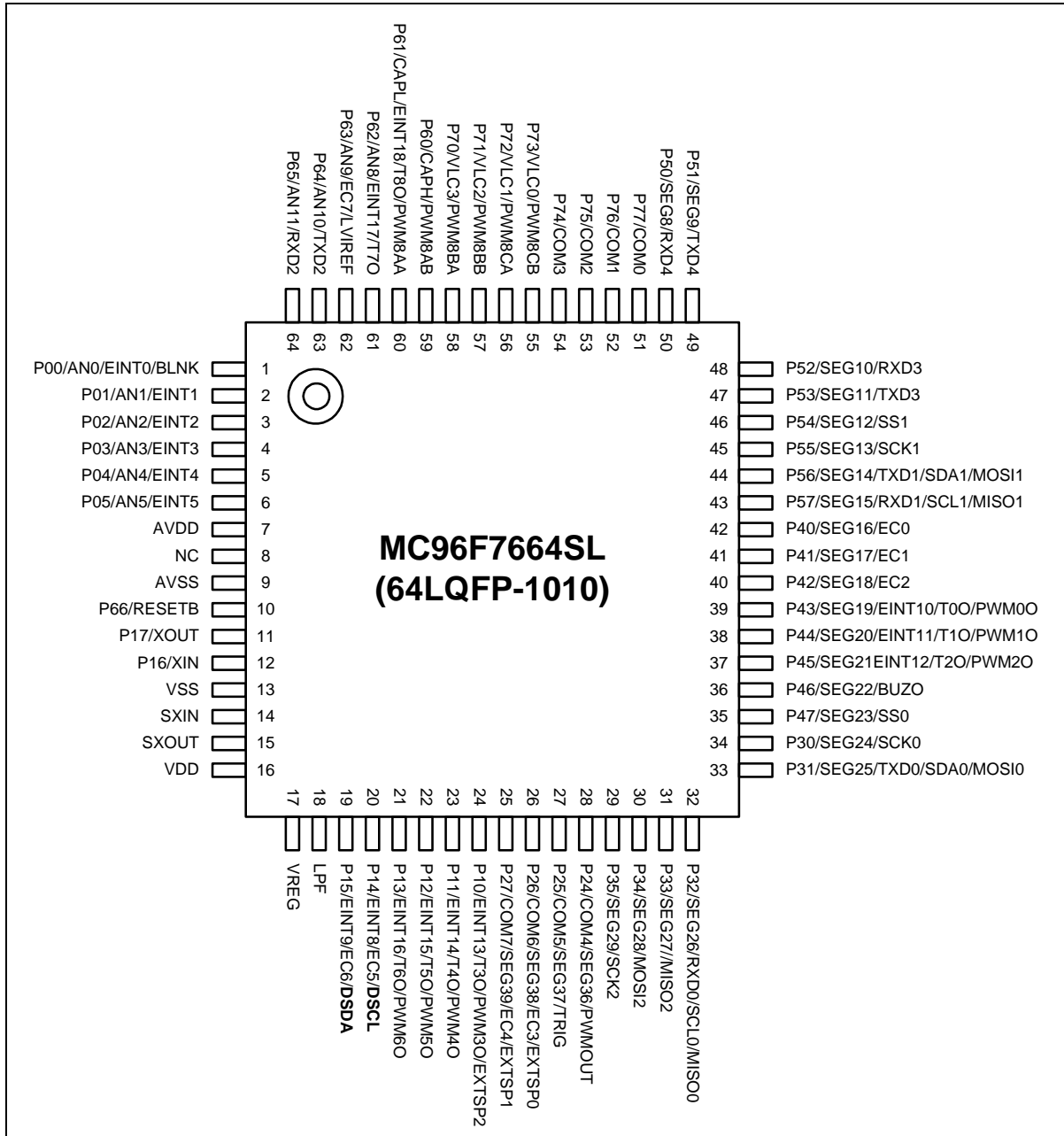
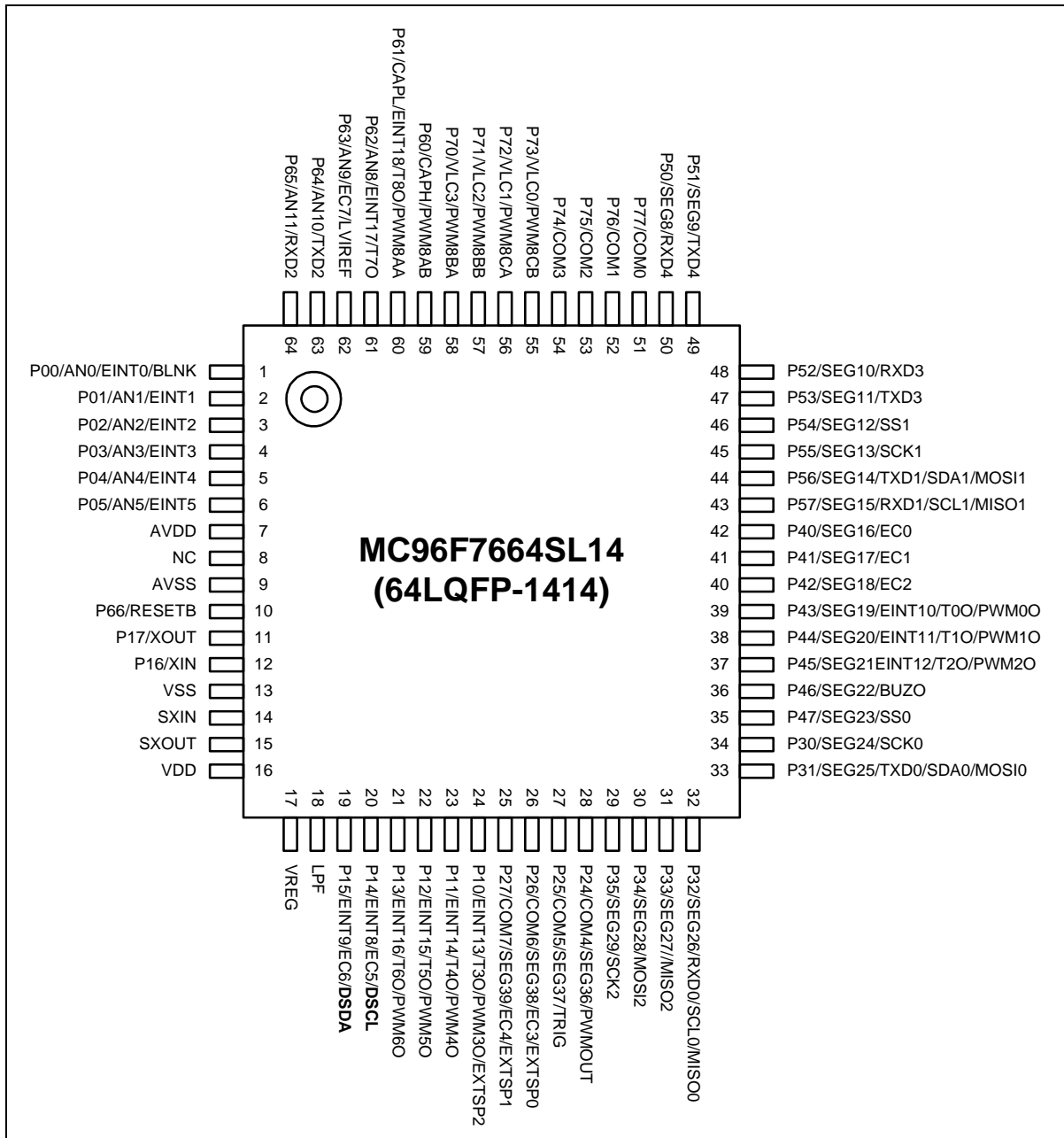


Figure 3.2 MC96F7664SL 64LQFP-1010 Pin Assignment

- NOTES) 1. On On-Chip Debugging, ISP uses P1[5:4] pin as DSDA, DSCL.  
 2. The P06-P07, P20-P23, P36-P37, and P8 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 64-pin package is used.



**Figure 3.3 MC96F7664SL14 64LQFP-1414 Pin Assignment**

- NOTES) 1. On On-Chip Debugging, ISP uses P1[5:4] pin as DSDA, DSCL.  
 2. The P06-P07, P20-P23, P36-P37, and P8 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 64-pin package is used.







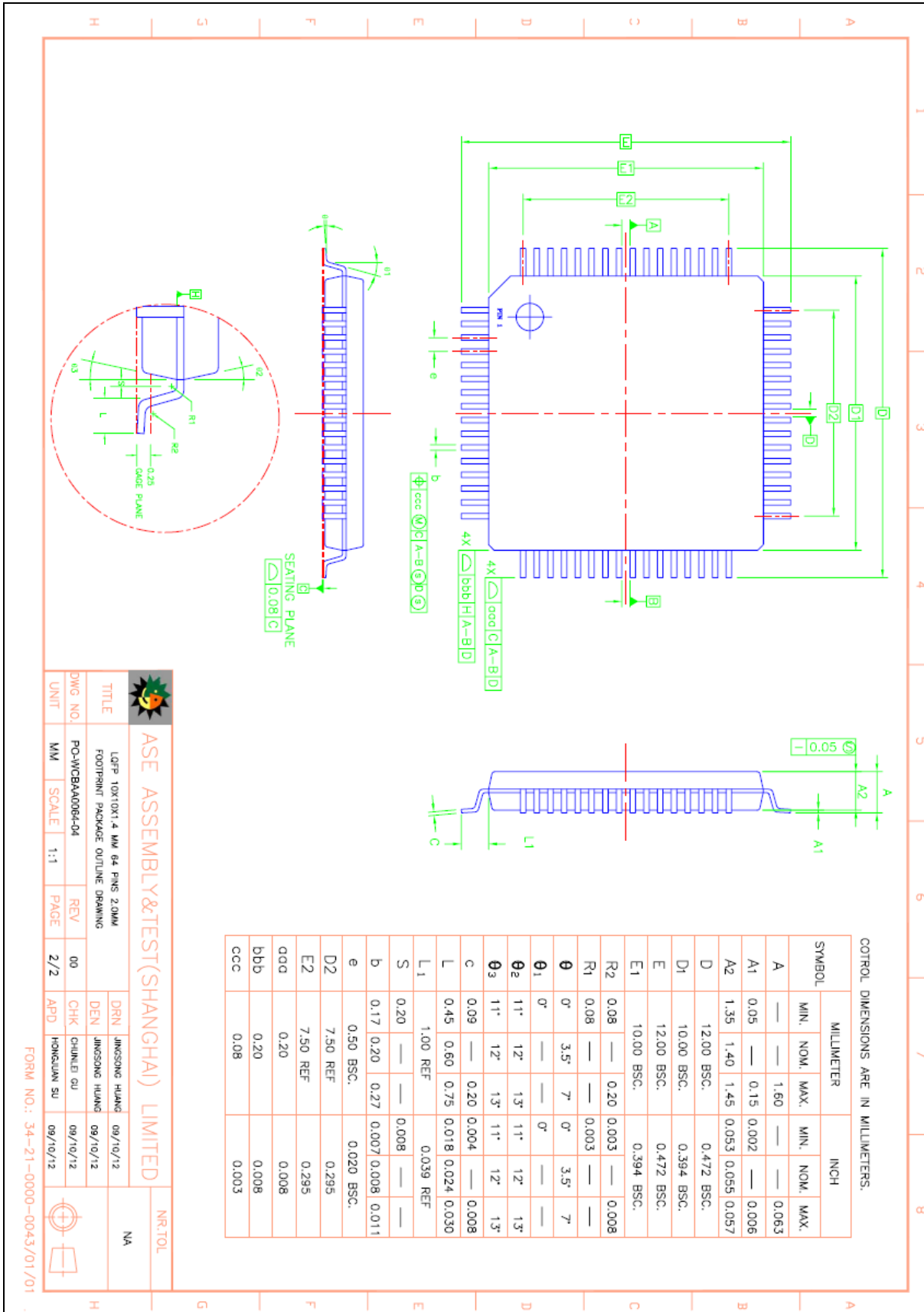


Figure 4.3 64-Pin LQFP-1010 Package

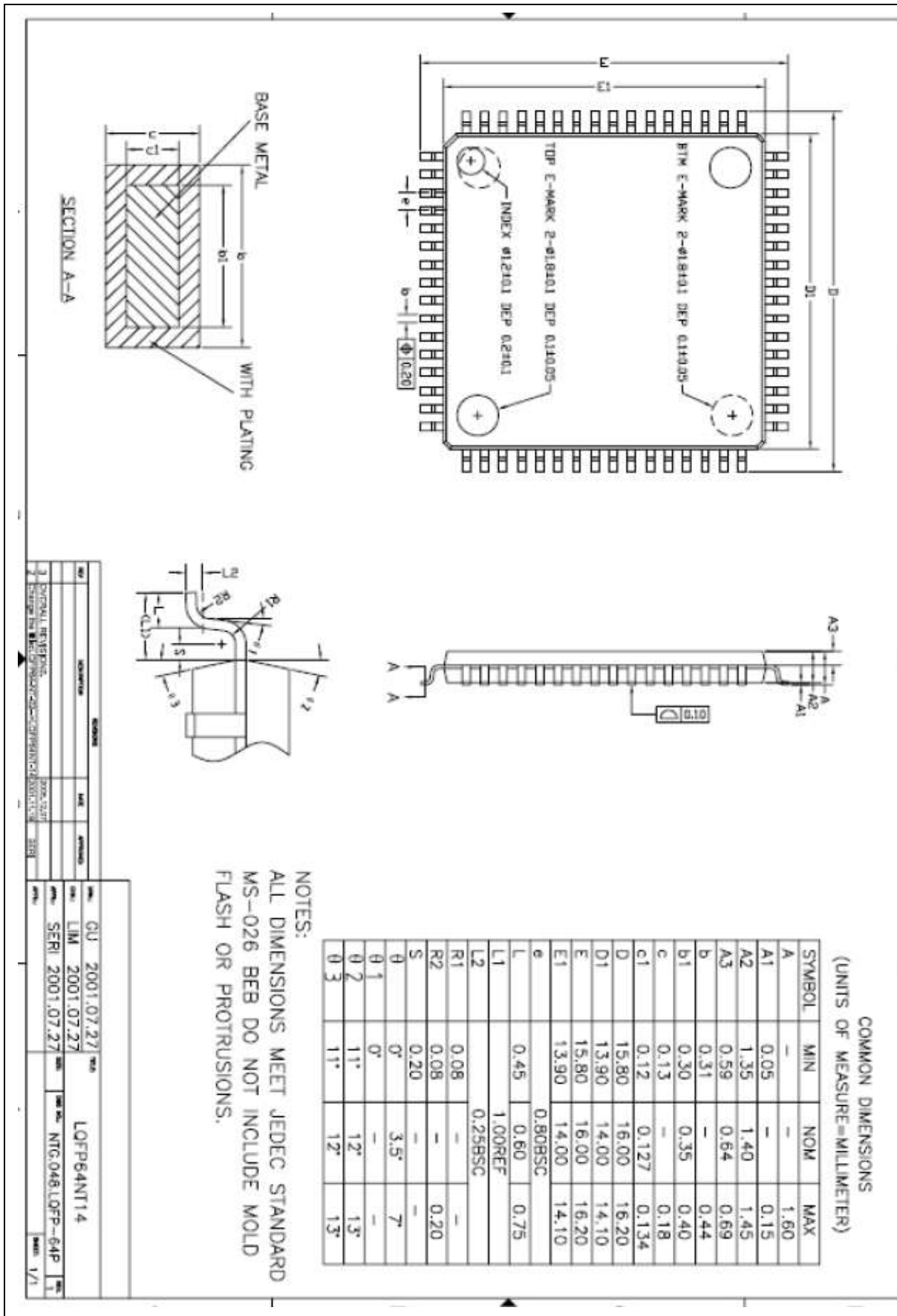


Figure 4.4 64-Pin LQFP-1414 Package

## 5. Pin Description

**Table 5-1 Normal Pin Description**

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P06-P07 are not in the 64-Pin package.	Input	AN0/EINT0/BLNK
P01				AN1/EINT1
P02				AN2/EINT2
P03				AN3/EINT3
P04				AN4/EINT4
P05				AN5/EINT5
P06				AN6/EINT6
P07				AN7/EINT7
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT13/T3O/PWM3O/EXTSP2
P11				EINT14/T4O/PWM4O
P12				EINT15/T5O/PWM5O
P13				EINT16/T6O/PWM6O
P14				EINT8/EC5/DSCL
P15				EINT9/EC6/DSDA
P16				XIN
P17				XOUT
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20 – P23 are not in the 64-pin package.	Input	SEG32/MOSI3
P21				SEG33/SCK3
P22				SEG34/SS3
P23				SEG35/(T3O/PWM3O/EXTSP2)
P24				COM4/SEG36/PWMOUT
P25				COM5/SEG37/TRIG
P26				COM6/SEG38/EC3/EXTSP0
P27				COM7/SEG39/EC4/EXTSP1
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P36-P37 are not in the 64-Pin package.	Input	SEG24/SCK0
P31				SEG25/TXD0/SDA0/MOSI0
P32				SEG26/RXD0/SCL0/MISO0
P33				SEG27/MISO2
P34				SEG28/MOSI2
P35				SEG29/SCK2
P36				SEG30/SS2
P37				SEG31/MISO3
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG16/EC0
P41				SEG17/EC1
P42				SEG18/EC2
P43				SEG19/EINT10/T0O/PWM0O
P44				SEG20/EINT11/T1O/PWM1O
P45				SEG21/EINT12/T2O/PWM2O
P46				SEG22/BUZO
P47				SEG23/SS0

Table 5-1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.  A pull-up resistor can be specified in 1-bit unit.	Input	SEG8/RXD4
P51				SEG9/TXD4
P52				SEG10/RXD3
P53				SEG11/TXD3
P54				SEG12/SS1
P55				SEG13/SCK1
P56				SEG14/TXD1/SDA1/MOSI1
P57				SEG15/RXD1/SCL1/MISO1
P60				I/O
P61	CAPL/EINT18/T8O/PWM8AA			
P62	AN8/EINT17/T7O			
P63	AN9/EC7/LVIREF			
P64	AN10/TXD2			
P65	AN11/RXD2			
P66	RESETB			
P70	I/O	Port 7 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output.  A pull-up resistor can be specified in 1-bit unit.	Input	VLC3/PWM8BA
P71				VLC2/PWM8BB
P72				VLC1/PWM8CA
P73				VLC0/PWM8CB
P74				COM3
P75				COM2
P76				COM1
P77				COM0
P80	I/O	Port 8 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output.  A pull-up resistor can be specified in 1-bit unit.  The P8 is not in the 64-Pin package.	Input	SEG0
P81				SEG1
P82				SEG2
P83				SEG3
P84				SEG4
P85				SEG5
P86				SEG6
P87				SEG7
EINT0	I/O	External interrupt inputs	Input	P00/AN0/BLNK
EINT1				P01/AN1
EINT2				P02/AN2
EINT3				P03/AN3
EINT4				P04/AN4
EINT5				P05/AN5
EINT6				P06/AN6
EINT7				P07/AN7
EINT8				P14/EC5/D_SCL
EINT9				P15/EC6/D_SDA
EINT10	I/O	External interrupt and Timer 0 capture input	Input	P43/SEG19/T0O/PWM0O
EINT11	I/O	External interrupt and Timer 1 capture input	Input	P44/SEG20/T1O/PWM1O



EINT12	I/O	External interrupt and Timer 2 capture input	Input	P45/SEG21/T2O/PWM2O
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**Table 5-1 Normal Pin Description (Continued)**

PIN Name	I/O	Function	@RESET	Shared with
EINT13	I/O	External interrupt and Timer 3 capture input	Input	P10/T3O/PWM3O/EXTSP2
EINT14	I/O	External interrupt and Timer 4 capture input	Input	P11/T4O/PWM4O
EINT15	I/O	External interrupt and Timer 5 capture input	Input	P12/T5O/PWM5O
EINT16	I/O	External interrupt and Timer 6 capture input	Input	P13/T6O/PWM6O
EINT17	I/O	External interrupt and Timer 7 capture input	Input	P62/AN8/T7O
EINT18	I/O	External interrupt and Timer 8 capture input	Input	P61/CAPL/T8O/PWM8AA
T0O	I/O	Timer 0 interval output	Input	P43/SEG19/EINT10/PWM0O
T1O	I/O	Timer 1 interval output	Input	P44/SEG20/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P45/SEG21/EINT12/PWM2O
T3O	I/O	Timer 3 interval output	Input	P10/EINT13/PWM3O/EXTSP2
T4O	I/O	Timer 4 interval output	Input	P11/EINT14/PWM4O
T5O	I/O	Timer 5 interval output	Input	P12/EINT15/PWM5O
T6O	I/O	Timer 6 interval output	Input	P13/EINT16/PWM6O
T7O	I/O	Timer 7 interval output	Input	P62/AN8/EINT17
T8O	I/O	Timer 8 interval output	Input	P61/CAPL/EINT18/PWM8AA
PWM0O	I/O	Timer 0 PWM output	Input	P43/SEG19/EINT10/T0O
PWM1O	I/O	Timer 1 PWM output	Input	P44/SEG20/EINT11/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P45/SEG21/EINT12/T2O
PWM3O	I/O	Timer 3 pulse output	Input	P10/EINT13/T3O/EXTSP2
PWM4O	I/O	Timer 4 pulse output	Input	P11/EINT14/T4O
PWM5O	I/O	Timer 5 pulse output	Input	P12/EINT15/T5O
PWM6O	I/O	Timer 6 pulse output	Input	P13/EINT16/T6O
PWM8AA	I/O	Timer 8's 6-ch PWM outputs	Input	P61/CAPL/EINT18/T8O
PWM8AB				P60/CAPH
PWM8BA				P70/VLC3
PWM8BB				P71/VLC2
PWM8CA				P72/VLC1
PWM8CB				P73/VLC0
BLNK	I/O	External sync signal input for 6-ch PWMs	Input	P00/AN0/EINT0
EC0	I/O	Timer 0 event count input	Input	P40/SEG16
EC1	I/O	Timer 1 event count input	Input	P41/SEG17
EC2	I/O	Timer 2 event count input	Input	P42/SEG18
EC3	I/O	Timer 3 event count input	Input	P26/COM6/SEG38/EXTSP0
EC4	I/O	Timer 4 event count input	Input	P27/COM7/SEG39/EXTSP1
EC5	I/O	Timer 5 event count input	Input	P14/EINT8/DSCL
EC6	I/O	Timer 6 event count input	Input	P15/EINT9/DSDA
EC7	I/O	Timer 7 event count input	Input	P63/AN9/LVIREF
SCK0	I/O	Serial 0 clock input/output	Input	P30/SEG24

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SCK1	I/O	Serial 1 clock input/output	Input	P55/SEG13
SCK2	I/O	Serial 2 clock input/output	Input	P35/SEG29
SCK3	I/O	Serial 3 clock input/output	Input	P21/SEG33



**Table 5-1 Normal Pin Description (Continued)**

PIN Name	I/O	Function	@RESET	Shared with
MOSI0	I/O	Serial 0 data input/output	Input	P31/SEG25/TXD0/SDA0
MOSI1	I/O	Serial 1 data input/output	Input	P56/SEG14/TXD1/SDA1
MOSI2	I/O	Serial 2 data input/output	Input	P34/SEG28
MOSI3	I/O	Serial 3 data input/output	Input	P20/SEG32
MISO0	I/O	Serial 0 data input/output	Input	P32/SEG26/RXD0/SCL0
MISO1	I/O	Serial 1 data input/output	Input	P57/SEG15/RXD1/SCL1
MISO2	I/O	Serial 2 data input/output	Input	P33/SEG27
MISO3	I/O	Serial 3 data input/output	Input	P37/SEG31
SS0	I/O	Slave 0 select input	Input	P47/SEG23
SS1	I/O	Slave 1 select input	Input	P54/SEG12
SS2	I/O	Slave 2 select input	Input	P36/SEG30
SS3	I/O	Slave 3 select input	Input	P22/SEG34
TXD0	I/O	UART 0 data output	Input	P31/SEG25/SDA0/MOSI0
TXD1	I/O	UART 1 data output	Input	P56/SEG14/SDA1/MOSI1
TXD2	I/O	UART 2 data output	Input	P64/AN10
TXD3	I/O	UART 3 data output	Input	P53/SEG11
TXD4	I/O	UART 4 data output	Input	P51/SEG9
RXD0	I/O	UART 0 data input	Input	P32/SEG26/SCL0/MISO0
RXD1	I/O	UART 1 data input	Input	P57/SEG15/SCL1/MISO1
RXD2	I/O	UART 2 data input	Input	P65/AN11
RXD3	I/O	UART 3 data input	Input	P52/SEG10
RXD4	I/O	UART 4 data input	Input	P50/SEG8
SCL0	I/O	I2C 0 clock input/output	Input	P32/SEG26/RXD0/MISO0
SCL1	I/O	I2C 1 clock input/output	Input	P57/SEG15/RXD1/MISO1
SDA0	I/O	I2C 0 data input/output	Input	P31/SEG25/TXD0/MOSI0
SDA1	I/O	I2C 1 data input/output	Input	P56/SEG14/TXD1/MOSI1
BUZO	I/O	Buzzer signal output	Input	P46/SEG22
AN0	I/O	A/D converter analog input channels	Input	P00/EINT0/BLNK
AN1				P01/EINT1
AN2				P02/EINT2
AN3				P03/EINT3
AN4				P04/EINT4
AN5				P05/EINT5
AN6				P06/EINT6
AN7				P07/EINT7
AN8				P62/EINT17/T7O
AN9				P63/EC7/LVIREF
AN10				P64/TXD2
AN11				P65/RXD2
LVIREF	I/O	Low voltage indicator reference voltage	Input	P63/AN9/EC7

Table 5-1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
VLC0	I/O	LCD bias voltage pins	Input	P73/PWM8CB
VLC1				P72/PWM8CA
VLC2				P71/PWM8BB
VLC3				P70/PWM8BA
CAPH	I/O	Capacitor terminals for voltage booster	Input	P60/PWM8AB
CAPL				P61/EINT18/T8O/PWM8AA
COM0–COM3	I/O	LCD common signal outputs	Input	P77–P74
COM4				P24/SEG36/PWMOUT
COM5				P25/SEG37/TRIG
COM6				P26/SEG38/EC3/EXTSP0
COM7				P27/SEG39/EC4/EXTSP1
SEG0–SEG7	I/O	LCD segment signal outputs	Input	P80–P87
SEG8				P50/RXD4
SEG9				P51/TXD4
SEG10				P52/RXD3
SEG11				P53/TXD3
SEG12				P54/SS1
SEG13				P55/SCK1
SEG14				P56/TXD1/SDA1/MOSI1
SEG15				P57/RXD1/SCL1/MISO1
SEG16–SEG18				P40–P42/EC0–EC2
SEG19				P43/EINT10/T0O/PWM0O
SEG20				P44/EINT11/T1O/PWM1O
SEG21				P45/EINT12/T2O/PWM2O
SEG22				P46/BUZO
SEG23				P47/SS0
SEG24				P30/SCK0
SEG25				P31/TXD0/SDA0/MOSI0
SEG26				P32/RXD0/SCL0/MISO0
SEG27				P33/MISO2
SEG28				P34/MOSI2
SEG29				P35/SCK2
SEG30				P36/SS2
SEG31				P37/MISO3
SEG32				P20/MOSI3
SEG33				P21/SCK3
SEG34				P22/SS3
SEG35				P23/(T3O/PWM3O/EXTSP2)
SEG36				P24/COM4/PWMOUT
SEG37				P25/COM5/TRIG
SEG38				P26/COM6/EC3/EXTSP0
SEG39				P27/COM7/EC4/EXTSP1

**Table 5-1 Normal Pin Description (Continued)**

PIN Name	I/O	Function	@RESET	Shared with
PWMOUT	I/O	10-bit PWM output	Input	P24/COM4/SEG36
TRIG	I/O	External trigger input for PWM generator	Input	P25/COM5/SEG37
EXTSP0	I/O	External shot/emergency stop inputs for PWM generator	Input	P26/COM6/SEG38/EC3
EXTSP1				P27/COM7/SEG39/EC4
EXTSP2				P10/EINT13/T3O/PWM3O
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P66
DSDA	I/O	On chip debugger data input/output <sup>(NOTE3,4)</sup>	Input	P15/EINT9/EC6
DSCL	I/O	On chip debugger clock input <sup>(NOTE3,4)</sup>	Input	P14/EINT8/EC5
XIN	I/O	Main oscillator pins	Input	P16
XOUT				P17
SXIN	-	Sub oscillator pins	-	-
SXOUT				-
LPF	-	Loop filter pump output for PLL	-	-
VREG	-	Regulator voltage output for sub clock 0.1uF capacitor needed	-	-
AVDD, AVSS	-	Analog power input pins	-	-
VDD, VSS	-	Digital Power input pins	-	-

- NOTES) 1. The P06-P07, P20-P23, P36-P37, and P8 are not in the 64-Pin package.  
 2. The P66/RESETB pin is configured as one of the P66 and the RESETB pin by the "CONFIGURE OPTION."  
 3. If the P14/EINT8/EC5/DSCL and P15/EINT9/EC6/DSDA pins are connected to an emulator during the reset or power-on reset, the pins are automatically configured as the debugger pins.  
 4. The P14/EINT8/EC5/DSCL and P15/EINT9/EC6/DSDA pins are configured as inputs with internal pull-up resistors only during the reset or power-on reset.  
 5. The P17/XOUT and P16/XIN pins are configured as a function pin by software control.

## 6. Port Structures

### 6.1 General Purpose I/O Port

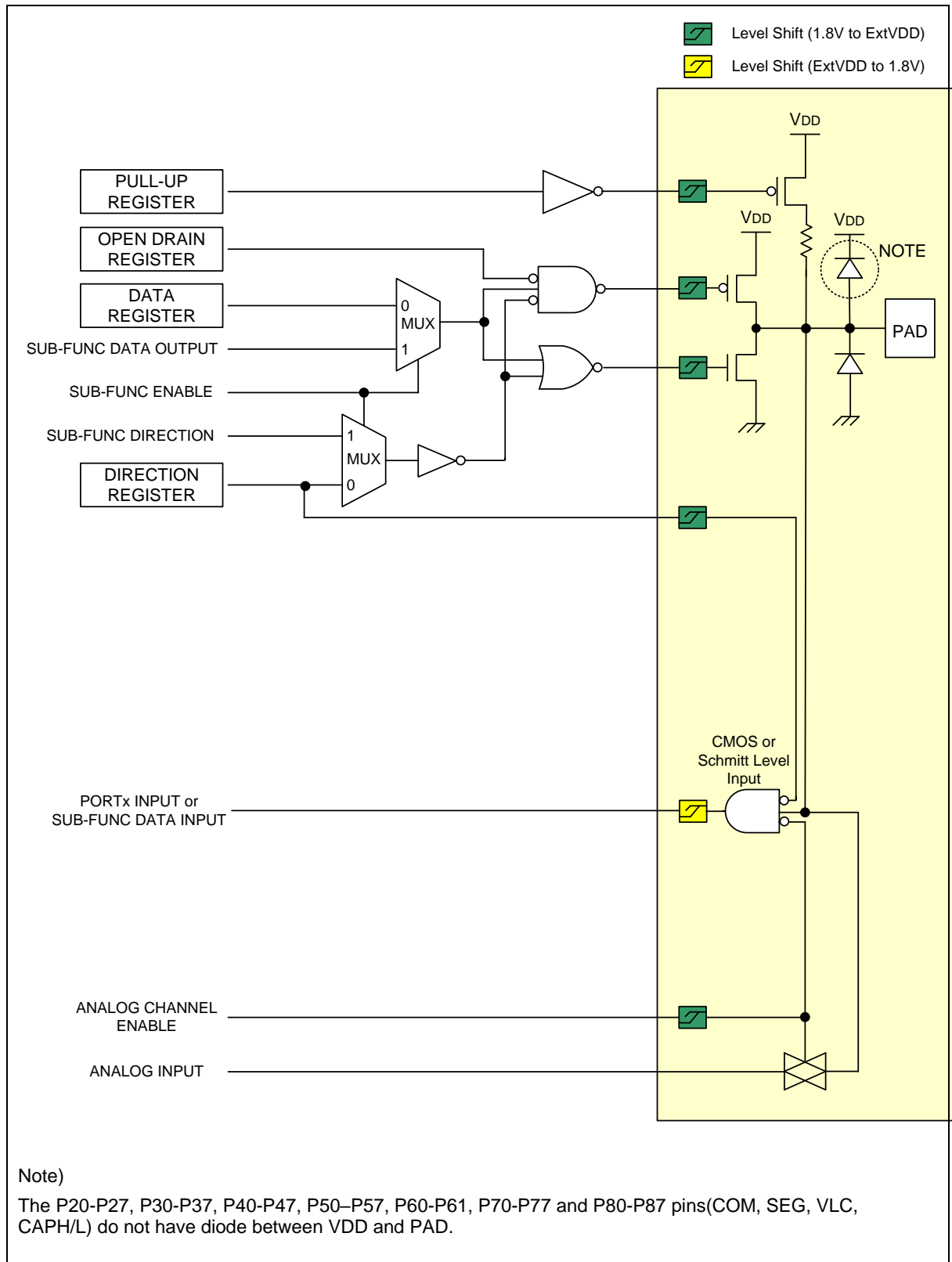


Figure 6.1 General Purpose I/O Port

### 6.2 External Interrupt I/O Port

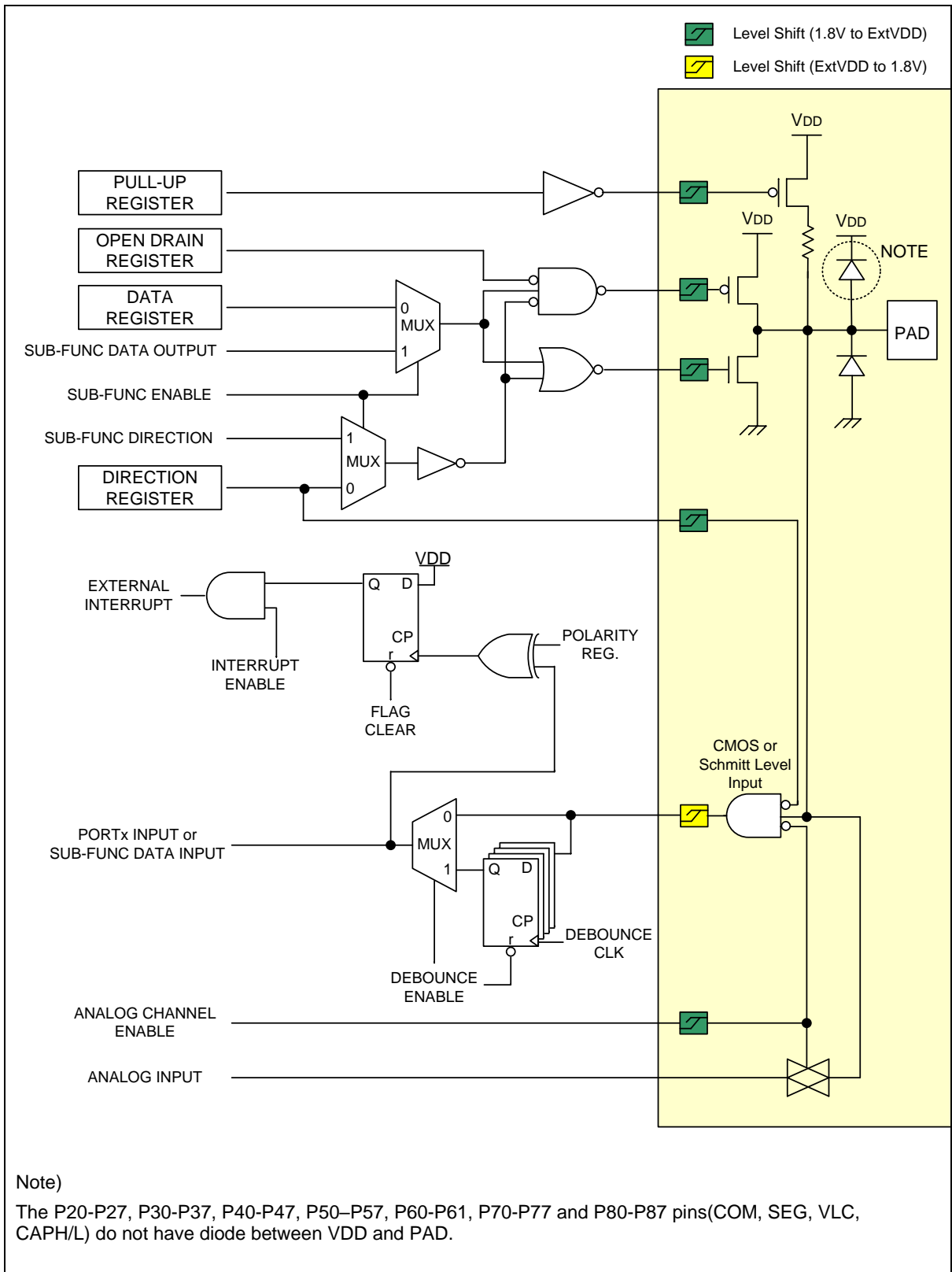


Figure 6.2 External Interrupt I/O Port

## 7. Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.5	V	–
Normal Voltage Pin	V <sub>I</sub>	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V <sub>O</sub>	-0.3 ~ VDD+0.3	V	
	I <sub>OH</sub>	-10	mA	Maximum current output sourced by (I <sub>OH</sub> per I/O pin)
	∑I <sub>OH</sub>	-80	mA	Maximum current (∑I <sub>OH</sub> )
	I <sub>OL</sub>	60	mA	Maximum current sunk by (I <sub>OL</sub> per I/O pin)
	∑I <sub>OL</sub>	120	mA	Maximum current (∑I <sub>OL</sub> )
Total Power Dissipation	P <sub>T</sub>	600	mW	–
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C	–

NOTE) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 7.2 Recommended Operating Conditions

Table 7-2 Recommended Operating Conditions

(T<sub>A</sub> = -40°C ~ +85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Operating Voltage	VDD	f <sub>X</sub> = 32 ~ 38kHz	SX-tal	1.8	–	5.5	V
		f <sub>X</sub> = 0.4 ~ 4.2MHz	X-tal	1.8	–	5.5	
		f <sub>X</sub> = 0.4 ~ 12.0MHz		2.7	–	5.5	
		f <sub>X</sub> = 0.5 ~ 8.0MHz	Internal RC	1.8	–	5.5	
		f <sub>X</sub> = 0.5 ~ 16.0MHz		2.0	–	5.5	
		f <sub>X</sub> = 1.0 ~ 16.0MHz	PLL	2.0	–	5.5	
Operating Temperature	T <sub>OPR</sub>	VDD = 1.8 ~ 5.5V	-40	–	85	°C	

### 7.3 A/D Converter Characteristics

**Table 7-3 A/D Converter Characteristics**

 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VDD=AVDD, VSS=AVSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Resolution	–	–	–	12	–	bit	
Integral Non-Linear	INL	AVDD= 2.7V – 5.5V fx= 8MHz	–	–	±6	LSB	
Differential Non-Linearity	DNL		–	–	±1		
Top Offset Error	TOE		–	–	±5		
Zero Offset Error	ZOE		–	–	±5		
Conversion Time	t <sub>CONV</sub>	12bit resolution, 8MHz	20	–	–	μs	
Analog Input Voltage	V <sub>AIN</sub>	–	AVSS	–	AVDD	V	
Internal VDC Voltage	VDD15	–	–	1.55	–	V	
Analog Input Leakage Current	I <sub>AIN</sub>	AVDD= 5.12V	–	–	2	μA	
ADC Current	I <sub>ADC</sub>	Enable	AVDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	μA

NOTES) 1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (AVSS).

2. Top scale error is the difference between 111111111111 and the converted output for top input voltage (AVDD).

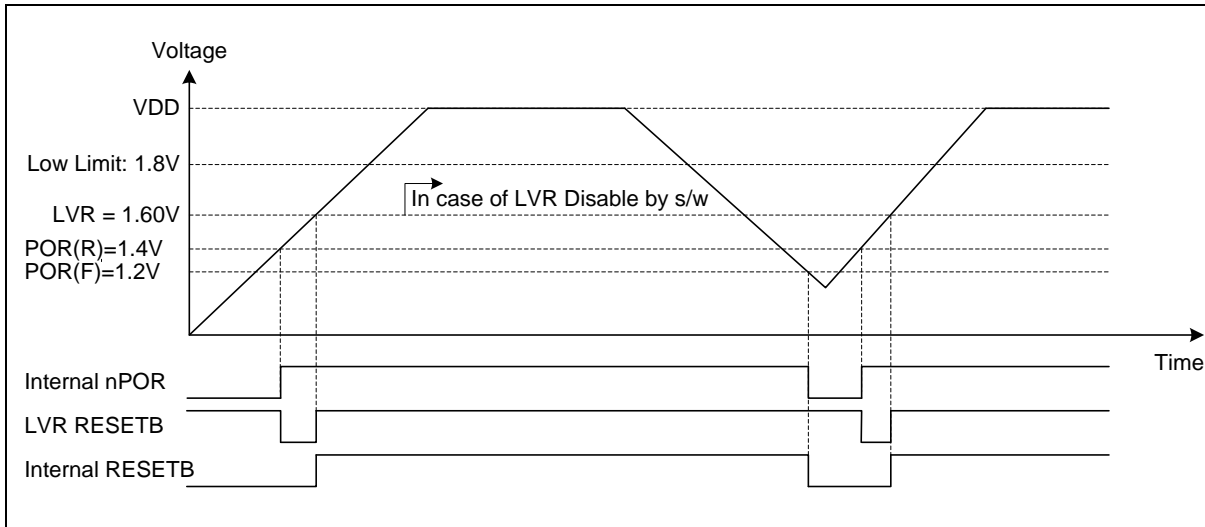
3. When AVDD is lower than 2.7V, the ADC resolution is worse.

### 7.4 Power-On Reset Characteristics

**Table 7-4 Power-on Reset Characteristics**

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	$V_{POR}$	–	–	1.4	–	V
VDD Voltage Rising Time	$t_R$	–	0.05	–	30.0	V/ms
POR Current	$I_{POR}$	–	–	0.2	–	$\mu\text{A}$



**Figure 7.1 Power-on Reset Timing**



## 7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

**Table 7-5 LVR and LVI Characteristics**

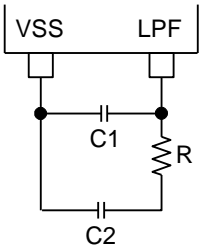
 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V <sub>LVR</sub> V <sub>LVI</sub>	The LVR can select all levels but LVI can select other levels except 1.60V.		–	1.60	1.79	V
				1.85	2.00	2.15	
				1.95	2.10	2.25	
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
4.10	4.40	4.70					
Hysteresis	ΔV	–		–	50	150	mV
Minimum Pulse Width	t <sub>LW</sub>	–		100	–	–	μs
LVR and LVI Current	I <sub>BL</sub>	Enable (Both)	VDD= 3V RUN Mode	–	3	6	μA
		Enable (One of two)		–	2	5	
		Disable (Both)	VDD= 3V	–	–	0.1	

## 7.6 Phase Locked Loop Characteristics

Table 7-6 Phase Locked Loop Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Frequency Range	–		–	32.768	–	kHz
Output Frequency Range	$f_{VCO}$		1.024	–	16.384	MHz
Clock Duty Ratio	$T_{OD}$		45	50	55	%
Tolerance	–		–	–	$\pm 1$	%
Settling Time	$t_D$		–	10	100	ms
PLL Current	$I_{PLL}$		Enable, $f_{VCO} = 16.384\text{MHz}$	–	0.5	1.0
		Disable	–	–	0.1	$\mu\text{A}$

NOTE) Where  $R = 6.8\text{k}\Omega$ ,  $C1 = 820\text{pF}$ , and  $C2 = 10\text{nF}$ .

## 7.7 Internal RC Oscillator Characteristics

Table 7-7 Internal RC Oscillator Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	$f_{IRC}$	$V_{DD} = 2.0\text{V to } 5.5\text{V}$	–	16	–	MHz
Tolerance	–	$T_A = 0^{\circ}\text{C to } +50^{\circ}\text{C}$	–	–	$\pm 1.5$	%
		$T_A = -20^{\circ}\text{C to } +85^{\circ}\text{C}$			$\pm 2.5$	
		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			$\pm 3.5$	
Clock Duty Ratio	$T_{OD}$	–	40	50	60	%
Stabilization Time	$T_{HFS}$	–	–	–	100	$\mu\text{s}$
IRC Current	$I_{IRC}$	Enable	–	0.2	–	mA
		Disable	–	–	0.1	$\mu\text{A}$

Note: A  $0.1\mu\text{F}$  Bypass capacitor should be connected to  $V_{DD}$  and  $V_{SS}$ . Refer to the “Recommend Circuit and Layout”.

## 7.8 Internal Watch-Dog Timer RC Oscillator Characteristics

Table 7-8 Internal WDTRC Oscillator Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	$f_{WDTRC}$	–	2	5	10	kHz
Stabilization Time	$t_{WDTS}$	–	–	–	1	ms
WDTRC Current	$I_{WDTRC}$	Enable	–	1	–	$\mu\text{A}$
		Disable	–	–	0.1	

## 7.9 LCD Voltage Characteristics

**Table 7-9 LCD Voltage Characteristics**

 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
LCD Voltage	V <sub>LC3</sub>	Voltage booster enabled, 1/4 bias	Typx0.93	0.75	Typx1.07	V	
				0.79			
				0.83			
				0.86			
				0.90			
				0.94			
				0.98			
				1.01			
				1.05			
				1.09			
				1.13			
				1.16			
				1.20			
				1.24			
1.28							
1.31							
LCD Mid Bias Voltage	V <sub>LC0</sub>	Voltage booster enabled, 1/4 bias, No panel load, VDD=3V	Typx0.95	4xVLC3	Typx1.05	V	
	V <sub>LC1</sub>		Typx0.95	3xVLC3	Typx1.05		
	V <sub>LC2</sub>		Typx0.95	2xVLC3	Typx1.05		
	V <sub>LC1</sub>	Voltage booster disabled, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, VLC0=VDD	Typ-0.2	0.75xVDD	Typ+0.2	V	
	V <sub>LC2</sub>		Typ-0.2	0.5xVDD	Typ+0.2		
	V <sub>LC3</sub>		Typ-0.2	0.25xVDD	Typ+0.2		
LCD Driver Output Impedance	R <sub>LO</sub>	VLCD=3V, ILOAD=±10uA	–	5	10	kΩ	
LCD Bias Dividing Resistor	R <sub>LCD1</sub>	Internal resistor mode, T <sub>A</sub> = 25 °C	Low	7.0	10	13.0	kΩ
	R <sub>LCD2</sub>		Mid	35	50	65	
	R <sub>LCD3</sub>		High	75	100	125	
LCD Block Current	I <sub>LCD</sub>	Voltage booster mode, VDD=3V, VLC0=3.15V, 1/3Bias	–	3	6	μA	

## 7.10 DC Characteristics

**Table 7-10 DC Characteristics**

 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f<sub>XIN</sub>= 12MHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Input High Voltage	V <sub>IH1</sub>	P0~P6, RESETB	0.8VDD	–	VDD	V	
	V <sub>IH2</sub>	All input pins except V <sub>IH1</sub>	0.7VDD	–	VDD	V	
	V <sub>IH3</sub>	P20, P33, P34, P37; 3V Interface mode	2.4	–	VDD	V	
Input Low Voltage	V <sub>IL1</sub>	P0~P6, RESETB	–	–	0.2VDD	V	
	V <sub>IL2</sub>	All input pins except V <sub>IL1</sub>	–	–	0.3VDD	V	
Output High Voltage	V <sub>OH</sub>	VDD= 4.5V, I <sub>OH</sub> = -2mA, All output ports;	VDD-1.0	–	–	V	
Output Low Voltage	V <sub>OL1</sub>	VDD=4.5V, I <sub>OL1</sub> = 10mA; All output ports except V <sub>OL2</sub>	–	–	1.0	V	
	V <sub>OL2</sub>	VDD= 4.5V, I <sub>OL2</sub> = 15mA ; P10~P13, P23~P24, P4	–	–	1.0	V	
Output High Current	I <sub>OH</sub>	VDD=4.5V, V <sub>OH</sub> = 3.5V; All output ports	-2	–	–	mA	
Output Low Current	I <sub>OL1</sub>	VDD=4.5V, V <sub>OL</sub> = 1.0V; All output ports except I <sub>OL2</sub>	10	–	–	mA	
	I <sub>OL2</sub>	VDD=4.5V, V <sub>OL</sub> = 1.0V; P10~P13, P23~P24, P4	15	–	–	mA	
Input High Leakage Current	I <sub>IH</sub>	All input ports	–	–	1	μA	
Input Low Leakage Current	I <sub>IL</sub>	All input ports	-1	–	–	μA	
Pull-Up Resistor	R <sub>PU1</sub>	V <sub>I</sub> =0V, T <sub>A</sub> = 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R <sub>PU2</sub>	V <sub>I</sub> =0V, T <sub>A</sub> = 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
OSC feedback resistor	R <sub>X1</sub>	XIN= VDD, XOUT= VSS T <sub>A</sub> = 25°C, VDD= 5V	600	1200	2000	kΩ	
	R <sub>X2</sub>	SXIN=VDD, SXOUT=VSS T <sub>A</sub> = 25 °C ,VDD=5V	2500	5000	10000		

**Table 7-10 DC Characteristics (Continued)**

 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f<sub>XIN</sub>= 12MHz)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	
Supply Current	I <sub>DD1</sub> (RUN)	f <sub>XIN</sub> = 12MHz, VDD= 5V±10%	–	2.5	5.0	mA	
		f <sub>XIN</sub> = 10MHz, VDD= 3V±10%	–	1.6	3.2		
		f <sub>IRC</sub> = 8MHz, VDD= 5V±10%	–	1.3	2.6		
		f <sub>XIN</sub> = 4MHz, VDD= 3V±10%	–	0.9	1.8		
	I <sub>DD2</sub> (IDLE)	f <sub>XIN</sub> = 12MHz, VDD= 5V±10%	–	1.2	2.4	mA	
		f <sub>XIN</sub> = 10MHz, VDD= 3V±10%	–	0.7	1.4		
		f <sub>IRC</sub> = 8MHz, VDD= 5V±10%	–	0.6	1.2		
		f <sub>XIN</sub> = 4MHz, VDD= 3V±10%	–	0.4	0.8		
	I <sub>DD3</sub>	f <sub>XIN</sub> = 32.768kHz VDD= 3V±10%	Sub RUN	–	45.0	90.0	μA
	I <sub>DD4</sub>	T <sub>A</sub> = 25°C PSAVE=1	Sub IDLE	–	3.5	7.0	μA
I <sub>DD5</sub>	STOP, VDD= 5V±10%, T <sub>A</sub> = 25°C		–	0.5	3.0	μA	

NOTES) 1. Where the f<sub>XIN</sub> is an external main oscillator, the f<sub>SUB</sub> is an external sub oscillator, the f<sub>IRC</sub> is an internal RC oscillator, the f<sub>PLL</sub> is the output frequency of the PLL (phase locked-loop), and the f<sub>x</sub> is the selected system clock.

2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.

3. All supply current items include the current of the power-on reset (POR) block.

### 7.11 AC Characteristics

Table 7-11 AC Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	$t_{RST}$	Input, $V_{DD} = 5\text{V}$	10	–	–	$\mu\text{s}$
Interrupt input high, low width	$t_{IWH}$ , $t_{IWL}$	All interrupt, $V_{DD} = 5\text{V}$	200	–	–	ns
External Counter Input High, Low Pulse Width	$t_{ECWH}$ , $t_{ECWL}$	$EC_n$ , $V_{DD} = 5\text{V}$ ( $n = 0, 1, 2, 3, 4, 5, 6, 7$ )	200	–	–	
External Counter Transition Time	$t_{REC}$ , $t_{FEC}$	$EC_n$ , $V_{DD} = 5\text{V}$ ( $n = 0, 1, 2, 3, 4, 5, 6, 7$ )	20	–	–	

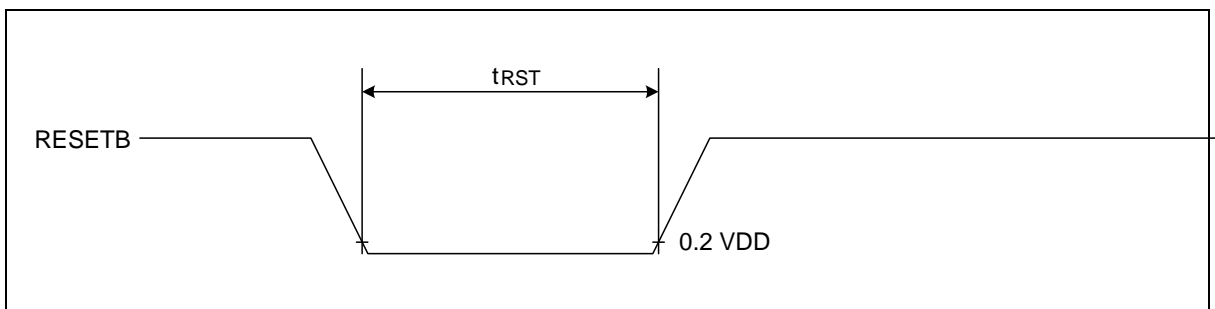


Figure 7.2 Input Timing for RESETB

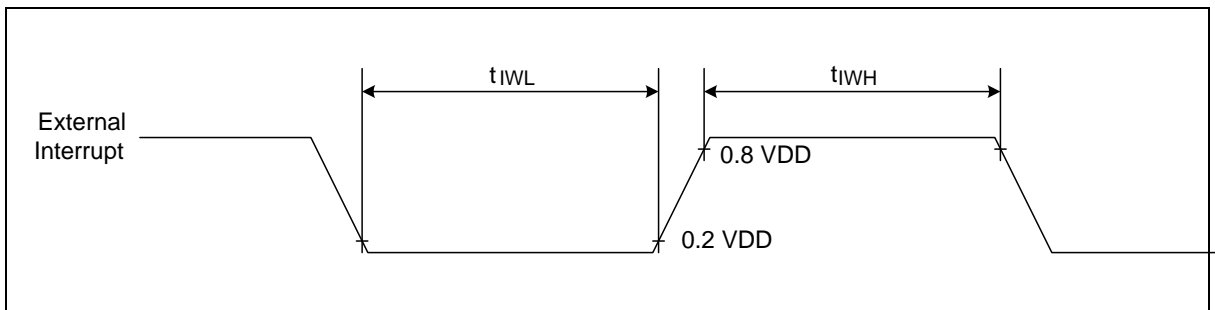


Figure 7.3 Input Timing for External Interrupts

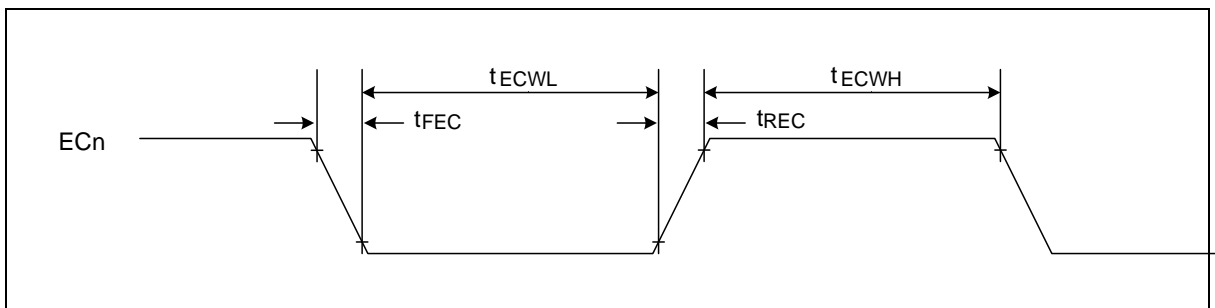


Figure 7.4 Input Timing for EC0, EC1, EC2, EC3, EC4, EC5, EC6, EC7

7.12 SPI Characteristics

Table 7-12 SPI Characteristics

(T<sub>A</sub>= -40°C – +85°C, VDD= 1.8V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t <sub>SCK</sub>	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t <sub>SCKH</sub> , t <sub>SCKL</sub>	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t <sub>FOD</sub>	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t <sub>DS</sub>	–	–	–	50	
Input Setup Time	t <sub>DIS</sub>	–	100	–	–	
Input Hold Time	t <sub>DIH</sub>	–	150	–	–	

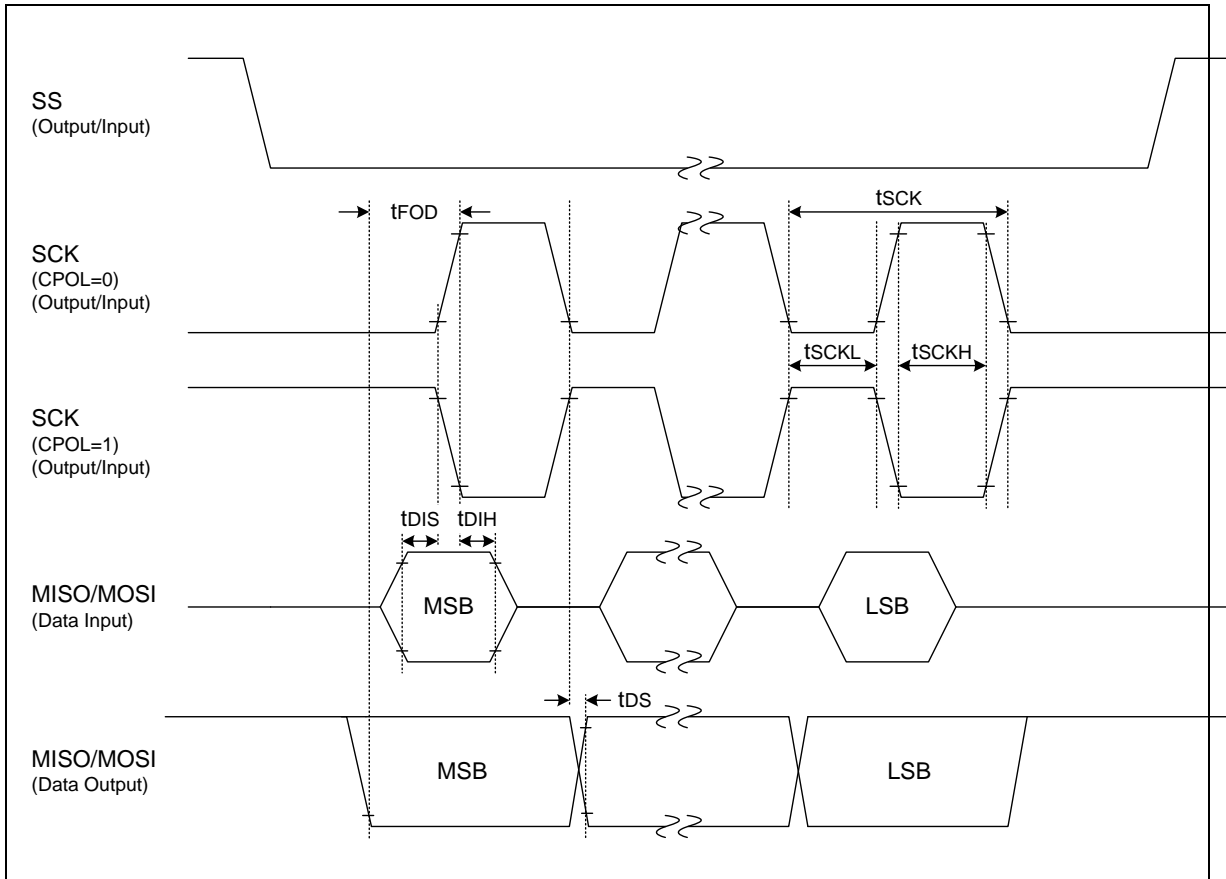


Figure 7.5 SPI Timing

### 7.13 UART Characteristics

Table 7-13 UART Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ ,  $f_{XIN} = 11.1\text{MHz}$ )

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	$t_{SCK}$	1250	$t_{CPU} \times 16$	1650	ns
Output data setup to clock rising edge	$t_{S1}$	590	$t_{CPU} \times 13$	—	ns
Clock rising edge to input data valid	$t_{S2}$	—	—	590	ns
Output data hold after clock rising edge	$t_{H1}$	$t_{CPU} - 50$	$t_{CPU}$	—	ns
Input data hold after clock rising edge	$t_{H2}$	0	—	—	ns
Serial port clock High, Low level width	$t_{HIGH}, t_{LOW}$	470	$t_{CPU} \times 8$	970	ns

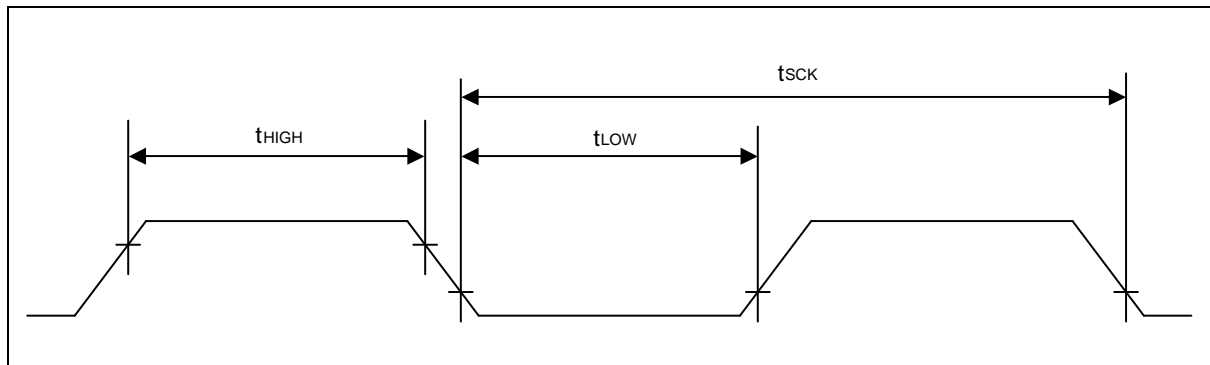


Figure 7.6 Waveform for UART Timing Characteristics

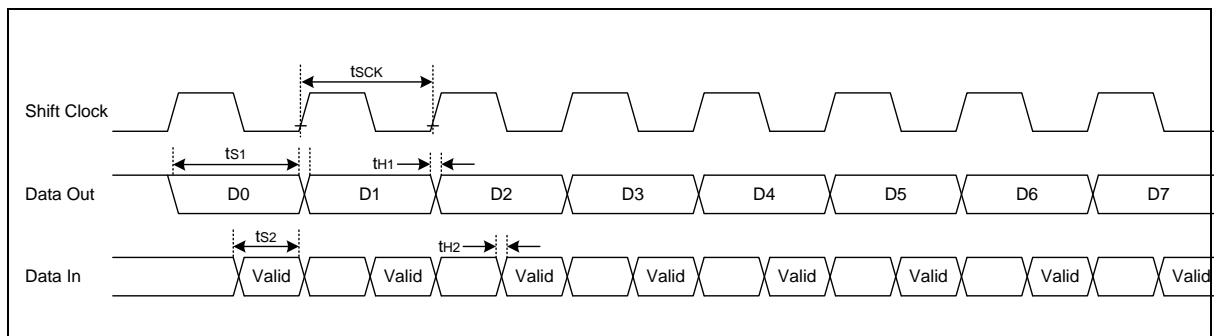


Figure 7.7 Timing Waveform for the UART Module



7.14 I2C Characteristics

Table 7-14 I2C Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit	
		MIN	MAX	MIN	MAX		
Clock frequency	$t_{SCL}$	0	100	0	400	$\mu\text{s}$	
Clock High Pulse Width	$t_{SCLH}$	4.0	–	0.6	–		
Clock Low Pulse Width	$t_{SCLL}$	4.7	–	1.3	–		
Bus Free Time	$t_{BF}$	4.7	–	1.3	–		
Start Condition Setup Time	$t_{STSU}$	4.7	–	0.6	–		
Start Condition Hold Time	$t_{STHD}$	4.0	–	0.6	–		
Stop Condition Setup Time	$t_{SPSU}$	4.0	–	0.6	–		
Stop Condition Hold Time	$t_{SPHD}$	4.0	–	0.6	–		
Output Valid from Clock	$t_{VD}$	0	–	0	–		
Data Input Hold Time	$t_{DIH}$	0	–	0	1.0		
Data Input Setup Time	$t_{DIS}$	250	–	100	–		
							ns

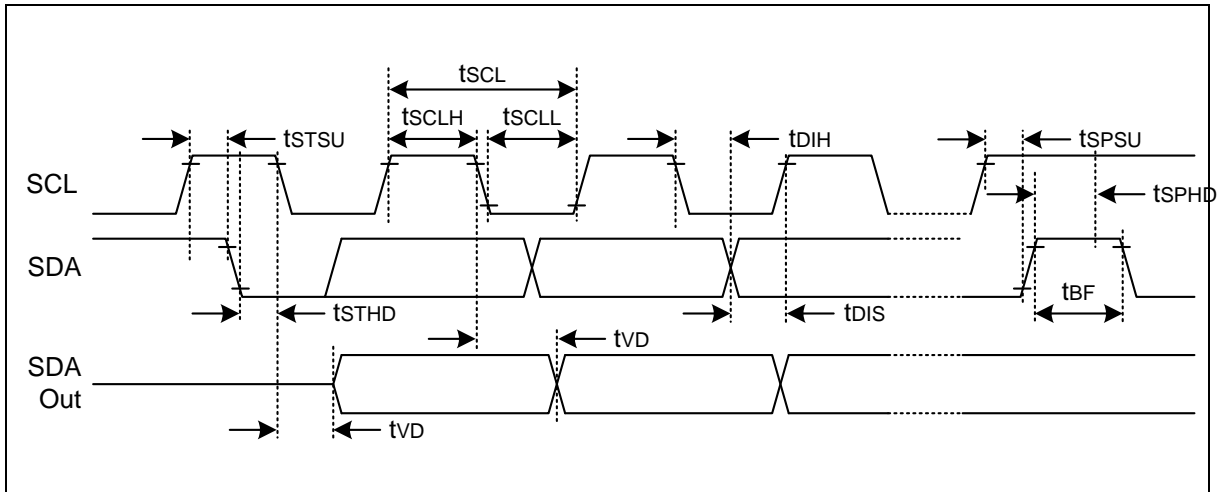


Figure 7.8 I2C Timing

### 7.15 Data Retention Voltage in Stop Mode

Table 7-15 Data Retention Voltage in Stop Mode

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	$V_{DDDR}$	–	1.0	–	5.5	V
Data retention supply current	$I_{DDDR}$	$V_{DDDR} = 1.0\text{V}$ , ( $T_A = 25^{\circ}\text{C}$ ), Stop mode	–	–	1	$\mu\text{A}$

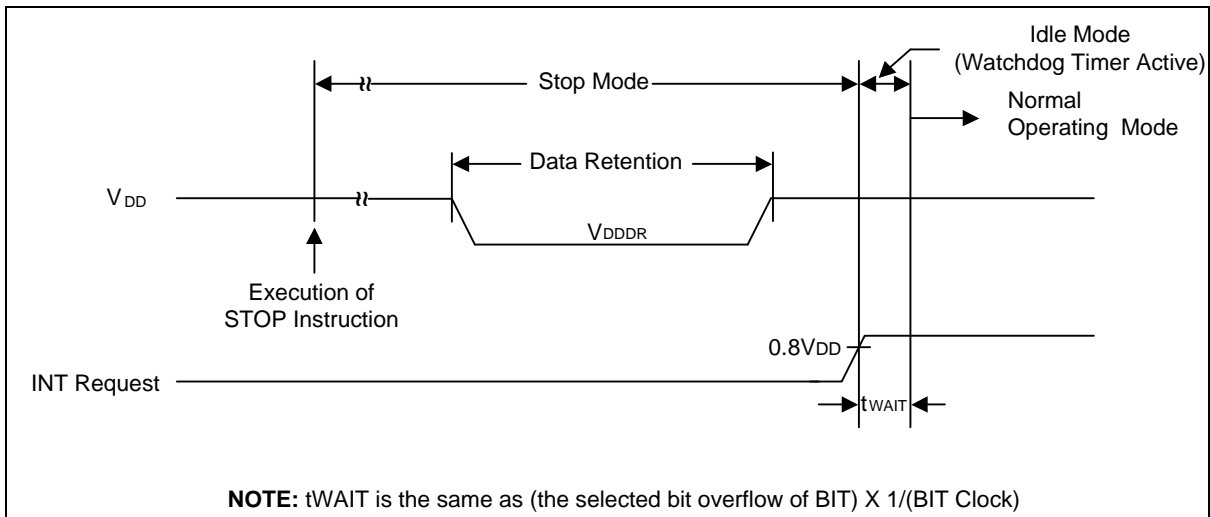


Figure 7.9 Stop Mode Release Timing when Initiated by an Interrupt

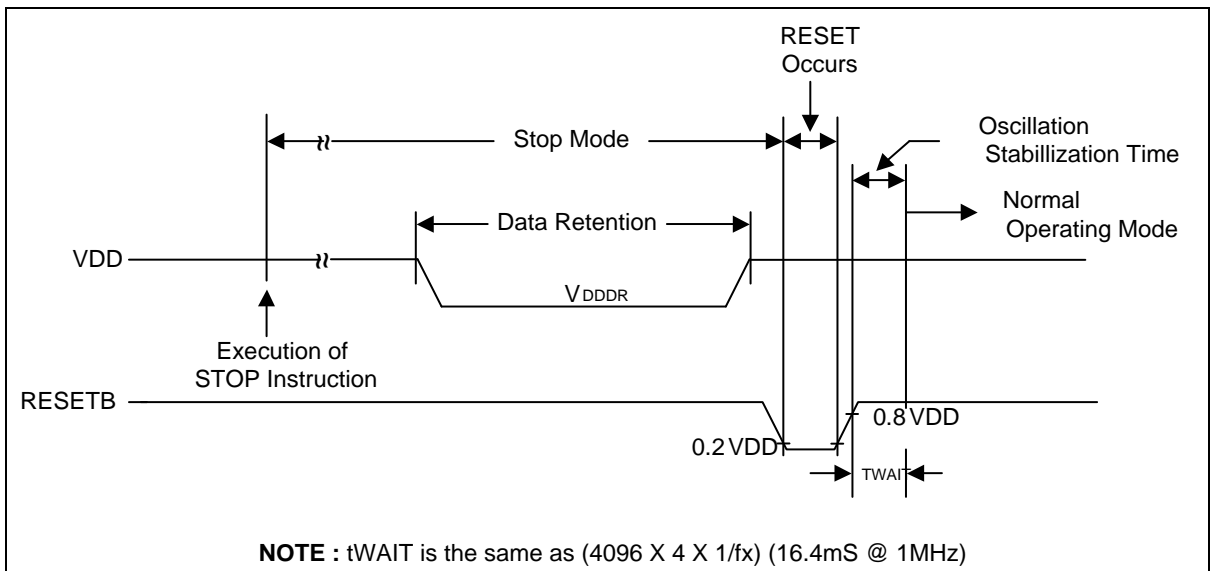


Figure 7.10 Stop Mode Release Timing when Initiated by RESETB

## 7.16 Internal Flash Rom Characteristics

**Table 7-16 Internal Flash Rom Characteristics**

 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t <sub>FSW</sub>	–	–	2.5	2.7	ms
Sector Erase Time	t <sub>FSE</sub>	–	–	3.0	3.3	
Code Write Protection Time	t <sub>FHL</sub>	–	–	2.5	2.7	
Page Buffer Reset Time	t <sub>FBR</sub>	–	–	–	5	μs
Flash Programming Voltage	V <sub>PGM</sub>	–	2.0	–	5.5	
Flash Programming Frequency	f <sub>PGM</sub>	–	0.4	–	–	MHz
Endurance of Write/Erase (Sector 0~1019)	NF <sub>WE</sub>	25°C	–	–	10,000	Times
Endurance of Write/Erase (Sector 1020~1023)					100,000	Times
Flash Data Retention Time	t <sub>RT</sub>	–	10	–	–	Years

NOTE) During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

## 7.17 Input/Output Capacitance

**Table 7-17 Input/Output Capacitance**

 (T<sub>A</sub>= -40°C ~ +85°C, VDD= 0V)

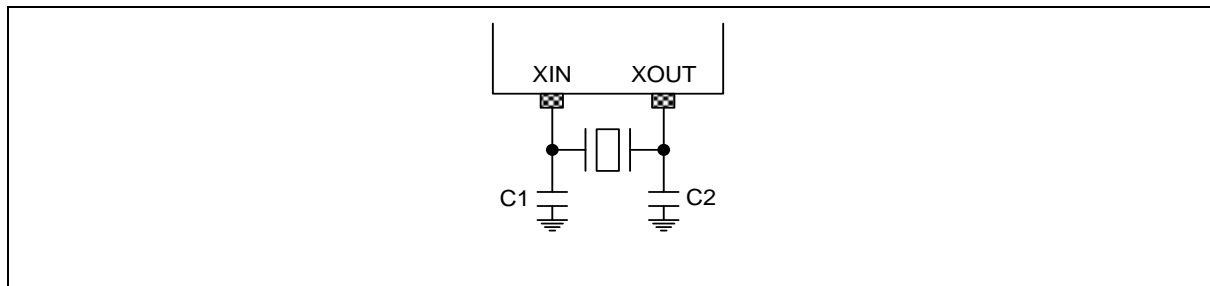
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C <sub>IN</sub>	f <sub>X</sub> = 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C <sub>OUT</sub>					
I/O Capacitance	C <sub>IO</sub>					

### 7.18 Main Clock Oscillator Characteristics

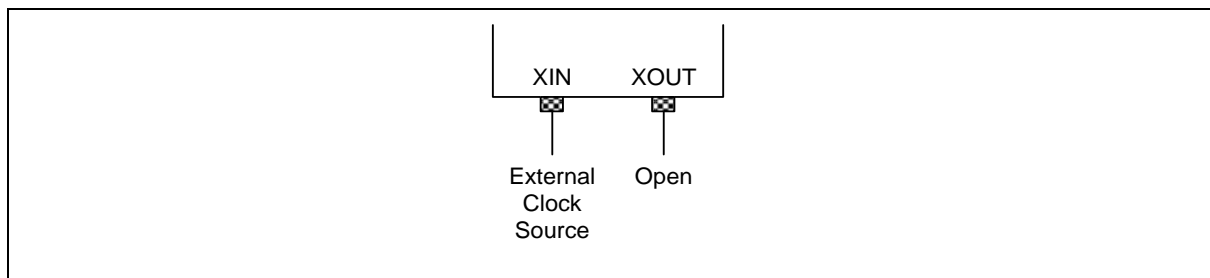
**Table 7-18 Main Clock Oscillator Characteristics**

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
External Clock	XIN input frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	



**Figure 7.11 Crystal/Ceramic Oscillator**



**Figure 7.12 External Clock**

### 7.19 Sub Clock Oscillator Characteristics

Table 7-19 Sub Clock Oscillator Characteristics

(T<sub>A</sub>= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

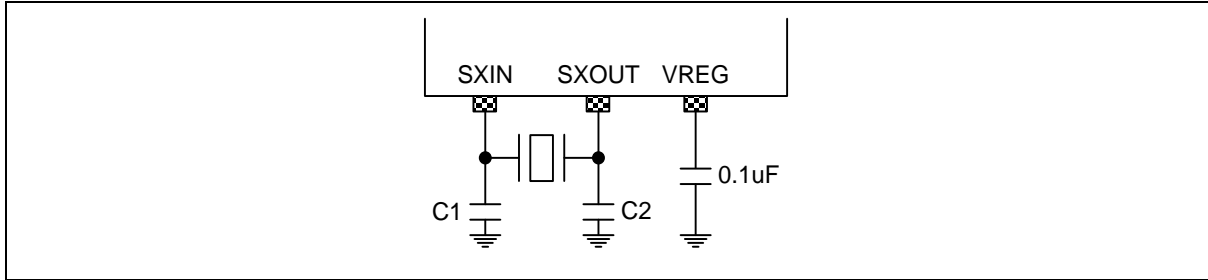


Figure 7.13 Crystal Oscillator

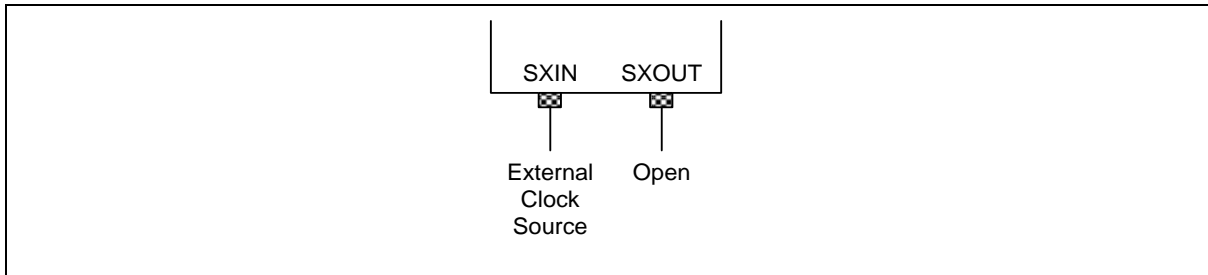


Figure 7.14 External Clock

### 7.20 Main Oscillation Stabilization Characteristics

Table 7-20 Main Oscillation Stabilization Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	$f_x > 1\text{MHz}$ Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	$f_{XIN} = 0.4 \text{ to } 12\text{MHz}$ XIN input high and low width ( $t_{XH}$ , $t_{XL}$ )	31	–	1250	ns

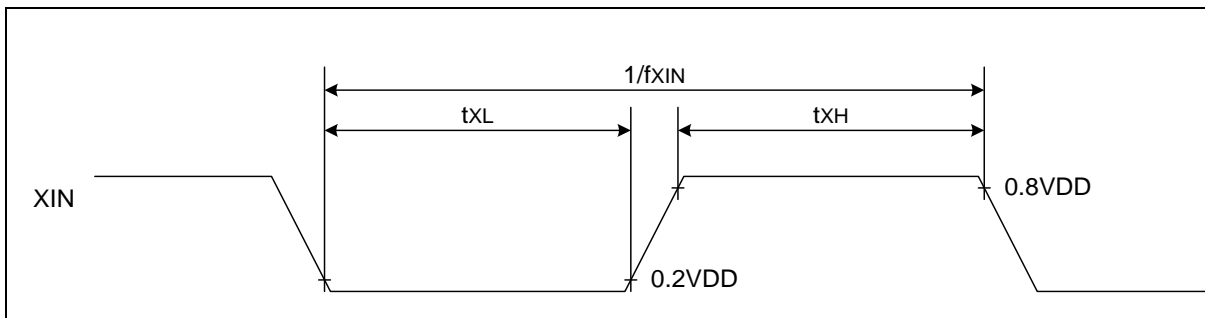


Figure 7.15 Clock Timing Measurement at XIN

### 7.21 Sub Oscillation Characteristics

Table 7-21 Sub Oscillation Stabilization Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width ( $t_{XH}$ , $t_{XL}$ )	5	–	15	$\mu\text{s}$

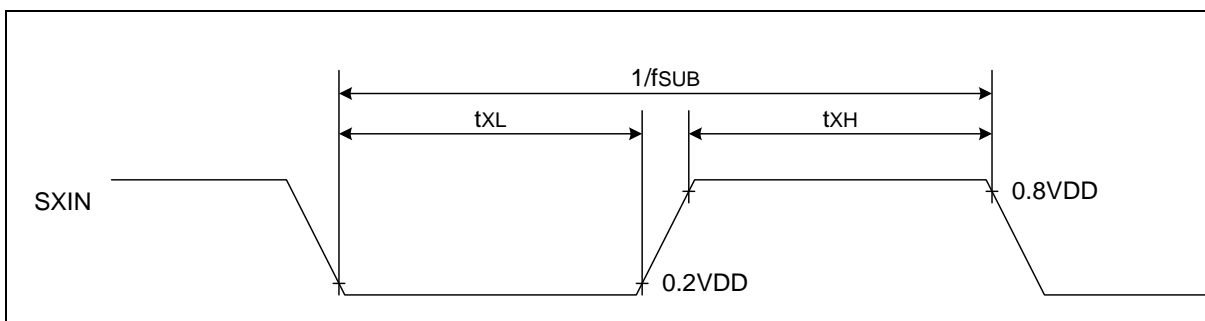


Figure 7.16 Clock Timing Measurement at SXIN

7.22 Operating Voltage Range

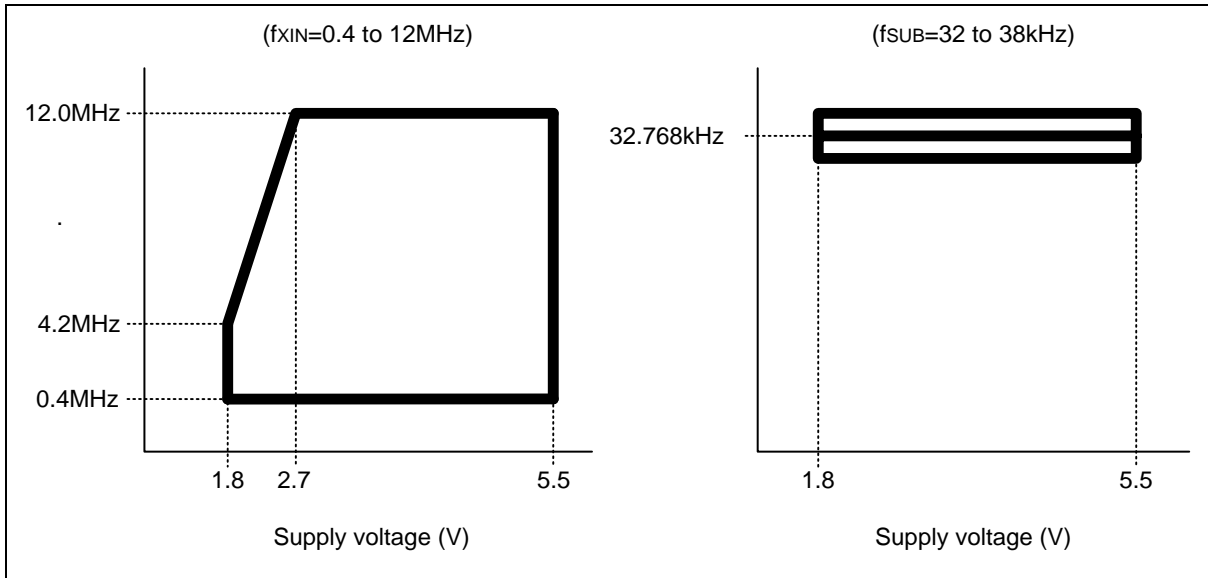


Figure 7.17 Operating Voltage Range

### 7.23 Recommended Circuit and Layout

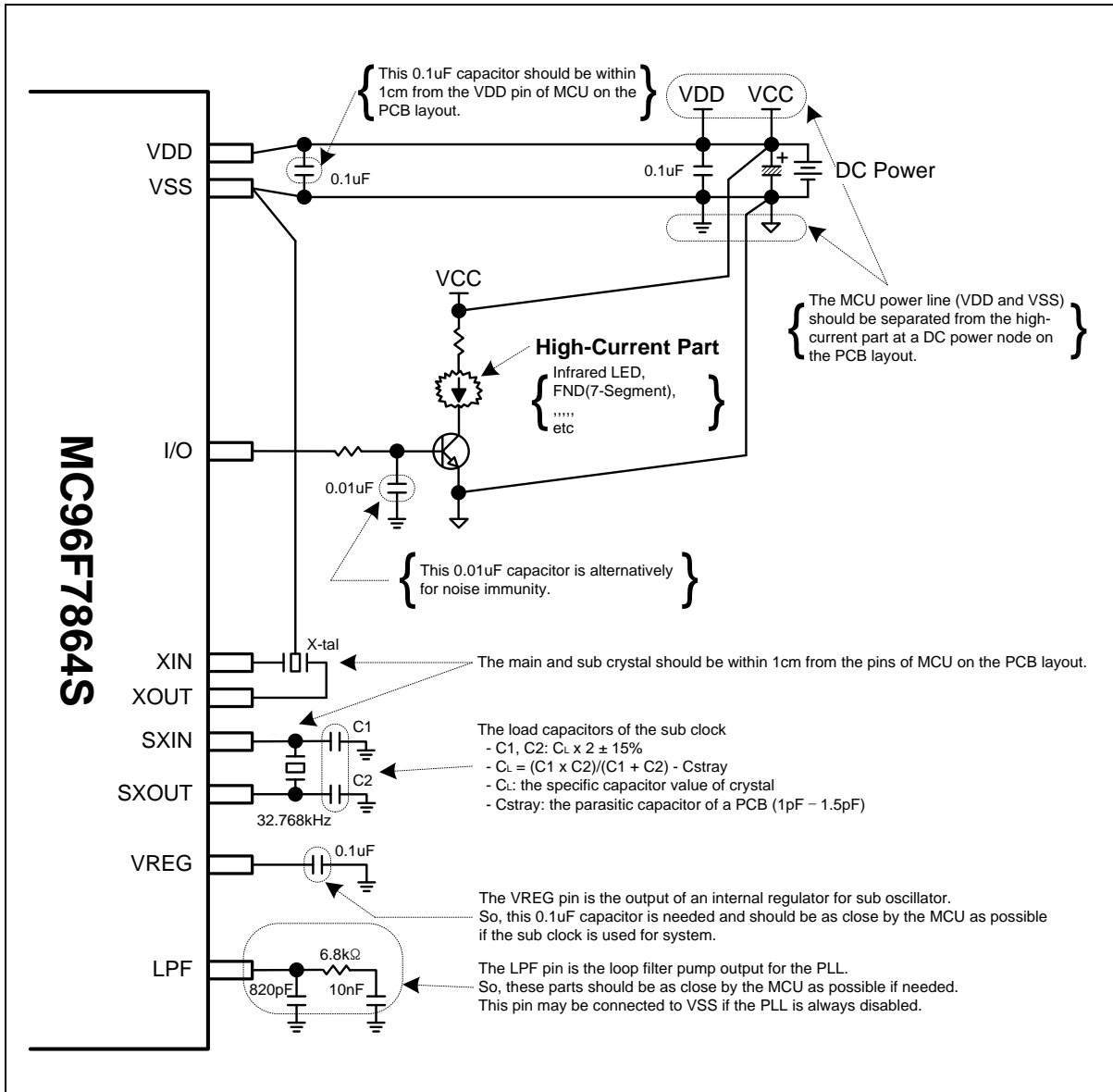


Figure 7.18 Recommended Circuit and Layout



7.24 Recommended Circuit and Layout with SMPS Power

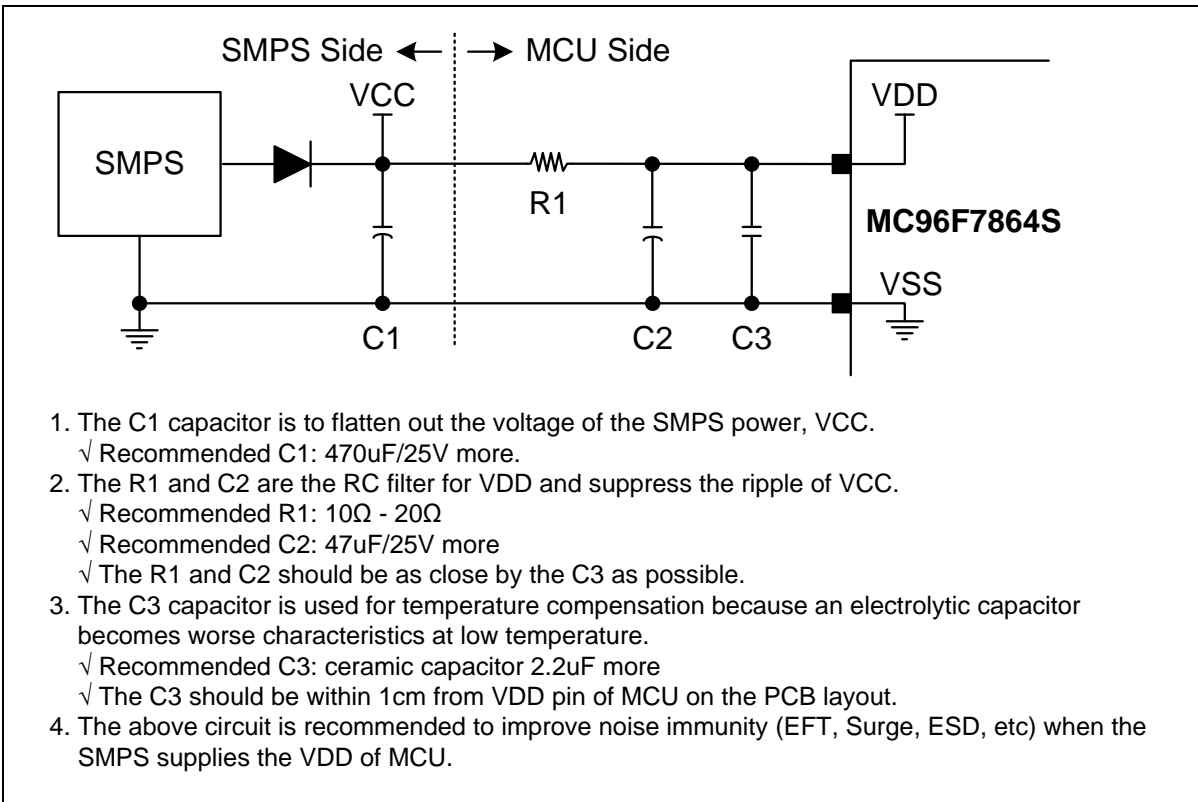


Figure 7.19 Recommended Circuit and Layout with SMPS Power

### 7.25 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

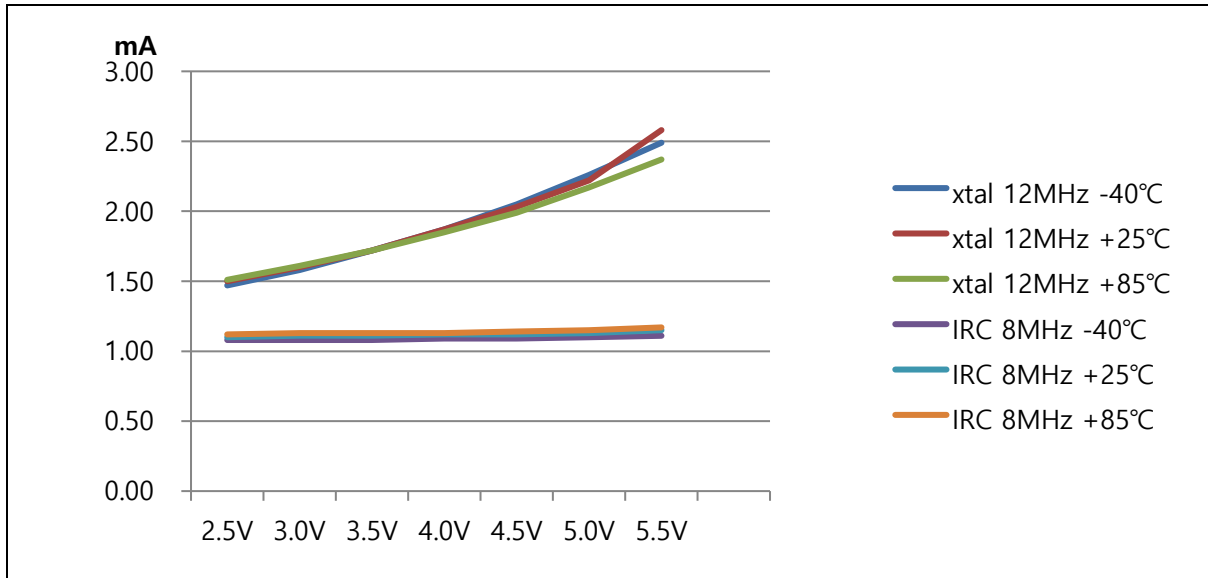


Figure 7.20 RUN (IDD1 ) Current

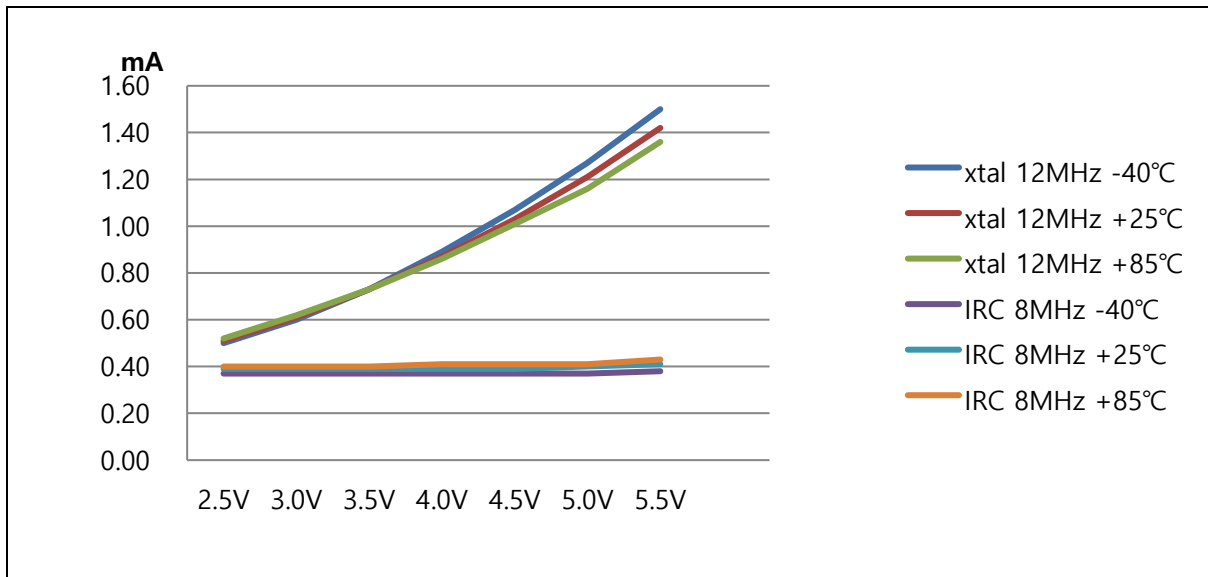


Figure 7.21 IDLE (IDD2) Current

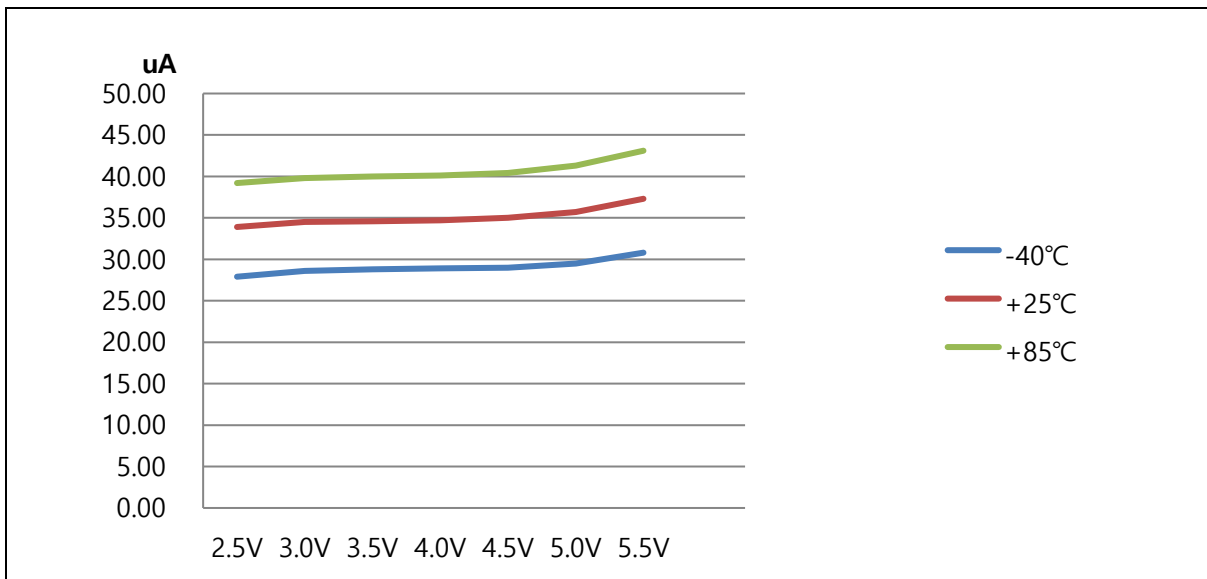


Figure 7.22 SUB RUN (IDD3) Current

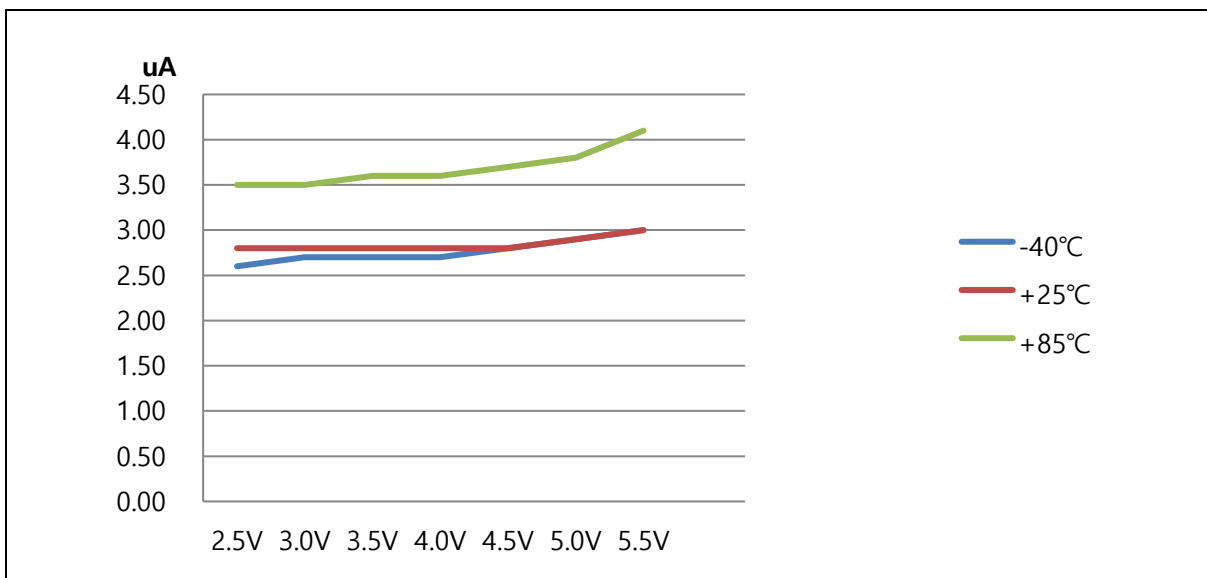


Figure 7.23 SUB IDLE (IDD4) Current

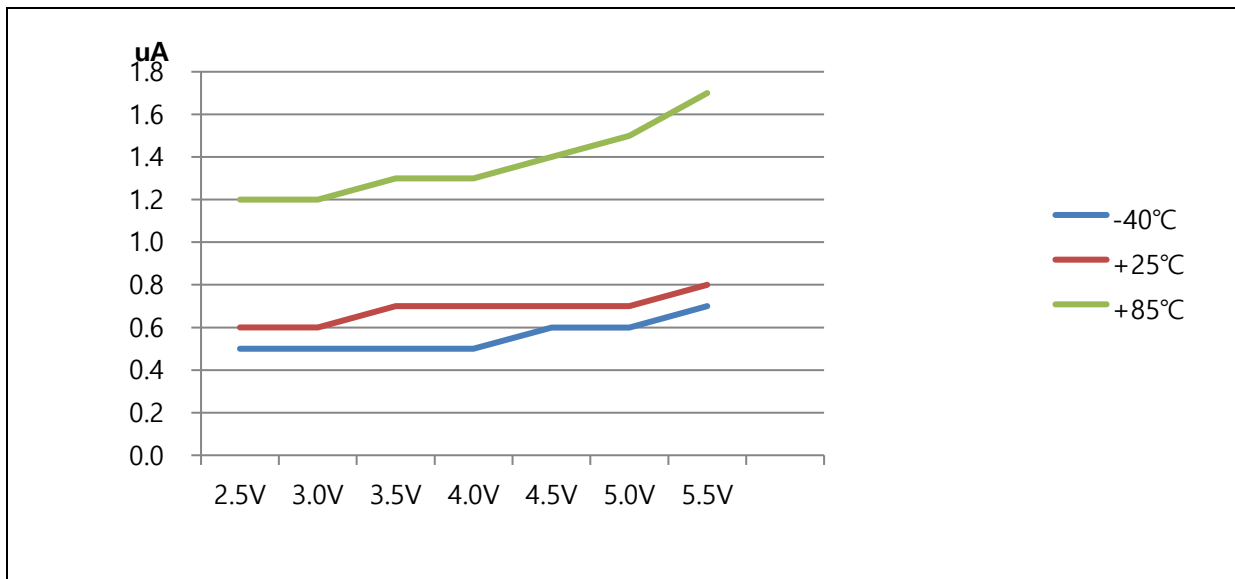


Figure 7.24 STOP (IDD5) Current